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Evaluation Board User Guide
UG-232

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the AD6642/AD6657 Analog-to-Digital Converters

FEATURES

Full featured evaluation board for the AD6642/AD6657
SPI interface for setup and control
External, on-board oscillator or AD9517 clocking options
Balun/transformer or amplifier input drive options
LDO regulator power supply
VisualAnalog® and SPI controller software interfaces

EQUIPMENT NEEDED

Analog signal source and antialiasing filter
Sample clock source (if not using the on-board oscillator)
2 switching power supplies (6.0 V, 2.5 A), CUI, Inc. EPS060250UH-PHP-SZ, provided
PC running Windows® 98 (2nd ed.), Windows 2000, Windows ME, or Windows XP
USB 2.0 port, recommended (USB 1.1 compatible)
AD6642 or AD6657 evaluation board
HSC-ADC-EVALCZ FPGA-based data capture kit

SOFTWARE NEEDED

VisualAnalog
SPI controller

DOCUMENTS NEEDED

AD6642 or AD6657 data sheet
HSC-ADC-EVALCZ data sheet
AN-905 Application Note, *VisualAnalog Converter Evaluation Tool, Version 1.0 User Manual*
AN-878 Application Note, *High Speed ADC SPI Control Software*
AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*
AN-835 Application Note, *Understanding ADC Testing and Evaluation*

GENERAL DESCRIPTION

This document describes the AD6642 and AD6657 evaluation board, which provides all of the support circuitry required to operate the AD6642 or AD6657 in their various modes and configurations. The application software used to interface with the devices is also described.

The AD6642 and AD6657 data sheets provide additional information and should be consulted when using the evaluation board. All documents and software tools are available at www.analog.com/fifo. For additional information or questions, send an email to highspeed.converters@analog.com.

TYPICAL MEASUREMENT SETUP

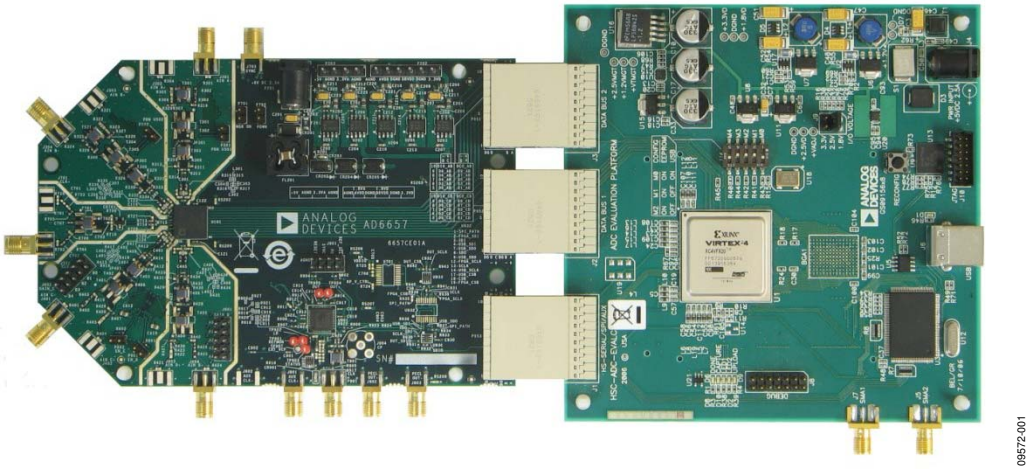

Figure 1. AD6642 and AD6657 Evaluation Board and HSC-ADC-EVALCZ Data Capture Board

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REVISION HISTORY

12/10—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The AD6642 and AD6657 evaluation board provides all of the support circuitry required to operate these parts in their various modes and configurations. Figure 2 shows the typical bench characterization setup used to evaluate the ac performance of the AD6642 or AD6657. It is critical that the signal sources used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the optimum performance of the signal chain. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is necessary to achieve the specified noise performance.

The AD6642 and AD6657 evaluation board covers two general part families. The boards are populated slightly differently for each family. The AD6642 is one part supported by this evaluation board, and the AD6657 is the second part supported by this evaluation board. The evaluation board supports quad-channel operation for the AD6657 while supporting dual-channel operation for the AD6642.

See the Evaluation Board Software Quick Start Procedures section to get started, and see Figure 20 to Figure 36 for the complete schematics and layout diagrams. These diagrams demonstrate the routing and grounding techniques that should be applied at the system level when designing application boards using these converters.

POWER SUPPLIES

This evaluation board comes with a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. Connect the supply to the rated 100 V ac to the 240 V ac wall outlet at 47 Hz to 63 Hz. The output from the supply is provided through a 2.1 mm inner diameter jack that connects to the printed circuit board (PCB) at P201. The 6 V supply is fused and conditioned on the PCB before connecting to the low dropout linear regulators (default configuration) that supply the proper bias to each of the various sections on the board.

The evaluation board can be powered in a nondefault condition using external bench power supplies. To do this, the E201, E202, E204, E205, and E207 ferrite beads can be removed to disconnect the outputs from the on-board LDOs. This enables the user to bias each section of the board individually. Use P202 and P203 to connect a different supply for each section. A 1.8 V supply is needed with a 1 A current capability for DUT_AVDD and DRVDD; however, it is recommended that separate supplies be used for both analog and digital domains. An additional supply is also required to supply 1.8 V for digital support circuitry on the board, DVDD. This should also have a 1 A current capability and can be combined with DRVDD with little or no degradation in performance. To operate the evaluation board using the SPI and alternate clock options, a separate 3.3 V analog supply is needed in addition to the other supplies. This 3.3 V supply, or 3P3V_ANALOG, should have a 1 A current capability. This 3.3 V supply is also used to support optional input path amplifiers (ADL5562) on Channel A and Channel B. An additional supply, 5V_SUPPORT, is used to bias the optional dual input path amplifier (AD8376) on Channel C and Channel D. If used, these supplies should each have 1 A current capability.

INPUT SIGNALS

When connecting the clock and analog source, use clean signal generators with low phase noise, such as the Rohde & Schwarz SMA, or HP 8644B signal generators or an equivalent. Use a 1 m shielded, RG-58, 50 Ω coaxial cable for connecting to the evaluation board. Enter the desired frequency and amplitude (see the Specifications section in the data sheet of the respective part). When connecting the analog input source, use of a multipole, narrow-band band-pass filter with 50 Ω terminations is recommended. Analog Devices, Inc., uses TTE and K&L Microwave, Inc., band-pass filters. The filters should be connected directly to the evaluation board.

If an external clock source is used, it should also be supplied with a clean signal generator as previously specified. Typically, most Analog Devices evaluation boards can accept ~2.8 V p-p or 13 dBm sine wave input for the clock.

OUTPUT SIGNALS

The default setup uses the Analog Devices high speed converter evaluation platform (HSC-ADC-EVALCZ) for data capture. The output signals from Channel A/Channel B for the AD6642 and Channel A/Channel B/Channel C/Channel D for the AD6657 are routed through P951 and P952, respectively, to the FPGA on the data capture board.

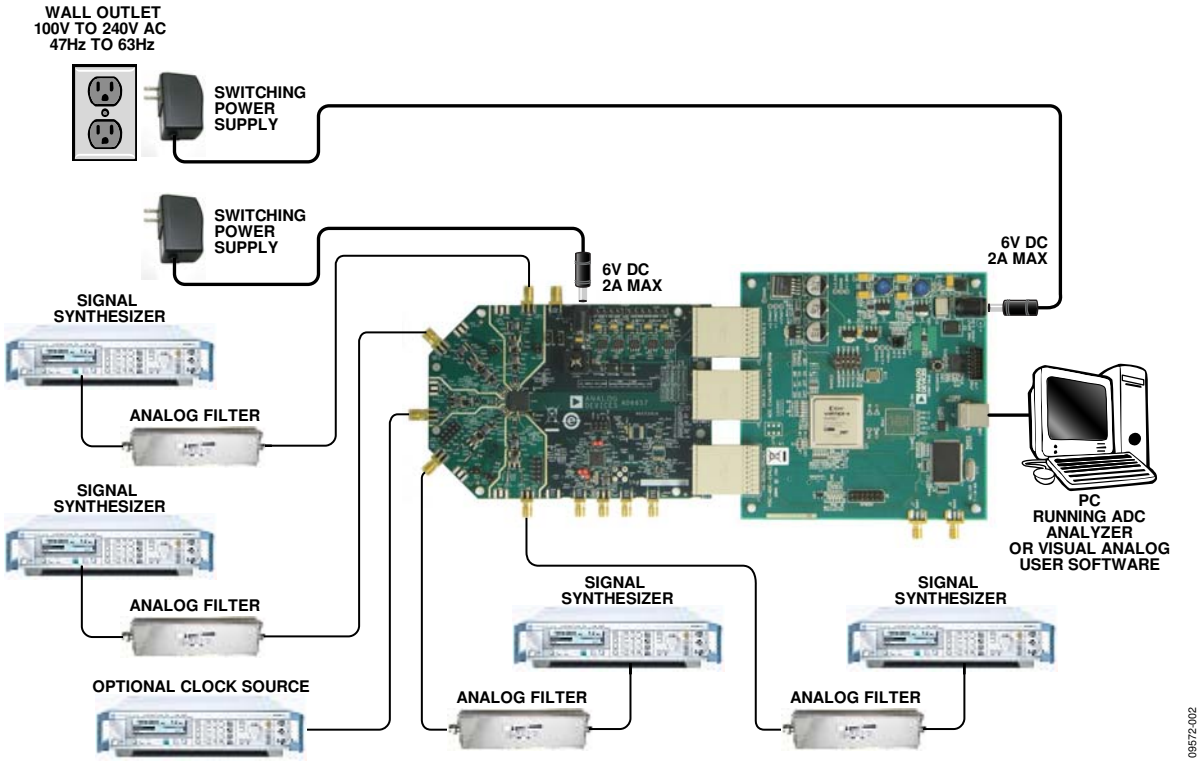

Figure 2. Evaluation Board Connection

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

This section explains the default and optional settings or modes allowed on the AD6642/AD6657 Rev. B evaluation board.

Power Circuitry

Connect the switching power supply that is supplied in the evaluation kit between a rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz and P201.

Analog Input

The A and B channel inputs on the evaluation board are set up for a double balun-coupled analog input with a 50 Ω impedance. This input network is optimized to support a wide frequency band. See the AD6642 and AD6657 data sheets for additional information on the recommended networks for different input frequency ranges. The nominal input drive level is 10 dBm to achieve 2 V p-p full scale into 50 Ω. At higher input frequencies, slightly higher input drive levels are required due to losses in the front-end network.

Optionally, Channel A and Channel B inputs on the board can be configured to use the ADL5562 ultralow distortion RF/IF differential amplifier. The ADL5562 components are included on the evaluation board at U501 and U502. However, the path into and out of the ADL5562 can be configured in many different ways depending on the application; therefore, the parts in the input and output path are left unpopulated. The user should see the ADL5562 data sheet for additional information on this part and for configuring the inputs and outputs. The ADL5562 by default is held in power-down mode but can be enabled by adding a jumper on P501 (Channel A) or P502 (Channel B). The ADL5562, on the Channel A and Channel B inputs, can also be substituted with the ADA4937 or the ADA4938 to allow evaluation of these parts with the ADC.

The Channel C and Channel D inputs are set up with an optional input path through the AD8376 digitally variable gain amplifier (DVGA). Similar to Channel A and Channel B, the amplifier is included on the board at U601; however, the input-/output-related components are not included. The user should see the AD8376 data sheet for additional information on this part and for configuring the inputs and outputs. The AD8376 channels are also normally held in power-down mode and can be enabled by adding a jumper on P602 (Channel C) or P601 (Channel D).

Clock Circuitry

The default clock input circuit that is populated on the AD6642/AD6657 evaluation board uses a simple transformer-coupled circuit using a high bandwidth 1:1 impedance ratio transformer (T701) that adds a very low amount of jitter to the clock path. The clock input is 50 Ω terminated and ac-coupled to handle single-ended sine wave types of inputs. The transformer converts the single-ended input to a differential signal that is clipped by CR701 before entering the ADC clock inputs.

The board is set by default to use an external clock generator. An external clock source capable of driving a 50 Ω terminated input should be connected to J702.

A differential LVPECL clock driver output can also be used to clock the ADC input using the AD9517 (U901). To place the AD9517 into the clock path, populate R727 and R728 with 0 Ω resistors and remove R713 and R714 to disconnect the default clock path inputs. In addition, populate R817 and R816 with 0 Ω resistors and remove R815 and R818 to disconnect the default clock path outputs and insert the AD9517 LVPECL Output 1. The AD9517 must be configured through the SPI controller software to set up the PLL and other operation modes. Consult the AD9517 data sheet for more information about these and other options.

PDWN

To enable the power-down feature, add a shorting jumper across P702 at Pin 1 and Pin 2 to connect the PDWN pin to AVDD.

NSR

To enable the noise shaping requantizer (NSR) feature, add a shorting jumper across P701 at Pin 1 and Pin 2 to connect the NSR ON pin to GND. The NSR feature can also be enabled via the SPI interface by writing to Register 0x3C. Writing to Bit 4 allows the user to ignore the MODE pin and enable the NSR via SPI control.

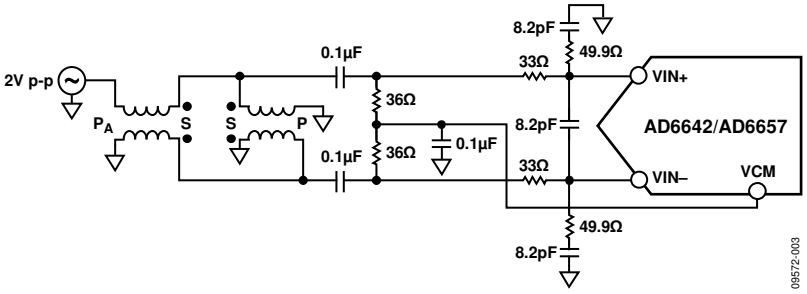

Figure 3. Default Analog Input Configuration of the AD6642/AD6657

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

This section provides quick start procedures for using the AD6642/AD6657 evaluation board. Both the default and optional settings are described.

CONFIGURING THE BOARD

Before using the software for testing, configure the evaluation board as follows:

1. Connect the evaluation board to the data capture board, as shown in Figure 1 and Figure 2.
2. Connect one 6 V, 2.5 A switching power supply (such as the CUI EPS060250UH-PHP-SZ supplied) to the AD6642/AD6657 board.
3. Connect one 6 V, 2.5 A switching power supply (such as the CUI EPS060250UH-PHP-SZ supplied) to the HSC-ADC-EVALCZ board.
4. Connect the HSC-ADC-EVALCZ board (J6) to the PC with a USB cable.
5. On the ADC evaluation board, confirm that there are no jumpers installed on any of the header pins.
6. Connect a low jitter sample clock to the connector J702.
7. When using the AD6642 version of the ADC evaluation board, use a clean signal generator with low phase noise to provide an input signal to the desired A and/or B channel(s). If using the AD6657 version of the ADC evaluation board, use a clean signal generator with low phase noise to provide an input signal to the desired A, B, C, and/or D channel(s). Use a 1 m, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator. For best results, use a narrow-band band-pass filter with 50 Ω terminations and an appropriate center frequency. (Analog Devices uses TTE, Allen Avionics, and K&L band-pass filters.)

USING THE SOFTWARE FOR TESTING

Setting Up the ADC Data Capture

After configuring the board, set up ADC data capture using the following steps:

1. Open VisualAnalog on the connected PC. The appropriate part type should be listed in the status bar of the **VisualAnalog – New Canvas** window. Select the template that corresponds to the type of testing to be performed (see Figure 4 where the AD6657 is shown as an example).

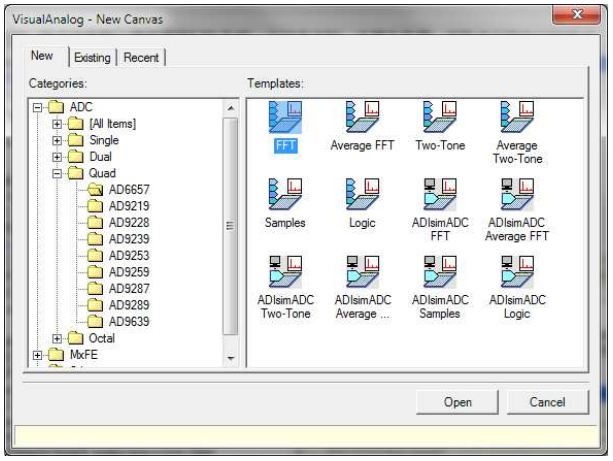

Figure 4. VisualAnalog - New Canvas Window

2. After the template is selected, a message appears asking if the default configuration can be used to program the FPGA (see Figure 5). Click **Yes**, and the window closes.

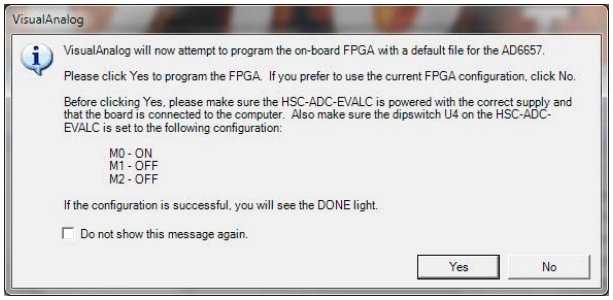

Figure 5. VisualAnalog Default Configuration Message

3. To change features to settings other than the default settings, click the **Expand Display** button, located on the bottom right corner of the window shown in Figure 6 to see what is shown in Figure 7.

   Detailed instructions for changing the features and capture settings can be found in the AN-905 Application Note, *VisualAnalog Converter Evaluation Tool Version 1.0 User Manual*. After the changes are made to the capture settings, click **Collapse Display** (see Figure 7).

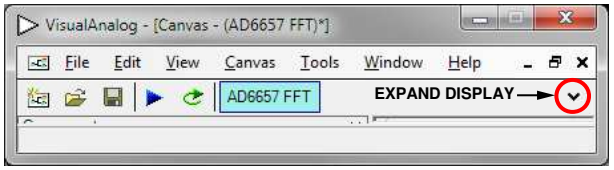

Figure 6. VisualAnalog – [Canvas – (AD6657 FFT)] Window Toolbar, Collapsed Display*

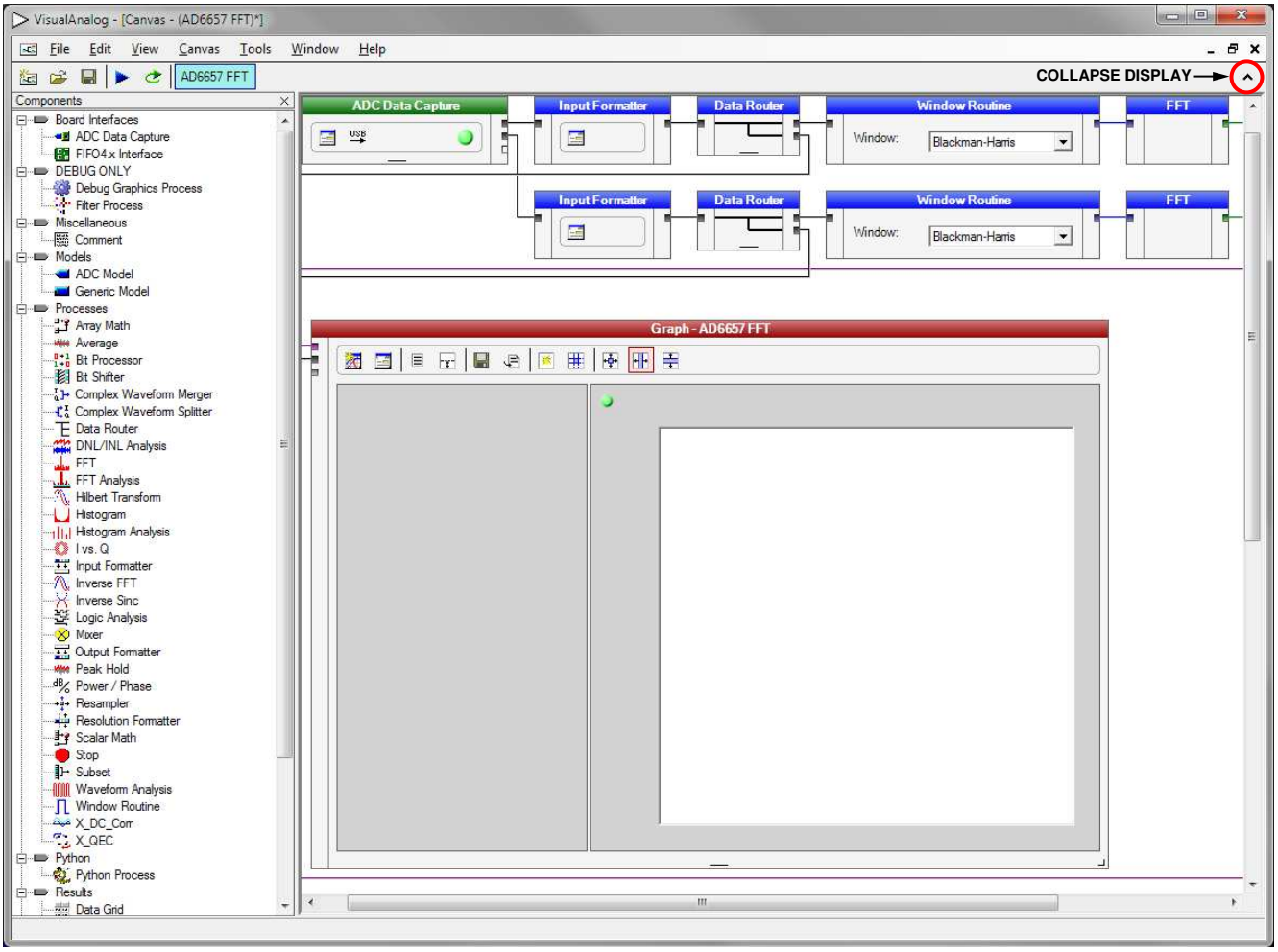

Figure 7. VisualAnalog – [Canvas – (AD6657 FFT)], Main Window*

Setting Up the SPI Controller Software

After the ADC data capture board setup is complete, set up the **SPIController** software using the following procedure:

1. Open the SPI controller software by going to the **Start** menu or by double-clicking the **SPIController** software desktop icon. If prompted for a configuration file, select the appropriate one. If not, check the title bar of the window to determine which configuration is loaded. If necessary, choose **Cfg Open** from the **File** menu and select the appropriate file based on your part type. Note that the **CHIP ID(1)** field should be filled to indicate whether the correct SPI controller configuration file is loaded (see Figure 8).

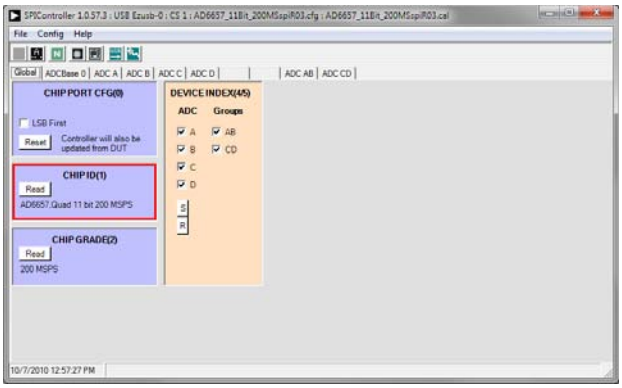

Figure 8. SPIController, CHIP ID(1) Box

2. Click the **New DUT** button in the **SPIController** window (see Figure 9).

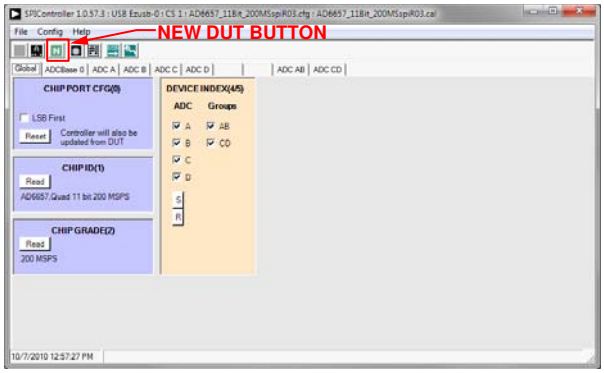

Figure 9. SPIController, New DUT Button

3. In the **ADCBase 0** tab of the **SPIController** window, find the **CLK DIV(B)** box (see Figure 10). If using the clock divider, use the drop-down box to select the correct clock divide ratio, if necessary. See the appropriate part data sheet; the AN-878 Application Note, *High Speed ADC SPI Control Software*; and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information.

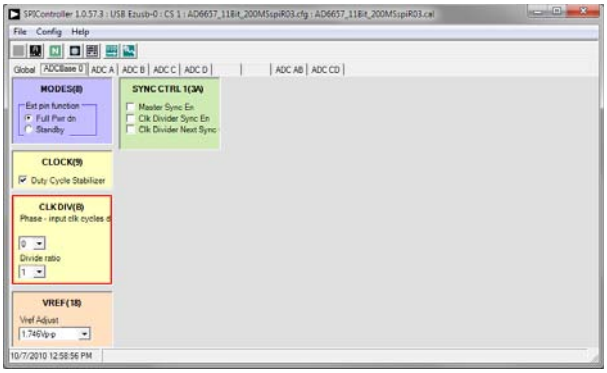

Figure 10. SPIController, CLK DIV(B) Box

4. Note that other settings can be changed on the **ADCBase 0** page (see Figure 10) and the **ADC A** and **ADC B** pages (see Figure 11) to set up the part in the desired mode (**ADC C** and **ADC D** can also be changed if using the AD6657). The **ADCBase 0** page settings affect the entire part, whereas the settings on the **ADC A** and **ADC B** (as well as **ADC C** and **ADC D**) pages affect the selected channel only. See the appropriate part data sheet; the AN-878 Application Note, *High Speed ADC SPI Control Software*; and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information on the available settings.

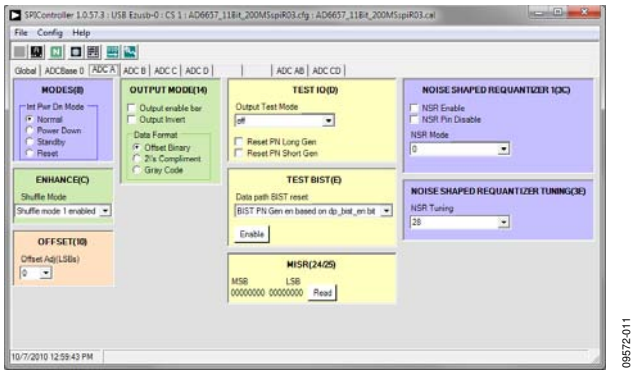

Figure 11. SPIController, Example ADC A Page

5. Click the **Run** button in the **VisualAnalog – [Canvas – (AD6657 FFT)*]** toolbar (see Figure 12).

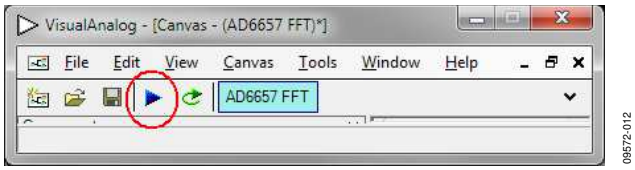

Figure 12. Run Button (Encircled in Red) in VisualAnalog – [Canvas – (AD6657 FFT)] Toolbar, Collapsed Display*

Adjusting the Amplitude of the Input Signal

The next step is to adjust the amplitude of the input signal for each channel as follows:

1. Adjust the amplitude of the input signal so that the fundamental is at the desired level. (Examine the **Fund Power** reading in the left panel of the **Graph – AD6657 Average FFT** window; see Figure 13.)

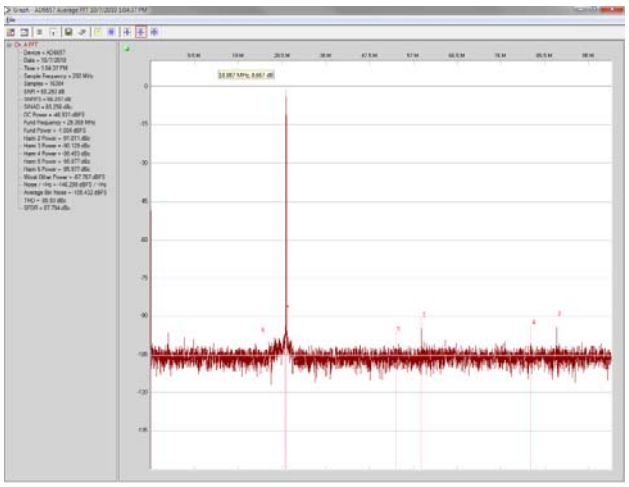

Figure 13. Graph – AD6657 Average FFT Window of VisualAnalog

2. Repeat this procedure for Channel B, Channel C, and/or Channel D.
3. Click the disk icon within the **Graph – AD6657 Average FFT** window to save the performance plot data as a .csv formatted file. See Figure 14 for an example.

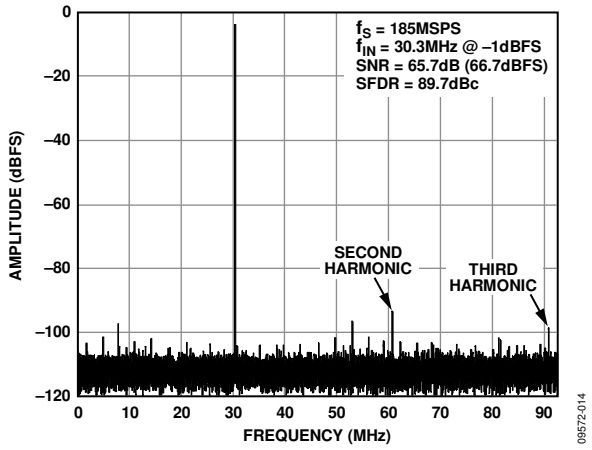

Figure 14. Typical FFT, AD6657

4. If using the NSR feature, first change the settings in the **ADC A**, **ADC B**, **ADC C**, and/or **ADC D** pages (see Figure 15) to the desired settings.

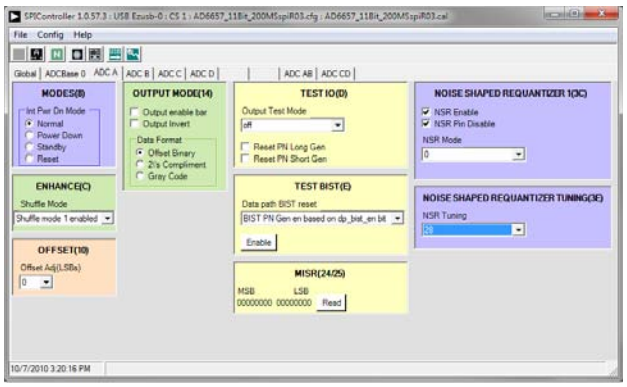

Figure 15. SPIController, Example ADC A Page – NSR Settings

5. Repeat this procedure for Channel B, Channel C, and/or Channel D.
6. Click on the button circled in the FFT Analysis box (see Figure 16) in Visual Analog to bring up the options for setting the NSR.

Figure 16. VisualAnalog – [Canvas – (AD6657 FFT)] Main Window – Showing AD6657 Average FFT Analysis*

7. Configure the settings in the FFT Analysis to match the settings selected for the NSR in the SPIController (see Figure 17).

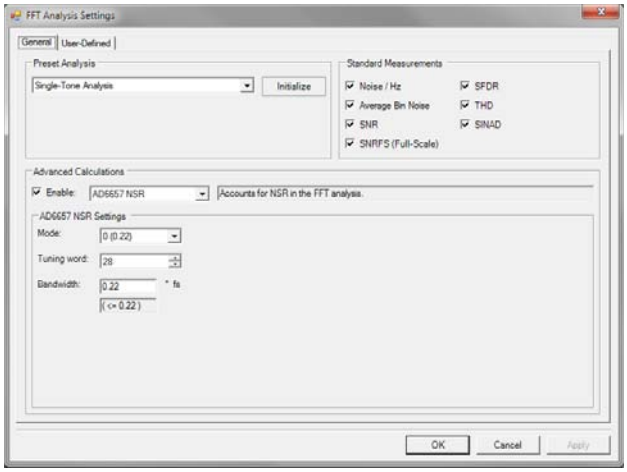

Figure 17. VisualAnalog, FFT Analysis Settings

8. The result should show an FFT plot that looks similar to Figure 18.

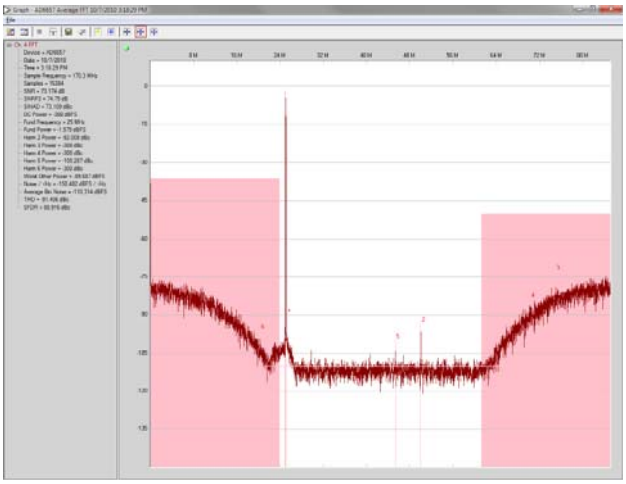

Figure 18. Graph – AD6657 Average FFT Window of VisualAnalog, NSR Enabled

9. The amplitude shows approximately 0.6 dB lower than when the NSR is disabled. The NSR circuitry introduces this loss. An amplitude of −1.6 dBFS with NSR enabled is analogous to an amplitude of −1.0 dBFS with NSR disabled.
10. Click the disk icon within the **Graph** window to save the performance plot data as a .csv formatted file. See Figure 19 for an example.

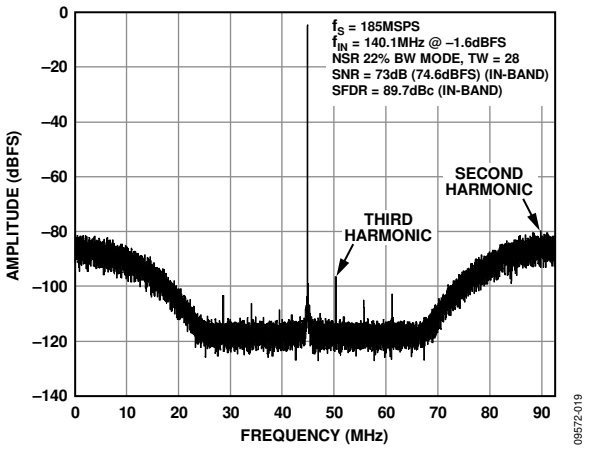

Figure 19. Typical FFT, AD6657 with NSR Enabled

Troubleshooting Tips

If the FFT plot appears abnormal, do the following:

- If you see a normal noise floor when you disconnect the signal generator from the analog input, be sure you are not overdriving the ADC. Reduce the input level, if necessary.
- In the **VisualAnalog** window, click the **Settings** button in the **Input Formatter** block. Check that **Number Format** is set to the correct encoding (offset binary by default). Repeat for the other channel.

If the FFT appears normal but the performance is poor, check the following:

- Make sure an appropriate filter is used on the analog input.
- Make sure the signal generators for the clock and the analog input are clean (low phase noise).
- Change the analog input frequency slightly if noncoherent sampling is being used.
- Make sure the SPI configuration file matches the product being evaluated.

If the FFT window remains blank after clicking **Run**, do the following:

- Make sure the evaluation board is securely connected to the HSC-ADC-EVALCZ board
- Make sure the FPGA has been programmed by verifying that the **DONE** LED is illuminated on the HSC-ADC-EVALCZ board. If this LED is not illuminated, make sure the U4 switch on the board is in the correct position for USB CONFIG.
- Make sure the correct FPGA program was installed by selecting the **Settings** button in the **ADC Data Capture** block in the **VisualAnalog** window. Then select the **FPGA** tab and verify that the proper FPGA bin file is selected for the part.

If **VisualAnalog** indicates that the **FIFO Capture timed out**, do the following:

- Make sure all power and USB connections are secure.
- Probe the DCOAB signal at either Pin A10 or Pin B10 on the P951 connector on the evaluation board and confirm that a clock signal is present at the ADC sampling rate.

EVALUATION BOARD SCHEMATICS AND ARTWORK

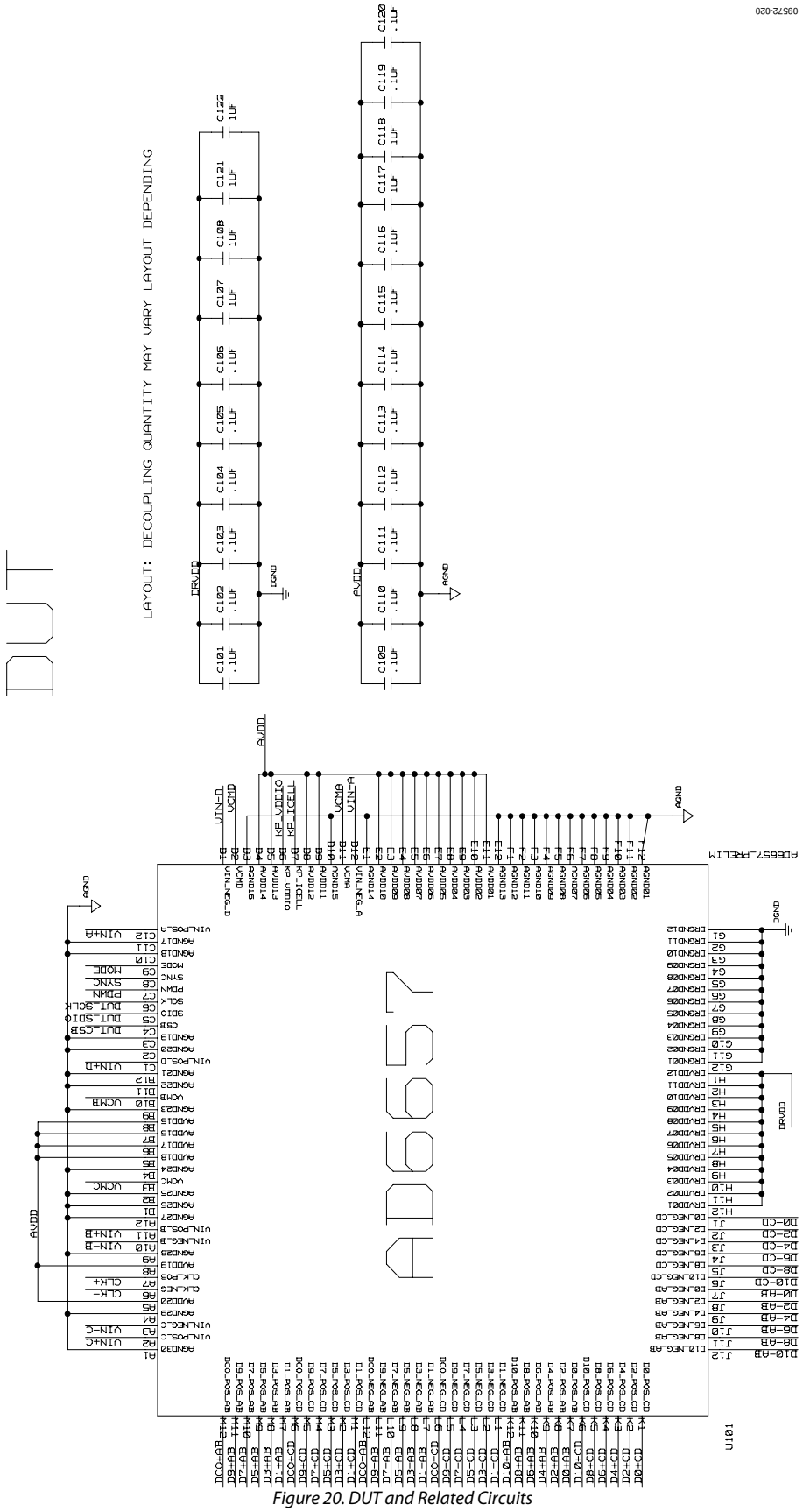

Figure 20. DUT and Related Circuits

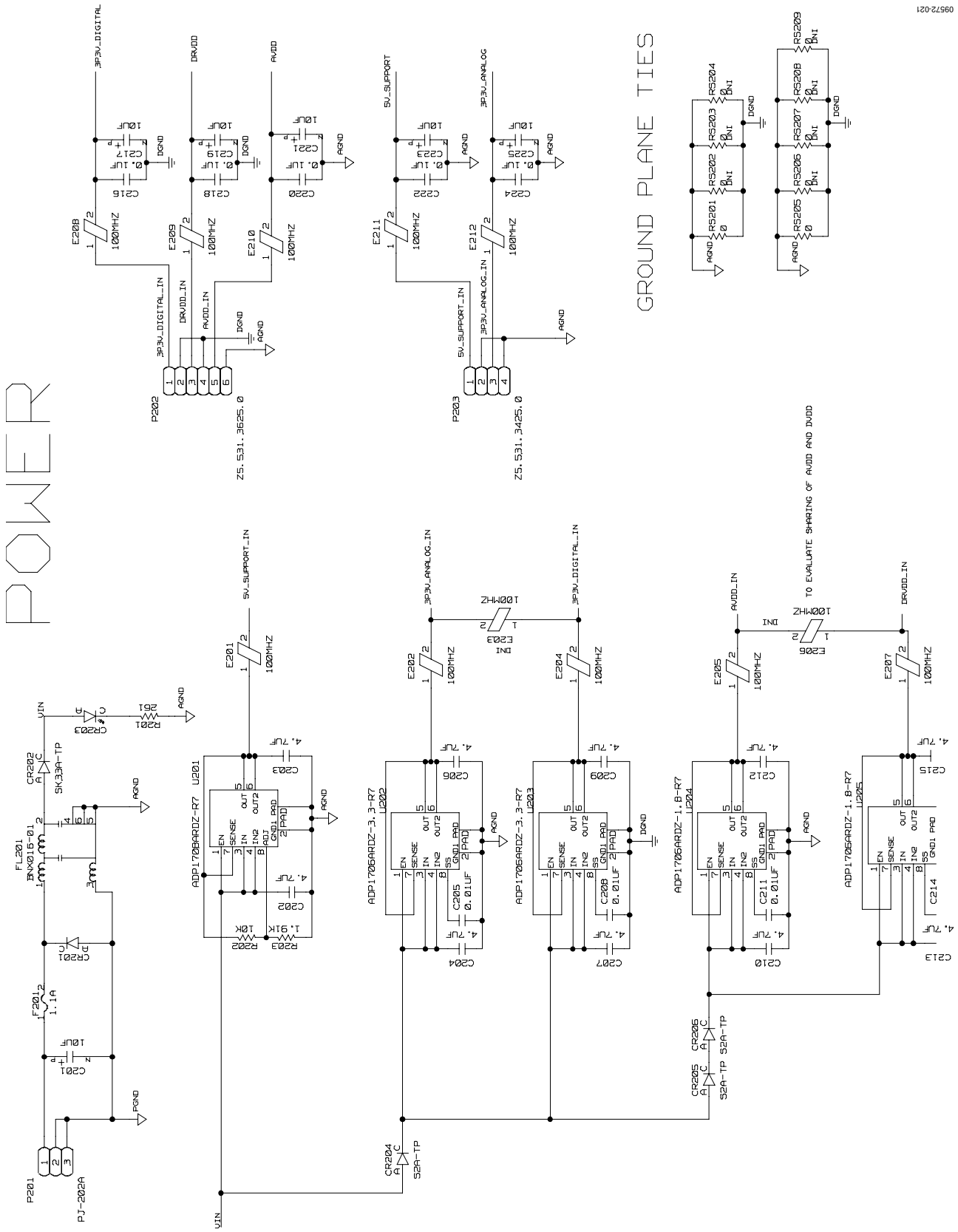

Figure 21. Board Power Input and Supply

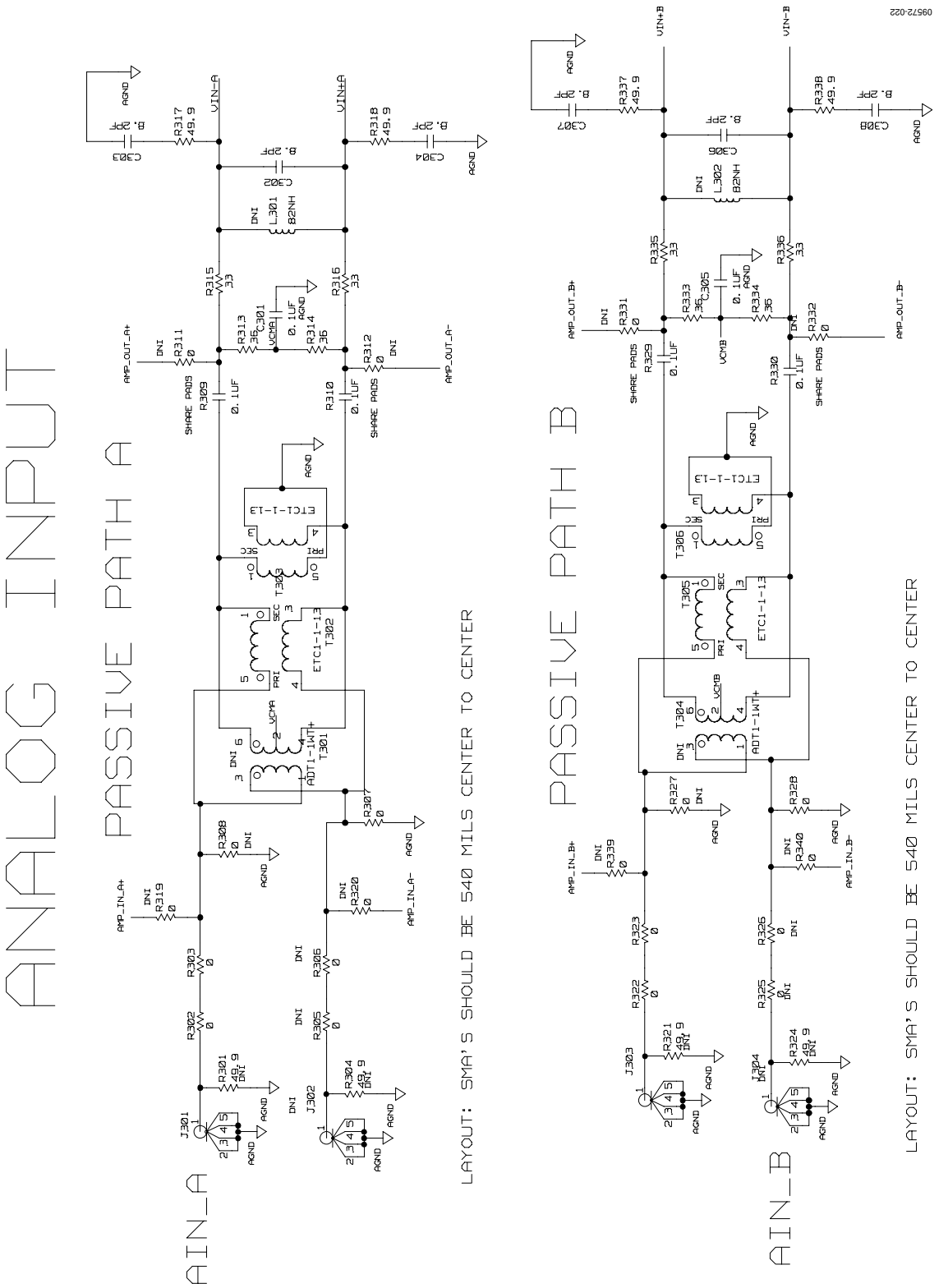

Figure 22. Passive Analog Input Circuits, Channel A and Channel B

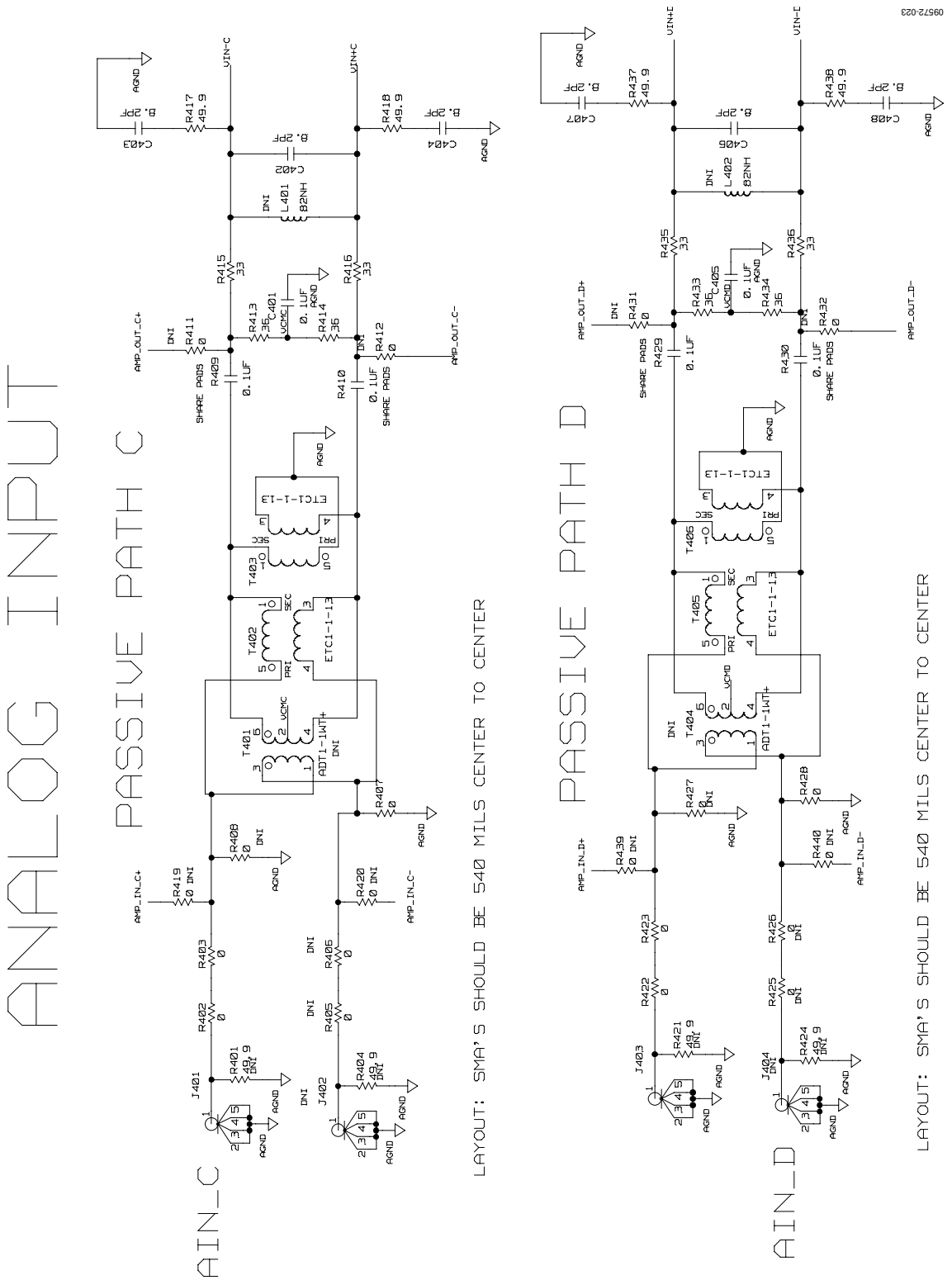

Figure 23. Passive Analog Input Circuits, Channel C and Channel D

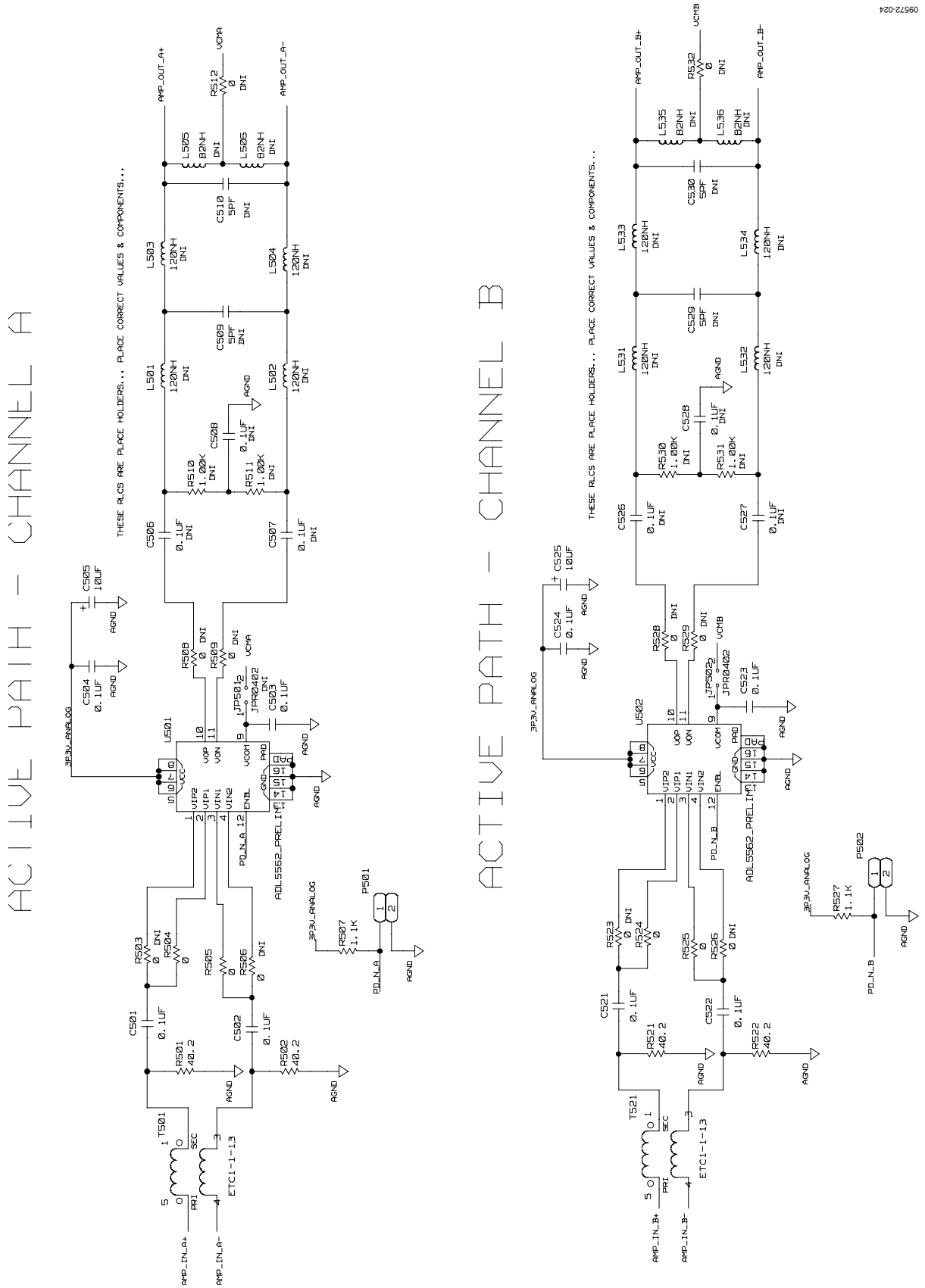

Figure 24. Optional Active Input Circuits, Channel A and Channel B

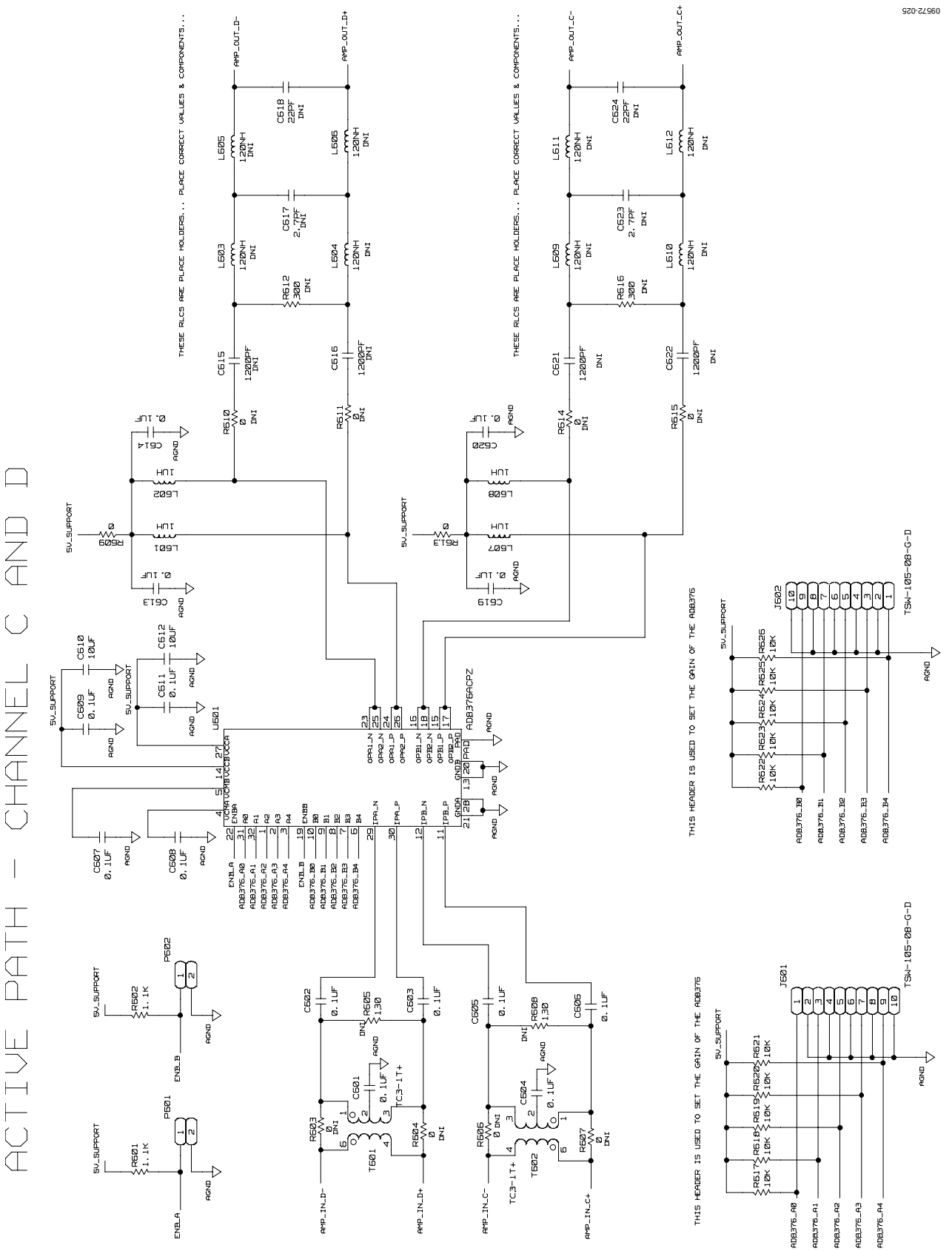

Figure 25. Optional Active Input Circuits, Channel C and Channel D

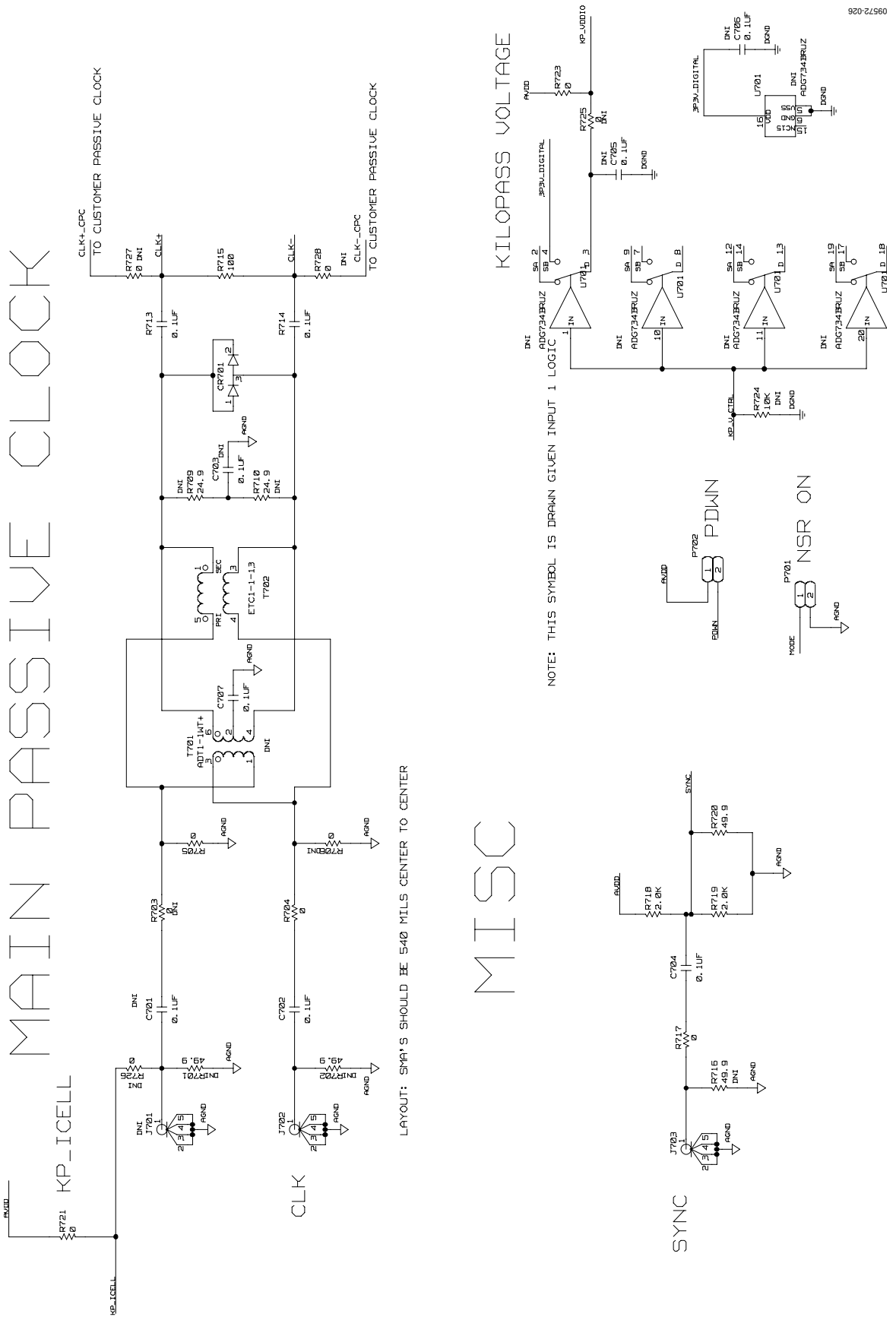

Figure 26. Default Clock Input Circuit

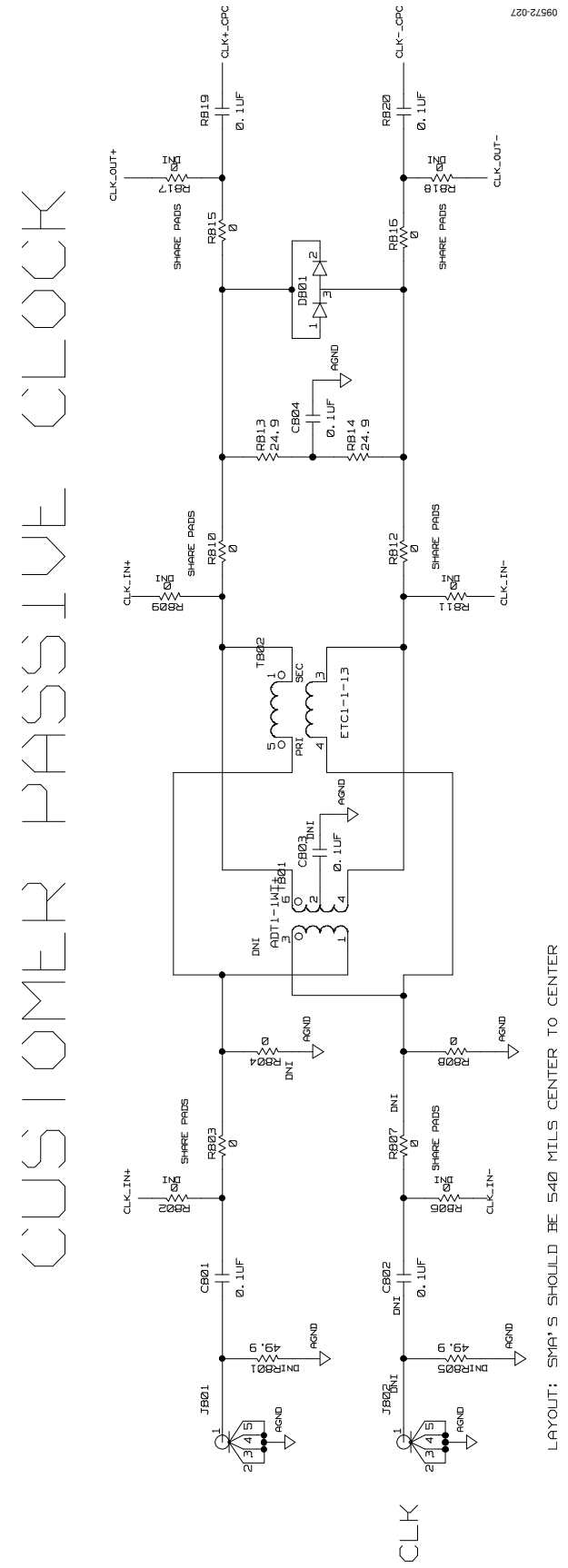

Figure 27. Optional Clock Input Circuit

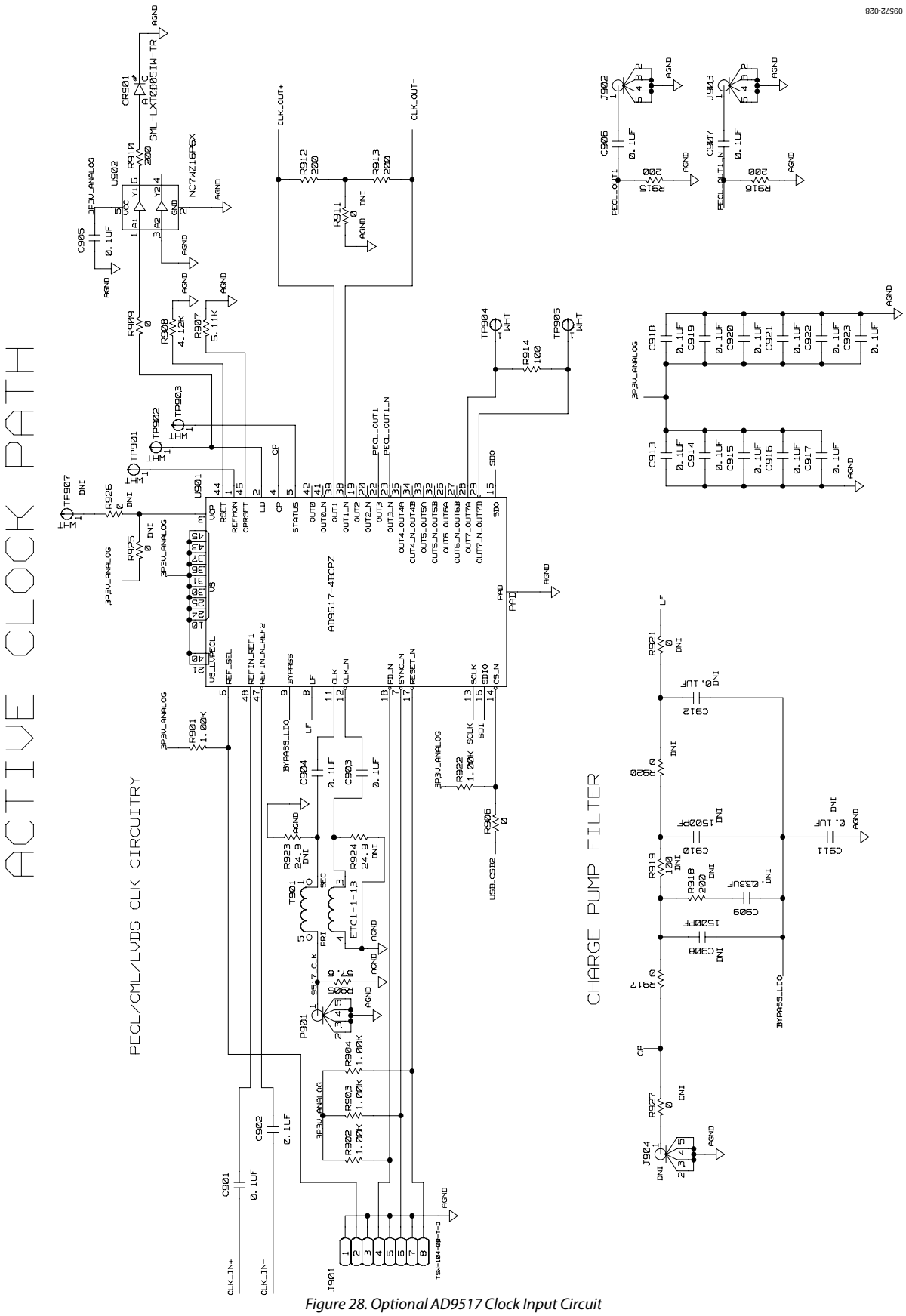

Figure 28. Optional AD9517 Clock Input Circuit

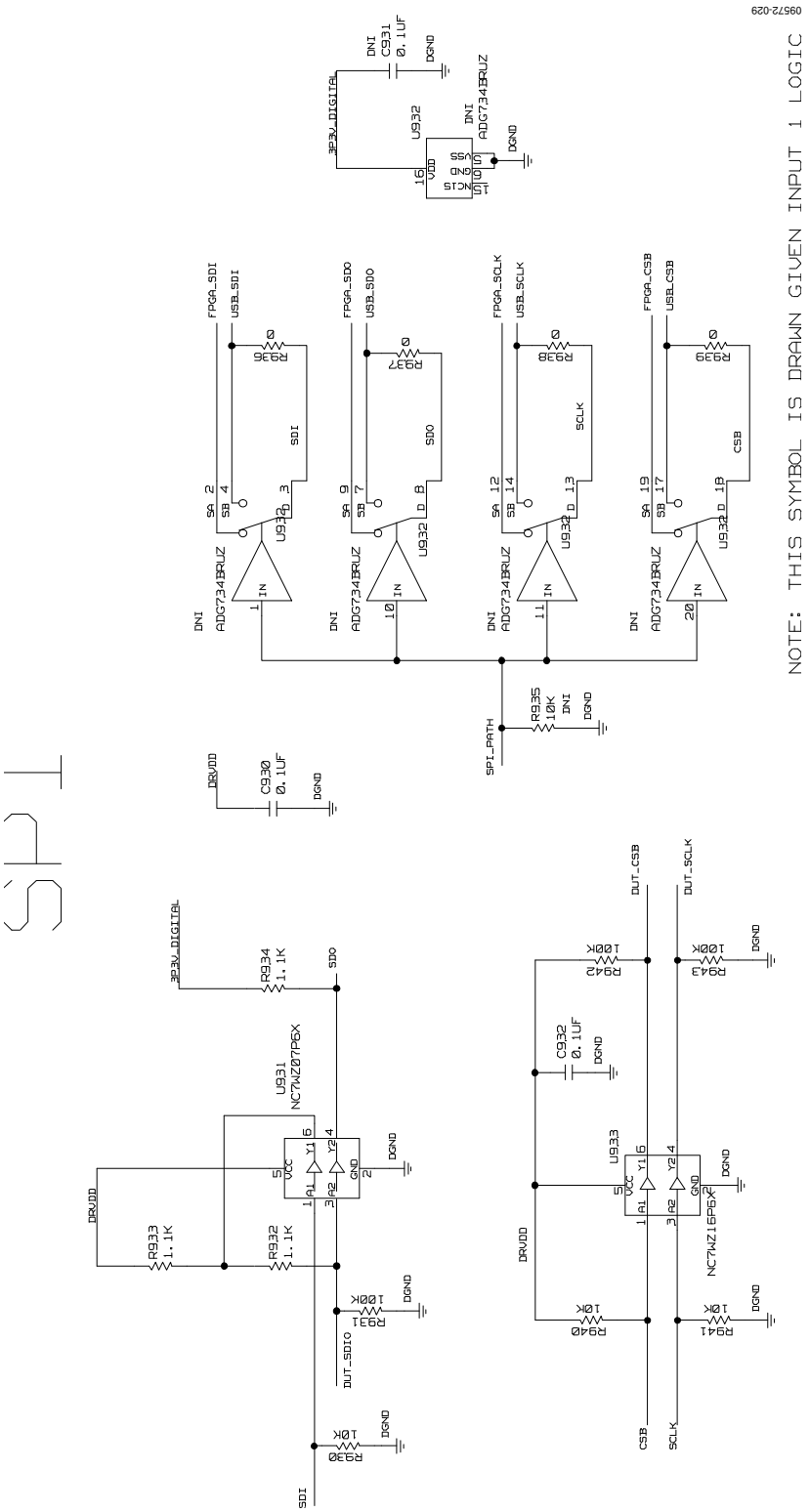

Figure 29. SPI Configuration Circuit

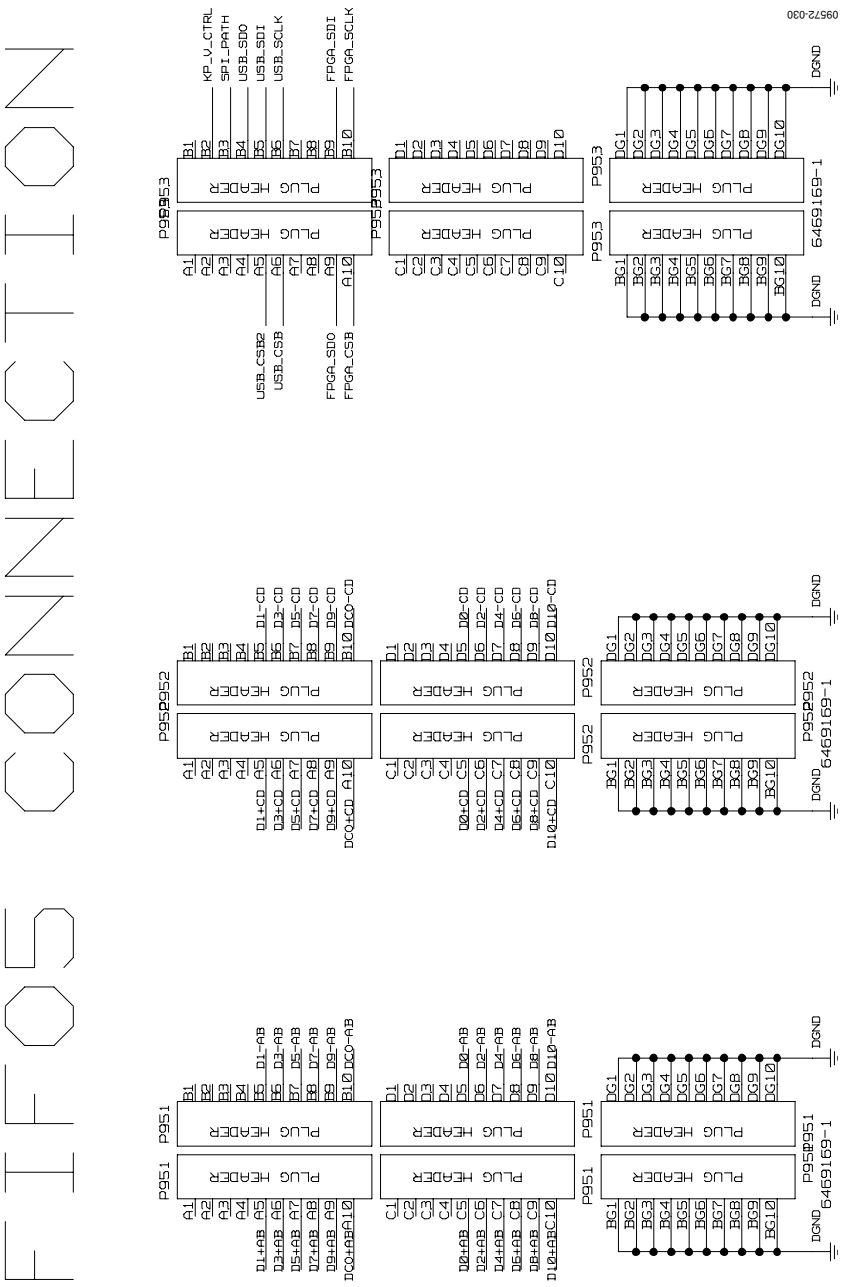

Figure 30. FIFO Board Connector Circuit

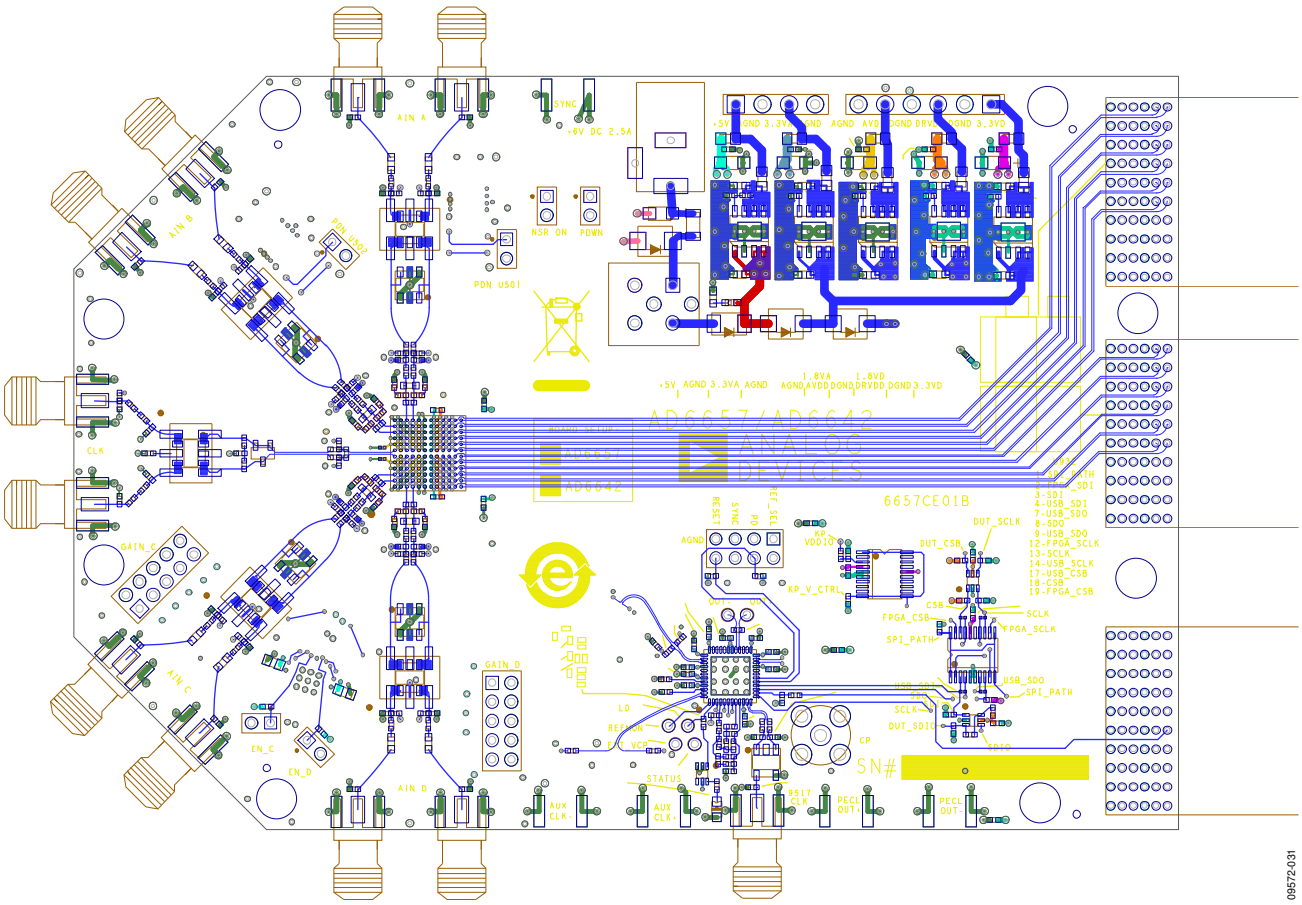

Figure 31. AD6657/AD6642 Evaluation Board, Top Side

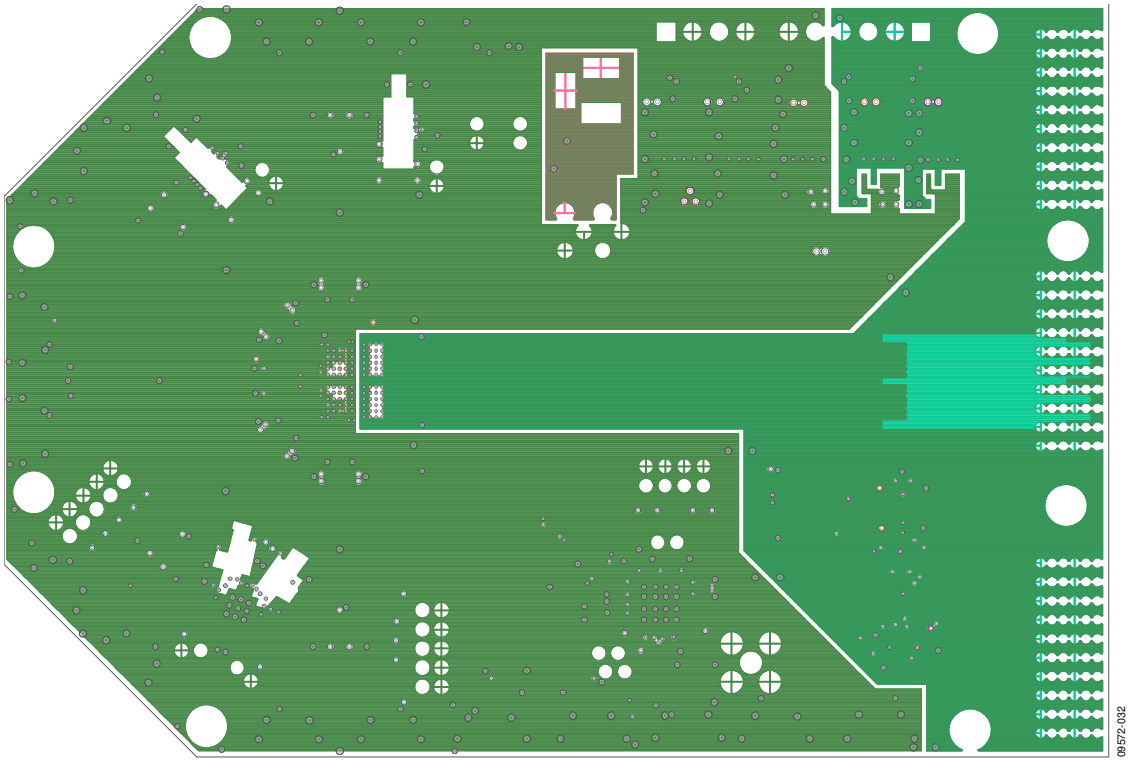

Figure 32. AD6657/AD6642 Evaluation Board, Ground Plane (Layer 2)

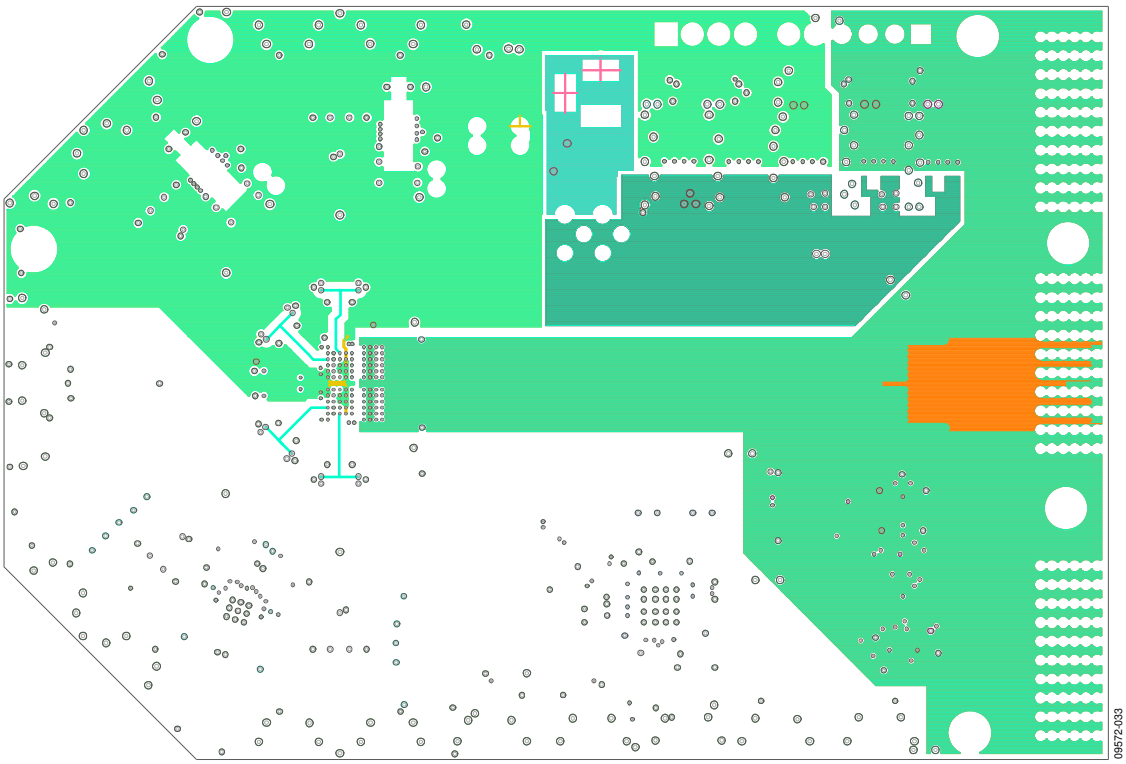

Figure 33. AD6657/AD6642 Evaluation Board, Power Plane (Layer 3)

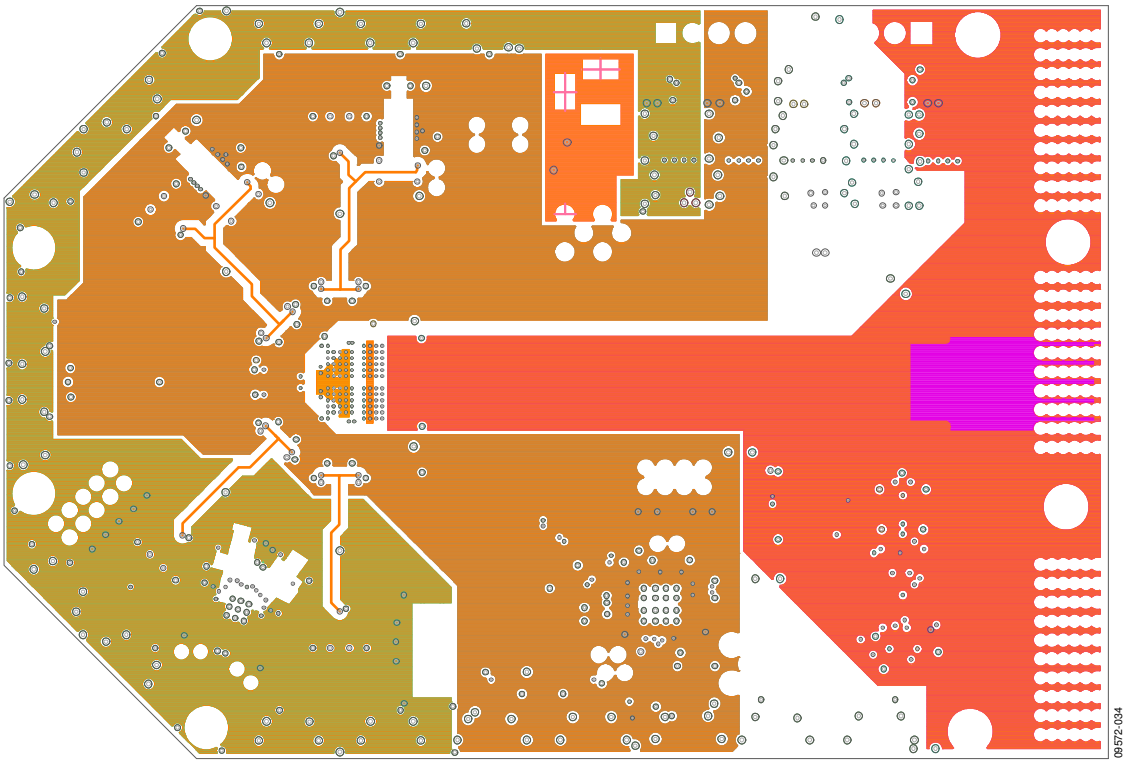

Figure 34. AD6657/AD6642 Evaluation Board, Power Plane (Layer 4)

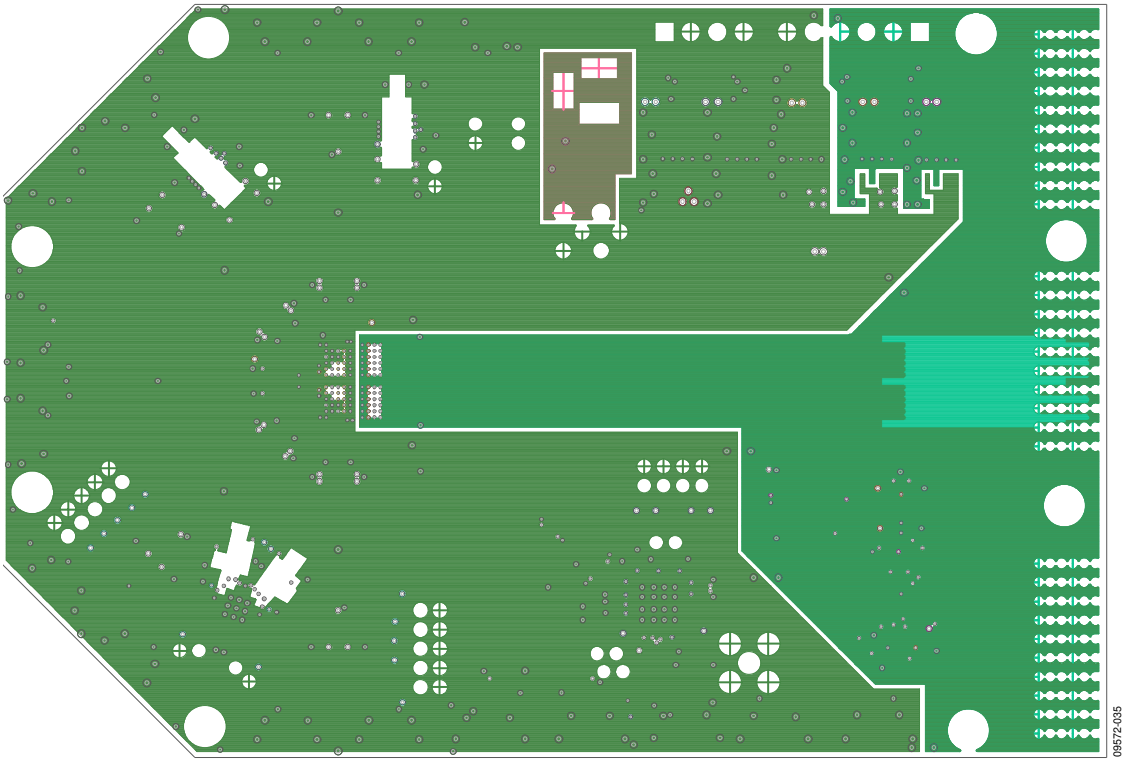

Figure 35. AD6657/AD6642 Evaluation Board, Ground Plane (Layer 5)

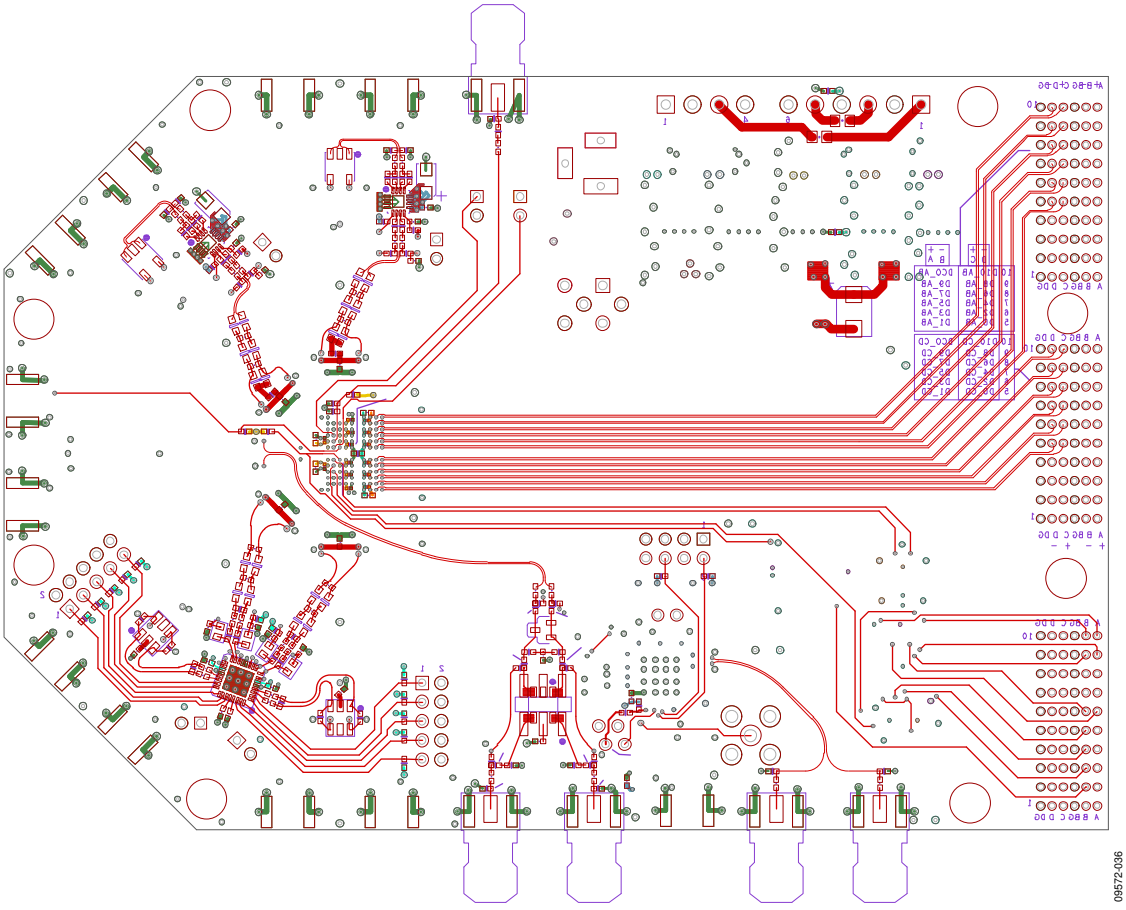

Figure 36. AD6657/AD6642 Evaluation Board, Bottom Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 1. AD6642 Board BOM

Item	Qty	Reference Designator	Description	Manufacturer/Part No.
1	1	Not applicable	PCBZ	
2	16	C101, C102, C103, C104, C105, C106, C109, C110, C111, C112, C113, C114, C115, C116, C119, C120	Ceramic capacitor, 0.1 µF, 6.3 V, X5R, 0201	Panasonic/ECJ-ZEB0J104M
3	6	C107, C108, C117, C118, C121, C122	Ceramic capacitor, 1.0 µF, 6.3 V, 10%, X5R, 0402	Murata/GRM155R60J105KE19D
4	8	C201, C217, C219, C221, C223, C225, C505, C525	Capacitor tantalum, 10 µF, 10 V, 10%, SMD	AVX/TAJA106K010RNJ
5	10	C202, C203, C204, C206, C207, C209, C210, C212, C213, C215	Ceramic capacitor, 4.7 µF, 6.3 V, X5R, 0603	Panasonic/ECJ-1VB0J475M
6	4	C205, C208, C211, C214	Ceramic capacitor, 25 V, 0.01 µF, X8R, 10%, 0402	TDK/C1005X8R1E103K
7	68	C216, C218, C220, C222, C224, C301, C305, C401, C405, C501, C502, C503, C504, C521, C522, C523, C524, C601, C602, C603, C604, C605, C606, C607, C608, C609, C611, C613, C614, C619, C620, C702, C704, C707, C801, C804, C901, C902, C903, C904, C905, C906, C907, C913, C914, C915, C916, C917, C918, C919, C920, C921, C922, C923, C930, C932, R309, R310, R329, R330, R409, R410, R429, R430, R713, R714, R819, R820	Ceramic capacitor, 16 V, 0.1 µF, X7R, 0402	Panasonic/ECJ-0EX1C104K
8	12	C302, C303, C304, C306, C307, C308, C402, C403, C404, C406, C407, C408	Ceramic capacitor, 50 V, 8.2 pF, NP0, 0402	Yageo/0402CG829D9B200
9	2	C610, C612	Ceramic capacitor, 6.3 V, 10 µF, X5R, 0805	Panasonic/ECJ-2FB0J106M
10	1	CR201	Diode, fast rec., 50 V, 1 A, SMB	Diode, Inc./RS1AB-13-F
11	1	CR202	Schottky diode, 3 amp rectifier	MCC/SK33A-TP
12	1	CR203	Green LED surface-mount	Panasonic/LNJ314G8TRA
13	3	CR204, CR205, CR206	Diode recovery rectifier	Micro Commercial Components Corp/S2A-TP
14	2	CR701, D801	Schottky diode, dual series	Avago/HSMS-2812BLK
15	1	CR901	Red LED surface-mount	Lumex/SML-LXT0805IW-TR
16	10	E201, E202, E204, E205, E207, E208, E209, E210, E211, E212	Inductor, bead core, 39 Ω, 4 A, 0805, SMD	Panasonic/EXC-ML20A390U
17	1	F201	Fuse, polyswitch, 1.10 A, reset fuse, SMD	Tyco Electronics/NANOSMDC110F-2
18	1	FL201	Filter, EMI, 50 MΩ, 15 A, 0.1 MHz to 1 GHz	Murata/BNX016-01
19	8	J301, J303, J702, J703, J801, J902, J903, P901	Connector, PCB, SMA, ST edge mount	Samtec/SMA-J-P-X-ST-EM1
20	2	J601, J602	Connector, PCB, HDR, ST, 10P	Samtec/TSW-105-08-G-D
21	1	J901	Connector, PCB header, 8-pin, double row	Samtec/TSW-104-08-T-D
22	4	L601, L602, L607, L608	Inductor, 1 µH, L7144SM	Coilcraft/0603LS-102XGLB
23	1	P201	Connector PCB dc power jack SM	CUI STACK/PJ-202A
24	1	P202	Connector, PCB header, 6 POS	Wieland/Z5.531.3625.0
25	1	P203	Connector, PCB header, 4 POS	Wieland/Z5.531.3425.0
26	6	P501, P502, P601, P602, P701, P702	Connector, PCB header, 2 POS	Samtec/TSW-102-08-G-S
27	3	P951, P952, P953	Connector, PCB, 60-pin RA connector	Tyco Electronics/6469169-1