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Dual IF Receiver

Data Sheet

AD6643

FEATURES

- 11-bit, 250 MSPS output data rate per channel
- Performance with NSR enabled
  - SNR: 74.5 dBFS in a 55 MHz band to 90 MHz at 250 MSPS
  - SNR: 72.0 dBFS in a 82 MHz band to 90 MHz at 250 MSPS
- Performance with NSR disabled
  - SNR: 66.2 dBFS up to 90 MHz at 250 MSPS
  - SFDR: 85 dBc up to 185 MHz at 250 MSPS
- Total power consumption: 706 mW at 200 MSPS
- 1.8 V supply voltages
- LVDS (ANSI-644 levels) outputs
- Integer 1-to-8 input clock divider (625 MHz maximum input)
- Internal ADC voltage reference
- Flexible analog input range
  - 1.4 V p-p to 2.0 V p-p (1.75 V p-p nominal)
- Differential analog inputs with 400 MHz bandwidth
- 95 dB channel isolation/crosstalk
- Serial port control
- Energy saving power-down modes

APPLICATIONS

- Communications
- Diversity radio and smart antenna (MIMO) systems
- Multimode digital receivers (3G)
  - WCDMA, LTE, CDMA2000
  - WiMAX, TD-SCDMA
- I/Q demodulation systems
- General-purpose software radios

FUNCTIONAL BLOCK DIAGRAM

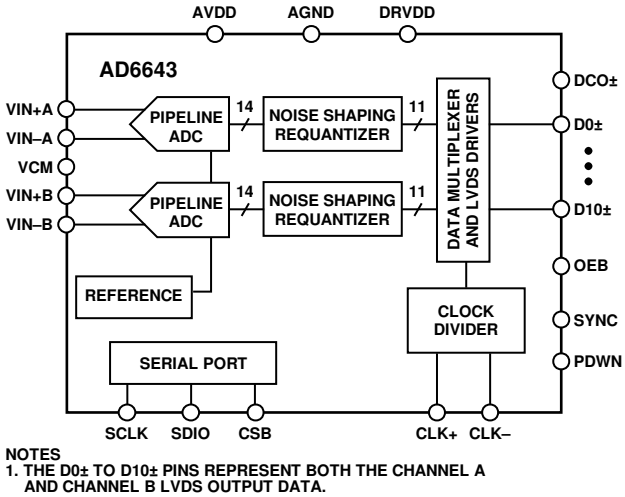

Figure 1.

GENERAL DESCRIPTION

The AD6643 is an 11-bit, 200 MSPS/250 MSPS, dual-channel intermediate frequency (IF) receiver specifically designed to support multi-antenna systems in telecommunication applications where high dynamic range performance, low power, and small size are desired.

The device consists of two high performance analog-to-digital converters (ADCs) and noise shaping requantizer (NSR) digital blocks. Each ADC consists of a multistage, differential pipelined architecture with integrated output error correction logic, and each ADC features a wide bandwidth switched capacitor sampling network within the first stage of the differential pipeline. An integrated voltage reference eases design considerations. A duty cycle stabilizer (DCS) compensates for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

Each ADC output is connected internally to an NSR block. The integrated NSR circuitry allows for improved SNR performance in a smaller frequency band within the Nyquist bandwidth. The device supports two different output modes selectable via the SPI. With the NSR feature enabled, the outputs of the ADCs are processed such that the AD6643 supports enhanced SNR performance within a limited portion of the Nyquist bandwidth while maintaining an 11-bit output resolution.

The NSR block can be programmed to provide a bandwidth of either 22% or 33% of the sample clock. For example, with a sample clock rate of 185 MSPS, the AD6643 can achieve up to 75.5 dBFS SNR for a 40 MHz bandwidth in the 22% mode and up to 73.7 dBFS SNR for a 60 MHz bandwidth in the 33% mode.

(continued on Page 3)

Rev. C Document Feedback

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AD6643* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD6643 Evaluation Board
- AD9643 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-586: LVDS Outputs for High Speed A/D Converters
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD6643: Dual IF Receiver Datasheet

User Guides

- UG-293: Evaluating the AD9643/AD9613/AD6649/AD6643 Analog-to-Digital Converters

TOOLS AND SIMULATIONS

- Visual Analog
- AD6643 IBIS Model
- AD6643 LFCSP Analog Input S-Parameter

DESIGN RESOURCES

- AD6643 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD6643 EngineerZone Discussions.

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4/11—Revision 0: Initial Version

When the NSR block is disabled, the ADC data is provided directly to the output at a resolution of 11 bits. The AD6643 can achieve up to 66.5 dBFS SNR for the entire Nyquist bandwidth when operated in this mode. This allows the AD6643 to be used in telecommunication applications such as a digital predistortion observation path where wider bandwidths are required.

After digital signal processing, multiplexed output data is routed into two 11-bit output ports such that the maximum data rate is 400 Mbps (DDR). These outputs are LVDS and support ANSI-644 levels.

The AD6643 receiver digitizes a wide spectrum of IF frequencies. Each receiver is designed for simultaneous reception of a separate antenna. This IF sampling architecture greatly reduces component cost and complexity compared with traditional analog techniques or less integrated digital methods.

Flexible power-down options allow significant power savings. Programming for device setup and control is accomplished using a 3-wire SPI-compatible serial interface with numerous modes to support board level system testing.

The AD6643 is available in a Pb-free, RoHS-compliant, 64-lead, 9 mm × 9 mm lead frame chip scale package (LFCSP_VQ) and is specified over the industrial temperature range of −40°C to +85°C. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Two ADCs are contained in a small, space-saving, 9 mm × 9 mm × 0.85 mm, 64-lead LFCSP package.
2. Pin selectable noise shaping requantizer (NSR) function that allows for improved SNR within a reduced bandwidth of up to 60 MHz at 185 MSPS.
3. LVDS digital output interface configured for low cost FPGA families.
4. Operation from a single 1.8 V supply.
5. Standard serial port interface (SPI) that supports various product features and functions, such as data formatting (offset binary or twos complement), NSR, power-down, test modes, and voltage reference mode.
6. On-chip integer 1-to-8 input clock divider and multichip sync function to support a wide range of clocking schemes and multichannel subsystems.

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, default SPI, unless otherwise noted.

Table 1.

		AD6643-200			AD6643-250			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	11			11			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full			±10			±10	mV
Gain Error	Full			+2/−6			−5/+3	% FSR
Differential Nonlinearity (DNL)[1]	Full		±0.1	±0.25		±0.1	±0.4	LSB
Integral Nonlinearity (INL)[1]	Full		±0.2	±0.25		±0.2	±0.4	LSB
MATCHING CHARACTERISTIC								
Offset Error	25°C			±13			±13	mV
Gain Error	25°C			−2/+3.5			−2.5/+3.5	% FSR
TEMPERATURE DRIFT								
Offset Error	Full		±15			±15		ppm/°C
Gain Error	Full		±87			±87		ppm/°C
INPUT REFERRED NOISE								
VREF = 1.75 V	25°C		0.614			0.614		LSB rms
ANALOG INPUT								
Input Span	Full		1.75			1.75		V p-p
Input Capacitance[2]	Full		2.5			2.5		pF
Input Resistance[3]	Full		20			20		kΩ
Input Common-Mode Voltage	Full		0.9			0.9		V
POWER SUPPLIES								
Supply Voltage								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current								
I_{AVDD}[1]	Full		238	260		256	275	mA
I_{DRVDD}[1] (NSR Disabled)	Full		154	215		180	215	mA
I_{DRVDD}[1] (NSR Enabled—22% Mode)	Full		172			206		mA
I_{DRVDD}[1] (NSR Enabled—33% Mode)	Full		186			218		mA
POWER CONSUMPTION								
Sine Wave Input[1] (DRVDD = 1.8 V, NSR Disabled)	Full		706	855		785	873	mW
Sine Wave Input[1] (DRVDD = 1.8 V, NSR Enabled—22% Mode)	Full		738			832		mW
Sine Wave Input[1] (DRVDD = 1.8 V, NSR Enabled—33% Mode)	Full		765			853		mW
Standby Power[4]	Full		90			90		mW
Power-Down Power	Full		10			10		mW

[1] Measured using a 10 MHz, 0 dBFS sine wave, and 100 Ω termination on each LVDS output pair.
[2] Input capacitance refers to the effective capacitance between one differential input pin and its complement.
[3] Input resistance refers to the effective resistance between one differential input pin and its complement.
[4] Standby power is measured using a dc input and the CLK± pins inactive (set to AVDD or AGND).

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, default SPI, unless otherwise noted.

Table 2.

		AD6643-200			AD6643-250			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE-RATIO (SNR)								
NSR Disabled								
f_{IN} = 30 MHz	25°C		66.6			66.4		dBFS
f_{IN} = 90 MHz	25°C		66.5			66.2		dBFS
	Full	66.2						dBFS
f_{IN} = 140 MHz	25°C		66.4			66.1		dBFS
f_{IN} = 185 MHz	25°C		66.2			65.9		dBFS
	Full				65.3			dBFS
f_{IN} = 220 MHz	25°C		66.0			65.6		dBFS
NSR Enabled								
22% BW Mode								
f_{IN} = 30 MHz	25°C		76.1			74.8		dBFS
f_{IN} = 90 MHz	25°C		76.1			74.5		dBFS
	Full	74.5						dBFS
f_{IN} = 140 MHz	25°C		75.5			74.2		dBFS
f_{IN} = 185 MHz	25°C		74.7			73.7		dBFS
	Full				72.6			dBFS
f_{IN} = 220 MHz	25°C		74.2			73.4		dBFS
33% BW Mode								
f_{IN} = 30 MHz	25°C		76.1			72.3		dBFS
f_{IN} = 90 MHz	25°C		73.6			72.0		dBFS
	Full	72.0						dBFS
f_{IN} = 140 MHz	25°C		73.1			71.7		dBFS
f_{IN} = 185 MHz	25°C		72.6			71.2		dBFS
	Full				70.1			dBFS
f_{IN} = 220 MHz	25°C		72.1			70.9		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION (SINAD)								
f_{IN} = 30 MHz	25°C		65.6			65.4		dBFS
f_{IN} = 90 MHz	25°C		65.5			65.2		dBFS
	Full	65.1						dBFS
f_{IN} = 140 MHz	25°C		65.3			65.1		dBFS
f_{IN} = 185 MHz	25°C		65.1			64.9		dBFS
	Full				64.3			dBFS
f_{IN} = 220 MHz	25°C		64.9			64.6		dBFS
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 30 MHz	25°C		−92			−90		dBc
f_{IN} = 90 MHz	25°C		−91			−88		dBc
	Full			−80				dBc
f_{IN} = 140 MHz	25°C		−88			−86		dBc
f_{IN} = 185 MHz	25°C		−88			−85		dBc
	Full						−80	dBc
f_{IN} = 220 MHz	25°C		−84			−85		dBc

Parameter[1]	Temperature	AD6643-200 Min	AD6643-200 Typ	AD6643-200 Max	AD6643-250 Min	AD6643-250 Typ	AD6643-250 Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 30 MHz	25°C		92			90		dBc
f_{IN} = 90 MHz	25°C		91			88		dBc
	Full	80						dBc
f_{IN} = 140 MHz	25°C		88			86		dBc
f_{IN} = 185 MHz	25°C		88			85		dBc
	Full				79			dBc
f_{IN} = 220 MHz	25°C		84			85		dBc
WORST OTHER HARMONIC OR SPUR								
f_{IN} = 30 MHz	25°C		−94			−94		dBc
f_{IN} = 90 MHz	25°C		−94			−93		dBc
	Full			−80				dBc
f_{IN} = 140 MHz	25°C		−95			−92		dBc
f_{IN} = 185 MHz	25°C		−94			−92		dBc
	Full						−80	dBc
f_{IN} = 220 MHz	25°C		−93			−88		dBc
TWO TONE SFDR								
f_{IN} = 184.12 MHz, 187.12 MHz (−7 dBFS)	25°C		88			88		dBc
CROSSTALK[2]	Full		95			95		dB
FULL POWER BANDWIDTH[3]	25°C		1000			1000		MHz

[1] For a complete set of definitions, see the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*.
[2] Crosstalk is measured at 100 MHz with −1 dBFS on one channel and with no input on the alternate channel.
[3] Full power bandwidth is the bandwidth for the ADC inputs at which the spectral power of the fundamental frequency is reduced by 3 dB.

DIGITAL SPECIFICATIONS—AD6643-200/AD6643-250

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, DCS enabled, default SPI, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
Input Current Level					
High	Full	10		22	µA
Low	Full	−22		−10	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
SYNC INPUT					
Logic Compliance			CMOS/LVDS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
Input Voltage Level					
High	Full	1.2		AVDD	V
Low	Full	AGND		0.6	V

Parameter	Temperature	Min	Typ	Max	Unit
Input Current Level					
High	Full	−5		+5	µA
Low	Full	−100		+100	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ
LOGIC INPUT (CSB)[1]					
Input Voltage Level					
High	Full	1.22		2.1	V
Low	Full	0		0.6	V
Input Current Level					
High	Full	−5		+5	µA
Low	Full	−80		−45	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK)[2]					
Input Voltage Level					
High	Full	1.22		2.1	V
Low	Full	0		0.6	V
Input Current Level					
High	Full	45		70	µA
Low	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (SDIO)[1]					
Input Voltage Level					
High	Full	1.22		2.1	V
Low	Full	0		0.6	V
Input Current Level					
High	Full	45		70	µA
Low	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
LOGIC INPUTS (OEB, PDWN)[2]					
Input Voltage Level					
High	Full	1.22		2.1	V
Low	Full	0		0.6	V
Input Current Level					
High	Full	45		70	µA
Low	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS					
LVDS Data and OR Outputs					
Differential Output Voltage (VOD)					
ANSI Mode	Full	250	350	450	mV
Reduced Swing Mode	Full	150	200	280	mV
Output Offset Voltage (VOS)					
ANSI Mode	Full	1.15	1.25	1.35	V
Reduced Swing Mode	Full	1.15	1.25	1.35	V

[1] Pull up.
[2] Pull down.

SWITCHING SPECIFICATIONS

Table 4.

Parameter	Symbol	Temperature	AD6643-200 Min	AD6643-200 Typ	AD6643-200 Max	AD6643-250 Min	AD6643-250 Typ	AD6643-250 Max	Unit
CLOCK INPUT PARAMETERS									
Input Clock Rate		Full			625			625	MHz
Conversion Rate[1]		Full	40		200	40		250	MSPS
CLK Period—Divide-by-1 Mode[2]	t_{CLK}	Full	4.0			4			ns
CLK Pulse Width High[2]	t_{CH}								
Divide-by-1 Mode, DCS Enabled		Full	2.25	2.5	2.75	1.8	2.0	2.2	ns
Divide-by-1 Mode, DCS Disabled		Full	2.375	2.5	2.625	1.9	2.0	2.1	ns
Divide-by-2 Through Divide-by-8 Modes, DCS Enabled		Full	0.8			0.8			ns
DATA OUTPUT PARAMETERS (DATA, OR)							1.0		
LVDS Mode							0.1		
Data Propagation Delay[2]	t_{PD}	Full		6.0			6.0		ns
DCO Propagation Delay[2]	t_{DCO}	Full		6.7			6.7		ns
DCO to Data Skew[2]	t_{SKEW}	Full	0.4	0.7	1.0	0.4	0.7	1.0	ns
Pipeline Delay (Latency)		Full		10			10		Cycles[3]
NSR Enabled		Full		13			13		Cycles[3]
Aperture Delay[4]	t_A	Full		1.0			1.0		ns
Aperture Uncertainty (Jitter)[4]	t_J	Full		0.1			0.1		ps rms
Wake-Up Time (from Standby)		Full		10			10		µs
Wake-Up Time (from Power-Down)		Full		250			250		µs
OUT-OF-RANGE RECOVERY TIME		Full		3			3		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] See Figure 2 for timing diagram.
[3] Cycles refers to ADC input sample rate cycles.
[4] Not shown in timing diagrams.

TIMING SPECIFICATIONS—AD6643-200/AD6643-250

Table 5.

Parameter	Conditions	Min	Typ	Max	Unit
SYNC TIMING REQUIREMENTS	See Figure 3 for timing details				
t_{SSYNC}	SYNC to the rising edge of CLK setup time		0.3		ns
t_{HSYNC}	SYNC to the rising edge of CLK hold time		0.4		ns
SPI TIMING REQUIREMENTS	See Figure 59 for SPI timing diagram				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK should be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK should be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 59)	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 59)	10			ns

Timing Diagrams

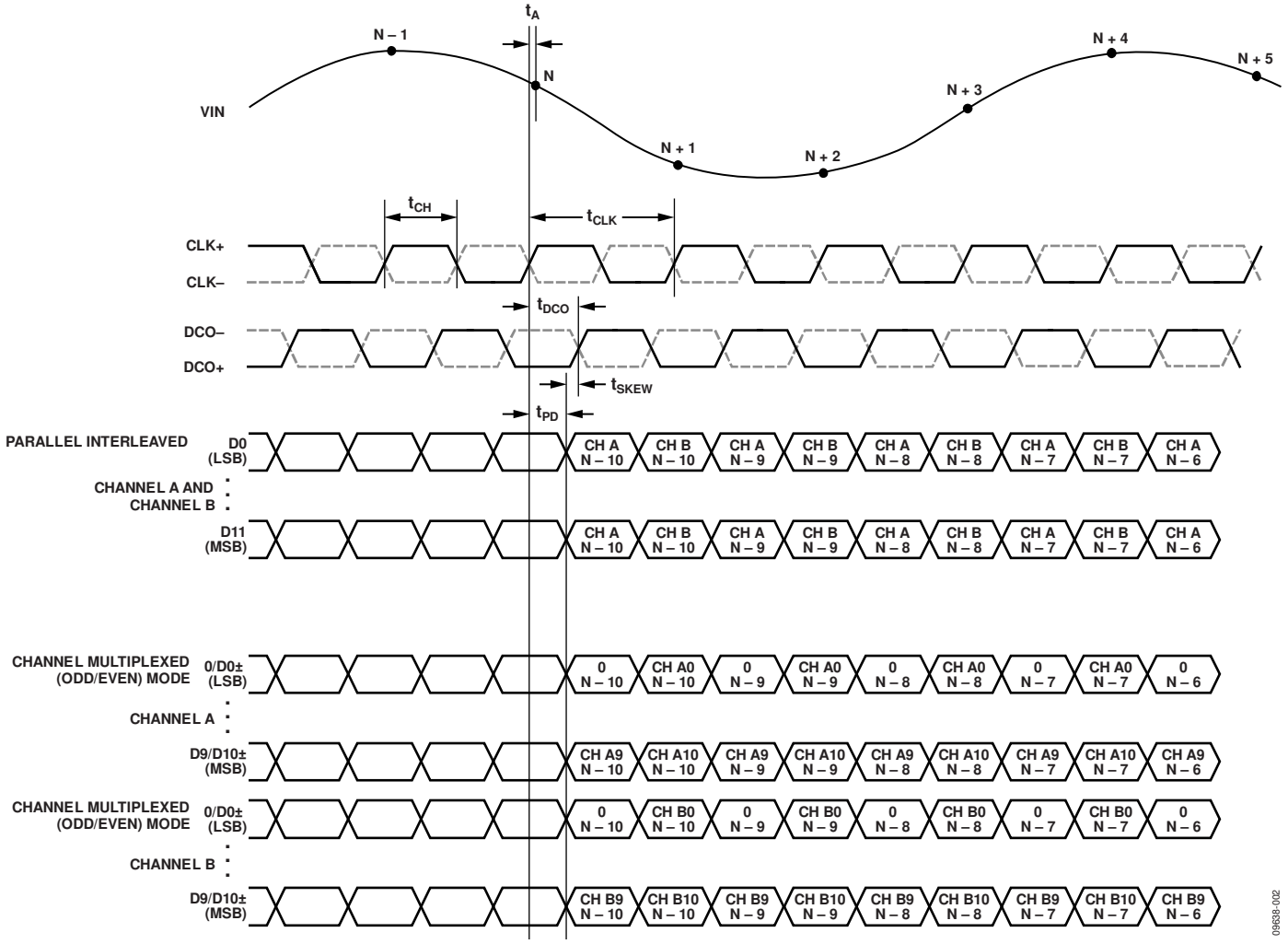


Figure 2. LVDS Modes for Data Output Timing Latency. NSR Disabled (Enabling NSR Adds an Additional Three Clock Cycles of Latency)

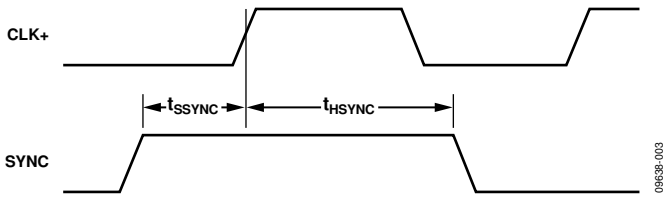


Figure 3. SYNC Timing Inputs

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.3 V
SCLK to AGND	−0.3 V to DRVDD + 0.3 V
SDIO to AGND	−0.3 V to DRVDD + 0.3 V
OEB to AGND	−0.3 V to DRVDD + 0.3 V
PDWN to AGND	−0.3 V to DRVDD + 0.3 V
OR+/OR− to AGND	−0.3 V to DRVDD + 0.3 V
D0−/D0+ Through D10−/D10+ to AGND	−0.3 V to DRVDD + 0.3 V
DCO+/DCO− to AGND	−0.3 V to DRVDD + 0.3 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the printed circuit board (PCB) increases the reliability of the solder joints, maximizing the thermal capability of the package.

Typical θ_{JA} is specified for a 4-layer PCB that uses a solid ground plane. As listed in Table 7, airflow increases heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces the θ_{JA}.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC}[1,3]	θ_{JB}[1,4]	Unit
64-Lead LFCSP 9 mm × 9 mm (CP-64-4)	0	26.8	1.14	10.4	°C/W
	1.0	21.6			°C/W
	2.0	20.2			°C/W

[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

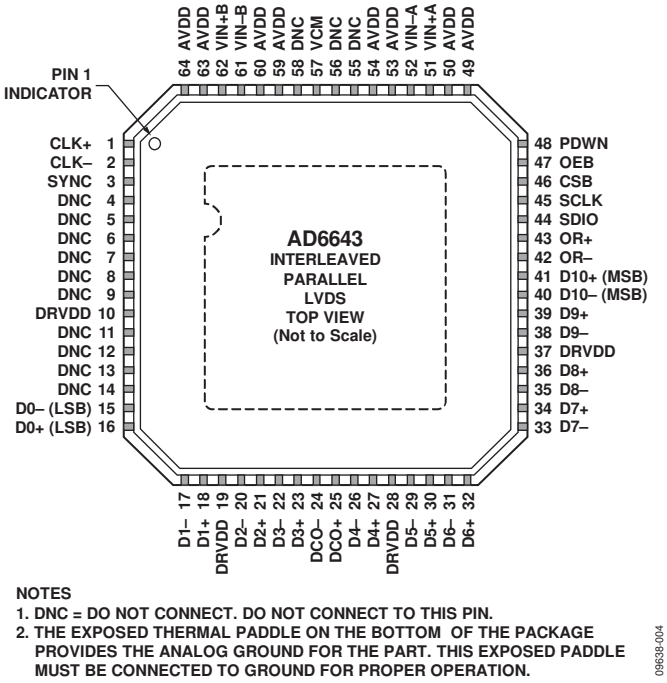
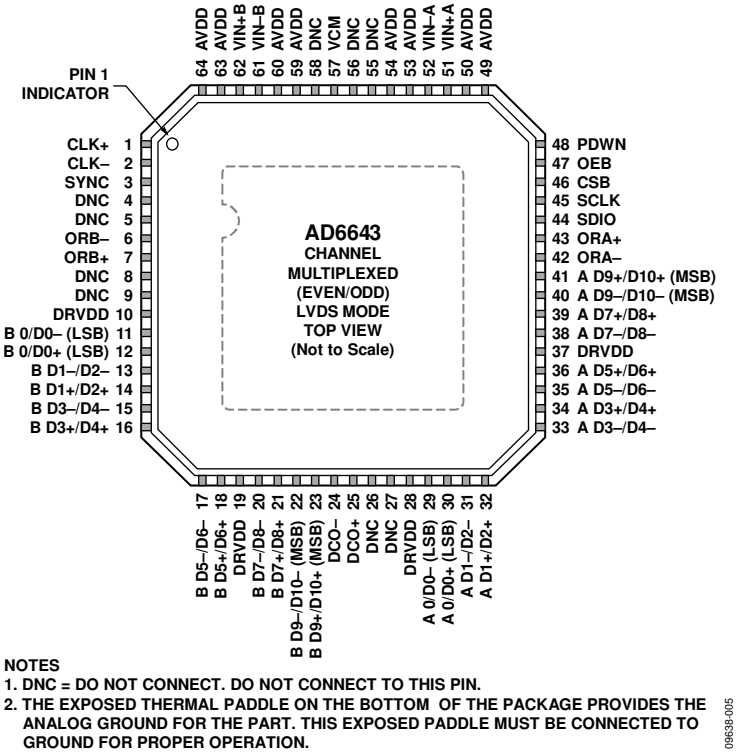


Figure 4. Pin Configuration (Top View), LFCSP Interleaved Parallel LVDS

Table 8. Pin Function Descriptions for the Interleaved Parallel LVDS Mode

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
4 to 9, 11 to 14, 55, 56, 58	DNC		Do Not Connect. Do not connect to these pins.
0	AGND, Exposed Paddle	Ground	Analog Ground. The exposed thermal paddle on the bottom of the package provides the analog ground for the device. This exposed paddle must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs. This pin should be decoupled to ground using a 0.1 µF capacitor.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
15	D0− (LSB)	Output	Channel A/Channel B LVDS Output Data 0—True.
16	D0+ (LSB)	Output	Channel A/Channel B LVDS Output Data 0—Complement.
18	D1+	Output	Channel A/Channel B LVDS Output Data 1—True.
17	D1−	Output	Channel A/Channel B LVDS Output Data 1—Complement.
21	D2+	Output	Channel A/Channel B LVDS Output Data 2—True.
20	D2−	Output	Channel A/Channel B LVDS Output Data 2—Complement.
23	D3+	Output	Channel A/Channel B LVDS Output Data 3—True.
22	D3−	Output	Channel A/Channel B LVDS Output Data 3—Complement.
27	D4+	Output	Channel A/Channel B LVDS Output Data 4—True.

Pin No.	Mnemonic	Type	Description
26	D4−	Output	Channel A/Channel B LVDS Output Data 4—Complement.
30	D5+	Output	Channel A/Channel B LVDS Output Data 5—True.
29	D5−	Output	Channel A/Channel B LVDS Output Data 5—Complement.
32	D6+	Output	Channel A/Channel B LVDS Output Data 6—True.
31	D6−	Output	Channel A/Channel B LVDS Output Data 6—Complement.
34	D7+	Output	Channel A/Channel B LVDS Output Data 7—True.
33	D7−	Output	Channel A/Channel B LVDS Output Data 7—Complement.
36	D8+	Output	Channel A/Channel B LVDS Output Data 8—True.
35	D8−	Output	Channel A/Channel B LVDS Output Data 8—Complement.
39	D9+	Output	Channel A/Channel B LVDS Output Data 9—True.
38	D9−	Output	Channel A/Channel B LVDS Output Data 9—Complement.
41	D10+ (MSB)	Output	Channel A/Channel B LVDS Output Data 10—True.
40	D10− (MSB)	Output	Channel A/Channel B LVDS Output Data 10—Complement.
43	OR+	Output	Channel A/Channel B LVDS Overrange—True.
42	OR−	Output	Channel A/Channel B LVDS Overrange—Complement.
25	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
24	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
45	SCLK	Input	SPI Serial Clock. The serial shift clock input, which is used to synchronize serial interface reads and writes.
44	SDIO	Input/Output	SPI Serial Data I/O. A dual purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
46	CSB	Input	Chip Select Bar (Active Low). CSB gates the read and write cycles.
Output Enable Bar and Power-Down			
47	OEB	Input/Output	Output Enable Bar Input (Active Low).
48	PDWN	Input/Output	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby (see Table 14).



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED THERMAL PADDLE ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PADDLE MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

09638-005

Figure 5. Pin Configuration (Top View), LFCSP Channel Multiplexed (Even/Odd) LVDS

Table 9. Pin Function Descriptions for the Channel Multiplexed (Even/Odd) LVDS Mode

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
4, 5, 8, 9, 26, 27, 55, 56, 58	DNC		Do Not Connect. Do not connect to these pins.
0	AGND, Exposed Paddle	Ground	The exposed thermal paddle on the bottom of the package provides the analog ground for the part. This exposed paddle must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs. This pin should be decoupled to ground using a 0.1 µF capacitor.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
7	ORB+	Output	Channel B LVDS Overrange Output—True. The overrange indication is valid on the rising edge of the DCO.
6	ORB−	Output	Channel B LVDS Overrange Output—Complement. The overrange indication is valid on the rising edge of the DCO.
11	B 0/D0− (LSB)	Output	Channel B LVDS Output 0/Data 0—Complement. The output bit on the rising edge of the data clock output (DCO) from this output is always a Logic 0.
12	B 0/D0+ (LSB)	Output	Channel B LVDS Output 0/Data 0—True. The output bit on the rising edge of the data clock output (DCO) from this output is always a Logic 0.

Pin No.	Mnemonic	Type	Description
13	B D1−/D2−	Output	Channel B LVDS Output Data 1/Data 2—Complement.
14	B D1+/D2+	Output	Channel B LVDS Output Data 1/Data 2—True.
15	B D3−/D4−	Output	Channel B LVDS Output Data 3/Data 4—Complement.
16	B D3+/D4+	Output	Channel B LVDS Output Data 3/Data 4—True.
17	B D5−/D6−	Output	Channel B LVDS Output Data 5/Data 6—Complement.
18	B D5+/D6+	Output	Channel B LVDS Output Data 5/Data 6—True.
20	B D7−/D8−	Output	Channel B LVDS Output Data 7/Data 8—Complement.
21	B D7+/D8+	Output	Channel B LVDS Output Data 7/Data 8—True.
22	B D9−/D10− (MSB)	Output	Channel B LVDS Output Data 9/Data 10—Complement.
23	B D9+/D10+ (MSB)	Output	Channel B LVDS Output Data 9/Data 10—True.
29	A 0/D0− (LSB)	Output	Channel B LVDS Output 0/Data 1—Complement. The first output bit from this output is always a Logic 0.
30	A 0/D0+ (LSB)	Output	Channel B LVDS Output 0/Data 1—True. The first output bit from this output is always a Logic 0.
31	A D1−/D2−	Output	Channel A LVDS Output Data 1/Data 0—Complement.
32	A D1+/D2+	Output	Channel A LVDS Output Data 1/Data 0—True.
33	A D3−/D4−	Output	Channel A LVDS Output Data 3/Data 2—Complement.
34	A D3+/D4+	Output	Channel A LVDS Output Data 3/Data 2—True.
35	A D5−/D6−	Output	Channel A LVDS Output Data 5/Data 4—Complement.
36	A D5+/D6+	Output	Channel A LVDS Output Data 5/Data 4—True.
38	A D7−/D8−	Output	Channel A LVDS Output Data 7/Data 6—Complement.
39	A D7+/D8+	Output	Channel A LVDS Output Data 7/Data 6—True.
40	A D9−/D10− (MSB)	Output	Channel A LVDS Output Data 9/Data 8—Complement.
41	A D9+/D10+ (MSB)	Output	Channel A LVDS Output Data 9/Data 8—True.
43	ORA+	Output	Channel A LVDS Overrange Output—True. The overrange indication is valid on the rising edge of the DCO.
42	ORA−	Output	Channel A LVDS Overrange Output—Complement. The overrange indication is valid on the rising edge of the DCO.
25	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
24	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
45	SCLK	Input	SPI Serial Clock (SCKL). The serial shift clock input, which is used to synchronize serial interface reads and writes.
44	SDIO	Input/Output	SPI Serial Data Input/Output (SDIO). A dual purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
46	CSB	Input	SPI Chip Select Bar (Active Low). An active low control that gates the read and write cycles.
Output Enable Bar and Power-Down			
47	OEB	Input	Output Enable Bar Input (Active Low).
48	PDWN	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby (see Table 14).

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, sample rate = maximum sample rate per speed grade, DCS enabled, 1.75 V p-p differential input, VIN = −1.0 dBFS, 32k sample, T_A = 25°C, unless otherwise noted.

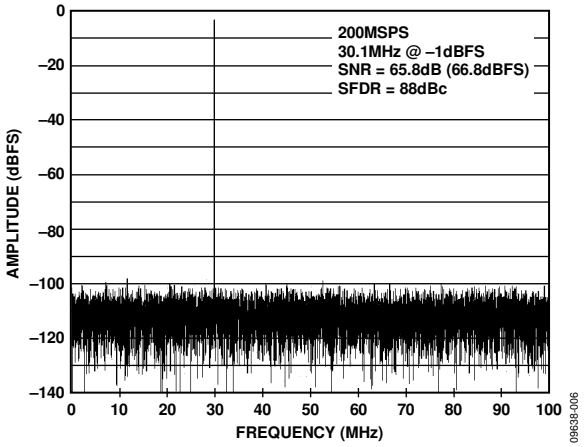


Figure 6. AD6643-200 Single Tone FFT, f_{IN} = 30.1 MHz

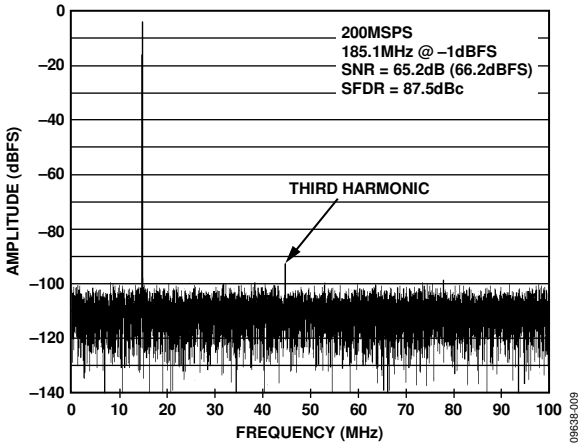


Figure 9. AD6643-200 Single Tone FFT, f_{IN} = 185.1 MHz

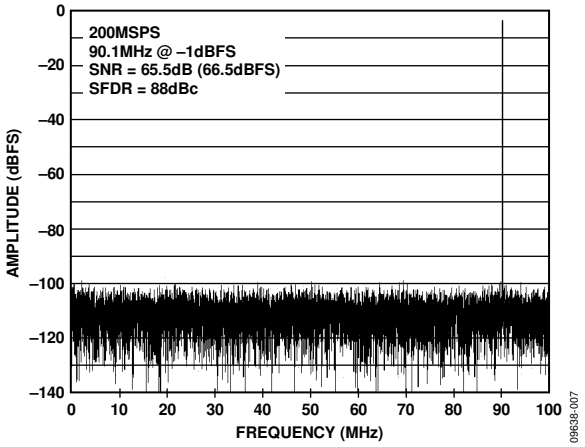


Figure 7. AD6643-200 Single Tone FFT, f_{IN} = 90.1 MHz

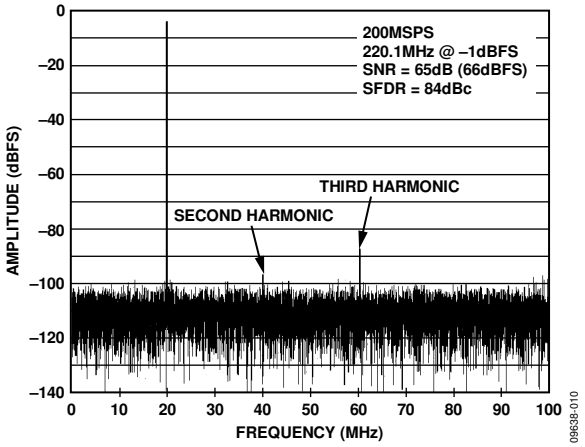


Figure 10. AD6643-200 Single Tone FFT, f_{IN} = 220.1 MHz

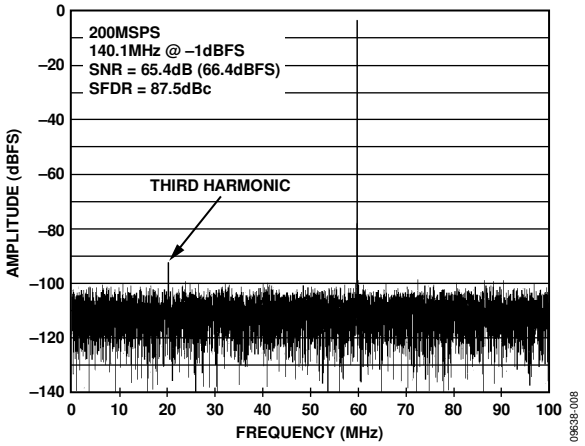


Figure 8. AD6643-200 Single Tone FFT, f_{IN} = 140.1 MHz

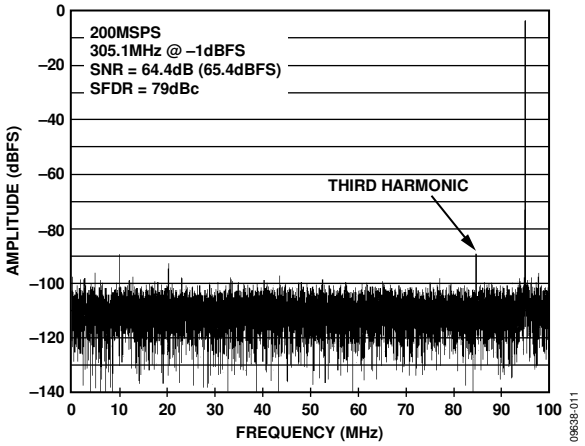


Figure 11. AD6643-200 Single Tone FFT, f_{IN} = 305.1 MHz

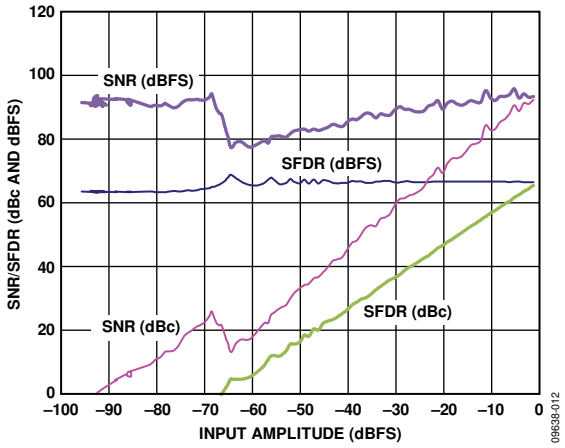


Figure 12. AD6643-200 Single Tone SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 90.1 MHz

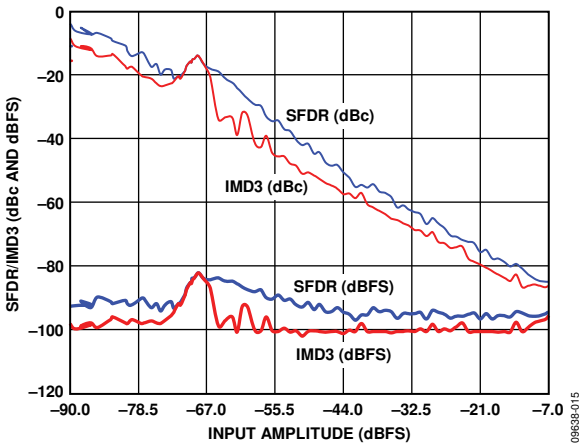


Figure 15. AD6643-200 Two Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz

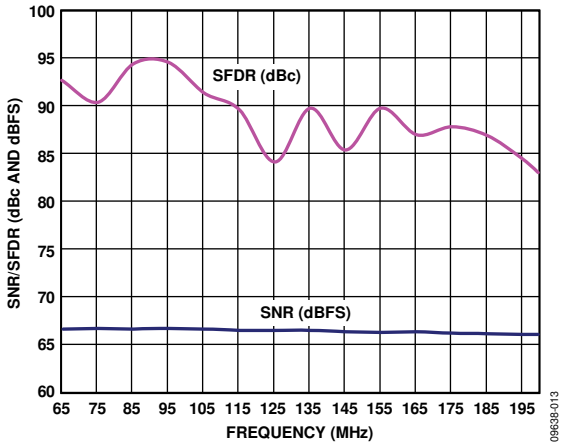


Figure 13. AD6643-200 Single Tone SNR/SFDR vs. Input Frequency (f_{IN})

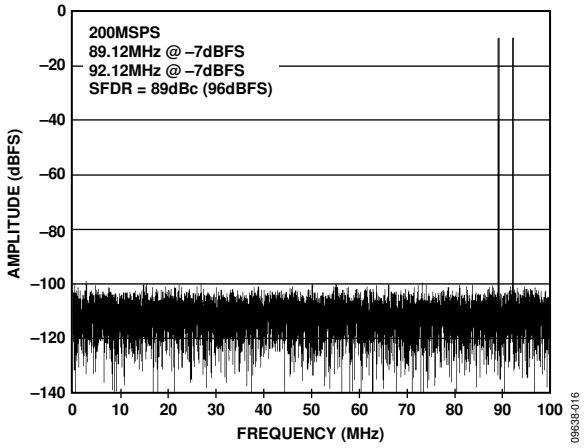


Figure 16. AD6643-200 Two Tone FFT with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz

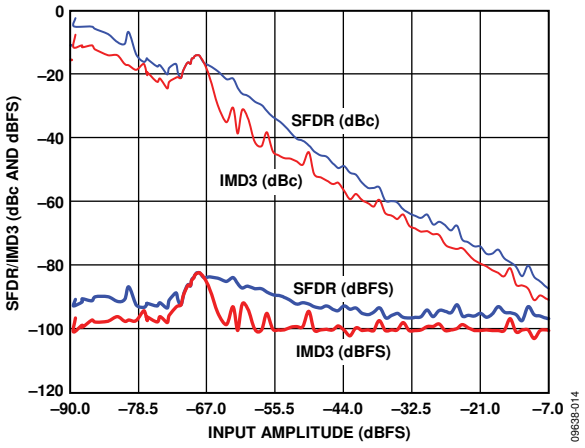


Figure 14. AD6643-200 Two Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz

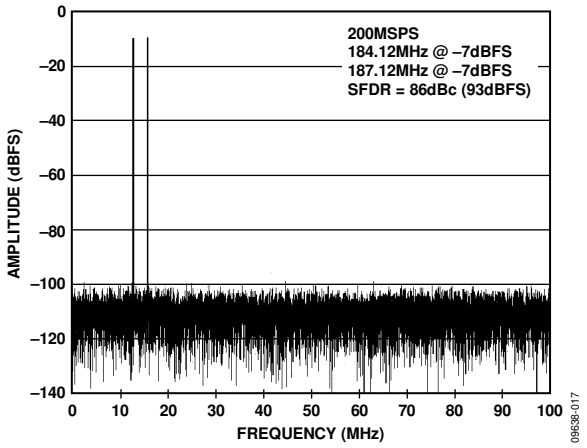


Figure 17. AD6643-200 Two Tone FFT with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz

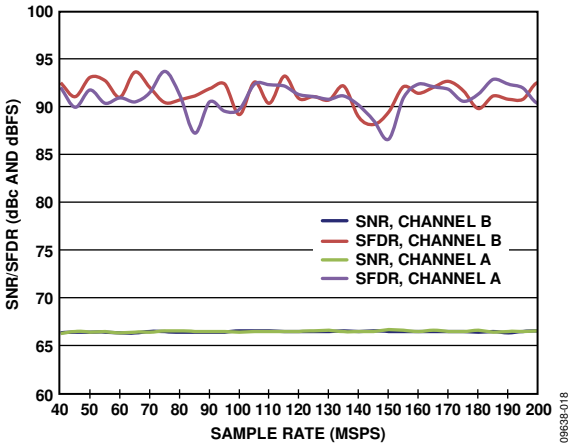


Figure 18. AD6643-200 Single Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90.1 MHz

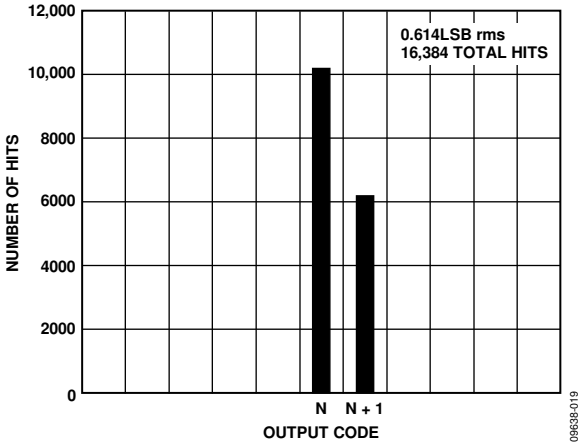


Figure 19. AD6643-200 Grounded Input Histogram

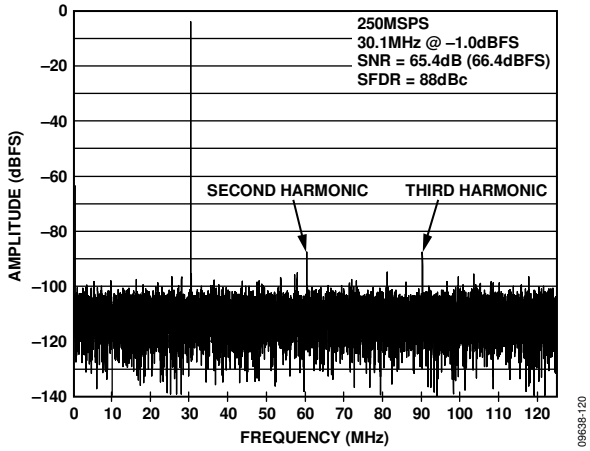


Figure 20. AD6643-250 Single Tone FFT, f_{IN} = 30.1 MHz

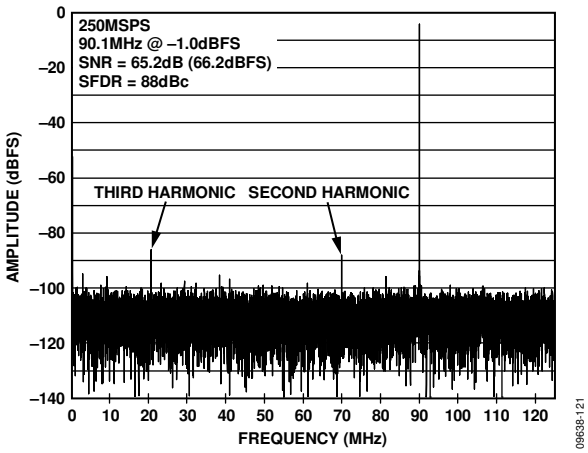


Figure 21. AD6643-250 Single Tone FFT, f_{IN} = 90.1 MHz

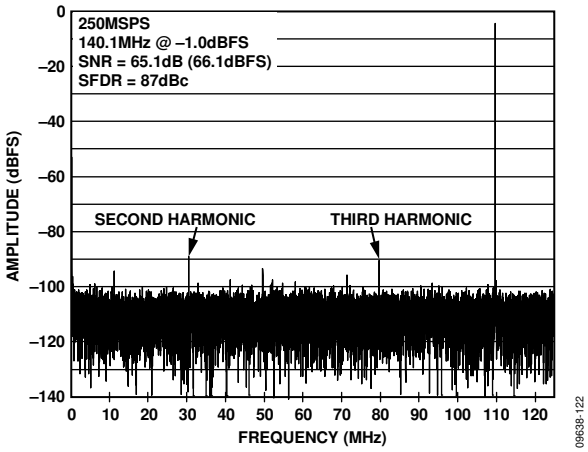


Figure 22. AD6643-250 Single Tone FFT, f_{IN} = 140.1 MHz

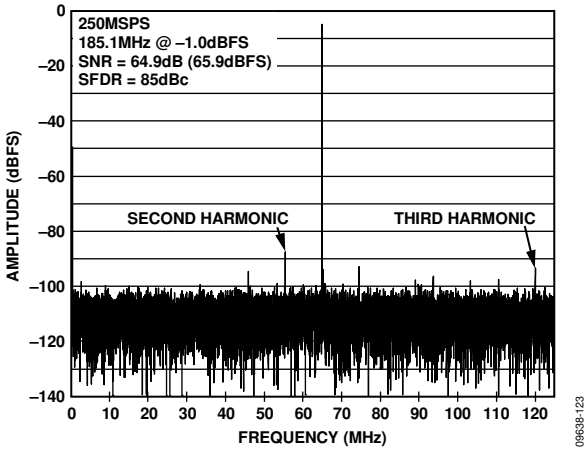


Figure 23. AD6643-250 Single Tone FFT, f_{IN} = 185.1 MHz

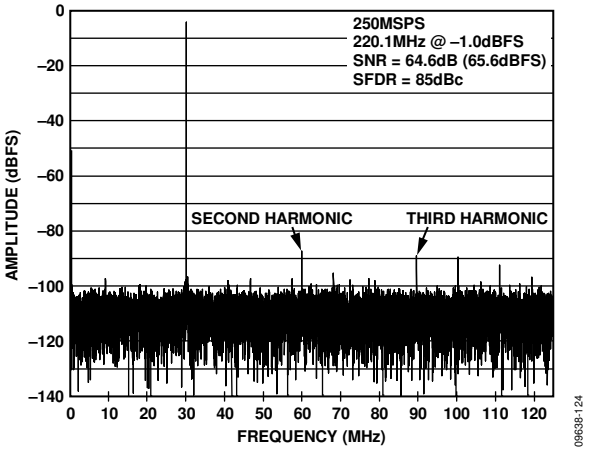


Figure 24. AD6643-250 Single Tone FFT, f_{IN} = 220.1 MHz

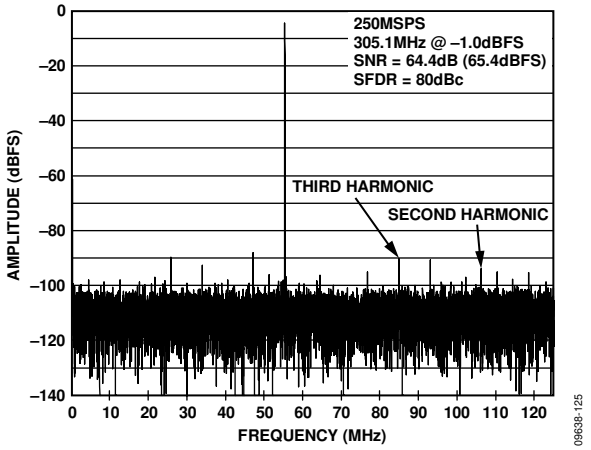


Figure 25. AD6643-250 Single Tone FFT, f_{IN} = 305.1 MHz

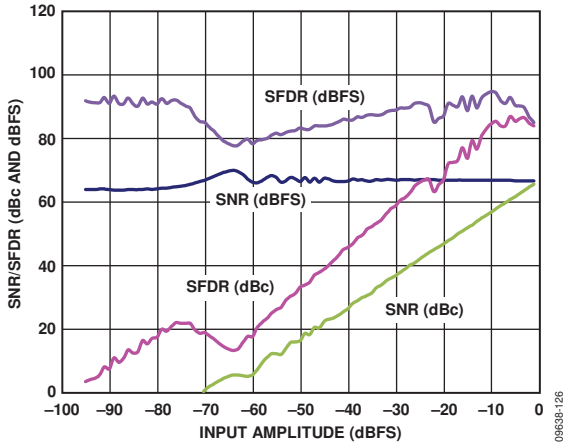


Figure 26. AD6643-250 Single Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 90.1 MHz

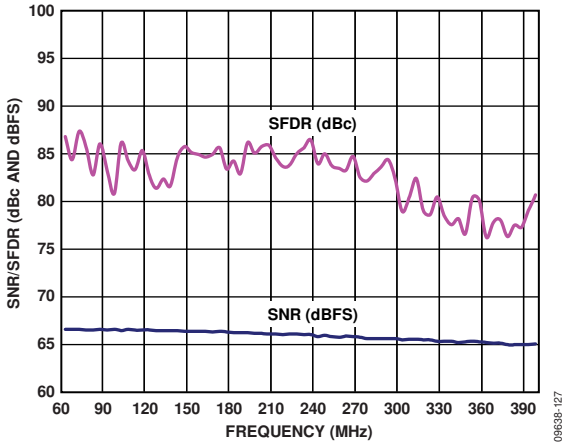


Figure 27. AD6643-250 Single Tone SNR/SFDR vs. Input Frequency (f_{IN}), V_{REF} = 1.75 V p-p

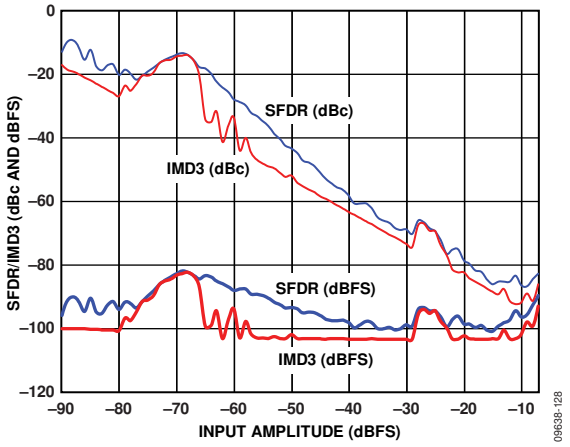


Figure 28. AD6643-250 Two Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz

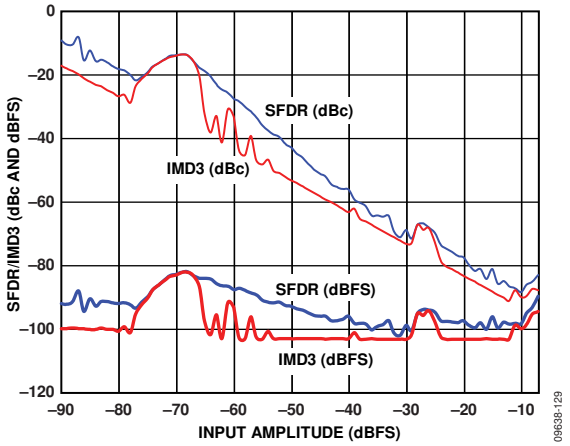


Figure 29. AD6643-250 Two Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz

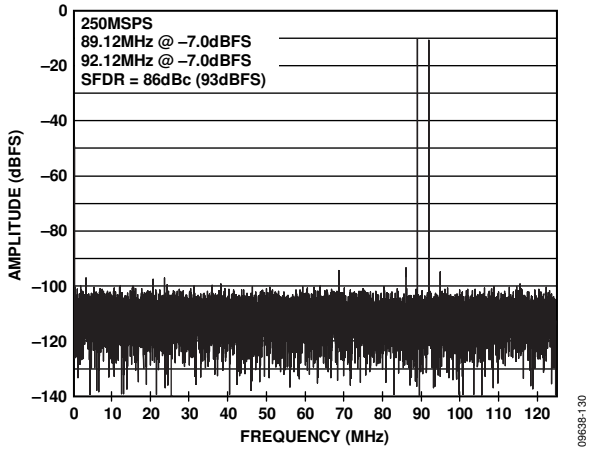


Figure 30. AD6643-250 Two Tone FFT with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz

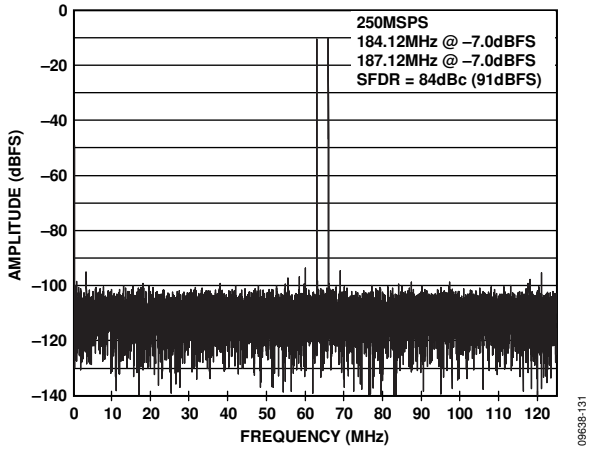


Figure 31. AD6643-250 Two Tone FFT with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz

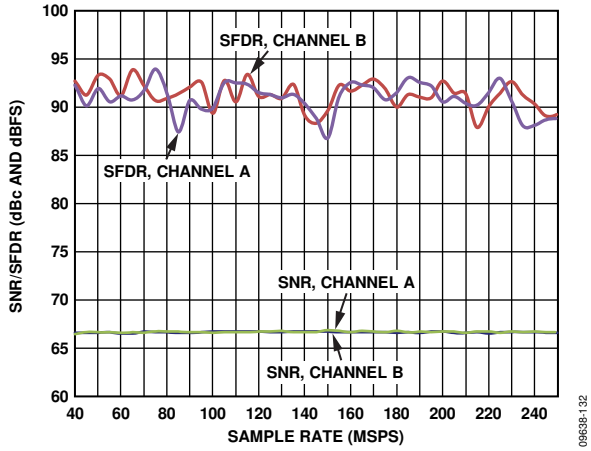


Figure 32. AD6643-250 Single Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90.1 MHz

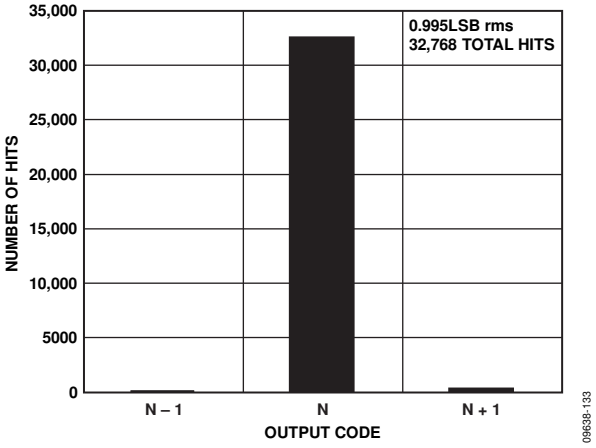


Figure 33. AD6643-250 Grounded Input Histogram

EQUIVALENT CIRCUITS

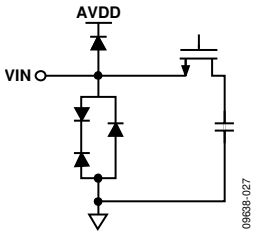


Figure 34. Equivalent Analog Input Circuit

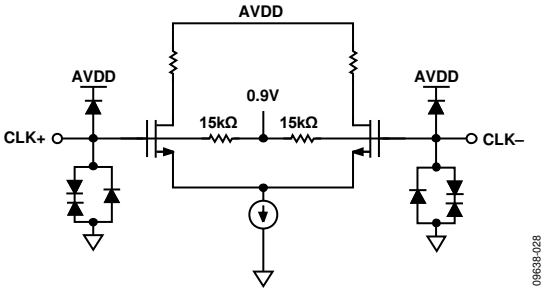


Figure 35. Equivalent Clock Input Circuit

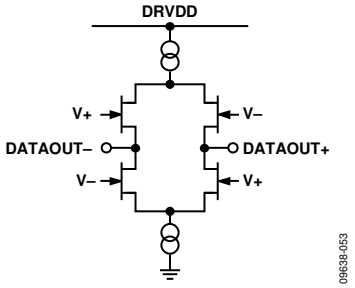


Figure 36. Equivalent LVDS Output Circuit

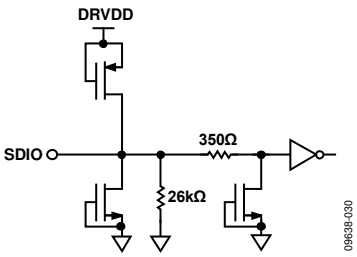


Figure 37. Equivalent SDIO Circuit

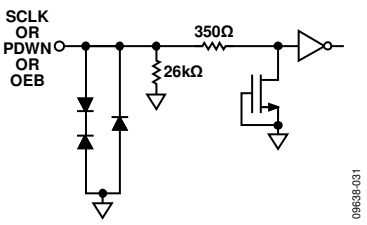


Figure 38. Equivalent SCLK or PDWN or OEB Input Circuit

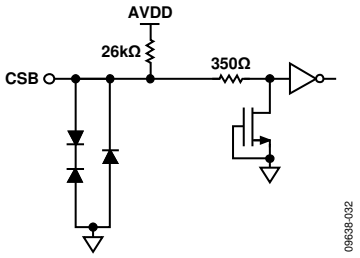


Figure 39. Equivalent CSB Input Circuit

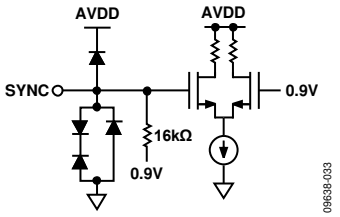


Figure 40. Equivalent SYNC Input Circuit

THEORY OF OPERATION

The AD6643 has two analog input channels and two digital output channels. The intermediate frequency (IF) input signal passes through several stages before appearing at the output port(s).

ADC ARCHITECTURE

The AD6643 architecture consists of dual front-end sample-and-hold circuits, followed by pipelined, switched capacitor ADCs. The quantized outputs from each stage are combined into a final 11-bit result in the digital correction logic. Alternately, the 11-bit result can be processed through the noise shaping requantizer (NSR) block before it is sent to the digital correction logic.

The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of each channel contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output drive current. During power-down, the output buffers enter a high impedance state.

The AD6643 dual IF receiver can simultaneously digitize two channels, making it ideal for diversity reception and digital predistortion (DPD) observation paths in telecommunication systems.

The dual IF receiver design can be used for diversity reception of signals, whereas the ADCs operate identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can input frequencies from dc to 300 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in performance. Operation to 400 MHz analog input is permitted but occurs at the expense of increased ADC noise and distortion.

Synchronization capability is provided to allow synchronized timing between multiple devices.

Programming and control of the AD6643 are accomplished using a 3-wire SPI-compatible serial interface.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD6643 is a differential switched capacitor circuit designed for optimum performance in differential signal processing.

The clock signal alternatively switches the input between sample mode and hold mode (see Figure 41). When the input is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within 1/2 of a clock cycle.

A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, any shunt capacitors placed across the inputs should be reduced. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. For more information, refer to the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters," available at www.analog.com.

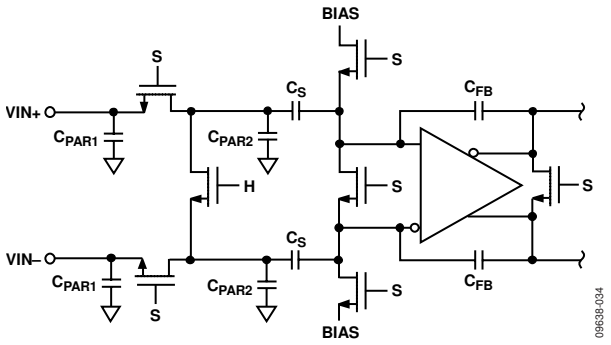


Figure 41. Switched Capacitor Input

For best dynamic performance, match the source impedances driving VIN+ and VIN– and differentially balance the inputs.

Input Common Mode

The analog inputs of the AD6643 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = 0.5 × AVDD (or 0.9 V) is recommended for optimum performance.

An on-board common-mode voltage reference is included in the design and is available from the VCM pin. Using the VCM output to set the input common mode is recommended. Optimum performance is achieved when the common-mode voltage of the analog input is set by the VCM pin voltage (typically 0.5 × AVDD). The VCM pin must be decoupled to ground by a 0.1 µF capacitor, as described in the Applications Information section. Place this

decoupling capacitor close to the VCM pin to minimize series resistance and inductance between the device and this capacitor.

Differential Input Configurations

Optimum performance is achieved by driving the AD6643 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, ADA4930-2, and ADA4938-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4938-2 is easily set with the VCM pin of the AD6643 (see Figure 42), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

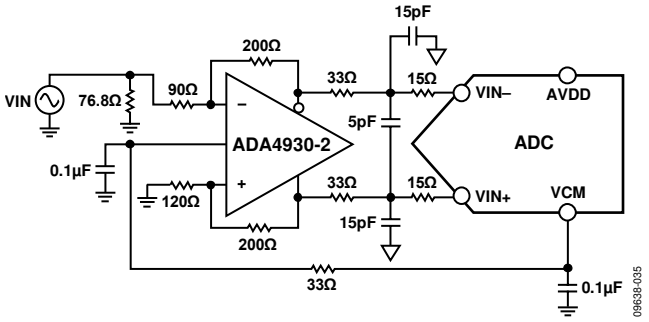


Figure 42. Differential Input Configuration Using the ADA4930-2

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration, as shown in Figure 43. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

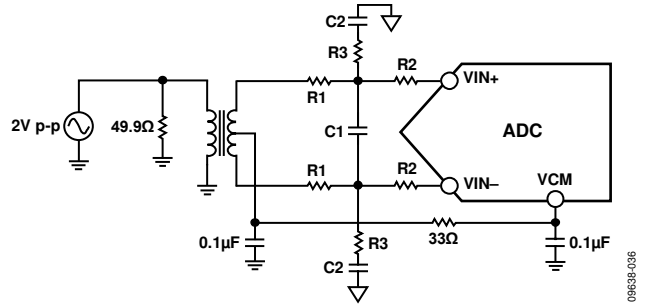


Figure 43. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz (MHz). Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD6643. For applications where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 44). In this configuration, the input is ac-coupled, and the CML is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver.

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance. Based on these parameters the value of the input resistors and capacitors may need to be adjusted, or some components may need to be removed. Table 10 lists recommended values to set the RC network for different input frequency ranges. However, because these values are dependent on the input signal and bandwidth, they are to be used as a starting guide only. Note that the values given in Table 10 are for each R1, R2, C2, and R3 component shown in Figure 43 and Figure 44.

Table 10. Example RC Network

Frequency Range (MHz)	R1 Series (Ω)	C1 Differential (pF)	R2 Series (Ω)	C2 Shunt (pF)	R3 Shunt (Ω)
0 to 100	33	8.2	0	15	49.9
100 to 300	15	3.9	0	8.2	49.9

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use an amplifier with variable gain. The AD8375 or AD8376 digital variable gain amplifiers (DVGAs) provide good performance for driving the AD6643. Figure 45 shows an example of the AD8376 driving the AD6643 through a band-pass antialiasing filter.

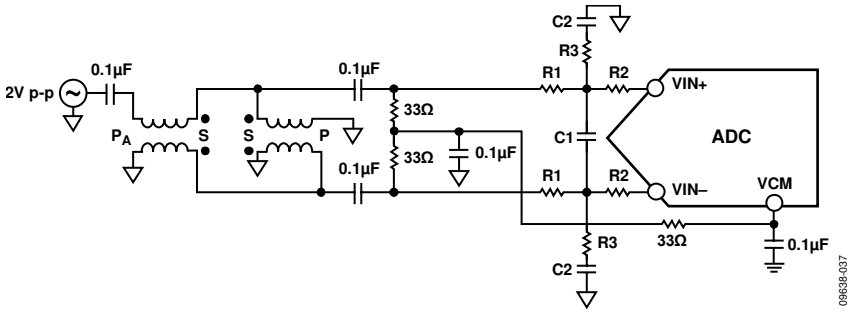


Figure 44. Differential Double Balun Input Configuration

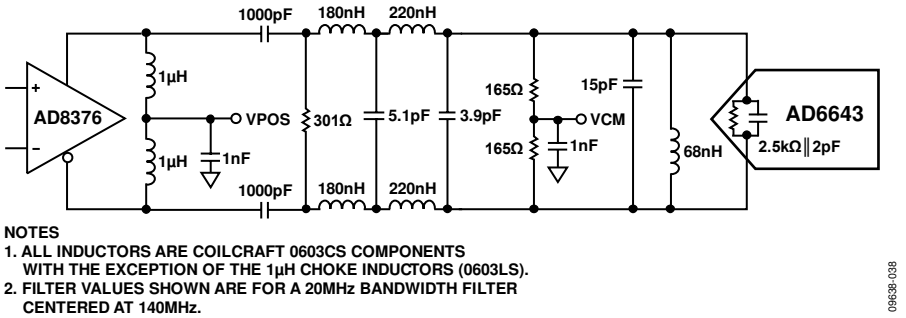


Figure 45. Differential Input Configuration Using the AD8376

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD6643. The full-scale input range can be adjusted by varying the reference voltage via the SPI. The input span of the ADC tracks reference voltage changes linearly.

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD6643 sample clock inputs (CLK+ and CLK−) by using a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally (see Figure 46) and require no external bias. If the inputs are floated, the CLK− pin is pulled low to prevent spurious clocking.

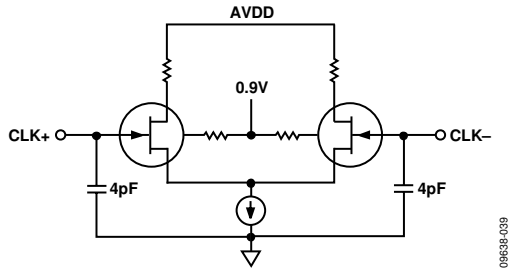


Figure 46. Equivalent Clock Input Circuit

Clock Input Options

The AD6643 has a very flexible clock input structure. Clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section.

Figure 47 and Figure 48 show two preferred methods for clocking the AD6643 (at clock rates of up to 625 MHz). A low jitter clock source is converted from a single-ended signal to a differential signal using an RF balun or RF transformer.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 625 MHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD6643 to approximately 0.8 V p-p differential. This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD6643, yet preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

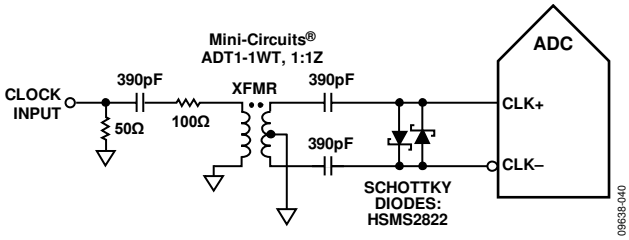


Figure 47. Transformer-Coupled Differential Clock (Up to 200 MHz)

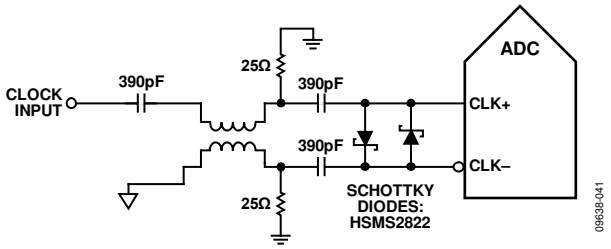


Figure 48. Balun-Coupled Differential Clock (Up to 625 MHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 49. The AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516, AD9517, AD9518, AD9520, AD9522, and the ADCLK905/ADCLK907/ADCLK925, clock drivers offer excellent jitter performance.

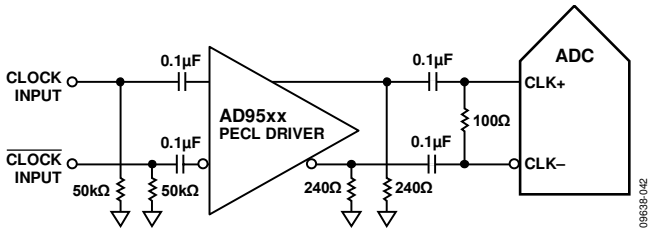


Figure 49. Differential PECL Sample Clock (Up to 625 MHz)

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 50. The AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516, AD9517, AD9518, AD9520, AD9522, AD9523, and AD9524 clock drivers offer excellent jitter performance.

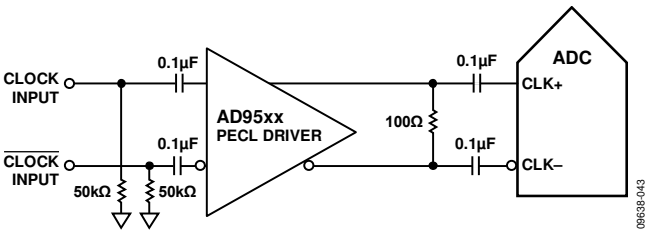


Figure 50. Differential LVDS Sample Clock (Up to 625 MHz)

Input Clock Divider

The AD6643 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8. The duty cycle stabilizer (DCS) is enabled by default on power-up.

The AD6643 clock divider can be synchronized using the external SYNC input. Bit 1 and Bit 2 of Register 0x3A allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD6643 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, thereby providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD6643.

Jitter on the rising edge of the input clock is of paramount concern and is not reduced by the duty cycle stabilizer. The duty cycle control loop does not function for clock rates of less than 40 MHz nominally. The loop has a time constant associated with it that must be considered when the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time period that the loop is not locked, the DCS loop is bypassed, and internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the DCS. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{IN}) due to jitter (t_J) can be calculated by

$$SNR_{HF} = -10\log[(2\pi \times f_{IN} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the root mean square of all jitter sources, which include the clock input, the analog input signal, and the ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter, as shown in Figure 51.

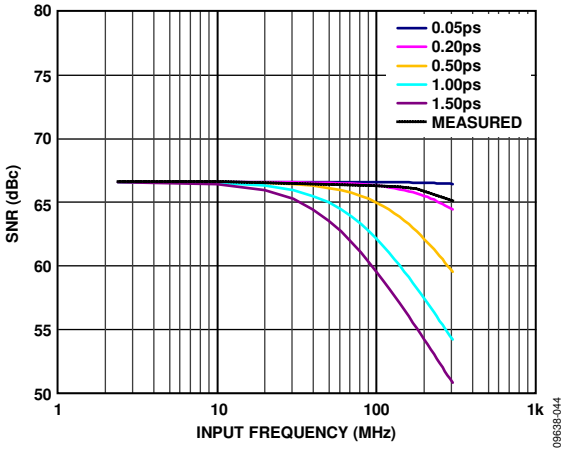


Figure 51. SNR vs. Input Frequency and Jitter

In cases where aperture jitter may affect the dynamic range of the AD6643, treat the clock input as an analog signal. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance*, and the AN-756 Application Note, *Sample Systems and the Effects of Clock Phase Noise and Jitter*, for more information about jitter performance as it relates to ADCs (see www.analog.com).

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 52, the power dissipated by the AD6643 is proportional to its sample rate. The data in Figure 52 was taken using the same operating conditions as those used for the Typical Performance Characteristics.

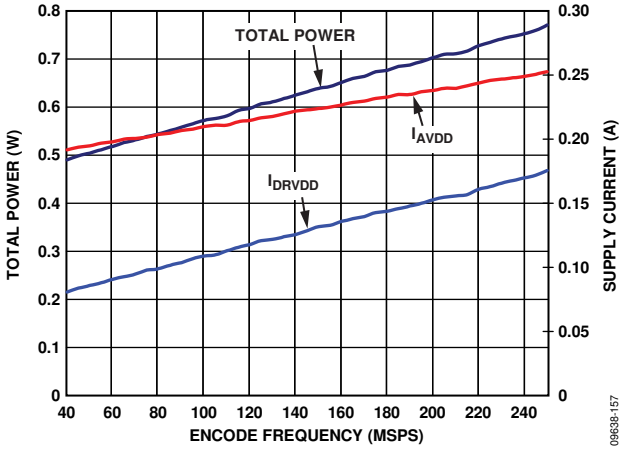


Figure 52. AD6643 Power and Current vs. Sample Rate

By asserting PDWN (either through the SPI port or by asserting the PDWN pin high), the AD6643 is placed in power-down mode. In this state, the ADC typically dissipates 10 mW. During