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ANALOG DEVICES

IF Diversity Receiver

Data Sheet **AD6649**

FEATURES

- SNR = 73.0 dBFS in a 95 MHz bandwidth at 185 MHz A_{IN} and 245.76 MSPS
- SFDR = 85 dBc at 185 MHz A_{IN} and 250 MSPS
- Noise density = −151.2 dBFS/Hz input at 185 MHz, −1 dBFS A_{IN} and 250 MSPS
- Total power consumption: 1 W with fixed-frequency NCO, 95 MHz FIR filter
- 1.8 V supply voltages
- LVDS (ANSI-644 levels) outputs
- Integer 1-to-8 input clock divider (625 MHz maximum input)
- Integrated dual-channel ADC
  - Sample rates of up to 250 MSPS
  - IF sampling frequencies to 400 MHz
  - Internal ADC voltage reference
  - Flexible input range
    - 1.4 V p-p to 2.1 V p-p (1.75 V p-p nominal)
  - ADC clock duty cycle stabilizer
  - 95 dB channel isolation/crosstalk
- Integrated wideband digital processor
  - 32-bit complex numerically controlled oscillator (NCO)
  - FIR filter with 2 modes
  - Real output from an f_S/4 output NCO
- Amplitude detect bits for efficient AGC implementation
- Energy saving power-down modes
- Decimated, interleaved real LVDS data outputs

APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers (3G)
  - TD-SCDMA, WiMax, WCDMA,
    - CDMA2000, GSM, EDGE, LTE
- General-purpose software radios
- Broadband data applications

GENERAL DESCRIPTION

The AD6649 is a mixed-signal intermediate frequency (IF) receiver consisting of dual 14-bit, 250 MSPS ADCs and a wideband digital downconverter (DDC). The AD6649 is designed to support communications applications, where low cost, small size, wide bandwidth, and versatility are desired.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

FUNCTIONAL BLOCK DIAGRAM

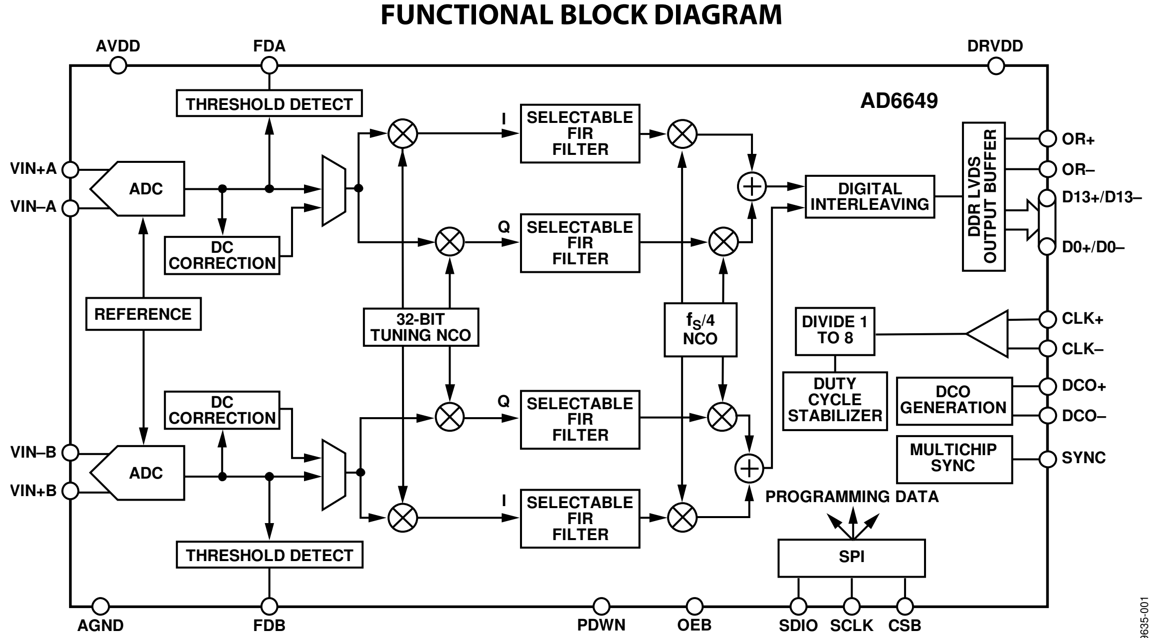

Figure 1.

Rev. C **Document Feedback**

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Technical Support www.analog.com

AD6649* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD6649 Evaluation Board
- AD9643 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-586: LVDS Outputs for High Speed A/D Converters
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD6649: IF Diversity Receiver Data Sheet

User Guides

- UG-293: Evaluating the AD9643/AD9613/AD6649/AD6643 Analog-to-Digital Converters

TOOLS AND SIMULATIONS

- Visual Analog
- AD6649 IBIS Model
- AD6649 LFCSP Analog Input S-Parameter

DESIGN RESOURCES

- AD6649 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD6649 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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4/11—Revision 0: Initial Version

ADC data outputs are internally connected directly to the digital downconverter (DDC) of the receiver. The digital receiver has two channels and provides processing flexibility. Each receive channel has four cascaded signal processing stages: a 32-bit frequency translator (numerically controlled oscillator (NCO)), an optional sample rate converter, a fixed FIR filter, and an $f_S/4$ fixed-frequency NCO.

In addition to the receiver DDC, the AD6649 has several functions that simplify the automatic gain control (AGC) function in the system receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

After digital processing, data is routed directly to the 14-bit output port. These outputs operate at ANSI or reduced swing LVDS signal levels.

The AD6649 receiver digitizes a wide spectrum of IF frequencies. Each receiver is designed for simultaneous reception of the main channel and the diversity channel. This IF sampling architecture greatly reduces component cost and complexity compared with traditional analog techniques or less integrated digital methods. In diversity applications, the output data format is real due to the final NCO, which shifts the output center frequency to $f_S/4$.

Flexible power-down options allow significant power savings, when desired.

Programming for setup and control is accomplished using a 3-pin SPI-compatible serial interface.

The AD6649 is available in a 64-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Integrated dual, 14-bit, 250 MSPS ADCs.
2. Integrated wideband filter and 32-bit complex NCO.
3. Fast overrange and threshold detect.
4. Proprietary differential input maintains excellent SNR performance for input frequencies of up to 400 MHz.
5. SYNC input allows synchronization of multiple devices.
6. 3-pin, 1.8 V SPI port for register programming and register readback.

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input,[1] 1.75 V p-p full-scale input range, duty cycle stabilizer (DCS) enabled, NCO enabled, FIR filter enabled, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	Full	14			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full			±10	mV
Gain Error	Full	−5.5		+2.5	%FSR
MATCHING CHARACTERISTIC					
Offset Error	Full			±13	mV
Gain Error	Full			±2.5	%FSR
TEMPERATURE DRIFT					
Offset Error	Full		±5		ppm/°C
Gain Error	Full		±100		ppm/°C
INPUT REFERRED NOISE					
VREF = 1.75 V	25°C		1.32		LSB rms
ANALOG INPUT					
Input Span	Full		1.75		V p-p
Input Capacitance[2]	Full		2.5		pF
Input Resistance[3]	Full		20		kΩ
Input Common-Mode Voltage	Full		0.9		V
POWER SUPPLIES					
Supply Voltage					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
Supply Current					
I_{AVDD}[4]	Full		271	275	mA
I_{DRVDD}[4] (Fixed-Frequency NCO, 95 MHz FIR Filter)	Full		283	300	mA
I_{DRVDD}[4] (Tunable-Frequency NCO, 100 MHz FIR Filter)	Full		375		mA
POWER CONSUMPTION					
Sine Wave Input (Fixed-Frequency NCO, 95 MHz FIR Filter)	Full		997	1035	mW
Sine Wave Input (Tunable-Frequency NCO, 100 MHz FIR Filter)	Full		1163		mW
Standby Power[5]	Full		104		mW
Power-Down Power	Full		10		mW

[1] A −1.0 dBFS input level at the analog inputs corresponds to an output level of −2.5 dBFS when using the fixed-frequency NCO and 95 MHz FIR filter. When using the tunable-frequency NCO and 100 MHz FIR filter, the output level is −1.3 dBFS. These respective output level reductions are due to FIR filter losses. See the FIR Filters section for more details.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND.
[3] Input resistance refers to the effective resistance between one differential input pin and its complement.
[4] Measured with a 185 MHz, full-scale sine wave input on both channels and an NCO frequency of 62.5 MHz (f_S/4).
[5] Standby power is measured with a dc input and the CLK pin inactive (set to AVDD or AGND).

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input,[1] 1.75 V p-p full-scale input range, DCS enabled, NCO enabled, FIR filter enabled, unless otherwise noted.

Table 2.

Parameter[2]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)[3]					
f_{IN} = 30 MHz	25°C		74.5		dBFS
f_{IN} = 90 MHz	25°C		74.1		dBFS
f_{IN} = 140 MHz	25°C		73.6		dBFS
f_{IN} = 185 MHz	25°C		73.0		dBFS
	Full	70.9			dBFS
f_{IN} = 220 MHz	25°C		72.4		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)					
f_{IN} = 30 MHz	25°C		71.9		dBFS
f_{IN} = 90 MHz	25°C		71.5		dBFS
f_{IN} = 140 MHz	25°C		70.8		dBFS
f_{IN} = 185 MHz	25°C		70.3		dBFS
	Full	68.7			dBFS
f_{IN} = 220 MHz	25°C		69.6		dBFS
WORST SECOND OR THIRD HARMONIC					
f_{IN} = 30 MHz	25°C		−92		dBc
f_{IN} = 90 MHz	25°C		−88		dBc
f_{IN} = 140 MHz	25°C		−85		dBc
f_{IN} = 185 MHz	25°C		−85		dBc
	Full			−80	dBc
f_{IN} = 220 MHz	25°C		−89		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 30 MHz	25°C		92		dBc
f_{IN} = 90 MHz	25°C		88		dBc
f_{IN} = 140 MHz	25°C		85		dBc
f_{IN} = 185 MHz	25°C		85		dBc
	Full	80			
f_{IN} = 220 MHz	25°C		84		dBc
WORST OTHER HARMONIC OR SPUR					
f_{IN} = 30 MHz	25°C		−95		dBc
f_{IN} = 90 MHz	25°C		−94		dBc
f_{IN} = 140 MHz	25°C		−93		dBc
f_{IN} = 185 MHz	25°C		−93		dBc
	Full			−80	dBc
f_{IN} = 220 MHz	25°C		−84		dBc
TWO-TONE SFDR					
f_{IN} = 184.12 MHz, 187.12 MHz (−7 dBFS)	25°C		88		dBc
CROSSTALK[4]	Full		95		dB
ANALOG INPUT BANDWIDTH	25°C		1000		MHz

[1] A −1.0 dBFS input level at the analog inputs corresponds to an output level of −2.5 dBFS when using the fixed-frequency NCO and 95 MHz FIR filter. When using the tunable-frequency NCO and 100 MHz FIR filter, the output level is −1.3 dBFS. These respective output level reductions are due to FIR filter losses. See the FIR Filters section for more details.
[2] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[3] SNR specifications are for filtered 95 MHz bandwidth.
[4] Crosstalk is measured at 100 MHz with −1 dBFS on one channel and with no input on the alternate channel.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input,[1] 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	+10		+22	µA
Low Level Input Current	Full	−22		−10	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
SYNC INPUT					
Logic Compliance			CMOS/LVDS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
High Level Input Voltage	Full	1.2		AVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−5		+5	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ
LOGIC INPUT (CSB)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−80		−45	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK)[3]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		70	µA
Low Level Input Current	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT/OUTPUT (SDIO)[3]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		70	µA
Low Level Input Current	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF

Parameter	Temperature	Min	Typ	Max	Unit
LOGIC INPUTS (OEB, PDWN)[3]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		70	µA
Low Level Input Current	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS					
FDA and FDB					
High Level Output Voltage					
I_{OH} = 50 µA	Full	1.79			V
I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage					
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V
LVDS Data and OR Outputs					
Differential Output Voltage (V_{OD}), ANSI Mode	Full	250	350	450	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.15	1.22	1.35	V
Differential Output Voltage (V_{OD}), Reduced Swing Mode	Full	150	200	280	mV
Output Offset Voltage (V_{OS}), Reduced Swing Mode	Full	1.15	1.22	1.35	V

[1] A −1.0 dBFS input level at the analog inputs corresponds to an output level of −2.5 dBFS when using the fixed-frequency NCO and 95 MHz FIR filter. When using the tunable-frequency NCO and 100 MHz FIR filter, the output level is −1.3 dBFS. These respective output level reductions are due to FIR filter losses. See the FIR Filters section for more details.
[2] Pull-up.
[3] Pull-down.

SWITCHING SPECIFICATIONS

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS					
Input Clock Rate	Full			625	MHz
Conversion Rate[1]	Full	40		250	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	4.0			ns
CLK Pulse Width High (t_{CH})					
Divide-by-1 Mode, DCS Enabled	Full	1.8	2.0	2.2	ns
Divide-by-1 Mode, DCS Disabled	Full	1.9	2.0	2.1	ns
Divide-by-3 Through Divide-by-8 Modes, DCS Enabled	Full	0.8			ns
DATA OUTPUT PARAMETERS (DATA, OR)					
Data Propagation Delay (t_{PD})	Full		6.0		ns
DCO Propagation Delay (t_{DCO})	Full		6.7		ns
DCO-to-Data Skew (t_{SKEW})	Full	0.4	0.7	1.0	ns
Pipeline Delay—Fixed-Frequency NCO, 95 MHz FIR Filter (Latency)	Full		23		Cycles
Pipeline Delay—Tunable-Frequency NCO, 100 MHz FIR Filter (Latency)	Full		43		Cycles
Aperture Delay (t_A)	Full		1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1		ps rms
Wake-Up Time (from Standby)	Full		10		μs
Wake-Up Time (from Power-Down)	Full		250		μs
OUT-OF-RANGE RECOVERY TIME	Full		3		Cycles

[1] Conversion rate is the clock rate after the divider.

TIMING SPECIFICATIONS

Table 5.

Parameter	Conditions	Min	Typ	Max	Unit
SYNC TIMING REQUIREMENTS					
t_{SSYNC}	SYNC to the rising edge of CLK setup time		0.3		ns
t_{HSYNC}	SYNC to the rising edge of CLK hold time		0.4		ns
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK should be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK should be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns

Timing Diagrams

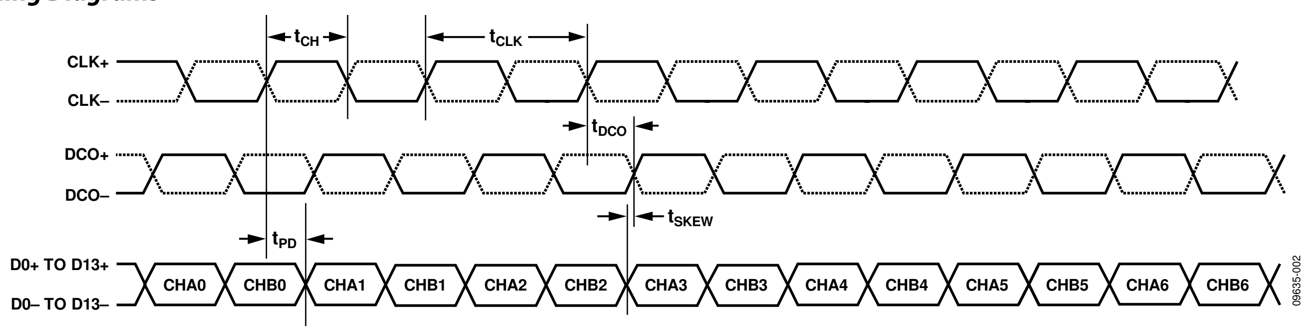


Figure 2. Interleaved LVDS Mode Data Output Timing

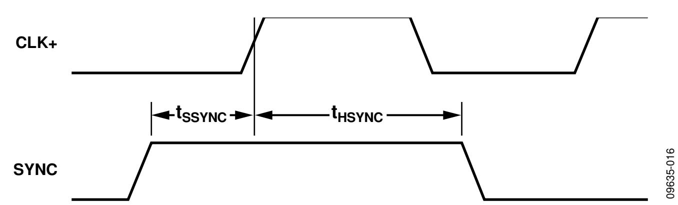


Figure 3. SYNC Timing Inputs

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.3 V
SCLK to AGND	−0.3 V to DRVDD + 0.3 V
SDIO to AGND	−0.3 V to DRVDD + 0.3 V
OEB to AGND	−0.3 V to DRVDD + 0.3 V
PDWN to AGND	−0.3 V to DRVDD + 0.3 V
D0−/D0+ through D13−/D13+ to AGND	−0.3 V to DRVDD + 0.3 V
FDA/FDB to AGND	−0.3 V to DRVDD + 0.3 V
OR+/OR− to AGND	−0.3 V to DRVDD + 0.3 V
DCO+/DCO− to AGND	−0.3 V to DRVDD + 0.3 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC}[1,3]	θ_{JB}[1,4]	Unit
64-Lead LFCSP 9 mm × 9 mm (CP-64-4)	0	26.8	1.14	10.4	°C/W
	1.0	21.6			°C/W
	2.0	20.2			°C/W

[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with solid ground plane. As shown in Table 7, airflow increases heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

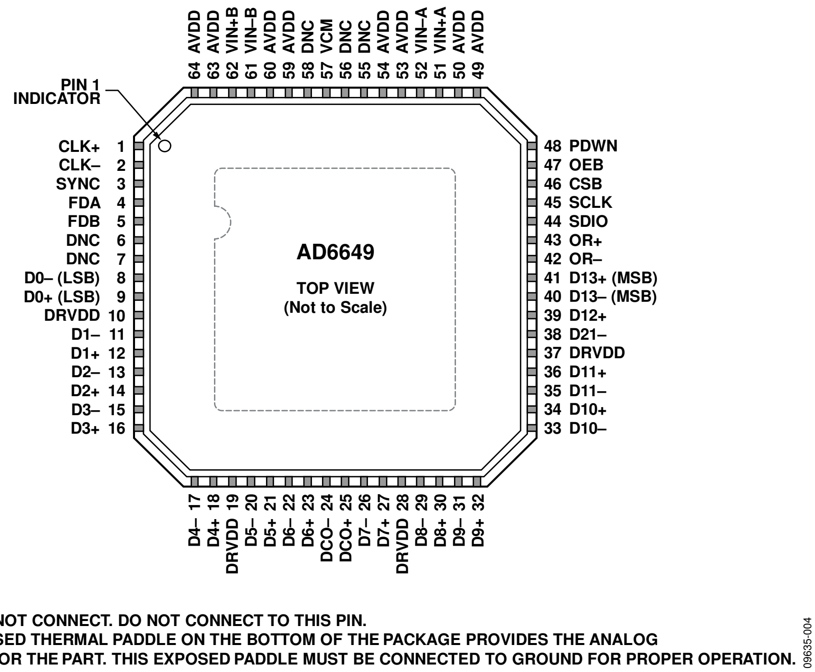


Figure 4. LFCSP Interleaved Parallel LVDS Pin Configuration (Top View)

Table 8. Pin Function Descriptions (Interleaved Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
6, 7, 55, 56, 58	DNC		Do Not Connect. Do not connect to this pin.
0	AGND, Exposed Paddle	Ground	Analog Ground. The exposed thermal paddle on the bottom of the package provides the analog ground for the part. This exposed paddle must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs. This pin should be decoupled to ground using a 0.1 μF capacitor.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.
ADC Fast Detect Outputs			
4	FDA	Output	Channel A Fast Detect Indicator (CMOS Levels).
5	FDB	Output	Channel B Fast Detect Indicator (CMOS Levels).
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
9	D0+ (LSB)	Output	Channel A/Channel B LVDS Output Data 0—True.
8	D0− (LSB)	Output	Channel A/Channel B LVDS Output Data 0—Complement.
12	D1+	Output	Channel A/Channel B LVDS Output Data 1—True.
11	D1−	Output	Channel A/Channel B LVDS Output Data 1—Complement.
14	D2+	Output	Channel A/Channel B LVDS Output Data 2—True.
13	D2−	Output	Channel A/Channel B LVDS Output Data 2—Complement.
16	D3+	Output	Channel A/Channel B LVDS Output Data 3—True.

Pin No.	Mnemonic	Type	Description
15	D3−	Output	Channel A/Channel B LVDS Output Data 3—Complement.
18	D4+	Output	Channel A/Channel B LVDS Output Data 4—True.
17	D4−	Output	Channel A/Channel B LVDS Output Data 4—Complement.
21	D5+	Output	Channel A/Channel B LVDS Output Data 5—True.
20	D5−	Output	Channel A/Channel B LVDS Output Data 5—Complement.
23	D6+	Output	Channel A/Channel B LVDS Output Data 6—True.
22	D6−	Output	Channel A/Channel B LVDS Output Data 6—Complement.
27	D7+	Output	Channel A/Channel B LVDS Output Data 7—True.
26	D7−	Output	Channel A/Channel B LVDS Output Data 7—Complement.
30	D8+	Output	Channel A/Channel B LVDS Output Data 8—True.
29	D8−	Output	Channel A/Channel B LVDS Output Data 8—Complement.
32	D9+	Output	Channel A/Channel B LVDS Output Data 9—True.
31	D9−	Output	Channel A/Channel B LVDS Output Data 9—Complement.
34	D10+	Output	Channel A/Channel B LVDS Output Data 10—True.
33	D10−	Output	Channel A/Channel B LVDS Output Data 10—Complement.
36	D11+	Output	Channel A/Channel B LVDS Output Data 11—True.
35	D11−	Output	Channel A/Channel B LVDS Output Data 11—Complement.
39	D12+	Output	Channel A/Channel B LVDS Output Data 12—True.
38	D12−	Output	Channel A/Channel B LVDS Output Data 12—Complement.
41	D13+ (MSB)	Output	Channel A/Channel B LVDS Output Data 13—True.
40	D13− (MSB)	Output	Channel A/Channel B LVDS Output Data 13—Complement.
43	OR+	Output	Channel A/Channel B LVDS Overrange—True.
42	OR−	Output	Channel A/Channel B LVDS Overrange—Complement.
25	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
24	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
45	SCLK	Input	SPI Serial Clock.
44	SDIO	Input/Output	SPI Serial Data Input/Output.
46	CSB	Input	SPI Chip Select (Active Low).
Output Enable Bar and Power-Down			
47	OEB	Input/Output	Output Enable Bar Input (Active Low).
48	PDWN	Input/Output	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby (see Table 15).

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, sample rate = 250 MSPS, DCS enabled, 1.75 V p-p differential input, VIN = −1.0 dBFS, 32k sample, T_A = 25°C, fixed-frequency NCO, 95 MHz BW FIR filter, unless otherwise noted. In the FFT plots that follow, the location of the second and third harmonics is noted when they fall in the pass band of the filter. A −1.0 dBFS input level at the analog inputs corresponds to an output level of −2.5 dBFS when using the fixed-frequency NCO and 95 MHz FIR filter. When using the tunable-frequency NCO and 100 MHz FIR filter, the output level is −1.3 dBFS. These respective output level reductions are due to FIR filter losses. See the FIR Filters section for more details.

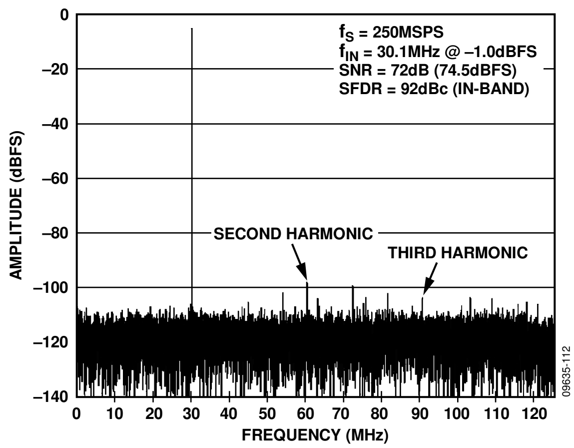


Figure 5. AD6649 Single-Tone FFT with f_{IN} = 30.1 MHz

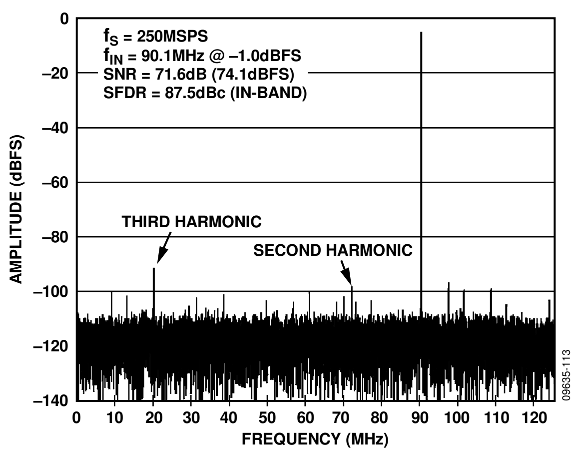


Figure 6. AD6649 Single-Tone FFT with f_{IN} = 90.1 MHz

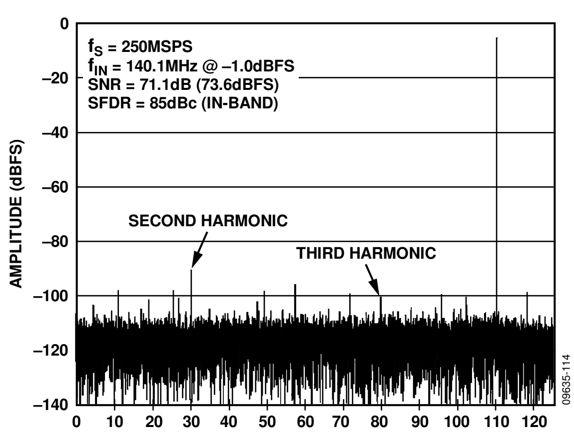


Figure 7. AD6649 Single-Tone FFT with f_{IN} = 140.1 MHz

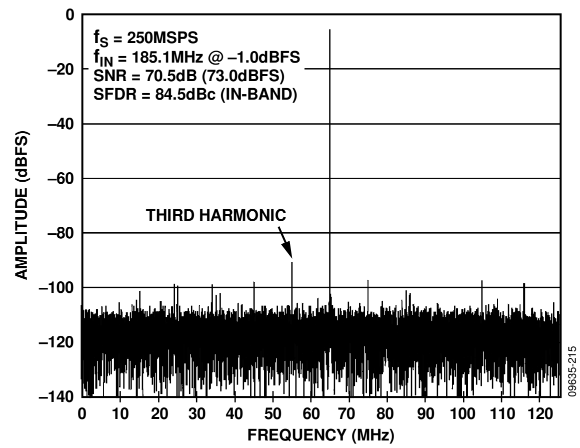


Figure 8. AD6649 Single-Tone FFT with f_{IN} = 185.1 MHz

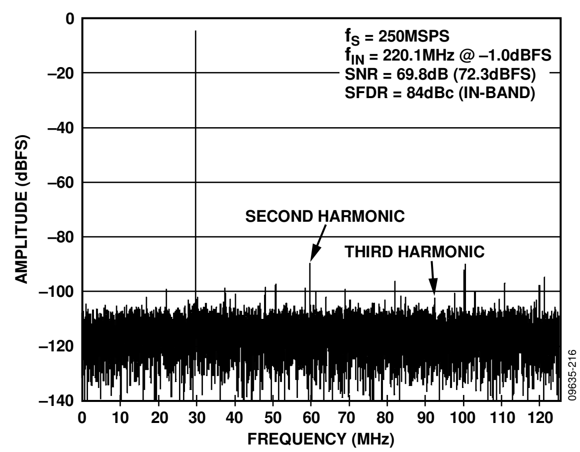


Figure 9. AD6649 Single-Tone FFT with f_{IN} = 220.1 MHz

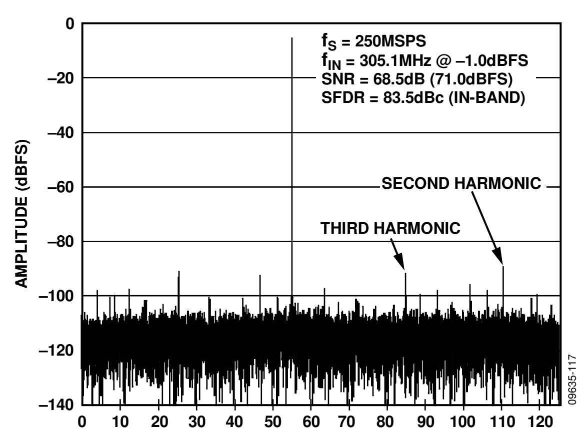


Figure 10. AD6649 Single-Tone FFT with f_{IN} = 305.1 MHz

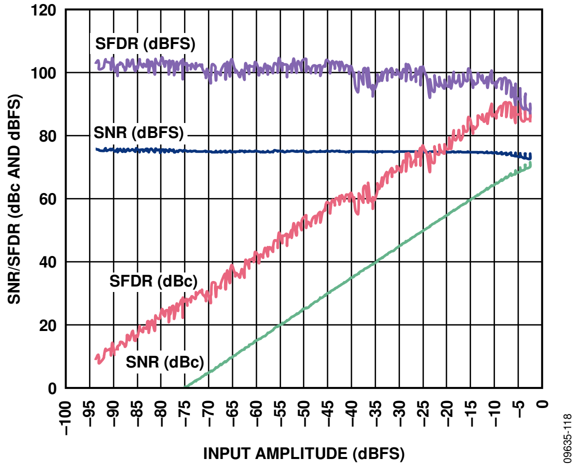


Figure 11. AD6649 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 90.1 MHz

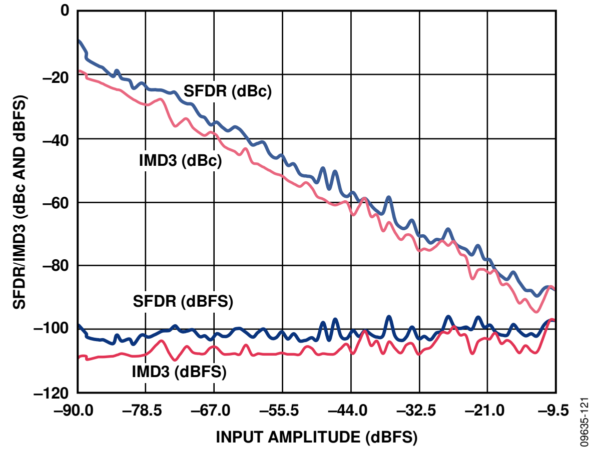


Figure 14. AD6649 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 250 MSPS

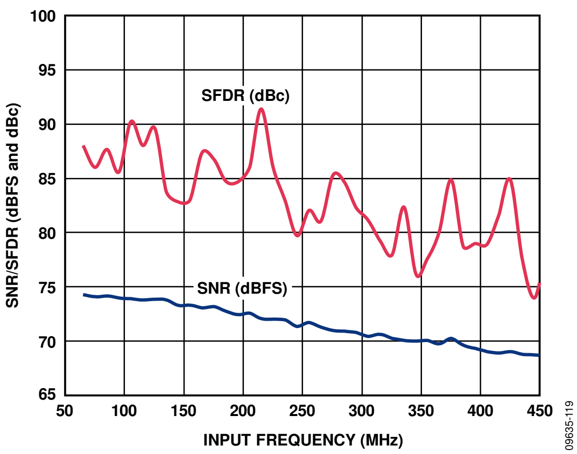


Figure 12. AD6649 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN})

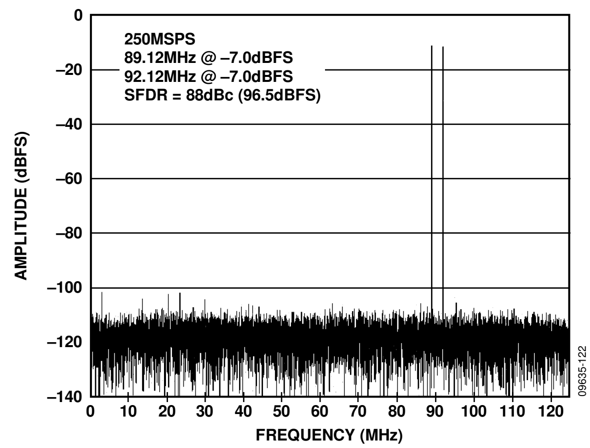


Figure 15. AD6649 Two-Tone FFT with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 250 MSPS

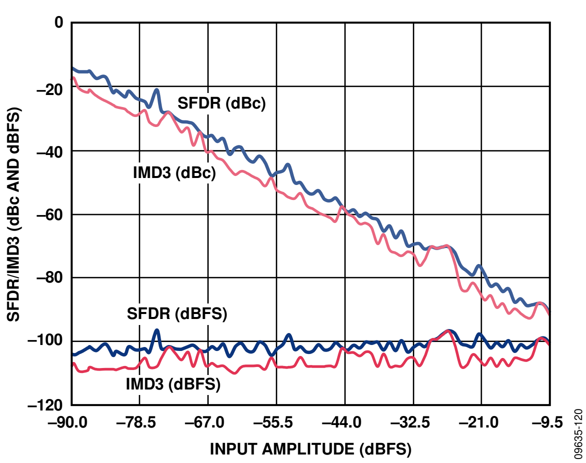


Figure 13. AD6649 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 250 MSPS

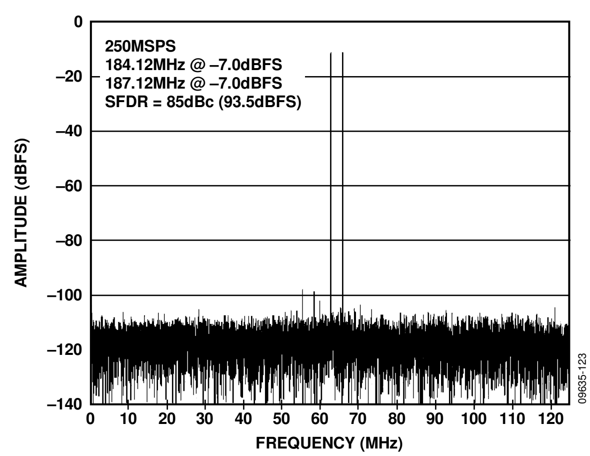


Figure 16. AD6649 Two-Tone FFT with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 250 MSPS

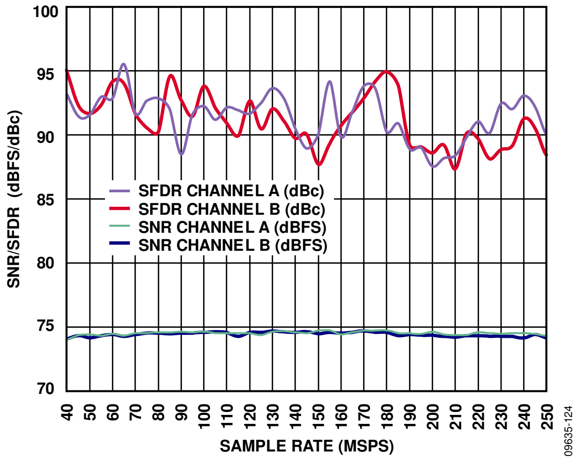


Figure 17. AD6649 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90.1 MHz

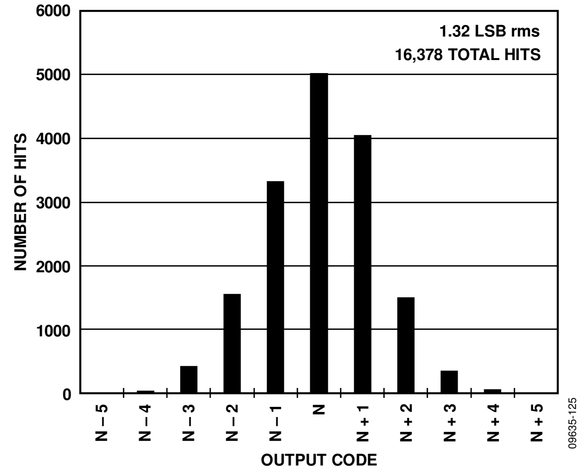


Figure 18. AD6649 Grounded Input Histogram

EQUIVALENT CIRCUITS

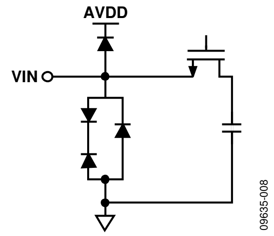


Figure 19. Equivalent Analog Input Circuit

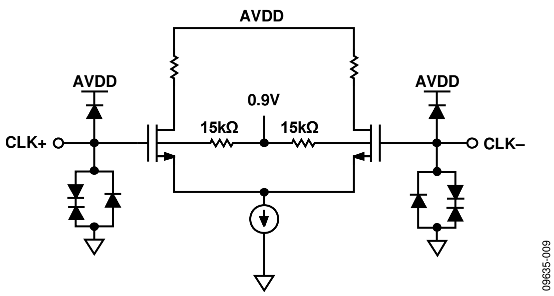


Figure 20. Equivalent Clock Input Circuit

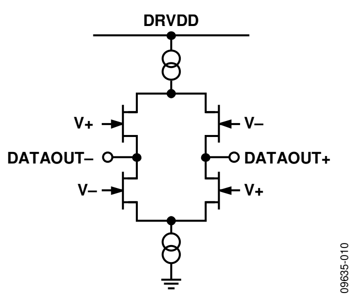


Figure 21. Equivalent LVDS Output Circuit

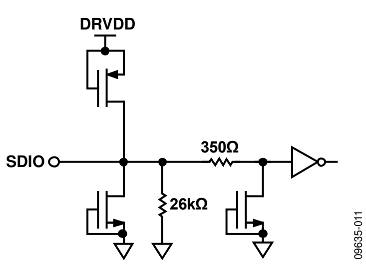


Figure 22. Equivalent SDIO Circuit

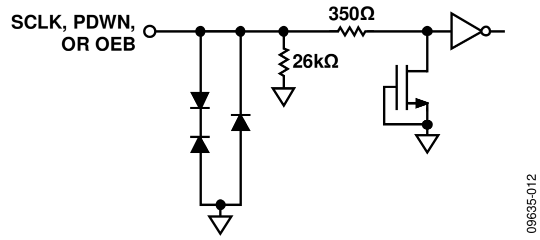


Figure 23. Equivalent SCLK, PDWN, or OEB Input Circuit

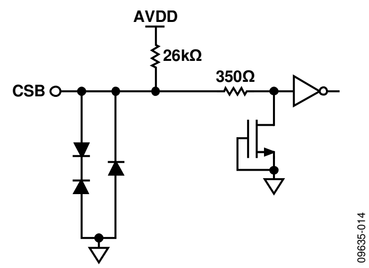


Figure 24. Equivalent CSB Input Circuit

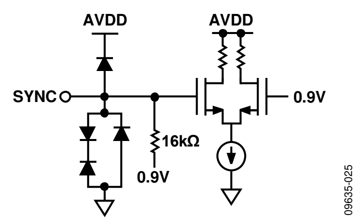


Figure 25. Equivalent SYNC Input Circuit

THEORY OF OPERATION

The AD6649 has two analog input channels, two filter channels, and two digital output channels. The intermediate frequency (IF) input signal passes through several stages before appearing at the output port(s) as a filtered and optionally decimated digital signal.

The dual ADC design can be used for diversity reception of signals, where the ADCs operate identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample frequencies from dc to 300 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. Operation to 400 MHz analog input is permitted but occurs at the expense of increased ADC noise and distortion.

Synchronization capability is provided to allow synchronized timing between multiple devices.

Programming and control of the AD6649 are accomplished using a 3-pin SPI-compatible serial interface.

ADC ARCHITECTURE

The AD6649 architecture consists of a dual front-end sample-and-hold circuit, followed by a pipelined switched-capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The MDAC magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of each channel contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing digital output noise to be separated from the analog core. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD6649 is a differential switched-capacitor circuit that has been designed for optimum performance while processing a differential input signal.

The clock signal alternatively switches the input between sample mode and hold mode (see the configuration shown in Figure 26). When the input is switched into sample mode, the signal source must be capable of charging the sampling capacitors and settling within 1/2 clock cycle.

A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, the shunt capacitors should be reduced. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. Refer to the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters," for more information on this subject.

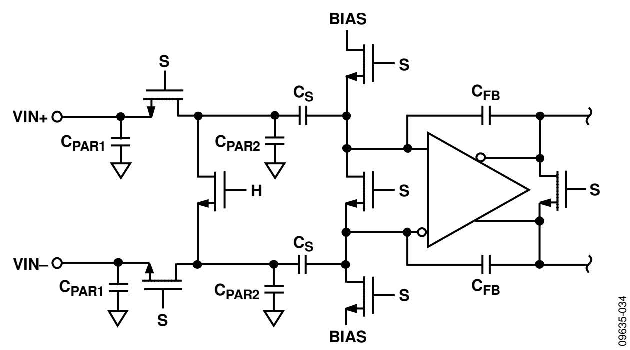


Figure 26. Switched-Capacitor Input

For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched, and the inputs should be differentially balanced.

Input Common Mode

The analog inputs of the AD6649 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that $V_{CM} = 0.5 \times AVDD$ (or 0.9 V) is recommended for optimum performance. An on-board common-mode voltage reference is included in the design and is available from the VCM pin. Using the VCM output to set the input common mode is recommended. Optimum performance is achieved when the common-mode voltage of the analog input is set by the VCM pin voltage (typically 0.5 × AVDD). The VCM pin must be decoupled to ground by a 0.1 µF capacitor, as described in the Applications Information section. This decoupling capacitor should be placed close to the pin to minimize the series resistance and inductance between the part and this capacitor.

Differential Input Configurations

Optimum performance is achieved while driving the AD6649 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, ADA4938-2, and ADA4930-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4930-2 is easily set with the VCM pin of the AD6649 (see Figure 27), and the driver can be configured in a Sallen-Key filter topology to provide band-limiting of the input signal.

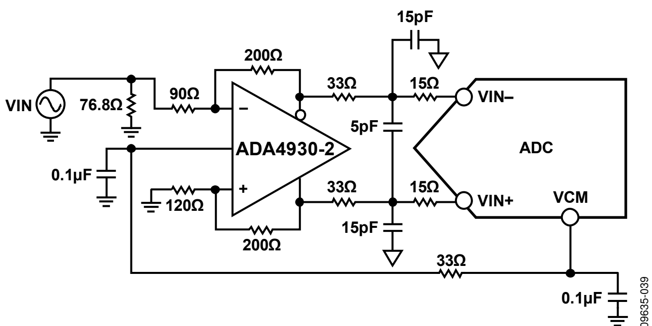


Figure 27. Differential Input Configuration Using the ADA4930-2

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 28. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

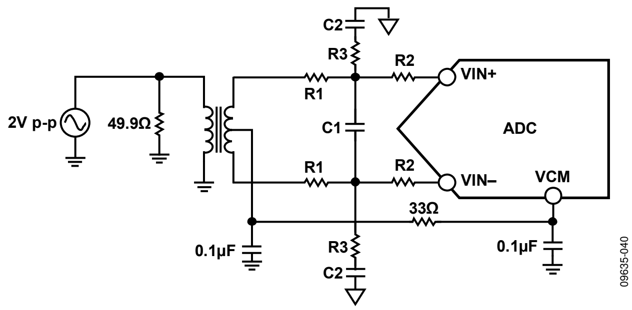


Figure 28. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz. Excessive signal power can also cause core saturation, which leads to distortion.

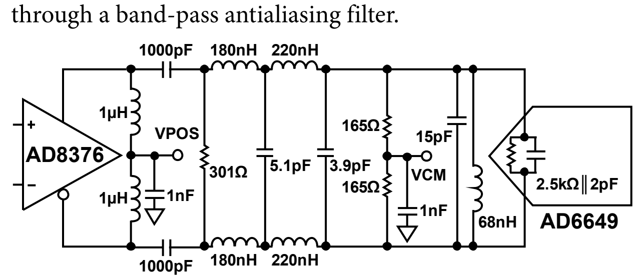
At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD6649. For applications where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 30). In this configuration, the input is ac-coupled and the CML is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver.

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance. Based on these parameters the value of the input resistors and capacitors may need to be adjusted or some components may need to be removed. Table 9 displays recommended values to set the RC network for different input frequency ranges. However, these values are dependent on the input signal and bandwidth and should be used only as a starting guide. Note that the values given in Table 9 are for each R1, R2, C2, and R3 component shown in Figure 28 and Figure 30.

Table 9. Example RC Network

Frequency Range (MHz)	R1 Series (Ω)	C1 Differential (pF)	R2 Series (Ω)	C2 Shunt (pF)	R3 Shunt (Ω)
0 to 100	33	8.2	0	15	49.9
100 to 250	15	3.9	0	8.2	49.9

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use an amplifier with variable gain. The AD8375 or AD8376 digital variable gain amplifier (DVGAs) provides good performance for driving the AD6649. Figure 29 shows an example of the AD8376 driving the AD6649 through a band-pass antialiasing filter.



NOTES
1. ALL INDUCTORS ARE COILCRAFT® 0603CS COMPONENTS WITH THE EXCEPTION OF THE 1µH CHOKE INDUCTORS (COILCRAFT 0603LS).
2. FILTER VALUES SHOWN ARE FOR A 20MHz BANDWIDTH FILTER CENTERED AT 140MHz.

09635-115

Figure 29. Differential Input Configuration Using the AD8376

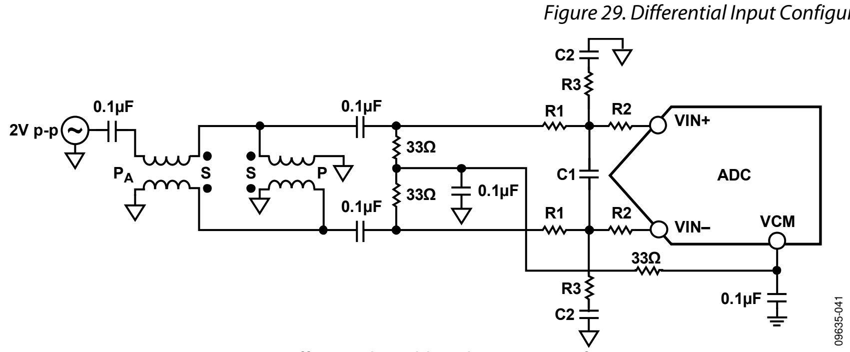


Figure 30. Differential Double Balun Input Configuration

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD6649. The full-scale input range can be adjusted by varying the reference voltage via SPI. The input span of the ADC tracks reference voltage changes linearly.

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD6649 sample clock inputs, CLK+ and CLK−, should be clocked with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or via capacitors. These pins are biased internally (see Figure 31) and require no external bias. If the inputs are floated, the CLK− pin is pulled low to prevent spurious clocking.

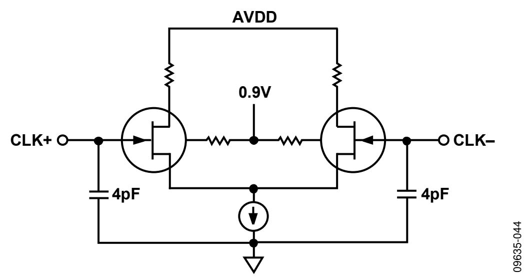


Figure 31. Simplified Equivalent Clock Input Circuit

Clock Input Options

The AD6649 has a very flexible clock input structure. Clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section.

Figure 32 and Figure 33 show two preferable methods for clocking the AD6649 (at clock rates of up to 625 MHz). A low jitter clock source is converted from a single-ended signal to a differential signal using an RF balun or RF transformer.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 625 MHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD6649 to approximately 0.8 V p-p differential. This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD6649 while preserving the fast rise and fall times of the signal, which are critical to low jitter performance.

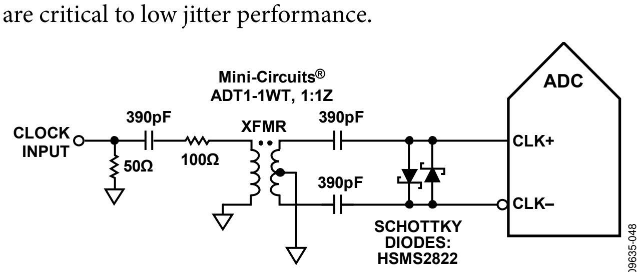


Figure 32. Transformer-Coupled Differential Clock (Up to 200 MHz)

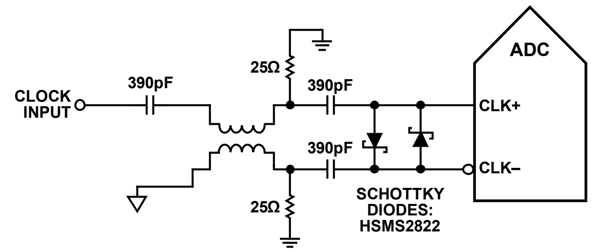


Figure 33. Balun-Coupled Differential Clock (Up to 625 MHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins as shown in Figure 34. The AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516, AD9517, AD9518, AD9520, AD9522, AD9523, AD9524, and ADCLK905/ADCLK907/ADCLK925 clock drivers offer excellent jitter performance.

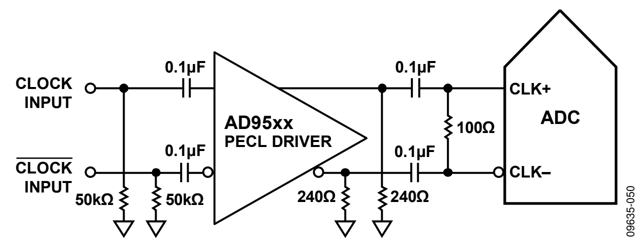


Figure 34. Differential PECL Sample Clock (Up to 625 MHz)

A third option is to ac-couple a differential LVDS signal to the sample clock input pins, as shown in Figure 35. The AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516, AD9517, AD9518, AD9520, AD9522, AD9523, and AD9524 clock drivers offer excellent jitter performance.

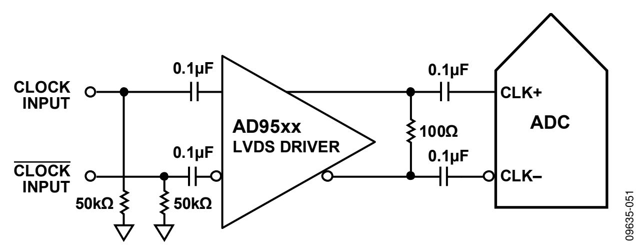


Figure 35. Differential LVDS Sample Clock (Up to 625 MHz)

Input Clock Divider

The AD6649 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8. The duty cycle stabilizer (DCS) is enabled by default on power-up.

The AD6649 clock divider can be synchronized using the external SYNC input. Bit 1 and Bit 2 of Register 0x3A allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD6649 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD6649.

Jitter on the rising edge of the input clock is still of paramount concern and is not reduced by the duty cycle stabilizer. The duty cycle control loop does not function for clock rates less than 40 MHz nominally. The loop has a time constant associated with it that must be considered when the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time period that the loop is not locked, the DCS loop is bypassed, and internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{IN}) due to jitter (t_J) can be calculated by

$$SNR_{HF} = -10\log[(2\pi \times f_{IN} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the root-mean-square of all jitter sources, which include the clock input, the analog input signal, and the ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter, as shown in Figure 36.

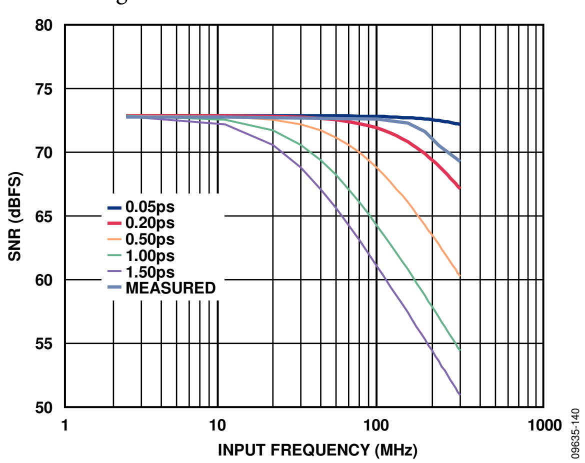


Figure 36. SNR (95 MHz BW) vs. Input Frequency and Jitter

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD6649. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance*, and the AN-756 Application Note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*, for more information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 37, the power dissipated by the AD6649 is proportional to its sample rate. The data in Figure 37 was taken using the same operating conditions as those used for the Typical Performance Characteristics.

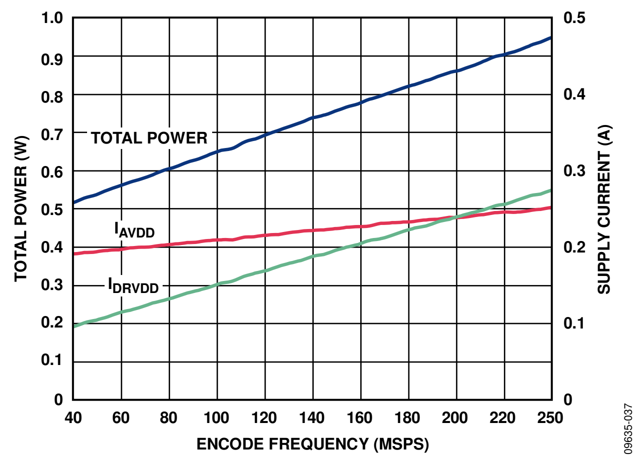


Figure 37. AD6649 Power and Current vs. Sample Rate

By asserting PDWN (either through the SPI port or by asserting the PDWN pin high), the AD6649 is placed in power-down mode. In this state, the ADC typically dissipates 10 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD6649 to its normal operating mode. Note that PDWN is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map Register Description section and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional details.

DIGITAL OUTPUTS

The AD6649 output drivers can be configured for either ANSI LVDS or reduced drive LVDS using a 1.8 V DRVDD supply.

As detailed in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, the data format can be selected for offset binary, twos complement, or gray code when using the SPI control.

Digital Output Enable Function (OEB)

The AD6649 has a flexible three-state ability for the digital output pins. The three-state mode is enabled using the OEB pin or through the SPI interface. If the OEB pin is low, the output data drivers are enabled. If the OEB pin is high, the output data drivers are placed in a high impedance state. This OEB function is not intended for rapid access to the data bus. Note that OEB is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

When using the SPI interface, the data and fast detect outputs of each channel can be independently three-stated by using the output enable bar bit (Bit 4) in Register 0x14. Because the output data is interleaved, if only one of the two channels is disabled, the data of the remaining channel is repeated in both the rising and falling output clock cycles.

Timing

The AD6649 provides latched data with a pipeline delay of 23 or 43 input sample clock cycles, depending on the mode of operation. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD6649. These transients can degrade converter dynamic performance.

The lowest typical conversion rate of the AD6649 is 40 MSPS. At clock rates below 40 MSPS, dynamic performance may degrade.

Data Clock Output (DCO)

The AD6649 also provides data clock output (DCO) intended for capturing the data in an external register. Figure 2 shows a graphical timing diagram of the AD6649 output modes.

OVERRANGE (OR)

The overrange indicator is asserted when an overrange is detected on the input of the AD6649. The overrange condition is determined at the output of the pipeline ADC and, therefore, is subject to a latency of 10 ADC clocks. An overrange at the input is indicated by this bit, 10 clock cycles after it occurs.

Table 10. Output Data Format

Input (V)	VIN+ – VIN−, Input Span = 1.75 V p-p (V)	Offset Binary Output Mode	Twos Complement Mode (Default)	OR
VIN+ – VIN−	<−0.875	00 0000 0000 0000	10 0000 0000 0000	1
VIN+ – VIN−	−0.875	00 0000 0000 0000	10 0000 0000 0000	0
VIN+ – VIN−	0	10 0000 0000 0000	00 0000 0000 0000	0
VIN+ – VIN−	+0.875	11 1111 1111 1111	01 1111 1111 1111	0
VIN+ – VIN−	>+0.875	11 1111 1111 1111	01 1111 1111 1111	1

DIGITAL PROCESSING

The AD6649 includes a digital processing section that provides filtering. This digital processing section includes a numerically controlled oscillator (NCO), a selectable FIR filter (high performance or low latency), and a second coarse NCO (f_S/4 fixed value) for output frequency translation (complex to real). These blocks can be configured in several modes to implement a signal processing function. Refer to Figure 1 for the functional block diagram of the AD6649.

NUMERICALLY CONTROLLED OSCILLATOR (NCO)

Frequency translation is accomplished with an NCO shared between the two channels. Amplitude and phase dither can be enabled on chip to improve the noise and spurious performance of the NCO.

Because the filtering prevents usage of part of the Nyquist spectrum, a means is needed to translate the sampled input spectrum into the usable range of the decimation filter. To achieve this, a 32-bit, tuning, complex NCO is provided. This NCO/mixer allows the input spectrum to be tuned to dc, where it can be effectively filtered by the subsequent filter blocks to prevent aliasing.

When using the low latency FIR, the NCO must be tuned to f_S/4 (0x40000000). This prevents unwanted aliases from falling back into the band of interest.

NCO AND FIR FILTER MODES

The NCO and FIR blocks can be used in two modes depending on the bandwidth and latency requirement of the application. The two modes of operation of these blocks are summarized in Table 11.

Table 11. Signal Path Modes

Mode	FIR	Output Bandwidth at 245.76 MSPS
Fixed-Frequency NCO, 95 MHz FIR Filter	Low latency (default)	95 MHz
Tunable-Frequency NCO, 100 MHz FIR Filter	High performance	99.5 MHz

Two fixed-coefficient FIR filters provide filtering capability. A low latency FIR or a high performance FIR can be selected. It removes the negative frequency images to avoid aliasing negative frequencies for real outputs. Figure 38, Figure 39, and Figure 40 show the progression of a 95 MHz bandwidth signal through the filter stages when using the fixed-frequency NCO and 95 MHz FIR filter with a sample rate of 245.76 MSPS. The tunable-frequency NCO can be used instead and operates in a similar fashion. In these modes, the output is centered at 61.44 MHz, assuming a 245.76 MSPS sample rate.

f_S/4 FIXED-FREQUENCY NCO

A fixed-frequency f_S/4 NCO is provided to translate the filtered, decimated signal from dc to f_S/4 to allow a real output. The f_S/4 NCO is required in all operation modes because complex output from the part is not supported.

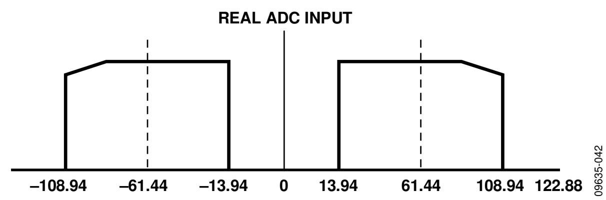


Figure 38. Example AD6649 Real 95 MHz Bandwidth Input Signal Centered at 61.44 MHz (f_{ADC} = 245.76 MHz)

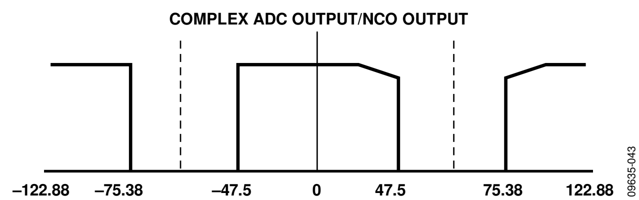


Figure 39. Example AD6649 95 MHz Bandwidth Input Signal Tuned to DC Using the NCO (NCO Frequency = 61.44 MHz)

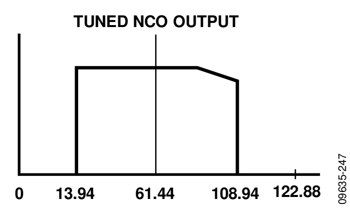


Figure 40. Example AD6649 95 MHz Bandwidth Output Signal Tuned to f_S/4 (NCO Frequency = 61.44 MHz)

NUMERICALLY CONTROLLED OSCILLATOR (NCO)

FREQUENCY TRANSLATION

This processing stage comprises a digital tuner consisting of a 32-bit complex numerically controlled oscillator (NCO). The NCO is always enabled. This NCO block accepts a real input from the ADC stage and outputs a frequency translated complex (I and Q) output.

The NCO frequency is programmed in Register 0x52 through Register 0x55. These four 8-bit registers make up a 32-bit unsigned frequency programming word. Frequencies between −CLK/2 and +CLK/2 are represented using the following frequency words:

- 0x80000000 represents a frequency given by −CLK/2.
- 0x00000000 represents dc (frequency = 0 Hz).
- 0x7FFFFFFF represents CLK/2 − CLK/2^{32}.

Use the following equation to calculate the NCO frequency:

$$NCO\_FREQ = 2^{32} \times \frac{Mod(f, f_{CLK})}{f_{CLK}}$$

where:
NCO_FREQ is a 32-bit twos complement number representing the NCO frequency register.
f is the desired carrier frequency in hertz.
f_{CLK} is the AD6649 ADC clock rate in hertz.

NCO SYNCHRONIZATION

The AD6649 NCOs within a single part or across multiple parts can be synchronized using the external SYNC input. Bit 0 and Bit 1 of Register 0x58 allow the NCO to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the NCO to restart at the programmed phase offset value.

NCO AMPLITUDE AND PHASE DITHER

The NCO block contains amplitude and phase dither to improve the spurious performance. Amplitude dither improves performance by randomizing the amplitude quantization errors within the angular-to-Cartesian conversion of the NCO. This option reduces spurs at the expense of a slightly raised noise floor. With amplitude dither enabled, the NCO has an SNR of greater than 93 dB and an SFDR of greater than 115 dB. With amplitude dither disabled, the SNR is increased to greater than 96 dB at the cost of SFDR performance, which is reduced to 100 dB. The NCO amplitude and phase dither are recommended and can be enabled by setting Bit 1 and Bit 2 in Register 0x51.

FIR FILTERS

The two FIR filters that can be used are either a 47-tap, high performance, fixed-coefficient FIR filter or a 21-tap, low latency, fixed-coefficient FIR filter. These filters are useful in providing alias protection at the device output. The high performance FIR is a simple sum-of-products FIR filter with 47 filter taps and 21-bit fixed coefficients. Note that this filter does not decimate. The normalized coefficients used in the implementation and the decimal equivalent value of the coefficients are listed for the low latency FIR in Table 12 and the high performance FIR in Table 13.

Table 12. Low Latency FIR Filter Coefficients

Coefficient Number	Normalized Coefficient	Decimal Coefficient (21-Bit)
C0, C20	0.00402830	1056
C1, C19	0.00518798	1360
C2, C18	−0.0047607	−1248
C3, C17	−0.0200195	−5248
C4, C16	0.0074463	1952
C5, C15	0.0502929	13184
C6, C14	−0.0096435	−2528
C7, C13	−0.1020507	−26752
C8, C12	0.0104980	−2752
C9, C11	0.3378906	88576
C10	0.4177246	109504

Table 13. High Performance FIR Filter Coefficients

Coefficient Number	Normalized Coefficient	Decimal Coefficient (21-Bit)
C0, C46	−0.0001335	−140
C1, C45	−0.0009689	−1016
C2, C44	−0.0024185	−2536
C3, C43	−0.0019341	−2028
C4, C42	0.0023584	2473
C5, C41	0.0051260	5375
C6, C40	−0.0009680	−1015
C7, C39	−0.0086231	−9042
C8, C38	−0.0011368	−1192
C9, C37	0.0142097	14900
C10, C36	0.0064697	6784
C11, C35	−0.0207596	−21768
C12, C34	−0.0161047	−16887
C13, C33	0.0274601	28794
C14, C32	0.0310631	32572
C15, C31	−0.0348339	−36526
C16, C30	−0.0557785	−58488
C17, C29	0.0415993	43620
C18, C28	0.0986786	103472
C19, C27	−0.0463982	−48652
C20, C26	−0.1893501	−198548
C21, C25	0.0505829	53040
C22, C24	0.6113434	641040
C23	0.9171314	961682

FIR SYNCHRONIZATION

The AD6649 filters within a single part or across multiple parts can be synchronized using the external SYNC input. The filters can be configured to be resynchronized on every SYNC signal or only on the first SYNC signal after the SPI control register is written. A valid SYNC causes the FIR filter to restart at the programmed decimation phase value. Bit 4 and Bit 5 of Register 0x58 allow the FIR to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written.

FILTER PERFORMANCE

When using the fixed-frequency NCO and a 95 MHz FIR filter, the output rate is equal to the sample clock rate. The composite response of this mode is shown in Figure 41. The detailed pass-band response for this mode is shown in Figure 42. To place the part in this mode, set SPI Register 0x50 to 0xB0. When operating in this mode, the NCO must be placed at $f_S/4$, and the low latency NCO select bit (Bit 0) in Register 0x5A must be set. It is important to note that a −1.0 dBFS input level at the analog inputs corresponds to an output level of −2.5 dBFS when using the low latency FIR filter. This output level reduction is a result of the −1.5 dB pass-band attenuation in the FIR filter in this mode and does not result in loss in the dynamic range of the converter.

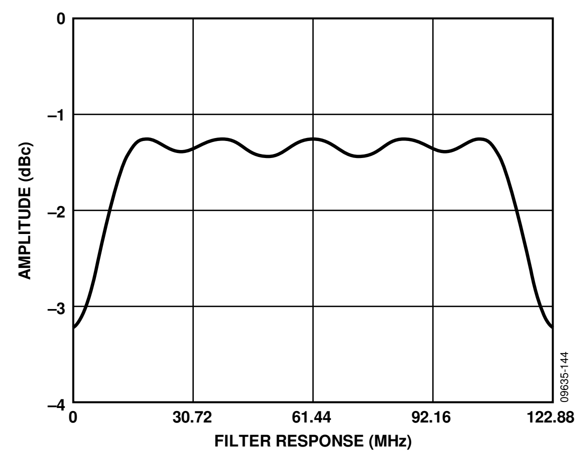


Figure 41. Low Latency FIR Filter Composite Response at 245.76 MSPS (Fixed-Frequency NCO, 95 MHz FIR Filter Mode)