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AD6650 Diversity IF-to-Baseband GSM/EDGE Narrow-Band Receiver

AD6650

FEATURES

116 dB dynamic range
Digital VGA
I/Q demodulators
Active low-pass filters
Dual wideband ADC
Programmable decimation and channel filters
VCO and phase-locked loop circuitry
Serial data output ports
Intermediate frequencies of 70 MHz to 260 MHz
10 dB noise figure
+43 dBm input IP2 at 70 MHz IF
−9.5 dBm input IP3 at 70 MHz IF
3.3 V I/O and CMOS core
Microprocessor interface
JTAG boundary scan

APPLICATIONS

PHS or GSM/EDGE single carrier, diversity receivers
Microcell and picocell systems
Wireless local loop
Smart antenna systems
Software radios
In-building wireless telephony

PRODUCT DESCRIPTION

The AD6650 is a diversity intermediate frequency-to-baseband (IF-to-baseband) receiver for GSM/EDGE. This narrow-band receiver consists of an integrated DVGA, IF-to-baseband I/Q demodulators, low-pass filtering, and a dual wideband ADC. The chip can accommodate IF input from 70 MHz to 260 MHz. The receiver architecture is designed such that only one external surface acoustic wave (SAW) filter for main and one for diversity are required in the entire receive signal path to meet GSM/EDGE blocking requirements.

Digital decimation and filtering circuitry provided on-chip remove unwanted signals and noise outside the channel of interest. Programmable RAM coefficient filters allow antialiasing, matched filtering, and static equalization functions to be combined in a single cost-effective filter. The output of the channel filters is provided to the user via serial output I/Q data streams.

FUNCTIONAL BLOCK DIAGRAM

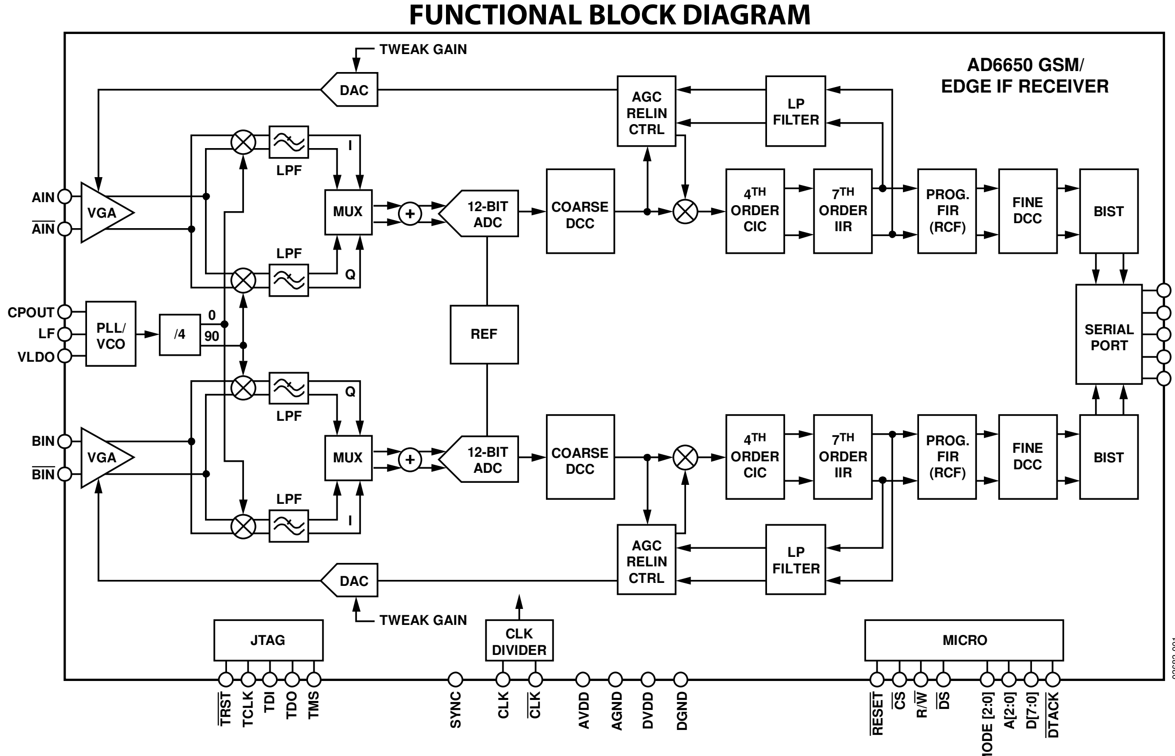

Figure 1.

Rev. A

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AD6650* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design

Data Sheet

- AD6650: Diversity IF-to-Baseband GSM/EDGE Narrow-Band Receiver Data Sheet

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC
- Smart Partitioning Eyes 3G Basestation
- The Hard Truth about System-on-Chip Designs

DESIGN RESOURCES

- AD6650 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD6650 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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TABLE OF CONTENTS

REVISION HISTORY

1/07—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Specifications ... 3
Changes to Figure 18 ... 13
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Changes to Ordering Guide ... 44

3/06—Revision 0: Initial Version

SPECIFICATIONS

EXPLANATION OF TEST LEVELS

I. 100% production tested.
II. 100% production tested at 25°C; sample tested at specified temperatures.
III. Sample tested only.
IV. Parameter guaranteed by design and analysis.
V. Parameter is typical value only.
VI. 100% production tested at 25°C; sample tested at temperature extreme.
VII. 100% production tested at +85°C.

C_{LOAD} = 40 pF on all outputs, unless otherwise specified. All timing specifications valid over VDD range of 3.0 V to 3.45 V and VDDIO range of 3.0 V to 3.45 V.

AC SPECIFICATIONS

AVDD and DVDD = 3.3 V, CLK = 52 MSPS (driven differentially), 50% duty cycle, unless otherwise noted. All minimum ac specifications are guaranteed from −25°C to +85°C. AC minimum specifications degrade slightly from −25°C to −40°C.

Table 1.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
OVERALL FUNCTION						
Frequency Range	Full	V	70		260	MHz
GAIN CONTROL						
Gain Step Size	25°C	V		0.094		dB
Gain Step Accuracy	25°C	V		±0.047		dB
AGC Range	25°C	V		36		dB
BASEBAND FILTERS						
Bandwidth	Full	IV	3.36	3.5	3.64	MHz
Alias Rejection at 25.9 MHz	25°C	V		77		dB
LO PHASE NOISE						
At 10 kHz Offset	25°C	V		−79		dBc/Hz
At 20 kHz Offset	25°C	V		−87		dBc/Hz
At 50 kHz Offset	25°C	V		−103		dBc/Hz
At 100 kHz Offset	25°C	V		−112		dBc/Hz
At 200 kHz Offset	25°C	V		−119		dBc/Hz
At 400 kHz Offset	25°C	V		−125		dBc/Hz
At 600 kHz Offset	25°C	V		−130		dBc/Hz
At 800 kHz Offset	25°C	V		−133		dBc/Hz
At 1600 kHz Offset	25°C	V		−138		dBc/Hz
At 3000 kHz Offset	25°C	V		−143		dBc/Hz
GAIN ERROR	25°C	V		−0.7		dB
PSRR (AVDD with 20 mV RMS Ripple)[1]						
At 5 kHz	25°C	V		−13.4		dBc
At 10 kHz	25°C	V		−17		dBc
At 50 kHz	25°C	V		−34		dBc
At 100 kHz	25°C	V		−39.8		dBc
At 150 kHz	25°C	V		−45.7		dBc
f = 70 MHz						
Coarse DC Correction		V		−70		dB
Noise Figure[2]		V		10		dB
Input IP2[2]	Full	IV	24	43		dBm
Input IP3[2]	Full	IV	−15	−9.5		dBm
Image Rejection	Full	IV		−49	−33	dBc
Full-Scale Input Power		V		4		dBm
Input Impedance		V		189.6 − j33.6		Ω

Parameter	Temp	Test Level	Min	Typ	Max	Unit
f = 150 MHz						
Coarse DC Correction		V		−70		dB
Noise Figure[2]		V		10		dB
Input IP2[2]	Full	IV	24	37		dBm
Input IP3[2]	Full	IV	−15	−11.5		dBm
Image Rejection	Full	IV		−46.5	−33	dBc
Full-Scale Input Power		V		4		dBm
Input Impedance		V		169.3 – j59.2		Ω
f = 200 MHz						
Coarse DC Correction		V		−70		dB
Noise Figure[2]		V		10		dB
Input IP2[2]	Full	IV	24	35		dBm
Input IP3[2]	Full	IV	−16	−12		dBm
Image Rejection	Full	IV		−46.5	−33	dBc
Full-Scale Input Power		V		4		dBm
Input Impedance		V		159.3 – j66.9		Ω
f = 250 MHz						
Coarse DC Correction		V		−70		dB
Noise Figure[2]		V		10		dB
Input IP2[2]	Full	VII	24	33		dBm
Input IP3[2]	Full	VII	−16	−13		dBm
Image Rejection	Full	VII		−45	−33	dBc
Full-Scale Input Power		V		4		dBm
Input Impedance		V		137.1 – j72.7		Ω

[1] See Figure 40 and Figure 41 for additional PSRR specifications.
[2] This measurement applies for maximum gain (36 dB).

DIGITAL SPECIFICATIONS

AVDD and DVDD = 3.3 V, CLK = 52 MSPS, unless otherwise noted.

Table 2.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
DVDD	Full	IV	3.0	3.3	3.45	V
AVDD	Full	IV	3.0	3.3	3.45	V
$T_{AMBIENT}$[1]		IV	−25	+25	+85	°C

[1] The AD6650 is guaranteed fully functional from −40°C to +85°C. All ac minimum specifications are guaranteed from −25°C to +85°C, but degrade slightly from −25°C to −40°C.

ELECTRICAL CHARACTERISTICS

Table 3.

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
LOGIC INPUTS						
Logic Compatibility	Full	IV		3.3 V CMOS		
Digital Logic						
Logic 1 Voltage	Full	IV	2.0		VDD	V
Logic 0 Voltage	Full	IV	0		0.8	V
Logic 1 Current	25°C	V		60		μA
Logic 0 Current	25°C	V		7		μA
Input Capacitance	25°C	V		5		pF
CLOCK INPUTS						
Differential Input Voltage[1]	25°C	V	0.4		3.6	V p-p
Common-Mode Input Voltage	25°C	V		DVDD/2		V
Differential Input Resistance	25°C	V		7.5		kΩ
Differential Input Capacitance	25°C	V		5		pF
LOGIC OUTPUTS						
Logic Compatibility	Full			3.3 V CMOS/TTL		
Logic 1 Voltage (I_{OH} = 0.25 mA)	Full	IV	2.4	VDD − 0.2		V
Logic 0 Voltage (I_{OL} = 0.25 mA)	Full	IV		0.2	0.8	V
IDD SUPPLY CURRENT						
CLK = 52 MHz (GSM Example)						
I_{DVDD}	Full	VII		155		mA
I_{AVDD}	Full	VII		360		mA
POWER DISSIPATION						
CLK = 52 MHz (GSM/EDGE Example)	Full	VII		1.7	2.1	W

[1] All ac specifications are tested by driving CLK and $\overline{\text{CLK}}$ differentially.

GENERAL TIMING CHARACTERISTICS

Table 4.

Parameter (Conditions)	Symbol	Temp	Test Level	Min	Typ	Max	Unit
CLK TIMING REQUIREMENTS							
CLK Period[1]	t_{CLK}	Full	I	9.6		19.2	ns
CLK Width Low	t_{CLKL}	Full	IV		0.5 × t_{CLK}		ns
CLK Width High	t_{CLKH}	Full	IV		0.5 × t_{CLK}		ns
$\overline{\text{RESET}}$ TIMING REQUIREMENTS							
$\overline{\text{RESET}}$ Width Low	t_{SSF}	Full	IV	30			ns
PIN_SYNC TIMING REQUIREMENTS							
SYNC to ↑ CLK Setup Time	t_{SS}	Full	IV	−3			ns
SYNC to ↑ CLK Hold Time	t_{HS}	Full	IV	6			ns
SERIAL PORT TIMING REQUIREMENTS: SWITCHING CHARACTERISTICS[2]							
↑ CLK to ↑ SCLK Delay (Divide-by-1)	t_{DSCLK1}	Full	IV	3.2		12.5	ns
↑ CLK to ↑ SCLK Delay (For Any Other Divisor)	t_{DSCLKH}	Full	IV	4.4		16	ns
↑ CLK to ↓ SCLK Delay (Divide-by-2 or Even Number)	t_{DSCLKL}	Full	IV	4.7		16	ns
↓ CLK to ↓ SCLK Delay (Divide-by-3 or Odd Number)	$t_{DSCLKLL}$	Full	IV	4		14	ns
↑ SCLK to SDFS Delay	t_{DSDFS}	Full	IV	1		2.6	ns
↑ SCLK to SDO0 Delay	t_{DSDO0}	Full	IV	0.5		3.5	ns
↑ SCLK to SDO1 Delay	t_{DSDO1}	Full	IV	0.5		3.5	ns
↑ SCLK to DR Delay	t_{DSDR}	Full	IV	1		3.5	ns

[1] Minimum specification is based on a 104 MSPS clock rate (an internal divide-by-2 must be used with a 104 MSPS clock rate); maximum specification is based on a 52 MSPS clock rate. This device is optimized to operate at a clock rate of 52 MSPS or 104 MSPS.
[2] The timing parameters for SCLK, SDFS, SDO0, SDO1, and DR apply to both Channel 0 and Channel 1.

MICROPROCESSOR PORT TIMING CHARACTERISTICS

All timing specifications valid over VDD range of 3.0 V to 3.45 V and VDDIO range of 3.0 V to 3.45 V.

Table 5. Microprocessor Port, Mode INM (MODE = 0); Asynchronous Operation

Parameter	Symbol	Temp	Test Level	Min	Typ	Max	Unit
WRITE TIMING							
$\overline{WR}$ (R/$\overline{W}$) to RDY ($\overline{DTACK}$) Hold Time[1]	t_{HWR}	Full	IV	0.0			ns
Address/Data to $\overline{WR}$ (R/$\overline{W}$) Setup Time[1]	t_{SAM}	Full	IV	0.0			ns
Address/Data to RDY ($\overline{DTACK}$) Hold Time[1]	t_{HAM}	Full	IV	0.0			ns
$\overline{WR}$ (R/$\overline{W}$) to RDY ($\overline{DTACK}$) Delay	t_{DRDY}[2]	Full	IV	9.0		15.0	ns
$\overline{WR}$ (R/$\overline{W}$) to RDY ($\overline{DTACK}$) High Delay[1]	t_{ACC}	Full	IV	$4 \times t_{CLK}$		$13 \times t_{CLK}$	ns
READ TIMING							
Address to $\overline{RD}$ ($\overline{DS}$) Setup Time[1]	t_{SAM}	Full	IV	0.0			ns
Address to Data Hold Time[1]	t_{HAM}	Full	IV	0.0			ns
Data Three-state Delay[1]	t_{ZD}	Full	V		12		ns
RDY ($\overline{DTACK}$) to Data Delay[1]	t_{DD}	Full	IV			0.0	ns
$\overline{RD}$ ($\overline{DS}$) to RDY ($\overline{DTACK}$) Delay	t_{DRDY}[2]	Full	IV	9.0		15.0	ns
$\overline{RD}$ ($\overline{DS}$) to RDY ($\overline{DTACK}$) High Delay[1]	t_{ACC}	Full	IV	$4 \times t_{CLK}$		$13 \times t_{CLK}$	ns

[1] Timing is guaranteed by design.
[2] Specification pertains to control signals R/$\overline{W}$, $\overline{WR}$, $\overline{DS}$, $\overline{RD}$, and $\overline{CS}$ such that the minimum specification is valid after the last control signal has reached a valid logic level.

Table 6. Microprocessor Port, Mode MNM (MODE = 1)

Parameter	Symbol	Temp	Test Level	Min	Typ	Max	Unit
WRITE TIMING							
$\overline{DS}$ ($\overline{RD}$) to $\overline{DTACK}$ (RDY) Hold Time	t_{HDS}	Full	IV	15.0			ns
R/$\overline{W}$ ($\overline{WR}$) to $\overline{DTACK}$ (RDY) Hold Time	t_{HRW}	Full	IV	15.0			ns
Address/Data to R/$\overline{W}$ ($\overline{WR}$) Setup Time[1]	t_{SAM}	Full	IV	0.0			ns
Address/Data to R/$\overline{W}$ ($\overline{WR}$) Hold Time[1]	t_{HAM}	Full	IV	0.0			ns
$\overline{DS}$ ($\overline{RD}$) to $\overline{DTACK}$ (RDY) Delay[2]	t_{DDTACK}	Full	V		16		ns
R/$\overline{W}$ ($\overline{WR}$) to $\overline{DTACK}$ (RDY) Low Delay[1]	t_{ACC}	Full	IV	$4 \times t_{CLK}$		$13 \times t_{CLK}$	ns
READ TIMING							
$\overline{DS}$ ($\overline{RD}$) to $\overline{DTACK}$ (RDY) Hold Time	t_{HDS}	Full	IV	15.0			ns
Address to $\overline{DS}$ ($\overline{RD}$) Setup Time[1]	t_{SAM}	Full	IV	0.0			ns
Address to Data Hold Time[1]	t_{HAM}	Full	IV	0.0			ns
Data Three-State Delay	t_{ZD}	Full	V		13		ns
$\overline{DTACK}$ (RDY) to Data Delay[1]	t_{DD}	Full	IV			0.0	ns
$\overline{DS}$ ($\overline{RD}$) to $\overline{DTACK}$ (RDY) Delay[2]	t_{DDTACK}	Full	V		16		ns
$\overline{DS}$ ($\overline{RD}$) to $\overline{DTACK}$ (RDY) Low Delay[1]	t_{ACC}	Full	IV	$4 \times t_{CLK}$		$13 \times t_{CLK}$	ns

[1] Timing is guaranteed by design.
[2] $\overline{DTACK}$ is an open-drain device and must be pulled up with a 1 kΩ resistor.

TIMING DIAGRAMS

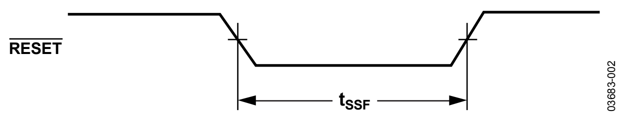


Figure 2. RESET Timing Requirements

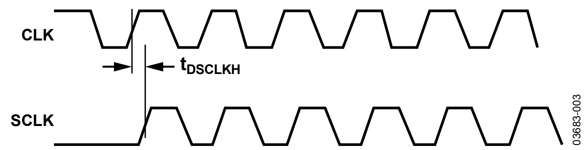


Figure 3. SCLK Switching Characteristics (Divide-by-1)

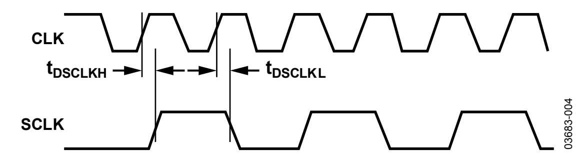


Figure 4. SCLK Switching Characteristics (Divide-by-2 or Even Integer)

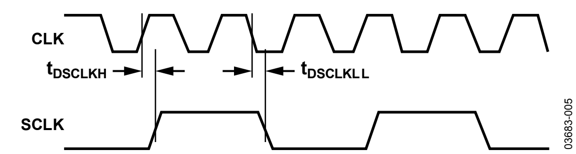


Figure 5. SCLK Switching Characteristics (Divide-by-3 or Odd Integer)

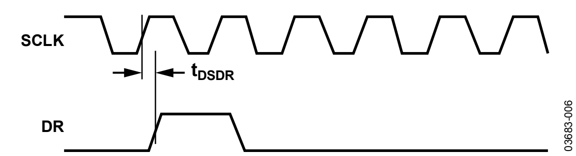


Figure 6. SCLK, DR Switching Characteristics

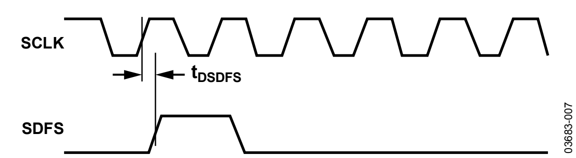


Figure 7. SCLK, SDFS Switching Characteristics

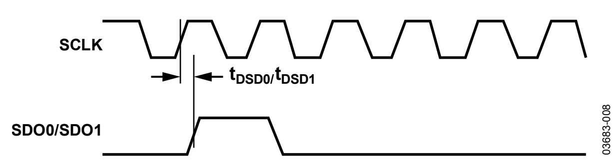


Figure 8. SCLK, SDO0/SDO1 Switching Characteristics

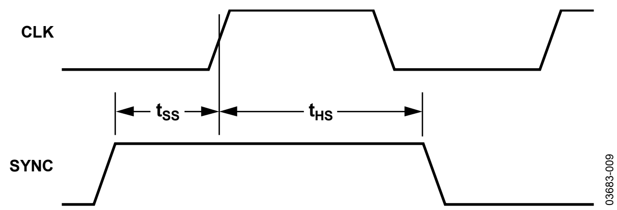
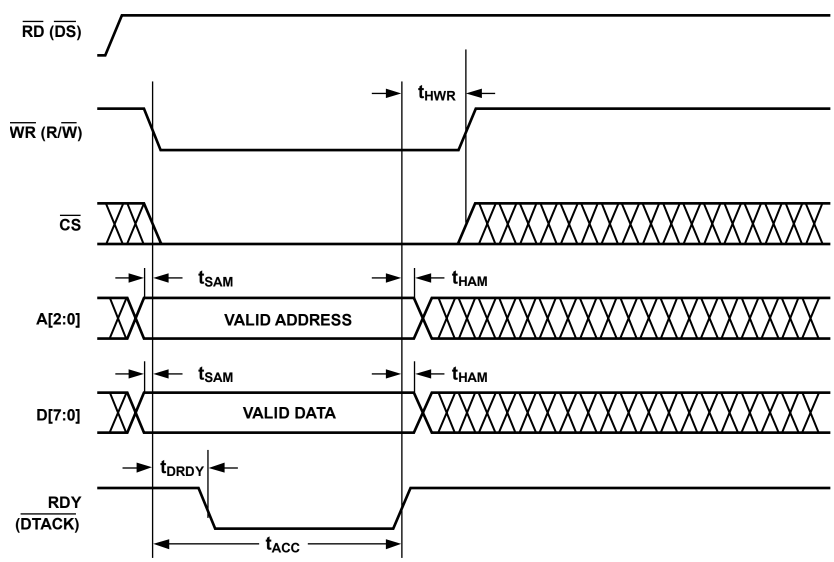
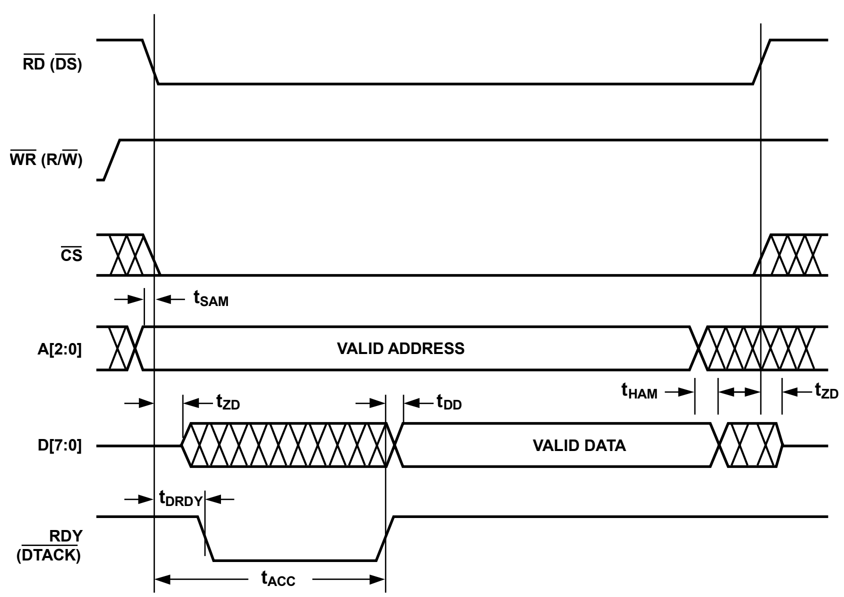


Figure 9. SYNC Timing Inputs



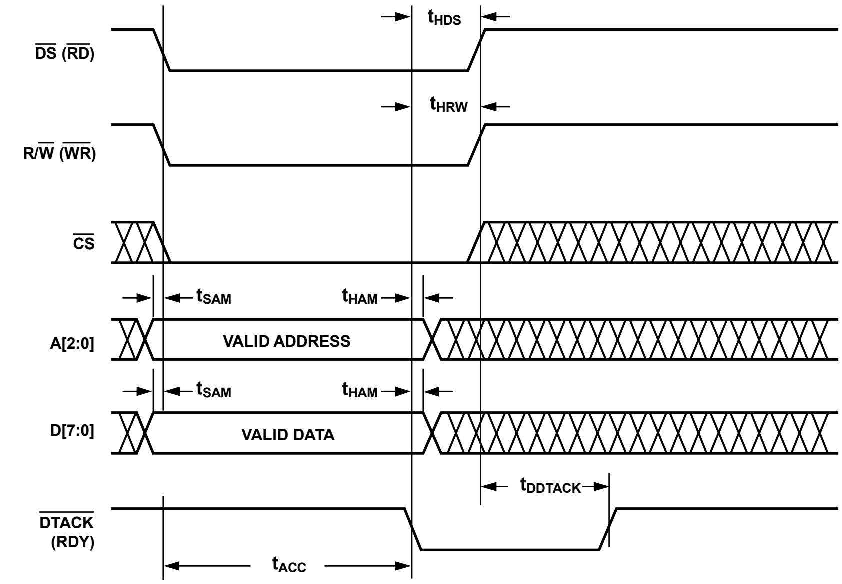
NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FALLING EDGE OF $\overline{WR}$ TO RISING EDGE OF RDY.
2. t_{ACC} REQUIRES A MAXIMUM OF NINE CLK PERIODS.

Figure 10. INM Microport Write Timing Requirements



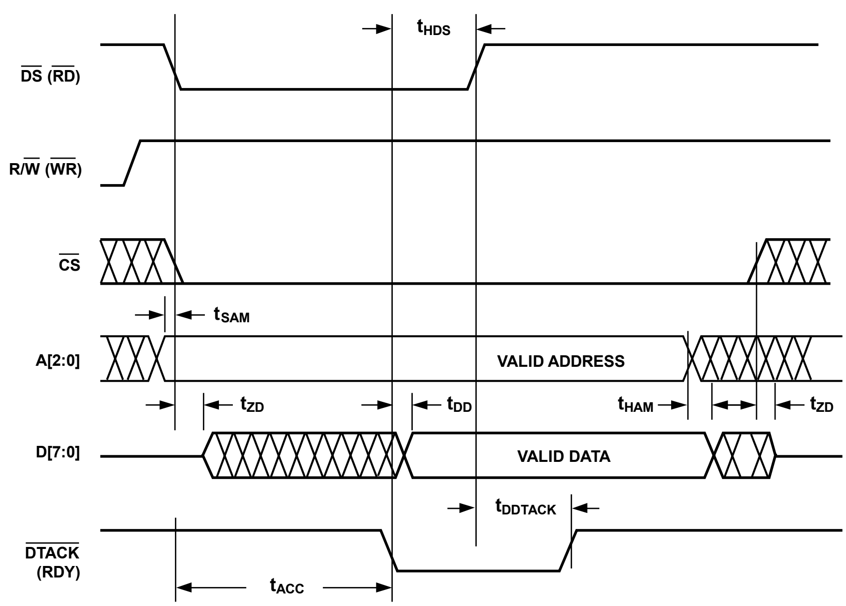
NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FALLING EDGE OF $\overline{RD}$ TO RISING EDGE OF RDY.
2. t_{ACC} REQUIRES A MAXIMUM OF 13 CLK PERIODS.

Figure 11. INM Microport Read Timing Requirements



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FALLING EDGE OF $\overline{DS}$ TO FALLING EDGE OF $\overline{DTACK}$.
2. t_{ACC} REQUIRES A MAXIMUM OF NINE CLK PERIODS.

Figure 12. MNM Microport Write Timing Requirements



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FALLING EDGE OF DS TO THE FALLING EDGE OF DTACK.
2. t_{ACC} REQUIRES A MAXIMUM OF 13 CLK PERIODS.

Figure 13. MNM Microport Read Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Supply Voltage	−0.3 V to +3.6 V
Input Voltage	−0.3 V to +3.6 V
Output Voltage Swing	−0.3 V to VDDIO + 0.3 V
Load Capacitance	200 pF
Junction Temperature Under Bias	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (5 sec)	280°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

121-lead chip scale package ball grid array:

θ_{JA} = 22.8°C/W, no airflow, measurements made in the horizontal position on a 4-layer board.

θ_{JA} = 20.2°C/W, 200 LFPM airflow, measurements made in the horizontal position on a 4-layer board.

θ_{JA} = 20.7°C/W, no airflow, soldered on an 8-layer board with two layers dedicated as ground planes.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

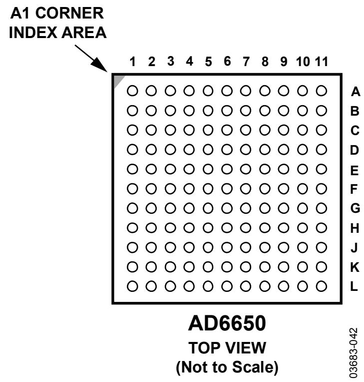


Figure 14. Pin Configuration

Table 8. Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	
A	DGND	TDI	TMS	$\overline{\text{TRST}}$	$\overline{\text{RESET}}$	DNC	AVDD	CLK	$\overline{\text{CLK}}$	AGND	AGND	**A**
B	SDFS	SCLK	TDO	TCLK	SYNC	DNC	AVDD	AVDD	AGND	AGND	$\overline{\text{BIN}}$	**B**
C	SDO1	SDO0	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AGND	AGND	BIN	**C**
D	D7	DR	DVDD	DGND	DGND	DGND	AVDD	AVDD	AGND	AGND	AGND	**D**
E	D5	D6	DVDD	DGND	DGND	DGND	AVDD	AVDD	AGND	AGND	LF	**E**
F	D3	D4	DVDD	DGND	DGND	DGND	AVDD	AVDD	AGND	DNC	VLDO	**F**
G	D1	D2	DVDD	DGND	DGND	DGND	AVDD	AVDD	AGND	AGND	CPOUT	**G**
H	$\overline{\text{DS}}$ ($\overline{\text{RD}}$)	D0	DVDD	DGND	DGND	DGND	AVDD	AVDD	AGND	AGND	AGND	**H**
J	R/$\overline{\text{W}}$ ($\overline{\text{WR}}$)	$\overline{\text{DTACK}}$ (RDY)	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AGND	AGND	AIN	**J**
K	A2	A1	$\overline{\text{CS}}$	MODE1	CHIP_ID1	DNC	AVDD	REFGND	REFT	AGND	$\overline{\text{AIN}}$	**K**
L	DGND	A0	MODE2	MODE0	CHIP_ID0	DNC	AVDD	VREF	REFB	AGND	AGND	**L**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	

Table 9. Pin Function Descriptions

Mnemonic	Type	Description	No. of Pins
POWER SUPPLY			
DVDD	Power	3.3 V Digital Supply.	13
AVDD	Power	3.3 V Analog Supply.	19
DGND	Ground	Digital Ground.	17
AGND	Ground	Analog Ground.	22
DIGITAL INPUTS			
$\overline{\text{RESET}}$	Input	Active Low Reset Pin.	1
SYNC	Input	Synchronizes Digital Filters.	1
CHIP_ID[1:0]	Input	Chip ID.	2
SERIAL DATA PORT			
SCLK	Bidirectional	Serial Clock.	1
SDFS	Bidirectional	Serial Data Frame Sync.	1
SDO[1:0]	Output	Serial Data Outputs. Three-stated when inactive.	2
DR	Output	Output Data Ready Indicator.	1
MICROPORTCONTROL			
D[7:0]	Bidirectional	Microport Data.	8
A[2:0]	Input	Microport Address Bits.	3
$\overline{\text{CS}}$	Input	Chip Select.	1
$\overline{\text{DS}}$ ($\overline{\text{RD}}$)	Input	Active Low Data Strobe (Active Low Read).	1

Mnemonic	Type	Description	No. of Pins
$\overline{\text{DTACK}}$ (RDY)	Output	Active Low Data Acknowledge (Microport Status Bit). Open-drain output, requires external pull-up resistor of 1 kΩ.	1
R/$\overline{\text{W}}$ ($\overline{\text{WR}}$)	Input	Read Write (Active Low Write).	1
MODE [2:0]	Input	Selects Control Port Mode.	3
JTAG			
$\overline{\text{TRST}}$	Input	Test Reset Pin.	1
TCLK	Input	Test Clock Input.	1
TMS	Input	Test Mode Select Input.	1
TDO	Output	Test Data Output. Three-stated when JTAG is in reset.	1
TDI	Input	Test Data input.	1
ANALOG INPUTS			
AIN	Input	Main Analog Input.	1
$\overline{\text{AIN}}$	Input	Complement of AIN. Differential analog input.	1
BIN	Input	Diversity Analog Input.	1
$\overline{\text{BIN}}$	Input	Complement of BIN. Differential analog input.	1
PLL INPUTS			
CPOUT	Output	Charge-Pump Output.	1
LF	Input	Loop Filter.	1
VLDO	Output	Compensation for Internal Low Dropout Regulator. Bypass to ground with a 220 nF chip capacitor.	1
REFT	Output	Internal ADC Voltage Reference. Bypass to ground with capacitors. See Figure 39 for recommended connection.	1
REFB	Output	Internal ADC Voltage Reference. Bypass to ground with capacitors. See Figure 39 for recommended connection.	1
VREF	Output	Internal ADC Voltage Reference. Bypass to ground with capacitors. See Figure 39 for recommended connection.	1
REFGND	Ground	ADC Ground Reference. See Figure 39 for recommended connection.	1
CLOCK INPUTS			
CLK	Input	Encode Input. Conversion initiated on rising edge.	1
$\overline{\text{CLK}}$	Input	Complement of Encode.	1
DNC		Do Not Connect.	5

TYPICAL PERFORMANCE CHARACTERISTICS

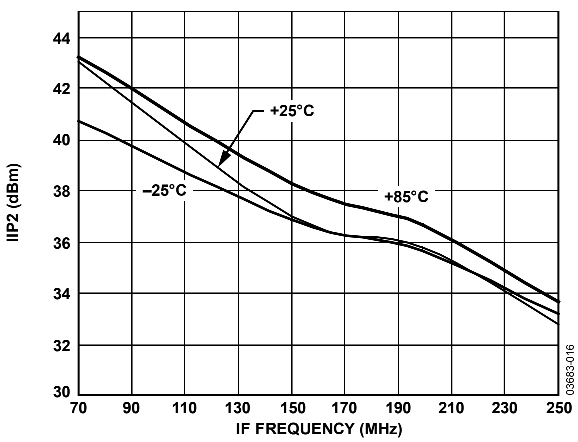


Figure 15. Input IP2 vs. Frequency

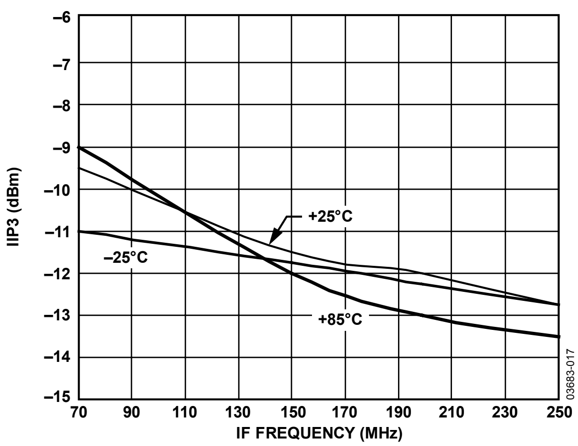


Figure 16. Input IP3 vs. Frequency

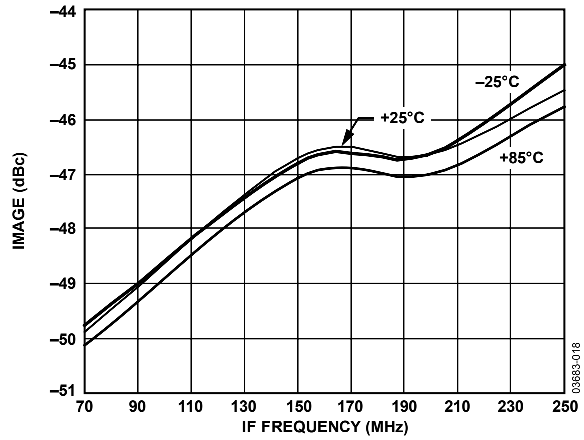


Figure 17. Image vs. Frequency

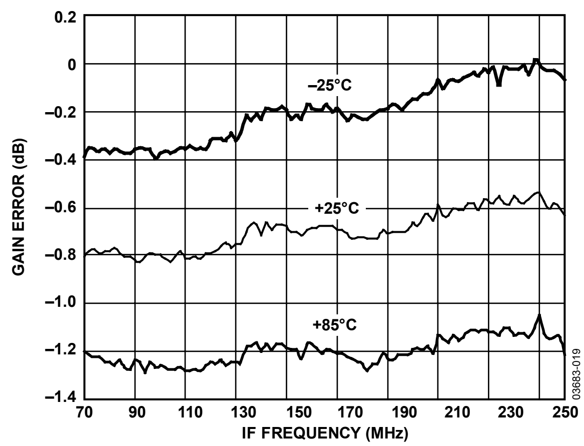


Figure 18. Gain Error vs. Frequency

TERMINOLOGY

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Noise Figure (NF)
The degradation in SNR performance (in dB) of an IF input signal after it passes through a component or system.

The AD6650 noise figure is determined by the equation

$$NF = \left(10\log\left(\frac{V^2{}_{rms}/Z_{in}}{0.001}\right) - SNR_{FS}\right) - 10\log\left(\frac{kTB}{0.001}\right) \quad (1)$$

where:

k is the Boltzmann constant = 1.38×10^{-23}.
T is the temperature in kelvin.
B is the channel bandwidth in hertz (200 kHz typical).
V^2_{rms} is the full-scale input voltage.
Z_{in} is the input impedance.
SNR_{FS} is the computed signal-to-noise ratio referred to full scale with a small input signal and the AD6650 in maximum gain.

Input Second-Order Intercept (IIP2)
A figure of merit used to determine a component's or system's susceptibility to intermodulation distortion (IMD) from its second-order nonlinearities. Two unmodulated carriers at a specified frequency relationship (f1 and f2) are injected into a nonlinear system exhibiting second-order nonlinearities producing IMD components at f1 − f2 and f2 − f1. IIP2 graphically represents the extrapolated intersection of the carrier's input power with the second-order IMD component when plotted in decibels.

Input Third-Order Intercept (IIP3)
A figure of merit used to determine a component's or system's susceptibility to intermodulation distortion (IMD) from its third-order nonlinearities. Two unmodulated carriers at a specified frequency relationship (f1 and f2) are injected into a nonlinear system exhibiting third-order nonlinearities producing IMD components at (2 × f1) − f2 and (2 × f2) − f1. IIP3 graphically represents the extrapolated intersection of the carrier's input power with the third-order IMD component when plotted in decibels.

Image
The AD6650 incorporates a quadrature demodulator that mixes the IF frequency to a baseband frequency. The phase and amplitude imbalance of this quadrature demodulator is observed in a complex FFT as an image of the fundamental frequency. The term image arises from the mirror-like symmetry of signal and image frequencies about the beating-oscillator frequency (in this case, this is dc).

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically, and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180° out of phase. The peak-to-peak differential voltage is computed by rotating the phases of the inputs 180° and taking the peak measurement again. Then the difference is computed between both peak measurements.

Full-Scale Input Power
Expressed in dBm. It is computed using the following equation:

$$Power_{Full\,scale} = 10\log\left(\frac{\dfrac{V^2{}_{Full\,scale_{rms}}}{Z_{Input}}}{0.001}\right) \quad (2)$$

where Z_{Input} is the input impedance.

Noise
The noise, including both thermal and quantization noise, for any range within the ADC is computed as

$$V_{noise} = \sqrt{Z \times 0.001 \times 10^{\left(\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10}\right)}} \quad (3)$$

where:

Z is the input impedance.
FS_{dBm} is the full scale of the device for the frequency in question.
SNR_{dBc} is the value for the particular input level.
$Signal_{dBFS}$ is the signal level within the ADC reported in decibels below full scale.

EQUIVALENT CIRCUITS

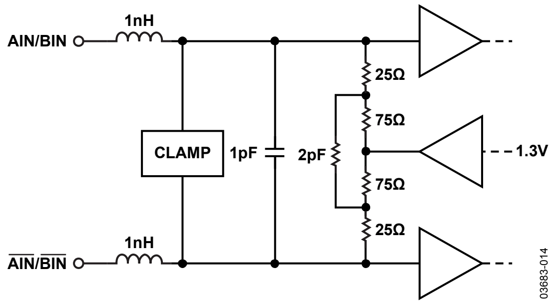


Figure 19. Analog Input

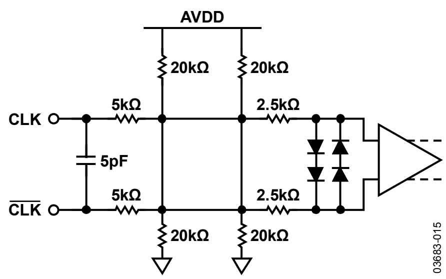


Figure 20. Clock Input

THEORY OF OPERATION

ANALOG FRONT END

The AD6650 is a mixed-signal front-end (MxFE®) component intended for direct IF sampling radios requiring high dynamic range. It is optimized for the demanding performance requirements of GSM and EDGE.

The AD6650 has five signal processing stages: a digital VGA, I/Q demodulators, seventh-order low-pass filters, dual ADCs, and digital filtering. Programming and control are accomplished via a microprocessor interface.

DVGA

A gain-ranging digital VGA is used to extend the dynamic range of the ADC and minimize signal clipping at the ADC input. The VGA has a maximum gain of 36 dB with a nominal step size of 0.094 dB. The amplifier serves as the input stage to the AD6650 and has a nominal input impedance of 200 Ω and a 4 dBm maximum input.

I/Q Demodulators

Frequency translation is accomplished with I/Q demodulators. Real data entering this stage is separated into in-phase (I) and quadrature (Q) components. This stage translates the input signal from an intermediate frequency (IF) of 70 MHz to 260 MHz to a baseband frequency.

Low-Pass Filters

In each I/Q signal path is a seventh-order low-pass active filter with 3.5 MHz bandwidth and automatic resistance-capacitance calibration to ±4%. This filter typically offers greater than 70 dB of alias rejection at 25.9 MHz.

Dual ADCs

The AD6650 has two ADCs. Each is implemented with an AD9238 core preceded by dual track-and-holds that multiplex in the I and Q signals at 26 MSPS each. The full-scale input power into the ADC is 4 dBm.

DIGITAL BACK END

The 12-bit ADC data goes through the coarse dc correction block, which performs a one-time calibration of the dc offsets in the I and Q paths. The output of this block drives the automatic gain control (AGC) loop block, which adjusts the digitally controlled VGA in the analog path. The AGC adjusts the amplitude of the incoming signal of interest to a programmable level and prevents the ADC from clipping. The gain of the VGA is subtracted in the relinearization block so that externally the AD6650 appears to have constant gain. For example, if the VGA must increase the gain from 20 dB to 30 dB due to a decrease in the signal power, the relinearization word changes from a −20 dB to a −30 dB gain so that the total AD6650 response is unchanged. The 19-bit output of the AGC block is then decimated and filtered using the CIC4 filter, the IIR filter, and the programmable RAM coefficient filter (RCF). Either 16-bit or 24-bit data is output through the serial port. With the 36 dB VGA gain, 12-bit ADC performance, and approximately 21 dB of processing gain, the AD6650 is capable of delivering approximately 116 dB of dynamic range or 19 bits of performance. For this reason, it is recommended that the 24-bit serial output be used so that dynamic range is not lost.

A block diagram of the digital signal path is shown in Figure 21.

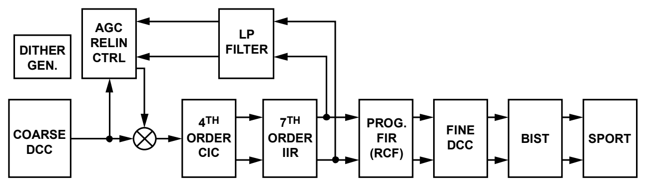


Figure 21. Channel Digital Signal Path

DC CORRECTION

The dc offset in the analog path of the AD6650 comes from three sources: the analog baseband filters, the ADCs, and the LO leakage of the mixers. The dc offsets of the analog filters and the ADCs dominate that of the LO leakage. The dc offsets on the I and Q data for both Channel A and Channel B are different because they use different analog paths. Each path is corrected independently.

The typical uncorrected dc offset is between −32 dB and −35 dB relative to full scale (dBFS) of the ADC. When the AGC range is considered along with this offset, the dc is effectively slid down by the gain setting so that it is approximately −68 dBFS to −71 dBFS or smaller when the AD6650 is in maximum gain.

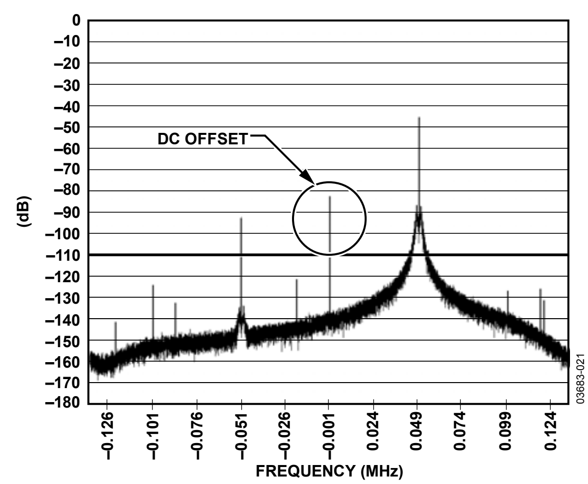


Figure 22. Uncorrected DC Offset

Coarse DC Correction

The coarse dc correction block is a simple integrate-and-dump that integrates the data for 16,384 cycles at the ADC clock rate (typically 26 MSPS) and then updates an estimate of the dc. This estimate is then subtracted from the signal path. The signal is clipped after the subtraction to avoid numerical wrap around with large signals.

The −32 dBFS to −35 dBFS uncorrected offset is sufficient to demodulate large signals, but it does not leave any margin if 30 dB of signal-to-dc is desired. It is essential to consider the dc offset of the signal at the point where the AGC of the AD6650 begins to range. This is important because once the signal or a blocker is in the range of the AGC loop, the dc signal that appears at the output of the AD6650 is modulated by the change in gain of the loop. If the gain decreases, the signal at the output remains at the same power level due to the digital relinearization, but the dc signal at the output is gained up by the relinearization process. For this reason, the coarse dc correction is used to provide additional correction before relinearizing the data to provide additional margin. This block gains another 5 dB to 8 dB (sometimes up to 25 dB) of dc rejection that provides additional margin.

The coarse dc correction is provided for two reasons:

- To provide additional margin on the carrier-to-dc term for large input signals.
- To provide more range for the fine dc correction upper threshold by decreasing the total input power to the block for small input signals. (This is described in more detail in the Fine DC Correction section.)

FOURTH-ORDER CASCADED INTEGRATOR COMB FILTER (CIC4)

The CIC4 processing stage implements a fixed-coefficient decimating filter. It reduces the sample rate of the signal and allows subsequent filtering stages to be implemented more efficiently. The input of the CIC4 is driven by the 19-bit relinearized data at a maximum input rate of 26 MHz (52 MHz clock rate).

The CIC4 decimation ratio, M_{CIC4}, can be programmed from 8 to 32 (all integer values). The CIC4 scale factor, S_{CIC4}, is a programmable unsigned integer between 0 and 8. It serves to control the attenuation of the data into the CIC4 stage in 6 dB increments such that the CIC4 does not overflow. Because this scale factor is in 6 dB steps, the CIC4 filter has a gain between 0 dB and −6.02 dB when properly scaled. For the best dynamic range, S_{CIC4} should be set to the smallest value possible (lowest attenuation) without creating an overflow condition.

$$S_{CIC4} = Ceil\left(4 \times \log_2(M_{CIC4})\right) - 12 \qquad (4)$$

$$CIC\_Gain = \frac{{M_{CIC4}}^4}{2^{S_{CIC4}+12}} \qquad (5)$$

The value of 12 that is subtracted in Equation 4 comes from the amount of scaling needed to compensate for the minimum decimation of 8. The frequency response of the CIC4 filter is given by Equation 6 and Equation 7. The gain and pass-band droop of the CIC4 can be calculated using these equations. If the gain and/or droop of the CIC4 filter are not acceptable, they can be compensated for in the programmable RCF filter stage.

$$CIC4(Z) = \left(\frac{1}{M_{CIC4}} \times \frac{1 - Z^{-M_{CIC4}}}{1 - Z^{-1}}\right)^4 \times CIC\_Gain \qquad (6)$$

$$CIC4(f) = \left(\frac{1}{M_{CIC4}} \times \frac{\sin\left(\pi \times \frac{f \times M_{CIC4}}{f_{ADC}}\right)}{\sin\left(\pi \times \frac{f}{f_{ADC}}\right)}\right)^4 \times CIC\_Gain \qquad (7)$$

The output rate of this stage is given by Equation 8.

$$f_{SAMP4} \le \frac{f_{ADC}}{M_{CIC4}} \qquad (8)$$

CIC4 Rejection

Table 10 shows the amount of bandwidth as a percentage of the input sample rate (ADC sample rate) that can be protected with various decimation rates and alias rejection specifications. The maximum input rate into the CIC4 is 26 MHz. Table 10 shows the half-bandwidth characteristics of the CIC4.

Table 10. SSB CIC4 Alias Rejection Table

	dB					
Rate	**−50**	**−60**	**−70**	**−80**	**−90**	**−100**
8	2.494	1.921	1.473	1.128	0.860	0.651
9	2.224	1.713	1.315	1.007	0.768	0.581
10	2.006	1.546	1.187	0.909	0.693	0.525
11	1.827	1.408	1.081	0.828	0.632	0.478
12	1.676	1.292	0.992	0.760	0.580	0.439
13	1.549	1.194	0.917	0.703	0.536	0.406
14	1.439	1.110	0.852	0.653	0.499	0.378
15	1.344	1.037	0.796	0.610	0.466	0.353
16	1.261	0.972	0.747	0.572	0.437	0.331
17	1.187	0.916	0.703	0.539	0.411	0.312
18	1.122	0.865	0.665	0.509	0.389	0.295
19	1.063	0.820	0.630	0.483	0.369	0.279
20	1.010	0.779	0.599	0.459	0.350	0.265
21	0.962	0.742	0.570	0.437	0.334	0.253
22	0.919	0.709	0.544	0.417	0.319	0.241
23	0.879	0.678	0.521	0.399	0.305	0.231
24	0.842	0.650	0.499	0.383	0.292	0.221
25	0.809	0.624	0.479	0.367	0.281	0.212
26	0.778	0.600	0.461	0.353	0.270	0.204
27	0.749	0.578	0.444	0.340	0.260	0.197
28	0.722	0.557	0.428	0.328	0.251	0.190
29	0.697	0.538	0.413	0.317	0.242	0.183
30	0.674	0.520	0.400	0.306	0.234	0.177
31	0.653	0.503	0.387	0.297	0.226	0.171
32	0.632	0.488	0.375	0.287	0.219	0.166

Table 10 enables the calculation of an upper bound on the decimation ratio (M_{CIC4}), given the desired filter characteristics and input sample rate.

INFINITE IMPULSE RESPONSE (IIR) FILTER

The IIR filter of the AD6650 is a seventh-order low-pass filter with an infinite impulse response. This filter cannot be bypassed and always performs a decimation of 2. As can be seen from the Z-transform, the IIR filter has a gain of –6.02 dB to accommodate signal peaking within the structure. It is designed to be free of limit cycles and is unconditionally stable. The IIR filter is described by the Z-transform and coefficients shown in the following equation:

$$IIR(z) = \frac{\left(n_0 \times z^7 + n_2 \times z^5 + n_3 \times z^3 + n_1 \times z + n_1 \times z^6 + n_3 \times z^4 + n_2 \times z^2 + n_0\right)}{\left(d_7 \times z^7 + d_5 \times z^5 + d_3 \times z^3 + d_1 \times z\right) \times 2} \tag{9}$$

where:

$n_0 = 0.046227$
$n_1 = 0.278961$
$n_2 = 0.76021$
$n_3 = 1.208472$
$d_0 = 0$
$d_1 = 0.12895$
$d_2 = 0$
$d_3 = 0.254698$
$d_4 = 0$
$d_5 = 1.026276$
$d_6 = 0$
$d_7 = 1$

Figure 23 shows the magnitude response of the IIR filter in a typical GSM/EDGE case where the ADCs are sampling at 26 MHz and the CIC filter is decimating by 12 to generate a 2.16 MHz (8× symbol rate) input rate to the IIR.

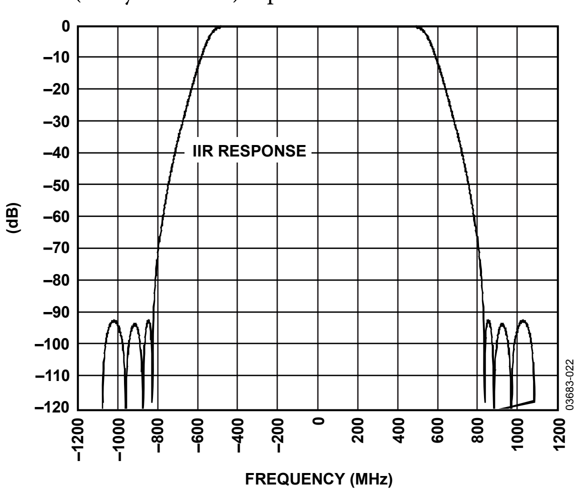


Figure 23. IIR Frequency Response

Figure 24 shows the phase response of the IIR filter over the range of ±100 kHz after a time delay during which ~13.449 input samples of the filter have been removed. The input rate is the same 2.16 MHz from the above GSM/EDGE configuration. Examining the plot shows that the IIR filter is not exactly phase linear. (Linear phase would be flat after the time delay has been removed). It can be seen, however, that the phase response over the band of interest is essentially perfect. From −100 kHz to +100 kHz, the phase distortion is ~0.056° rms. This phase response is several orders of magnitude below the analog LO and analog filter phase distortions.

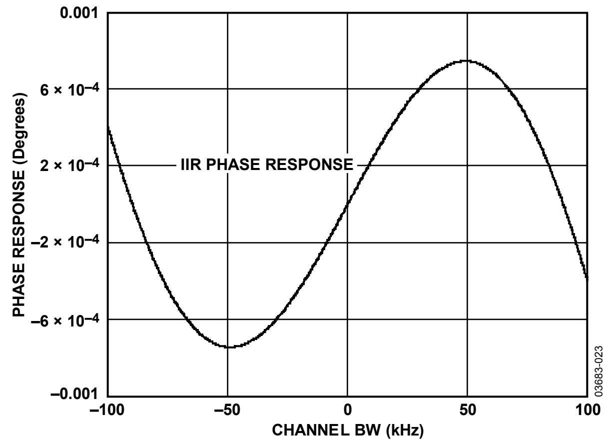


Figure 24. IIR Phase Response

RAM COEFFICIENT FILTER

The final signal processing stage is a sum-of-products decimating filter with programmable coefficients (see Figure 25). The I-RAM and Q-RAM data memories store the most recent complex samples from the IIR filter with 23-bit resolution. The number of samples stored in these memories is equal to the coefficient length (N_{taps}), up to 48 taps. The coefficient memory, CMEM, stores up to 48 coefficients with 20-bit resolution. On every CLK (up to 52 MHz) cycle, one tap for I and one tap for Q are calculated using the same coefficients. The RCF output consists of 16-bit or 24-bit data.

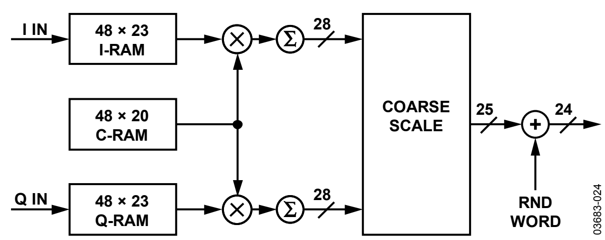


Figure 25. Block Diagram of the RCF

RCF Decimation Register

Each RCF channel can decimate the data rate by a factor of 1 to 8. The decimation register is a 3-bit register. The RCF decimation is stored in Address 0x18 in the form of $M_{RCF} – 1$. The input rate to the RCF is $f_{SAMPIIR}$.

RCF Decimation Phase Register

The AD6650 uses the value stored in this register to preload the RCF counter. Therefore, instead of starting from 0, the counter is loaded with this value, thus creating a time offset in the output data. This data is stored in Address 0x19 as a 3-bit number. Time delays can be achieved in even units of the RCF input rate, which is typically ¼ of the symbol time for GSM.

RCF Filter Length

The maximum number of taps this filter can calculate, N_{taps}, is given by Equation 10. The value $N_{taps} - 1$ is written to the channel register within the AD6650 at Address 0x1B.

$$N_{taps} \le \min\left(\frac{f_{CLK} \times M_{RCF}}{f_{SAMPIIR}}, 48\right) \quad (10)$$

where:

f_{CLK} is the external frequency oscillator.
M_{RCF} is the RCF filter decimation rate.
$f_{SAMPIIR}$ is the input rate to the RCF.

The RCF coefficients are located in Address 0x40 to Address 0x6F, and are interpreted as 20-bit twos complement numbers. When writing the coefficient RAM, the lower addresses are multiplied by relatively older data from the IIR, and the higher coefficient addresses are multiplied by relatively newer data from the IIR. The coefficients need not be symmetric, and the coefficient length, N_{taps}, can be even or odd. If the coefficients are symmetric, both sides of the impulse response must be written into the coefficient RAM.

The RCF stores the data from the IIR into a 46 × 48 RAM. A RAM of 23 × 48 is assigned to I data, and a RAM of 23 × 48 is assigned to Q data.

When the RCF is triggered to calculate a filter output, it starts by multiplying the oldest value in the data RAM by the first coefficient, which is pointed to by the RCF coefficient offset register (Address 0x1A). This value is accumulated with the products of newer data-words multiplied by the subsequent locations in the coefficient RAM until the coefficient address $RCF_{OFF} + N_{taps} - 1$ is reached.

Table 11. Three-Tap Filter

Coefficient Address	Impulse Response	Data
0	h(0)	N(0) oldest
1	h(1)	N(1)
2 = ($N_{taps} - 1$)	h(2)	N(2) newest

The RCF coefficient offset register can be used for two purposes. The main purpose is to allow multiple filters to be loaded into memory and selected simply by changing the offset. The other is to contribute to the symbol timing adjustment. If the desired filter length is padded with 0s on the ends, the starting point can be adjusted to form slight delays in the time the filter is computed with reference to the high speed clock. This allows for vernier adjustment of the symbol timing. Coarse adjustments can be made with the RCF decimation phase.

The output rate of this filter (f_{SAMPR}) is determined by the output rate of the IIR stage and M_{RCF}.

$$f_{SAMPR} = \frac{f_{SAMPIIR}}{M_{RCF}} \quad (11)$$

where:

$f_{SAMPIIR}$ is the input rate to the RCF.
M_{RCF} is the RCF filter decimation rate.

RCF Output Scale Factor and Control Register

Address 0x1C is used to configure the scale factor for the RCF filter. This 2-bit register is used to scale the output data in 6 dB increments. The possible output scales range from 0 dB to −18 dB.

The AD6650 RCF uses a recirculating multiply accumulator (MAC) to compute the filter. This accumulator has three bits of growth, allowing the output of the accumulator to be up to eight times as large as the input signal. To achieve the best filter performance, the coefficients should be as large as possible without overflowing the accumulator. The gain of a filter is merely the sum of the coefficients; therefore, for normal steady state signals, the sum of the coefficients must be less than 8. If the sum of the coefficients is 8 or slightly less, very rare transient events can overflow the accumulator. To prevent this, the sum of the absolute values of the coefficients should be less than 8. It is then impossible for the RCF filter to overflow.

The RCF filter has a 4-position mux at the output of the accumulator. This mux chooses which 24 bits are propagated to the output and adjusts the rounding appropriately. This can be viewed as a gain block that can be varied in 6 dB steps and is controlled by the 2-bit RCF scale register.

The resulting gain of the RCF (RCFgain) is then represented by the following equation:

$$RCFgain = \sum Coef \times \frac{1}{2^{3 - RCFScale}} \quad (12)$$

where *RCFScale* is the value in the RCF scale register.

COMPOSITE FILTER

The total gain of the digital filters can be calculated with Equation 13 and must be less than or equal to 1 (0 dB). Typically, the RCF coefficient gain is scaled to compensate for the gain of the CIC and IIR, and the RCF scale factor is set to 3.

$$Gain = \frac{{M_{CIC4}}^4}{2^{S_{CIC4} + 12}} \times \frac{1}{2} \times \left(\sum Coef \times \frac{1}{2^{3 - RCFScale}}\right) \quad (13)$$

where:

Gain is the gain of the digital filters.
M_{CIC4} is the CIC4 decimation ratio.
S_{CIC4} is the CIC4 scale factor.
RCFScale is the value in the RCF scale register.

The individual responses of the CIC4 and IIR filters, along with the composite response of all the filters, are shown in Figure 26.

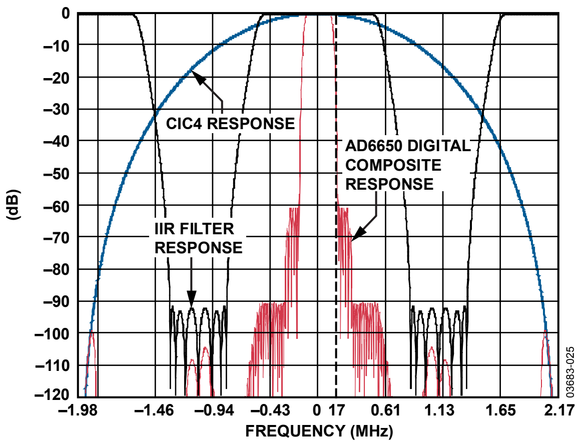


Figure 26. Composite Digital Response with 8× Rate

FINE DC CORRECTION

The fine dc correction block in the AD6650 lies between the RCF and serial output port. While the coarse dc correction block at the front of the channel is included to provide a one-time correction at startup or at rare intervals when commanded by the user, the fine dc correction block is intended to run continuously and track any changes in the dc offsets of the analog front end. To achieve this efficiently under varying signal conditions, this dc estimation process is adaptive.

Adaptive DC Correction Filter

In typical applications where dc offsets are to be corrected, a high-pass filter (HPF) is used to remove the dc and some small percentage of the input signal power. This approach is straightforward and works well when the input signal has a relatively constant power or when the bandwidth of the HPF is extremely small (in the μHz or nHz range) and the dc content does not vary. In general, the more the input signal power can vary, the narrower the bandwidth of the high-pass filter must be to avoid low frequency transients in the filter that are larger than the smallest expected signals. A fundamental trade-off exists because if the high-pass filter has a very low bandwidth, it can only track very slow changes (over hours, days, or weeks) in the dc offsets of the device. On the other hand, if it has a higher bandwidth, it may not be able to estimate the dc properly in the presence of a large baseband signal.

Given the assumption that the signal of interest is uniformly distributed across frequency, the processing gain equation can be used to provide a starting point for system optimization. Enough processing gain must be guaranteed for the dc estimate to be valid for a minimum signal case. This is typically 20 dB to 30 dB but depends on the baseband signal processing of a particular system. For GSM/EDGE, which is distributed over ~100 kHz single sideband (SSB), this implies that the HPF bandwidth must be between 100 Hz to 1 kHz SSB. For every 6 dB that the signal power increases, 6 dB more processing gain is required; therefore, the HPF bandwidth needs to decrease by a factor of 4 or more.

(14)

$$PG = 10 \times \log\left(\frac{f_{BW}}{f_{HPF}}\right) \tag{14}$$

where:

f_{BW} is the channel filter bandwidth.
f_{HPF} is the HPF bandwidth.

In the case of GSM, a simple HPF is not well suited to this problem because the signal power can vary 50 dB or more from time slot to time slot and has a total dynamic range of 91 dB or more. A large time slot would excite the impulse response of the HPF, possibly resulting in a peak occurring later when a small time slot is present. To provide a more optimal dc correction, the AD6650 adaptively adjusts the bandwidth of the HPF based on the signal power. As the signal level decreases, the HPF bandwidth increases. Conversely, as the signal level increases, the HPF bandwidth decreases.

The AD6650 implements this high-pass filter in the form of an accumulator that integrates a number of samples of the output of the RCF and produces an estimate after the samples are accumulated. The estimated dc is then removed from the signal path by a simple subtraction. The subtraction is clamped to avoid overflow problems. The HPF bandwidth is varied by changing the integration time (equivalent to a SYNC 1 filter decimation of the integrator). The integration time is varied based on the output of a peak detector circuit according to the process described in the Peak Detector DC Correction Ranging section.

PEAK DETECTOR DC CORRECTION RANGING

The peak detector of the AD6650 always looks at the maximum signal power present in the I or Q data path. The I and Q paths are treated totally independently in the dc correction circuitry because the analog paths are not guaranteed to match. The first sample that arrives is rectified and preloaded into the peak detector. A control counter is set to the minimum period control register setting. On every input sample, the peak detector determines if the new sample is larger than the currently held sample, and if so, the peak detector is updated. The contents of the peak detector are then examined. If they are below the lower threshold, the control counter counts down and when it reaches 0, it updates the dc estimate, resets the dc accumulator, and reloads the peak detector with the newest input sample magnitude. If the peak detector value is above the upper threshold of the dc correction, the estimate currently being calculated is discarded. When the signal drops below the upper threshold, the calculation of a new dc estimate begins. The current estimate is held, so the last known dc content continues to be removed.

The AI, AQ, BI, and BQ paths of the AD6650 are each treated independently in the dc correction circuitry because the analog paths are not guaranteed to match, and separate dc estimates need to be kept for each. Separate peak detectors, dc estimate accumulators, dc estimate subtractors, and control counters are implemented for each of these paths.

Peak Detector

The peak detector always stores the input sample with the largest magnitude. The absolute value of every input sample is compared to what is currently in the peak detector's holding register. The only exception is when the control counter reaches 0; at this point, the dc offset estimate is updated and the peak detector is set to the current input magnitude. The output of each of the peak detectors is then encoded into a digital word that represents the signal power in 6 dB steps relative to full scale (FS).

DC Accumulator

The dc accumulator accumulates the 24-bit samples input from the RCF filter until the control counter reaches 0. At this time, the dc estimate in the holding register is updated, and the accumulator is directly loaded with the new input sample to begin work on the next estimate.

Control Counter

This counter controls the update of the dc correction block based on the peak detector value and the input control registers. The following three conditions are possible:

- If the digital word from the peak detector indicates that the desired signal is below the lower threshold, the counter merely cycles through at the minimum period.
- If the digital word from the peak detector indicates that the desired signal is above the upper threshold, the control counter is held at the minimum period value and does not count down; therefore, no update is made. When the signal returns below the upper threshold, this counter resumes counting.
- If the digital word from the peak detector indicates that the desired signal is between the lower threshold and the upper threshold, the fine dc correction circuit is in its normal mode of operation. In this mode, the control counter starts with the minimum period but is reloaded with 4× minimum period every time the peak detector output words increment by 6 dB. This errs on the side of caution and ensures that the dc correction integrates long enough to obtain a valid estimate. If smaller integrations are preferred, the minimum period can be decreased or the lower threshold can be raised.

The integration period is given by Equation 15 and Equation 16. The factor of 2 in the exponent shows that as peak signal power increases, the integration time is increased by a factor of 4. This decreases the bandwidth of the estimation filter, thus providing the additional processing gain in the dc estimation term.

When the desired signal power equals the upper threshold,

$$I\_P = 2^{Min\_Period + Ceil\left(\frac{|Upper\_Threshold - Lower\_Threshold|}{6.02}\right)\times 2} \tag{15}$$

When the desired signal power is less than the upper threshold,

$$I\_P = 2^{Min\_Period + Ceil\left(\frac{|Desired\_Signal\_Power - Lower\_Threshold|}{6.02}\right)\times 2} \tag{16}$$

where *Min_Period*, *Upper_Threshold*, and *Lower_Threshold* are register-programmable values.

To calculate the time required for the fine dc correction to converge, use the following equation:

$$Fine\_DC\_Converge = \frac{I\_P \times T_{SYM}}{60} \tag{17}$$

where:

T_{SYM} is the output symbol rate of the AD6650.
Fine_DC_Converge is expressed in minutes, and for a GSM application with 1× oversampling, it is 3.69×10^{-6}.

USER-CONFIGURABLE BUILT-IN SELF-TEST (BIST)

The AD6650 includes a BIST to assess digital functionality. This feature verifies the integrity of the main digital signal paths of the AD6650. Each BIST register is independent, meaning that each channel can be tested independently at the same time.

The BIST is a thorough test of the selected AD6650 digital signal path. With this test mode, it is possible to use the internal pseudorandom generator to produce known test data. A signature register follows the fine dc correction block. This register can be read back and compared to a known good signature. If the known good signature matches the register value, the channel is fully operational.

If an error is detected, each internal block can be bypassed and another test can be run to debug the fault. The I and Q paths are tested independently. Use the following steps to perform this test:

1. Reset the AD6650.
2. Program the desired AD6650 channel parameters for the desired application (these parameters include decimation rates, scalars, and RCF coefficients). Also, ensure that the start holdoff counter is set to a nonzero value.
3. Set Register 0xA, Bit 1, to 1 (PN_EN).
4. Set Register 0x21, Bit 8, to 0 (fine DCC to BIST).
5. Start the A and/or B channels with a microprocessor write (Soft_SYNC) or a pulse on the SYNC pin (Pin_SYNC).
6. Wait at least 300 µs.
7. Read the four BIST registers and compare the values to a known good device. This ensures that the AD6650 is programmed correctly and that each channel is functioning correctly.

LO SYNTHESIS

The AD6650 has a fully integrated quadrature LO synthesizer consisting of a voltage-controlled oscillator (VCO) and a phase-locked loop (PLL). Together these blocks generate quadrature IF LO signals for the demodulators.

Figure 27 shows a block diagram of the LO synthesis block. Besides the usual PLL and VCO, there is also a programmable half-rate divider (Div-X and a fixed divide-by-4 quadrature divider that produces the final I and Q LO signals).

VCO

The VCO generates an on-chip RF signal in the range of 2.2 GHz to 2.8 GHz. The only external component required is a bypass capacitor for the low dropout (LDO) voltage regulator used to power the VCO tank core. The VCO uses overlapping bands to achieve the wide tuning range while maintaining excellent phase noise and spurious performance. During band selection, which takes 5 PFD cycles, the VCO V_{TUNE} is disconnected from the output of the loop filter and connected to an internal reference voltage. After band select, normal PLL action resumes. The nominal value of K_V is 65 MHz/V, where K_V is the VCO sensitivity.

Immediately following the VCO is a programmable half-rate divider that has settings of divide-by-2, -2.5, -3, -3.5, and so on, up to divide-by-8. This function divides the VCO frequency down to four times the LO frequency and effectively extends the tuning range of the VCO. The VCO and the half-rate divider can be thought of as a single lower frequency VCO with a frequency range of 280 MHz to 1040 MHz.

Autocalibration selects both the VCO operating band and the oscillator amplitude to ensure peak operating performance across the entire frequency range. The half-rate divide setting is also selected as part of the VCO calibration. Autocalibration is performed whenever PLL Register 3 (the test mode latch) is written; therefore, all other PLL registers should be set first, and Register 3 should be written to last. This is true whenever programming any portion of the LO synthesizer because the VCO may need to recalibrate itself, depending on the changes made to the registers.

PLL

The integer-N type PLL consists of a programmable reference divider (R-divider), a prescaler and feedback divider (N-divider), a phase-frequency detector (PFD), and a charge pump. The output of the charge pump drives an external loop filter, which in turn drives the input of the VCO.

R-Divider

The 14-bit R-divider divides down the input clock frequency to produce the reference frequency for the phase-frequency detector. Although division ratios from 1 to 16,383 are allowed, the maximum update rate for the PFD is 1 MHz. The selected update rate of the PFD and the subsequent charge pump determines the spurious performance of the LO synthesizer; therefore, the PFD reference frequency should be set for optimal placement of spurs.

Prescaler and Feedback Dividers

The dual modulus prescaler, P/(P + 1), and the A and B feedback dividers (5 bits and 13 bits, respectively) combine to provide a wide ranging N-divider in the PLL feedback loop. The feedback division is N = 8B + A. Including the final quadrature divider (divide-by-4), the LO frequency is given by

$$f_{LO} = \frac{f_{CLK} \times \left(B \times 8 + A\right)}{4R} \quad (18)$$

where:

f_{LO} is the local oscillator frequency.
f_{CLK} is the external frequency oscillator.
B is the 13-bit divider (3 to 8191).
A is the 5-bit swallow divider (0 to 31).
R is the input reference divider (1 to 16,384).

The f_{CLK}/4R term combines the effects of the reference divider and the final quadrature divider, and determines the frequency spacing for the LO synthesizer. For a typical GSM application, f_{CLK} = 52 MHz and R = 65 result in a 200 kHz PFD update rate, which sets the frequency spacing at a desired 200 kHz. However, this also places LO spurs at offsets of 200 kHz multiples, which might degrade the interferer/blocker performance.

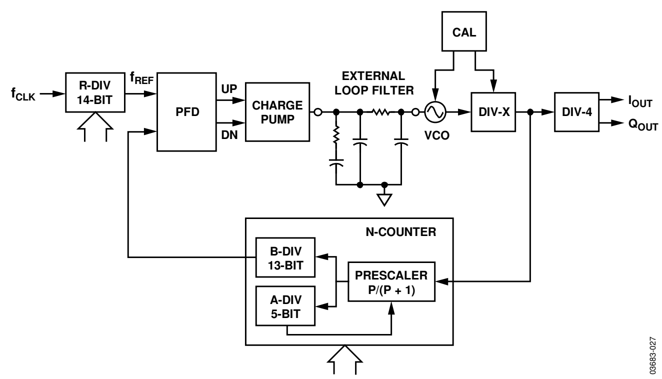


Figure 27. PLL Circuit

PFD and Charge Pump

The phase-frequency detector (PFD) takes inputs from the R-divider and N-divider and produces an output proportional to the phase and frequency difference between them. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes reference spurs.

Loop Filter

The final element in the LO synthesizer is the external loop filter, which is generally a first-order or second-order RC low-pass filter. A filter like the one shown in Figure 28 is recommended to provide a good balance of stability, spurs, and phase noise. This partiular filter is optimized for an update rate of 1 MHz.

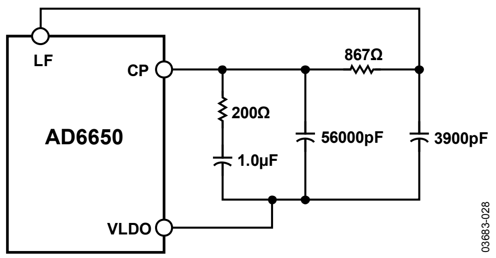


Figure 28. Loop Filter Circuit

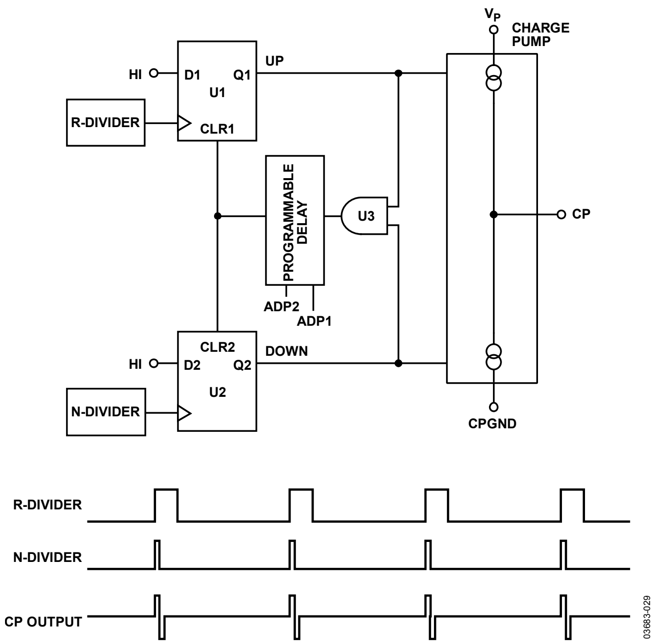


Figure 29. PFD Simplified Schematic and Timing (Locked)

LDO

The AD6650 includes an on-chip 2.6 V low dropout (LDO) voltage regulator that supplies the VCO and other sections of the PLL. A 0.22 µF bypass capacitor is required on the VLDO output to ensure stability. This LDO employs the same technology used in the anyCAP® line of regulators from Analog Devices, Inc., making it insensitive to the type of capacitor used. Driving an external load from the VLDO output is not supported.

AGC LOOP/RELINEARIZATION

The AGC consists of three gain control loops: a slow loop, a fast attack (FA) loop, and a fast decay (FD) loop.

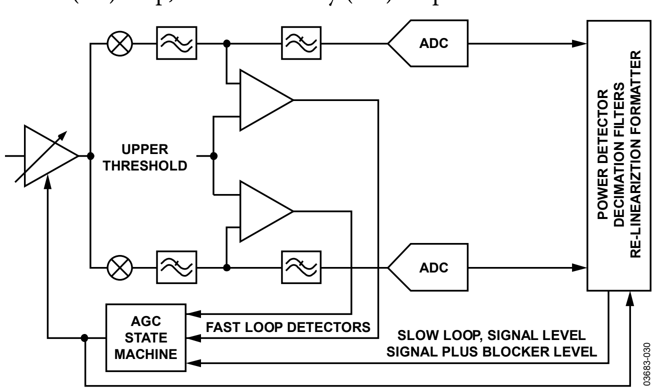


Figure 30. AGC Loop Block Diagram

Slow Loop

The slow loop is the main loop and is associated with a loop gain parameter. This parameter controls the rate of change of the gain and should always be less than 1. To determine the loop gain, Equation 19 should be used.

$$AGCLoopGain = \left(\frac{K_{Mantissa}}{256}\right) \times 2^{-K_{Exponent}} \quad (19)$$

where:

$K_{Mantissa}$ is the loop gain mantissa. Values can range from 0 to 63.
$K_{Exponent}$ is the loop gain exponent. Values can range from 0 to 7.

As the loop gain value increases, the speed of the response of the AGC loop increases; as the loop gain value decreases, so does the speed of the response of the AGC loop. The slow loop attempts to maintain the signal entering the ADC at a given level, referred to as the requested level. This level is specified in dBFS and can be between 0 dBFS and −24 dBFS (in 0.094 dB steps) of the converter resolution. The default value is −6.02 dBFS. The slow loop has a peak detection function, the period of which can be set by the user. This period should be set to ¼ of the symbol period, or greater, to prevent the AGC loop from gaining off the envelope of the EDGE signal. This detection period works because the peak detector's operation is based on dB (max(|I|, |Q|)); therefore, all of the I/Q samples are reflected back into one quadrant of the I/Q plane. At a 26 MHz sampling frequency, one symbol period is 96 clock cycles. Therefore, to obtain a peak detector period that is ¼ of the symbol period, the peak detector period should be set to a minimum of 24 samples. The following equation can also be used:

$$SPB\ Peak\ Samples \geq \tfrac{1}{4} \times \left(f_{SAMP} / f_{SYM}\right) \quad (20)$$

where:

f_{SYM} = 270.833 kHz (GSM symbol rate).
f_{SAMP} = 26 MHz.

Fast Attack (FA) Loop

The FA loop utilizes an analog threshold detector that prevents overdrive of the analog signal path. In a situation that could potentially overdrive the ADC, the FA loop takes over from the slow loop and decreases the gain to the VGA in the front end. The step size used for the FA loop is programmable between 0 dB and 1.504 dB in 0.094 dB steps. The FA loop also has a counter that is programmable between 1 and 16. When initialized to count + 1, the FA loop decreases the gain for count + 1 clock cycles when the threshold is crossed.

Fast Decay (FD) Loop

The FD loop is a fast loop that increases the gain when the signal falls below a threshold during a deep channel fade or on the ramp down. The fast loop accomplishes this task by comparing the peak signal-plus-blocker level at the ADC output (which includes the signal and any blockers that pass through the SAW filter) with a programmable level (SPB_level) that determines when this loop is activated. The SBP_level default value is −40 dBFS. When the wideband signal is below the SPB level, the FD loop is activated. This loop overrides the slow loop and has a programmable step size (default 0.094 dB) and a programmable peak detect period (defaults four samples at 1.08 MHz).

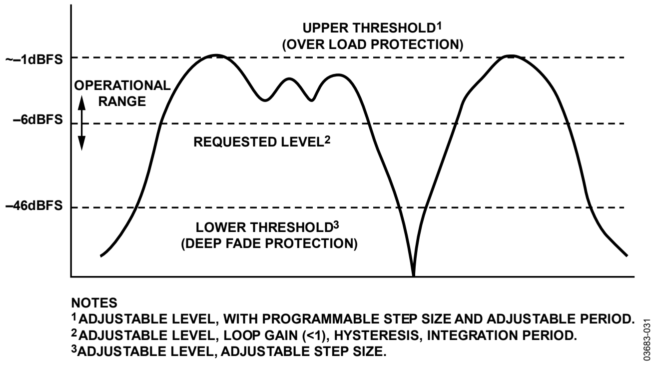


Figure 31. AGC Thresholds

SERIAL OUTPUT DATA PORT

The AD6650 has two configurable serial output ports (SDO0 and SDO1). Both ports must be identically configured and are programmed using the same control register. The ports share a common SFDS, SCLK, and DR pin for connection to an external ASIC or DSP; therefore, the outputs cannot be programmed independently.

Serial Output Data Format

The AD6650 utilizes a twos complement data format with a selectable serial data-word length of 16 bits or 24 bits. The data is shifted out of the device in MSB-first format.

Serial Data Frame Sync

The serial data frame sync (SDFS) pin signals the start of the serial data frame. As channel data becomes available at the output of the AD6650's filters, this data is transferred into the serial data buffer. The internal serial controller initiates the SDFS on the next rising edge of the serial clock. In the AD6650, there are three modes in which the frame sync can be generated, which are described in the SDFS Modes section.

Configuring the Serial Ports

Both serial output ports must function as master serial ports. A serial bus master provides SCLK and SDFS outputs. Serial Port 0 and Serial Port 1 must be programmed as the bus masters by setting Bit 3 of the serial control register high.

Serial Port Data Rate

The SCLK frequency is defined by Equation 21.

$$f_{SCLK} = \frac{f_{CLK}}{SDIV + 1} \quad (21)$$

where:

f_{CLK} is the frequency of the master clock of the AD6650 channel.
SDIV is the serial division word for the channel.

The SDIV for Serial Port 0 and Serial Port 1 can be programmed via Internal Control Register 0x21. Valid SDIV values are between 0 and 7, corresponding to divide ratios between 1 and 8.

Serial Output Frame Timing

The SDFS signal transitions high to signal the start of a data frame. On the next rising edge of SCLK, the port drives the first bit of the serial data on the SDO pin. The falling edge of SCLK or the subsequent rising edge can then be used by the DSP to sample the data until the required number of bits is received (determined by the serial output port word length). If the DSP has the ability to count bits, it can identify when the complete frame is received.

Serial Port Timing Specifications

Figure 32 to Figure 35 indicate the timing required for the AD6650 serial port.

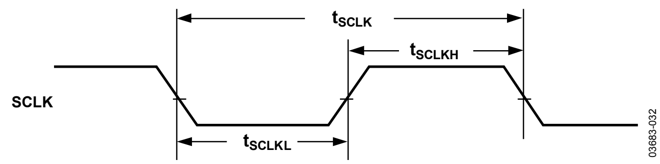


Figure 32. SCLK Timing Requirements

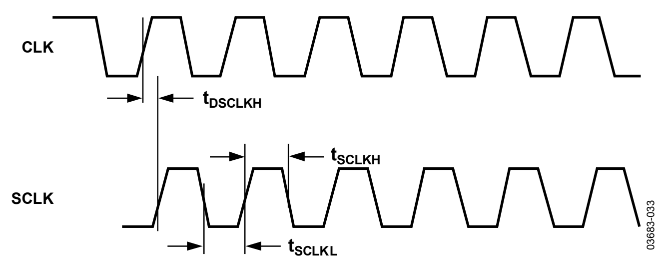


Figure 33. SCLK Switching Characteristics (Divide-by-1)

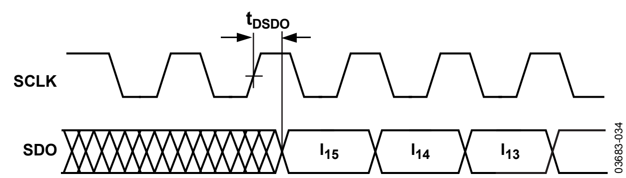


Figure 34. Serial Output Data Switching Characteristics

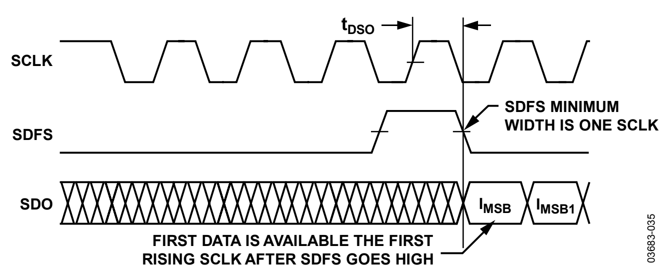


Figure 35. Timing for Serial Output Port

SCLK

SCLK is an output on the AD6650. All outputs are switched on the rising edge of SCLK. The SDFS pin is sampled on the falling edge of SCLK. This allows the AD6650 to recognize the SDFS in time to initiate a frame on the next SCLK rising edge. The maximum speed of this port is 52 MHz.