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12-Bit, 65 MSPS IF to Baseband Diversity Receiver

AD6652

FEATURES

- SNR = 90 dB in 150 kHz bandwidth (to Nyquist @ 61.44 MSPS)
- Worst harmonic = 83 dBc (to Nyquist @ 61.44 MSPS)
- Integrated dual-channel ADC:
  - Sample rates up to 65 MSPS
  - IF sampling frequencies to 200 MHz
  - Internal ADC voltage reference
  - Integrated ADC sample-and-hold inputs
  - Flexible analog input range (1 V to 2 V p-p)
  - Differential analog inputs
  - ADC clock duty cycle stabilizer
  - 85 dB channel isolation/crosstalk
- Integrated wideband digital downconverter (DDC):
  - Crossbar switched DDC inputs
  - Digital resampling for noninteger decimation
  - Programmable decimating FIR filters
  - Flexible control for multicarrier and phased array
  - Dual AGC stages for output level control
  - Dual 16-bit parallel or 8-bit link output ports
  - User-configurable built-in self-test (BIST) capability
  - Energy-saving power-down modes

APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers:
  - GSM, EDGE, PHS, AMPS, UMTS, WCDMA, CDMA-ONE, IS95, IS136, CDMA2000, IMT-2000
- I/Q demodulation systems
- Smart antenna systems
- General-purpose software radios
- Broadband data applications
- Instrumentation and test equipment

FUNCTIONAL BLOCK DIAGRAM

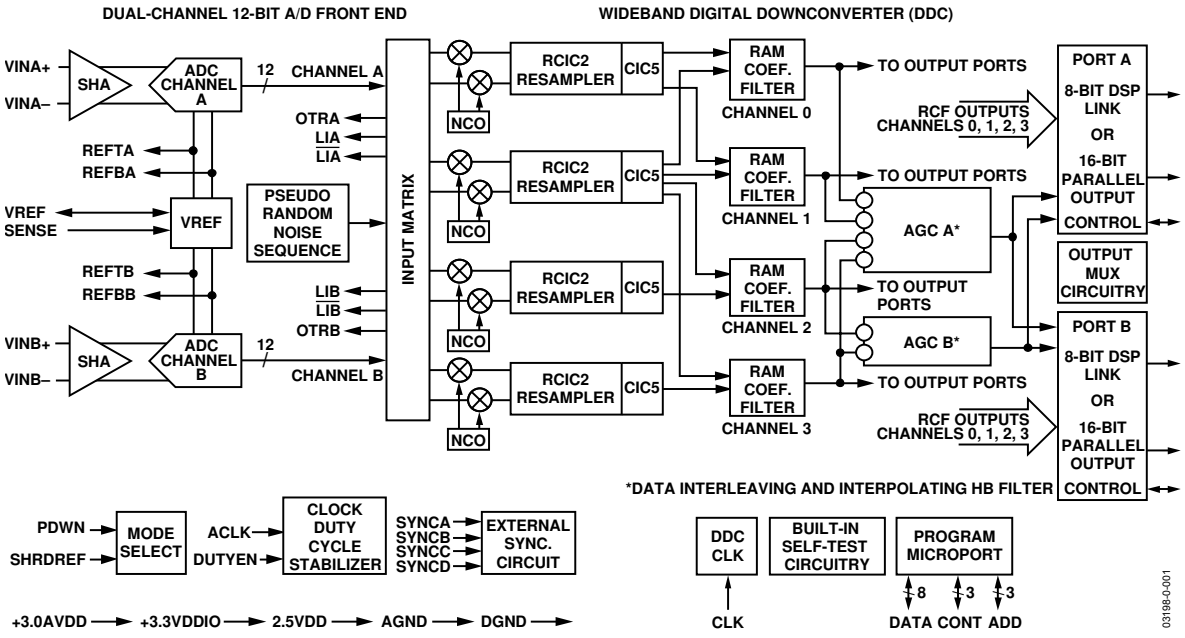

Figure 1.

Rev. 0

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Fax: 781.326.8703

AD6652* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-813: Interfacing the ADSP-BF533/ADSP-BF561 Blackfin®; Processors to High Speed Parallel ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design

Data Sheet

- AD6652: 12-Bit, 65 MSPS IF to Base Band Diversity Receiver Data Sheet

REFERENCE MATERIALS

Technical Articles

- Analog Devices' New Integrated Converter Solutions Reduce Design Costs For Next-Generation Wireless Infrastructures
- Smart Partitioning Eyes 3G Basestation

DESIGN RESOURCES

- AD6652 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD6652 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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REVISION HISTORY

7/04—Revision 0: Initial Version

PRODUCT DESCRIPTION

The AD6652 is a mixed-signal IF to baseband receiver consisting of dual 12-bit 65 MSPS ADCs and a wideband multimode digital downconverter (DDC). The AD6652 is designed to support communications applications where low cost, small size, and versatility are desired. The AD6652 is also suitable for other applications in imaging, medical ultrasound, instrumentation, and test equipment.

The dual ADC core features a multistage differential pipelined architecture with integrated output error correction logic. Both ADCs feature wide bandwidth differential sample-and-hold analog input amplifiers supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

ADC data outputs are internally connected directly to the receiver's digital downconverter (DDC) input matrix, simplifying layout and reducing interconnection parasitics. Overrange bits are provided for each ADC channel to alert the user to ADC clipping. Level indicator bits are also provided for each DDC input port that can be used for external digital VGA control.

The digital receiver has four reconfigurable channels and provides extraordinary processing flexibility. The receiver input matrix routes the ADC data to individual channels, or to all four receive processing channels. Each receive channel has five cascaded signal processing stages: a 32-bit frequency translator (numerically controlled oscillator (NCO)), two fixed-coefficient decimating filters (CIC), a programmable RAM coefficient decimating FIR filter (RCF), and an interpolating half-band filter/AGC stage. Following the CIC filters, one, several, or all channels can be configured to use one, several, or all the RCF filters. This permits the processing power of four 160-tap RCF FIR filters to be combined or used individually.

After FIR filtering, data can be routed directly to the two external 16-bit output ports. Alternatively, data can be routed through two additional half-band interpolation stages, where up to four channels can be combined (interleaved), interpolated, and processed by an automatic gain control (AGC) circuit with 96 dB range. The outputs from the two AGC stages are also routed directly to the two external 16-bit output ports. Each output port has a 16-bit parallel output and an 8-bit link port to permit seamless data interface with DSP devices such as the TS-101 TigerSHARC® DSP. A multiplexer for each port selects one of six data sources to appear on the device outputs pins.

The AD6652 is part of the Analog Devices SoftCell® multimode and multicarrier transceiver chipset. The SoftCell receiver digitizes a wide spectrum of IF frequencies and then downconverts the desired signals to baseband using individual channel NCOs. The AD6652 provides user-configurable digital filters for removal of undesired baseband components, and the data is then passed on to an external DSP, where demodulation and other signal processing tasks are performed to complete the information retrieval process. Each receive channel is independently configurable to provide simultaneous reception of the carrier to which it is tuned. This IF sampling architecture greatly reduces component cost and complexity compared with traditional analog techniques or less integrated digital methods.

High dynamic range decimation filters offer a wide range of decimation rates. The RAM-based architecture allows easy reconfiguration for multimode applications. The decimating filters remove unwanted signals and noise from the channel of interest. When the channel occupies less bandwidth than the input signal, this rejection of out-of-band noise is referred to as *processing gain*. By using large decimation factors, this processing gain can improve the SNR of the ADC by 20 dB or more. In addition, the programmable RAM coefficient filter allows antialiasing, matched filtering, and static equalization functions to be combined in a single, cost-effective filter.

Flexible power-down options allow significant power savings, when desired.

PRODUCT HIGHLIGHTS

- Integrated dual 12-bit 65 MSPS ADC.
- Integrated wideband digital downconverter (DDC).
- Proprietary, differential SHA input maintains excellent SNR performance for input frequencies up to 200 MHz.
- Crossbar-switched digital downconverter input ports.
- Digital resampling permits noninteger relationships between the ADC clock and the digital output data rate.
- Energy-saving power-down modes.
- 32-bit NCOs with selectable amplitude and phase dithering for better than −100 dBc spurious performance.
- CIC filters with user-programmable decimation and interpolation factors.
- 160-tap RAM coefficient filter for each DDC channel.
- Dual 16-bit parallel output ports and dual 8-bit link ports.
- 8-bit microport for register programming, register readback, and coefficient memory programming.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Table 1.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
AVDD	Full	IV	2.75	3.0	3.3	V
VDD	Full	IV	2.25	2.5	2.75	V
VDDIO	Full	IV	3.0	3.3	3.6	V
$T_{AMBIENT}$		IV	−40	+25	+85	°C

ADC DC SPECIFICATIONS

AVDD = 3.0 V, VDD = 2.5 V, VDDIO = 3.3 V, 61.44 MSPS, −1.0 dBFS differential input, 1.0 V internal reference, unless otherwise noted.

Table 2.

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
RESOLUTION	Full	IV	12			Bits
INTERNAL VOLTAGE REFERENCE						
Output Voltage Error (1 V Mode)	Full	IV		±5	±35	mV
Load Regulation @ 1.0 mA	Full	V		0.8		mV
Output Voltage Error (0.5 V Mode)	Full	V		±2.5		mV
Load Regulation @ 0.5 mA	Full	V		0.1		mV
INPUT REFERRED NOISE						
Input Span = 1 V Internal	25°C	V		0.54		LSB rms
Input Span = 2 V Internal	25°C	V		0.27		LSB rms
ANALOG INPUT						
Input Span = 1.0 V	Full	IV		1		V p-p
Input Span = 2.0 V	Full	IV		2		V p-p
Input Capacitance	Full	V		7		pF
REFERENCE INPUT RESISTANCE	Full	V		7		kΩ
MATCHING CHARACTERISTICS						
Offset Error	Full	V		±0.1		% FSR
Gain Error	Full	V		±0.1		% FSR

ADC SWITCHING SPECIFICATIONS

AVDD = 3.0 V, VDD = 2.5 V, VDDIO = 3.3 V, 61.44 MSPS, −1.0 dBFS differential input, 1.0 V internal reference, unless otherwise noted.

Table 3.

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
SWITCHING PERFORMANCE						
Maximum Conversion Rate	Full	IV	65			MSPS
Minimum Conversion Rate	Full	V			1	MSPS
ACLK Period	Full	V	15.4			ns
ACLK Pulse Width High[1]	Full	V	6.2	ACLK/2		ns
ACLK Pulse Width Low[1]	Full	V	6.2	ACLK/2		ns
DATA OUTPUT PARAMETERS						
Wake-Up Time[2]	Full	V		2.5		ms
OUT-OF-RANGE RECOVERY TIME	Full	V		2		Cycles

[1] Duty cycle stabilizer enabled.
[2] Wake-up time is dependent on the value of decoupling capacitors, typical values shown with 0.1 µF and 10 µF capacitors on REFT and REFB.

ADC AC SPECIFICATIONS

AVDD = 3.0 V, VDD = 2.5 V, VDDIO = 3.3 V, 61.44 MSPS, −1.0 dBFS differential input, 1.0 V internal reference.

Table 4.

Parameter (Conditions)		Temp	Test Level	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO[1] (WITHOUT HARMONICS)							
Analog Input Frequency	10.4 MHz	25°C	V		90		dB
		Full	V		90		dB
	25.0 MHz	25°C	II	85	90		dB
		Full	V		90		dB
	68.0 MHz	25°C	II	84	89.5		dB
		Full	V		88.5		dB
	101 MHz	25°C	V		88.0		dB
	150 MHz	25°C	V		87.5		dB
	200 MHz	25°C	V		85		dB
WORST HARMONIC (2^{nd} or 3^{rd})[1]							
Analog Input Frequency	10.4 MHz	25°C	V		−85		dBc
		Full	V		−83		dBc
	25 MHz	25°C	II		−83	−71	dBc
		Full	V		−80		dBc
	68 MHz	25°C	II		−80		dBc
		Full	V		−76		dBc
	101 MHz	25°C	V		−79		dBc
	150 MHz	25°C	V		−72		dBc
	200 MHz	25°C	V		−69		dBc
TWO-TONE IMD REJECTION (TWO TONES SEPARATED BY 1 MHz)[2]							
Analog Inputs = 15/16 MHz		25°C	V		−81		dBc
Analog Inputs = 55/56 MHz		25°C	V		−79		dBc
CHANNEL ISOLATION/CROSSTALK[3]		Full	V		85		dB

[1] Analog Input A or B = single tone @ −1 dB below full scale, 150 kHz DDC filter bandwidth.
[2] Analog Input A or B = each single tone @ −7 dB below full scale, 5 MHz DDC filter bandwidth.
[3] Analog Inputs A and B = each single tone @ −1 dB below full scale at 4.3 MHz and 68 MHz, 150 kHz DDC filter bandwidth.

ELECTRICAL CHARACTERISTICS

AVDD = 3.0 V, VDD = 2.5 V, VDDIO = 3.3 V, 61.44 MSPS, −1.0 dBFS differential input, 1.0 V internal reference, unless otherwise noted.

Table 5.

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
LOGIC INPUTS						
Logic Compatibility	Full	IV		3.3 V CMOS		
Logic 1 Voltage	Full	IV	2.0			V
Logic 0 Voltage	Full	IV			0.8	V
Logic 1 Current	Full	IV	−10		+10	µA
Logic 0 Current	Full	IV	−10		+10	µA
Input Capacitance	25°C	V		4		pF
LOGIC OUTPUTS						
Logic Compatibility	Full	IV		3.3 V CMOS/TTL		
Logic 1 Voltage (V_{OH}) (I_{OH} = 0.25 mA)	Full	IV	2.4	VDDIO − 0.2		V
Logic 0 Voltage (V_{OL}) (I_{OL} = 0.25 mA)	Full	IV		0.2	0.4	V
SUPPLY CURRENTS						
Narrow Band (150 kHz BW) (61.44 MHz CLK) Four Individual Channels						
I_{AVDD}	25°C	II	160	200	215	mA
I_{VDD}	25°C	II	240	280	300	mA
I_{VDDIO}	25°C	II	25	40	45	mA
CDMA (1.25MHz BW) (61.44 MHz CLK) Example[1]						
I_{AVDD}	25°C	V		200		mA
I_{VDD}	25°C	V		336		mA
I_{VDDIO}	25°C	V		68		mA
WCDMA (5 MHz BW) (61.44 MHz CLK) Example[1]						
I_{AVDD}	25°C	V		200		mA
I_{VDD}	25°C	V		330		mA
I_{VDDIO}	25°C	V		89		mA
TOTAL POWER DISSIPATION						
Narrow Band (150 kHz BW) (61.44 MHz CLK) Four Individual Channels	25°C	II	1.2	1.5	1.6	W
CDMA (61.44 MHz)[1]	25°C	V		1.7		W
WCDMA (61.44 MHz)[1]	25°C	V		1.7		W
ADC in Standby and DDC in Sleep Mode[2]	25°C	V		2.3		mW

[1] All signal processing stages and all DDC channels active.
[2] ADC standby power measured with ACLK inactive.

GENERAL TIMING CHARACTERISTICS

All timing specifications valid over VDD range of 2.25 V to 2.75 V and VDDIO range of 3.0 V to 3.6 V.
CLOAD = 40 pF on all outputs, unless otherwise specified.

Table 6.

Parameter (Conditions)		Temp	Test Level	Min	Typ	Max	Unit
CLK TIMING REQUIREMENTS							
t_{CLK}	CLK Period	Full	IV	15.4			ns
t_{CLKL}	CLK Width Low	Full	IV	6.2	$t_{CLK}/2$		ns
t_{CLKH}	CLK Width High	Full	IV	6.2	$t_{CLK}/2$		ns
$\overline{\text{RESET}}$ TIMING REQUIREMENTS							
t_{RESL}	$\overline{\text{RESET}}$ Width Low	Full	IV	30.0			ns
LEVEL INDICATOR OUTPUT SWITCHING CHARACTERISTICS							
t_{DLI}	↑CLK to LI (LIA, $\overline{\text{LIA}}$; LIB, $\overline{\text{LIB}}$) Output Delay Time	Full	IV	3.3		10.0	ns
SYNC TIMING REQUIREMENTS							
t_{SS}	SYNC(A,B,C,D) to ↑CLK Setup Time	Full	IV	2.0			ns
t_{HS}	SYNC(A,B,C,D) to ↑CLK Hold Time	Full	IV	1.0			ns
PARALLEL PORT TIMING REQUIREMENTS (MASTER MODE)							
Switching Characteristics[1]							
$t_{DPOCLKL}$	↓CLK to ↑PCLK Delay (Divide-by-1)	Full	IV	6.5		10.5	ns
$t_{DPOCLKLL}$	↓CLK to ↑PCLK Delay (Divide-by-2, -4, or -8)	Full	IV	8.3		14.6	ns
t_{DPREQ}	↑PCLK to ↑PxREQ Delay					1.0	ns
t_{DPP}	↑PCLK to Px[15:0] Delay					0.0	ns
Input Characteristics							
t_{SPA}	PxACK to ↓PCLK Setup Time			7.0			ns
t_{HPA}	PxACK to ↓PCLK Hold Time			−3.0			ns
PARALLEL PORT TIMING REQUIREMENTS (SLAVE MODE)							
Switching Characteristics[1]							
t_{POCLK}	PCLK Period	Full	IV	12.5			ns
t_{POCLKL}	PCLK Low Period (when PCLK Divisor = 1)	Full	IV	2.0	$0.5 \times t_{POCLK}$		ns
t_{POCLKH}	PCLK High Period (when PCLK Divisor = 1)	Full	IV	2.0	$0.5 \times t_{POCLK}$		ns
t_{DPREQ}	↑PCLK to ↑PxREQ Delay					10.0	ns
t_{DPP}	↑PCLK to Px[15:0] Delay					11.0	ns
Input Characteristics							
t_{SPA}	PxACK to ↓PCLK Setup Time		IV	1.0			ns
t_{HPA}	PxACK to ↓PCLK Hold Time		IV	1.0			ns
LINK PORT TIMING REQUIREMENTS							
Switching Characteristics[1]							
t_{RDLCLK}	↑PCLK to ↑LxCLKOUT Delay	Full	IV			2.5	ns
t_{FDLCLK}	↓PCLK to ↓LxCLKOUT Delay	Full	IV			0	ns
$t_{RLCLKDAT}$	↑LCLKOUT to Lx[7:0] Delay	Full	IV	0		2.9	ns
$t_{FLCLKDAT}$	↓LCLKOUT to Lx[7:0] Delay	Full	IV	0		2.2	ns

[1] The timing parameters for Px[15:0], PxREQ, and PxACK apply for Port A and B (x stands for A or B).

MICROPROCESSOR PORT TIMING CHARACTERISTICS

All timing specifications valid over VDD range of 2.25 V to 2.75 V and VDDIO range of 3.0 V to 3.6 V.
CLOAD = 40 pF on all outputs, unless otherwise specified.

Table 7.

MICROPROCESSOR PORT, MODE INM (MODE = 0)		Temp	Test Level	Min	Typ	Max	Unit
MODE INM WRITE TIMING							
t_{SC}	Control[1] to ↑CLK Setup Time	Full	IV	2.0			ns
t_{HC}	Control[1] to ↑CLK Hold Time	Full	IV	2.5			ns
t_{HWR}	$\overline{WR}$(R/$\overline{W}$) to RDY($\overline{DTACK}$) Hold Time	Full	IV	7.0			ns
t_{SAM}	Address/Data to $\overline{WR}$(R/$\overline{W}$) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to RDY($\overline{DTACK}$) Hold Time	Full	IV	5.0			ns
t_{DRDY}	$\overline{WR}$(R/$\overline{W}$) to RDY($\overline{DTACK}$) Delay	Full	IV	8.0			ns
t_{ACC}	$\overline{WR}$(R/$\overline{W}$) to RDY($\overline{DTACK}$) High Delay	Full	IV	$4 \times t_{CLK}$	$5 \times t_{CLK}$	$9 \times t_{CLK}$	ns
MODE INM READ TIMING							
t_{SC}	Control[1] to ↑CLK Setup Time	Full	IV	5.0			ns
t_{HC}	Control[1] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{SAM}	Address to $\overline{RD}$($\overline{DS}$) Setup Time	Full	IV	0.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	5.0			ns
t_{DRDY}	$\overline{RD}$($\overline{DS}$) to RDY($\overline{DTACK}$) Delay	Full	IV	8.0			ns
t_{ACC}	$\overline{RD}$($\overline{DS}$) to RDY($\overline{DTACK}$) High Delay	Full	IV	$8 \times t_{CLK}$	$10 \times t_{CLK}$	$13 \times t_{CLK}$	ns
MICROPROCESSOR PORT, MODE MNM (MODE = 1)		**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
MODE MNM WRITE TIMING							
t_{SC}	Control[1] to ↑CLK Setup Time	Full	IV	2.0			ns
t_{HC}	Control[1] to ↑CLK Hold Time	Full	IV	2.5			ns
t_{HDS}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{HRW}	R/$\overline{W}$($\overline{WR}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	7.0			ns
t_{SAM}	Address/Data To R/$\overline{W}$($\overline{WR}$) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to R/$\overline{W}$($\overline{WR}$) Hold Time	Full	IV	5.0			ns
t_{DDTACK}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Delay	Full	IV	8.0			ns
t_{ACC}	R/$\overline{W}$($\overline{WR}$) to $\overline{DTACK}$(RDY) Low Delay	Full	IV	$4 \times t_{CLK}$	$5 \times t_{CLK}$	$9 \times t_{CLK}$	ns
MODE MNM READ TIMING							
t_{SC}	Control[1] to ↑CLK Setup Time	Full	IV	5.0			ns
t_{HC}	Control[1] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{HDS}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{SAM}	Address to $\overline{DS}$($\overline{RD}$) Setup Time	Full	IV	0.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	5.0			ns
t_{DDTACK}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Delay	Full	IV	8.0			ns
t_{ACC}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Low Delay	Full	IV	$8 \times t_{CLK}$	$10 \times t_{CLK}$	$13 \times t_{CLK}$	ns

[1] Specification pertains to control signals: R/W, ($\overline{WR}$), $\overline{DS}$, ($\overline{RD}$), and $\overline{CS}$.

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
ELECTRICAL	
AVDD Voltage	−0.3 V to +3.9 V
VDD Voltage	−0.3 V to +2.75 V
VDDIO Voltage	−0.3 V to +3.9 V
AGND, DGND	−0.3 V to +0.3 V
ADC VINA, VINB Analog Input Voltage	−0.3 V to AVDD + 0.3 V
ADC Digital Input Voltage	−0.3 V to AVDD + 0.3 V
ADC OTRA, OTRB Digital Output Voltage	−0.3 V to VDDIO + 0.3 V
ADC VREF, REFA, REFB Input Voltage	−0.3 V to AVDD + 0.3 V
DDC Digital Input Voltage	−0.3 V to VDDIO + 0.3 V
DDC Digital Output Voltage	−0.3 V to VDDIO + 0.3 V
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

256-lead CSPBGA, 17 mm sq.

θ_{JA} = 23°C/W, still air.

Estimate based on JEDEC JC51-2 model using horizontally positioned 4-layer board.

TEST LEVEL

I. 100% production tested.

II. 100% production tested at 25°C.

III. Sample tested only.

IV. Parameter guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 9. BGA Pin Configuration (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	DGND	PA7_LA7	A2	PA6_LA6	D1	D3	$\overline{CS}$	$\overline{RESET}$	MODE	SYNCD	OTRA	PDWN	AVDD	AVDD	AGND	AGND
B	Do Not Connect	PA4_LA4	PACH0_ LACLK OUT	A0	DGND	R/$\overline{W}$ ($\overline{WR}$)	D4	D6	SYNCC	SYNCA	LIA	DUTYEN	AVDD	AVDD	AGND	AGND
C	PA9	PA3_LA3	A1	$\overline{DS}$ ($\overline{RD}$)	D0	D2	D5	D7	$\overline{DTACK}$ (RDY)	SYNCB	$\overline{LIA}$	LIB	AVDD	AVDD	AGND	VIN+B
D	PA1_LA1	PA2_LA2	PACH1_ LACLKIN	VDD	VDD	VDD	VDD	VDDIO	VDDIO	VDDIO	VDDIO	VDDIO	AVDD	AVDD	AGND	VIN−B
E	PA8	PA5_LA5	n.c.	VDD	VDD	VDD	VDD	VDDIO	VDDIO	VDDIO	VDDIO	VDDIO	AVDD	AVDD	AGND	AGND
F	PA0_LA0	DGND	PA10	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	AGND	AGND
G	PA12	PA11	PA13	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	REFBB	REFTB
H	PAREQ	PA15	PA14	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	AGND	SENSE
J	CHIP_ID1	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	AGND	VREF
K	CHIP_ID3	PAACK	CHIP_ID0	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	REFBA	REFTA
L	PB6_LB6	PB7_LB7	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	AGND	AGND
M	CHIP_ID2	PB3_LB3	PB4_LB4	VDDIO	VDDIO	VDDIO	VDDIO	VDD	VDD	VDD	VDD	VDDIO	AVDD	AVDD	AGND	AGND
N	PAIQ	PBCH1_ LBCLK IN	PB2_LB2	VDDIO	VDDIO	VDDIO	VDDIO	VDD	VDD	VDD	VDD	VDDIO	AVDD	AVDD	AGND	VIN−A
P	DGND	PB0_LB0	PB8	PB10	PB14	VDDIO	PBACK	$\overline{LIB}$	n.c.	n.c.	OTRB	n.c.	AVDD	AVDD	AGND	VIN+A
R	PBIQ	PBCH0_L BCLKOUT	PB1_ LB1	PB9	PB12	PB15	n.c.	n.c.	n.c.	n.c.	n.c.	PDWN	AVDD	AVDD	AGND	AGND
T	DGND	PCLK	PB5_ LB5	PB11	PB13	PBREQ	n.c.	n.c.	n.c.	n.c.	DCLK	SHRDREF	AVDD	ACLK	AGND	AGND

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type	Function
POWER SUPPLY			
A13, B13, C13, D13, E13, F13, G13, H13, J13, K13, L13, M13, N13, P13, R13, T13, A14, B14, C14, D14, E14, M14, N14, P14, R14	AVDD	Power	3.0 V Analog Supply, 25 Pins.
D4, D5, D6, D7, E4, E5, E6, E7, M8, M9, M10, M11, N8, N9, N10, N11	VDD	Power	2.5 V Digital Core Supply, 16 Pins.
D8, D9, D10, D11, D12, E8, E9, E10, E11, E12, F12, G12, H12, J12, K12, L12, M4, M5, M6, M7, M12, N4, N5, N6, N7, N12, P6	VDDIO	Power	3.3 V Digital I/O Supply, 27 Pins.
A1, B5, F2, F4, F5, F6, F7, F8, F9, F10, F11, G4, G5, G6, G7, G8, G9, G10, G11, H4, H5, H6, H7, H8, H9, H10, H11, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, K4, K5, K6, K7, K8, K9, K10, K11, L3, L4, L5, L6, L7, L8, L9, L10, L11, P1, T1	DGND	Ground	Digital Ground, 56 Pins.
A15, A16, B15, B16, C15, D15, E15, E16, F14, F15, F16, G14, H14, H15, J14, J15, K14, L14, L15, L16, M15, M16, N15, P15, R15, R16, T15, T16	AGND	Ground	Analog Ground, 28 Pins.
MISCELLANEOUS			
E3, P9, P10, P12, R7, R8, R9, R10, R11, T7, T8, T9, T10	NC	N/A	No Connect, 13 Pins.
B1	DNC	N/A	Do Not Connect.

Pin No.	Mnemonic	Type	Function
ADC INPUTS			
P16	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
N16	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
C16	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
D16	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
J16	VREF	I/O	Voltage Reference Input/Output.
H16	SENSE	Input	Voltage Reference Mode Select.
T14	ACLK	Input	ADC Master Clock.
B12	DUTYEN	Input	Duty Cycle Stabilizer, Active High.
A12, R12	PDWN[1]	Input	Power-Down Enable, Active High.
T12	SHRDREF	Input	Shared Voltage Reference Select, Low = Independent, High = Shared.
ADC OUTPUTS			
A11	OTRA	Output	Out-of-Range Indicator for Channel A, High = Overrange.
P11	OTRB	Output	Out-of-Range Indicator for Channel B, High = Overrange.
K16	REFTA	Output	Top Reference Voltage, Channel A.
G16	REFTB	Output	Top Reference Voltage, Channel B.
K15	REFBA	Output	Bottom Reference Voltage, Channel A.
G15	REFBB	Output	Bottom Reference Voltage, Channel B.
DDC INPUTS			
A8	$\overline{\text{RESET}}$	Input	Master Reset, Active Low.
T11	DCLK	Input	DDC Master Clock.
T2	PCLK	I/O	Link Port Clock Output or Parallel Port Clock Input.
D3	PACH1_LACLKIN[2]	I/O	Channel ID Output Bit, MSB, for Parallel Port A, or Link Port A Data Ready Input. Function depends on logic state of 0x1B:7 of output port control register.
N2	PBCH1_LBCLKIN[2]	I/O	Channel ID Output Bit, MSB, for Parallel Port B, or Link Port B Data Ready Input. Function depends on logic state of 0x1D:7 of output port control register.
B10	SYNCA[3]	Input	Hardware Sync, Pin A, Routed to All Receiver Channels.
C10	SYNCB[3]	Input	Hardware Sync, Pin B, Routed to All Receiver Channels.
B9	SYNCC[3]	Input	Hardware Sync, Pin C, Routed to All Receiver Channels.
A10	SYNCD[3]	Input	Hardware Sync, Pin D, Routed to All Receiver Channels.
K3, J1, M1, K1	CHIP_ID[3:0][3]	Input	Chip ID Selector, Four Pins, Used in Conjunction with Access Control Register Bits 5–2.

Pin No.	Mnemonic	Type	Function
DDC OUTPUTS			
B11	LIA	Output	Level Indicator, Input A, Data A.
C11	$\overline{\text{LIA}}$	Output	Level Indicator, Input A, Data $\overline{\text{A}}$.
C12	LIB	Output	Level Indicator, Input B, Data B.
P8	$\overline{\text{LIB}}$	Output	Level Indicator, Input B, Data $\overline{\text{B}}$.
B3	PACH0_LACLKOUT[2]	Output	Channel ID Output Bit, LSB, for Parallel Port A, or Link Port A Clock Output. Function depends on logic state of 0x1B:7 of output port control register.
R2	PACH0_LBCLKOUT[2]	Output	Channel ID Output Bit, LSB, for Parallel Port B, or Link Port B Clock Output. Function depends on logic state of 0x1D:7 of output port control register.
F1, D1, D2, C2, B2, E2, A4, A2	PA[7:0]_LA[7:0]	Output	Link Port A Data or Parallel Port A Data [7:0], Eight Pins.
P2, R3, N3, M2, M3, T3, L1, L2	PB[7:0_LB[7:0]	Output	Link Port B Data or Parallel Port B Data [7:0], Eight Pins.
E1, C1, F3, G2, G1, G3, H3, H2	PA[15:8]	Output	Parallel Port A Data [15:8], Eight Pins.
P3, R4, P4, T4, R5, T5, P5, R6	PB[15:8]	Output	Parallel Port B Data [15:8], Eight Pins.
N1	PAIQ	Output	Parallel Port A I or Q Data Indicator, I = High, Q = Low.
R1	PBIQ	Output	Parallel Port B I or Q Data Indicator, I = High, Q = Low.
PARALLEL OUTPUT PORT CONTROL			
K2	PAACK	Input	Parallel Port A Acknowledge.
H1	PAREQ	Output	Parallel Port A Request.
P7	PBACK	Input	Parallel Port B Acknowledge.
T6	PBREQ	Output	Parallel Port B Request.
MICROPORT CONTROL			
C5, A5, C6, A6, B7, C7, B8, C8	D[7:0]	I/O	Bidirectional Microport Data, Eight Pins. This bus is three-stated when $\overline{\text{CS}}$ is high.
B4, C3, A3	A[2:0]	Input	Microport Address Bus, 3 Pins.
C4	$\overline{\text{DS}}(\overline{\text{RD}})$[4]	Input	Function depends upon MODE pin. Active Low Data Strobe when MODE = 1. Active Low Read Strobe when MODE = 0.
C9	$\overline{\text{DTACK}}$(RDY)[4, 5]	Output	Function depends upon MODE pin. Active Low Data Acknowledge when MODE = 1. Microport Status Pin when MODE = 0.
B6	R/$\overline{\text{W}}$ ($\overline{\text{WR}}$)[4]	Input	Read/Write Strobe when MODE = 1. Active Low Write strobe when MODE = 0.
A9	MODE[4]	Input	Mode Select Pin. 0 = Intel mode, 1 = Motorola mode.
A7	$\overline{\text{CS}}$[3]	Input	Active Low Chip Select. Logic 1 three-states the microport data bus.

[1] PDWN pins must be the same logic level: both logic high or both logic low.
[2] PACH0 and PACH1 form a 2-bit output word in the parallel output mode that identifies the processing channel (0, 1, 2, or 3) whose data appears on Port A parallel outputs. Likewise, PBCH0 and PBCH1 identify the channel for Port B.
[3] Pins with a pull-down resistor of nominal 70 kΩ.
[4] Mode 0 is Intel nonmultiplexed (IMN), and Mode 1 is Motorola nonmultiplexed (MNM). Pin logic level corresponds to mode.
[5] Pins with a pull-up resistor of nominal 70 kΩ.

TYPICAL PERFORMANCE CHARACTERISTICS

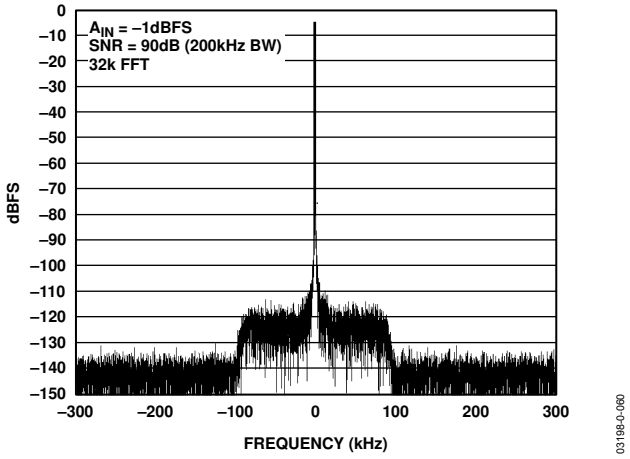

Figure 2. GSM/EDGE with Single Tone A_{IN} = 30 MHz; Encode = 61.44 MSPS

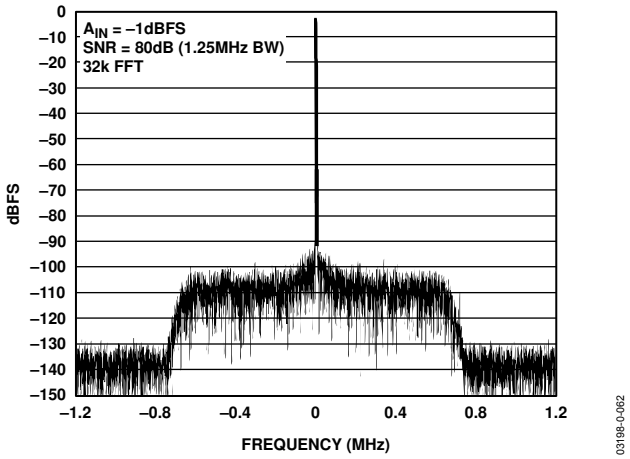

Figure 3. CDMA2000 with Single Tone A_{IN} = 76 MHz; Encode = 61.44 MSPS

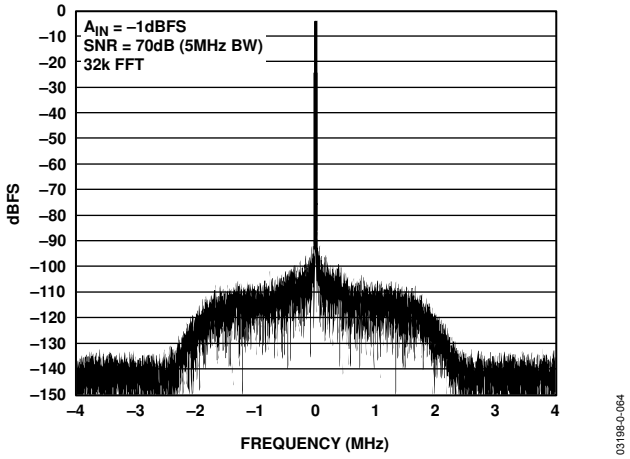

Figure 4. WCDMA with Single Tone A_{IN} = 169 MHz; Encode = 61.44 MSPS

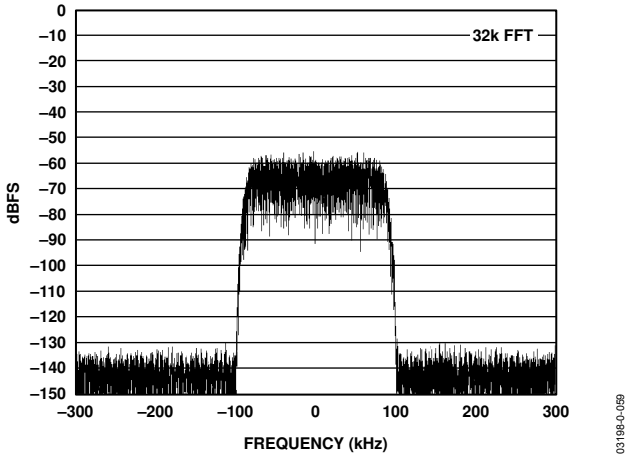

Figure 5. GSM/EDGE Carrier A_{IN} = 30 MHz; Encode = 61.44 MSPS

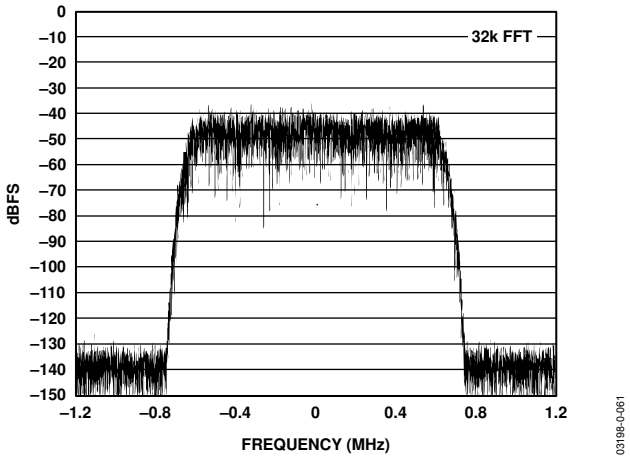

Figure 6. CDMA2000 Carrier A_{IN} = 76 MHz; Encode = 61.44 MSPS

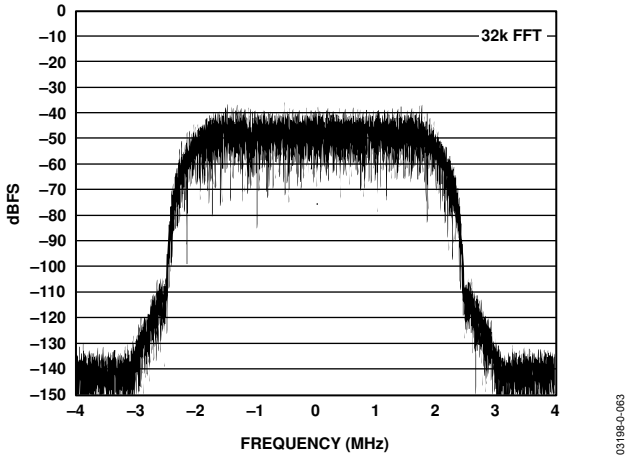

Figure 7. WCDMA Carrier A_{IN} = 169 MHz; Encode = 61.44 MSPS

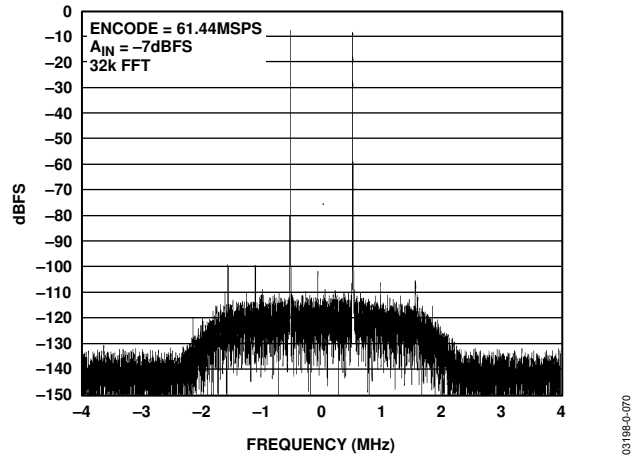

Figure 8. Two Tones at 15 MHz and 16 MHz

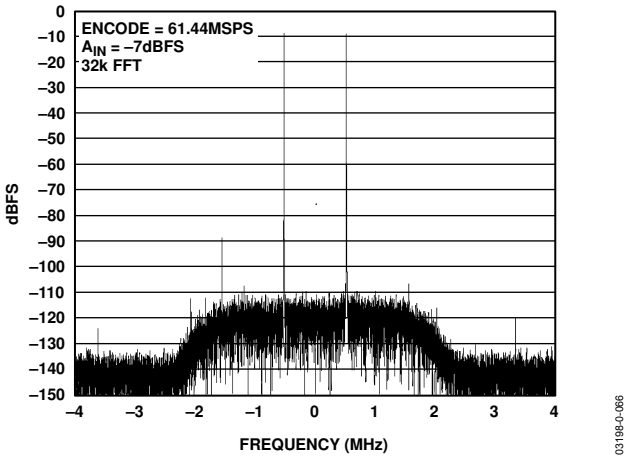

Figure 11. Two Tones at 55 MHz and 56 MHz

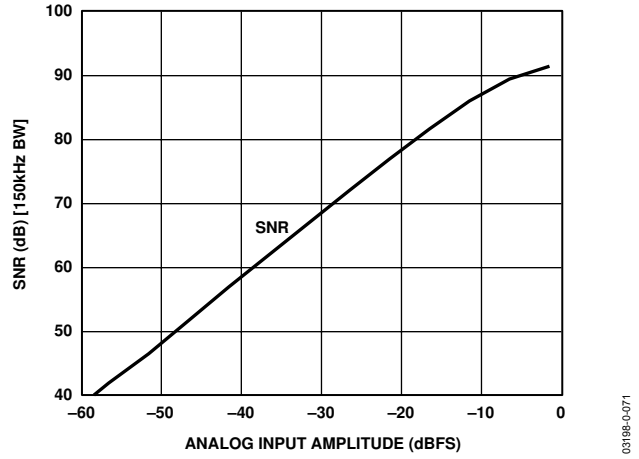

Figure 9. Noise vs. Analog Amplitude at 25 MHz

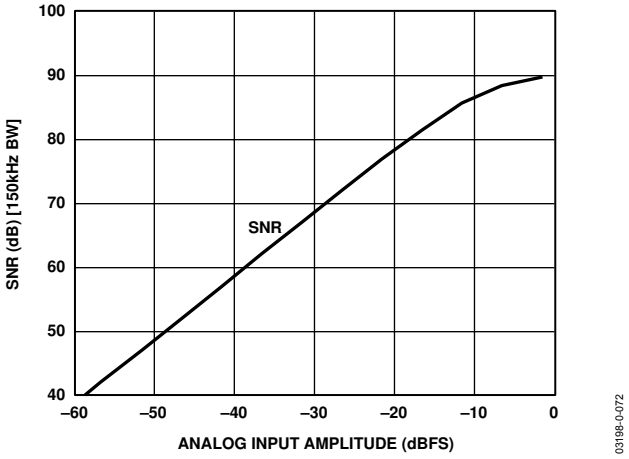

Figure 12. Noise vs. Analog Amplitude at 68 MHz

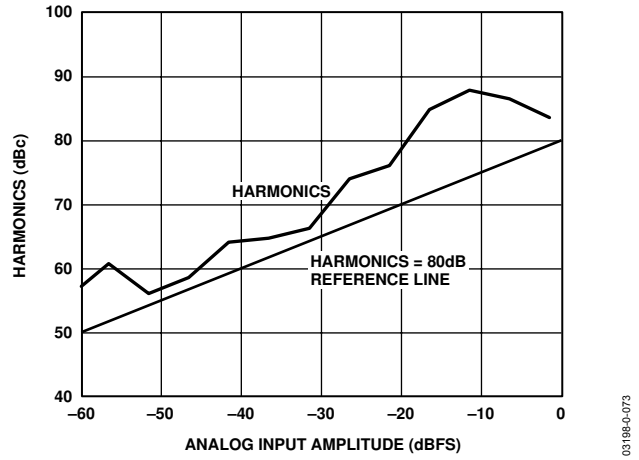

Figure 10. Harmonics vs. Analog Amplitude at 25 MHz

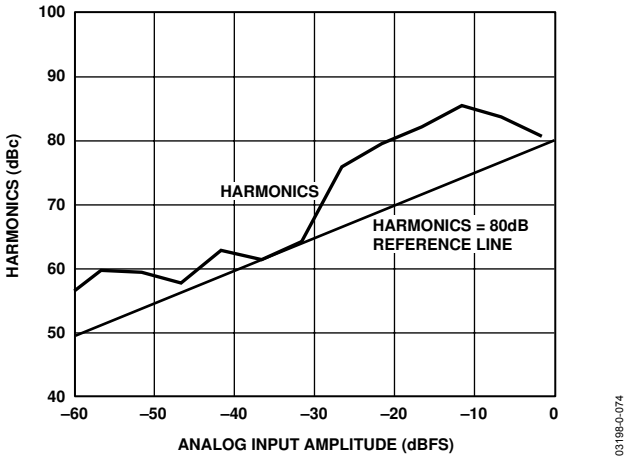

Figure 13. Harmonics vs. Analog Amplitude at 68 MHz

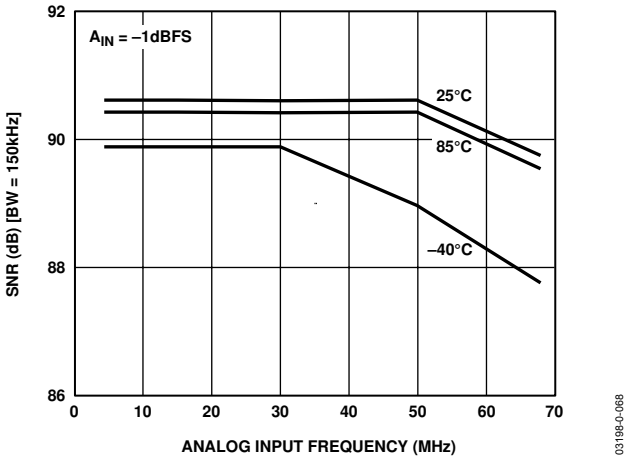

Figure 14. Noise vs. Analog Frequency

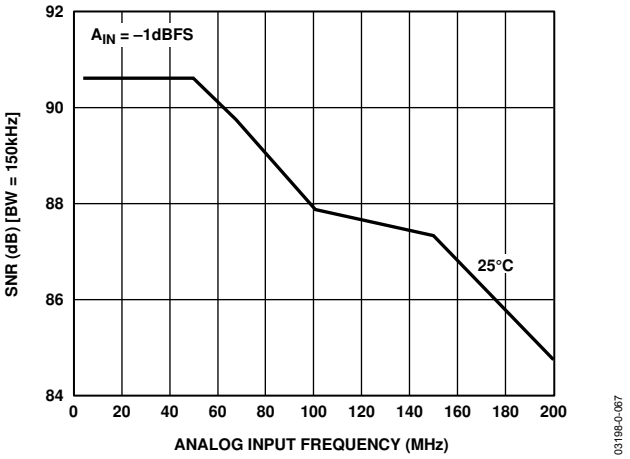

Figure 16. Noise vs. Analog Frequency (IF)

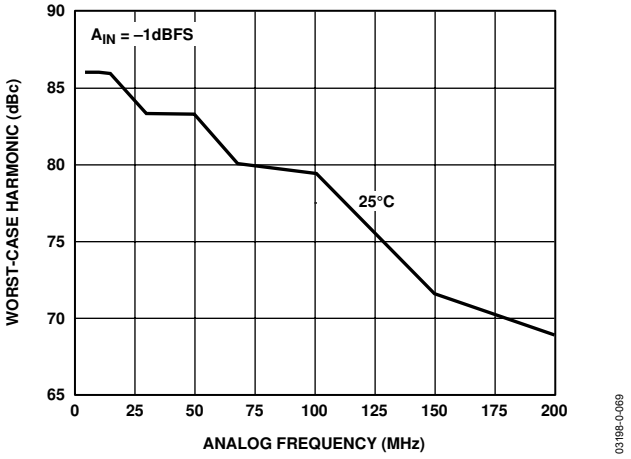

Figure 15. Harmonics vs. Analog Frequency

DDC TIMING DIAGRAMS

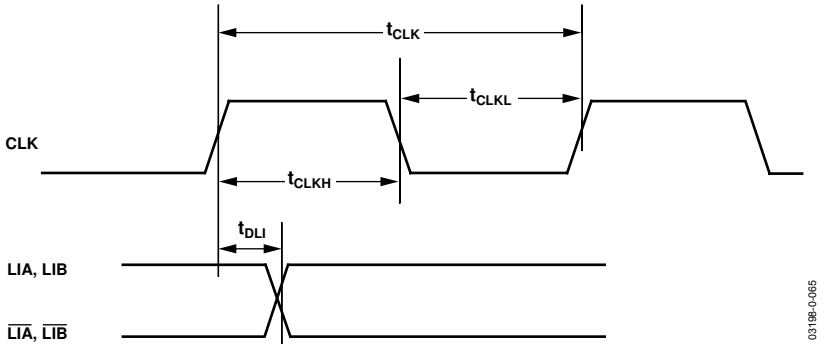

Figure 17. Level Indicator Output Switching Characteristics

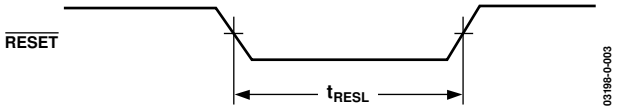

Figure 18. Reset Timing Requirements

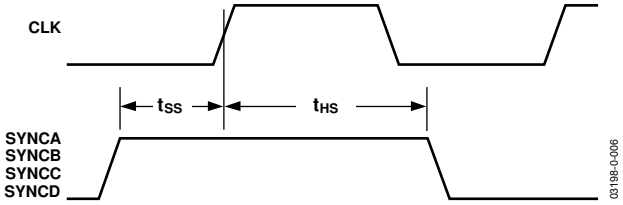

Figure 19. SYNC Timing Inputs

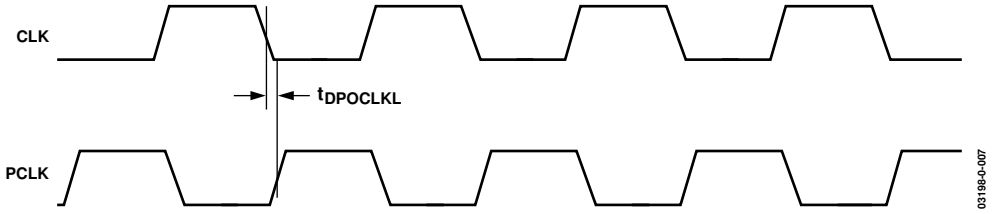

Figure 20. PCLK to CLK Switching Characteristics Divide-by-1

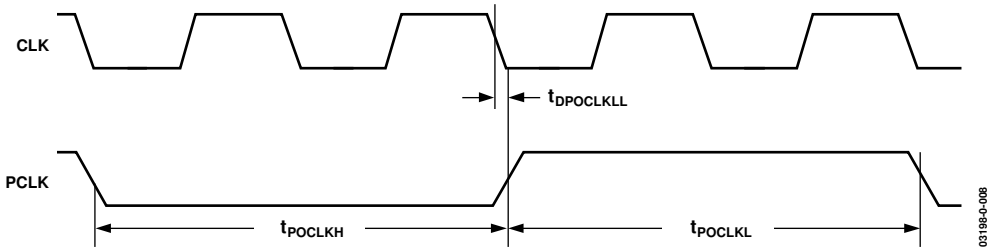

Figure 21. PCLK to CLK Switching Characteristics Divide-by-2, -4, or -8

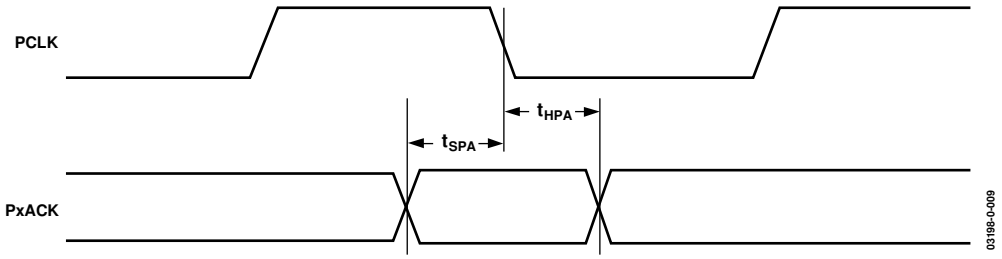

Figure 22. Master Mode PxACK to PCLK Setup and Hold Characteristics

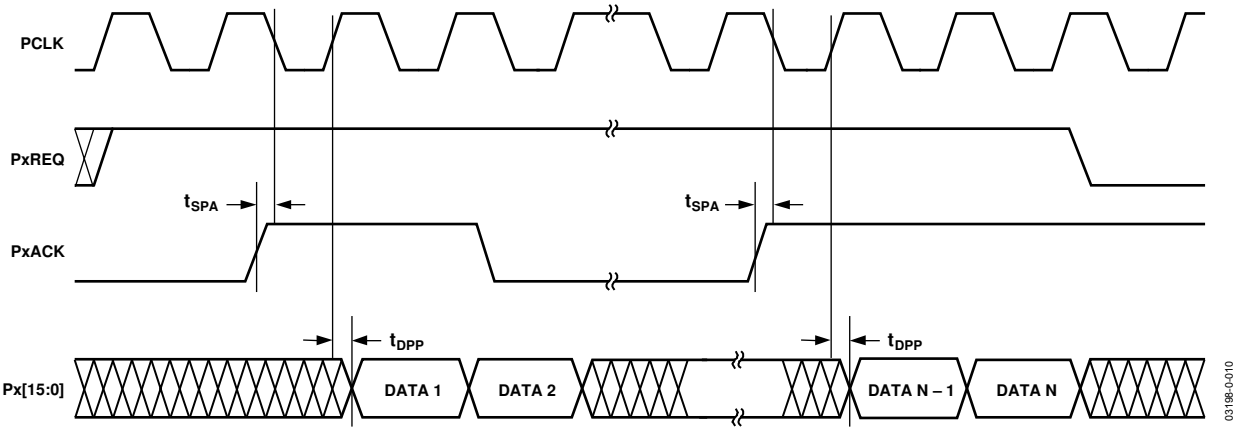

Figure 23. Master Mode PxACK to PCLK Switching Characteristics

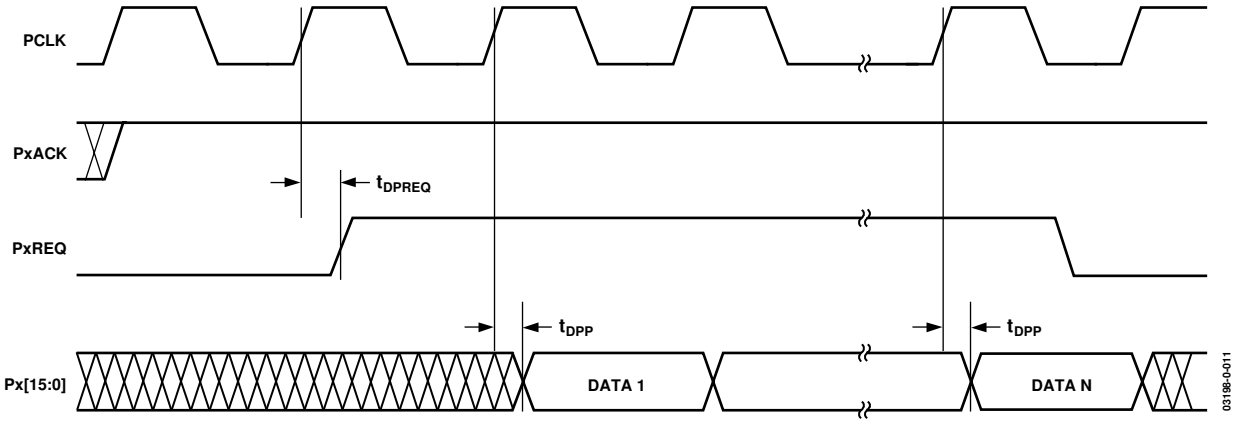

Figure 24. Master Mode PxREQ to PCLK Switching Characteristics

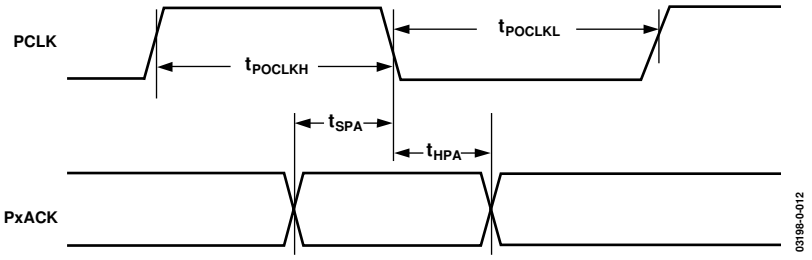

Figure 25. Slave Mode PxACK to PCLK Setup and Hold Characteristics

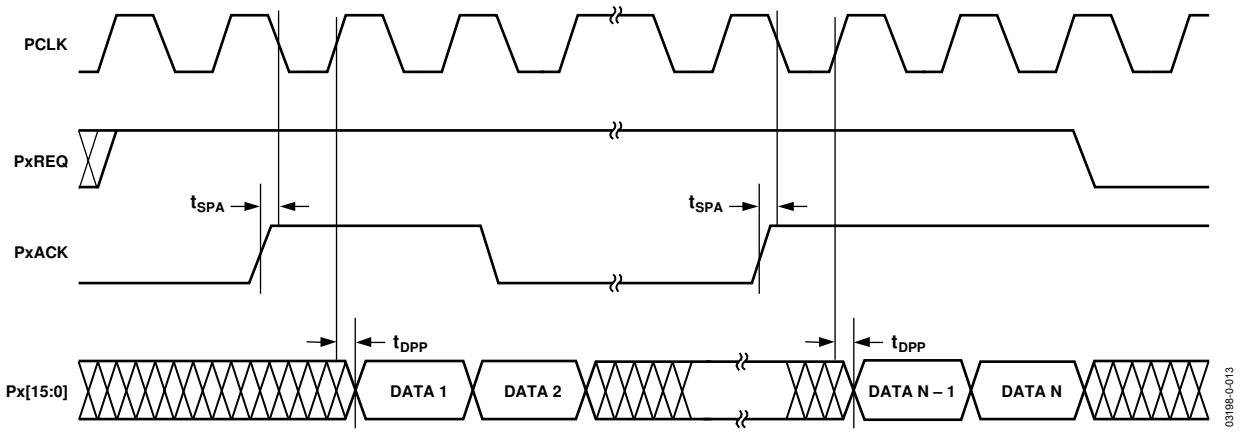

Figure 26. Slave Mode PxACK to PCLK Switching Characteristics

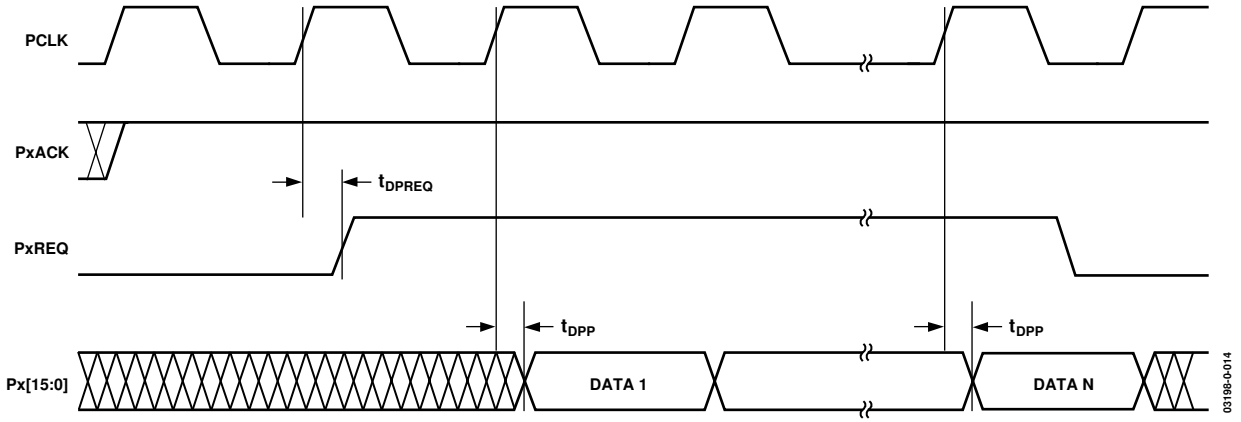

Figure 27. Slave Mode PxREQ to PCLK Switching Characteristics

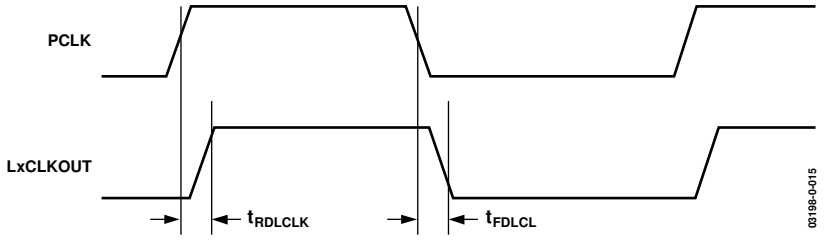

Figure 28. LxCLKOUT to PCLK Switching Characteristics

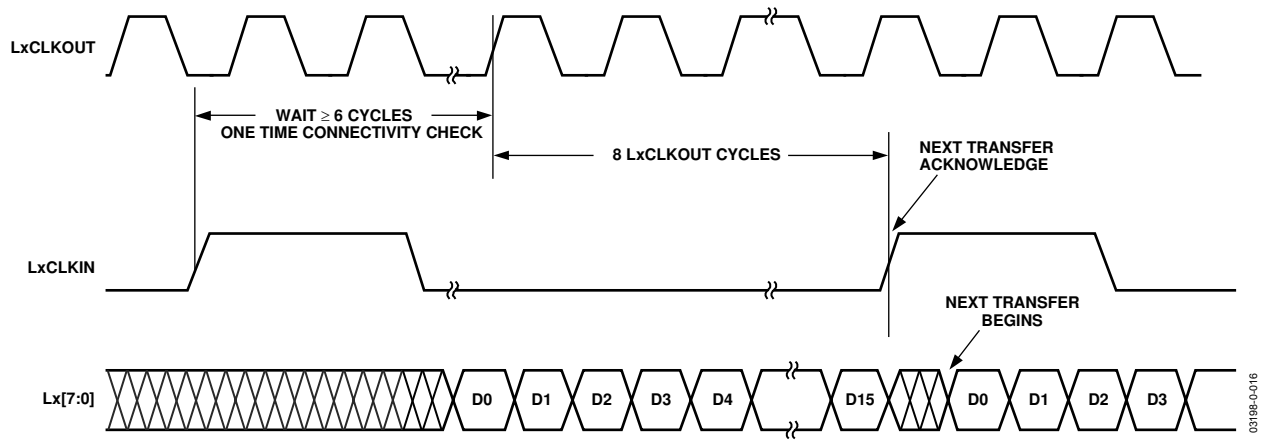

Figure 29. LxCLKIN to LxCLKOUT Data Switching Characteristics

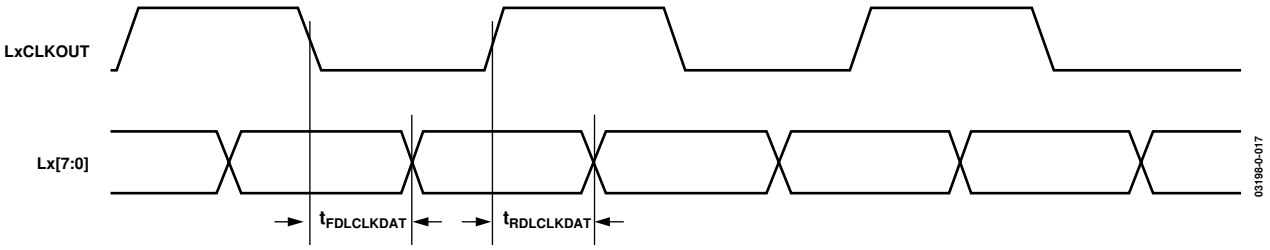

Figure 30. LxCLKOUT to Lx[7:0] Data Switching Characteristics

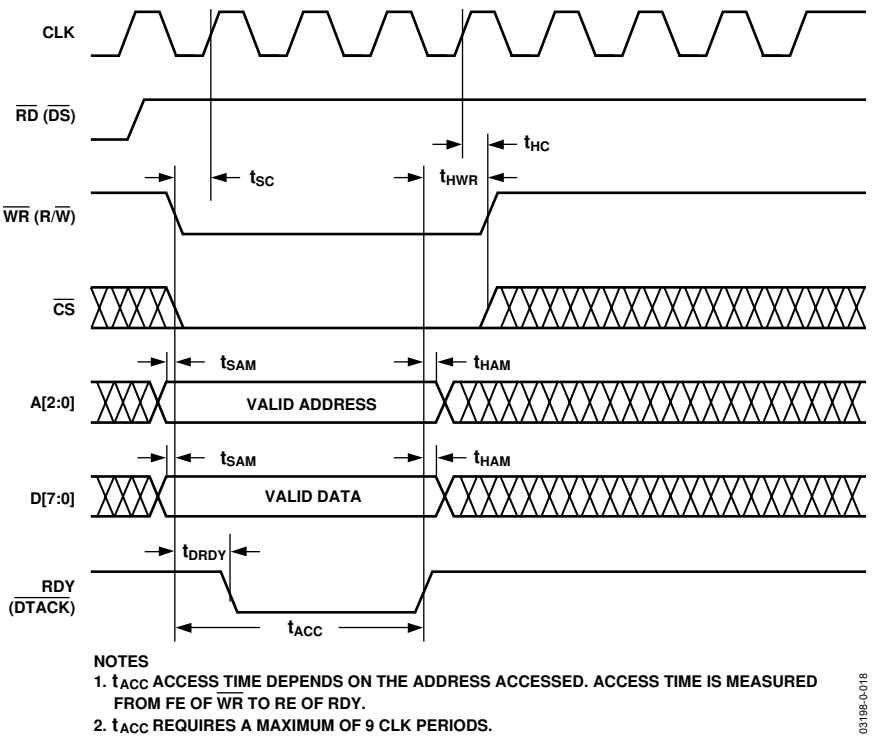

Figure 31. INM Microport Write Timing Requirements

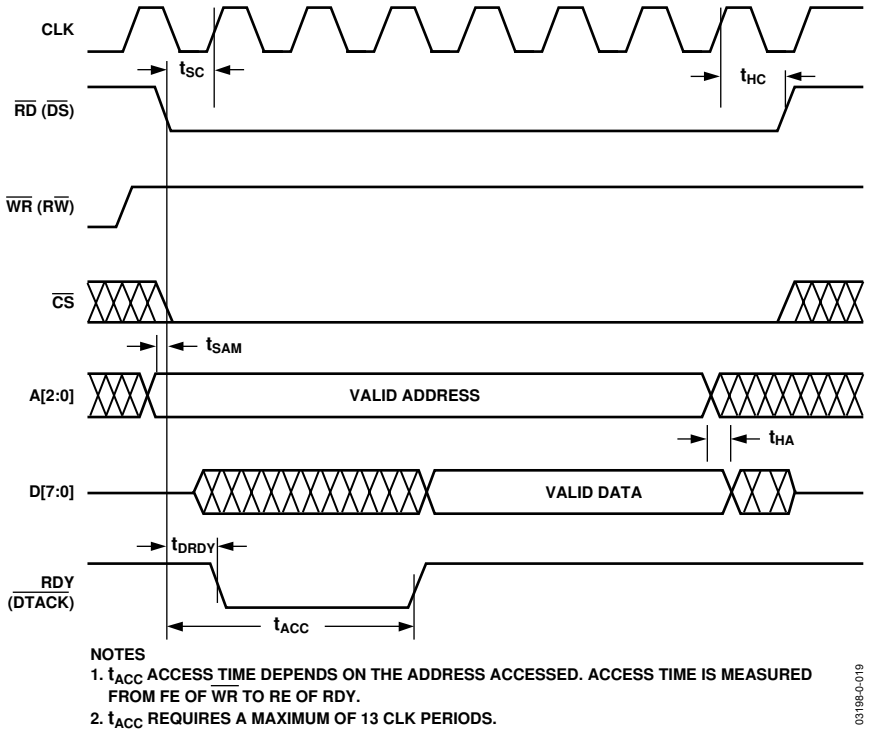

Figure 32. INM Microport Read Timing Requirements

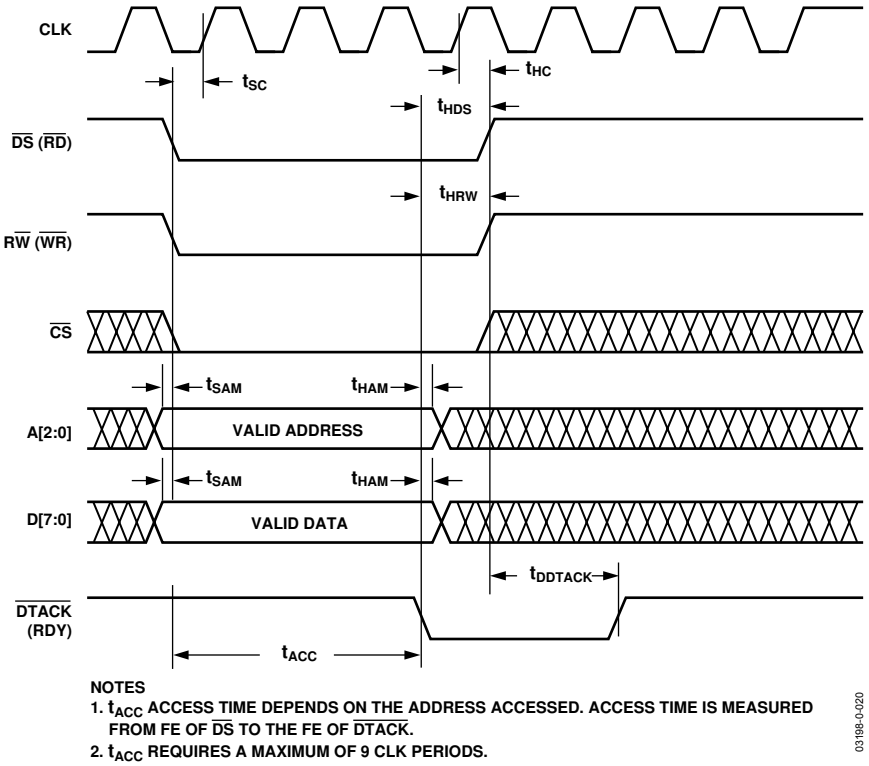

Figure 33. MNM Microport Write Timing Requirements

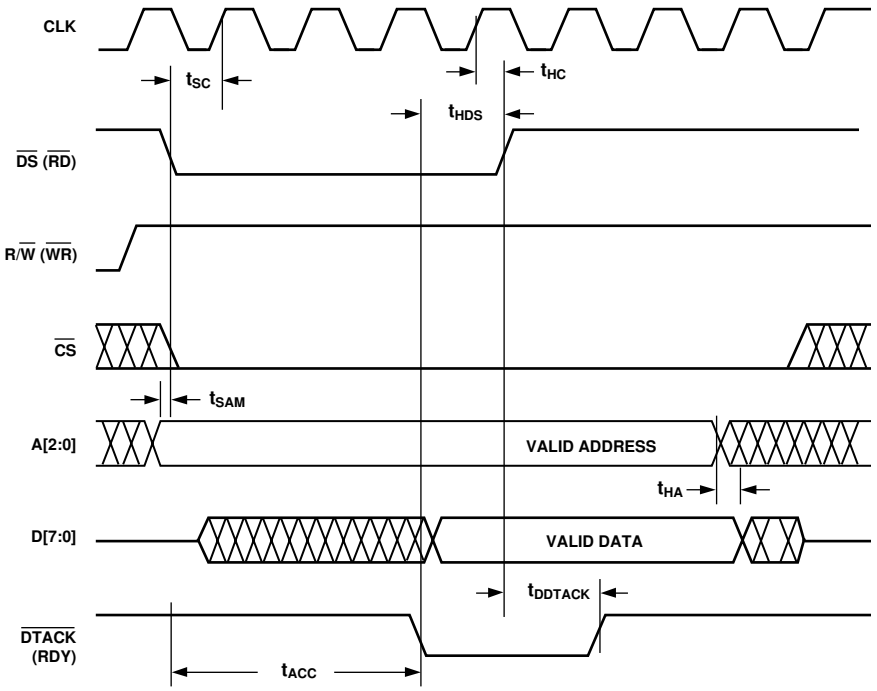

Figure 34. MNM Microport Read Timing Requirements

TERMINOLOGY

Crosstalk
Coupling onto one channel being driven by a (−0.5 dBFS) signal when the adjacent interfering channel is driven by a full-scale signal. Measurement includes all spurs resulting from both direct coupling and mixing components.

IF Sampling (Undersampling)
Due to the effects of aliasing, an ADC is not necessarily limited to Nyquist sampling. Frequencies above Nyquist are aliased and appear in the first Nyquist zone (dc to Sample Rate/2). Care must be taken to limit the bandwidth of the sampled signal so that it does not overlap Nyquist zones and alias onto itself. IF sampling performance is limited by the bandwidth of the input SHA (sample-and-hold amplifier) and clock jitter. (Jitter adds more noise at higher input frequencies.)

Nyquist Sampling (Oversampling)
Oversampling occurs when the frequency components of the analog input signal are below the Nyquist frequency ($F_{clock}/2$), and requires that the analog input frequency be sampled at least two samples per cycle.

Out-of-Range Recovery Time
Out-of-range recovery time is the time it takes for the analog-to-digital converter (ADC) to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

Processing Gain
When the tuned channel occupies less bandwidth than the input signal, this rejection of out-of-band noise is referred to as *processing gain*. By using large decimation factors, this processing gain can improve the SNR of the ADC by 20 dB or more. The following equation can be used to estimate processing gain:

$$Processing\_Gain = 10 \log \left[\frac{Sample\_Rate/2}{Filter\_Bandwidth} \right]$$

Signal-to-Noise Ratio (SNR)
The ratio of the rms value of the measured input signal to the rms sum of all other spectral components within the programmed DDC filter bandwidth, excluding the first six harmonics and dc. The value for SNR is expressed in decibels (dB).

Two-Tone IMD Rejection
The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product; reported in dBc.

ADC EQUIVALENT CIRCUITS

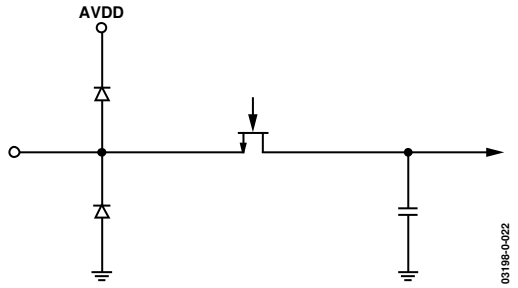

Figure 35. Analog Input Circuit

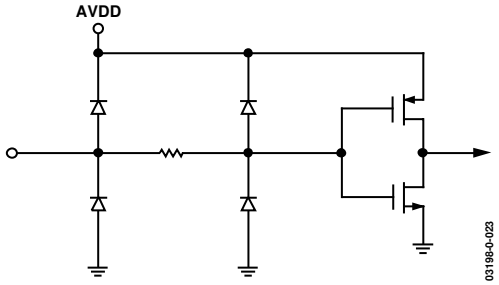

Figure 36. Digital Input

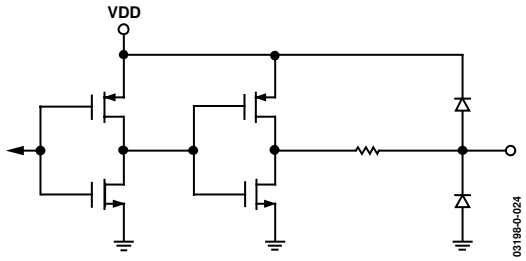

Figure 37. Digital Output

THEORY OF OPERATION

The AD6652 has two analog input channels, four digital filtering channels, and two digital output channels. The IF input signal passes through several stages before it appears at the output port(s) as a well-filtered, decimated digital baseband signal:

- 12-bit A/D conversion
- Frequency translation from IF to baseband using quadrature mixers and NCOs
- Second-order resampling decimating CIC FIR filter (rCIC2)
- Fifth-order decimating CIC FIR filter (CIC5)
- RAM coefficient decimating FIR filter (RCF)
- Automatic gain control (AGC)
- 2× interpolation and channel interleave

Any stage can be bypassed with the exception of the ADC front end. Any combination of processing channels can be combined or interleaved after the RCF stages to achieve demanding filtering objectives that are not possible with just one channel. In the following sections, each stage is examined to allow the user to fully utilize the AD6652's capabilities.

The dual ADC design is useful for diversity reception of signals, where the ADCs are operating identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample any fs/2 frequency segment from dc to 100 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. Operation to 200 MHz analog input is permitted, but at the expense of increased ADC distortion.

In nondiversity applications, up to four GSM/EDGE-type carriers can be concurrently processed from the ADC stage. Wideband signals, such as WCDMA/CDMA2000, require the power of two AD6652 processing channels per carrier to adequately remove adjacent channel interference. When diversity techniques are employed, the number of carriers that can be processed is halved due to the dual processing requirement of diversity reception.

Flexible channel multiplexing in the digital downconverter (DDC) stage allows one to four channels to be interleaved onto one output port. Four synchronization input pins allow startup, frequency hop, and AGC functions to be precisely orchestrated with other devices. The NCO's phase can be set to produce a known offset relative to another channel or device.

Programming and control of the AD6652 is accomplished using an 8-bit parallel interface.

ADC ARCHITECTURE

The AD6652 front-end consists of two high performance, 12-bit ADCs, preceded by differential sample-and-hold amplifiers (SHA) that provide excellent SNR performance from dc to 200 MHz. A flexible, integrated voltage reference allows analog inputs up to 2 V p-p. Each channel is equipped with an overrange pin that toggles high whenever the analog input exceeds the upper or lower reference voltage boundary. ADC outputs are internally routed to the input matrix of the DDC stage for channel distribution. The ADC data outputs are not directly accessible to the user.

Each sample-and-hold amplifier (SHA) is followed by a pipelined switched capacitor ADC. The pipelined ADC is divided into three sections, consisting of a 4-bit first stage followed by eight 1.5-bit stages and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample while the remaining stages operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Analog Input Operation

The analog inputs to the AD6652 are differential switched capacitor SHAs that have been designed for optimum performance while processing differential input signals. The AD6652 accepts inputs over a wide common-mode range; however, an input common-mode voltage V_{CM}, one-half of AVDD, is recommended to maintain optimal performance and to minimize signal-dependent errors.

Referring to Figure 38, the clock signal alternatively switches the SHA between sample mode and hold mode. When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. Also, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC's input; therefore, the precise values are dependent upon the application. In IF undersampling applications, any shunt capacitors should be removed. In combination with the driving source impedance, the shunt capacitors would limit the input bandwidth.