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14-Bit, 92.16 MSPS, 4-/6-Channel Wideband IF to Baseband Receiver

AD6654

FEATURES

- SNR = 90 dB in 1.25 MHz bandwidth to Nyquist
- SNR = 87 dB in 1.25 MHz bandwidth to 200 MHz
- Integrated 14-bit, 92.16 MSPS ADC
- IF sampling frequencies to 200 MHz
- Internal 2.4 V reference, 2.2 V p-p analog input range
- Internal differential track-and-hold analog input
- Processes 4/6 wideband carriers simultaneously
- Fractional clock multiplier to 200 MHz
- Programmable decimating FIR filters, interpolating half-band filters and programmable AGC loops with 96 dB range
- Three 16-bit configurable parallel output ports
- User-configurable built-in self-test (BIST) capability
- 8-/16-bit microport and SPORT/SPI® serial port control

APPLICATIONS

- Multicarrier, multimode digital receivers
- GSM, EDGE, PHS, UMTS, WCDMA, CDMA2000, TD-SCDMA, WiMAX
- Micro and pico cell systems, software radios
- Wireless local loop
- Smart antenna systems
- In-building wireless telephony
- Broadband data applications
- Instrumentation and test equipment

FUNCTIONAL BLOCK DIAGRAM

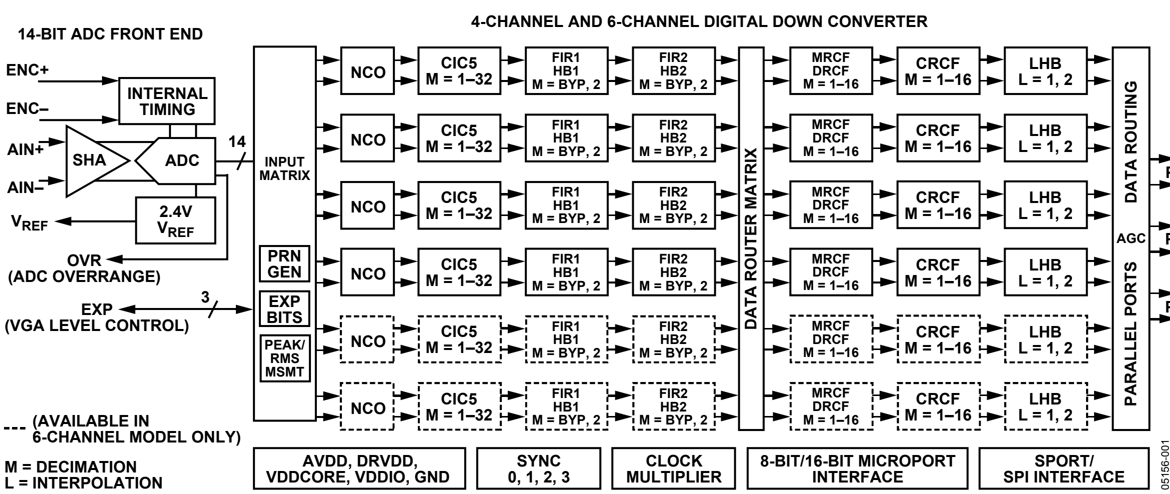

Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

AD6654* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD6654 Evaluation Board

DOCUMENTATION

Application Notes

- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design

Data Sheet

- AD6654: 14-Bit, 92.16 MSPS, 4-/6-Channel Wideband IF to Baseband Receiver Data Sheet

TOOLS AND SIMULATIONS

- AD6654 IBIS Model

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC
- Software-Defined Radio Comes of Age

DESIGN RESOURCES

- AD6654 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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REVISION HISTORY

4/05—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD6654 is a mixed-signal IF-to-baseband receiver consisting of a 14-bit, 92.16 MSPS analog-to-digital converter (ADC) and a 4-/6-channel, multimode digital down-converter (DDC) capable of processing up to six WCDMA (wideband code division multiple access) channels. The AD6654 has been optimized for the demanding filtering requirements of wide-band standards such as CDMA2000, UMTS, and TD-SCDMA, but is flexible enough to support wider standards such as WiMAX. It is typically used as part of a radio system that digitally demodulates and filters IF sampled signals.

The ADC stage features a high performance track-and-hold input amplifier (T/H), integrated voltage reference, and 14-bit sampling resolution. Input signals up to 200 MHz can be accurately digitized at encode rates up to 92.16 MSPS. The ADC data outputs are internally routed directly into the DDC inputs, where down-conversion, decimation and digital filtering are performed. An overrange (OVR) output bit provides indication of excessive ADC input levels. An ADC data-ready (DR) output bit provides a synchronized clock for the integrated DDC.

Data from the ADC is evaluated for peak or mean power in the input stage of the DDC, and the result is available to the user via control register access. The DDC input stage also outputs 3-bit level-indicator data (EXP) bits that can be used to control the gain of the external DVGA in 6 dB steps (up to 48 dB) to optimize signal amplitude into the ADC input.

The DDC stage has the following signal processing stages: six WCDMA-ready channels, each consisting of a frequency translator, a fifth-order cascaded integrated comb filter, two sets of cascaded fixed coefficient FIR and half-band filters, three cascaded programmable sum of product FIR filters, an interpolating half-band filter (IHB), and a digital automatic gain control (AGC) block. Multiple modes are supported for clocking data out of the chip. Programming is accomplished via serial or microport interfaces.

Frequency translation is accomplished with a 32-bit complex numerically controlled oscillator (NCO). The NCO has greater than 110 dBc SDFR. This stage translates a real input signal from an intermediate frequency (IF) to a baseband complex digital output. Phase and amplitude dither can be enabled on-chip to improve spurious performance of the NCO. A 16-bit phase-offset word is available to create a known phase relationship between multiple AD6654 chips or channels. The NCO can also be bypassed.

Following frequency translation is a fifth-order CIC filter with a programmable decimation between 1 and 32. This filter is used to efficiently lower the sample rate, while providing sufficient alias rejection at frequencies at higher offsets from the signal of interest.

Following the CIC5 are two sets of filters. Each filter set includes a nondecimating FIR filter and a decimate-by-2 half-band filter. The FIR1 filter provides about 30 dB of rejection, while the HB1 provides about 77 dB of rejection. These two sets of filters can be used together to achieve a 107 dB stop-band alias rejection, or they can be individually bypassed to save power.

The FIR2 filter provides about 30 dB of rejection, while the HB2 filter provides about 65 dB of rejection. The filters can be used together to achieve more than 95 dB stop-band alias rejection, or they can be individually bypassed to save power. FIR1 and HB1 filters can run at the maximum ADC data port rate. In contrast, FIR2 and HB2 can run with a maximum input rate of 75 MSPS (input rate to FIR2 and HB2 filters).

The programmable filtering is divided into three cascaded RAM coefficient filters (RCFs) for flexible and power-efficient filtering. The first filter in the cascade is the MRCF, consisting of a programmable nondecimating FIR. It is followed by programmable FIR filters (DRCF) with decimation from 1 to 16. They can be used either together to provide high rejection filters, or independently to save power. The maximum input rate to the MRCF is one-fourth the PLL clock rate.

The CRCF (Channel RCF) is the last programmable FIR filter with programmable decimation from 1 to 16. It is typically used to meet the spectral mask requirements for the air standard of interest. This could be an RRC, antialiasing filter or any other real data filter. Decimation in preceding blocks is used to keep the input rate of this stage as low as possible for the best filter performance.

The last filter stage in the chain is an interpolate-by-2 half-band filter, which is used to up-sample the CRCF output to produce higher output oversampling. Signal rejection requirements for this stage are relaxed, because preceding filters have already filtered the blockers and adjacent carriers.

The DDC input port of the AD6654 has its own clock input used for latching the input data, as well as for providing the input for an onboard PLL clock multiplier. The output of the PLL clock is used for processing all filters and processing blocks beyond the data router following CIC filter. The PLL clock can be programmed to have a maximum clock rate of 200 MHz. Typically, the DDC input clock is driven directly from the integrated ADC's data-ready (DR) output to ensure proper synchronization.

A data routing block is used to distribute data from the CICs to the various channel filters. This block allows multiple back-end filter chains to work together to process high bandwidth signals or to make even sharper filter transitions than a single channel can perform. It can also allow complex filtering operations to be achieved in the programmable filters.

The digital AGC provides the user with scaled digital outputs based on the rms level of the signal present at the output of the digital filters. The user can set the requested level and time constant of the AGC loop for optimum performance of the postprocessor. This is a critical function in the base station for CDMA application, where the power level must be well controlled going into the RAKE receivers. It has programmable clipping and rounding control to provide different output resolutions.

The overall filter response for the AD6654 is the composite of all the combined filter stages. Each successive filter stage is capable of narrower transition bandwidths, but requires a greater number of CLK cycles to calculate the output. The AD6654 features a fractional clock multiplier that uses the ADC clock (which is slower than the DDC's processing speed) to produce a DDC master clock up to 200 MHz. This feature allows fractional multiplication of the input clock to allow the DDC to function at maximum speed while maintaining edge identity to the ADC clock.

More decimation in the first filter stage minimizes overall power consumption. Data from the device is interfaced to a DSP/FPGA/baseband processor via high speed parallel ports (preferred), or a DSP-compatible microprocessor interface.

The AD6654 is available in 4-channel and 6-channel versions. The primary focus of the data sheet is on the 6-channel part. The only difference between the 6-channel and 4-channel devices is that, on the 4-channel version, Channel 4 and Channel 5 are not available (see Figure 1). The 4-channel device has the same DDC input port features, output ports, and memory map as the 6-channel device. On the 4-channel version, the memory map section for Channel 4 and Channel 5 can be programmed and read back, but the two extra channels are disabled internally.

PRODUCT HIGHLIGHTS

1. Integrated 14-bit, 92.16 MSPS ADC.
2. Track-and-hold amplifier analog input for excellent IF sampling up to 200 MHz.
3. Four or six independent digital filtering channels.
4. RMS/peak power monitoring of the ADC data port and 96 dB range AGCs before the output ports.
5. Three programmable RAM coefficient filters, three half-band filters, two fixed coefficient filters, and one fifth-order CIC filter per channel.
6. Complex filtering by combining filtering capability of multiple channels.
7. Three 16-bit parallel output ports operating at up to 200 MHz clock.
8. Blackfin®- and TigerSHARC®-compatible, 8-/16-bit microprocessor port.
9. Synchronous serial communications port is compatible with most serial interface standards: SPORT, SPI, and SSR.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Table 1.

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
AVDD[1]	Full	IV	4.75	5.0	5.25	V
DRVDD[2]	Full	IV	3.0	3.3	3.6	V
VDDCORE	Full	IV	1.65	1.8	1.95	V
VDDIO[2]	Full	IV	3.0	3.3	3.6	V
$T_{AMBIENT}$		IV	−25	+25	+85	°C

[1] Specified for dc supplies with linear rise-time <250 ms.

[2] DRVDD and VDDIO can be operated from the same supply.

ADC DC SPECIFICATIONS

AVDD = 5.0 V, DRVDD = 3.3 V, VDDCORE = 1.8 V, VDDIO = 3.3 V, maximum rated sample rate, differential ENC and AIN, unless otherwise noted.

Table 2.

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
RESOLUTION	Full	IV		14		Bits
INTERNAL VOLTAGE REFERENCE (V_{REF})[1]						
Output Voltage	Full	IV		2.4		V
ANALOG INPUTS						
Differential Input Voltage Range	Full	IV		2.2		V p-p
Differential Input Capacitance	Full	V		1.5		pF
Differential Input Resistance	Full	V		1		kΩ
Power Supply Rejection (PSRR)	25°C	V		±1.0		mV/V

[1] V_{REF} is provided for setting the common-mode offset of a differential amplifier such as the AD8138 when a dc-coupled analog input is required. V_{REF} should be buffered if used to drive additional circuit functions.

ADC DIGITAL SPECIFICATIONS

AVDD = 5.0 V, DRVDD = 3.3 V, VDDCORE = 1.8 V, VDDIO = 3.3 V, maximum rated sample rate, differential ADC input, unless otherwise noted.

Table 3.

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
ENCODE INPUTS (ENC+, ENC−)						
Differential Input Voltage	Full	IV	0.4			V p-p
Differential Input Resistance	25°C	V		10		kΩ
Differential Input Capacitance	25°C	V		2.5		pF

ADC SWITCHING SPECIFICATIONS

AVDD = 5.0 V, DRVDD = 3.3 V, VDDCORE = 1.8 V, VDDIO = 3.3 V, maximum rated sample rate, differential input, unless otherwise noted.

Table 4.

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
SWITCHING PERFORMANCE						
Maximum Conversion Rate	Full	II	92.16			MSPS
Minimum Conversion Rate	Full	IV			30	MSPS
ENC Pulse Width High[1] (t_{ENCH})	Full	IV	5.154	5.425		ns
ENC Pulse Width Low[1] (t_{ENCL})	Full	IV	5.154	5.425		ns

[1] Several internal timing parameters are a function of t_{ENCL} and t_{ENCH}, optimum performance will be achieved with 50/50 duty cycle.

ADC AC SPECIFICATIONS

AVDD = 5.0 V, DRVDD = 3.3 V, VDDCORE = 1.8 V, VDDIO = 3.3 V, maximum rated sample rate, differential input, unless otherwise noted.

Table 5.

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO[1] (WITHOUT HARMONICS)						
Analog Input Frequency 37 MHz						
ADC (46.08 MHz BW)	25°C	V		74.5		dB
CDMA (1.25 MHz BW)	Full	II	88	90.0		dB
WCDMA (5.0 MHz BW)	25°C	V		84		dB
Analog Input Frequency 70 MHz						
ADC (46.08 MHz BW)	25°C	V		73.5		dB
CDMA (1.25 MHz BW)	Full	II	87.5	89		dB
WCDMA (5.0 MHz BW)	25°C	V		83		dB
Analog Input Frequency 150 MHz						
ADC (46.08 MHz BW)	25°C	V		73		dB
CDMA (1.25 MHz BW)	25°C	V		88		dB
WCDMA (5.0 MHz BW)	25°C	V		82		dB
Analog Input Frequency 200 MHz						
ADC (46.08 MHz BW)	25°C	V		72		dB
CDMA (1.25 MHz BW)	25°C	V		87		dB
WCDMA (5.0 MHz BW)	25°C	V		81		dB
WORST HARMONIC[2] (ANALOG INPUT @ −1 dBFS)						
37 MHz	Full	II	85	93		dBc
70 MHz	Full	V		91		dBc
150 MHz	Full	V		71		dBc
200 MHz	Full	V		63		dBc
INTERMODULATION DISTORTION (TWO-TONES SEPARATED BY 1 MHz)[3]						
Analog Input = 55/56 MHz	25°C	V		90		dBc
ANALOG INPUT BANDWIDTH	25°C	V		270		MHz

[1] Analog input = −1 dB below full scale.
[2] Includes Harmonic 2 through Harmonic 6.
[3] Analog input = each −7 dB below full scale.

ELECTRICAL CHARACTERISTICS

AVDD = 5.0 V, DRVDD = 3.3 V, VDDCORE = 1.8 V, VDDIO = 3.3 V, maximum rated sample rate, differential input, unless otherwise noted.

Table 6.

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
LOGIC INPUTS (NOT 5 V TOLERANT)						
Logic Compatibility	Full	IV		3.3 V CMOS		
Logic 1 Voltage	Full	IV	2.0		3.6	V
Logic 0 Voltage	Full	IV	−0.3		+0.8	V
Logic 1 Current	Full	IV		1	10	μA
Logic 0 Current	Full	IV		1	10	μA
Logic 1 Current (Inputs With Pull-Down)	Full	IV				
Logic 0 Current (Inputs With Pull-Up)	Full	IV				
Input Capacitance	25°C	V		4		pF
LOGIC OUTPUTS						
Logic Compatibility	Full	IV		3.3 V CMOS		
Logic 1 Voltage (I_{OH} = 0.25 mA)	Full	IV	2.4	VDDIO − 0.2		V
Logic 0 Voltage (I_{OL} = 0.25 mA)	Full	IV		0.2	0.4	V
SUPPLY CURRENTS						
WCDMA (92.16 MSPS) EXAMPLE[1]						
I_{AVDD}	25°C	V		275		mA
I_{DRVDD}	25°C	V		32		mA
I_{VDD}	25°C	V		460		mA
I_{VDDIO}	25°C	V		60		mA
CDMA2000 (92.16 MSPS) EXAMPLE[1]						
I_{AVDD}	25°C	V		275		mA
I_{DRVDD}	25°C	V		32		mA
I_{VDD}	25°C	V		435		mA
I_{VDDIO}	25°C	V		25		mA
TDS-CDMA (76.8 MSPS) EXAMPLE[1, 2]						
I_{AVDD}	25°C	V		275		mA
I_{DRVDD}	25°C	V		32		mA
I_{VDD}	25°C	V		250		mA
I_{VDDIO}	25°C	V		15		mA
TOTAL POWER DISSIPATION						
WCDMA (92.16 MSPS)[1]	25°C	V		2.5		W
CDMA2000 (92.16 MSPS)[1]	25°C	V		2.3		W
TDS-CDMA (76.8 MSPS)[1, 2]	25°C	V		2.0		W

[1] ADC input port, all six DDC channels, and the relevant signal processing blocks are active.
[2] PLL is turned off for power savings.

TIMING CHARACTERISTICS

Table 7.

Parameter[1, 2, 3]		Temp	Test Level	Min	Typ	Max	Unit
CLK TIMING REQUIREMENTS							
t_{CLK}	CLK Period	Full	IV		10.85		ns
t_{CLKL}	CLK Width Low	Full	IV	5.154	0.5 × t_{CLK}		ns
t_{CLKH}	CLK Width High	Full	IV	5.154	0.5 × t_{CLK}		ns
INPUT WIDEBAND DATA TIMING REQUIREMENTS							
t_{DEXP}	↑CLK to EXP[2:0] Delay	Full	IV	5.98		10.74	ns
PARALLEL OUTPUT PORT TIMING REQUIREMENTS (MASTER)							
t_{DPREQ}	↑PCLK to ↑Px REQ Delay (x = A, B, C)	Full	IV	1.77		3.86	ns
t_{DPP}	↑PCLK to Px[15:0] Delay (x = A, B, C)	Full	IV	2.07		5.29	ns
t_{DPIQ}	↑PCLK to Px IQ Delay (x = A, B, C)	Full	IV	0.48		5.49	ns
t_{DPCH}	↑PCLK to Px CH[2:0] Delay (x = A, B, C)	Full	IV	0.38		5.35	ns
t_{DPGAIN}	↑PCLK to Px Gain Delay (x = A, B, C)	Full	IV	0.23		4.95	ns
t_{SPA}	Px ACK to ↑PCLK Setup Time (x = A, B, C)	Full	IV	4.59			ns
t_{HPA}	Px ACK to ↑PCLK Hold Time (x = A, B, C)	Full	IV	0.90			ns
PARALLEL OUTPUT PORT TIMING REQUIREMENTS (SLAVE)							
t_{PCLK}	PCLK Period	Full	IV	5.0			ns
t_{PCLKL}	PCLK Low Period	Full	IV	1.7	0.5 × t_{PCLK}		ns
t_{PCLKH}	PCLK High Period	Full	IV	0.7	0.5 × t_{PCLK}		ns
t_{DPREQ}	↑PCLK to ↑Px REQ Delay (x = A, B, C)	Full	IV	4.72		8.87	ns
t_{DPP}	↑PCLK to Px[15:0] Delay (x = A, B, C)	Full	IV	4.8		8.48	ns
t_{DPIQ}	↑PCLK to Px IQ Delay (x = A, B, C)	Full	IV	4.83		10.94	ns
t_{DPCH}	↑PCLK to Px CH[2:0] Delay (x = A, B, C)	Full	IV	4.88		10.09	ns
t_{DPGAIN}	↑PCLK to Px Gain Delay (x = A, B, C)	Full	IV	5.08		11.49	ns
t_{SPA}	Px ACK to ↓PCLK Setup Time (x = A, B, C)	Full	IV	6.09			ns
t_{HPA}	Px ACK to ↓PCLK Hold Time (x = A, B, C)	Full	IV	1.0			ns
MISC PINS TIMING REQUIREMENTS							
t_{RESET}	$\overline{RESET}$ Width Low	Full	IV	30			ns
t_{DIRP}	CPUCLK/SCLK to $\overline{IRP}$ Delay	Full	V	7.5			ns
t_{SSYNC}	SYNC(0, 1, 2, 3) to ↑CLK Setup Time	Full	IV	0.87			ns
t_{HSYNC}	SYNC(0, 1, 2, 3) to ↑CLK Hold Time	Full	IV	0.67			ns

[1] All timing specifications are valid over the VDDCORE range of 1.7 V to 1.9 V, and the VDDIO range of 3.0 V to 3.6 V.
[2] C_{LOAD} = 40 pF on all outputs, unless otherwise noted.
[3] These timing parameters are derived from the ADC ENC rate with DDC CLK driven directly from ADC DR output.

MICROPORT TIMING CHARACTERISTICS

Table 8.

Parameter[1, 2]		Temp	Test Level	Min	Typ	Max	Unit
MICROPORT CLOCK TIMING REQUIREMENTS							
t_{CPUCLK}	CPUCLK Period	Full	IV	10.0			ns
$t_{CPUCLKL}$	CPUCLK Low Time	Full	IV	1.53	$0.5 \times t_{CPUCLK}$		ns
$t_{CPUCLKH}$	CPUCLK High Time	Full	IV	1.70	$0.5 \times t_{CPUCLK}$		ns
INM MODE WRITE TIMING (MODE = 0)							
t_{SC}	Control[3] to ↑CPUCLK Setup Time	Full	IV	0.80			ns
t_{HC}	Control[3] to ↑CPUCLK Hold Time	Full	IV	0.09			ns
t_{SAM}	Address/Data to ↑CPUCLK Setup Time	Full	IV	0.76			ns
t_{HAM}	Address/Data to ↑CPUCLK Hold Time	Full	IV	0.20			ns
t_{DRDY}	↑CPUCLK to RDY ($\overline{DTACK}$) Delay	Full	IV	3.51		6.72	ns
t_{ACC}	Write Access Time	Full	IV	$3 \times t_{CPUCLK}$		$9 \times t_{CPUCLK}$	ns
INM MODE READ TIMING (MODE = 0)							
t_{SC}	Control[3] to ↑CPUCLK Setup Time	Full	IV		1.00		ns
t_{HC}	Control[3] to ↑CPUCLK Hold Time	Full	IV		0.03		ns
t_{SAM}	Address to ↑CPUCLK Setup Time	Full	IV		0.80		ns
t_{HAM}	Address to ↑CPUCLK Hold Time	Full	IV		0.20		ns
t_{DD}	↑CPUCLK to Data Delay	Full	V		5.0		ns
t_{DRDY}	↑CPUCLK to RDY ($\overline{DTACK}$) Delay	Full	IV	4.50		6.72	ns
t_{ACC}	Read Access Time	Full	IV	$3 \times t_{CPUCLK}$		$9 \times t_{CPUCLK}$	ns
MNM MODE WRITE TIMING (MODE = 1)							
t_{SC}	Control[3] to ↑CPUCLK Setup Time	Full	IV	1.00			ns
t_{HC}	Control[3] to ↑CPUCLK Hold Time	Full	IV	0.00			ns
t_{SAM}	Address/Data to ↑CPUCLK Setup Time	Full	IV	0.00			ns
t_{HAM}	Address/Data to ↑CPUCLK Hold Time	Full	IV	0.57			ns
t_{DDTACK}	↑CPUCLK to $\overline{DTACK}$ (RDY) Delay	Full	IV	4.10		5.72	ns
t_{ACC}	Write Access Time	Full	IV	$3 \times t_{CPUCLK}$		$9 \times t_{CPUCLK}$	ns
MNM MODE READ TIMING (MODE = 1)							
t_{SC}	Control[3] to ↑CPUCLK Setup Time	Full	IV	1.00			ns
t_{HC}	Control[3] to ↑CPUCLK Hold Time	Full	IV	0.00			ns
t_{SAM}	Address to ↑CPUCLK Setup Time	Full	IV	0.00			ns
t_{HAM}	Address to ↑CPUCLK Hold Time	Full	IV	0.57			ns
t_{DD}	CPUCLK to Data Delay	Full	V		5.0		ns
t_{DDTACK}	↑CPUCLK to $\overline{DTACK}$ (RDY) Delay	Full	IV	4.20		6.03	ns
t_{ACC}	Read Access Time	Full	IV	$3 \times t_{CPUCLK}$		$9 \times t_{CPUCLK}$	ns

[1] All timing specifications are valid over the VDDCORE range of 1.7 V to 1.9 V, and the VDDIO range of 3.0 V to 3.6 V.
[2] C_{LOAD} = 40 pF on all outputs, unless otherwise noted.
[3] Specification pertains to control signals: R/$\overline{W}$, ($\overline{WR}$), $\overline{DS}$, ($\overline{RD}$), and $\overline{CS}$.

SERIAL PORT TIMING CHARACTERISTICS

Table 9.

Parameter[1, 2, 3]		Temp	Test Level	Min	Typ	Max	Unit
SERIAL PORT CLOCK TIMING REQUIREMENTS							
t_{SCLK}	SCLK Period	Full	IV	10.0			ns
t_{SCLKL}	SCLK Low Time	Full	IV	1.60	0.5 × t_{SCLK}		ns
t_{SCLKH}	SCLK High Time	Full	IV	1.60	0.5 × t_{SCLK}		ns
SPI PORT CONTROL TIMING REQUIREMENTS (MODE = 0)							
t_{SSDI}	SDI to ↑SCLK Setup Time	Full	IV	1.30			ns
t_{HSDI}	SDI to ↑SCLK Hold Time	Full	IV	0.40			ns
t_{SSCS}	$\overline{SCS}$ to ↑SCLK Setup Time	Full	IV	4.12			ns
t_{HSCS}	$\overline{SCS}$ to ↑SCLK Hold Time	Full	IV	−2.78			ns
t_{DSDO}	↑SCLK to SDO Delay Time	Full	IV	4.28		7.96	ns
SPORT MODE CONTROL TIMING REQUIREMENTS (MODE = 1)							
t_{SSDI}	SDI to ↑SCLK Setup Time	Full	IV	0.80			ns
t_{HSDI}	SDI to ↑SCLK Hold Time	Full	IV	0.40			ns
t_{SSRFS}	SRFS to ↓SCLK Setup Time	Full	IV	1.60			ns
t_{HSRFS}	SRFS to ↓SCLK Hold Time	Full	IV	−0.13			ns
t_{SSTFS}	STFS to ↓SCLK Setup Time	Full	IV	1.60			ns
t_{HSTFS}	STFS to ↓SCLK Hold Time	Full	IV	−0.30			ns
t_{SSCS}	$\overline{SCS}$ to ↑SCLK Setup Time	Full	IV	4.12			ns
t_{HSCS}	$\overline{SCS}$ to ↑SCLK Hold Time	Full	IV	−2.76			ns
t_{DSDO}	↑SCLK to SDO Delay Time	Full	IV	4.29		7.95	ns

[1] All timing specifications are valid over the VDDCORE range of 1.7 V to 1.9 V and the VDDIO range of 3.0 V and 3.6 V.
[2] C_{LOAD} = 40 pF on all outputs, unless otherwise noted.
[3] SCLK rise/fall time should be 3 ns maximum.

TIMING DIAGRAMS

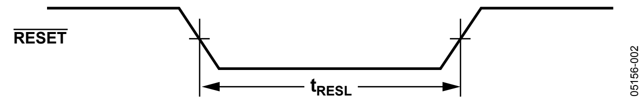


Figure 2. Reset Timing Requirements

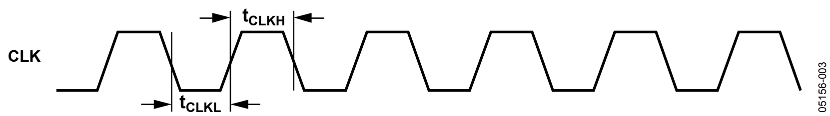


Figure 3. CLK Switching Characteristics

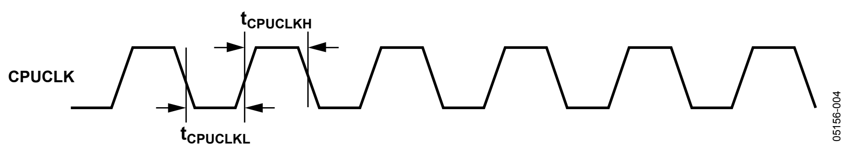


Figure 4. CPUCLK Switching Characteristics

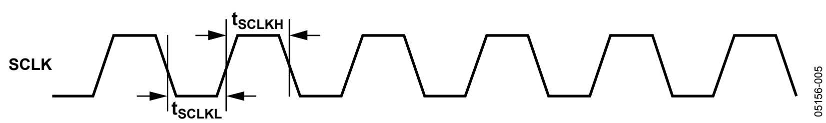


Figure 5. SCLK Switching Characteristics

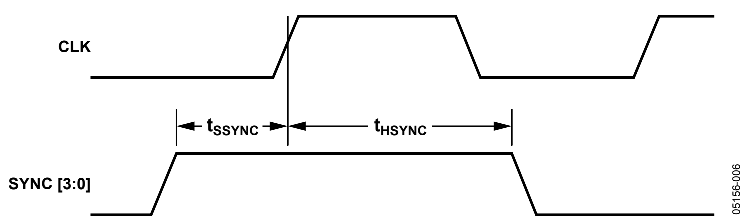


Figure 6. SYNC Timing Inputs

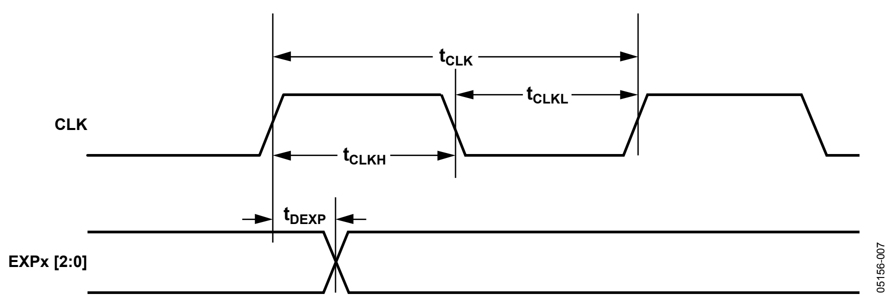


Figure 7. Gain Control Word Output Switching Characteristics

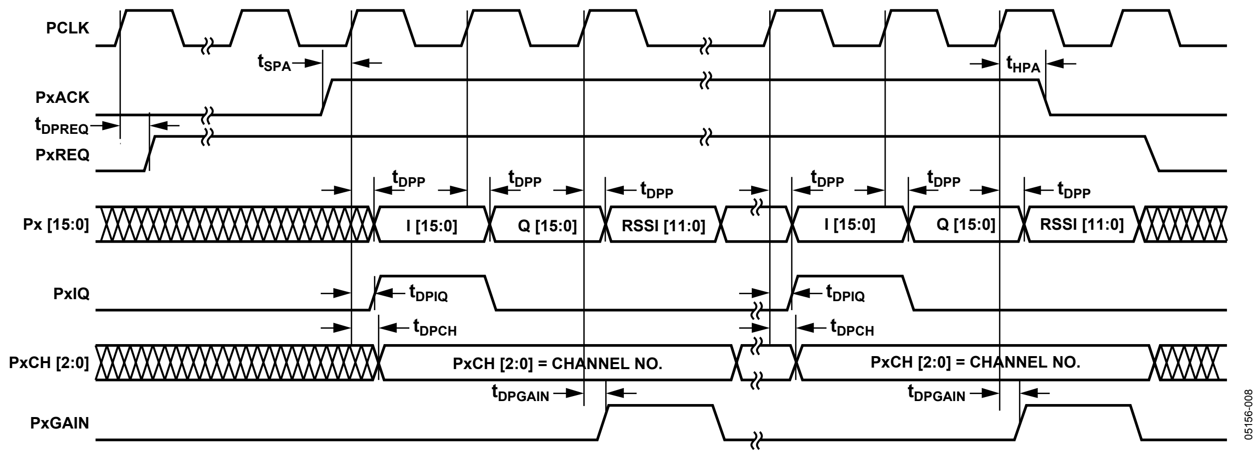


Figure 8. Master Mode PxACK to PCLK Switching Characteristics

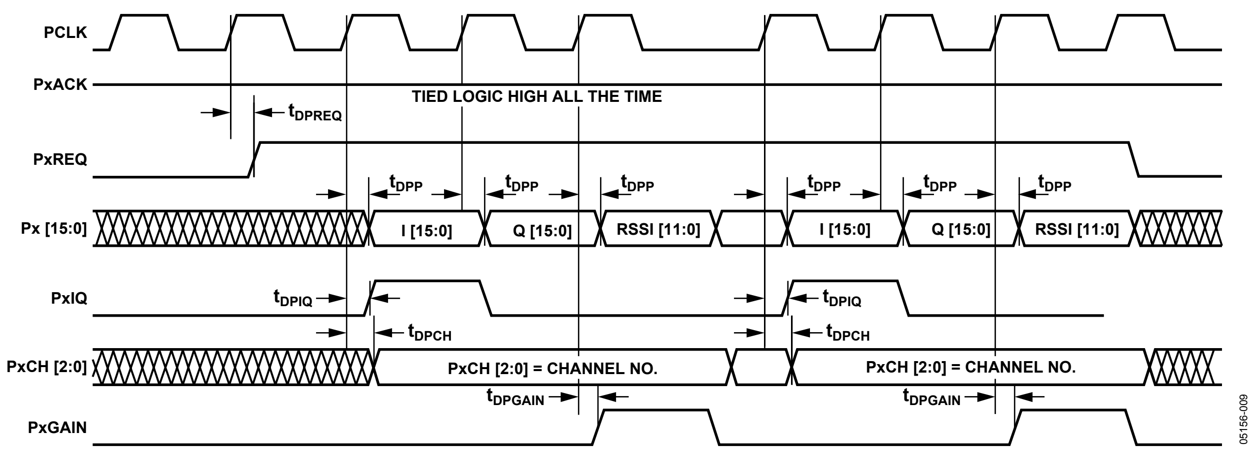
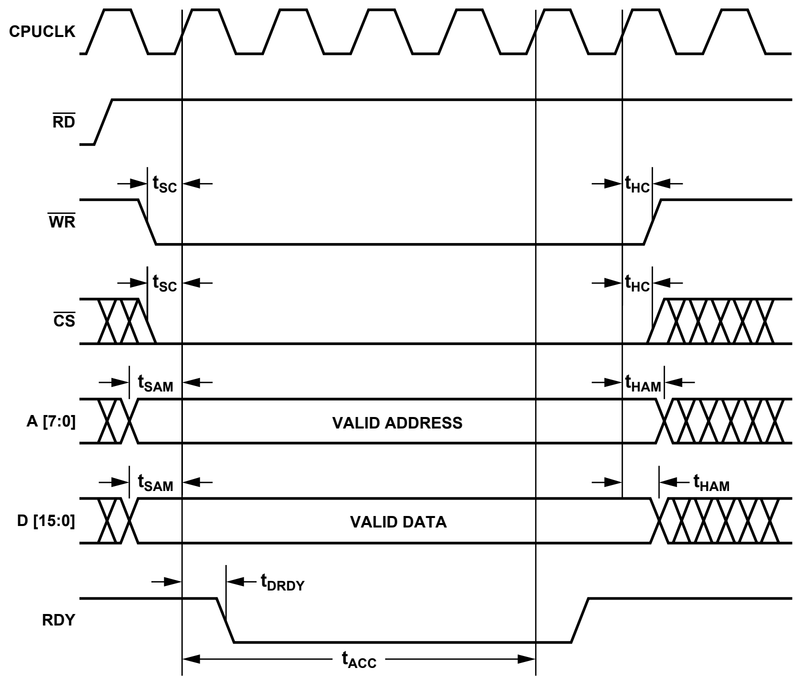


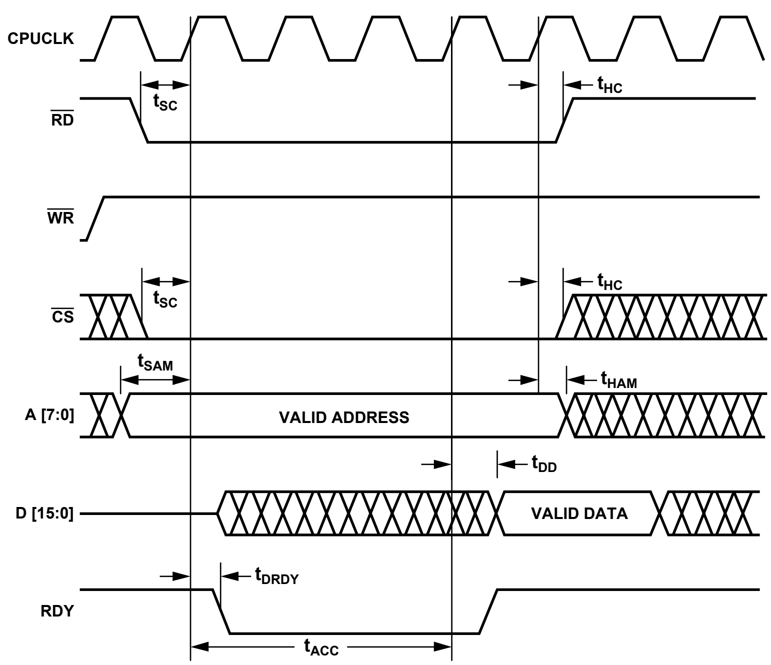
Figure 9. Master Mode PxREQ to PCLK Switching Characteristics



NOTE:
t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. IT CAN VARY FROM 3 TO 9 CPUCLK CYCLES.

05156-010

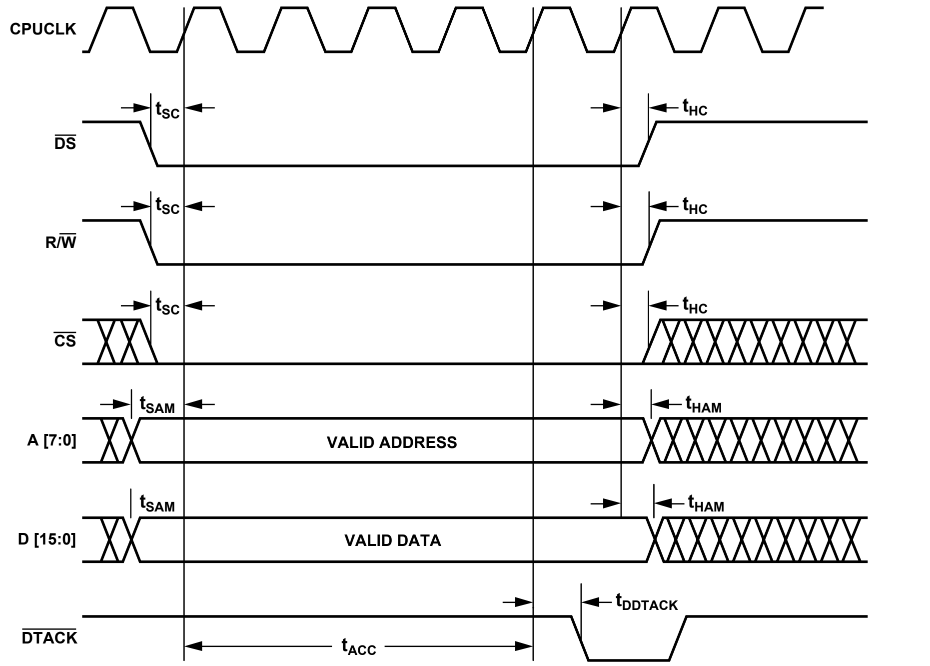
Figure 10. INM Microport Write Timing Requirements



NOTE:
t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. IT CAN VARY FROM 3 TO 9 CPUCLK CYCLES.

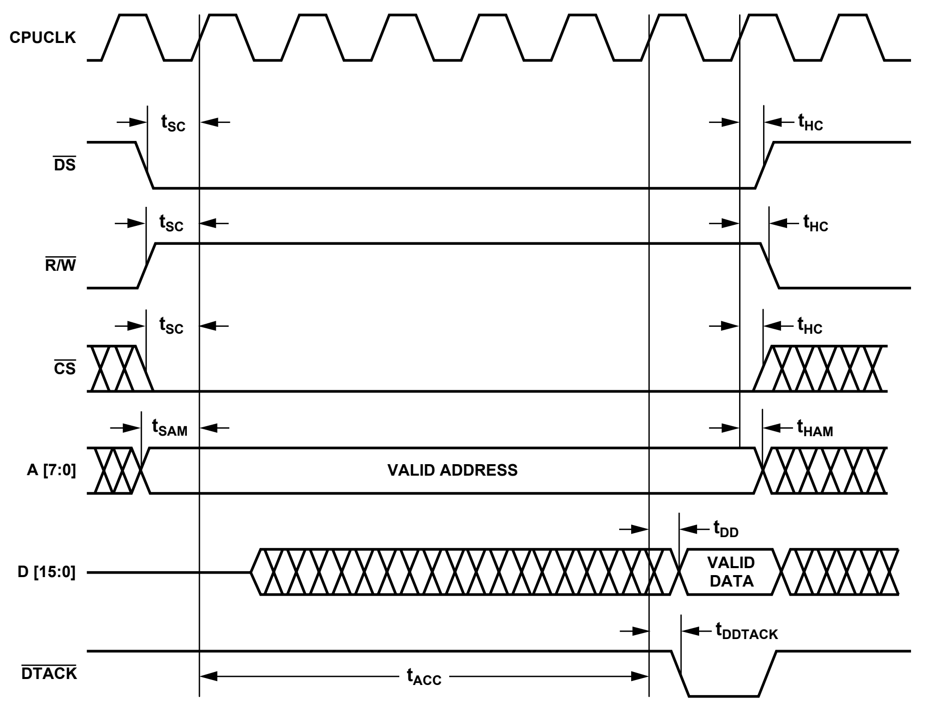
05156-011

Figure 11. INM Microport Read Timing Requirements



NOTE:
t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. IT CAN VARY FROM 3 TO 9 CPUCLK CYCLES.

Figure 12. MNM Microport Write Timing Requirements



NOTE:
t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. IT CAN VARY FROM 3 TO 9 CPUCLK CYCLES.

Figure 13. MNM Microport Read Timing Requirements

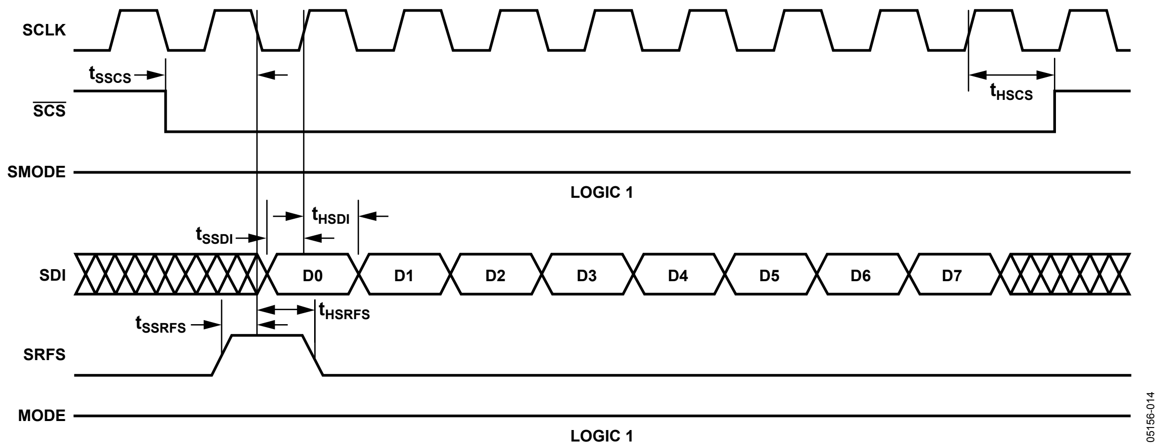


Figure 14. SPORT Mode Write Timing Characteristics

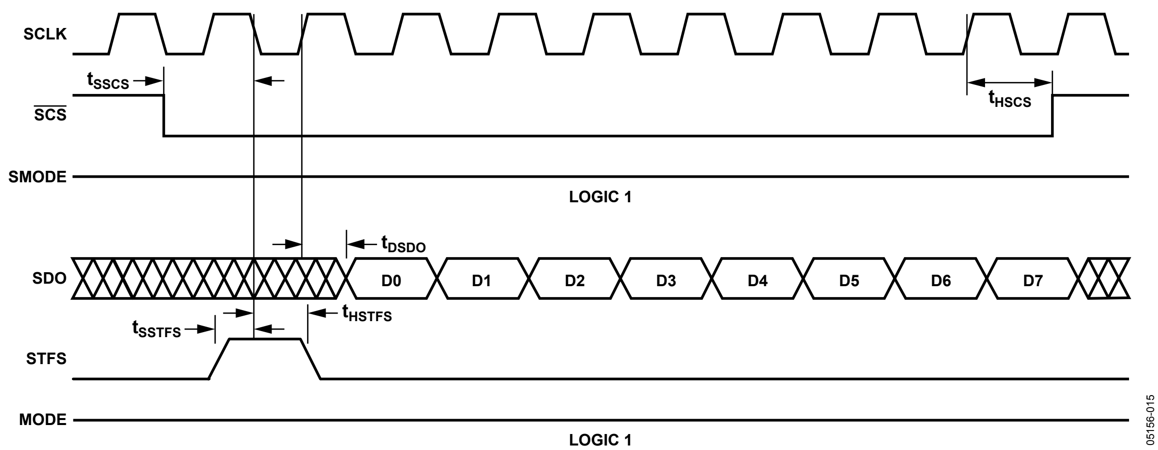


Figure 15. SPORT Mode Read Timing Characteristics

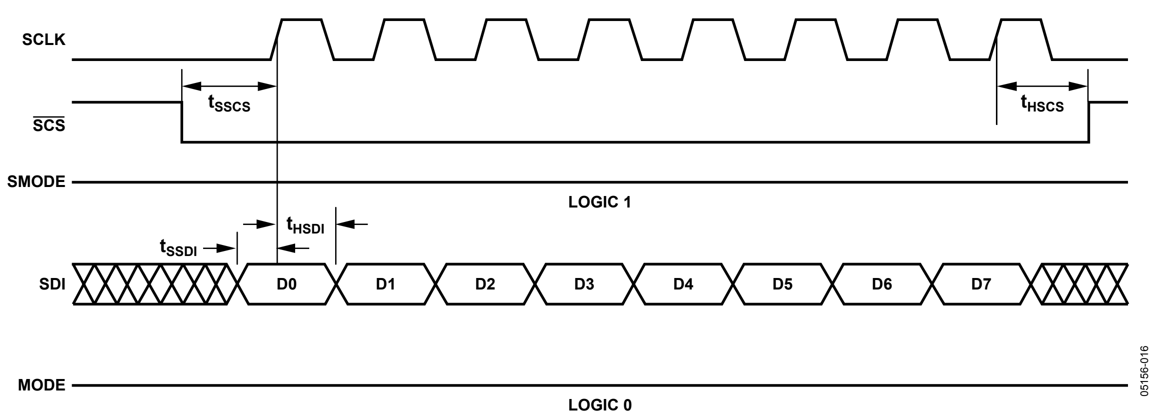


Figure 16. SPI Mode Write Timing Characteristics

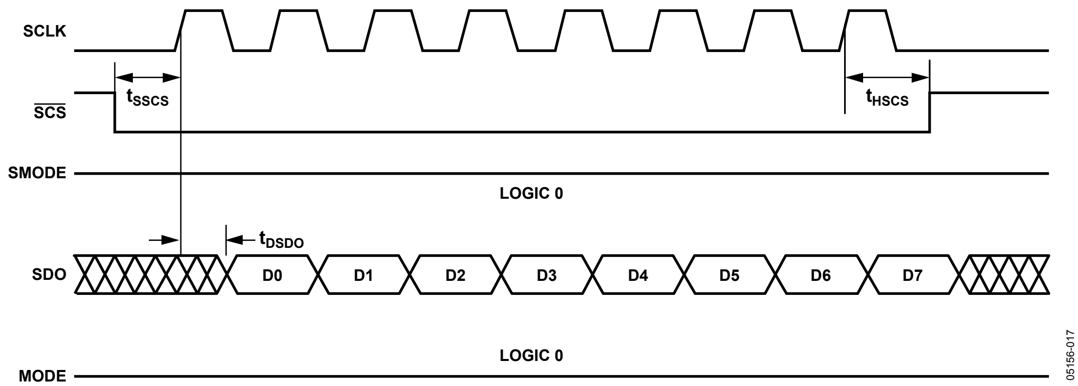


Figure 17. SPI Mode Read Timing Characteristics

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
AVDD	0 to +7.0 V
DRVDD	0 to +4.0 V
VDDCORE	−0.3 V to +2.2 V
VDDIO	0 to +4.0 V
Analog/Encode Input Voltage	0 to AVDD
Analog Input Current	25 mA
Digital Input Voltage	−0.3 V to + 3.6 V (not 5 V tolerant)
Digital Output Voltage	−0.3 V to VDDIO + 0.3 V
Operating Temperature Range (Ambient)	−25°C to +85°C
Junction Temperature Under Bias	150°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

256 BGA, 17 mm sq.

θ_{JA} = 21°C/W, no airflow.

Estimate based on JEDEC JC51-2 model using horizontally positioned 4-layer board.

EXPLANATION OF TEST LEVELS

Test Level	Description
I	100% production tested.
II	100% production tested at 25°C.
III	Sample tested only.
IV	Parameter guaranteed by design and analysis.
V	Parameter is typical value only.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	DGND	D14	D12	CPUCLK (SCLK)	PC3	PCCH1	PA12	PAIQ	PAGAIN	PB6	CLK	OVR	AVDD	AVDD	AGND	AGND	A
B	D7	CHIPID3	CHIPID2	$\overline{DS}$ (RD, SRFS)	PC5	PA5	PA15	PAACK	PB2	PB4	EXPC2	DNC	AVDD	AVDD	AGND	AGND	B
C	CHIPID0	MODE	$\overline{DTACK}$ (RDY, SDO)	R/$\overline{W}$ (WR, STFS)	PC0	PA3	PA9	PACH2	PB3	PB9	EXPC1	AVDD	AVDD	AVDD	AGND	AGND	C
D	EXT_ FILTER	MSB_ FIRST	$\overline{CS}$ ($\overline{SCS}$)	PC6	PC2	PA1	PA7	PACH0	PB0	PB15	EXPC0	DRVDD	AVDD	AVDD	AGND	AGND	D
E	CHIPID1	$\overline{IRP}$	VDDIO	VDD CORE	PCACK	VDD CORE	VDD CORE	VDD CORE	VDDIO	VDDIO	VDDIO	DRVDD	AVDD	AVDD	AGND	AGND	E
F	SMODE	D13	D15	$\overline{RESET}$	D1	VDD CORE	VDD CORE	VDD CORE	VDDIO	VDDIO	VDDIO	DRVDD	AVDD	AVDD	AGND	C2	F
G	DGND	D8	D9	D2	D5	DGND	DGND	DGND	DGND	DGND	DGND	DRVDD	AVDD	AVDD	AGND	AGND	G
H	D3	D11	D4	D10	A6	DGND	DGND	DGND	DGND	DGND	DGND	DRVDD	AVDD	AVDD	AGND	C1	H
J	DGND	D6	D0	A7	A1	DGND	DGND	DGND	DGND	DGND	DGND	DRVDD	AVDD	AVDD	AGND	AGND	J
K	A5	A4	A0 (SDI)	A2	PC8	DGND	DGND	DGND	DGND	DGND	DGND	DRVDD	AVDD	AVDD	AGND	AGND	K
L	A3	PC12	PC11	PC15	PC10	VDDIO	VDDIO	VDDIO	VDD CORE	VDD CORE	VDD CORE	DRVDD	AVDD	AVDD	AGND	AIN–	L
M	PC14	PC13	PC9	PC7	PCCH0	VDDIO	VDDIO	VDDIO	VDD CORE	VDD CORE	VDD CORE	DRVDD	AVDD	AVDD	AGND	AIN+	M
N	PC1	PC4	PA13	PA8	PA0	PAREQ	PB1	PBREQ	DGND	DGND	DGND	DRVDD	AVDD	AVDD	AGND	AGND	N
P	PCIQ	PCREQ	PA14	PA10	PB10	PB7	PB8	PBCH1	PBACK	PBCH0	SYNC2	DRVDD	AVDD	AVDD	AGND	AGND	P
R	PCCH2	PCGAIN	PA6	PA2	PACH1	PB13	PB11	PBCH2	PB14	PBGAIN	SYNC1	DRVDD	AGND	AGND	AGND	ENC–	R
T	DGND	PA11	PA4	PCLK	PB5	PB12	PBIQ	DGND	DNC	SYNC0	SYNC3	DR	AGND	V_{REF}	AGND	ENC+	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

DNC = DO NOT CONNECT

05156-018

Figure 18. 256 BGA Configuration (Top View)

Table 11. Pin Function Descriptions

Name	Type	Pin Number	Function
POWER SUPPLY			
AVDD	Power	See Table 12	5 V Analog ADC Core Supply.
DRVDD	Power	See Table 12	3.3 V ADC Output Driver Supply.
VDDCORE	Power	See Table 12	1.8 V Digital DDC Core Supply.
VDDIO	Power	See Table 12	3.3 V Digital DDC I/O Supply.
DGND	Ground	See Table 12	Digital Core and I/O Ground.
AGND	Ground	See Table 12	Analog ADC Ground.
ADC INPUTS			
AIN+	Input	M16	Differential Analog Input.
AIN–	Input	L16	Differential Analog Input.
ENC+	Input	T16	Differential Encode Input. Conversion initiated on rising edge.
ENC–	Input	R16	Differential Encode Input.
ADC OUTPUTS			
DR	Output	T12	Data Ready. Inverted and delayed representation of ENC+ used for driving the DDC CLK input.
OVR	Output	A12	Overange Bit. A logic high indicates analog input exceeds ±FS.
V_{REF}	Output	T14	2.4 V Fixed Internal Voltage Reference. Bypass to AGND with 0.1 µF chip capacitor.
C1	Output	H16	Compensation Pin for ADC Voltage Reference. Bypass to AGND with 0.1 µF chip capacitor.
C2	Output	F16	Compensation Pin for ADC Voltage Reference. Bypass to AGND with 0.1 µF chip capacitor.

Name	Type	Pin Number	Function
DDC INPUTS			
CLK	Input	A11	DDC Clock Input.
SYNC0	Input	T10	Synchronization Input 0. SYNC pins are independent of channels.
SYNC1	Input	R11	Synchronization Input 1.
SYNC2	Input	P11	Synchronization Input 2.
SYNC3	Input	T11	Synchronization Input 3.
DDC OUTPUTS			
EXPC [2:0]	Output	D11, C11, B11	External VGA Gain Control Bits. GND all pins if not used.
DDC OUTPUT PORTS			
PCLK	Bi-dir	T4	Parallel Output Port Clock. PCLK is bi-directional: master mode = output, slave mode = input.
PADATA[15:0]	Output	See Table 12	Parallel Output Port A Data Bus.
PACH[2:0]	Output	D8, R5, C8	Channel Indicator Output Port A.
PAIQ	Output	A8	Parallel Port A I/Q Data Indicator. Logic 1 indicates I data on data bus.
PAGAIN	Output	A9	Parallel Port A Gain Word Output Indicator. Logic 1 indicates gain word on data bus.
PAACK	Input	B8	Parallel Port A Acknowledge (Active High).
PAREQ	Output	N6	Parallel Port A Request (Active High).
PBDATA[15:0]	Output	See Table 12	Parallel Output Port B Data Bus.
PBCH[2:0]	Output	P10, P8, R8	Channel Indicator Output Port B.
PBIQ	Output	T7	Parallel Port B I/Q Data Indicator. Logic 1 indicates I data on data bus.
PBGAIN	Output	R10	Parallel Port B Gain Word Output Indicator. Logic 1 indicates gain word on data bus.
PBACK	Input	P9	Parallel Port B Acknowledge (Active High).
PBREQ	Output	N8	Parallel Port B Request (Active High)
PCDATA[15:0]	Output	See Table 12	Parallel Output Port C Data Bus.
PCCH[2:0]	Output	M5, A6, R1	Channel Indicator Output Port C.
PCIQ	Output	P1	Parallel Port C I/Q Data Indicator. Logic 1 indicates I data on data bus.
PCGAIN	Output	R2	Parallel Port C Gain word Output Indicator. Logic 1 indicates gain word on data bus.
PCACK	Input	E5	Parallel Port C Acknowledge (Active High).
PCREQ	Output	P2	Parallel Port C Request (Active High).
MICROPORT CONTROL			
D[15:0]	Bi-Dir	See Table 12	Bidirectional Microport Data. This bus is three-stated when $\overline{\text{CS}}$ is high.
A[7:0]	Input	See Table 12	Microport Address Bus.
$\overline{\text{DS}}$ ($\overline{\text{RD}}$)	Input	B4	Active Low Data Strobe, MODE = 1. Active low read strobe when MODE = 0.
$\overline{\text{DTACK}}$ (RDY)[1]	Output	C3	Active Low Data Acknowledge, MODE = 1. Microport status pin when MODE = 0. Terminate to VDDIO through external 1 kΩ pull-up resistor.
R/$\overline{\text{W}}$ ($\overline{\text{WR}}$)	Input	C4	Read/Write Strobe, MODE = 1. Active low write strobe when MODE = 0.
MODE	Input	C2	Mode Select. Logic 0 = Intel® mode, Logic 1 = Motorola mode.
$\overline{\text{CS}}$	Input	D3	Active Low Chip Select. Logic 1 three-states the microport data bus.
CPUCLK	Input	A4	Microport CLK Input. (Input only.)
CHIPID[3:0]	Input	C1, E1, B3, B2	Chip ID Input Pins.
SERIAL PORT CONTROL			
SCLK	Input	A4	Serial Clock. Should have a rise/fall time of 3ns max.
SDO[1]	Output	C3	Serial Port Data Output. Terminate to VDDIO through external 1 kΩ pull-up resistor.
SDI[2]	Input	K3	Serial Port Data Input.
STFS	Input	C4	Serial Transmit Frame Sync.
$\overline{\text{SRFS}}$	Input	B4	Serial Receive Frame Sync.
$\overline{\text{SCS}}$	Input	D3	Serial Chip Select.
MSB_FIRST	Input	D2	Most Significant Bit_First. Selects MSB_FIRST into SDI pin, and MSB_FIRST out of SDO pin. Logic 1 = MSB_FIRST; Logic 0 = LSB_FIRST
SMODE	Input	F1	Serial Mode Select.
MISC PINS			
DNC	-------	B12, T9	Do Not Connect.
$\overline{\text{IRP}}$[1]	Output	E2	Interrupt Pin (Active Low). Terminate to VDDIO through external 1 kΩ pull-up resistor.
$\overline{\text{RESET}}$	Input	F4	Master Reset, Active Low.
EXT_FILTER	Input	D1	PLL Loop Filter (Analog Pin). Connect to VDDCORE through series 250 Ω and 0.01 μF capacitor.

[1] Pins with internal pull-up resistor of nominal 70 kΩ.

[2] Pins with internal pull-down resistor of nominal 70 kΩ.

Table 12. Pin Listing for Power, Ground, and Data Buses

Name	Pin Number
AVDD	A13, A14, B13, B14, C12, C13, C14, D13, D14, E13, E14, F13, F14, G13, G14, H13, H14, J13, J14, K13, K14, L13, L14, M13, M14, N13, N14, P13, P14
AGND	A15, A16, B15, B16, C15, C16, D15, D16, E15, E16, F15, G15, G16, H15, J15, J16, K15, K16, L15, M15, N15, N16, P15, P16, R13, R14, R15, T13, T15
DRVDD	D12, E12, F12, G12, H12, J12, K12, L12, M12, N12, P12, R12
VDDIO	E3, E9, E10, E11, F9, F10, F11, L6, L7, L8, M6, M7, M8
VDDCORE	E4, E6, E7, E8, F6, F7, F8, L9, L10, L11, M9, M10, M11
DGND	A1, G1, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J1, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, N9, N10, N11, T1, T8
PADATA[15:0]	N5, D6, R4, C6,T3, B6, R3, D7, N4, C7, P4, T2, A7, N3, P3, B7
PBDATA[15:0]	D9, N7, B9, C9, B10, T5, A10, P6, P7, C10, P5, R7, T6, R6, R9, D10
PCDATA[15:0]	C5, N1, D5, A5, N2, B5, D4, M4, K5, M3, L5, L3, L2, M2, M1, L4
D[15:0]	J3, F5, G4, H1, H3, G5, J2, B1, G2, G3, H4, H2, A3, F2, A2, F3
A[7:0]	K3, J5, K4, L1, K2, K1, H5, J4

TYPICAL PERFORMANCE CHARACTERISTICS

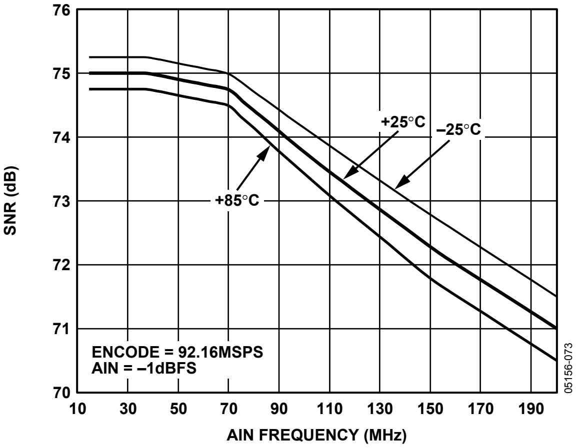


Figure 19. ADC Noise vs. Analog Frequency (46.08 MHz BW)

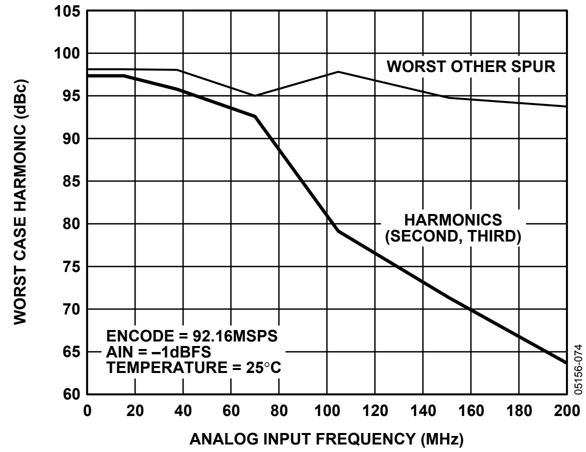


Figure 22. Harmonics vs. Analog Frequency (IF)

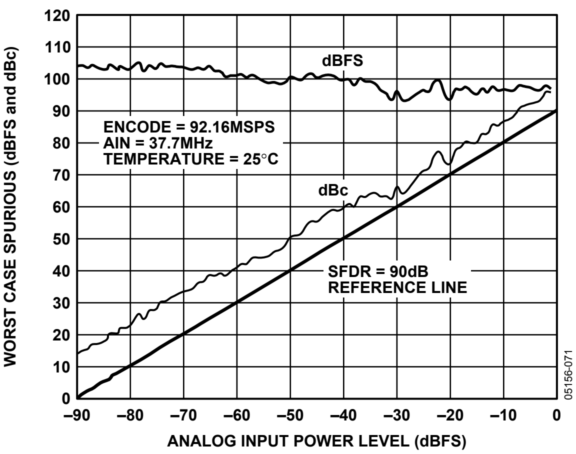


Figure 20. Single Tone SFDR at 37.7 MHz

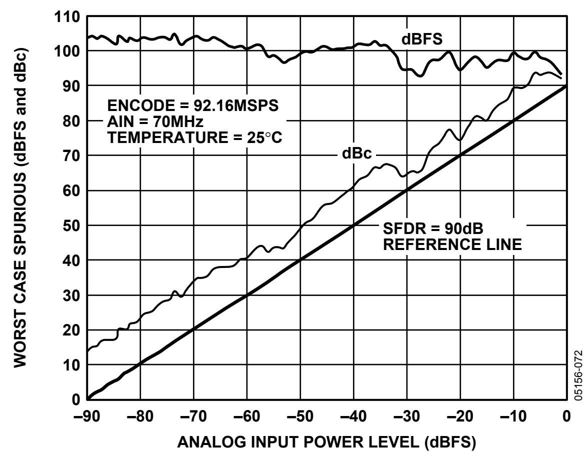


Figure 23. Single Tone SFDR at 70 MHz

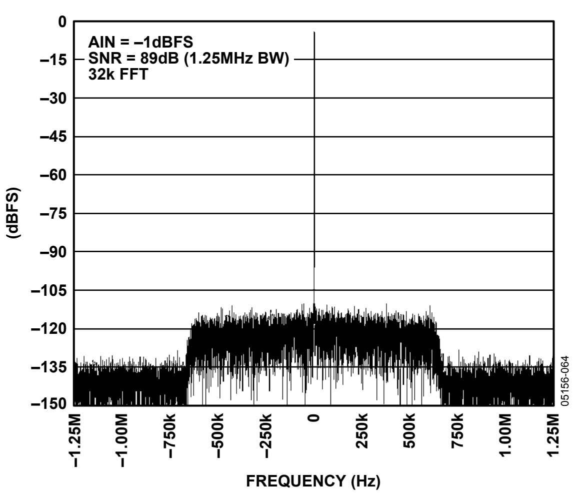


Figure 21. CDMA Single Tone AIN = 70 MHz; ENC = 92.16 MSPS

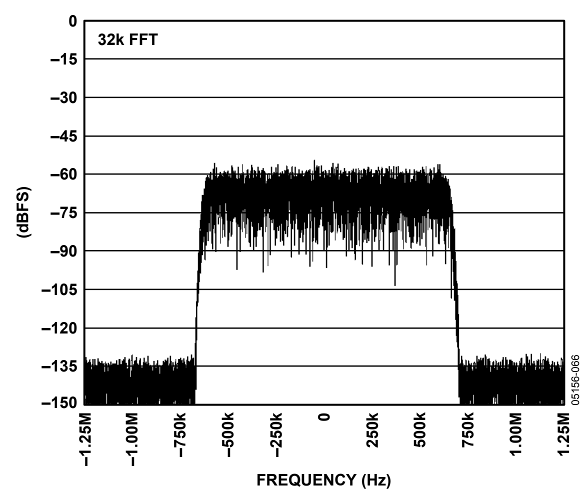


Figure 24. CDMA Carrier AIN = 70 MHz; ENC = 92.16 MSPS

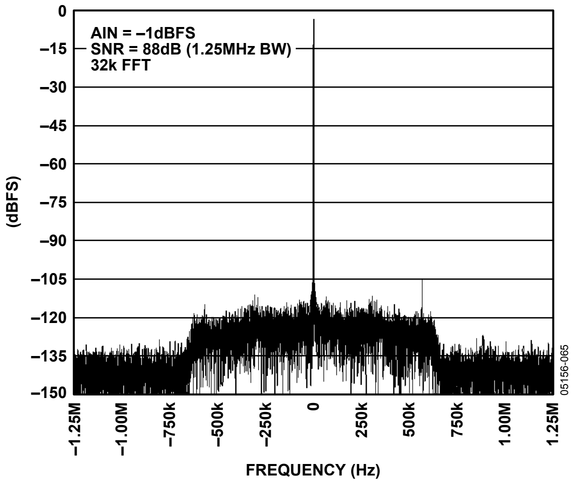


Figure 25. CDMA Single Tone AIN = 151.5 MHz; ENC = 92.16 MSPS

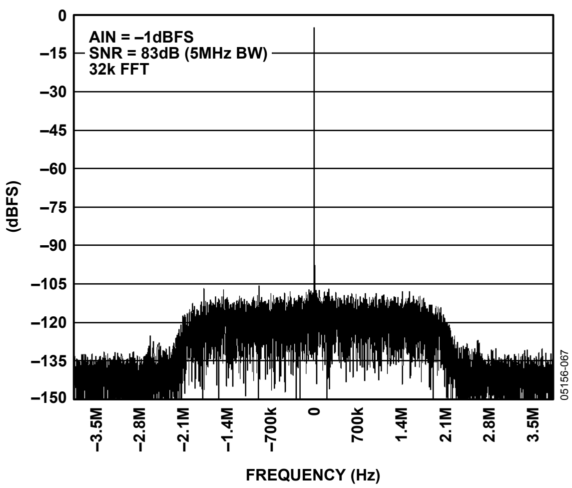


Figure 26. WCDMA Single Tone AIN = 70 MHz; Encode = 92.16 MSPS

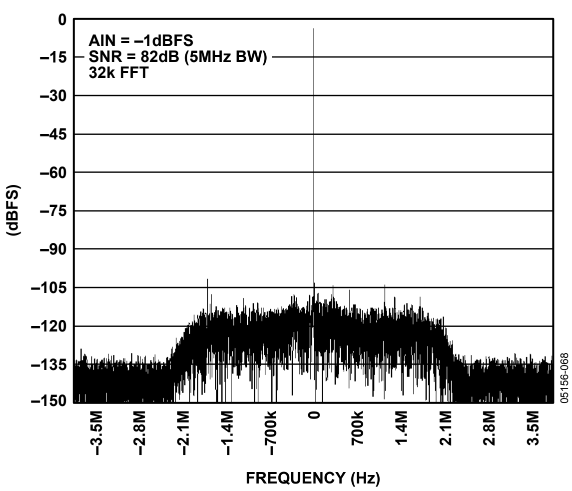


Figure 27. WCDMA Single Tone AIN = 151.5 MHz; Encode = 92.16 MSPS

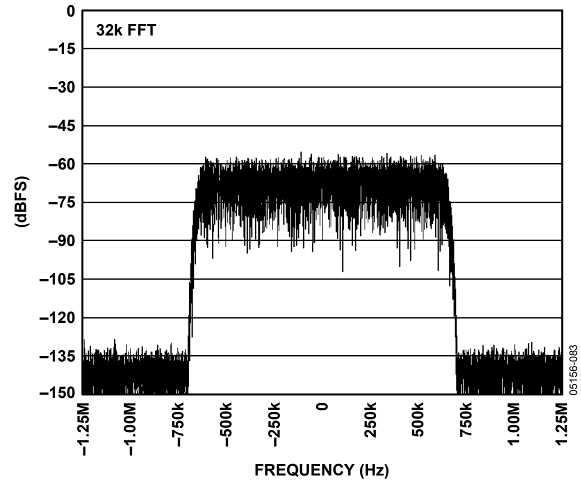


Figure 28. CDMA Carrier AIN = 151.5 MHz; ENC = 92.16 MSPS

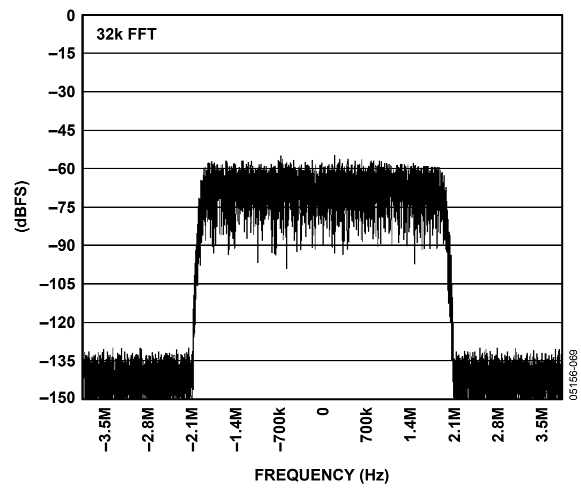


Figure 29. WCDMA Carrier AIN = 70 MHz; Encode = 92.16 MSPS

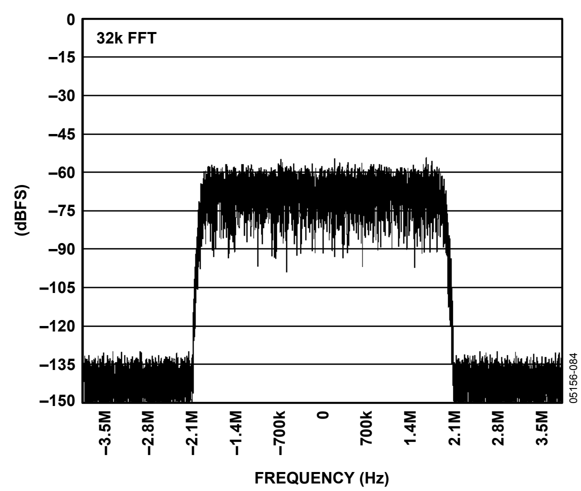


Figure 30. WCDMA Carrier AIN = 151.5 MHz; Encode = 92.16 MSPS

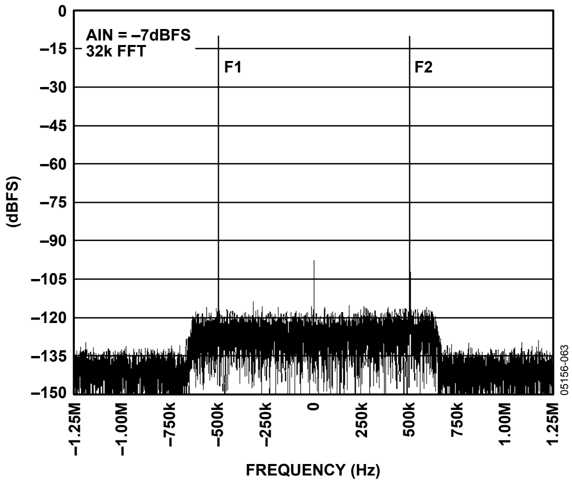


Figure 31. CDMA Two Tones at 55 MHz and 56 MHz; ENC = 92.16 MSPS

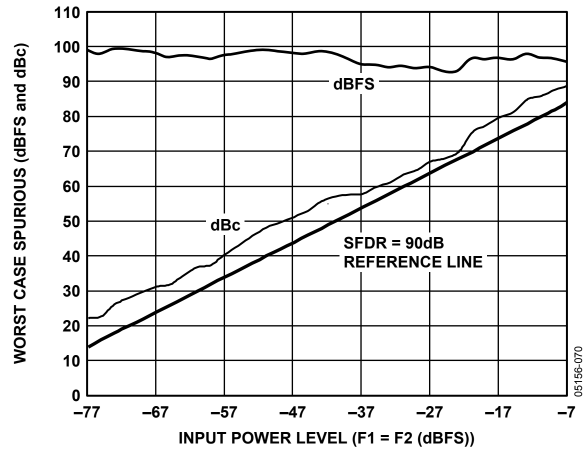


Figure 32. Two Tone SFDR at 55 MHz and 56 MHz