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IF Diversity Receiver

Data Sheet

AD6655

FEATURES

- SNR = 74.5 dBc (75.5 dBFS) in a 32.7 MHz BW at 70 MHz at 150 MSPS
- SFDR = 80 dBc to 70 MHz at 150 MSPS
- 1.8 V analog supply operation
- 1.8 V to 3.3 V CMOS output supply or 1.8 V LVDS output supply
- Integer 1-to-8 input clock divider
- Integrated dual-channel ADC
  - Sample rates up to 150 MSPS
  - IF sampling frequencies to 450 MHz
  - Internal ADC voltage reference
  - Integrated ADC sample-and-hold inputs
  - Flexible analog input range: 1 V p-p to 2 V p-p
  - ADC clock duty cycle stabilizer
  - 95 dB channel isolation/crosstalk
- Integrated wideband digital downconverter (DDC)
  - 32-bit complex, numerically controlled oscillator (NCO)
  - Decimating half-band filter and FIR filter
  - Supports real and complex output modes
- Fast attack/threshold detect bits
- Composite signal monitor
- Energy-saving power-down modes

APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers (3G)
  - TD-SCDMA, WiMax, WCDMA, CDMA2000, GSM, EDGE, LTE
- I/Q demodulation systems
- Smart antenna systems
- General-purpose software radios
- Broadband data applications

PRODUCT HIGHLIGHTS

1. Integrated dual, 14-bit, 150 MSPS ADC.
2. Integrated wideband decimation filter and 32-bit complex NCO.
3. Fast overrange detect and signal monitor with serial output.
4. Proprietary differential input maintains excellent SNR performance for input frequencies up to 450 MHz.
5. Flexible output modes, including independent CMOS, interleaved CMOS, IQ mode CMOS, and interleaved LVDS.
6. SYNC input allows synchronization of multiple devices.
7. 3-bit SPI port for register programming and register readback.

FUNCTIONAL BLOCK DIAGRAM

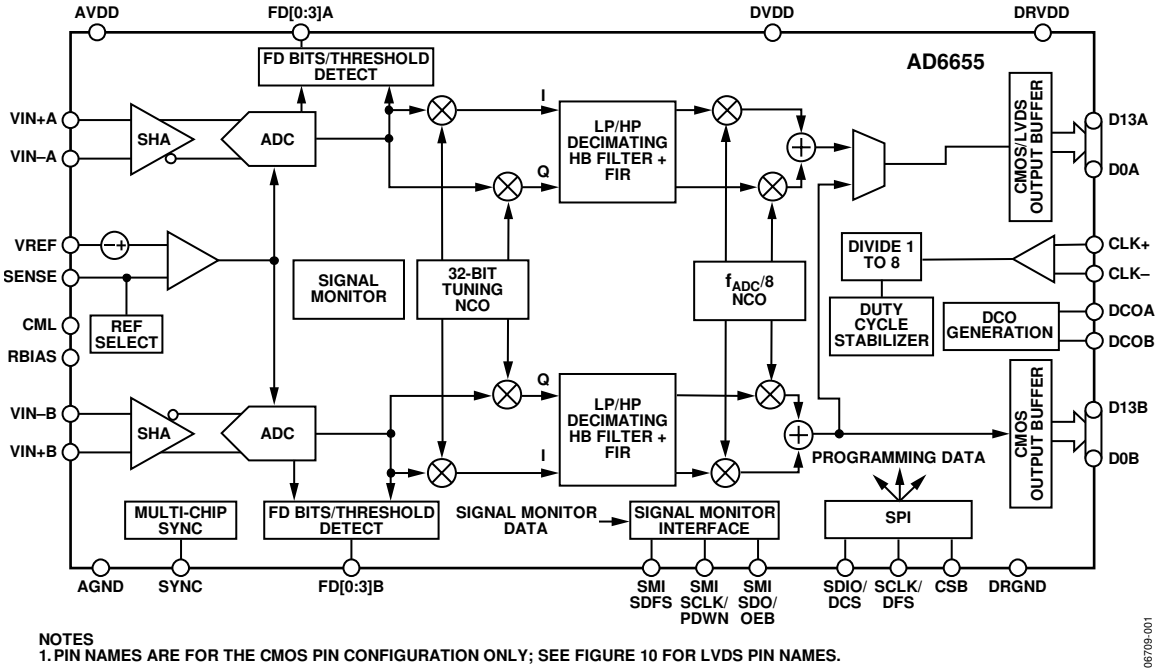

Figure 1.

Rev. B Document Feedback

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Tel: 781.329.4700

Technical Support www.analog.com

AD6655* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD6655 Evaluation Board

DOCUMENTATION

Application Notes

- AN-0974: Multicarrier TD-SCMA Feasibility
- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-812: MicroController-Based Serial Port Interface (SPI) Boot Circuit
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD6655: IF Diversity Receiver Data Sheet

TOOLS AND SIMULATIONS

- Visual Analog
- AD6655 IBIS Models
- AD6653/AD6655 S-Parameters

REFERENCE MATERIALS

Technical Articles

- Matching An ADC To A Transformer

DESIGN RESOURCES

- AD6655 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD6655 EngineerZone Discussions.

SAMPLE AND BUY

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GENERAL DESCRIPTION

The AD6655 is a mixed-signal intermediate frequency (IF) receiver consisting of dual 14-bit, 80 MSPS/105 MSPS/125 MSPS/150 MSPS ADCs and a wideband digital downconverter (DDC). The AD6655 is designed to support communications applications where low cost, small size, and versatility are desired.

The dual ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth differential sample-and-hold analog input amplifiers supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

ADC data outputs are internally connected directly to the digital downconverter (DDC) of the receiver, simplifying layout and reducing interconnection parasitics. The digital receiver has two channels and provides processing flexibility. Each receive channel has four cascaded signal processing stages: a 32-bit frequency translator (numerically controlled oscillator (NCO)), a half-band decimating filter, a fixed FIR filter, and an $f_{ADC}/8$ fixed-frequency NCO.

In addition to the receiver DDC, the AD6655 has several functions that simplify the automatic gain control (AGC) function in the system receiver. The fast detect feature allows fast overrange detection by outputting four bits of input level information with short latency.

In addition, the programmable threshold detector allows monitoring of the incoming signal power using the four fast detect bits of the ADC with low latency. If the input signal level exceeds the programmable threshold, the coarse upper threshold indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition.

The second AGC-related function is the signal monitor. This block allows the user to monitor the composite magnitude of the incoming signal, which aids in setting the gain to optimize the dynamic range of the overall system.

After digital processing, data can be routed directly to the two external 14-bit output ports. These outputs can be set from 1.8 V to 3.3 V CMOS or as 1.8 V LVDS. The CMOS data can also be output in an interleaved configuration at a double data rate using only Port A.

The AD6655 receiver digitizes a wide spectrum of IF frequencies. Each receiver is designed for simultaneous reception of the main channel and the diversity channel. This IF sampling architecture greatly reduces component cost and complexity compared with traditional analog techniques or less integrated digital methods.

Flexible power-down options allow significant power savings, when desired.

Programming for setup and control is accomplished using a 3-bit SPI-compatible serial interface.

The AD6655 is available in a 64-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C.

SPECIFICATIONS

ADC DC SPECIFICATIONS—AD6655-80/AD6655-105

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 1.

		AD6655-80			AD6655-105			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	14			14			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full		±0.2	±0.6		±0.2	±0.6	% FSR
Gain Error	Full	−3.6	−1.8	−0.1	−4.3	−2.2	−0.5	% FSR
MATCHING CHARACTERISTIC								
Offset Error	25°C		±0.2	±0.6		±0.2	±0.6	% FSR
Gain Error	25°C		±0.2	±0.75		±0.2	±0.75	% FSR
TEMPERATURE DRIFT								
Offset Error	Full		±15			±15		ppm/°C
Gain Error	Full		±95			±95		ppm/°C
INTERNAL VOLTAGE REFERENCE								
Output Voltage Error (1 V Mode)	Full		±5	±18		±5	±18	mV
Load Regulation at 1.0 mA	Full		7			7		mV
INPUT-REFERRED NOISE								
VREF = 1.0 V	25°C		0.85			0.85		LSB rms
ANALOG INPUT								
Input Span, VREF = 1.0 V	Full		2			2		V p-p
Input Capacitance[1]	Full		8			8		pF
VREF INPUT RESISTANCE	Full		6			6		kΩ
POWER SUPPLIES								
Supply Voltage								
AVDD, DVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD (CMOS Mode)	Full	1.7	3.3	3.6	1.7	3.3	3.6	V
DRVDD (LVDS Mode)	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current								
I_{AVDD}[2, 3]	Full		235	420		315	575	mA
I_{DVDD}[2, 3]	Full		175			225		mA
I_{DRVDD}[2] (3.3 V CMOS)	Full		18			21		mA
I_{DRVDD}[2] (1.8 V CMOS)	Full		8			11		mA
I_{DRVDD}[2] (1.8 V LVDS)	Full		55			56		mA
POWER CONSUMPTION								
DC Input	Full		470	490		620	650	mW
Sine Wave Input[2] (DRVDD = 1.8 V)	Full		755			995		mW
Sine Wave Input[2] (DRVDD = 3.3 V)	Full		800			1040		mW
Standby Power[4]	Full		52			68		mW
Power-Down Power	Full		2.5	8		2.5	8	mW

[1] Input capacitance refers to the effective capacitance between one differential input pin and AGND. See Figure 11 for the equivalent analog input structure.
[2] Measured with a 9.7 MHz, full-scale sine wave input, NCO enabled with a frequency of 13 MHz, FIR filter enabled and the $f_S/8$ output mix enabled with approximately 5 pF loading on each output bit.
[3] The maximum limit applies to the combination of I_{AVDD} and I_{DVDD} currents.
[4] Standby power is measured with a dc input and with the CLK pin inactive (set to AVDD or AGND).

ADC DC SPECIFICATIONS—AD6655-125/AD6655-150

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 2.

		AD6655-125			AD6655-150			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	14			14			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full		±0.3	±0.6		±0.2	±0.6	% FSR
Gain Error	Full	−4.7	−2.7	−0.8	−5.1	−3.2	−1.0	% FSR
MATCHING CHARACTERISTIC								
Offset Error	25°C		±0.3	±0.7		±0.2	±0.7	% FSR
Gain Error	25°C		±0.1	±0.7		±0.2	±0.8	% FSR
TEMPERATURE DRIFT								
Offset Error	Full		±15			±15		ppm/°C
Gain Error	Full		±95			±95		ppm/°C
INTERNAL VOLTAGE REFERENCE								
Output Voltage Error (1 V Mode)	Full		±5	±18		±5	±18	mV
Load Regulation at 1.0 mA	Full		7			7		mV
INPUT-REFERRED NOISE								
VREF = 1.0 V	25°C		0.85			0.85		LSB rms
ANALOG INPUT								
Input Span, VREF = 1.0 V	Full		2			2		V p-p
Input Capacitance[1]	Full		8			8		pF
VREF INPUT RESISTANCE	Full		6			6		kΩ
POWER SUPPLIES								
Supply Voltage								
AVDD, DVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD (CMOS Mode)	Full	1.7	1.8	3.6	1.7	1.8	3.6	V
DRVDD (LVDS Mode)	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current								
I_{AVDD}[2, 3]	Full		390	705		440	805	mA
I_{DVDD}[2, 3]	Full		270			320		mA
I_{DRVDD}[2] (3.3 V CMOS)	Full		26			28		mA
I_{DRVDD}[2] (1.8 V CMOS)	Full		13			17		mA
I_{DRVDD}[2] (1.8 V LVDS)	Full		57			57		mA
POWER CONSUMPTION								
DC Input	Full		770	810		870	920	mW
Sine Wave Input[2] (DRVDD = 1.8 V)	Full		1215			1395		mW
Sine Wave Input[2] (DRVDD = 3.3 V)	Full		1275			1450		mW
Standby Power[4]	Full		77			77		mW
Power-down Power	Full		2.5	8		2.5	8	mW

[1] Input capacitance refers to the effective capacitance between one differential input pin and AGND. See Figure 11 for the equivalent analog input structure.
[2] Measured with a 9.7 MHz, full-scale sine wave input, NCO enabled with a frequency of 13 MHz, FIR filter enabled and the $f_S/8$ output mix enabled with approximately 5 pF loading on each output bit.
[3] The maximum limit applies to the combination of I_{AVDD} and I_{DVDD} currents.
[4] Standby power is measured with a dc input, the CLK pin inactive (set to AVDD or AGND).

ADC AC SPECIFICATIONS—AD6655-80/AD6655-105

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, NCO enabled, half-band filter enabled, FIR filter enabled, unless otherwise noted.

Table 3.

		AD6655-80			AD6655-105			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE-RATIO (SNR)								
f_{IN} = 2.4 MHz	25°C		74.9			74.8		dB
f_{IN} = 70 MHz	25°C		74.8			74.7		dB
	Full	73.0			73.0			dB
f_{IN} = 140 MHz	25°C		74.5			74.3		dB
f_{IN} = 220 MHz	25°C		73.4			73.4		dB
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 2.4 MHz	25°C		−86			−86		dBc
f_{IN} = 70 MHz	25°C		−85			−85		dBc
	Full			−74			−74	dBc
f_{IN} = 140 MHz	25°C		−84			−84		dBc
f_{IN} = 220 MHz	25°C		−83			−83		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 2.4 MHz	25°C		86			86		dBc
f_{IN} = 70 MHz	25°C		85			85		dBc
	Full	74			74			dBc
f_{IN} = 140 MHz	25°C		84			84		dBc
f_{IN} = 220 MHz	25°C		83			83		dBc
WORST OTHER HARMONIC OR SPUR[2]								
f_{IN} = 2.4 MHz	25°C		−93			−93		dBc
f_{IN} = 70 MHz	25°C		−90			−90		dBc
	Full			−82			−82	dBc
f_{IN} = 140 MHz	25°C		−89			−89		dBc
f_{IN} = 220 MHz	25°C		−86			−86		dBc
TWO-TONE SFDR								
f_{IN} = 29.12 MHz, 32.12 MHz (−7 dBFS)	25°C		85			85		dBc
f_{IN} = 169.12 MHz, 172.12 MHz (−7 dBFS)	25°C		81			81		dBc
CROSSTALK[3]	Full		95			95		dB
ANALOG INPUT BANDWIDTH	25°C		650			650		MHz

[1] See Application Note AN-835, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] See the Applications Information section for more information about the worst other specifications for the AD6655.
[3] Crosstalk is measured at 100 MHz with −1 dBFS on one channel and with no input on the alternate channel.

ADC AC SPECIFICATIONS—AD6655-125/AD6655-150

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, NCO enabled, half-band filter enabled, FIR filter enabled, unless otherwise noted.

Table 4.

		AD6655-125			AD6655-150			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE-RATIO (SNR)								
f_{IN} = 2.4 MHz	25°C		74.7			74.6		dB
f_{IN} = 70 MHz	25°C		74.6			74.5		dB
	Full	73.0			72.5			dB
f_{IN} = 140 MHz	25°C		74.2			73.9		dB
f_{IN} = 220 MHz	25°C		73.3			73.0		dB
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 2.4 MHz	25°C		−86			−85		dBc
f_{IN} = 70 MHz	25°C		−85			−84		dBc
	Full			−73			−73	dBc
f_{IN} = 140 MHz	25°C		−84			−83		dBc
f_{IN} = 220 MHz	25°C		−83			−77		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 2.4 MHz	25°C		86			85		dBc
f_{IN} = 70 MHz	25°C		85			80		dBc
	Full	73			73			dBc
f_{IN} = 140 MHz	25°C		84			76		dBc
f_{IN} = 220 MHz	25°C		83			74		dBc
WORST OTHER HARMONIC OR SPUR[2]								
f_{IN} = 2.4 MHz	25°C		−92			−87		dBc
f_{IN} = 70 MHz	25°C		−90			−80		dBc
	Full			−82			−80	dBc
f_{IN} = 140 MHz	25°C		−88			−76		dBc
f_{IN} = 220 MHz	25°C		−84			−74		dBc
TWO-TONE SFDR								
f_{IN} = 29.12 MHz, 32.12 MHz (−7 dBFS)	25°C		85			85		dBc
f_{IN} = 169.12 MHz, 172.12 MHz (−7 dBFS)	25°C		81			81		dBc
CROSSTALK[3]	Full		95			95		dB
ANALOG INPUT BANDWIDTH	25°C		650			650		MHz

[1] See Application Note AN-835, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] See the Applications Information section for more information about the worst other specifications for the AD6655.
[3] Crosstalk is measured at 100 MHz with −1 dBFS on one channel and with no input on the alternate channel.

DIGITAL SPECIFICATIONS—AD6655-80/AD6655-105

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 5.

		AD6655-80			AD6655-105			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)								
Logic Compliance			CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		1.2			1.2		V
Differential Input Voltage	Full	0.2		6	0.2		6	V p-p
Input Voltage Range	Full	AVDD − 0.3		AVDD + 1.6	AVDD − 0.3		AVDD + 1.6	V
Input Common-Mode Range	Full	1.1		AVDD	1.1		AVDD	V
High Level Input Voltage	Full	1.2		3.6	1.2		3.6	V
Low Level Input Voltage	Full	0		0.8	0		0.8	V
High Level Input Current	Full	−10		+10	−10		+10	µA
Low Level Input Current	Full	−10		+10	−10		+10	µA
Input Capacitance	Full		4			4		pF
Input Resistance	Full	8	10	12	8	10	12	kΩ
SYNC INPUT								
Logic Compliance			CMOS			CMOS		
Internal Bias	Full		1.2			1.2		V
Input Voltage Range	Full	AVDD − 0.3		AVDD + 1.6	AVDD − 0.3		AVDD + 1.6	V
High Level Input Voltage	Full	1.2		3.6	1.2		3.6	V
Low Level Input Voltage	Full	0		0.8	0		0.8	V
High Level Input Current	Full	−10		+10	−10		+10	µA
Low Level Input Current	Full	−10		+10	−10		+10	µA
Input Capacitance	Full		4			4		pF
Input Resistance	Full	8	10	12	8	10	12	kΩ
LOGIC INPUT (CSB)[1]								
High Level Input Voltage	Full	1.22		3.6	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	0		0.6	V
High Level Input Current	Full	−10		+10	−10		+10	µA
Low Level Input Current	Full	40		132	40		132	µA
Input Resistance	Full		26			26		kΩ
Input Capacitance	Full		2			2		pF
LOGIC INPUT (SCLK/DFS)[2]								
High Level Input Voltage	Full	1.22		3.6	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	0		0.6	V
High Level Input Current	Full	−92		−135	−92		−135	µA
Low Level Input Current	Full	−10		+10	−10		+10	µA
Input Resistance	Full		26			26		kΩ
Input Capacitance	Full		2			2		pF
LOGIC INPUTS (SDIO/DCS, SMI SDFS)[1]								
High Level Input Voltage	Full	1.22		3.6	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	0		0.6	V
High Level Input Current	Full	−10		+10	−10		+10	µA
Low Level Input Current	Full	38		128	38		128	µA
Input Resistance	Full		26			26		kΩ
Input Capacitance	Full		5			5		pF

Parameter	Temp	AD6655-80 Min	AD6655-80 Typ	AD6655-80 Max	AD6655-105 Min	AD6655-105 Typ	AD6655-105 Max	Unit
LOGIC INPUTS (SMI SDO/OEB, SMI SCLK/PDWN)[2]								
High Level Input Voltage	Full	1.22		3.6	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	0		0.6	V
High Level Input Current	Full	−90		−134	−90		−134	µA
Low Level Input Current	Full	−10		+10	−10		+10	µA
Input Resistance	Full		26			26		kΩ
Input Capacitance	Full		5			5		pF
DIGITAL OUTPUTS								
CMOS Mode—DRVDD = 3.3 V								
High Level Output Voltage								
I_{OH} = 50 µA	Full	3.29			3.29			V
I_{OH} = 0.5 mA	Full	3.25			3.25			V
Low Level Output Voltage								
I_{OL} = 1.6 mA	Full			0.2			0.2	V
I_{OL} = 50 µA	Full			0.05			0.05	V
CMOS Mode—DRVDD = 1.8 V								
High Level Output Voltage								
I_{OH} = 50 µA	Full	1.79			1.79			V
I_{OH} = 0.5 mA	Full	1.75			1.75			V
Low Level Output Voltage								
I_{OL} = 1.6 mA	Full			0.2			0.2	V
I_{OL} = 50 µA	Full			0.05			0.05	V
LVDS Mode, DRVDD = 1.8 V								
Differential Output Voltage (VOD), ANSI Mode	Full	250	350	450	250	350	450	mV
Output Offset Voltage (VOS), ANSI Mode	Full	1.15	1.25	1.35	1.15	1.25	1.35	V
Differential Output Voltage (VOD), Reduced Swing Mode	Full	150	200	280	150	200	280	mV
Output Offset Voltage (VOS), Reduced Swing Mode	Full	1.15	1.25	1.35	1.15	1.25	1.35	V

[1] Pull up.
[2] Pull down.

DIGITAL SPECIFICATIONS—AD6655-125/AD6655-150

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 6.

		AD6655-125			AD6655-150			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK–)								
Logic Compliance			CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		1.2			1.2		V
Differential Input Voltage	Full	0.2		6	0.2		6	V p-p
Input Voltage Range	Full	AVDD – 0.3		AVDD + 1.6	AVDD – 0.3		AVDD + 1.6	V
Input Common-Mode Range	Full	1.1 V		AVDD	1.1 V		AVDD	V
High Level Input Voltage	Full	1.2		3.6	1.2		3.6	V
Low Level Input Voltage	Full	0		0.8	0		0.8	V
High Level Input Current	Full	−10		+10	−10		+10	µA
Low Level Input Current	Full	−10		+10	−10		+10	µA
Input Capacitance	Full		4			4		pF
Input Resistance	Full	8	10	12	8	10	12	kΩ
SYNC INPUT								
Logic Compliance			CMOS			CMOS		
Internal Bias	Full		1.2			1.2		V
Input Voltage Range	Full	AVDD – 0.3		AVDD + 1.6	AVDD – 0.3		AVDD + 1.6	V
High Level Input Voltage	Full	1.2		3.6	1.2		3.6	V
Low Level Input Voltage	Full	0		0.8	0		0.8	V
High Level Input Current	Full	−10		+10	−10		+10	µA
Low Level Input Current	Full	−10		+10	−10		+10	µA
Input Capacitance	Full		4			4		pF
Input Resistance	Full	8	10	12	8	10	12	kΩ
LOGIC INPUT (CSB)[1]								
High Level Input Voltage	Full	1.22		3.6	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	0		0.6	V
High Level Input Current	Full	−10		+10	−10		+10	µA
Low Level Input Current	Full	40		132	40		132	µA
Input Resistance	Full		26			26		kΩ
Input Capacitance	Full		2			2		pF
LOGIC INPUT (SCLK/DFS)[2]								
High Level Input Voltage	Full	1.22		3.6	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	0		0.6	V
High Level Input Current	Full	−92		−135	−92		−135	µA
Low Level Input Current	Full	−10		+10	−10		+10	µA
Input Resistance	Full		26			26		kΩ
Input Capacitance	Full		2			2		pF
LOGIC INPUTS (SDIO/DCS, SMI SDFS)[1]								
High Level Input Voltage	Full	1.22		3.6	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	0		0.6	V
High Level Input Current	Full	−10		+10	−10		+10	µA
Low Level Input Current	Full	38		128	38		128	µA
Input Resistance	Full		26			26		kΩ
Input Capacitance	Full		5			5		pF

Parameter	Temp	AD6655-125 Min	AD6655-125 Typ	AD6655-125 Max	AD6655-150 Min	AD6655-150 Typ	AD6655-150 Max	Unit
LOGIC INPUTS (SMI SDO/OEB, SMI SCLK/PDWN)[2]								
High Level Input Voltage	Full	1.22		3.6	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	0		0.6	V
High Level Input Current	Full	−90		−134	−90		−134	µA
Low Level Input Current	Full	−10		+10	−10		+10	µA
Input Resistance	Full		26			26		kΩ
Input Capacitance	Full		5			5		pF
DIGITAL OUTPUTS								
CMOS Mode—DRVDD = 3.3 V								
High Level Output Voltage								
I_{OH} = 50 µA	Full	3.29			3.29			V
I_{OH} = 0.5 mA	Full	3.25			3.25			V
Low Level Output Voltage								
I_{OL} = 1.6 mA	Full			0.2			0.2	V
I_{OL} = 50 µA	Full			0.05			0.05	V
CMOS Mode—DRVDD = 1.8 V								
High Level Output Voltage								
I_{OH} = 50 µA	Full	1.79			1.79			V
I_{OH} = 0.5 mA	Full	1.75			1.75			V
Low Level Output Voltage								
I_{OL} = 1.6 mA	Full			0.2			0.2	V
I_{OL} = 50 µA	Full			0.05			0.05	V
LVDS Mode—DRVDD = 1.8 V								
Differential Output Voltage (VOD), ANSI Mode	Full	250	350	450	250	350	450	mV
Output Offset Voltage (VOS), ANSI Mode	Full	1.15	1.25	1.35	1.15	1.25	1.35	V
Differential Output Voltage (VOD), Reduced Swing Mode	Full	150	200	280	150	200	280	mV
Output Offset Voltage (VOS), Reduced Swing Mode	Full	1.15	1.25	1.35	1.15	1.25	1.35	V

[1] Pull up.
[2] Pull down.

SWITCHING SPECIFICATIONS—AD6655-80/AD6655-105

Table 7.

Parameter	Temp	AD6655-80 Min	AD6655-80 Typ	AD6655-80 Max	AD6655-105 Min	AD6655-105 Typ	AD6655-105 Max	Unit
CLOCK INPUT PARAMETERS								
Input Clock Rate	Full			625			625	MHz
Conversion Rate[1]								
DCS Enabled	Full	20		80	20		105	MSPS
DCS Disabled	Full	10		80	10		105	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	12.5			9.5			ns
CLK Pulse Width High (t_{CLKH})								
Divide-by-1 Mode, DCS Enabled	Full	3.75	6.25	8.75	2.85	4.75	6.65	ns
Divide-by-1 Mode DCS Disabled	Full	5.63	6.25	6.88	4.28	4.75	5.23	ns
Divide-by-2 Mode, DCS Enabled	Full	1.6			1.6			ns
Divide-by-3 Through Divide-by-8 Modes, DCS Enabled	Full	0.8			0.8			ns
DATA OUTPUT PARAMETERS (DATA, FD)								
CMOS Noninterleaved Mode—DRVDD = 1.8 V								
Data Propagation Delay (t_{PD})[2]	Full	1.6	3.9	6.2	1.6	3.9	6.2	ns
DCO Propagation Delay (t_{DCO})	Full	4.0	5.4	7.3	4.0	5.4	7.3	ns
Setup Time (t_S)	Full		14.0			11.0		ns
Hold Time (t_H)	Full		11.0			8.0		ns
CMOS Noninterleaved Mode—DRVDD = 3.3 V								
Data Propagation Delay (t_{PD})[2]	Full	1.9	4.1	6.4	1.9	4.1	6.4	ns
DCO Propagation Delay (t_{DCO})	Full	4.4	5.8	7.7	4.4	5.8	7.7	ns
Setup Time (t_S)	Full		14.2			11.2		ns
Hold Time (t_H)	Full		10.8			7.8		ns
CMOS Interleaved and IQ Mode—DRVDD = 1.8 V								
Data Propagation Delay (t_{PD})[2]	Full	1.6	3.9	6.2	1.6	3.9	6.2	ns
DCO Propagation Delay (t_{DCO})	Full	3.4	4.8	6.7	3.4	4.8	6.7	ns
Setup Time (t_S)	Full		7.15			5.65		ns
Hold Time (t_H)	Full		5.35			3.85		ns
CMOS Interleaved and IQ Mode—DRVDD = 3.3 V								
Data Propagation Delay (t_{PD})[2]	Full	1.9	4.1	6.4	1.9	4.1	6.4	ns
DCO Propagation Delay (t_{DCO})	Full	3.8	5.2	7.1	3.8	5.2	7.1	ns
Setup Time (t_S)	Full		7.35			5.85		ns
Hold Time (t_H)	Full		5.15			3.65		ns
LVDS Mode—DRVDD = 1.8 V								
Data Propagation Delay (t_{PD})[2]	Full	2.5	4.8	7.0	2.5	4.8	7.0	ns
DCO Propagation Delay (t_{DCO})	Full	3.7	5.3	7.3	3.7	5.3	7.3	ns
Pipeline Delay (Latency) NCO, FIR, $f_S/8$ Mix Disabled	Full		38			38		Cycles
Pipeline Delay (Latency) NCO Enabled, FIR and $f_S/8$ Mix Disabled (Complex Output Mode)	Full		38			38		Cycles
Pipeline Delay (Latency) NCO, FIR, and $f_S/8$ Mix Enabled	Full		109			109		Cycles
Aperture Delay (t_A)	Full		1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1			0.1		ps rms
Wake-Up Time[3]	Full		350			350		us
OUT-OF-RANGE RECOVERY TIME	Full		2			2		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Output propagation delay is measured from CLK 50% transition to DATA 50% transition, with a 5 pF load.
[3] Wake-up time is dependent on the value of the decoupling capacitors.

SWITCHING SPECIFICATIONS—AD6655-125/AD6655-150

Table 8.

Parameter	Temp	AD6655-125 Min	AD6655-125 Typ	AD6655-125 Max	AD6655-150 Min	AD6655-150 Typ	AD6655-150 Max	Unit
CLOCK INPUT PARAMETERS								
Input Clock Rate	Full			625			625	MHz
Conversion Rate[1]								
DCS Enabled	Full	20		125	20		150	MSPS
DCS Disabled	Full	10		125	10		150	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	8			6.66			ns
CLK Pulse Width High (t_{CLKH})								
Divide-by-1 Mode, DCS Enabled	Full	2.4	4	5.6	2.0	3.33	4.66	ns
Divide-by-1 Mode, DCS Disabled	Full	3.6	4	4.4	3.0	3.33	3.66	ns
Divide-by-2 Mode, DCS Enabled	Full	1.6			1.6			ns
Divide-by-3 Through Divide-by-8 Modes, DCS Enabled	Full	0.8			0.8			ns
DATA OUTPUT PARAMETERS (DATA, FD)								
CMOS Noninterleaved Mode—DRVDD = 1.8 V								
Data Propagation Delay (t_{PD})[2]	Full	1.6	3.9	6.2	1.6	3.9	6.2	ns
DCO Propagation Delay (t_{DCO})	Full	4.0	5.4	7.3	4.0	5.4	7.3	ns
Setup Time (t_S)	Full		9.5			8.16		ns
Hold Time (t_H)	Full		6.5			5.16		ns
CMOS Noninterleaved Mode—DRVDD = 3.3 V								
Data Propagation Delay (t_{PD})[2]	Full	1.9	4.1	6.4	1.9	4.1	6.4	ns
DCO Propagation Delay (t_{DCO})	Full	4.4	5.8	7.7	4.4	5.8	7.7	ns
Setup Time (t_S)	Full		9.7			8.36		ns
Hold Time (t_H)	Full		6.3			4.96		ns
CMOS Interleaved and IQ Mode—DRVDD = 1.8 V								
Data Propagation Delay (t_{PD})[2]	Full	1.6	3.9	6.2	1.6	3.9	6.2	ns
DCO Propagation Delay (t_{DCO})	Full	3.4	4.8	6.7	3.4	4.8	6.7	ns
Setup Time (t_S)	Full		4.9			4.23		ns
Hold Time (t_H)	Full		3.1			2.43		ns
CMOS Interleaved and IQ Mode—DRVDD = 3.3 V								
Data Propagation Delay (t_{PD})[2]	Full	1.9	4.1	6.4	1.9	4.1	6.4	ns
DCO Propagation Delay (t_{DCO})	Full	3.8	5.2	7.1	3.8	5.2	7.1	ns
Setup Time (t_S)	Full		5.1			4.43		ns
Hold Time (t_H)	Full		2.9			2.23		ns
LVDS Mode—DRVDD = 1.8 V								
Data Propagation Delay (t_{PD})[2]	Full	2.5	4.8	7.0	2.5	4.8	7.0	ns
DCO Propagation Delay (t_{DCO})	Full	3.7	5.3	7.3	3.7	5.3	7.3	ns
Pipeline Delay (Latency) NCO, FIR, $f_S/8$ Mix Disabled	Full		38			38		Cycles
Pipeline Delay (Latency) NCO Enabled; FIR and $f_S/8$ Mix Disabled (Complex Output Mode)	Full		38			38		Cycles
Pipeline Delay (Latency) NCO, FIR, and $f_S/8$ Mix Enabled	Full		109			109		Cycles
Aperture Delay (t_A)	Full		1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1			0.1		ps rms
Wake-Up Time[3]	Full		350			350		us
OUT-OF-RANGE RECOVERY TIME	Full		3			3		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Output propagation delay is measured from CLK 50% transition to DATA 50% transition, with a 5 pF load.
[3] Wake-up time is dependent on the value of the decoupling capacitors.

TIMING SPECIFICATIONS

Table 9.

Parameter	Conditions	Min	Typ	Max	Unit
SYNC TIMING REQUIREMENTS					
t_{SSYNC}	SYNC to the rising edge of CLK setup time		0.24		ns
t_{HSYNC}	SYNC to the rising edge of CLK hold time		0.4		ns
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK should be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK should be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns
SPORT TIMING REQUIREMENTS					
t_{CSSCLK}	Delay from rising edge of CLK+ to rising edge of SMI SCLK	3.2	4.5	6.2	ns
$t_{SSLKSDO}$	Delay from rising edge of SMI SCLK to SMI SDO	−0.4	0	+0.4	ns
$t_{SSCLKSDFS}$	Delay from rising edge of SMI SCLK to SMI SDFS	−0.4	0	+0.4	ns

Timing Diagrams

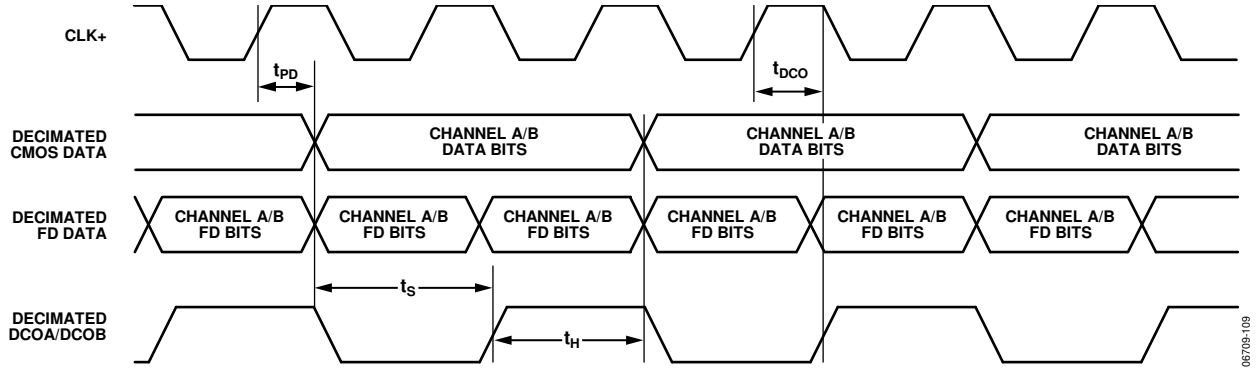


Figure 2. Decimated Noninterleaved CMOS Mode Data and Fast Detect Output Timing (Fast Detect Mode Select Bits = 000)

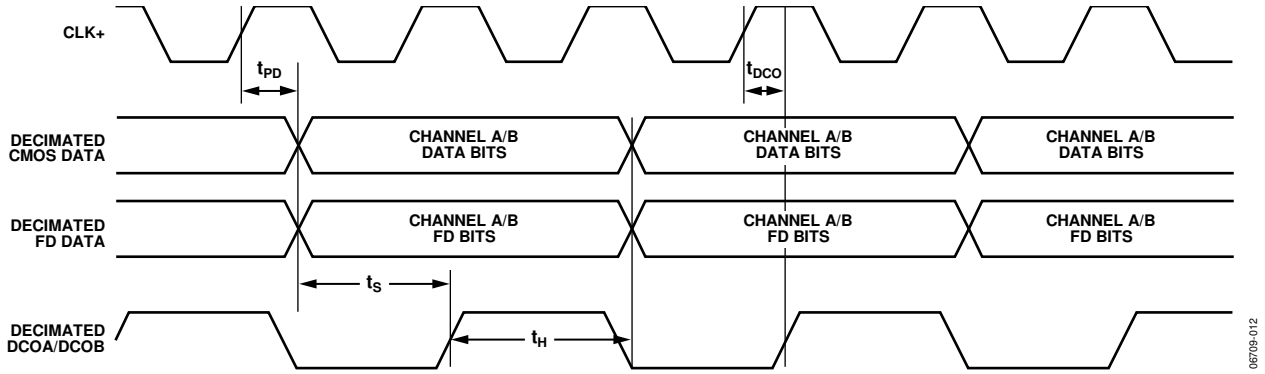


Figure 3. Decimated Noninterleaved CMOS Mode Data and Fast Detect Output Timing (Fast Detect Mode Select Bits = 001 Through Fast Detect Mode Select Bits = 100)

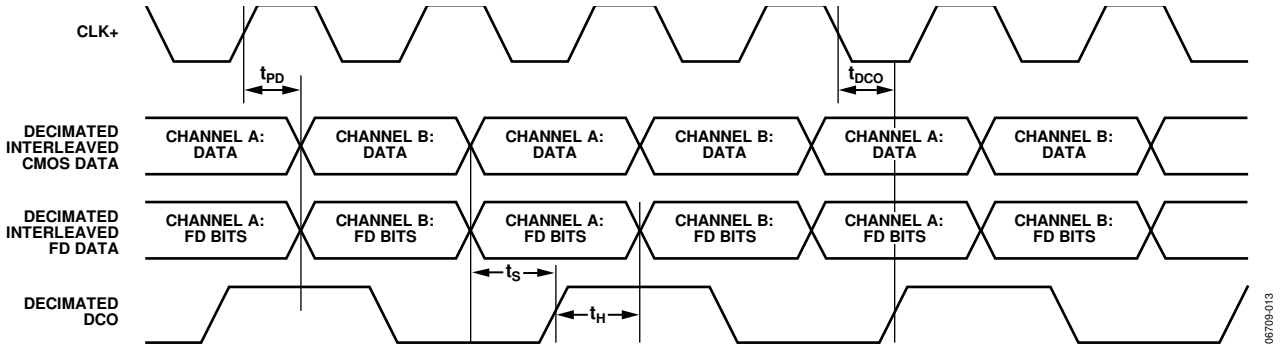


Figure 4. Decimated Interleaved CMOS Mode Data and Fast Detect Output Timing

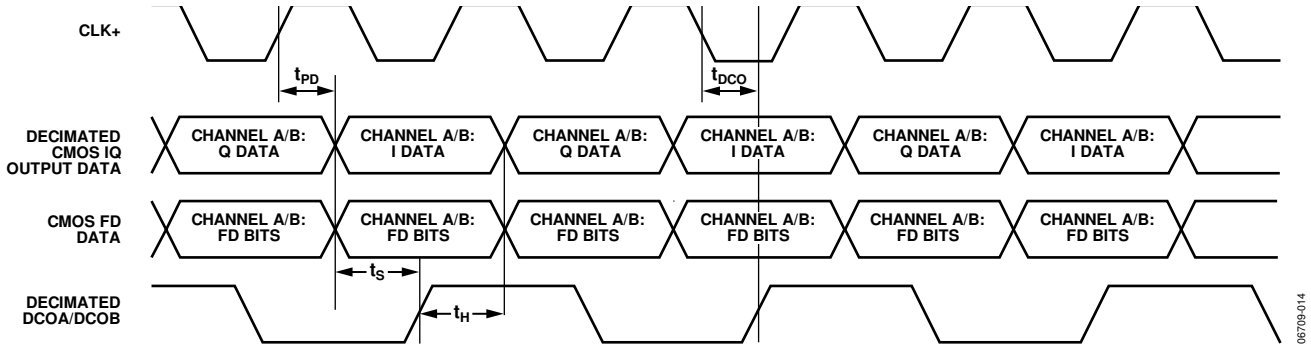


Figure 5. Decimated IQ Mode CMOS Data and Fast Detect Output Timing

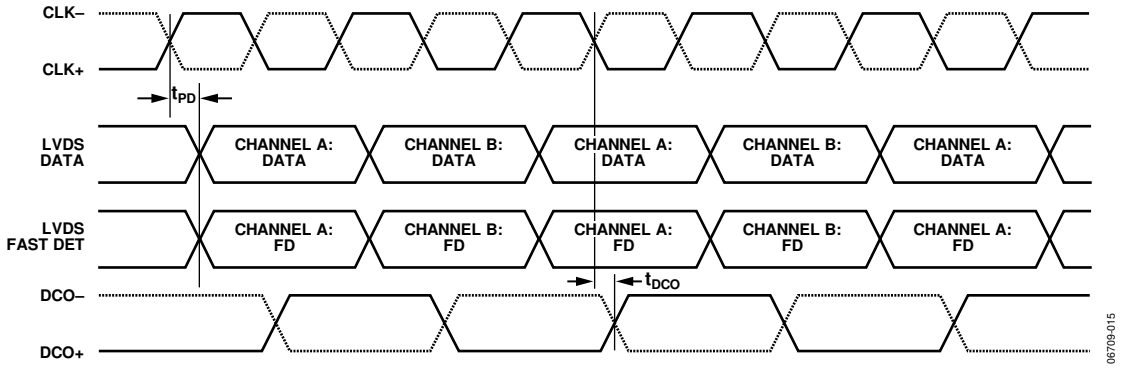


Figure 6. Decimated Interleaved LVDS Mode Data and Fast Detect Output Timing

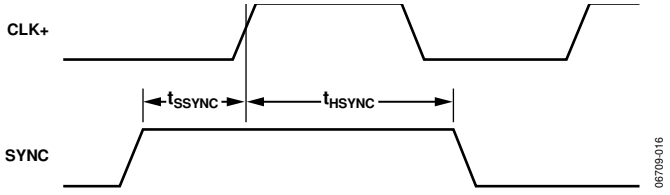


Figure 7. SYNC Timing Inputs

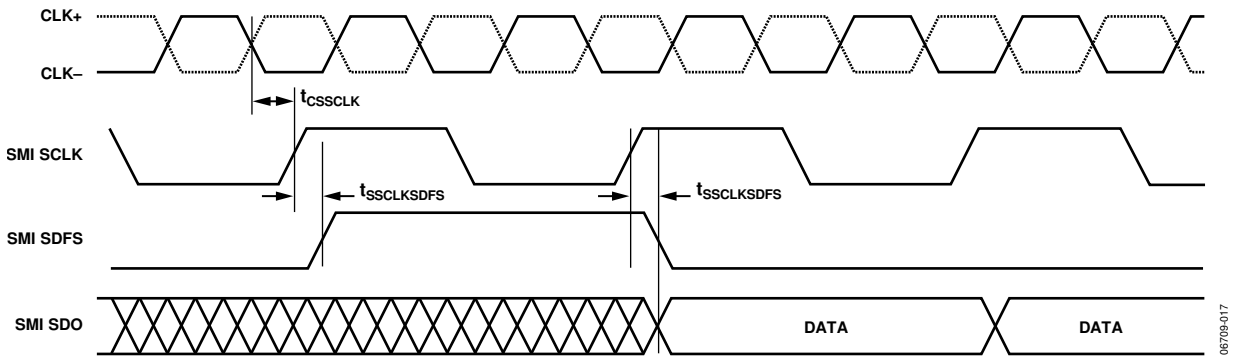


Figure 8. Signal Monitor SPORT Output Timing

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
ELECTRICAL	
AVDD, DVDD to AGND	−0.3 V to +2.0 V
DRVDD to DRGND	−0.3 V to +3.9 V
AGND to DRGND	−0.3 V to +0.3 V
VIN+A/VIN+B, VIN-A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to +3.9 V
SYNC to AGND	−0.3 V to +3.9 V
VREF to AGND	−0.3 V to AVDD + 0.2 V
SENSE to AGND	−0.3 V to AVDD + 0.2 V
CML to AGND	−0.3 V to AVDD + 0.2 V
RBIAS to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to +3.9 V
SCLK/DFS to DRGND	−0.3 V to +3.9 V
SDIO/DCS to DRGND	−0.3 V to DRVDD + 0.3 V
SMI SDO/OEB to DRGND	−0.3 V to DRVDD + 0.3 V
SMI SCLK/PDWN to DRGND	−0.3 V to DRVDD + 0.3 V
SMI SDFS to DRGND	−0.3 V to DRVDD + 0.3 V
D0A/D0B through D13A/D13B to DRGND	−0.3 V to DRVDD + 0.3 V
FD0A/FD0B through FD3A/FD3B to DRGND	−0.3 V to DRVDD + 0.3 V
DCOA/DCOB to DRGND	−0.3 V to DRVDD + 0.3 V
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 11. Thermal Resistance

Package Type	Airflow Velocity (m/s)	θ_{JA}[1,2]	θ_{JC}[1,3]	θ_{JB}[1,4]	Unit
64-Lead LFCSP 9 mm × 9 mm (CP-64-6)	0	18.8	0.6	6.0	°C/W
	1.0	16.5			°C/W
	2.0	15.8			°C/W

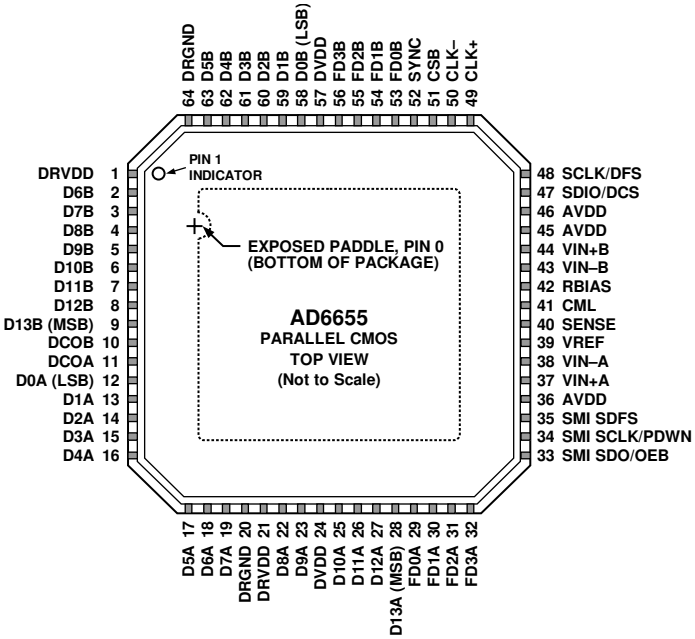
[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with solid ground plane. As shown, airflow increases heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

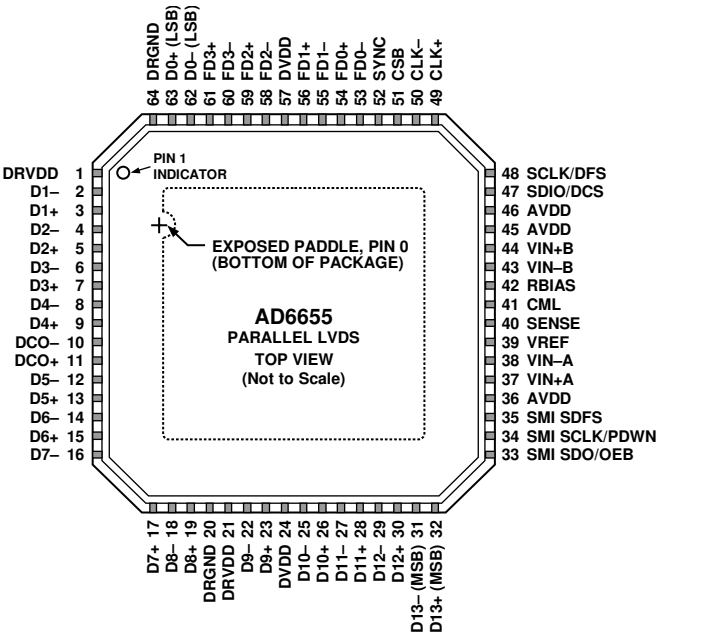
06709-002

Figure 9. LFCSP Parallel CMOS Pin Configuration (Top View)

Table 12. Pin Function Descriptions (Parallel CMOS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
20, 64	DRGND	Ground	Digital Output Ground.
1, 21	DRVDD	Supply	Digital Output Driver Supply (1.8 V to 3.3 V).
24, 57	DVDD	Supply	Digital Power Supply (1.8 V Nominal).
36, 45, 46	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
0	AGND, Exposed Pad	Ground	Analog Ground. The exposed thermal pad on the bottom of the package provides the analog ground for the part. This pad must be connected to ground for proper operation.
ADC Analog			
37	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
38	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
44	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
43	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
39	VREF	Input/Output	Voltage Reference Input/Output.
40	SENSE	Input	Voltage Reference Mode Select. (See Table 15 for details.)
42	RBIAS	Input/Output	External Reference Bias Resistor.
41	CML	Output	Common-Mode Level Bias Output for Analog Inputs.
49	CLK+	Input	ADC Clock Input—True.
50	CLK−	Input	ADC Clock Input—Complement.
ADC Fast Detect Outputs			
29	FD0A	Output	Channel A Fast Detect Indicator. (See Table 21 for details.)
30	FD1A	Output	Channel A Fast Detect Indicator. (See Table 21 for details.)
31	FD2A	Output	Channel A Fast Detect Indicator. (See Table 21 for details.)
32	FD3A	Output	Channel A Fast Detect Indicator. (See Table 21 for details.)
53	FD0B	Output	Channel B Fast Detect Indicator. (See Table 21 for details.)
54	FD1B	Output	Channel B Fast Detect Indicator. (See Table 21 for details.)
55	FD2B	Output	Channel B Fast Detect Indicator. (See Table 21 for details.)
56	FD3B	Output	Channel B Fast Detect Indicator. (See Table 21 for details.)

Pin No.	Mnemonic	Type	Description
Digital Input			
52	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
12	D0A (LSB)	Output	Channel A CMOS Output Data.
13	D1A	Output	Channel A CMOS Output Data.
14	D2A	Output	Channel A CMOS Output Data.
15	D3A	Output	Channel A CMOS Output Data.
16	D4A	Output	Channel A CMOS Output Data.
17	D5A	Output	Channel A CMOS Output Data.
18	D6A	Output	Channel A CMOS Output Data.
19	D7A	Output	Channel A CMOS Output Data.
22	D8A	Output	Channel A CMOS Output Data.
23	D9A	Output	Channel A CMOS Output Data.
25	D10A	Output	Channel A CMOS Output Data.
26	D11A	Output	Channel A CMOS Output Data.
27	D12A	Output	Channel A CMOS Output Data.
28	D13A (MSB)	Output	Channel A CMOS Output Data.
58	D0B (LSB)	Output	Channel B CMOS Output Data.
59	D1B	Output	Channel B CMOS Output Data.
60	D2B	Output	Channel B CMOS Output Data.
61	D3B	Output	Channel B CMOS Output Data.
62	D4B	Output	Channel B CMOS Output Data.
63	D5B	Output	Channel B CMOS Output Data.
2	D6B	Output	Channel B CMOS Output Data.
3	D7B	Output	Channel B CMOS Output Data.
4	D8B	Output	Channel B CMOS Output Data.
5	D9B	Output	Channel B CMOS Output Data.
6	D10B	Output	Channel B CMOS Output Data.
7	D11B	Output	Channel B CMOS Output Data.
8	D12B	Output	Channel B CMOS Output Data.
9	D13B (MSB)	Output	Channel B CMOS Output Data.
11	DCOA	Output	Channel A Data Clock Output.
10	DCOB	Output	Channel B Data Clock Output.
SPI Control			
48	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
47	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
51	CSB	Input	SPI Chip Select. Active low.
Signal Monitor Port			
33	SMI SDO/OEB	Input/Output	Signal Monitor Serial Data Output/Output Enable Input (Active Low) in External Pin Mode.
35	SMI SDFS	Output	Signal Monitor Serial Data Frame Sync.
34	SMI SCLK/PDWN	Input/Output	Signal Monitor Serial Clock Output/Power-Down Input (Active High) in External Pin Mode.



NOTES
1. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

06709-003

Figure 10. LFCSP Interleaved Parallel LVDS Pin Configuration (Top View)

Table 13. Pin Function Descriptions (Interleaved Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
20, 64	DRGND	Ground	Digital Output Ground.
1, 21	DRVDD	Supply	Digital Output Driver Supply (1.8 V to 3.3 V).
24, 57	DVDD	Supply	Digital Power Supply (1.8 V Nominal.)
36, 45, 46	AVDD	Supply	Analog Power Supply (1.8 V Nominal.)
0	AGND, Exposed Pad	Ground	Analog Ground. The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
37	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
38	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
44	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
43	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
39	VREF	Input/Output	Voltage Reference Input/Output.
40	SENSE	Input	Voltage Reference Mode Select. See Table 15 for details.
42	RBIAS	Input/Output	External Reference Bias Resistor.
41	CML	Output	Common-Mode Level Bias Output for Analog Inputs.
49	CLK+	Input	ADC Clock Input—True.
50	CLK−	Input	ADC Clock Input—Complement.
ADC Fast Detect Outputs			
54	FD0+	Output	Channel A/Channel B LVDS Fast Detect Indicator 0—True. See Table 21 for details.
53	FD0-	Output	Channel A/Channel B LVDS Fast Detect Indicator 0—Complement. See Table 21 for details.
56	FD1+	Output	Channel A/Channel B LVDS Fast Detect Indicator 1—True. See Table 21 for details.
55	FD1−	Output	Channel A/Channel B LVDS Fast Detect Indicator 1—Complement. See Table 21 for details.
59	FD2+	Output	Channel A/Channel B LVDS Fast Detect Indicator 2—True See Table 21 for details.
58	FD2−	Output	Channel A/Channel B LVDS Fast Detect Indicator 2—Complement. See Table 21 for details.
61	FD3+	Output	Channel A/Channel B LVDS Fast Detect Indicator 3—True. See Table 21 for details.
60	FD3−	Output	Channel A/Channel B LVDS Fast Detect Indicator 3—Complement. See Table 21 for details.

Pin No.	Mnemonic	Type	Description
Digital Input			
52	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
63	D0+ (LSB)	Output	Channel A/Channel B LVDS Output Data 0—True.
62	D0− (LSB)	Output	Channel A/Channel B LVDS Output Data 0—Complement.
3	D1+	Output	Channel A/Channel B LVDS Output Data 1—True.
2	D1−	Output	Channel A/Channel B LVDS Output Data 1—Complement.
5	D2+	Output	Channel A/Channel B LVDS Output Data 2—True.
4	D2−	Output	Channel A/Channel B LVDS Output Data 2—Complement.
7	D3+	Output	Channel A/Channel B LVDS Output Data 3—True.
6	D3−	Output	Channel A/Channel B LVDS Output Data 3—Complement.
9	D4+	Output	Channel A/Channel B LVDS Output Data 4—True.
8	D4−	Output	Channel A/Channel B LVDS Output Data 4—Complement.
13	D5+	Output	Channel A/Channel B LVDS Output Data 5—True.
12	D5−	Output	Channel A/Channel B LVDS Output Data 5—Complement.
15	D6+	Output	Channel A/Channel B LVDS Output Data 6—True.
14	D6−	Output	Channel A/Channel B LVDS Output Data 6—Complement.
17	D7+	Output	Channel A/Channel B LVDS Output Data 7—True.
16	D7−	Output	Channel A/Channel B LVDS Output Data 7—Complement.
19	D8+	Output	Channel A/Channel B LVDS Output Data 8—True.
18	D8−	Output	Channel A/Channel B LVDS Output Data 8—Complement.
23	D9+	Output	Channel A/Channel B LVDS Output Data 9—True.
22	D9−	Output	Channel A/Channel B LVDS Output Data 9—Complement.
26	D10+	Output	Channel A/Channel B LVDS Output Data 10—True.
25	D10−	Output	Channel A/Channel B LVDS Output Data 10—Complement.
28	D11+	Output	Channel A/Channel B LVDS Output Data 11—True.
27	D11−	Output	Channel A/Channel B LVDS Output Data 11—Complement.
30	D12+	Output	Channel A/Channel B LVDS Output Data 12—True.
29	D12−	Output	Channel A/Channel B LVDS Output Data 12—Complement.
32	D13+ (MSB)	Output	Channel A/Channel B LVDS Output Data 13—True.
31	D13− (MSB)	Output	Channel A/Channel B LVDS Output Data 13—Complement.
11	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
10	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
48	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
47	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer in External Pin Mode.
51	CSB	Input	SPI Chip Select (Active Low).
Signal Monitor Port			
33	SMI SDO/OEB	Input/Output	Signal Monitor Serial Data Output/Output Enable Input (Active Low) in External Pin Mode.
35	SMI SDFS	Output	Signal Monitor Serial Data Frame Sync.
34	SMI SCLK/PDWN	Input/Output	Signal Monitor Serial Clock Output/Power-Down Input (Active High) in External Pin Mode.

EQUIVALENT CIRCUITS

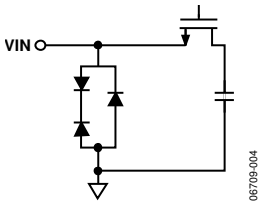


Figure 11. Equivalent Analog Input Circuit

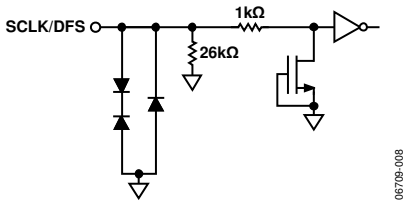


Figure 15. Equivalent SCLK/DFS Input Circuit

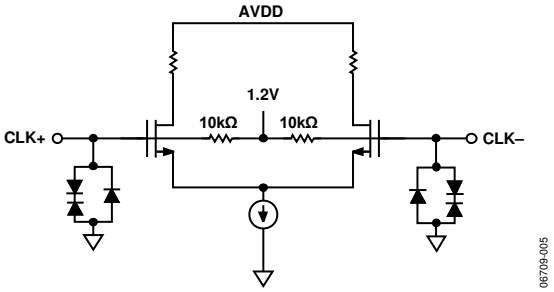


Figure 12. Equivalent Clock Input Circuit

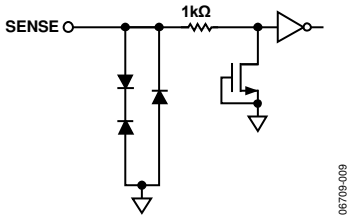


Figure 16. Equivalent SENSE Circuit

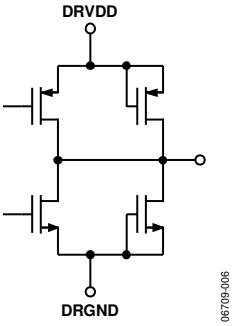


Figure 13. Equivalent Digital Output Circuit

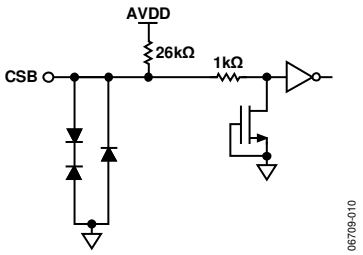


Figure 17. Equivalent CSB Input Circuit

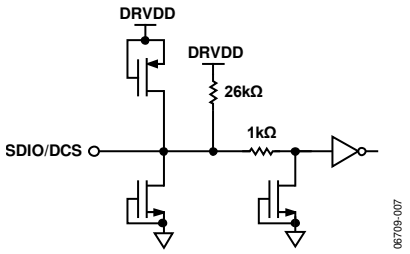


Figure 14. Equivalent SDIO/DCS Circuit or SMI SDFS Circuit

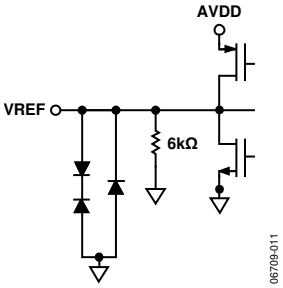


Figure 18. Equivalent VREF Circuit

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TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 1.8 V, sample rate = 150 MSPS, DCS enabled, 1.0 V internal reference, 2 V p-p differential input, VIN = −1.0 dBFS, 64k sample, T_A = 25°C, NCO enabled, FIR filter enabled, unless otherwise noted. In the FFT plots that follow, the location of the second and third harmonics is noted when they fall in the pass band of the filter.

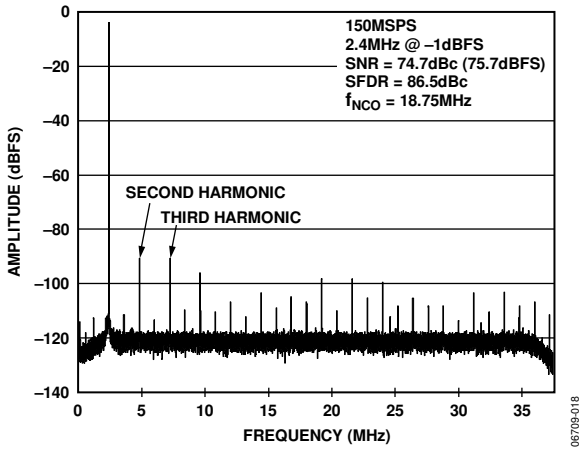

Figure 19. AD6655-150 Single-Tone FFT with f_{IN} = 2.4 MHz, f_{NCO} = 18.75 MHz

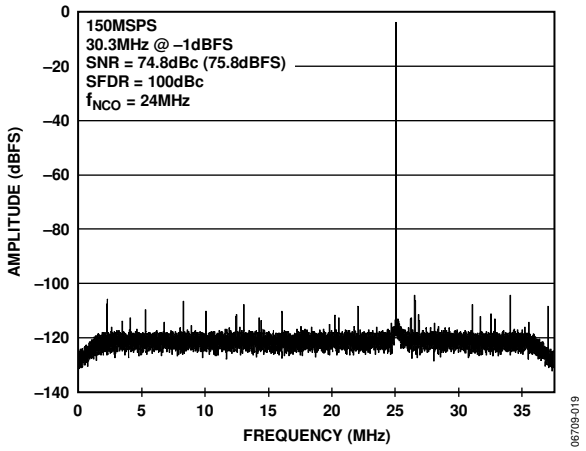

Figure 20. AD6655-150 Single-Tone FFT with f_{IN} = 30.3 MHz, f_{NCO} = 24 MHz

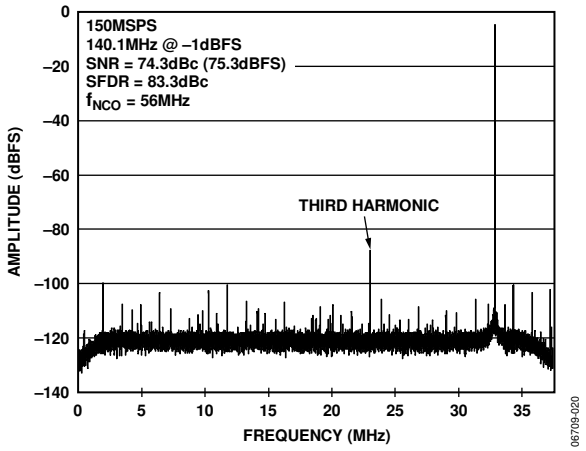

Figure 21. AD6655-150 Single-Tone FFT with f_{IN} = 70.1 MHz, f_{NCO} = 56 MHz

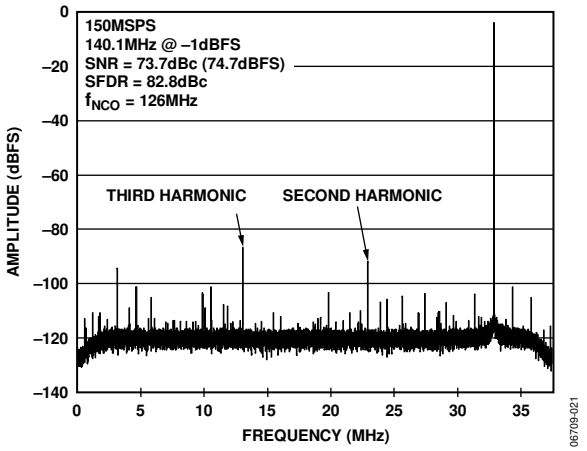

Figure 22. AD6655-150 Single-Tone FFT with f_{IN} = 140.1 MHz, f_{NCO} = 126 MHz

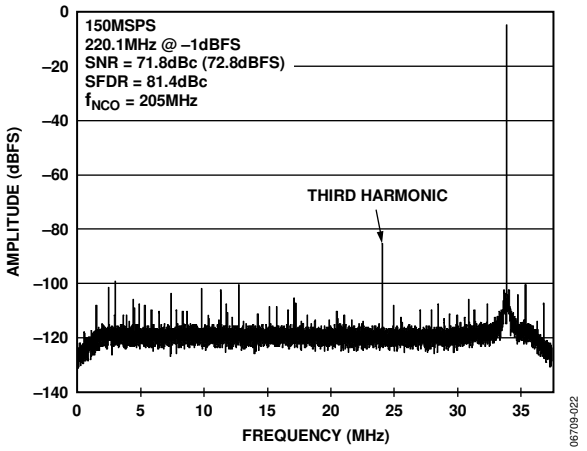

Figure 23. AD6655-150 Single-Tone FFT with f_{IN} = 220.1 MHz, f_{NCO} = 205 MHz

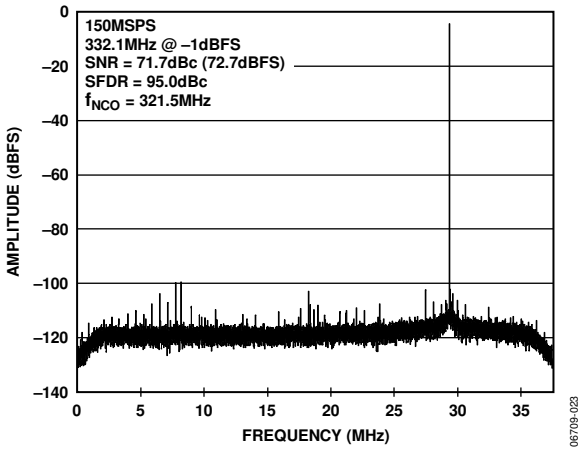

Figure 24. AD6655-150 Single-Tone FFT with f_{IN} = 332.1 MHz, f_{NCO} = 321.5 MHz