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Quad IF Receiver

Data Sheet

AD6657A

FEATURES

- 11-bit, 200 MSPS output data rate per channel
- Integrated noise shaping requantizer
- Performance with NSR enabled
  - SNR: 76.0 dBFS in 40 MHz band to 70 MHz at 185 MSPS
  - SNR: 73.6 dBFS in 60 MHz band to 70 MHz at 185 MSPS
  - SNR: 72.8 dBFS in 65 MHz band to 70 MHz at 185 MSPS
- Performance with NSR disabled
  - SNR: 66.5 dBFS to 70 MHz at 185 MSPS
  - SFDR: 88 dBc to 70 MHz at 185 MSPS
- Low power: 1.2 W at 185 MSPS
- 1.8 V analog supply operation
- 1.8 V LVDS (ANSI-644 levels) output
- 1-to-8 integer clock divider
- Internal ADC voltage reference
- 1.75 V p-p analog input range (programmable to 2.0 V p-p)
- Differential analog inputs with 800 MHz bandwidth
- 95 dB channel isolation/crosstalk
- Serial port control
- User-configurable built-in self test (BIST) capability
- Energy saving power-down modes

APPLICATIONS

- Communications
- Diversity radio and smart antenna (MIMO) systems
- Multimode digital receivers (3G)
  - WCDMA, LTE, CDMA2000
  - WiMAX, TD-SCDMA
- I/Q demodulation systems
- General-purpose software radios

FUNCTIONAL BLOCK DIAGRAM

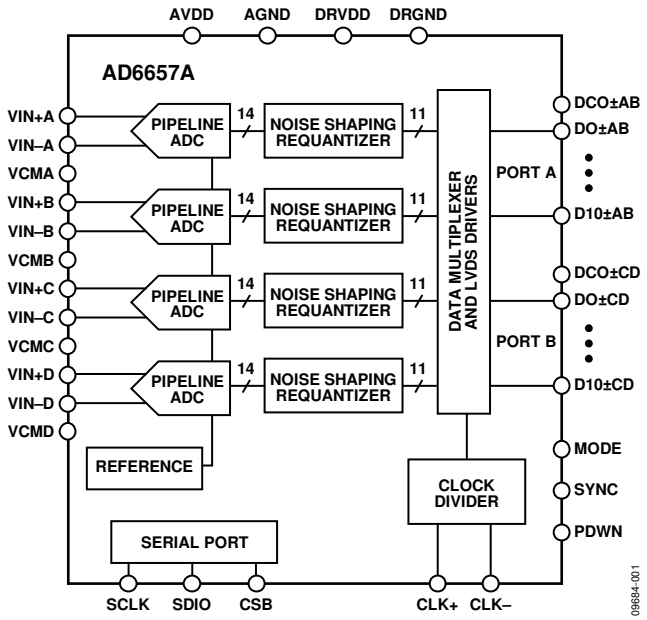

Figure 1.

GENERAL DESCRIPTION

The AD6657A is an 11-bit, 200 MSPS, quad channel intermediate frequency (IF) receiver specifically designed to support multiple antenna systems in telecommunication applications where high dynamic range performance, low power, and small size are desired.

The device consists of four high performance ADCs and NSR digital blocks. Each ADC consists of a multistage, differential pipelined architecture with integrated output error correction logic. The ADC features a wide bandwidth switched capacitor sampling network within the first stage of the differential pipeline. An integrated voltage reference eases design considerations. A duty cycle stabilizer (DCS) compensates for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

Each ADC output is connected internally to an NSR block. The integrated NSR circuitry allows for improved SNR performance in a smaller frequency band within the Nyquist bandwidth. The device supports two different output modes selectable via the external MODE pin or the serial port interface (SPI).

With the NSR feature enabled, the outputs of the ADCs are processed such that the AD6657A supports enhanced SNR performance within a limited portion of the Nyquist bandwidth while maintaining an 11-bit output resolution. The NSR block can be programmed to provide a bandwidth of either 22%, 33%, or 36% of the sample clock. For example, with a sample clock rate of 185 MSPS, the AD6657A can achieve up to 76.0 dBFS SNR for a 40 MHz bandwidth in the 22% mode, up to 73.6 dBFS SNR for a 60 MHz bandwidth in the 33% mode, or up to 72.8 dBFS SNR for a 65 MHz bandwidth in the 36% mode.

(General Description continued on Page 3)

Rev. A
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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AD6657A* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD6657A Evaluation Board

DOCUMENTATION

Application Notes

- AN-282: Fundamentals of Sampled Data Systems
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-737: How ADIsimADC Models an ADC
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD6657A: Quad IF Receiver Data Sheet

User Guides

- UG-232: Evaluating the AD6642/AD6657 Analog-to-Digital Converters

TOOLS AND SIMULATIONS

- Visual Analog
- AD6657A IBIS Model

REFERENCE DESIGNS

- CN0259

DESIGN RESOURCES

- AD6657A Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD6657A EngineerZone Discussions.

SAMPLE AND BUY

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TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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TABLE OF CONTENTS

REVISION HISTORY

2/14—Rev. 0 to Rev. A

Changed DCO to Data Skew (t_{SKEW}) Parameter Unit from ns to ps, Table 4 ... 9

10/11—Revision 0: Initial Version

With the NSR block disabled, the ADC data is provided directly to the output with a resolution of 11 bits. The AD6657A can achieve up to 66.5 dBFS SNR for the entire Nyquist bandwidth when operated in this mode. This allows the AD6657A to be used in telecommunication applications such as a digital predistortion observation path where wider bandwidths are used.

After digital signal processing, multiplexed output data is routed into two 11-bit output ports such that the maximum digital data rate (DDR) is 400 Mbps. These outputs are set at 1.8 V LVDS and support ANSI-644 levels.

The AD6657A receiver digitizes a wide spectrum of IF frequencies. Each receiver is designed for simultaneous reception of a separate antenna. This IF sampling architecture greatly reduces component cost and complexity compared with traditional analog techniques or less integrated digital methods.

Flexible power-down options allow significant power savings. Programming for device setup and control is accomplished using a 3-wire SPI-compatible serial interface with numerous modes to support board level system testing.

The AD6657A is available in a Pb-free, RoHS compliant, 144-ball, 10 mm × 10 mm chip scale package ball grid array (CSP_BGA) that is specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Four analog-to-digital converters (ADCs) are contained in a small, space-saving, 10 mm × 10 mm × 1.4 mm, 144-ball CSP_BGA package.
2. Pin selectable noise shaping requantizer (NSR) function that allows for improved SNR within a reduced bandwidth of up to 65 MHz at 185 MSPS.
3. LVDS digital output interface configured for low cost FPGA families.
4. 230 mW per ADC core power consumption.
5. Operation from a single 1.8 V supply.
6. Standard SPI that supports various product features and functions, such as data formatting (offset binary or twos complement), NSR, power-down, test modes, and voltage reference mode.
7. On-chip integer 1-to-8 input clock divider and multichip sync function to support a wide range of clocking schemes and multichannel subsystems.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, f_S = 185 MSPS, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, and default SPI, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	Full	11			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−0.9	+0.1	+0.9	mV
Gain Error	Full	+4	+11	+18	% FSR
Differential Nonlinearity (DNL)[1]	Full	−0.4	±0.1	+0.4	LSB
Integral Nonlinearity (INL)[1]	Full	−0.55	±0.17	+0.55	LSB
MATCHING CHARACTERISTIC					
Offset Error	Full	−5	+3	+11	mV
Gain Error	Full	0	+2.1	+8	% FSR
TEMPERATURE DRIFT					
Offset Error	Full		2		ppm/°C
Gain Error	Full		40		ppm/°C
ANALOG INPUT					
Input Range	Full	1.4	1.75	2.0	V p-p
Input Common-Mode Voltage	Full		0.95		V
Input Resistance (Differential)	Full		20		kΩ
Input Capacitance[2]	Full		5		pF
POWER SUPPLIES					
Supply Voltage					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
Supply Current					
I_{AVDD}[1]	Full		466	510	mA
I_{DRVDD}[1] (1.8 V LVDS)	Full		170	183	mA
POWER CONSUMPTION					
Sine Wave Input[1]	Full		1145	1247	mW
Standby Power[3]	Full		129		mW
Power-Down Power	Full		3.8	10	mW

[1] Measured with a 10 MHz, 0 dBFS sine wave, with 100 Ω termination on each LVDS output pair.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND.
[3] Standby power is measured with a dc input and the CLKx pins inactive (set to AVDD or AGND).

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, f_S = 185 MSPS, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, and default SPI, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE-RATIO (SNR)—NSR DISABLED					
f_{IN} = 10 MHz	25°C		66.6		dBFS
f_{IN} = 50 MHz	25°C		66.5		dBFS
f_{IN} = 70 MHz	25°C		66.5		dBFS
f_{IN} = 170 MHz	25°C		66.3		dBFS
	Full	65.6			dBFS
f_{IN} = 250 MHz	25°C		65.9		dBFS
SIGNAL-TO-NOISE-RATIO (SNR)—NSR ENABLED					
22% BW Mode					
f_{IN} = 10 MHz	25°C		76.0		dBFS
f_{IN} = 50 MHz	25°C		75.7		dBFS
f_{IN} = 70 MHz	25°C		75.7		dBFS
f_{IN} = 170 MHz	25°C		74.3		dBFS
	Full	72.9			dBFS
f_{IN} = 250 MHz	25°C		72.8		dBFS
33% BW Mode					
f_{IN} = 10 MHz	25°C		73.6		dBFS
f_{IN} = 50 MHz	25°C		73.6		dBFS
f_{IN} = 70 MHz	25°C		73.3		dBFS
f_{IN} = 170 MHz	25°C		72.5		dBFS
	Full	71.3			dBFS
f_{IN} = 230 MHz	25°C		71.2		dBFS
36% BW Mode					
f_{IN} = 10 MHz	25°C		72.8		dBFS
f_{IN} = 50 MHz	25°C		72.6		dBFS
f_{IN} = 70 MHz	25°C		72.6		dBFS
f_{IN} = 170 MHz	25°C		71.8		dBFS
	Full	70.7			dBFS
f_{IN} = 250 MHz	25°C		70.8		dBFS
SIGNAL-TO-NOISE-AND DISTORTION (SINAD)					
f_{IN} = 10 MHz	25°C		65.5		dBFS
f_{IN} = 50 MHz	25°C		65.5		dBFS
f_{IN} = 70 MHz	25°C		65.5		dBFS
f_{IN} = 170 MHz	25°C		65.3		dBFS
	Full	64.6			dBFS
f_{IN} = 250 MHz	25°C		64.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 10 MHz	25°C		10.6		Bits
f_{IN} = 50 MHz	25°C		10.6		Bits
f_{IN} = 70 MHz	25°C		10.6		Bits
f_{IN} = 170 MHz	25°C		10.6		Bits
f_{IN} = 250 MHz	25°C		10.5		Bits

Parameter[1]	Temperature	Min	Typ	Max	Unit
WORST SECOND OR THIRD HARMONIC					
f_{IN} = 10 MHz	25°C		−94		dBc
f_{IN} = 50 MHz	25°C		−91		dBc
f_{IN} = 70 MHz	25°C		−88		dBc
f_{IN} = 170 MHz	25°C		−90		dBc
	Full			−80	dBc
f_{IN} = 250 MHz	25°C		−83		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 10 MHz	25°C		94		dBc
f_{IN} = 50 MHz	25°C		91		dBc
f_{IN} = 70 MHz	25°C		88		dBc
f_{IN} = 170 MHz	25°C		90		dBc
	Full	80			dBc
f_{IN} = 250 MHz	25°C		83		dBc
WORST OTHER HARMONIC (FOURTH THROUGH EIGHTH)					
f_{IN} = 10 MHz	25°C		−94		dBc
f_{IN} = 50 MHz	25°C		−95		dBc
f_{IN} = 70 MHz	25°C		−94		dBc
f_{IN} = 170 MHz	25°C		−94		dBc
	Full			−80	dBc
f_{IN} = 250 MHz	25°C		−90		dBc
TWO TONE SFDR (−7 dBFS)					
f_{IN1} = 169 MHz, f_{IN2} = 172 MHz	25°C		89		dBc
CROSSTALK[2]	Full		95		dB
ANALOG INPUT BANDWIDTH	25°C		800		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 155 MHz with −1 dBFS on one channel and no input on the alternate channel.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, f_S = 185 MSPS, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, and default SPI, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.2		3.6	V p-p
Input Voltage Range	Full	AGND − 0.3		AVDD + 0.2	V
High Level Input Voltage	Full	1.2		2.0	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full	8	10	12	kΩ
Input Capacitance	Full		4		pF
SYNC INPUT					
Logic Compliance			CMOS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
High Level Input Voltage	Full	1.2		AVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Resistance	Full	12	16	20	kΩ
Input Capacitance	Full		1		pF
LOGIC INPUT (CSB)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		132	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−92		−135	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT/OUTPUT (SDIO)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	38		128	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF

Parameter	Temperature	Min	Typ	Max	Unit
LOGIC INPUT (MODE)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		132	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (PDWN)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−90		−134	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS (LVDS)					
Differential Output Voltage (V_{OD})	Full	247		454	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	V

[1] Pull up.
[2] Pull down.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, f_S = 185 MSPS, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, and default SPI, unless otherwise noted.

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS					
Input Clock Rate	Full			625	MHz
Conversion Rate[1]	Full	40	185	200	MSPS
CLK Pulse Width High (t_{CH})[2]	Full		2.7		ns
Aperture Delay (t_A)[2]	Full		1.3		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.13		ps rms
DATA OUTPUT PARAMETERS					
Data Propagation Delay (t_{PD})[2]	Full	3.0	4.0	4.9	ns
DCO Propagation Delay (t_{DCO})[2]	Full	3.1	4.0	4.9	ns
DCO to Data Skew (t_{SKEW})[2]	Full	−41	+6.1	+33	ps
Pipeline Delay (Latency)	Full		9		Cycles
With NSR Enabled	Full		12		Cycles
Wake-Up Time (from Standby)[3]	Full		0.5		µs
Wake-Up Time (from Power Down)[3]	Full		310		µs
OUT-OF-RANGE RECOVERY TIME	Full		2		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] See Figure 2 for details.
[3] Wake-up time is dependent on the value of the decoupling capacitors.

Data Output Timing Diagram

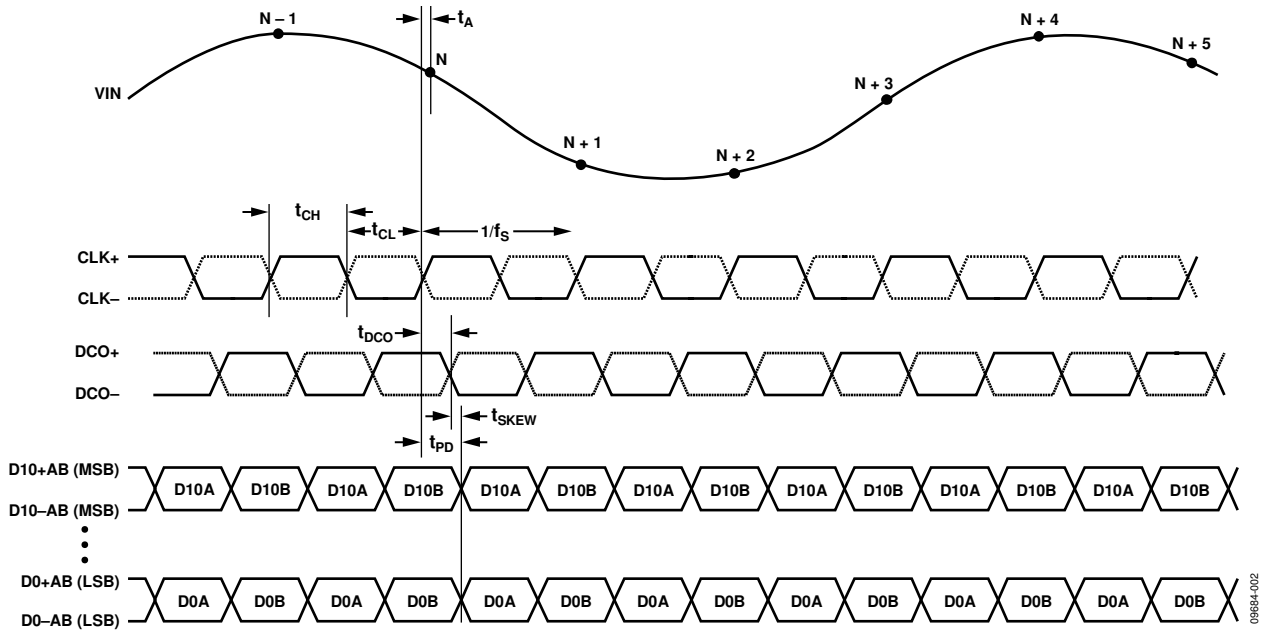

Figure 2. Data Output Timing (Timing for Channel C and Channel D Is Identical to Timing for Channel A and Channel B)

TIMING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, f_S = 185 MSPS, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, and default SPI, unless otherwise noted.

Table 5.

Parameter	Description	Min	Typ	Max	Unit
SYNC TIMING REQUIREMENTS	See Figure 3 for details				
t_{SSYNC}	SYNC to rising edge of CLK setup time		0.24		ns
t_{HSYNC}	SYNC to rising edge of CLK hold time		0.40		ns
SPI TIMING REQUIREMENTS	See Figure 60 for details, except where noted				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	SCLK pulse width high	10			ns
t_{LOW}	SCLK pulse width low	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not pictured in Figure 60)	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not pictured in Figure 60)	10			ns

Sync Input Timing Diagram

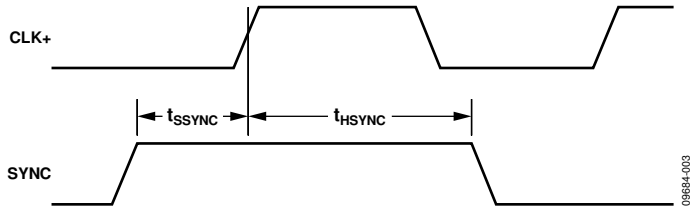

Figure 3. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
VIN+x, VIN−x to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to AGND	−0.3 V to AVDD + 0.2 V
VCMx to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.2 V
SCLK to AGND	−0.3 V to DRVDD + 0.2 V
SDIO to AGND	−0.3 V to DRVDD + 0.2 V
PDWN to AGND	−0.3 V to DRVDD + 0.2 V
MODE to AGND	−0.3 V to DRVDD + 0.2 V
Digital Outputs to AGND	−0.3 V to DRVDD + 0.2 V
DCO+AB, DCO−AB, DCO+CD, DCO−CD to AGND	−0.3 V to DRVDD + 0.2 V
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The values in Table 7 are per JEDEC JESD51-7 and JEDEC JESD25-5 for a 2S2P test board. Typical θ_{JA} is specified for a 4-layer printed circuit board (PCB) with a solid ground plane. As shown in Table 7, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Table 7.

Package Type	Airflow Velocity	θ_{JA}[1]	θ_{JC}[2]	θ_{JB}[3]	Unit
144-Ball CSP_BGA	0 m/s	26.9	8.9	6.6	°C/W
	1 m/s	24.2			°C/W
	2.5 m/s	23.0			°C/W

[1] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[2] Per MIL-STD 883, Method 1012.1.
[3] Per JEDEC JESD51-8 (still air).

The values in Table 8 are from simulations. The PCB is a JEDEC multilayer board. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine whether they are similar to those assumed in these calculations.

Table 8.

Package Type	Airflow Velocity	Ψ_{JB}	Ψ_{JT}	Unit
144-Ball CSP_BGA	0 m/s	14.4	0.23	°C/W
	1 m/s	14.0	0.50	°C/W
	2.5 m/s	13.9	0.53	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12
A	AGND	VIN+C	VIN–C	AGND	AVDD	CLK–	CLK+	AVDD	AGND	VIN–B	VIN+B	AGND
B	AGND	AGND	VCMC	AGND	AVDD	AVDD	AVDD	AVDD	AGND	VCMB	AGND	AGND
C	VIN+D	AGND	AGND	CSB	SDIO	SCLK	PDWN	SYNC	MODE	AGND	AGND	VIN+A
D	VIN–D	VCMD	AGND	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AGND	VCMA	VIN–A
E	AGND	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AGND
F	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND
G	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND
H	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD	DRVDD
J	D0–CD	D2–CD	D4–CD	D6–CD	D8–CD	D10–CD	D0–AB	D2–AB	D4–AB	D6–AB	D8–AB	D10–AB
K	D0+CD	D2+CD	D4+CD	D6+CD	D8+CD	D10+CD	D0+AB	D2+AB	D4+AB	D6+AB	D8+AB	D10+AB
L	D1–CD	D3–CD	D5–CD	D7–CD	D9–CD	DCO–CD	D1–AB	D3–AB	D5–AB	D7–AB	D9–AB	DCO–AB
M	D1+CD	D3+CD	D5+CD	D7+CD	D9+CD	DCO+CD	D1+AB	D3+AB	D5+AB	D7+AB	D9+AB	DCO+AB

09684-004

Figure 4. Pin Configuration (Top View)

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A5, A8, B5 to B8, D4 to D9, E2 to E11	AVDD	Supply	Analog Power Supply. 1.8 V nominal.
A1, A4, A9, A12, B1, B2, B4, B9, B11, B12, C2, C3, C10, C11, D3, D10, E1, E12, F1 to F12	AGND	Ground	Analog Ground.
H1 to H12	DRVDD	Supply	Digital Output Driver Supply. 1.8 V nominal.
G1 to G12	DRGND	Ground	Digital Output Driver Ground.
A7	CLK+	Input	ADC Clock Input—True.
A6	CLK–	Input	ADC Clock Input—Complement.
C12	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
D12	VIN–A	Input	Differential Analog Input Pin (–) for Channel A.
D11	VCMA	Output	Common-Mode Level Bias Output for Analog Input Channel A.
A11	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
A10	VIN–B	Input	Differential Analog Input Pin (–) for Channel B.
B10	VCMB	Output	Common-Mode Level Bias Output for Analog Input Channel B.
A2	VIN+C	Input	Differential Analog Input Pin (+) for Channel C.
A3	VIN–C	Input	Differential Analog Input Pin (–) for Channel C.
B3	VCMC	Output	Common-Mode Level Bias Output for Analog Input Channel C.
C1	VIN+D	Input	Differential Analog Input Pin (+) for Channel D.
D1	VIN–D	Input	Differential Analog Input Pin (–) for Channel D.
D2	VCMD	Output	Common-Mode Level Bias Output for Analog Input Channel D.
K7	D0+AB	Output	Channel A and Channel B LVDS Output Data 0—True.
J7	D0–AB	Output	Channel A and Channel B LVDS Output Data 0—Complement.
M7	D1+AB	Output	Channel A and Channel B LVDS Output Data 1—True.
L7	D1–AB	Output	Channel A and Channel B LVDS Output Data 1—Complement.
K8	D2+AB	Output	Channel A and Channel B LVDS Output Data 2—True.
J8	D2–AB	Output	Channel A and Channel B LVDS Output Data 2—Complement.
M8	D3+AB	Output	Channel A and Channel B LVDS Output Data 3—True.
L8	D3–AB	Output	Channel A and Channel B LVDS Output Data 3—Complement.
K9	D4+AB	Output	Channel A and Channel B LVDS Output Data 4—True.
J9	D4–AB	Output	Channel A and Channel B LVDS Output Data 4—Complement.

Pin No.	Mnemonic	Type	Description
M9	D5+AB	Output	Channel A and Channel B LVDS Output Data 5—True.
L9	D5−AB	Output	Channel A and Channel B LVDS Output Data 5—Complement.
K10	D6+AB	Output	Channel A and Channel B LVDS Output Data 6—True.
J10	D6−AB	Output	Channel A and Channel B LVDS Output Data 6—Complement.
M10	D7+AB	Output	Channel A and Channel B LVDS Output Data 7—True.
L10	D7−AB	Output	Channel A and Channel B LVDS Output Data 7—Complement.
K11	D8+AB	Output	Channel A and Channel B LVDS Output Data 8—True.
J11	D8−AB	Output	Channel A and Channel B LVDS Output Data 8—Complement.
M11	D9+AB	Output	Channel A and Channel B LVDS Output Data 9—True.
L11	D9−AB	Output	Channel A and Channel B LVDS Output Data 9—Complement.
K12	D10+AB	Output	Channel A and Channel B LVDS Output Data 10—True.
J12	D10−AB	Output	Channel A and Channel B LVDS Output Data 10—Complement.
M12	DCO+AB	Output	Data Clock LVDS Output for Channel A and Channel B—True.
L12	DCO−AB	Output	Data Clock LVDS Output for Channel A and Channel B—Complement.
K1	D0+CD	Output	Channel C and Channel D LVDS Output Data 0—True.
J1	D0−CD	Output	Channel C and Channel D LVDS Output Data 0—Complement.
M1	D1+CD	Output	Channel C and Channel D LVDS Output Data 1—True.
L1	D1−CD	Output	Channel C and Channel D LVDS Output Data 1—Complement.
K2	D2+CD	Output	Channel C and Channel D LVDS Output Data 2—True.
J2	D2−CD	Output	Channel C and Channel D LVDS Output Data 2—Complement.
M2	D3+CD	Output	Channel C and Channel D LVDS Output Data 3—True.
L2	D3−CD	Output	Channel C and Channel D LVDS Output Data 3—Complement.
K3	D4+CD	Output	Channel C and Channel D LVDS Output Data 4—True.
J3	D4−CD	Output	Channel C and Channel D LVDS Output Data 4—Complement.
M3	D5+CD	Output	Channel C and Channel D LVDS Output Data 5—True.
L3	D5−CD	Output	Channel C and Channel D LVDS Output Data 5—Complement.
K4	D6+CD	Output	Channel C and Channel D LVDS Output Data 6—True.
J4	D6−CD	Output	Channel C and Channel D LVDS Output Data 6—Complement.
M4	D7+CD	Output	Channel C and Channel D LVDS Output Data 7—True.
L4	D7−CD	Output	Channel C and Channel D LVDS Output Data 7—Complement.
K5	D8+CD	Output	Channel C and Channel D LVDS Output Data 8—True.
J5	D8−CD	Output	Channel C and Channel D LVDS Output Data 8—Complement.
M5	D9+CD	Output	Channel C and Channel D LVDS Output Data 9—True.
L5	D9−CD	Output	Channel C and Channel D LVDS Output Data 9—Complement.
K6	D10+CD	Output	Channel C and Channel D LVDS Output Data 10—True.
J6	D10−CD	Output	Channel C and Channel D LVDS Output Data 10—Complement.
M6	DCO+CD	Output	Data Clock LVDS Output for Channel C and Channel D—True.
L6	DCO−CD	Output	Data Clock LVDS Output for Channel C and Channel D—Complement.
C9	MODE	Input	Mode Select Pin. Logic low enables NSR; logic high disables NSR.
C8	SYNC	Input	Digital Synchronization Pin.
C7	PDWN	Input	Power-Down Input (Active High).
C6	SCLK	Input	SPI Clock.
C5	SDIO	Input/Output	SPI Data.
C4	CSB	Input	SPI Chip Select (Active Low).

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, sample rate = 185 MSPS, 1.75 V p-p differential input, VIN = −1.0 dBFS, 32,000 sample, T_A = 25°C, unless otherwise noted.

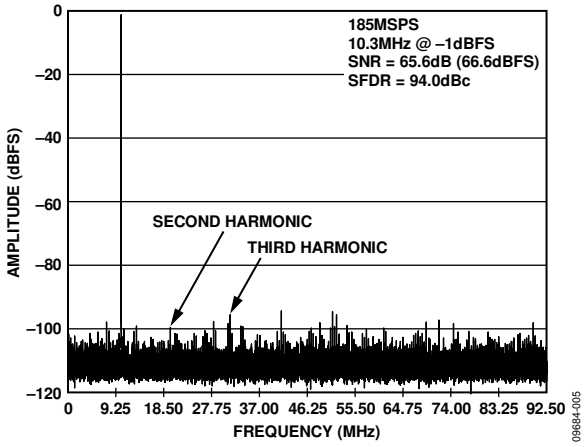

Figure 5. Single Tone FFT, f_{IN} = 10.3 MHz

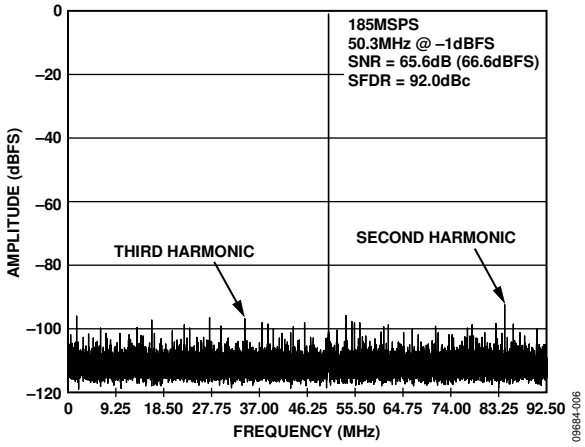

Figure 6. Single Tone FFT, f_{IN} = 50.3 MHz

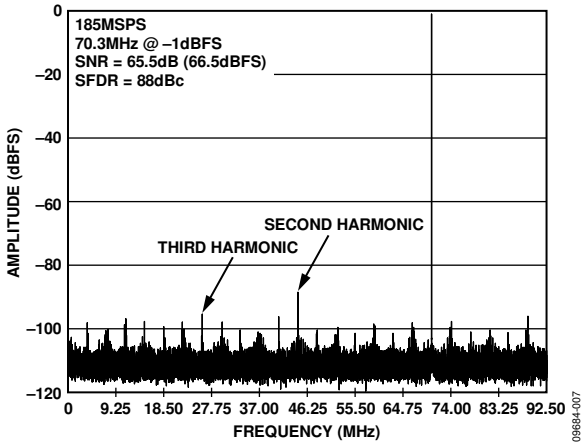

Figure 7. Single Tone FFT, f_{IN} = 70.3 MHz

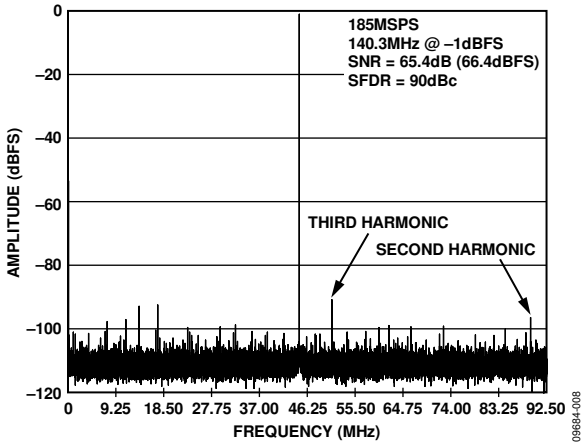

Figure 8. Single Tone FFT, f_{IN} = 140.3 MHz

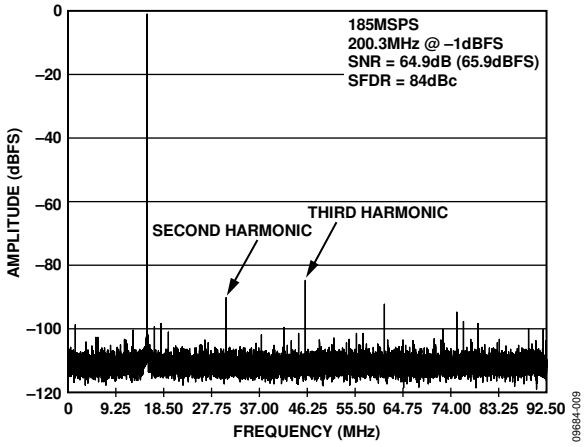

Figure 9. Single Tone FFT, f_{IN} = 200.3 MHz

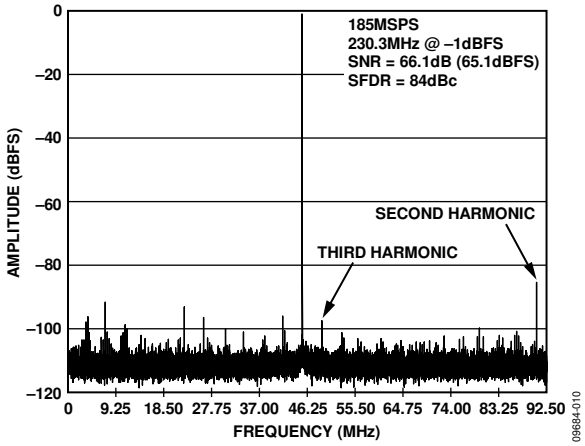

Figure 10. Single Tone FFT, f_{IN} = 230.3 MHz

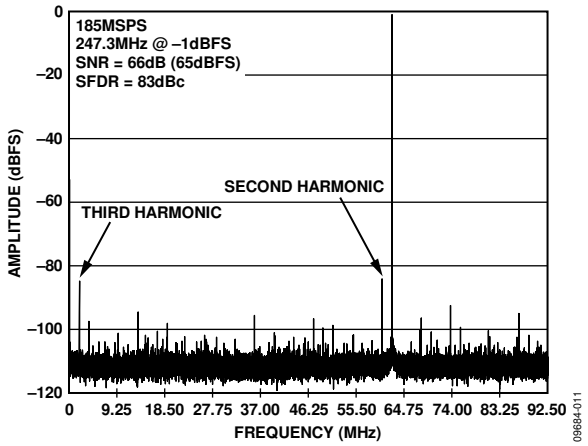

Figure 11. Single Tone FFT, f_{IN} = 247.3 MHz

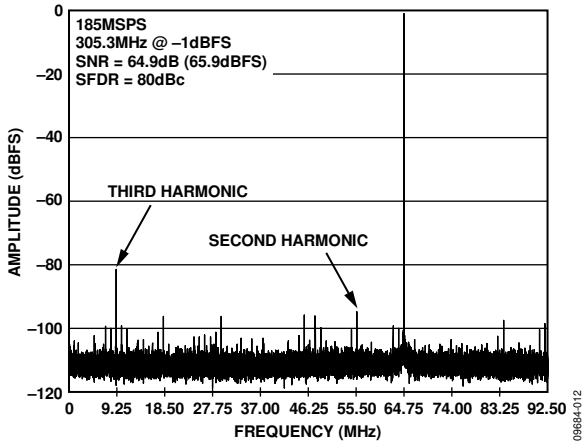

Figure 12. Single Tone FFT, f_{IN} = 305.3 MHz

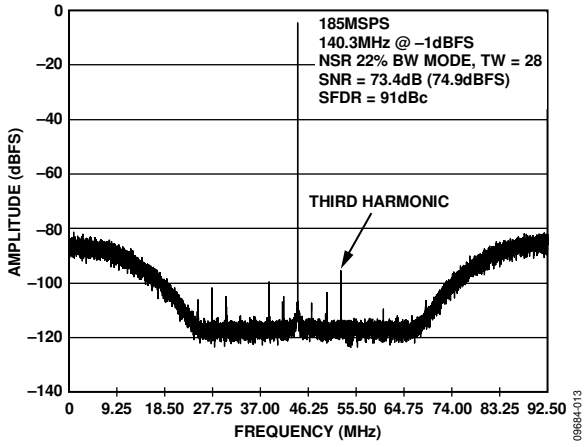

Figure 13. Single Tone FFT, f_{IN} = 140.3 MHz, NSR Enabled in 22% BW Mode, Tuning Word = 28

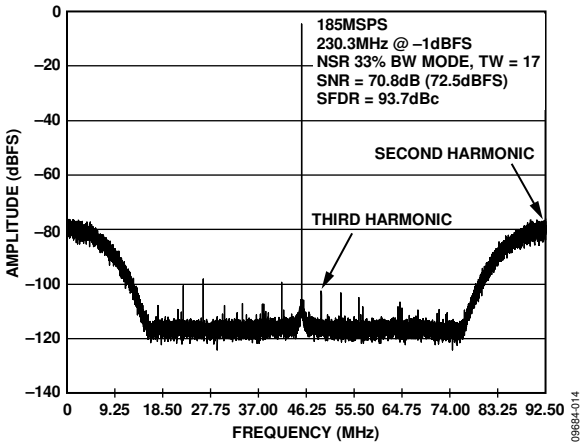

Figure 14. Single Tone FFT, f_{IN} = 230.3 MHz, NSR Enabled in 33% BW Mode, Tuning Word = 17

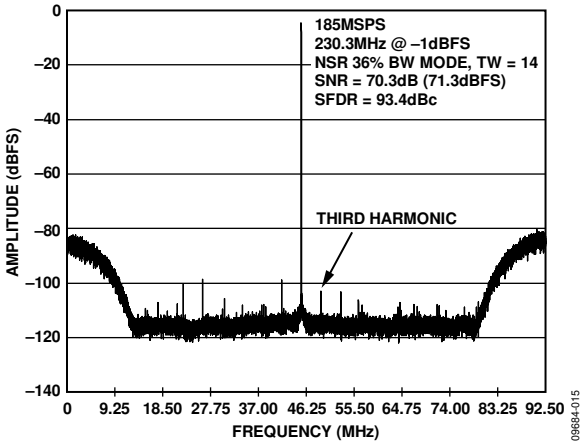

Figure 15. Single Tone FFT, f_{IN} = 230.3 MHz, NSR Enabled in 36% BW Mode, Tuning Word = 14

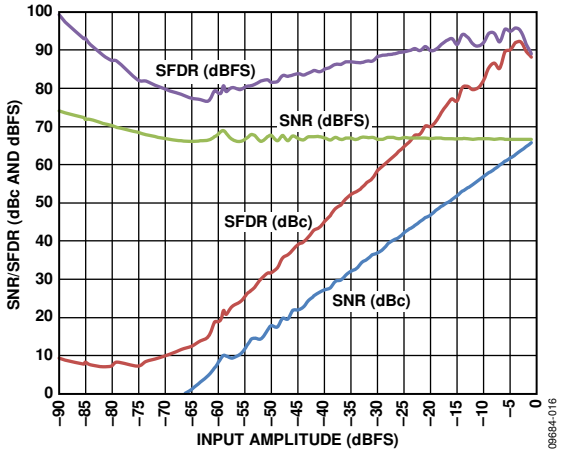

Figure 16. Single Tone SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 70.3 MHz

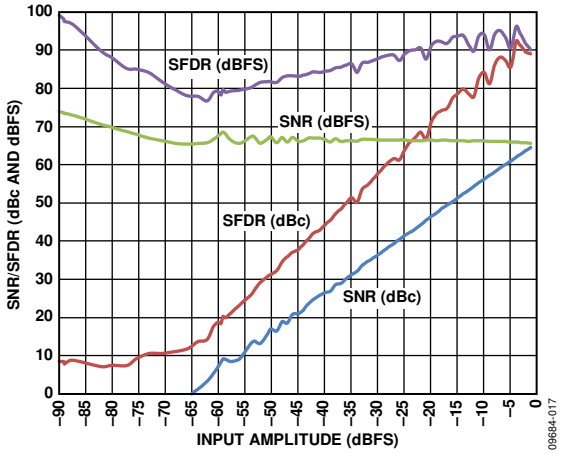

Figure 17. Single Tone SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 140.3 MHz

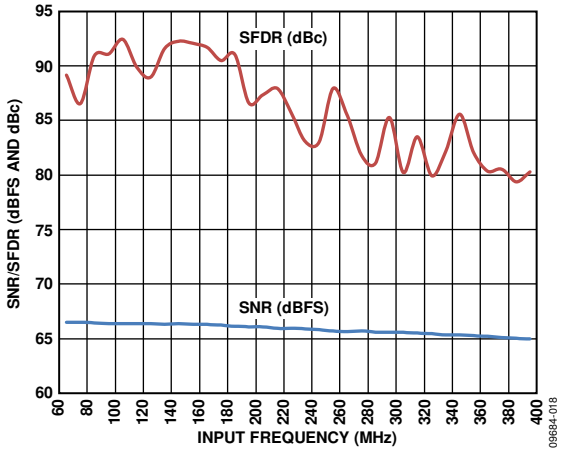

Figure 18. Single Tone SNR/SFDR vs. Input Frequency (f_{IN}), 1.75 V p-p Full Scale

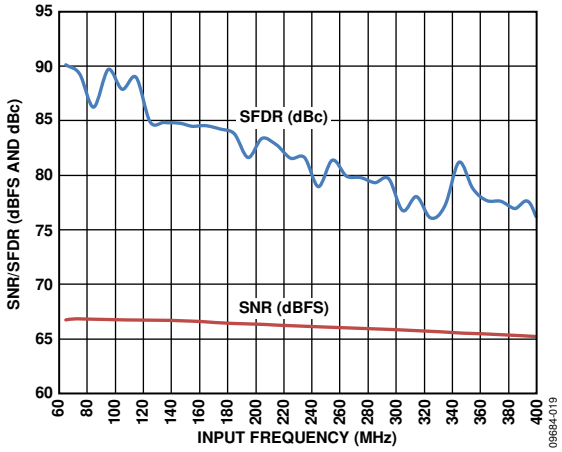

Figure 19. Single Tone SNR/SFDR vs. Input Frequency (f_{IN}), 2.0 V p-p Full Scale

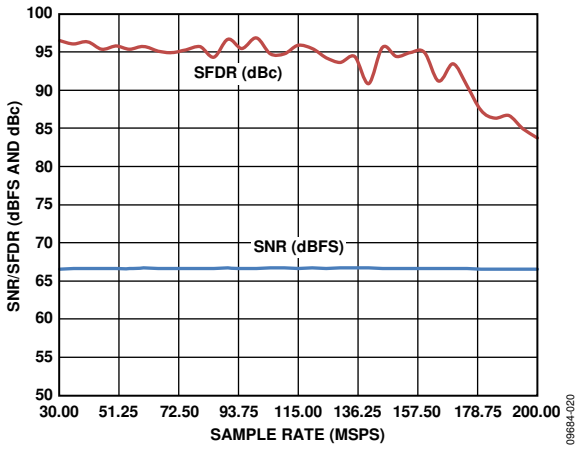

Figure 20. Single Tone SNR/SFDR vs. Sample Rate (f_S), f_{IN} = 70.3 MHz

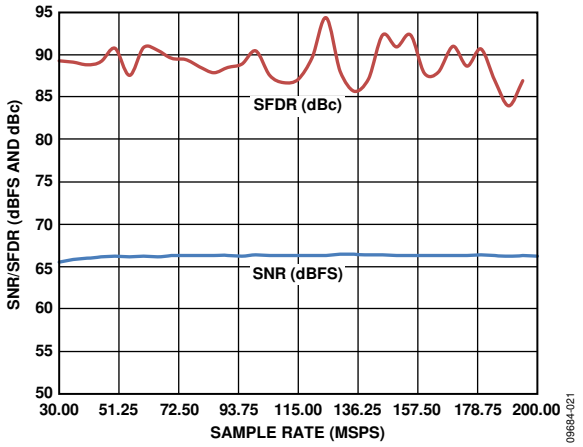

Figure 21. Single Tone SNR/SFDR vs. Sample Rate (f_S), f_{IN} = 140.3 MHz

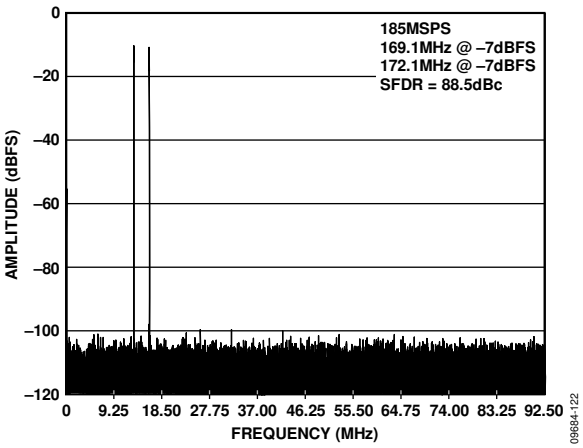

Figure 22. Two Tone FFT, f_{IN1} = 169.1 MHz and f_{IN2} = 172.1 MHz

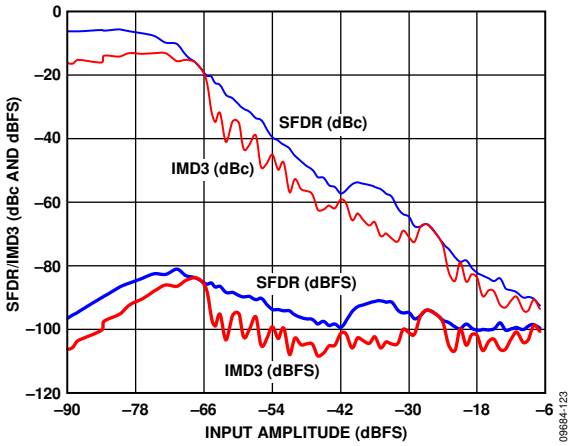

Figure 23. Two Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}), f_{IN1} = 169.1 MHz and f_{IN2} = 172.1 MHz

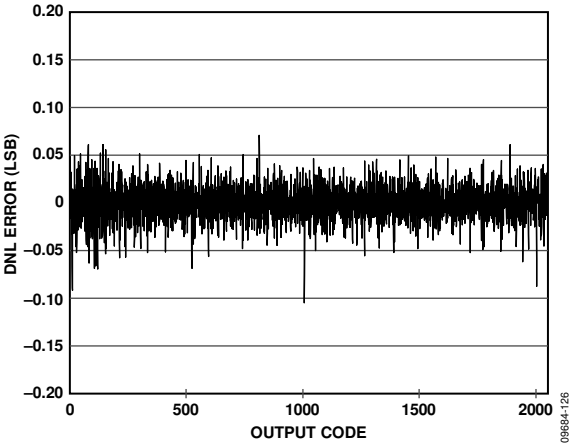

Figure 26. DNL, f_{IN} = 30.3 MHz

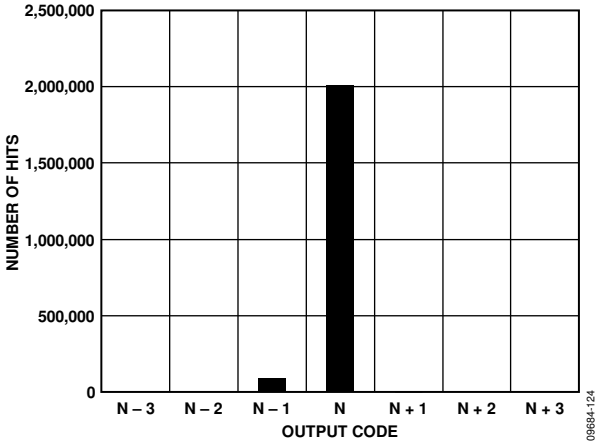

Figure 24. Grounded Input Histogram

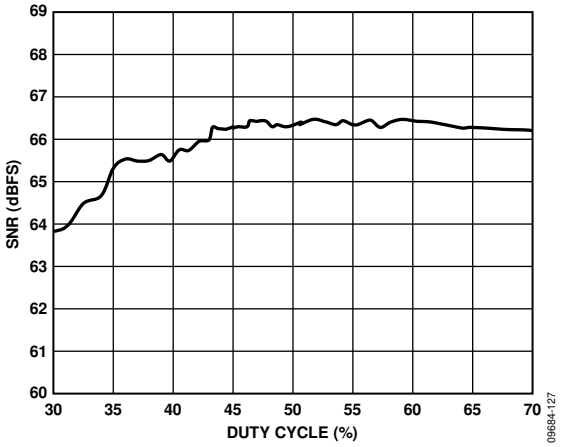

Figure 27. SNR vs. Duty Cycle, f_{IN} = 10.3 MHz

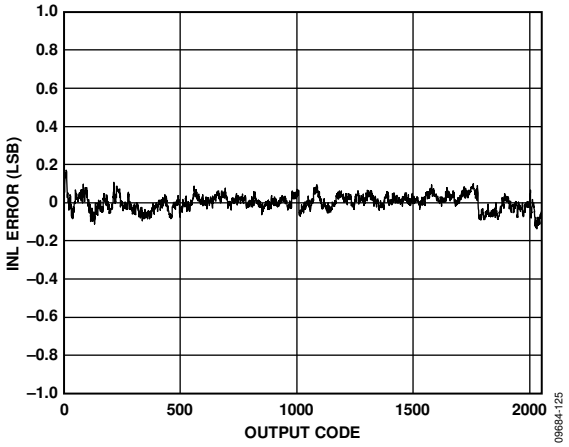

Figure 25. INL, f_{IN} = 30.3 MHz

EQUIVALENT CIRCUITS

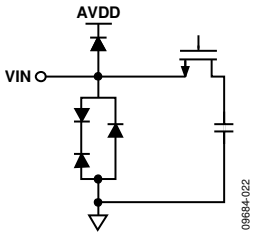

Figure 28. Equivalent Analog Input Circuit

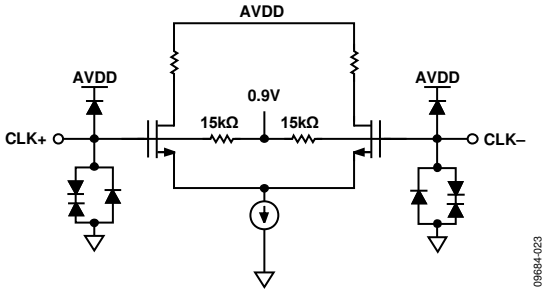

Figure 29. Equivalent Clock Input Circuit

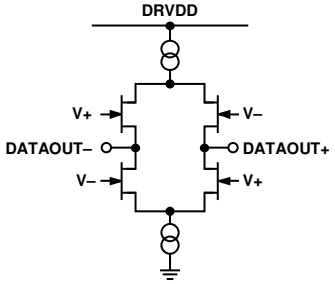

Figure 30. Equivalent LVDS Output Circuit

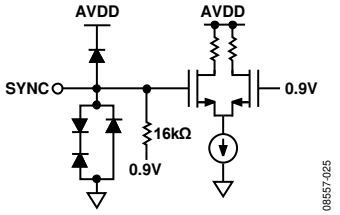

Figure 31. Equivalent SYNC Input Circuit

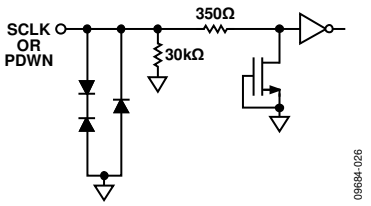

Figure 32. Equivalent SCLK and PDWN Input Circuit

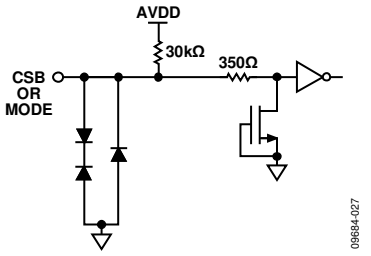

Figure 33. Equivalent CSB and MODE Input Circuit

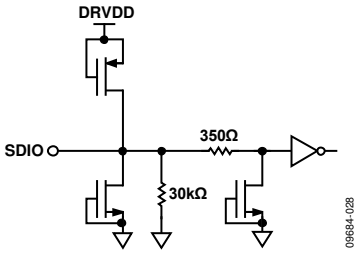

Figure 34. Equivalent SDIO Circuit

THEORY OF OPERATION

ADC ARCHITECTURE

The AD6657A architecture consists of a quad front-end sample-and-hold circuit, followed by a pipelined, switched capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. Alternately, the 14-bit result can be processed through the NSR block before it is sent to the digital correction logic.

The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of each channel contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output drive current. During power-down, the output buffers go into a high impedance state.

The AD6657A quad IF receiver can simultaneously digitize four channels, making it ideal for diversity reception and digital pre-distortion (DPD) observation paths in telecommunication systems.

Synchronization capability is provided to allow synchronized timing between multiple channels or multiple devices.

Programming and control of the AD6657A are accomplished using a 3-wire SPI-compatible serial interface.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD6657A is a differential switched capacitor circuit that has been designed for optimum performance while processing a differential input signal.

The clock signal alternatively switches the input between sample mode and hold mode (see Figure 35). When the input is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within 1/2 of a clock cycle.

A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, any shunt capacitors should be reduced. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. For more information on this subject, see the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters" (see www.analog.com).

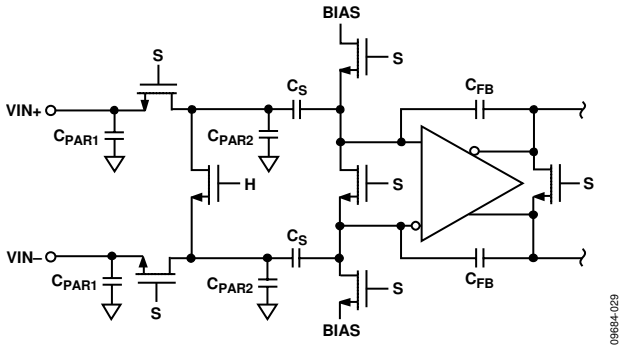

Figure 35. Switched Capacitor Input

For best dynamic performance, match the source impedances driving the VIN+ and VIN− pins.

An internal differential reference buffer creates positive and negative reference voltages that define the input span of the ADC core. The span of the ADC core is set by this buffer to 2 × V_{REF}.

Input Common Mode

The analog inputs of the AD6657A are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. An on-board common-mode voltage reference is included in the design and is available from the VCMx pins. Optimum performance is achieved when the common-mode voltage of the analog input is set by the VCMx pin voltage (typically 0.5 × AVDD). The VCMx pins must be decoupled to ground by a 0.1 µF capacitor.

Differential Input Configurations

Optimum performance is achieved when driving the AD6657A in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, and ADA4938-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4938-2 is easily set with the VCMx pin of the AD6657A (see Figure 36), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

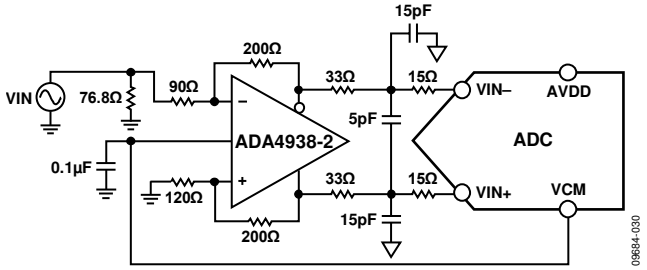

Figure 36. Differential Input Configuration Using the ADA4938-2

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 37. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

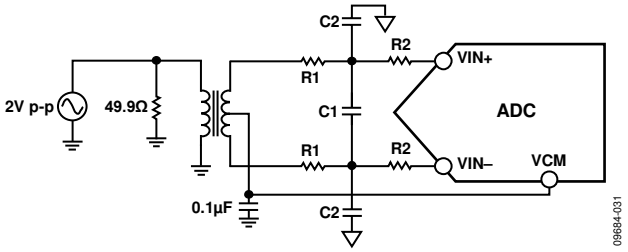

Figure 37. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz (MHz). Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD6657A. For applications in which SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 38). In this configuration, the input is ac-coupled and the CML is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver.

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance and may need to be reduced or removed. Table 10 lists recommended values to set the RC network. At higher input frequencies, good performance can be achieved by using a ferrite bead in series with a resistor and removing the capacitors. However, these values are dependent on the input signal and should be used as a starting guide only.

Table 10. Example RC Network

Frequency Range (MHz)	R1 Series (Each)	C1 Differential	R2 Series (Each)	C2 Shunt (Each)
0 to 100	33 Ω	5 pF	15 Ω	15 pF
100 to 200	10 Ω	5 pF	10 Ω	10 pF
100 to 300	10 Ω[1]	Remove	66 Ω	Remove

[1] In this configuration, R1 is a ferrite bead with a value of 10 Ω @ 100 MHz.

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use the AD8352 differential driver (see Figure 39). For more information, see the AD8352 data sheet.

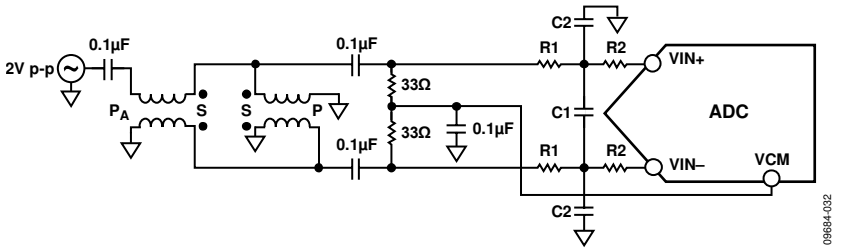

Figure 38. Differential Double Balun Input Configuration

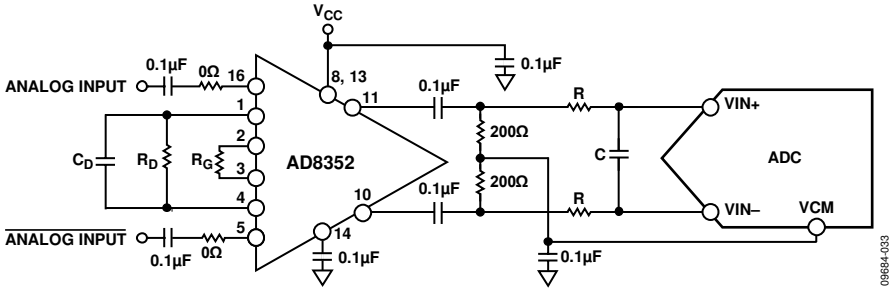

Figure 39. Differential Input Configuration Using the AD8352

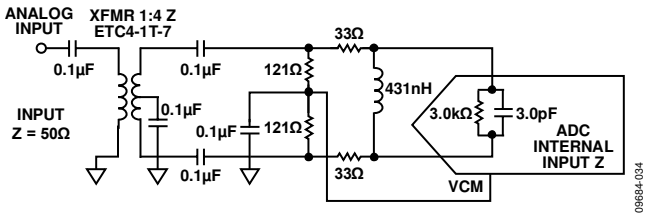

Figure 40. 1:4 Transformer Passive Configuration

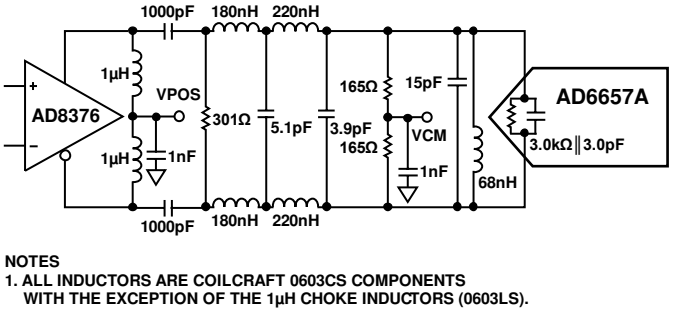

Figure 41. Active Front-End Configuration Using the AD8376

For the popular IF band of 140 MHz, Figure 40 shows an example of a 1:4 transformer passive configuration where a differential inductor is used to resonate with the internal input capacitance of the AD6657A. This configuration realizes excellent noise and distortion performance. Figure 41 shows an example of an active front-end configuration using the AD8376 dual variable gain amplifier (VGA). This configuration is recommended when signal gain is required.

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD6657A sample clock inputs, CLK+ and CLK–, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or capacitors. These pins are biased internally and require no external bias (see Figure 42).

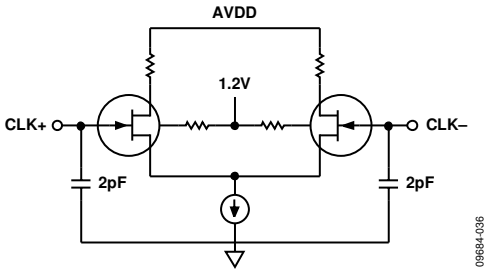

Figure 42. Equivalent Clock Input Circuit

Clock Input Options

The AD6657A has a very flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern (see the Jitter Considerations section).

Figure 43 and Figure 44 show two preferred methods for clocking the AD6657A (at clock rates of up to 625 MHz). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF balun or an RF transformer.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 625 MHz, and the RF transformer configuration is recommended for clock frequencies from 10 MHz to 200 MHz. The back-to-back Schottky diodes across the transformer/balun secondary limit clock excursions into the AD6657A to approximately 0.8 V p-p differential. This limit helps to prevent the large voltage swings of the clock from feeding through to other portions of the AD6657A, yet preserves the fast rise and fall times of the signal that are critical to a low jitter performance.

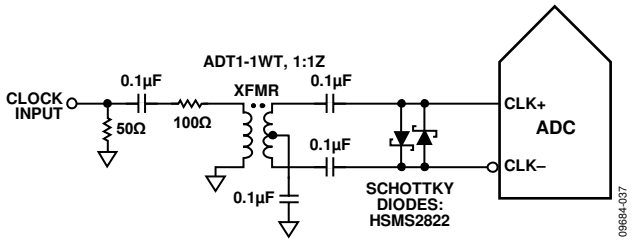

Figure 43. Transformer-Coupled Differential Clock (Up to 200 MHz)

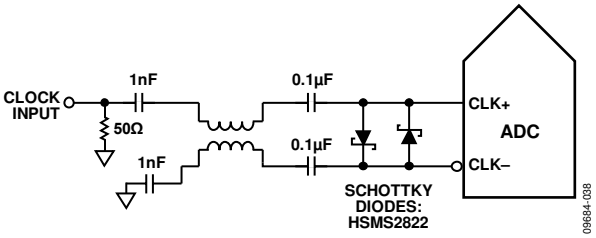

Figure 44. Balun-Coupled Differential Clock (Up to 625 MHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 45. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516 clock drivers offer excellent jitter performance.

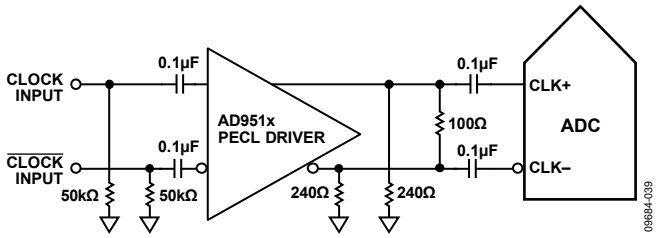

Figure 45. Differential PECL Sample Clock (Up to 625 MHz)

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 46. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516 clock drivers offer excellent jitter performance.

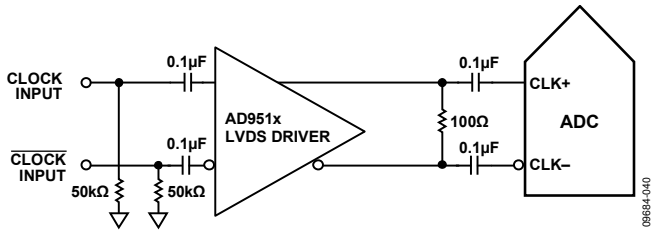

Figure 46. Differential LVDS Sample Clock (Up to 625 MHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK– pin to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 47).

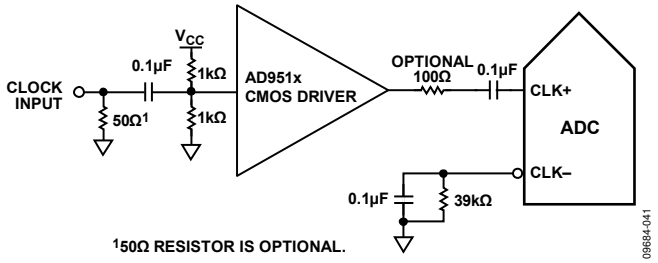

Figure 47. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

CLK+ can be driven directly from a CMOS gate. Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages of up to 3.6 V, making the selection of the drive logic voltage very flexible (see Figure 48).

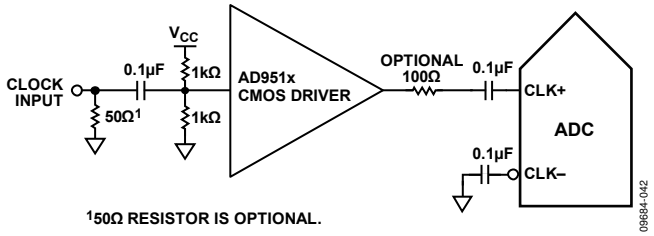

Figure 48. Single-Ended 3.3 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD6657A contains an input clock divider with the ability to divide the input clock by integer values from 1 to 8.

The AD6657A clock divider can be synchronized using the external SYNC input. Bit 1 of Register 0x3A enables the clock divider to be resynchronized on every SYNC signal. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD6657A contains a DCS that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD6657A. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS enabled.

Jitter in the rising edge of the input is of paramount concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates at less than 40 MHz nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time period that the loop is not locked, the DCS loop is bypassed, and internal device timing is dependent on the duty cycle of the input clock signal.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR from the low frequency SNR (SNR_{LF}) at a given input frequency (f_{IN}) due to jitter (t_{JRMS}) can be calculated by

$$SNR_{HF} = -10\log[(2\pi \times f_{IN} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the clock input jitter specification. IF undersampling applications are particularly sensitive to jitter, as shown in Figure 49.

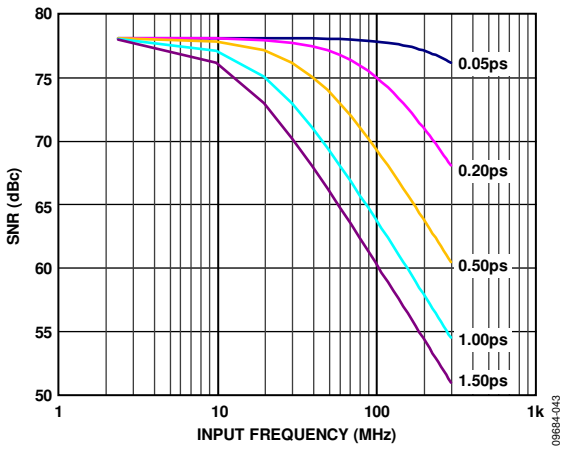

Figure 49. SNR vs. Input Frequency and Jitter

In cases where aperture jitter may affect the dynamic range of the AD6657A, treat the clock input as an analog signal. Separate power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock at the last step. Refer to the AN-501 Application Note and AN-756 Application Note for more information about jitter performance as it relates to ADCs (available at www.analog.com).

POWER DISSIPATION AND STANDBY MODE

The power dissipated by the AD6657A is proportional to its clock rate (see Figure 50). The digital power dissipation does not vary significantly because it is determined primarily by the DRVDD supply and the bias current of the LVDS drivers.

Reducing the capacitive load presented to the output drivers can minimize digital power consumption. The data in Figure 50 was obtained using the same operating conditions as those used in the Typical Performance Characteristics section, with a 5 pF load on each output driver.

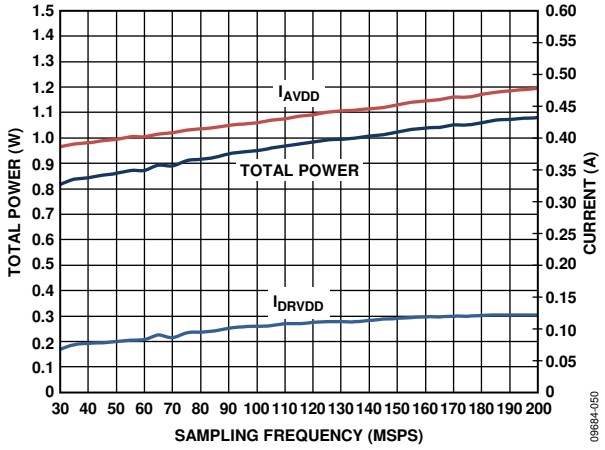

Figure 50. Power and Current vs. Sampling Frequency

By asserting PDWN (either through the SPI port or by asserting the PDWN pin high), the AD6657A is placed in power-down mode. In this state, the ADC typically dissipates 4.5 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD6657A to its normal operating mode. Note that PDWN is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode; shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map Register Descriptions section for more details.

CHANNEL/CHIP SYNCHRONIZATION

The AD6657A has a SYNC input that offers the user flexible synchronization options for synchronizing the clock divider. The clock divider sync feature is useful for guaranteeing synchronized sample clocks across multiple ADCs.

The SYNC input is internally synchronized to the sample clock; however, to ensure that there is no timing uncertainty between multiple parts, externally synchronize the SYNC input signal to the input clock signal, meeting the setup and hold times shown in Table 5. Drive the SYNC input using a single-ended CMOS type signal.

DIGITAL OUTPUTS

The AD6657A output drivers are configured to interface with LVDS outputs using a DRVDD supply voltage of 1.8 V. The output bits are DDR LVDS as shown in Figure 2. Applications that require the ADC to drive large capacitive loads or large fanouts may require external buffers or latches.

As described in the AN-877 Application Note , *Interfacing to High Speed ADCs via SPI*, the data format can be selected for offset binary or twos complement when using the SPI control.

TIMING

The AD6657A provides latched data with a latency of nine clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

Minimize the length of the output data lines and minimize the loads placed on them to reduce transients within the AD6657A because these transients can degrade converter dynamic performance.

The lowest typical conversion rate of the AD6657A is 40 MSPS. At clock rates below 40 MSPS, dynamic performance can degrade.

Data Clock Output (DCO)

The AD6657A provides a data clock output (DCO) signal intended for capturing the data in an external register. The output data for Channel A and Channel C is valid when DCO is high; the output data for Channel B and Channel D is valid when DCO is low (see Figure 2).

Table 11. Output Data Format

Input (V)	Condition (V)	Offset Binary Output Mode	Twos Complement Mode
VIN+ – VIN–	< $-V_{REF}$ – 0.5 LSB	000 0000 0000	100 0000 0000
VIN+ – VIN–	= $-V_{REF}$	000 0000 0000	100 0000 0000
VIN+ – VIN–	= 0	100 0000 0000	000 0000 0000
VIN+ – VIN–	= $+V_{REF}$ – 1.0 LSB	111 1111 1111	011 1111 1111
VIN+ – VIN–	> $+V_{REF}$ – 0.5 LSB	111 1111 1111	011 1111 1111