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80 MHz Bandwidth, Dual IF Receiver

Data Sheet

AD6673

FEATURES

- JESD204B Subclass 0 or Subclass 1 coded serial digital outputs
- Signal-to-noise ratio (SNR) = 71.9 dBFS at 185 MHz AIN and 250 MSPS with NSR set to 33%
- Spurious-free dynamic range (SFDR) = 88 dBc at 185 MHz AIN and 250 MSPS
- Total power consumption: 707 mW at 250 MSPS
- 1.8 V supply voltages
- Integer 1-to-8 input clock divider
- Sample rates of up to 250 MSPS
- IF sampling frequencies of up to 400 MHz
- Internal analog-to-digital converter (ADC) voltage reference
- Flexible analog input range
  - 1.4 V p-p to 2.0 V p-p (1.75 V p-p nominal)
- ADC clock duty cycle stabilizer (DCS)
- 95 dB channel isolation/crosstalk
- Serial port control
- Energy saving power-down modes

APPLICATIONS

- Communications
- Diversity radio and smart antenna (MIMO) systems
- Multimode digital receivers (3G)
  - TD-SCDMA, WiMAX, WCDMA, CDMA2000, GSM, EDGE, LTE
- I/Q demodulation systems
- General-purpose software radios

FUNCTIONAL BLOCK DIAGRAM

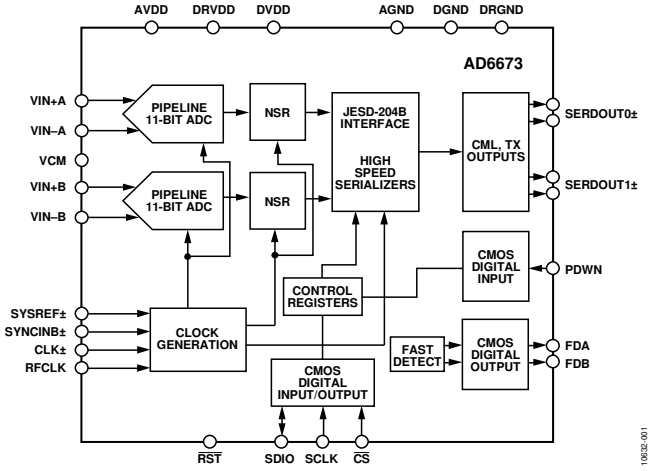

Figure 1.

PRODUCT HIGHLIGHTS

1. The configurable JESD204B output block with an integrated phase-locked loop (PLL) to support up to 5 Gbps per lane with up to two lanes.
2. IF receiver includes two, 11-bit, 250 MSPS ADCs with programmable noise shaping requantizer (NSR) function that allows for improved SNR within a reduced bandwidth of 22% or 33% of the sample rate.
3. Support for an optional RF clock input to ease system board design.
4. Proprietary differential input maintains excellent SNR performance for input frequencies of up to 400 MHz.
5. An on-chip integer, 1-to-8 input clock divider and SYNC input allows synchronization of multiple devices.
6. Operation from a single 1.8 V power supply.
7. Standard serial port interface (SPI) that supports various product features and functions, such as controlling the clock DCS, power-down, test modes, voltage reference mode, overrange fast detection, and serial output configuration.

Rev. C

Document Feedback

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COMPARABLE PARTS

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EVALUATION KITS

- AD6673 Evaluation Board
- High Speed ADC FMC Interposer

DOCUMENTATION

Data Sheet

- AD6673: 80 MHz Bandwidth, Dual IF Receiver Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD6673 Evaluation Board, ADC-FMC Interposer & Xilinx KC705 Reference Design

TOOLS AND SIMULATIONS

- Visual Analog
- AD6673 AMI Model

REFERENCE MATERIALS

Informational

- JESD204 Serial Interface

DESIGN RESOURCES

- AD6673 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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TABLE OF CONTENTS

REVISION HISTORY

12/15—Rev. B to Rev. C

Changes to Nyquist Clock Input Options Section 20
Added Synchronization Section 27
Added Clock Adjustment Register Writes Section 28
Changes to Link Setup Parameters Section 28
Changes to Additional Digital Output Configuration Options Section 30
Added Table 14; Renumbered Sequentially 31
Changes to Table 18 39
Changes to Figure 57 Caption 45

12/13—Rev. A to Rev. B

Changes to Features Section 1
Changes to Functional Block Diagram 1
Changes to Table 4 8
Change to Figure 3 9
Changes to Table 8 11
Change to Figure 20, Figure 21, and Figure 24 15
Added Figure 26; Renumbered Sequentially 16
Changes to Table 9 18
Changes to JESD204B Overview Section 25
Changes to JESD204B Synchronization Section 26
Change to Table 10 26
Change to Configure Detailed Options Section 27
Changes to Figure 50 29
Changes to Figure 52, Figure 53, and Figure 54 30
Deleted Built-In Self-Test (BIST) and Output Test Section 33
Changes to Table 17 37
Changes to Power and Ground Recommendations Section 41
Updated Outline Dimensions 42

10/12—Rev.0 to Rev. A

Changes to Applications Section and Figure 1 1

10/12—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD6673 is an 11-bit, 250 MSPS, dual-channel intermediate frequency (IF) receiver specifically designed to support multi-antenna systems in telecommunication applications where high dynamic range performance, low power, and small size are desired.

The device consists of two high performance analog-to-digital converters (ADCs) and noise shaping requantizer (NSR) digital blocks. Each ADC consists of a multistage, differential pipelined architecture with integrated output error correction logic, and each ADC features a wide bandwidth switched capacitor sampling network within the first stage of the differential pipeline. An integrated voltage reference eases design considerations. A duty cycle stabilizer (DCS) compensates for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

Each ADC output is connected internally to an NSR block. The integrated NSR circuitry allows for improved SNR performance in a smaller frequency band within the Nyquist bandwidth. The device supports two different output modes selectable via the SPI. With the NSR feature enabled, the outputs of the ADCs are processed such that the AD6673 supports enhanced SNR performance within a limited portion of the Nyquist bandwidth while maintaining an 11-bit output resolution.

The NSR block can be programmed to provide a bandwidth of either 22% or 33% of the sample clock. For example, with a sample clock rate of 250 MSPS, the AD6673 can achieve up to 76.3 dBFS SNR for a 55 MHz bandwidth in the 22% mode and up to 73.5 dBFS SNR for a 82 MHz bandwidth in the 33% mode.

When the NSR block is disabled, the ADC data is provided directly to the output at a resolution of 11 bits. The AD6673 can achieve up to 65.9 dBFS SNR for the entire Nyquist bandwidth when operated in this mode. This allows the AD6673 to be used in telecommunication applications such as a digital predistortion observation path where wider bandwidths are required.

By default, the ADC output data is routed directly to the two external JESD204B serial output lanes. These outputs are at current mode logic (CML) voltage levels. Two modes are supported such that output coded data is either sent through one lane or two (L = 1; F = 4 or L = 2; F = 2). Single lane operation supports converter rates up to 125 MSPS. Synchronization input controls (SYNCINB± and SYSREF±) are provided.

The AD6673 receiver digitizes a wide spectrum of IF frequencies. Each receiver is designed for simultaneous reception of a separate antenna. This IF sampling architecture greatly reduces component cost and complexity compared with traditional analog techniques or less integrated digital methods.

Flexible power-down options allow significant power savings, when desired. Programmable overrange level detection is supported for each channel via dedicated fast detect pins.

Programming for setup and control are accomplished using a 3-wire SPI-compatible serial interface with numerous modes to support board level system testing.

The AD6673 is available in a 48-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C.

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, maximum sample rate for speed grade, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, DCS enabled, link parameters used are M = 2 and L = 2, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	Full	11			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−16		+16	mV
Gain Error	Full	−6		+2.5	%FSR
Differential Nonlinearity (DNL)	Full			±0.6	LSB
	25°C		±0.25		LSB
Integral Nonlinearity (INL)[1]	Full			±0.7	LSB
	25°C		±0.3		LSB
MATCHING CHARACTERISTIC					
Offset Error	Full	−15		+15	mV
Gain Error	Full	−2		+3	%FSR
TEMPERATURE DRIFT					
Offset Error	Full		±2		ppm/°C
Gain Error	Full		±50		ppm/°C
INPUT REFERRED NOISE					
VREF = 1.0 V	25°C		0.32		LSB rms
ANALOG INPUT					
Input Span	Full		1.75		V p-p
Input Capacitance[2]	Full		2.5		pF
Input Resistance[3]	Full		20		kΩ
Input Common-Mode Voltage	Full		0.9		V
POWER SUPPLIES					
Supply Voltage					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
DVDD	Full	1.7	1.8	1.9	V
Supply Current					
IAVDD	Full		254	282	mA
IDRVDD + IDVDD	Full				mA
NSR Disabled	Full		139	150	mA
NSR Enabled, 22% Mode	Full		187		mA
NSR Enabled, 33% Mode	Full		211		mA
POWER CONSUMPTION					
Sine Wave Input	Full				
NSR Disabled	Full		707		mW
NSR Enabled, 22% Mode	Full		794		mW
NSR Enabled, 33% Mode	Full		837		mW
Standby Power[4]	Full		334		mW
Power-Down Power	Full		9		mW

[1] Measured with a low input frequency, full-scale sine wave.
[2] Input capacitance refers to the effective capacitance between one differential input pin and its complement.
[3] Input resistance refers to the effective resistance between one differential input pin and its complement.
[4] Standby power is measured with a dc input and the CLK± pin active.

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, maximum sample rate for speed grade, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, DCS enabled, link parameters used are M = 2 and L = 2, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE-RATIO (SNR)					
NSR Disabled					
f_{IN} = 30 MHz	25°C		66.6		dBFS
f_{IN} = 90 MHz	25°C		66.2		dBFS
f_{IN} = 140 MHz	25°C		66.4		dBFS
f_{IN} = 185 MHz	25°C		66.2		dBFS
	Full	65.6			dBFS
f_{IN} = 220 MHz	25°C		65.9		dBFS
NSR Enabled 22% Bandwidth Mode					
f_{IN} = 30 MHz	25°C		76.3		dBFS
f_{IN} = 90 MHz	25°C		75.7		dBFS
f_{IN} = 140 MHz	25°C		74.8		dBFS
f_{IN} = 185 MHz	25°C		74.2		dBFS
	Full	72.6			dBFS
f_{IN} = 220 MHz	25°C		73.6		dBFS
NSR Enabled 33% Bandwidth Mode					
f_{IN} = 30 MHz	25°C		73.5		dBFS
f_{IN} = 90 MHz	25°C		72.1		dBFS
f_{IN} = 140 MHz	25°C		72.6		dBFS
f_{IN} = 185 MHz	25°C		71.9		dBFS
	Full	70.0			dBFS
f_{IN} = 220 MHz	25°C		71.4		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)					
f_{IN} = 30 MHz	25°C		65.5		dBFS
f_{IN} = 90 MHz	25°C		65.4		dBFS
f_{IN} = 140 MHz	25°C		65.2		dBFS
f_{IN} = 185 MHz	25°C		65.1		dBFS
	Full	64.5			dBFS
f_{IN} = 220 MHz	25°C		64.7		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 30 MHz	25°C		10.6		Bits
f_{IN} = 90 MHz	25°C		10.6		Bits
f_{IN} = 140 MHz	25°C		10.5		Bits
f_{IN} = 185 MHz	25°C		10.5		Bits
f_{IN} = 220 MHz	25°C		10.5		Bits
WORST SECOND OR THIRD HARMONIC					
f_{IN} = 30 MHz	25°C		−90		dBc
f_{IN} = 90 MHz	25°C		−87		dBc
f_{IN} = 140 MHz	25°C		−86		dBc
f_{IN} = 185 MHz	25°C		−88		dBc
	Full			−80	dBc
f_{IN} = 220 MHz	25°C		−86		dBc

Parameter[1]	Temperature	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 30 MHz	25°C		90		dBc
f_{IN} = 90 MHz	25°C		87		dBc
f_{IN} = 140 MHz	25°C		86		dBc
f_{IN} = 185 MHz	25°C		88		dBc
	Full	80			dBc
f_{IN} = 220 MHz	25°C		86		dBc
WORST OTHER (HARMONIC OR SPUR)					
f_{IN} = 30 MHz	25°C		−96		dBc
f_{IN} = 90 MHz	25°C		−94		dBc
f_{IN} = 140 MHz	25°C		−94		dBc
f_{IN} = 185 MHz	25°C		−94		dBc
	Full			−80	dBc
f_{IN} = 220 MHz	25°C		−91		dBc
TWO-TONE SFDR					
f_{IN} = 184.12 MHz (−7 dBFS), 187.12 MHz (−7 dBFS)	25°C		88		dBc
CROSSTALK[2]	Full		95		dB
FULL POWER BANDWIDTH[3]	25°C		1000		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1.0 dBFS on one channel and no input on the alternate channel.
[3] Full power bandwidth is the bandwidth of operation determined by where the spectral power of the fundamental frequency is reduced by 3 dB.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, maximum sample rate for speed grade, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, DCS enabled, link parameters used are M = 2 and L = 2, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK–)					
Input CLK± Clock Rate	Full	40		625	MHz
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	0		+60	µA
Low Level Input Current	Full	−60		0	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
RF CLOCK INPUT (RFCLK)					
Input CLK± Clock Rate	Full	650		1500	MHz
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
Input Voltage Level					
High	Full	1.2		AVDD	V
Low	Full	AGND		0.6	V
High Level Input Current	Full	0		+150	µA
Low Level Input Current	Full	−150		0	µA
Input Capacitance	Full		1		pF
Input Resistance (AC-Coupled)	Full	8	10	12	kΩ

Parameter	Temperature	Min	Typ	Max	Unit
SYNCIN INPUT (SYNCINB+, SYNCINB−)					
Logic Compliance			LVDS		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage Range	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		DVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−5		+5	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ
SYSREF INPUT (SYSREF+/SYSREF−)					
Logic Compliance			LVDS		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage Range	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−5		+5	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
LOGIC INPUT ($\overline{RST}$, $\overline{CS}$)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−100		−45	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK, PDWN)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		100	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (SDIO)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	−100		−45	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS (SERDOUT0±, SERDOUT1±)					
Logic Compliance	Full		CML		
Differential Output Voltage (V_{OD})	Full	400	600	750	mV
Output Offset Voltage (V_{OS})	Full	0.75	DRVDD/2	1.05	V
DIGITAL OUTPUTS (SDIO, FDA, FDB)					
High Level Output Voltage (V_{OH})	Full				
I_{OH} = 50 µA	Full	1.79			V
I_{OH} = 0.5 mA	Full	1.75			V

Parameter	Temperature	Min	Typ	Max	Unit
Low Level Output Voltage (V_{OL})	Full				
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V

[1] Pull-up.
[2] Pull-down.

SWITCHING SPECIFICATIONS

Table 4.

Parameter	Symbol	Temperature	Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS						
Conversion Rate[1]	f_S	Full	40		250	MSPS
SYSREF± Setup Time to Rising Edge CLK±[2]	t_{REFS}	Full		0.31		ns
SYSREF± Hold Time from Rising Edge CLK±[2]	t_{REFH}	Full		0		ns
SYSREF± Setup Time to Rising Edge RFCLK[2]	t_{REFSRF}	Full		0.50		ns
SYSREF± Hold Time from Rising Edge RFCLK[2]	t_{REFHRF}	Full		0		ns
CLK± Pulse Width High	t_{CH}					
Divide-by-1 Mode, DCS Enabled		Full	1.8	2.0	2.2	ns
Divide-by-1 Mode, DCS Disabled		Full	1.9	2.0	2.1	ns
Divide-by-2 Mode Through Divide-by-8 Mode		Full	0.8			ns
Aperture Delay	t_A	Full		1.0		ns
Aperture Uncertainty (Jitter)	t_J	Full		0.16		ps rms
DATA OUTPUT PARAMETERS						
Data Output Period or Unit Interval (UI)		Full		$L/(20 \times M \times f_S)$		Seconds
Data Output Duty Cycle		25°C		50		%
Data Valid Time		25°C		0.78		UI
PLL Lock Time (t_{LOCK})		25°C		25		µs
Wake-Up						
Time (Standby)		25°C		10		µs
Time ADC (Power-Down)[3]		25°C		250		ms
Time Output (Power-Down)[4]		25°C		50		ms
Subclass 0: SYNCINB± Falling Edge to First Valid K.28 Characters (Delay Required for Rx CGS Start)		Full	5			Multiframes
Subclass 1: SYSREF± Rising Edge to First Valid K.28 Characters (Delay Required for SYNCB± Rising Edge/Rx CGS Start)		Full	5			Multiframes
CGS Phase K.28 Characters Duration		Full	1			Multiframe
Pipeline Delay						
JESD204B M1, L1 Mode (Latency)		Full		36		Cycles[5]
JESD204B M1, L2 Mode (Latency)		Full		59		Cycles
JESD204B M2, L1 Mode (Latency)		Full		25		Cycles
JESD204B M2, L2 Mode (Latency)		Full		36		Cycles
Additional Pipeline Latency with NSR Enabled		Full		2		Cycles
Fast Detect (Latency)		Full		7		Cycles
Data Rate per Lane		25°C			5.0	Gbps
Uncorrelated Bounded High Probability (UBHP) Jitter		25°C		8		ps
Random Jitter at 5.0 Gbps		25°C		1.7		ps rms
Output Rise/Fall Time		25°C		60		ps
Differential Termination Resistance		25°C		100		Ω
Out-of-Range Recovery Time		Full		3		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Refer to Figure 3 for timing diagram.
[3] Wake-up time ADC is defined as the time required for the ADC to return to normal operation from power-down mode.
[4] Wake-up time output is defined as the time required for JESD204B output to return to normal operation from power-down mode.
[5] Cycles refers to ADC conversion rate cycles.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPI TIMING REQUIREMENTS (See Figure 56)					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between $\overline{CS}$ and SCLK	2			ns
t_H	Hold time between $\overline{CS}$ and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK should be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK should be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in figures)	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in figures)	10			ns
t_{SPI_RST}	Time required after hard or soft reset until SPI access is available (not shown in figures)	500			µs

Timing Diagrams

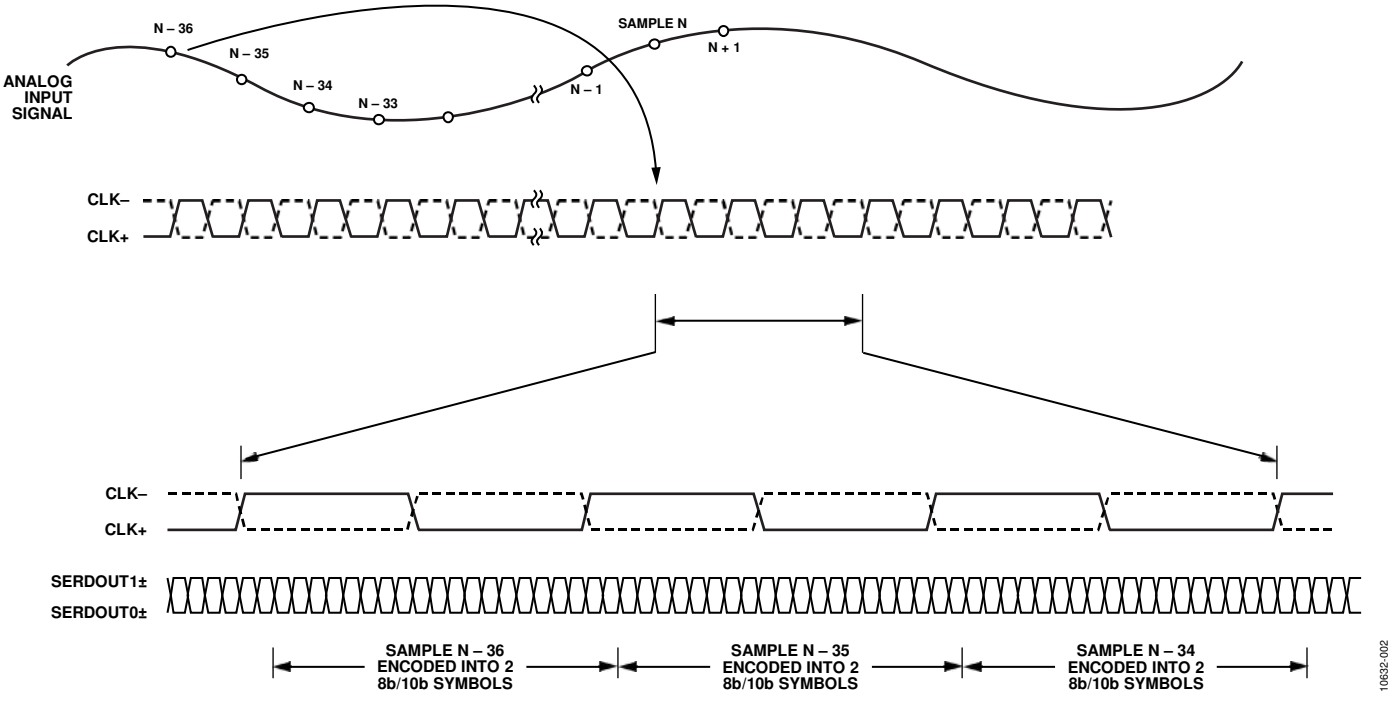

Figure 2. Data Output Timing

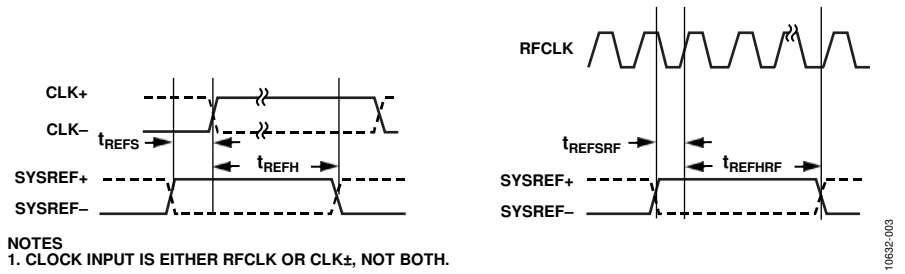

Figure 3. SYSREF± Setup and Hold Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
ELECTRICAL	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
DVDD to DGND	−0.3 V to +2.0 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
RFCLK to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
$\overline{CS}$, PDWN to AGND	−0.3 V to AVDD + 0.3 V
SCLK to AGND	−0.3 V to AVDD + 0.3 V
SDIO to AGND	−0.3 V to AVDD + 0.3 V
$\overline{RST}$ to DGND	−0.3 V to DVDD + 0.3 V
FDA, FDB to DGND	−0.3 V to DVDD + 0.3 V
SERDOUT0+, SERDOUT0−, SERDOUT1+, SERDOUT1− to AGND	−0.3 V to DRVDD + 0.3 V
SYNCINB+, SYNCINB− to DGND	−0.3 V to DVDD + 0.3 V
SYSREF+, SYSREF− to AGND	−0.3 V to AVDD + 0.3 V
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. This increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA} [1,2]	θ_{JC} [1,3]	θ_{JB} [1,4]	Unit
48-Lead LFCSP 7 mm × 7 mm (CP-48-13)	0	25	2	14	°C/W
	1.0	22			°C/W
	2.5	20			°C/W

[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-STD-883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer printed circuit board (PCB) with a solid ground plane. As shown in Table 7, airflow increases heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

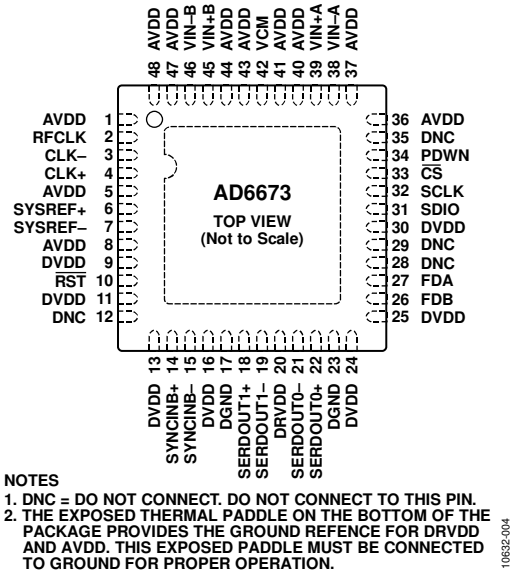

Figure 4. Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
1, 5, 8, 36, 37, 40, 41, 43, 44, 47, 48	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
9, 11, 13, 16, 24, 25, 30	DVDD	Supply	Digital Power Supply (1.8 V Nominal).
12, 28, 29, 35	DNC		Do Not Connect.
17, 23	DGND		Ground Reference for DVDD.
20	DRVDD	Supply	JESD204B PHY Serial Output Driver Supply (1.8 V Nominal). Note that the DRVDD power is referenced to the AGND Plane.
Exposed Paddle	AGND/DRGND	Ground	The exposed thermal paddle on the bottom of the package provides the ground reference for DRVDD and AVDD. This exposed paddle must be connected to ground for proper operation.
ADC Analog			
2	RFCLK	Input	ADC RF Clock Input.
3	CLK–	Input	ADC Nyquist Clock Input—Complement.
4	CLK+	Input	ADC Nyquist Clock Input—True.
38	VIN–A	Input	Differential Analog Input Pin (–) for Channel A.
39	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
42	VCM	Output	Common-Mode Level Bias Output for Analog Inputs. Decouple this pin to ground using a 0.1 µF capacitor.
45	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
46	VIN–B	Input	Differential Analog Input Pin (–) for Channel B.
ADC Fast Detect Outputs			
26	FDB	Output	Channel B Fast Detect Indicator (CMOS Levels).
27	FDA	Output	Channel A Fast Detect Indicator (CMOS Levels).
Digital Inputs			
6	SYSREF+	Input	JESD204B LVDS SYSREF Input—True
7	SYSREF–	Input	JESD204B LVDS SYSREF Input—Complement.
14	SYNCINB+	Input	JESD204B LVDS SYNC Input—True
15	SYNCINB–	Input	JESD204B LVDS SYNC Input—Complement.

Pin No.	Mnemonic	Type	Description
Data Outputs			
18	SERDOUT1+	Output	Lane B CML Output Data—True.
19	SERDOUT1−	Output	Lane B CML Output Data—Complement.
21	SERDOUT0−	Output	Lane A CML Output Data—Complement.
22	SERDOUT0+	Output	Lane A CML Output Data—True.
DUT Controls			
10	$\overline{\text{RST}}$	Input	Digital Reset (Active Low).
31	SDIO	Input/Output	SPI Serial Data I/O.
32	SCLK	Input	SPI Serial Clock.
33	$\overline{\text{CS}}$	Input	SPI Chip Select (Active Low).
34	PDWN	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby (see Table 18).

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, sample rate is 250 MSPS, DCS enabled, 1.75 V p-p differential input, VIN = −1.0 dBFS, 32k sample, T_A = 25°C, link parameters used were M = 2 and L = 2, unless otherwise noted.

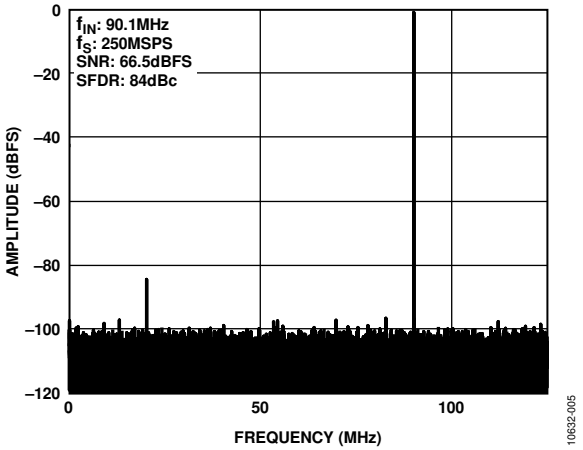

Figure 5. AD6673-250 Single-Tone FFT with f_{IN} = 90.1 MHz

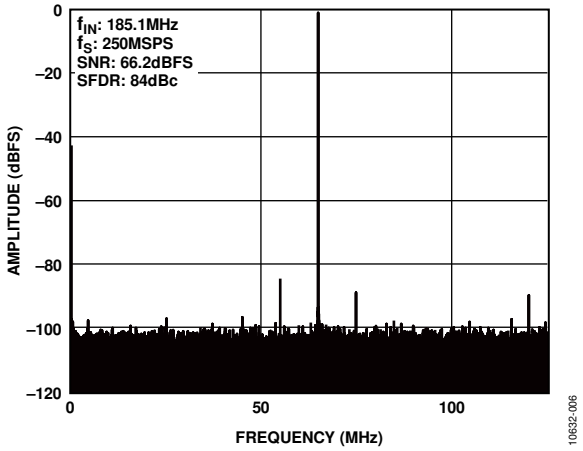

Figure 6. AD6673-250 Single-Tone FFT with f_{IN} = 185.1 MHz

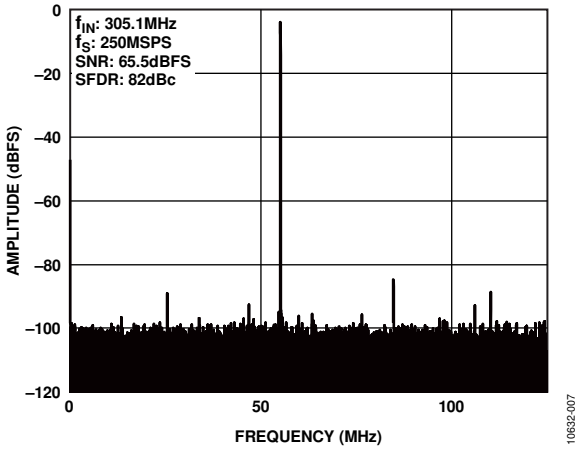

Figure 7. AD6673-250 Single-Tone FFT with f_{IN} = 305.1 MHz

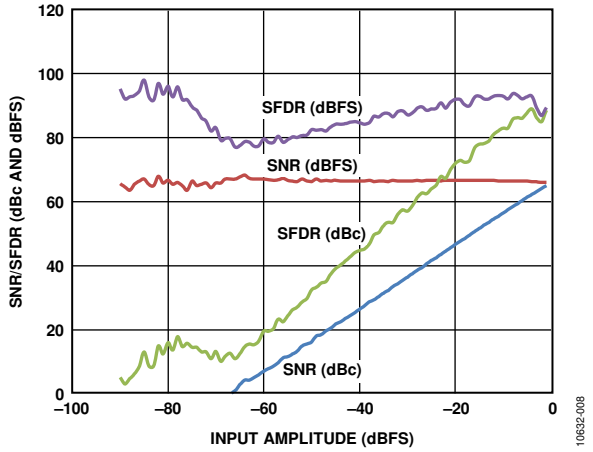

Figure 8. AD6673-250 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 185.1 MHz

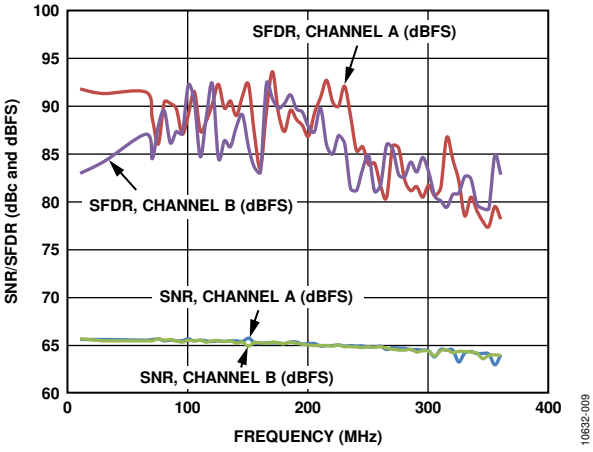

Figure 9. AD6673-250 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN})

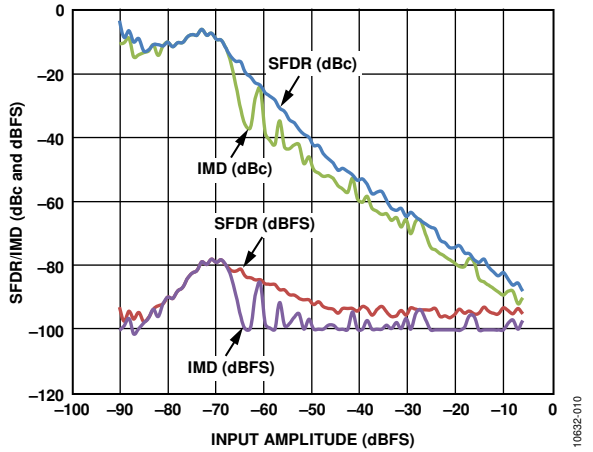

Figure 10. AD6673-250 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz

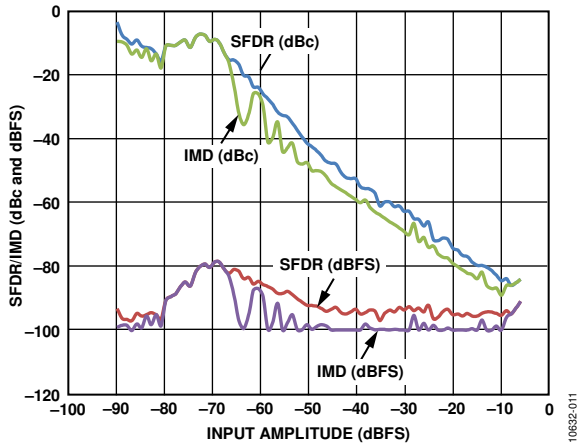

Figure 11. AD6673-250 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz

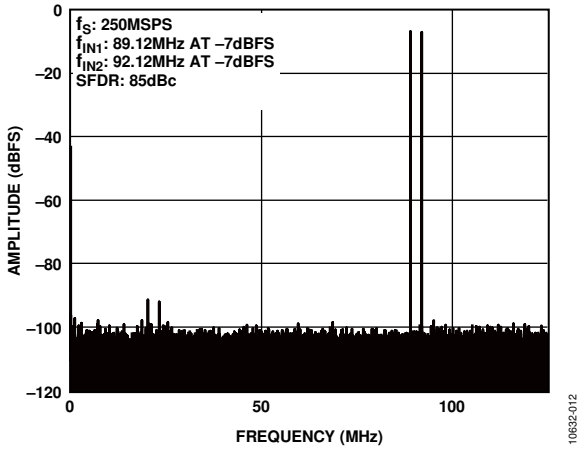

Figure 12. AD6673-250 Two-Tone FFT with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz

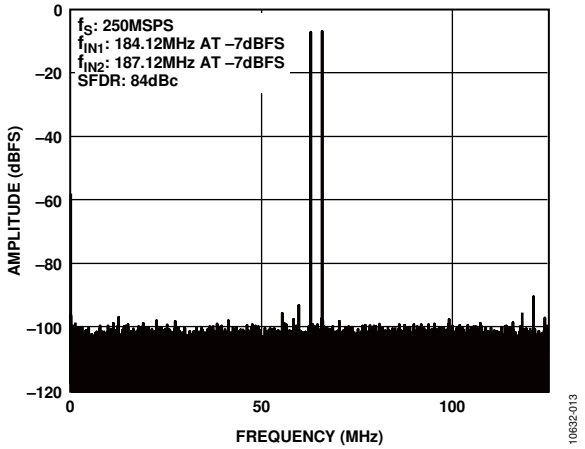

Figure 13. AD6673-250 Two-Tone FFT with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz

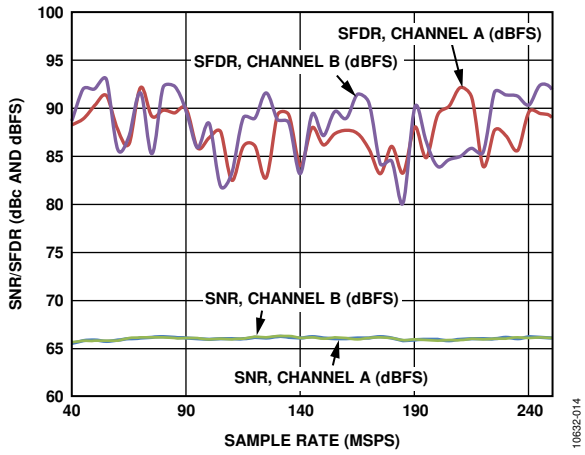

Figure 14. AD6673-250 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90.1 MHz

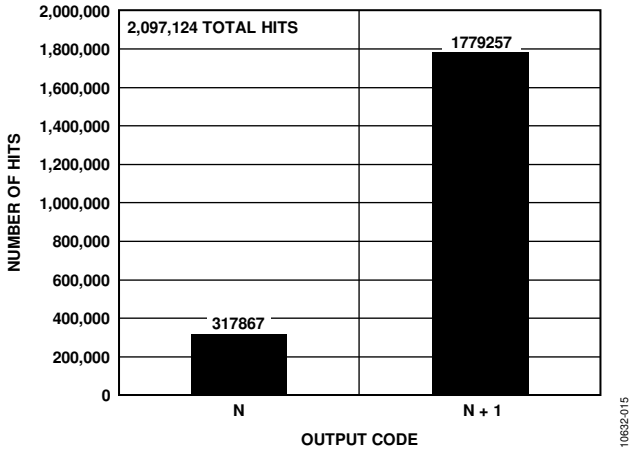

Figure 15. AD6673-250 Grounded Input Histogram

EQUIVALENT CIRCUITS

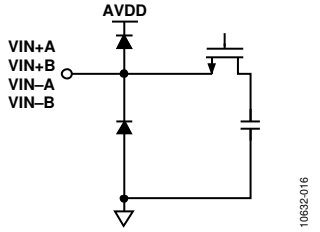

Figure 16. Equivalent Analog Input Circuit

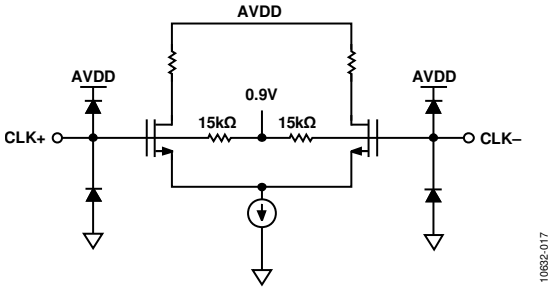

Figure 17. Equivalent Clock Input Circuit

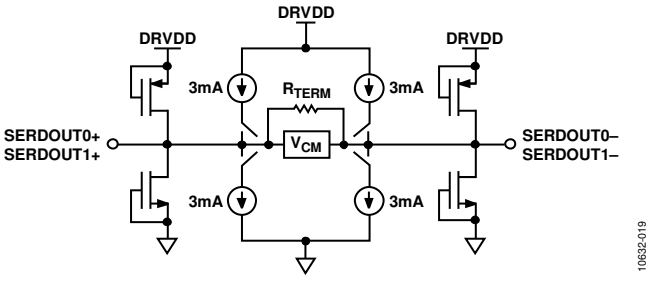

Figure 18. Digital CML Output Circuit

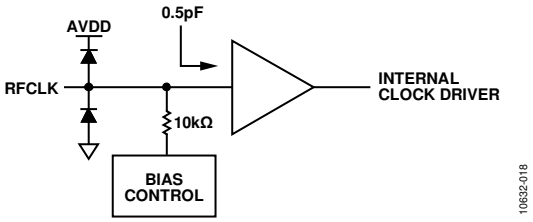

Figure 19. Equivalent RF Clock Input Circuit

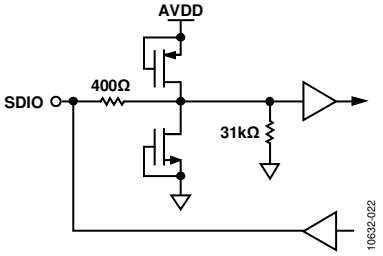

Figure 20. Equivalent SDIO Circuit

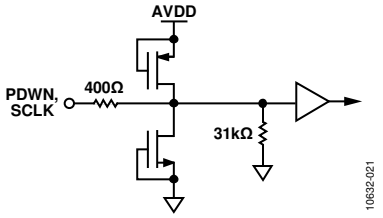

Figure 21. Equivalent SCLK or PDWN Input Circuit

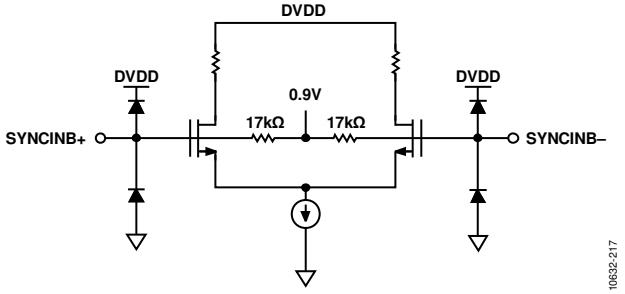

Figure 22. Equivalent SYNCINB± Input Circuit

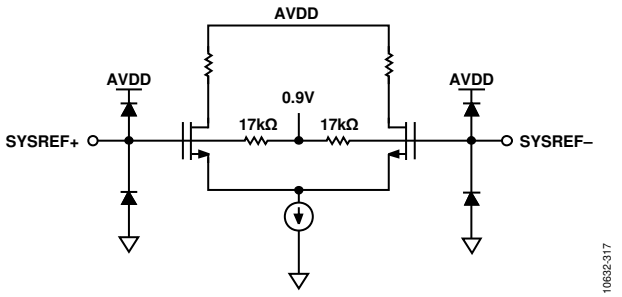

Figure 23. Equivalent SYSREF± Input Circuit

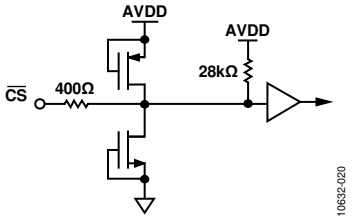

Figure 24. Equivalent $\overline{CS}$ Input Circuit

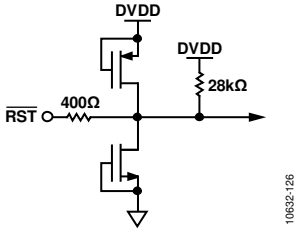

Figure 26. $\overline{RST}$ Equivalent Circuit

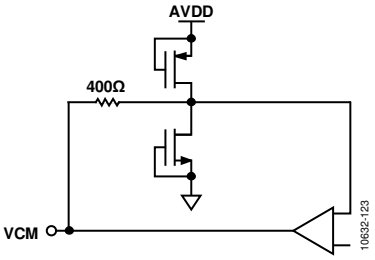

Figure 25. Equivalent VCM Circuit

THEORY OF OPERATION

The AD6673 has two analog input channels and two JESD204B output lanes. The signal passes through several stages before appearing at the output port(s).

The dual ADC design can be used for diversity reception of signals, where the ADCs operate identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample frequencies from dc to 300 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. Operation to 400 MHz analog input is permitted but occurs at the expense of increased ADC noise and distortion.

A synchronization capability is provided to allow synchronized timing between multiple devices.

Programming and control of the AD6673 are accomplished using a 3-pin, SPI-compatible serial interface.

ADC ARCHITECTURE

The AD6673 architecture consists of a dual, front-end, sample-and-hold circuit, followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 11-bit result in the digital correction logic. Alternately, the 11-bit result can be processed through the NSR block before it is sent to the digital correction logic.

The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The MDAC magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of each channel contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing digital output noise to be separated from the analog core.

The AD6673 dual IF receiver can simultaneously digitize two channels, making it ideal for diversity reception and digital predistortion (DPD) observation paths in telecommunication systems. The dual IF receiver design can be used for diversity reception of signals, whereas the ADCs operate identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can input frequencies from dc to 300 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in performance. Operation to a 400 MHz analog input is permitted; however, it occurs at the expense of increased ADC noise and distortion. A synchronization capability is provided to allow synchronized timing between multiple devices. Programming and control of the AD6673 are accomplished using a 3-wire SPI-compatible serial interface.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD6673 is a differential, switched capacitor circuit that has been designed for optimum performance while processing a differential input signal.

The clock signal alternatively switches the input between sample mode and hold mode (see the configuration shown in Figure 27). When the input is switched into sample mode, the signal source must be capable of charging the sampling capacitors and settling within 1/2 clock cycle.

A small resistor in series with each input can help reduce the peak transient current that is required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, reduce the shunt capacitors. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. Refer to the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters," for more information on this subject.

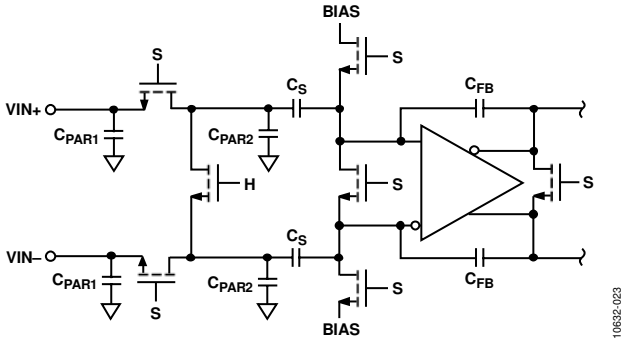

Figure 27. Switched-Capacitor Input

For best dynamic performance, match the source impedances driving VIN+ and VIN– and differentially balance the inputs.

Input Common Mode

The analog inputs of the AD6673 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = 0.5 × AVDD (or 0.9 V) is recommended for optimum performance. An on-board common-mode voltage reference is included in the design and is available from the VCM pin. Using the VCM output to set the input common mode is recommended. Optimum performance is achieved when the common-mode voltage of the analog input is set by the VCM pin voltage (typically 0.5 × AVDD). Decouple the VCM pin to ground by using a 0.1 µF capacitor, as described in the Applications Information section. Place this decoupling capacitor close to the pin to minimize the series resistance and inductance between the part and this capacitor.

Differential Input Configurations

Optimum performance is achieved while driving the AD6673 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, ADA4938-2, and ADA4930-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4930-2 is easily set with the VCM pin of the AD6673 (see Figure 28), and the driver can be configured in a Sallen-Key filter topology to provide band-limiting of the input signal.

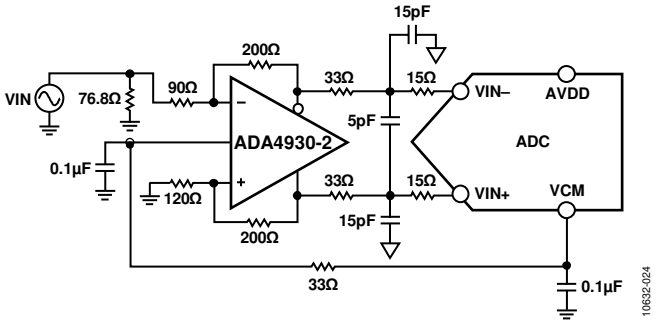

Figure 28. Differential Input Configuration Using the ADA4930-2

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 29. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

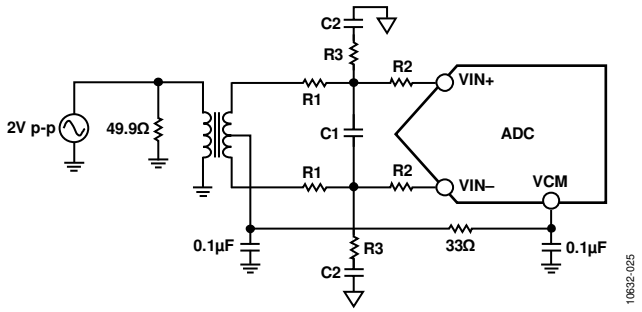

Figure 29. Differential Transformer-Coupled Configuration

Consider the signal characteristics when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz. Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD6673. For applications where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 30). In this configuration, the input is ac-coupled and the VCM voltage is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver.

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance. Based on these parameters, the value of the input resistors and capacitors may need to be adjusted or some components may need to be removed. Table 9 displays recommended values to set the RC network for different input frequency ranges. However, these values are dependent on the input signal and bandwidth and should be used only as a starting guide. Note that the values given in Table 9 are for each R1, R2, C1, C2, and R3 components shown in Figure 29 and Figure 30.

Table 9. Example RC Network

Frequency Range (MHz)	R1 Series (Ω)	C1 Differential (pF)	R2 Series (Ω)	C2 Shunt (pF)	R3 Shunt (Ω)
0 to 100	33	8.2	0	15	24.9
100 to 300	15	3.9	0	8.2	24.9

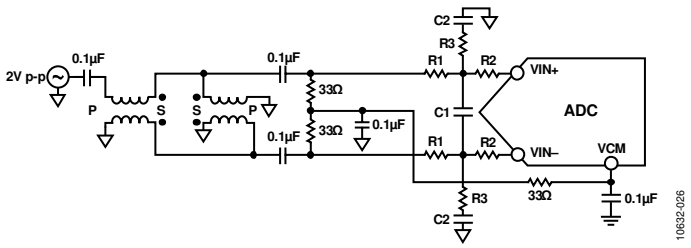

Figure 30. Differential Double Balun Input Configuration

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use an amplifier with variable gain. The AD8375 or AD8376 digital variable gain amplifier (DVGA) provides good performance for driving the AD6673. Figure 31 shows an example of the AD8376 driving the AD6673 through a band-pass antialiasing filter.

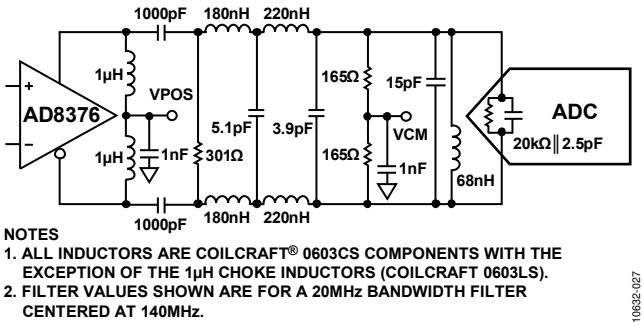

Figure 31. Differential Input Configuration Using the AD8376

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD6673. The full-scale input range can be adjusted by varying the reference voltage via the SPI. The input span of the ADC tracks the reference voltage changes linearly.

CLOCK INPUT CONSIDERATIONS

The AD6673 has two options for deriving the input sampling clock, a differential Nyquist sampling clock input or an RF clock input (which is internally divided by 4). The clock input is selected in Register 0x09 and, by default, is configured for the Nyquist clock input. For optimum performance, clock the AD6673 Nyquist sample clock input, CLK+ and CLK−, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or via capacitors. These pins are biased internally (see Figure 32) and require no external bias. If the clock inputs are floated, CLK− is pulled slightly lower than CLK+ to prevent spurious clocking.

Nyquist Clock Input Options

The AD6673 Nyquist clock input supports a differential clock between 40 MHz to 625 MHz. The clock input structure supports differential input voltages from 0.3 V to 3.6 V and is therefore compatible with various logic family inputs, such as CMOS, LVDS, and LVPECL. A sine wave input is also accepted, but higher slew rates typically provide optimal performance. Clock source jitter is a critical parameter that can affect performance, as described in the Jitter Considerations section. If the inputs are floated, pull the CLK− pin low to prevent spurious clocking.

The Nyquist clock input pins, CLK+ and CLK−, are internally biased to 0.9 V and have a typical input impedance of 4 pF in parallel with 10 kΩ (see Figure 32). The input clock is typically ac-coupled to CLK+ and CLK−. Some typical clock drive circuits are presented in Figure 33 through Figure 36 for reference.

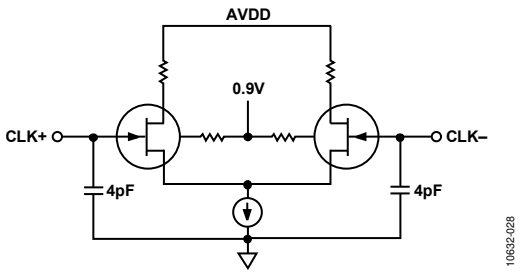

Figure 32. Equivalent Nyquist Clock Input Circuit

For applications where a single-ended low jitter clock between 40 MHz to 200 MHz is available, an RF transformer is recommended. An example using an RF transformer in the clock network is shown in Figure 33. At frequencies above 200 MHz, an RF balun is recommended, as seen in Figure 34. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD6673 to approximately 0.8 V p-p differential. This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD6673, yet preserves the fast rise and fall times of the clock, which are critical to low jitter performance.

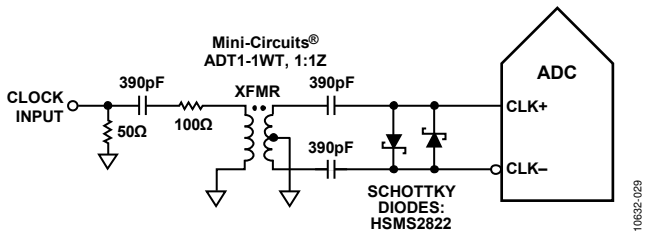

Figure 33. Transformer-Coupled Differential Clock (Up to 200 MHz)

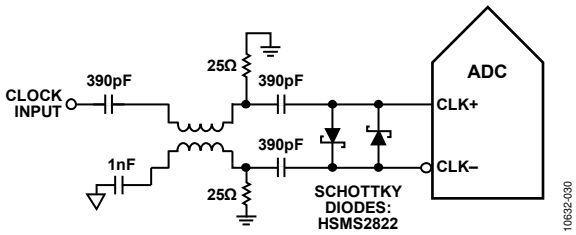

Figure 34. Balun-Coupled Differential Clock (Up to 625 MHz)

In some cases, it is desirable to buffer or generate multiple clocks from a single source. In those cases, Analog Devices, Inc., offers clock drivers with excellent jitter performance. Figure 35 shows a typical PECL driver circuit that uses PECL drivers such as the AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516-0, AD9516-1, AD9516-2, AD9516-3, AD9516-4, AD9516-5, AD9517-0, AD9517-1, AD9517-2, AD9517-3, AD9517-4, AD9518-0, AD9518-1, AD9518-2, AD9518-3, AD9518-4, AD9520-0, AD9520-1, AD9520-2, AD9520-3, AD9520-4, AD9520-5, AD9522-0, AD9522-1, AD9522-2, AD9522-3, AD9522-4, AD9522-5, AD9523, AD9524, ADCLK905, ADCLK907, and ADCLK925.

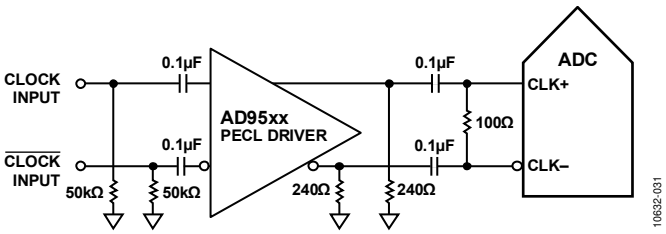

Figure 35. Differential PECL Sample Clock (Up to 625 MHz)

Analog Devices also offers LVDS clock drivers with excellent jitter performance. A typical circuit is shown in Figure 36 and uses LVDS drivers such as the AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516-0, AD9516-1, AD9516-2, AD9516-3, AD9516-4, AD9516-5, AD9517-0, AD9517-1, AD9517-2, AD9517-3, AD9517-4, AD9518-0, AD9518-1, AD9518-2, AD9518-3, AD9518-4, AD9520-0, AD9520-1, AD9520-2, AD9520-3, AD9520-4, AD9520-5, AD9522-0, AD9522-1, AD9522-2, AD9522-3, AD9522-4, AD9522-5, AD9523, and AD9524.

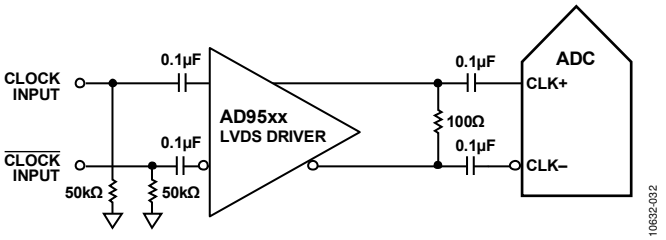

Figure 36. Differential LVDS Sample Clock (Up to 625 MHz)

RF Clock Input Options

The AD6673 RF clock input supports a single-ended clock between 625 GHz to 1.5 GHz. The equivalent RF clock input circuit is shown in Figure 37. The input is self biased to 0.9 V and is typically ac-coupled. The input has a typical input impedance of 10 kΩ in parallel with 1 pF at the RFCLK pin.

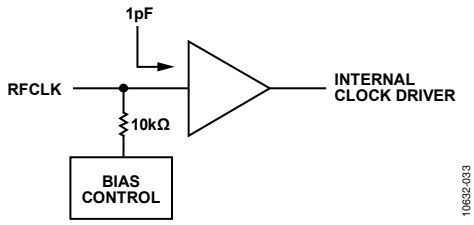

Figure 37. Equivalent RF Clock Input Circuit

It is recommended that the RF clock input of the AD6673 be driven with a PECL or sine wave signal with a minimum signal amplitude of 600 mV peak to peak. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section. Figure 38 shows the preferred method of clocking when using the RF clock input on the AD6673. It is recommended that a 50 Ω transmission line be used to route the clock signal to the RF clock input of the AD6673 due to the high frequency nature of the signal and terminate the transmission line close to the RF clock input.

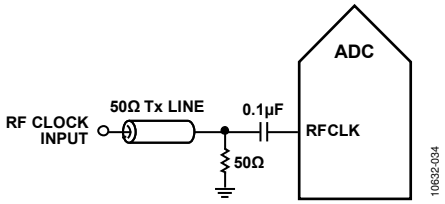

Figure 38. Typical RF Clock Input Circuit

Figure 39 shows the RF clock input of the AD6673 being driven from the LVPECL outputs of the AD9515. The differential LVPECL output signal from the AD9515 is converted to a single-ended signal using an RF balun or RF transformer. The RF balun configuration is recommended for clock frequencies associated with the RF clock input.

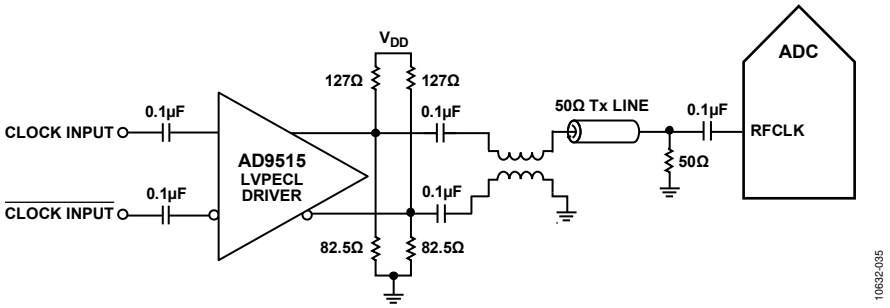

Figure 39. Differential PECL RF Clock Input Circuit

Input Clock Divider

The AD6673 contains an input clock divider with the ability to divide the Nyquist input clock by integer values between 1 and 8. The RF clock input uses an on-chip predivider to divide the clock input by four before it reaches the 1-to-8 divider. This allows for higher input frequencies to be achieved on the RF clock input. The divide ratios can be selected using Register 0x09 and Register 0x0B. Register 0x09 is used to set the RF clock input, and Register 0x0B can be used to set the divide ratio of the 1-to-8 divider for both the RF clock input and the Nyquist clock input. For divide ratios other than 1, the duty-cycle stabilizer is automatically enabled.

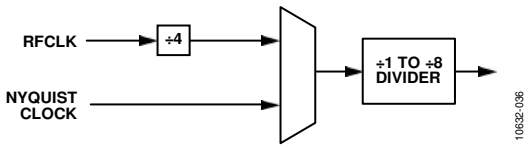

Figure 40. AD6673 Clock Divider Circuit

The AD6673 clock divider can be synchronized using the external system reference (SYSREF) input. Bit 1 and Bit 2 of Register 0x3A allow the clock divider to be resynchronized on every SYSREF signal or only on the first signal after the register is written. A valid SYSREF causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD6673 contains a DCS that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD6673.

Jitter on the rising edge of the input clock is still of paramount concern and is not reduced by the duty cycle stabilizer. The duty cycle control loop does not function for clock rates of less than 40 MHz nominally. The loop has a time constant associated with it that must be considered when the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time that the loop is not locked, the DCS loop is bypassed, and the internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{IN}) due to jitter (t_j) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{IN} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the root-mean-square of all jitter sources, which include the clock input, the analog input signal, and the ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter, as shown in Figure 41.

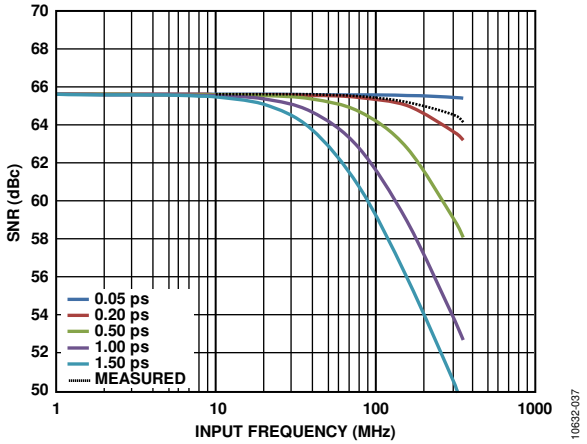

Figure 41. AD6673-250 SNR vs. Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD6673. Separate the power supplies for the clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), retime it by the original clock at the last step.

Refer to the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance*, and the AN-756 Application Note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*, for more information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 42, the power dissipated by the AD6673 is proportional to its sample rate. The data in Figure 42 was taken using the same operating conditions as those used for the Typical Performance Characteristics section.

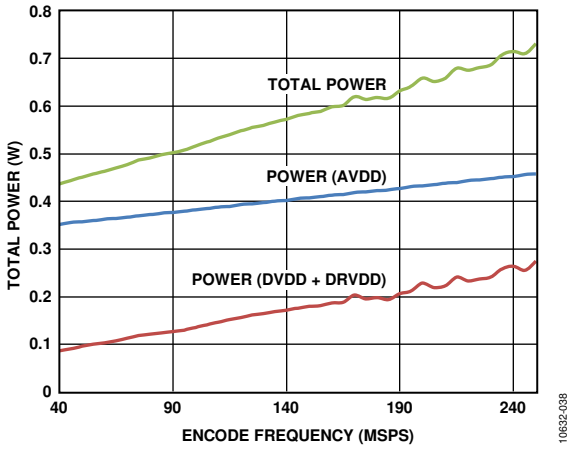

Figure 42. AD6673-250 Power vs. Encode Rate

By asserting PDWN (either through the SPI port or by asserting the PDWN pin high), the AD6673 is placed in power-down mode. In this state, the ADC typically dissipates about 9 mW. Asserting the PDWN pin low returns the AD6673 to its normal operating mode.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map Register Description section and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional details.

NOISE SHAPING REQUANTIZER

The AD6673 features a NSR to allow higher than 11-bit SNR to be maintained in a subset of the Nyquist band. The harmonic performance of the receiver is unaffected by the NSR feature. When enabled, the NSR contributes an additional 0.6 dB of loss to the input signal, such that a 0 dBFS input is reduced to −0.6 dBFS at the output pins.

The NSR feature can be independently controlled per channel via the SPI.

Two different bandwidth modes are provided; the mode can be selected from the SPI port. In each of the two modes, the center frequency of the band can be tuned such that IFs can be placed anywhere in the Nyquist band.

22% BANDWIDTH MODE (>40 MHz AT 184.32 MSPS)

The first bandwidth mode offers excellent noise performance over 22% of the ADC sample rate (44% of the Nyquist band) and can be centered by setting the NSR mode bits in the NSR control register (Address 0x3C) to 0. In this mode, the useful frequency range can be set using the 6-bit tuning word in the NSR tuning register (Address 0x3E). There are 57 possible tuning words (TW); each step is 0.5% of the ADC sample rate. The following three equations describe the left band edge (f_0), the channel center (f_{CENTER}), and the right band edge (f_1), respectively:

$$f_0 = f_{ADC} \times .005 \times TW$$

$$f_{CENTER} = f_0 + 0.11 \times f_{ADC}$$

$$f_1 = f_0 + 0.22 \times f_{ADC}$$

Figure 43 to Figure 45 show the typical spectrum that can be expected from the AD6673 in the 22% bandwidth mode for three different tuning words.

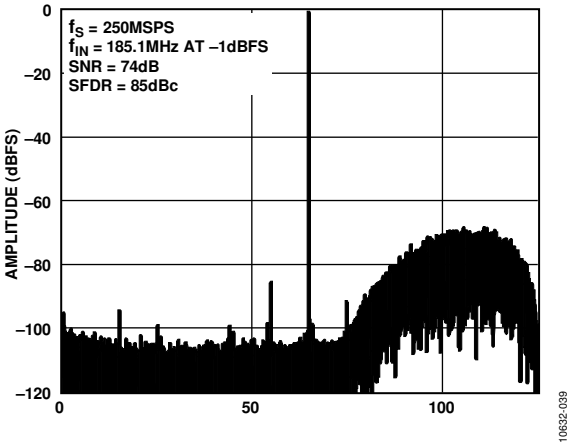

Figure 43. 22% Bandwidth Mode, Tuning Word = 13

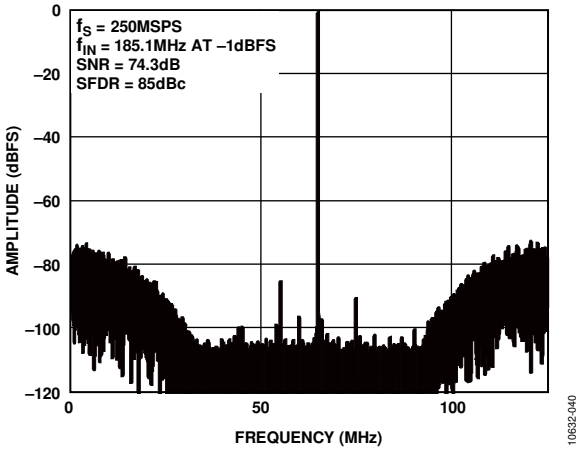

Figure 44. 22% Bandwidth Mode, Tuning Word = 28 (f_S/4 Tuning)

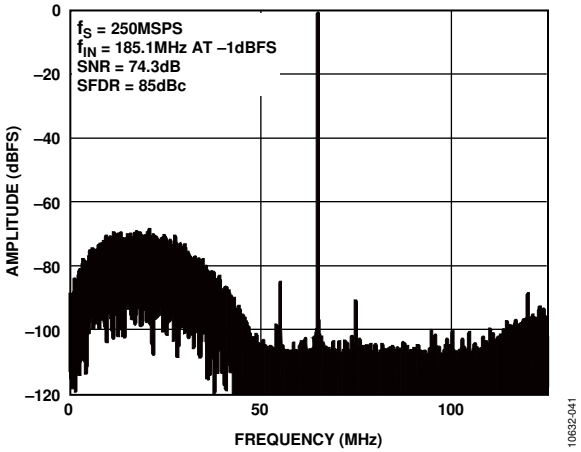

Figure 45. 22% Bandwidth Mode, Tuning Word = 41