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385 MHz BW IF Diversity Receiver

Data Sheet

AD6674

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
- In band SFDR = 83 dBFS at 340 MHz (750 MSPS)
- In band SNR = 66.7 dBFS at 340 MHz (750 MSPS)
- 1.4 W total power per channel at 750 MSPS (default settings)
- Noise density = −153 dBFS/Hz at 750 MSPS
- 1.25 V, 2.5 V, and 3.3 V dc supply operation
- Flexible input range
  - AD6674-750 and AD6674-1000
    - 1.46 V p-p to 1.94 V p-p (1.70 V p-p nominal)
  - AD6674-500
    - 1.46 V p-p to 2.06 V p-p (2.06 V p-p nominal)
- 95 dB channel isolation/crosstalk
- Amplitude detect bits for efficient automatic gain control (AGC) implementation
- Noise shaping requantizer (NSR) option for main receiver function
- Variable dynamic range (VDR) option for digital predistortion (DPD) function
- 2 integrated wideband digital processors per channel
  - 12-bit numerically controlled oscillator (NCO), up to 4 cascaded half-band filters
- Differential clock inputs
- Integer clock divide by 1, 2, 4, or 8
- Energy saving power-down modes
- Flexible JESD204B lane configurations
- Small signal dither

APPLICATIONS

- Diversity multiband, multimode digital receivers
  - 3G/4G, TD-SCDMA, W-CDMA, GSM, LTE, LTE-A
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers

GENERAL DESCRIPTION

The AD6674 is a 385 MHz bandwidth mixed-signal intermediate frequency (IF) receiver. It consists of two, 14-bit 1.0 GSPS/750 MSPS/500 MSPS analog-to-digital converters (ADC) and various digital signal processing blocks consisting of four wideband DDCs, an NSR, and VDR monitoring. It has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed to support communications applications capable of sampling wide bandwidth analog signals of up to 2 GHz. The AD6674 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

FUNCTIONAL BLOCK DIAGRAM

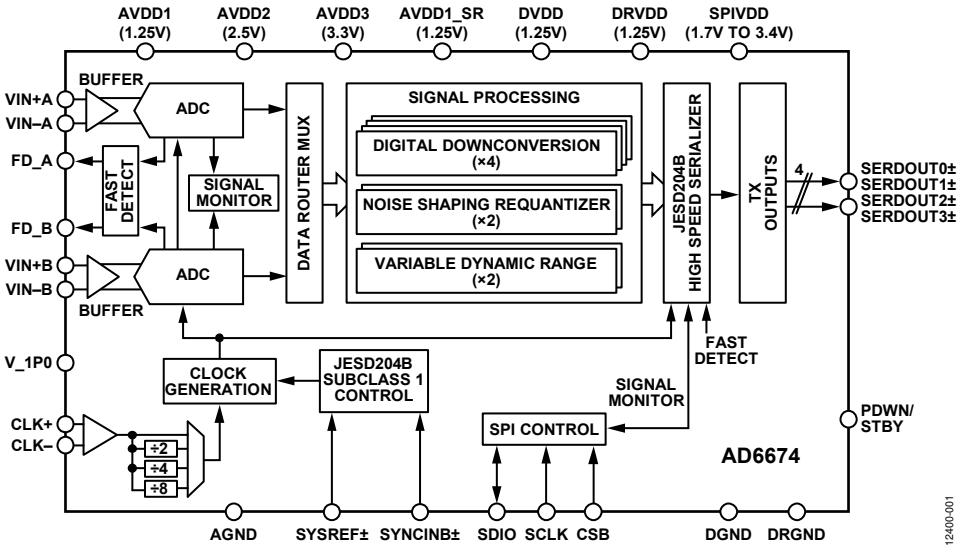

Figure 1.

Rev. C Document Feedback

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Technical Support www.analog.com

AD6674* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- [NO TITLE FOUND] EvalBoard

DOCUMENTATION

Application Notes

- AN-1371: Variable Dynamic Range

Data Sheet

- AD6674: 385 MHz BW IF Diversity Receiver Data Sheet

TOOLS AND SIMULATIONS

- AD6674 Delphi Model
- AD9680 / AD6674 IBIS Model

REFERENCE MATERIALS

Technical Articles

- MS-2714: Understanding Layers in the JESD204B Specificaton: A High Speed ADC Perspective, Part 1
- MS-2735: Maximizing the Dynamic Range of Software-Defined Radio

DESIGN RESOURCES

- AD6674 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD6674 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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12/2014—Revision A: Initial Version

The analog input and clock signals are differential inputs. The ADC data outputs are internally connected to four DDCs through a crossbar mux. Each DDC consists of up to five cascaded signal processing stages: a 12-bit frequency translator (NCO), and up to four half-band decimation filters.

Each ADC output is connected internally to an NSR block. The integrated NSR circuitry allows improved SNR performance in a smaller frequency band within the Nyquist bandwidth. The device supports two different output modes selectable via the SPI. With the NSR feature enabled, the outputs of the ADCs are processed such that the AD6674 supports enhanced SNR performance within a limited portion of the Nyquist bandwidth while maintaining a 9-bit output resolution. NSR is enabled by default on the AD6674.

Each ADC output is also connected internally to a VDR block. This optional mode allows full dynamic range for defined input signals. Inputs that are within a defined mask (based on DPD applications) are passed unaltered. Inputs that violate this defined mask result in the reduction of the output resolution.

With VDR, the dynamic range of the observation receiver is determined by a defined input frequency mask. For signals falling within the mask, the outputs are presented at the maximum resolution allowed. For signals exceeding defined power levels within this frequency mask, the output resolution is truncated. This mask is based on DPD applications and supports tunable real IF sampling, and zero IF or complex IF receive architectures.

Operation of the AD6674 between the DDC, NSR, and VDR modes is selectable via SPI-programmable profiles.

In addition to the DDC blocks, the AD6674 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect control bits in Register 0x245 of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input. Besides the fast detect outputs, the AD6674 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal being digitized by the ADC.

Users can configure the Subclasss 1 JESD204B-based high speed serialized output in a variety of two-lane and four-lane configurations, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multidevice synchronization is supported through the SYSREF± and SYNCINB± input pins.

The AD6674 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 1.8 V capable 3-wire serial port interface (SPI).

The AD6674 is available in a Pb-free, 64-lead LFCSP, specified over the −40°C to +85°C industrial temperature range. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Wide full power bandwidth supports IF sampling of signals up to 2 GHz.
2. Buffered inputs with programmable input termination eases filter design and implementation.
3. Four integrated wideband decimation filters and numerically controlled oscillator (NCO) blocks supporting multiband receivers.
4. Flexible SPI controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection and signal monitoring.
6. Programmable fast overrange detection.
7. 9 mm × 9 mm 64-lead LFCSP.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference (V_{REF}), A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 1.

		AD6674-1000			AD6674-750			AD6674-500			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		14						14			Bits
ACCURACY											
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error	Full	−0.31	0	+0.31	−0.51	0	+0.42	−0.3	0	+0.3	% FSR
Offset Matching	Full		0	+0.23		0	+0.41		0	+0.3	% FSR
Gain Error	Full	−6	0	+6	−6	0	+6	−6	0	+6	% FSR
Gain Matching	Full		1	+4.5		1	+5.2		1	+5.1	% FSR
Differential Nonlinearity (DNL)	Full	−0.7	±0.5	+0.8	−0.6	±0.5	+0.8	−0.6	±0.5	+0.7	LSB
Integral Nonlinearity (INL)	Full	−5.7	±2.5	+6.9	−3.4	±2.5	+5.0	−4.5	±2.5	+5.0	LSB
TEMPERATURE DRIFT											
Offset Error	Full		−14			−9			−3		ppm/°C
Gain Error	Full		±13.8			−57			±25		ppm/°C
INTERNAL VOLTAGE REFERENCE											
Voltage	Full		1.0			1.0			1.0		V
INPUT REFERRED NOISE											
V_{REF} = 1.0 V	25°C		2.63			2.48			2.06		LSB rms
ANALOG INPUTS											
Differential Input Voltage Range (Internal V_{REF} = 1.0 V)	Full	1.46	1.70	1.94	1.46	1.70	1.94	1.46	2.06	2.06	V p-p
Common-Mode Voltage (V_{CM})	Full		2.05			2.05			2.05		V
Differential Input Capacitance[1]	Full		1.5			1.5			1.5		pF
Analog Full Power Bandwidth	Full		2			2			2		GHz
POWER SUPPLY											
AVDD1	Full	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	V
AVDD2	Full	2.44	2.50	2.56	2.44	2.50	2.56	2.44	2.50	2.56	V
AVDD3	Full	3.2	3.3	3.4	3.2	3.3	3.4	3.2	3.3	3.4	V
AVDD1_SR	Full	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	V
DVDD	Full	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	V
DRVDD	Full	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	V
SPIVDD	Full	1.7	1.8	3.4	1.7	1.8	3.4	1.7	1.8	3.4	V
I_{AVDD1}[2]	Full		685	721		545	623		427	466	mA
I_{AVDD2}[2]	Full		595	677		460	572		398	463	mA
I_{AVDD3}[2]	Full		125	142		125	142		89	100	mA
I_{AVDD1_SR}[2]	Full		16	18		10	17		10	18	mA
I_{DVDD}[2]	Full		263	292		165	217		139	183	mA
I_{DRVDD}[2, 3]	Full		200	225		190	258		182	237	mA
L = 2 Mode[4]	25°C		N/A[5]			N/A[5]			140		mA
I_{SPIVDD}	Full		5	6		5	7.0		5	7	mA

Parameter	Temp	AD6674-1000 Min	AD6674-1000 Typ	AD6674-1000 Max	AD6674-750 Min	AD6674-750 Typ	AD6674-750 Max	AD6674-500 Min	AD6674-500 Typ	AD6674-500 Max	Unit
POWER CONSUMPTION											
Total Power Dissipation[2]	Full		3.3	3.6		2.8	3.1		2.24	2.5	W
Power-Down Dissipation	Full		835			835			710		mW
Standby[6]	Full		1.4			1.4			1.2		W

[1] Differential capacitance is measured between the VIN+x and VIN−x pins (x = A, B).
[2] Measured with a low input frequency, full-scale sine wave.
[3] All lanes running. Power dissipation on DRVDD changes with lane rate and number of lanes used.
[4] L is the number of lanes per converter device (lanes per link).
[5] N/A means not applicable. At the maximum sample rate, it is not applicable to use L = 2 mode on the JESD204B output interface because this exceeds the maximum lane rate of 12.5 Gbps. L = 2 mode is supported when the equation ((M × N´ × (10/8) × f_{OUT})/L) results in a lane rate that is ≤12.5 Gbps. f_{OUT} is the output sample rate and is denoted by f_S/DCM, where DCM = decimation ratio.
[6] Can be controlled by the SPI.

AC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter[1]	Temp	AD6674-1000 Min	AD6674-1000 Typ	AD6674-1000 Max	AD6674-750 Min	AD6674-750 Typ	AD6674-750 Max	AD6674-500 Min	AD6674-500 Typ	AD6674-500 Max	Unit
ANALOG INPUT FULL SCALE	Full		1.7			1.7			2.06		V p-p
NOISE DENSITY[2]	Full		−154			−153			−153		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[3]											
VDR Mode (Input Mask Not Triggered)											
f_{IN} = 10 MHz	25°C		67.2			67.3			69.2		dBFS
f_{IN} = 170 MHz	Full	65.1	66.6		65.8	67.1		67.8	69.0		dBFS
f_{IN} = 340 MHz	25°C		65.3			66.7			68.6		dBFS
f_{IN} = 450 MHz	25°C		64.0			66.2			68.0		dBFS
f_{IN} = 765 MHz	25°C		62.4			64.3			64.4		dBFS
f_{IN} = 985 MHz	25°C		61.4			63.6			63.8		dBFS
f_{IN} = 1950 MHz	25°C		57.0			59.9			60.5		dBFS
NSR Enabled (21% BW Mode)[4]											
f_{IN} = 10 MHz	25°C		73.8			74.0			75.2		dBFS
f_{IN} = 170 MHz	25°C		73.6			73.8			75.2		dBFS
f_{IN} = 340 MHz	25°C		73.5			73.7			74.8		dBFS
f_{IN} = 450 MHz	25°C		71.9			72.2			74.2		dBFS
f_{IN} = 765 MHz	25°C		69.0			71.4			70.3		dBFS
f_{IN} = 985 MHz	25°C		68.2			71.0			69.3		dBFS
f_{IN} = 1950 MHz	25°C		63.6			66.6			65.3		dBFS
NSR Enabled (28% BW Mode)[4]											
f_{IN} = 10 MHz	25°C		72.4			72.8			72.4		dBFS
f_{IN} = 170 MHz	25°C		72.2			72.6			72.4		dBFS
f_{IN} = 340 MHz	25°C		72.1			72.5			72.1		dBFS
f_{IN} = 450 MHz	25°C		70.5			71.0			71.9		dBFS
f_{IN} = 765 MHz	25°C		67.0			70.0			68.3		dBFS
f_{IN} = 985 MHz	25°C		66.3			68.9			67.7		dBFS
f_{IN} = 1950 MHz	25°C		61.9			65.1			64.1		dBFS

Parameter[1]	Temp	AD6674-1000 Min	AD6674-1000 Typ	AD6674-1000 Max	AD6674-750 Min	AD6674-750 Typ	AD6674-750 Max	AD6674-500 Min	AD6674-500 Typ	AD6674-500 Max	Unit
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)[3]											
VDR Mode (Input Mask Not Triggered)											
f_{IN} = 10 MHz	25°C		67.1			67.1			69.0		dBFS
f_{IN} = 170 MHz	Full	65.0	66.4		65.6	67.0		67.6	68.8		dBFS
f_{IN} = 340 MHz	25°C		65.2			66.5			68.4		dBFS
f_{IN} = 450 MHz	25°C		63.8			66.1			67.9		dBFS
f_{IN} = 765 MHz	25°C		62.1			64.1			64.2		dBFS
f_{IN} = 985 MHz	25°C		61.1			63.1			63.6		dBFS
f_{IN} = 1950 MHz	25°C		56.0			59.0			60.3		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)[3]											
VDR Mode (Input Mask Not Triggered)											
f_{IN} = 10 MHz	25°C		10.8			10.8			11.2		Bits
f_{IN} = 170 MHz	Full	10.5	10.7		10.4	10.8		10.8	11.1		Bits
f_{IN} = 340 MHz	25°C		10.5			10.7			11.1		Bits
f_{IN} = 450 MHz	25°C		10.3			10.5			11.0		Bits
f_{IN} = 765 MHz	25°C		10.0			10.4			10.4		Bits
f_{IN} = 985 MHz	25°C		9.8			10.2			10.3		Bits
f_{IN} = 1950 MHz	25°C		9.0			9.5			9.7		Bits
SPURIOUS FREE DYNAMIC RANGE (SFDR), SECOND OR THIRD HARMONIC[3]											
VDR Mode (Input Mask Not Triggered)											
f_{IN} = 10 MHz	25°C		88			85			83		dBFS
f_{IN} = 170 MHz	Full	75	85		75	86		80	88		dBFS
f_{IN} = 340 MHz	25°C		85			83			83		dBFS
f_{IN} = 450 MHz	25°C		82			82			81		dBFS
f_{IN} = 765 MHz	25°C		82			80			80		dBFS
f_{IN} = 985 MHz	25°C		80			76			75		dBFS
f_{IN} = 1950 MHz	25°C		68			68			70		dBFS
WORST OTHER (EXCLUDING SECOND OR THIRD HARMONIC)[3]											
VDR Mode (Input Mask Not Triggered)											
f_{IN} = 10 MHz	25°C		−95			−95			−95		dBFS
f_{IN} = 170 MHz	Full	−81	−94		−81	−89		−82	−95		dBFS
f_{IN} = 340 MHz	25°C		−88			−83			−93		dBFS
f_{IN} = 450 MHz	25°C		−86			−82			−93		dBFS
f_{IN} = 765 MHz	25°C		−81			−85			−88		dBFS
f_{IN} = 985 MHz	25°C		−82			−83			−89		dBFS
f_{IN} = 1950 MHz	25°C		−75			−80			−84		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD)[3] A_{IN1} AND A_{IN2} = −7.0 dBFS											
f_{IN1} = 185 MHz, f_{IN2} = 188 MHz	25°C		−87			−85			−88		dBFS
f_{IN1} = 338 MHz, f_{IN2} = 341 MHz	25°C		−88			−83			−88		dBFS
CROSSTALK[5]	25°C		95			95			95		dB
FULL POWER BANDWIDTH	25°C		2			2			2		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Noise density is measured at low analog input frequency (30 MHz).
[3] See Table 10 for recommended device settings to achieve stated typical performance.
[4] When NSR is activated on the AD6674-750 and AD6674-1000, the decimating half-band filter is also enabled.
[5] Crosstalk is measured at 185 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel.

DIGITAL SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Temp	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	600	1200	1800	mV p-p
Input Common-Mode Voltage	Full		0.85		V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
SYSTEM REFERENCE INPUTS (SYSREF+, SYSREF−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance (Differential)	Full			2.5	pF
LOGIC INPUTS (SDIO, SCLK, CSB, PDWN/STBY)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8 × SPIVDD			V
Logic 0 Voltage	Full	0			V
Input Resistance	Full		30		kΩ
LOGIC OUTPUT (SDIO)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage (I_{OH} = 800 µA)	Full	0.8 × SPIVDD			V
Logic 0 Voltage (I_{OL} = 50 µA)	Full	0			V
SYNC INPUTS (SYNCINB+, SYNCINB−)					
Logic Compliance	Full		LVDS/LVPECL/CMOS		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
LOGIC OUTPUTS (FD_A, FD_B)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8 × SPIVDD			V
Logic 0 Voltage	Full	0			V
Input Resistance	Full		30		kΩ
DIGITAL OUTPUTS (SERDOUTx±, x = 0 TO 3)					
Logic Compliance	Full		CML		
Differential Output Voltage	Full	360		770	mV p-p
Output Common-Mode Voltage (V_{CM})					
AC-Coupled	25°C	0		1.8	V
Short-Circuit Current (I_{DSHORT})	25°C	−100		+100	mA
Differential Return Loss (RL_{DIFF})[1]	25°C	8			dB
Common-Mode Return Loss (RL_{CM})[1]	25°C	6			dB
Differential Termination Impedance	Full	80	100	120	Ω

[1] Differential and common-mode return loss is measured from 100 MHz to 0.75 × baud rate.

SWITCHING SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 4.

		AD6674-1000			AD6674-750			AD6674-500			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK											
Clock Rate (at CLK+/CLK− Pins)	Full	0.3		4	0.3		4	0.3		4	GHz
Maximum Sample Rate[1]	Full	1000			750			500			MSPS
Minimum Sample Rate[2]	Full	300			300			300			MSPS
Clock Pulse Width High	Full	500			666.67			1000			ps
Clock Pulse Width Low	Full	500			666.67			1000			ps
OUTPUT PARAMETERS											
Unit Interval (UI)[3]	Full		100			133.33			200		ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)	25°C		32			32			32		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)	25°C		32			32			32		ps
PLL Lock Time	25°C		2			2			2		ms
Data Rate per Channel (NRZ)[4]	25°C	3.125	10	12.5	3.125	7.5	12.5	3.125	5	12.5	Gbps
LATENCY											
Pipeline Latency	Full		75			75			75		Clock cycles
Fast Detect Latency	Full			28			28			28	Clock cycles
Wake-Up Time (Standby)[5]	25°C		1			1			1		ms
Wake-Up Time (Power-Down)[5]	25°C			4			4			4	ms
APERTURE											
Aperture Delay (t_A)	Full		530			530			530		ps
Aperture Uncertainty (Jitter, t_J)	Full		55			55			55		fs rms
Out-of-Range Recovery Time	Full		1			1			1		Clock cycles

[1] The maximum sample rate is the clock rate after the divider.
[2] The minimum sample rate operates at 300 MSPS with L = 2 or L = 1.
[3] Baud rate = 1/UI. A subset of this range can be supported.
[4] At full baud rate (12.5 Gbps), each ADC outputs data on two differential pair lanes.
[5] Wake-up time is defined as the time required to return to normal operation from power-down mode or standby mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Unit**
CLK± to SYSREF± TIMING REQUIREMENTS					
t_{SU_SR}	Device clock to SYSREF± setup time		117		ps
t_{H_SR}	Device clock to SYSREF± hold time		−96		ps
SPI TIMING REQUIREMENTS	See Figure 4				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK is in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK is in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between the falling edge of SCLK and the output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 4)	10			ns

Timing Diagrams

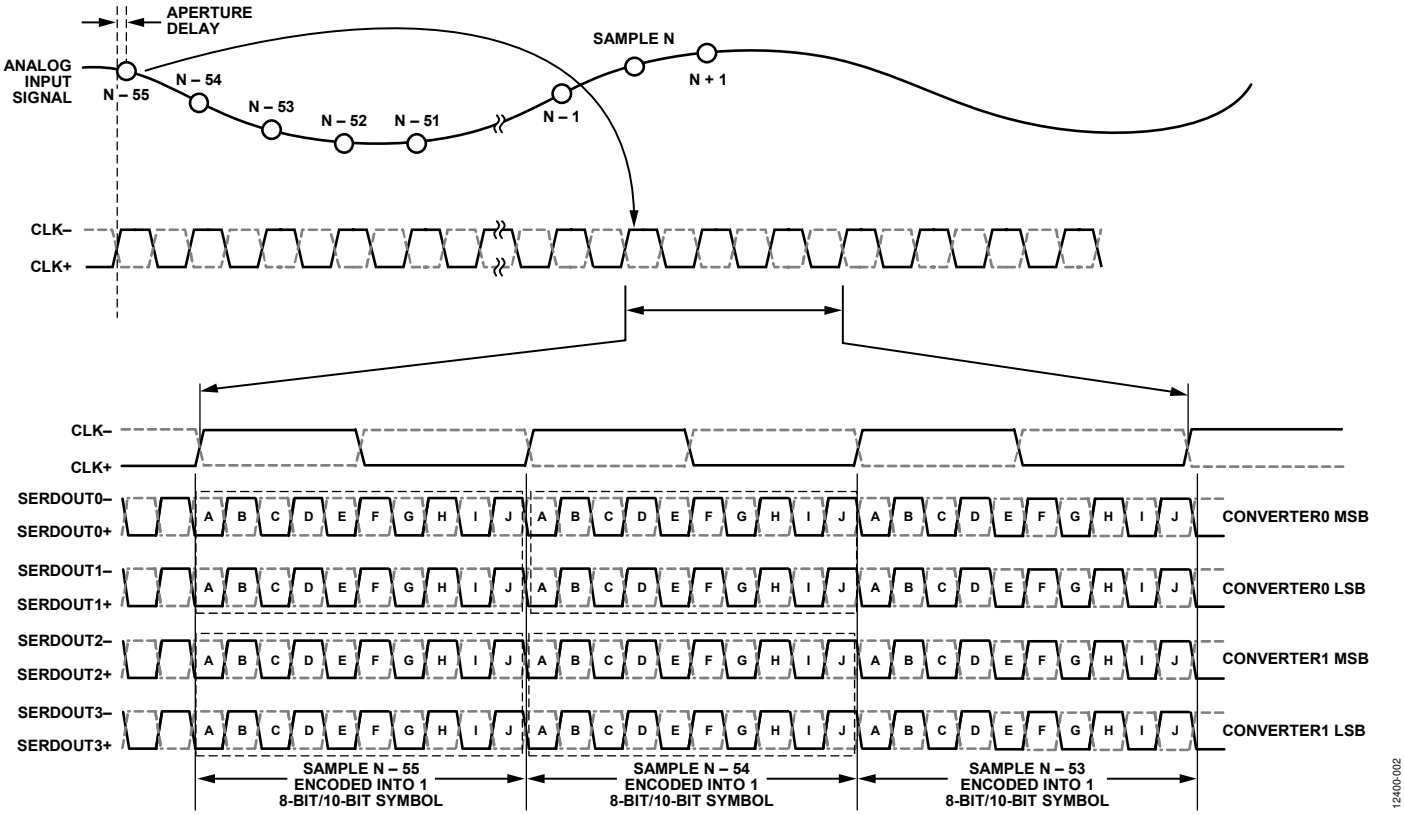


Figure 2. Data Output Timing (VDR Mode; L = 4; M = 2; F = 1)

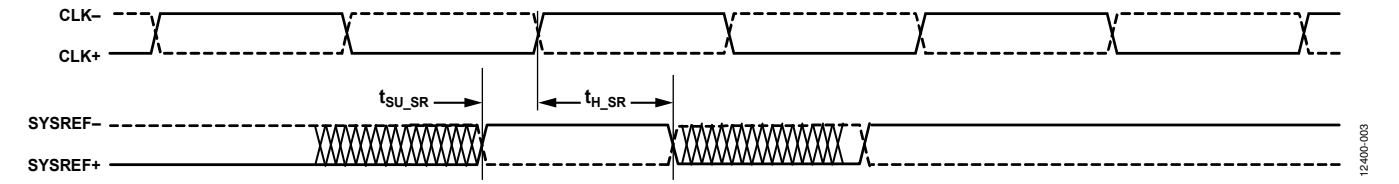


Figure 3. SYSREF± Setup and Hold Timing

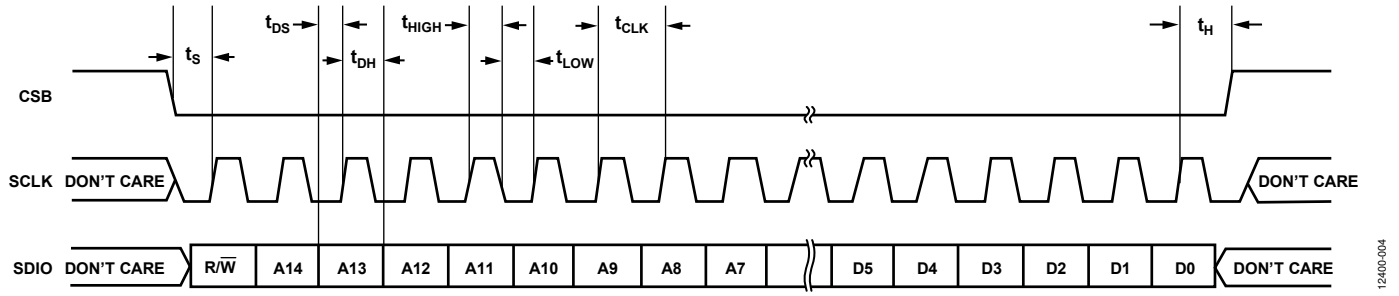


Figure 4. Serial Port Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.32 V
AVDD1_SR to AGND	1.32 V
AVDD2 to AGND	2.75 V
AVDD3 to AGND	3.63 V
DVDD to DGND	1.32 V
DRVDD to DRGND	1.32 V
SPIVDD to AGND	3.63 V
AGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	3.2 V
SCLK, SDIO, CSB to AGND	−0.3 V to SPIVDD + 0.3 V
PDWN/STBY to AGND	−0.3 V to SPIVDD + 0.3 V
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−40°C to +115°C
Storage Temperature Range (Ambient)	−60°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA}, Ψ_{JB}, and θ_{JC} are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation, effectively reducing θ_{JA} and Ψ_{JB}. In addition, metal in direct contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes reduces the θ_{JA}. Thermal performance for actual applications requires careful inspection of the conditions in an application. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 6.

Table 7. Thermal Resistance Values

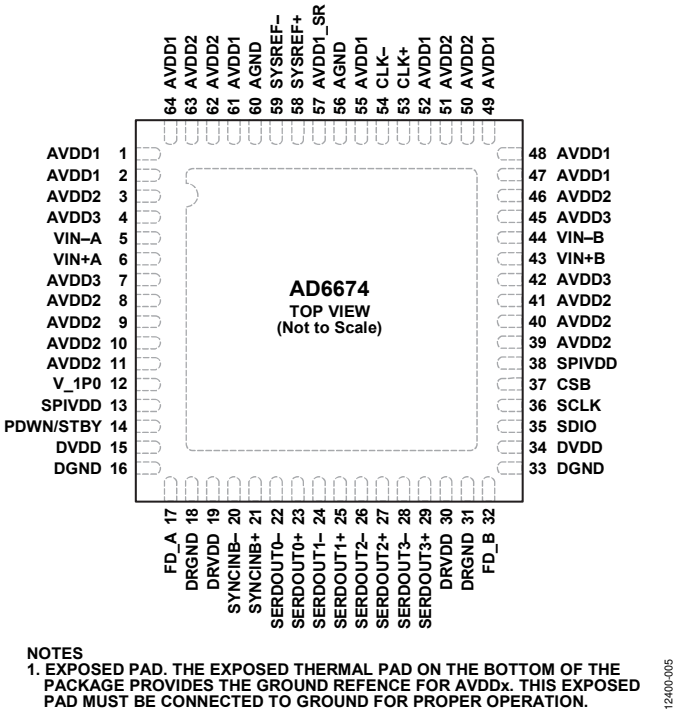
PCB Type	Airflow Velocity (m/sec)	θ_{JA}	Ψ_{JB}	θ_{JC_TOP}	θ_{JC_BOT}	Unit
JEDEC 2s2p Board	0.0	17.8[1, 2]	6.3[1, 3]	4.7[1, 5]	1.2[1, 5]	°C/W
	1.0	15.6[1, 2]	5.9[1, 3]	N/A[4]		°C/W
	2.5	15.0[1, 2]	5.7[1, 3]	N/A[4]		°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per JEDEC JESD51-8 (still air).
[4] N/A means not applicable.
[5] Per MIL-STD 883, Method 1012.1.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE GROUND REFENCE FOR AVDDx. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
Power Supplies			
0	EPAD	Ground	Exposed Pad. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDx. This exposed pad must be connected to ground for proper operation. See the Applications Information section for more details.
1, 2, 47, 48, 49, 52, 55, 61, 64	AVDD1	Supply	Analog Power Supply (1.25 V Nominal).
3, 8, 9, 10, 11, 39, 40, 41, 46, 50, 51, 62, 63	AVDD2	Supply	Analog Power Supply (2.5 V Nominal).
4, 7, 42, 45	AVDD3	Supply	Analog Power Supply (3.3 V Nominal).
13, 38	SPIVDD	Supply	Digital Power Supply for SPI (1.7 V to 3.4 V).
15, 34	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
16, 33	DGND	Ground	Ground Reference for DVDD.
18, 31	DRGND	Ground	Ground Reference for DRVDD.
19, 30	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
56, 60	AGND[1]	Ground	Ground Reference for SYSREF±.
57	AVDD1_SR[1]	Supply	Analog Power Supply for SYSREF± (1.25 V Nominal).
Analog			
5, 6	VIN–A, VIN+A	Input	ADC A Analog Input Complement/True.
12	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or an input. Do not connect this pin if using the internal reference. This pin requires a 1.0 V reference voltage input if using an external voltage reference source.
43, 44	VIN+B, VIN–B	Input	ADC B Analog Input True/Complement.
53, 54	CLK+, CLK–	Input	Clock Input True/Complement.

Pin No.	Mnemonic	Type	Description
CMOS Outputs			
17, 32	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B.
Digital Inputs			
20, 21	SYNCINB−, SYNCINB+	Input	Active Low JESD204B LVDS Sync Input True/Complement.
58, 59	SYSREF+, SYSREF−	Input	Active Low JESD204B LVDS System Reference Input True/Complement.
Data Outputs			
22, 23	SERDOUT0−, SERDOUT0+	Output	Lane 0 Output Data Complement/True.
24, 25	SERDOUT1−, SERDOUT1+	Output	Lane 1 Output Data Complement/True.
26, 27	SERDOUT2−, SERDOUT2+	Output	Lane 2 Output Data Complement/True.
28, 29	SERDOUT3−, SERDOUT3+	Output	Lane 3 Output Data Complement/True.
Device Under Test (DUT) Controls			
14	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby. This pin requires an external 10 kΩ pull-down resistor.
35	SDIO	Input/Output	SPI Serial Data Input/Output.
36	SCLK	Input	SPI Serial Clock.
37	CSB	Input	SPI Chip Select (Active Low).

[1] To ensure proper ADC operation, connect AVDD1_SR and AGND separately from the AVDD1 and EPAD connection. For more information, see the Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS

AD6674-1000

AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, A_{IN} = −1.0 dBFS, VDR mode (no violation of VDR mask), clock divider = 2, otherwise default SPI settings, T_A = 25°C, 128k FFT sample, unless otherwise noted. See Table 10 for recommended settings.

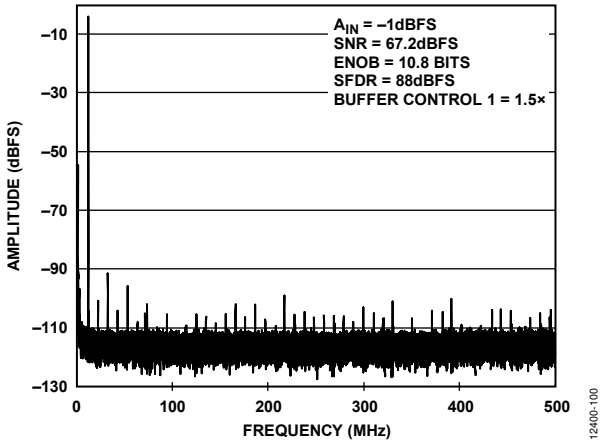


Figure 6. Single Tone FFT with f_{IN} = 10.3 MHz

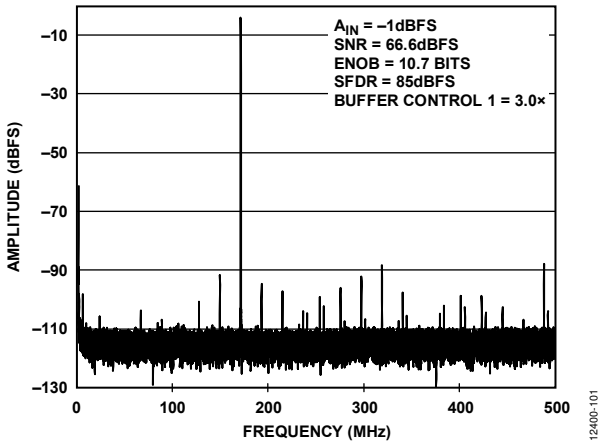


Figure 7. Single Tone FFT with f_{IN} = 170.3 MHz

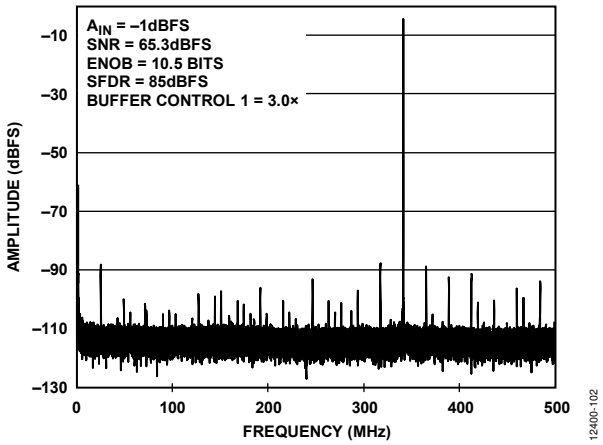


Figure 8. Single Tone FFT with f_{IN} = 340.3 MHz

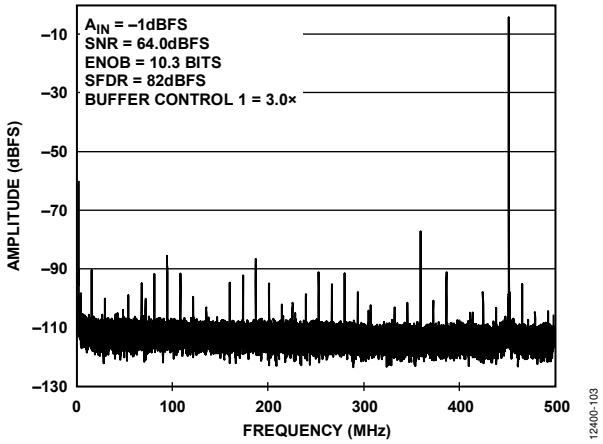


Figure 9. Single Tone FFT with f_{IN} = 450.3 MHz

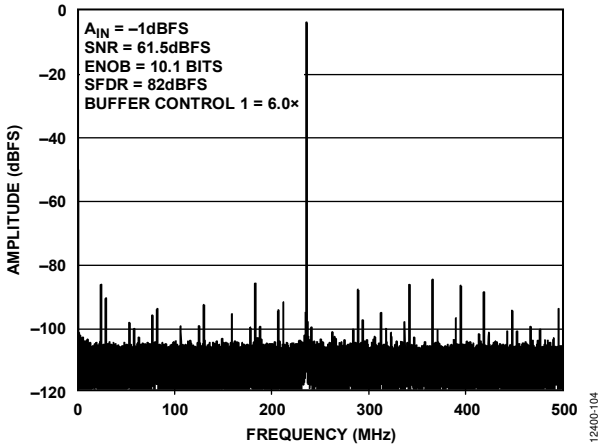


Figure 10. Single Tone FFT with f_{IN} = 765.3 MHz

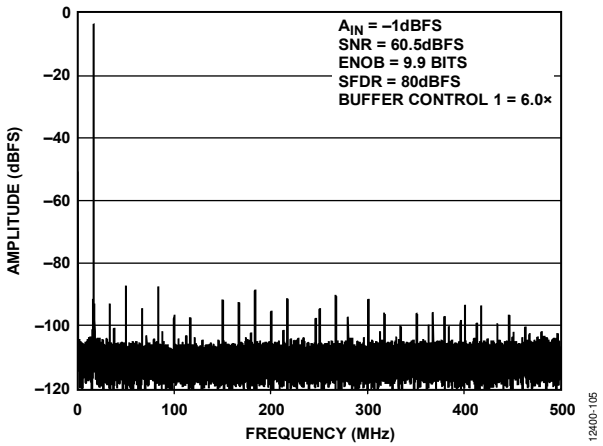


Figure 11. Single Tone FFT with f_{IN} = 985.3 MHz

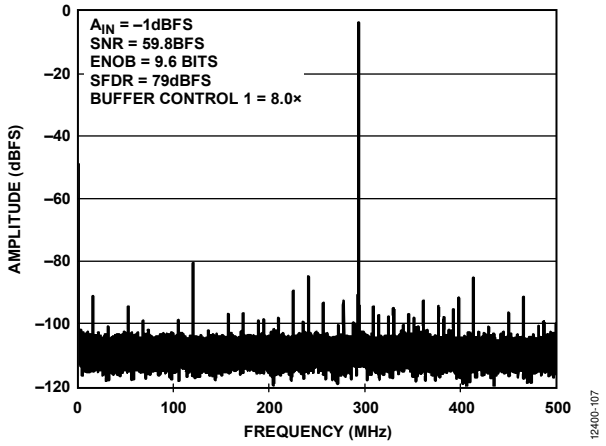


Figure 12. Single Tone FFT with f_{IN} = 1293.3 MHz

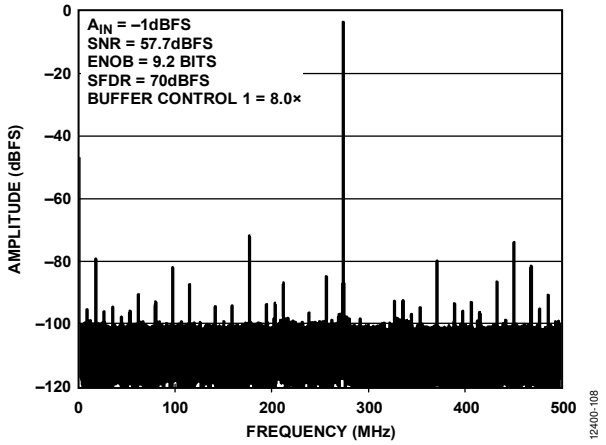


Figure 13. Single Tone FFT with f_{IN} = 1725.3 MHz

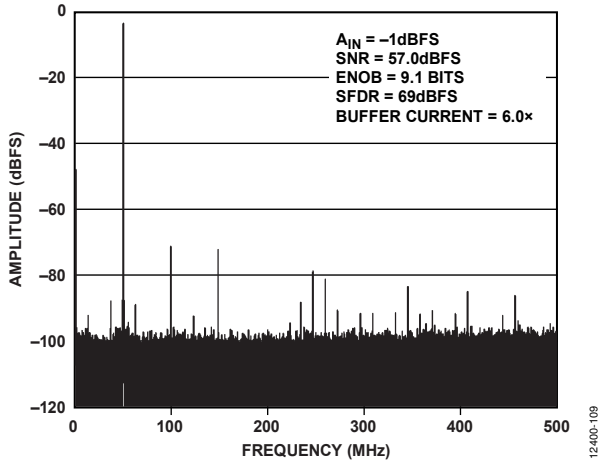


Figure 14. Single Tone FFT with f_{IN} = 1950.3 MHz

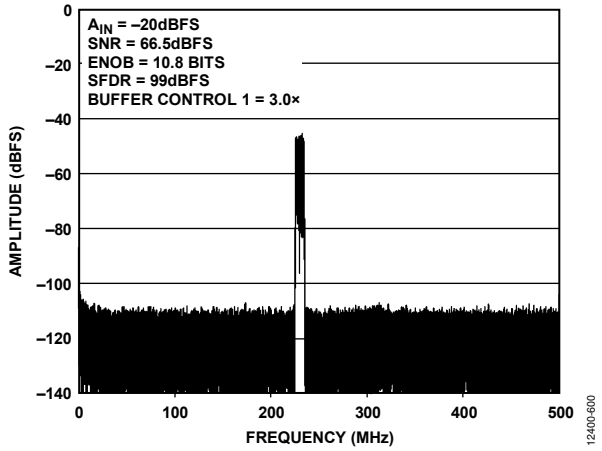


Figure 15. LTE-FDD 10 MHz Channel FFT with f_{IN} = 230 MHz

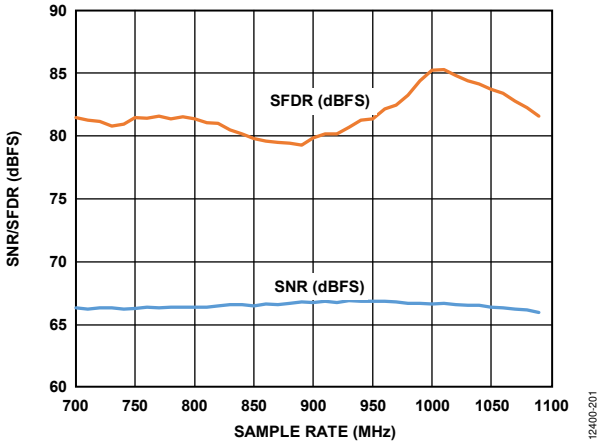


Figure 16. SNR/SFDR vs. Sample Rate (f_S), f_{IN} = 170.3 MHz; Buffer Control 1 = 3.0×

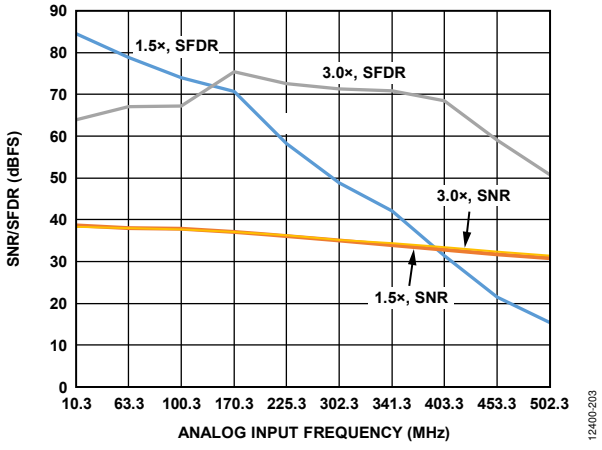


Figure 17. SNR/SFDR vs. Analog Input Frequency (f_{IN}); f_{IN} < 500 MHz; Buffer Control 1 = 1.5× and 3.0×

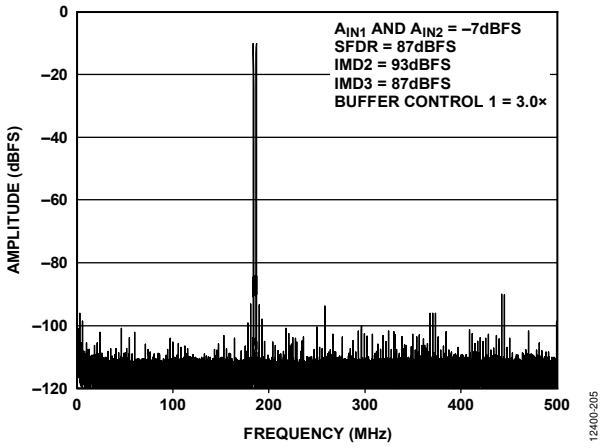


Figure 18. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

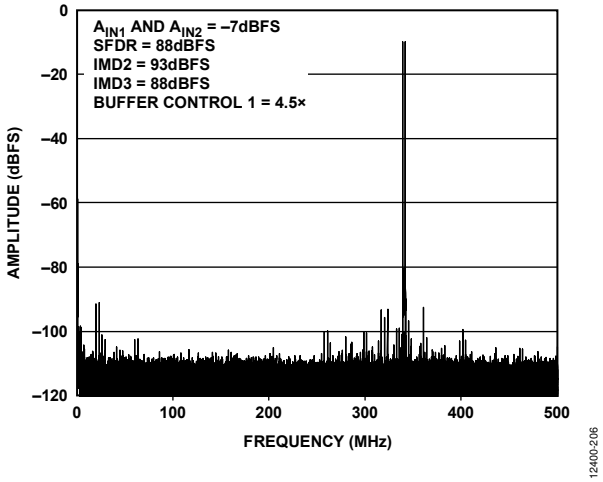


Figure 19. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

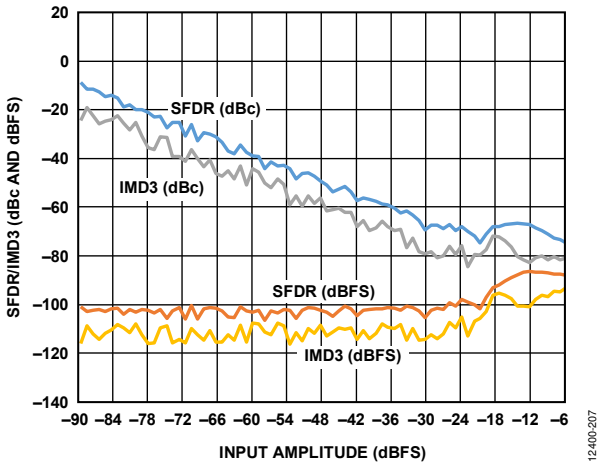


Figure 20. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

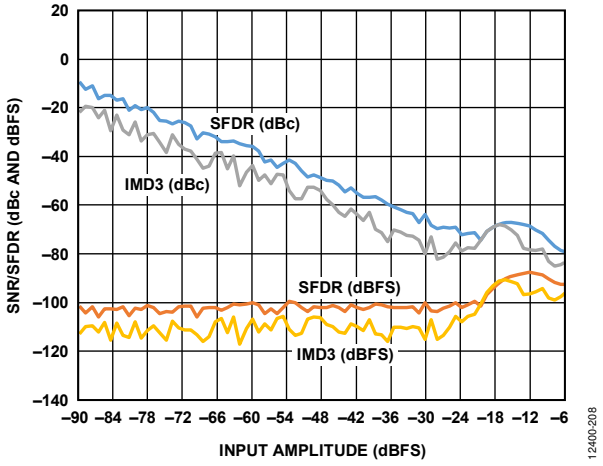


Figure 21. Two-Tone IMD3/SFDR vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz

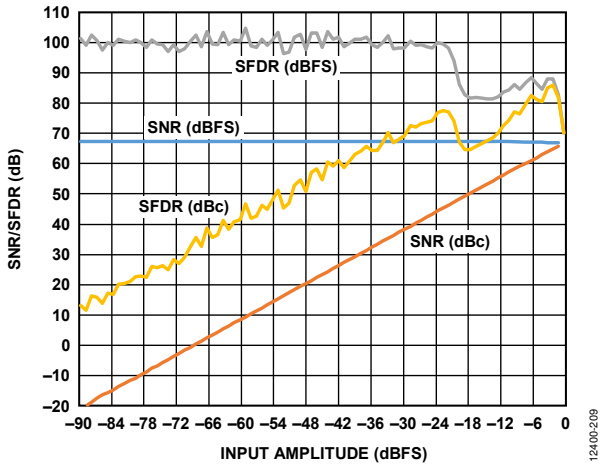


Figure 22. SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 170.3 MHz

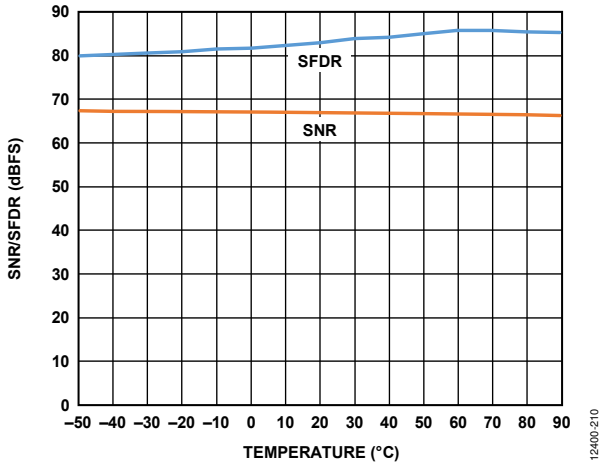


Figure 23. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

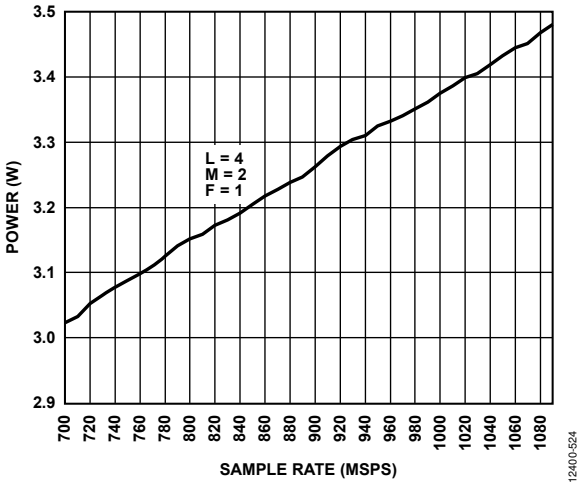


Figure 24. Power Dissipation vs. Sampel Rate (f_S) (Default SPI)

AD6674-750

AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, A_{IN} = −1.0 dBFS, VDR mode (no violation of VDR mask), clock divider = 2, otherwise default SPI settings, T_A = 25°C, 128k FFT sample, unless otherwise noted. See Table 10 for recommended settings.

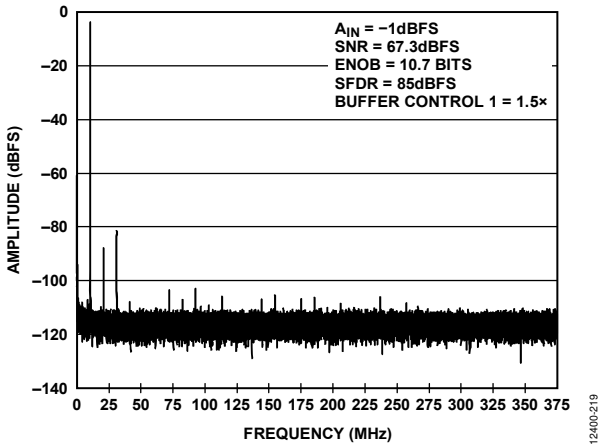


Figure 25. Single Tone FFT with f_{IN} = 10.3 MHz

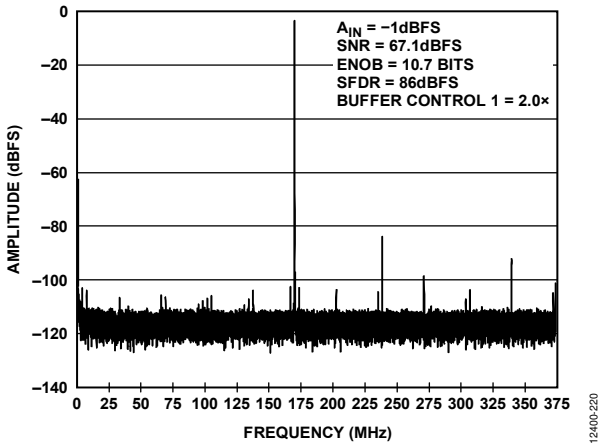


Figure 26. Single Tone FFT with f_{IN} = 170.3 MHz

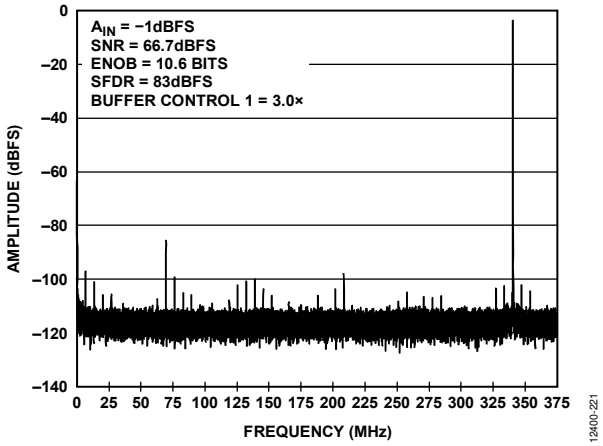


Figure 27. Single Tone FFT with f_{IN} = 340.3 MHz

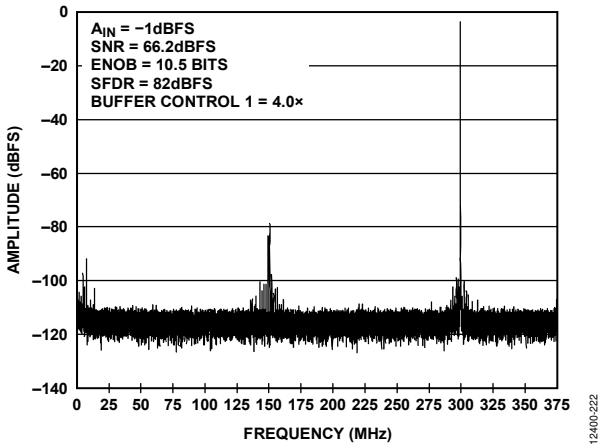


Figure 28. Single Tone FFT with f_{IN} = 450.3 MHz

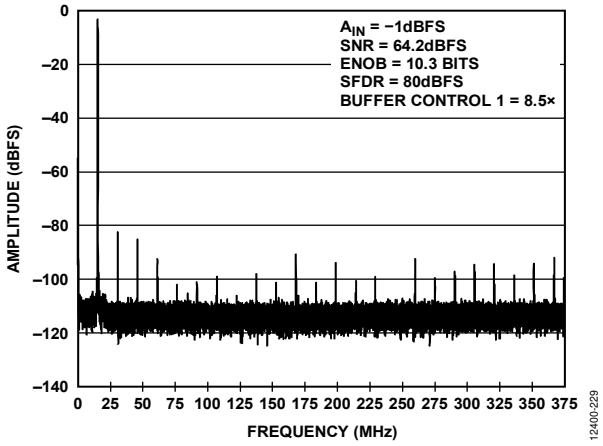


Figure 29. Single Tone FFT with f_{IN} = 765.3 MHz

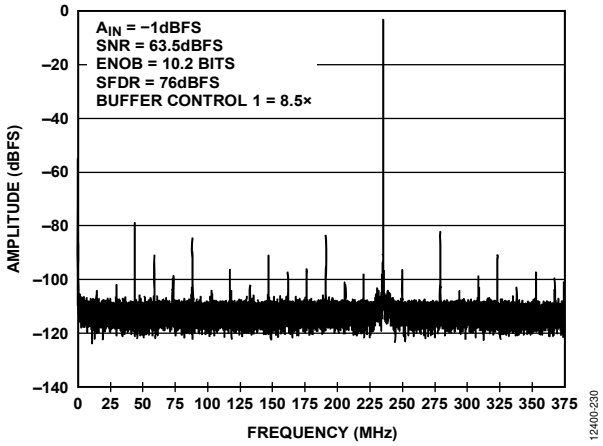


Figure 30. Single Tone FFT with f_{IN} = 985.3 MHz

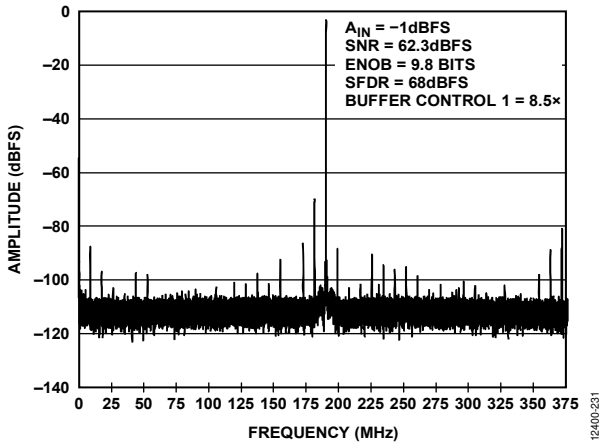


Figure 31. Single Tone FFT with f_{IN} = 1310.3 MHz

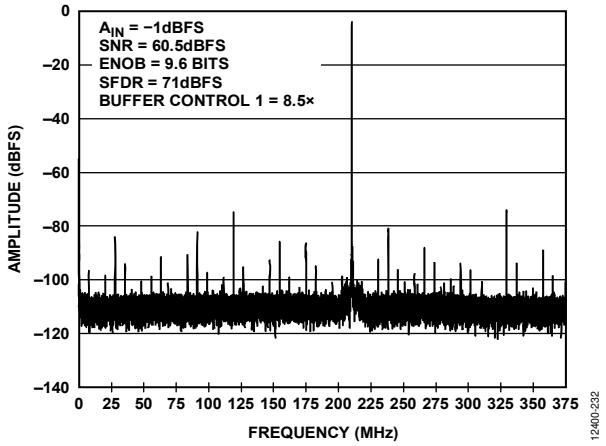


Figure 32. Single Tone FFT with f_{IN} = 1710.3 MHz

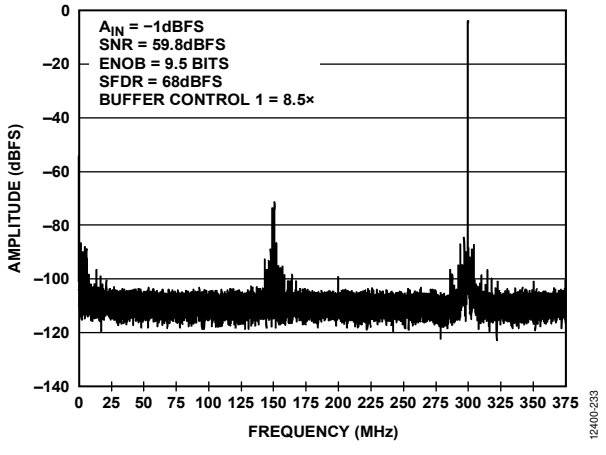


Figure 33. Single Tone FFT with f_{IN} = 1950.3 MHz

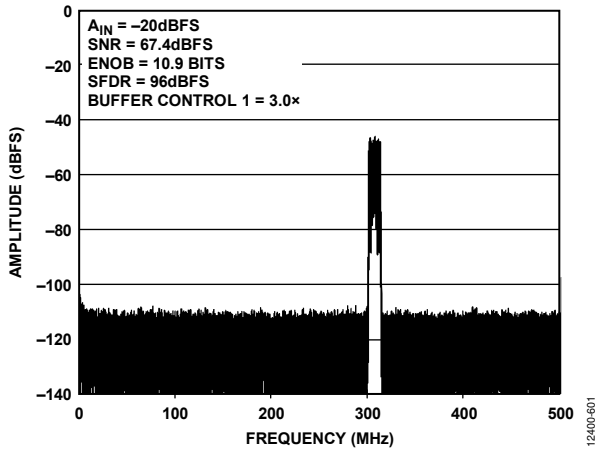


Figure 34. LTE-FDD 10 MHz Channel FFT with f_{IN} = 230 MHz

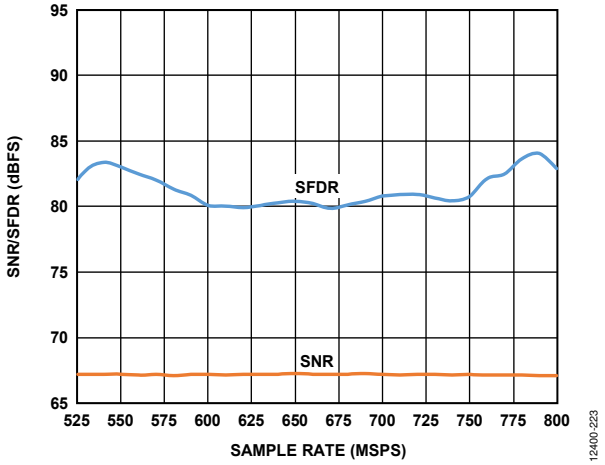


Figure 35. SNR/SFDR vs. Sample Rate (f_S); f_{IN} = 170.3 MHz, Buffer Control 1 = 3.0×

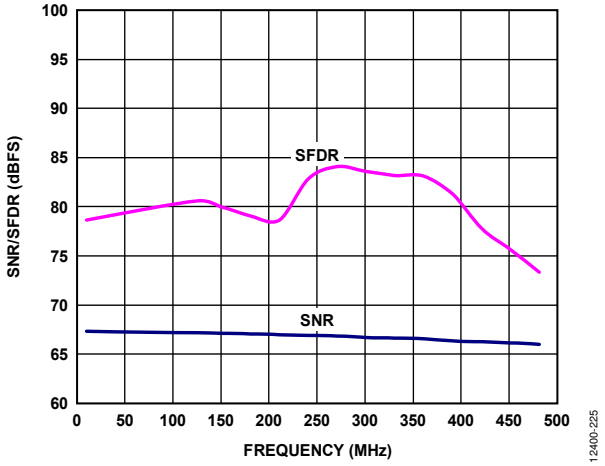


Figure 36. SNR/SFDR vs. Analog Input Frequency (f_{IN}); f_{IN} < 500 MHz; Buffer Control 1 = 3.0×

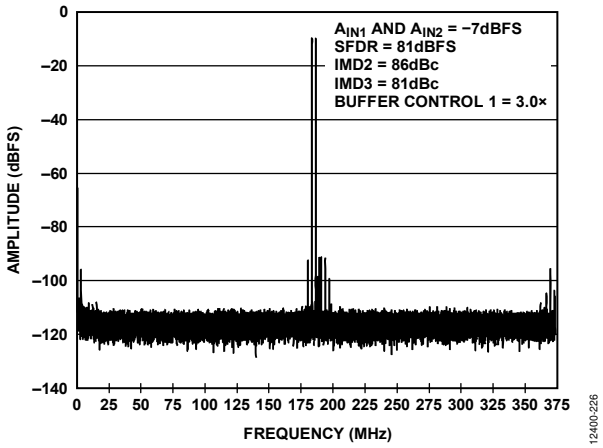


Figure 37. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

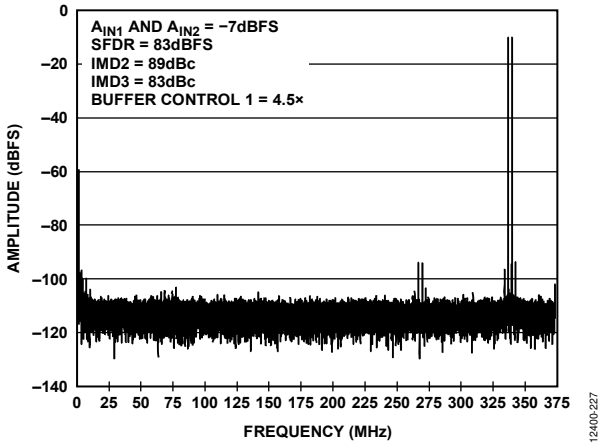


Figure 38. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

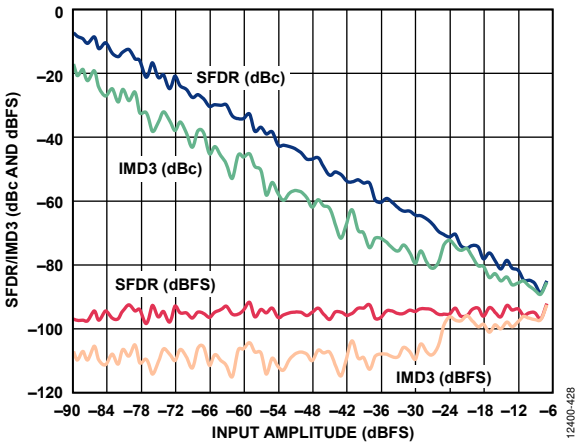


Figure 39. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

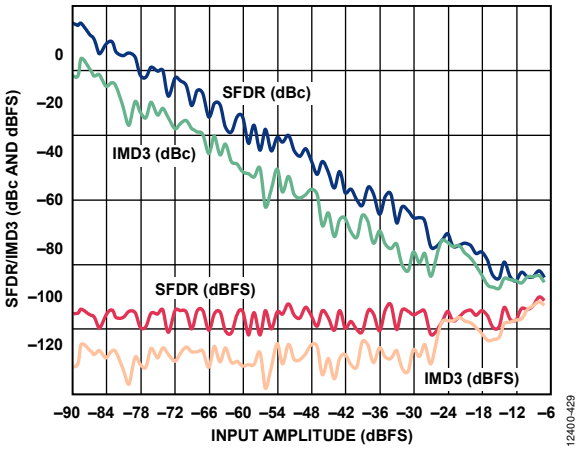


Figure 40. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz

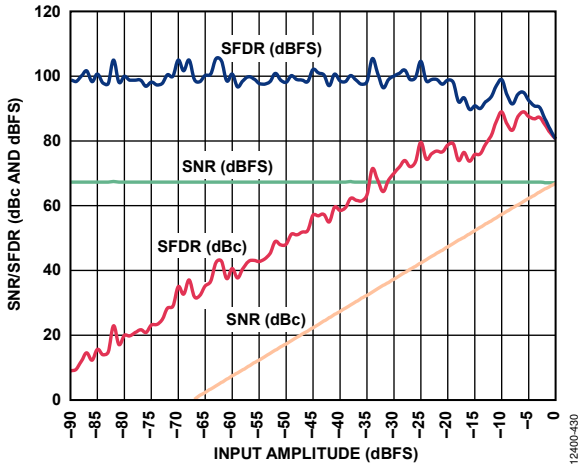


Figure 41. SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 170.3 MHz

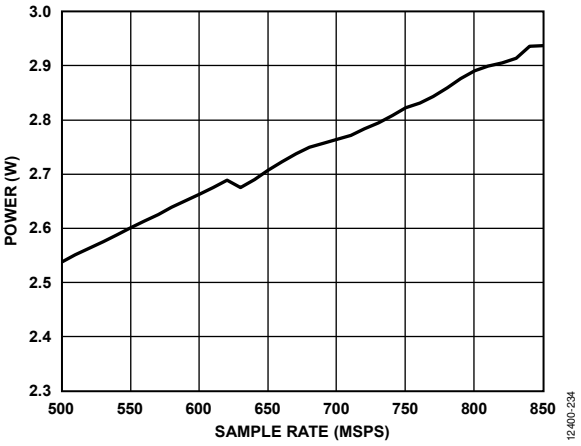


Figure 43. Power Dissipation vs. Sample Rate (f_S); L = 4, M = 2, F = 1 for $f_S \geq 625$ MSPS and L= 2, M = 2, F = 2 for $f_S < 625$ MSPS (Default SPI)

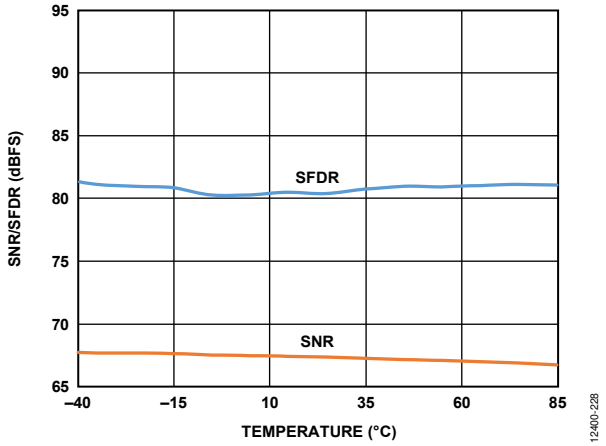


Figure 42. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

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AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, A_{IN} = −1.0 dBFS, VDR mode (no violation of VDR mask), clock divider = 2, otherwise default SPI settings, T_A = 25°C, 128k FFT sample, unless otherwise noted. See Table 10 for recommended settings.

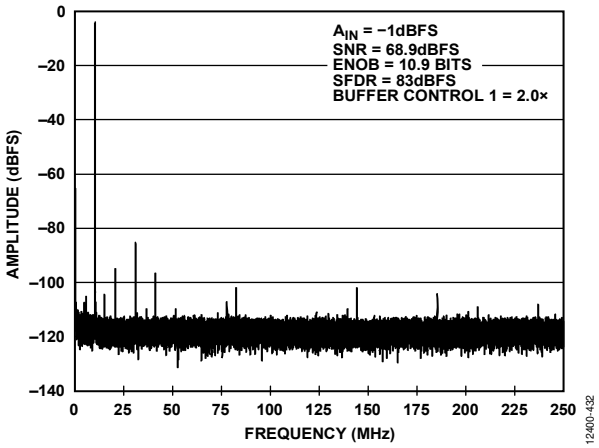

Figure 44. Single Tone FFT with f_{IN} = 10.3 MHz

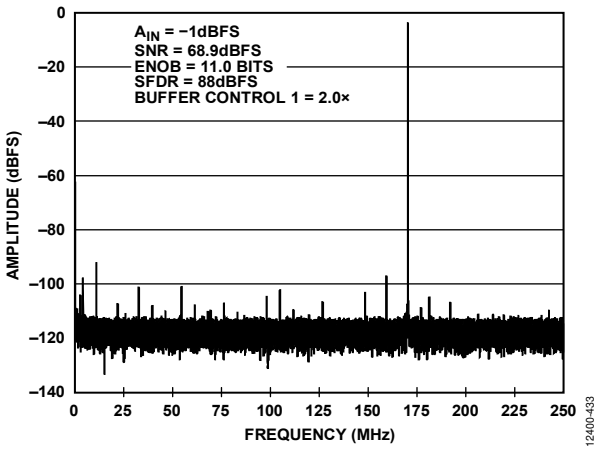

Figure 45. Single Tone FFT with f_{IN} = 170.3 MHz

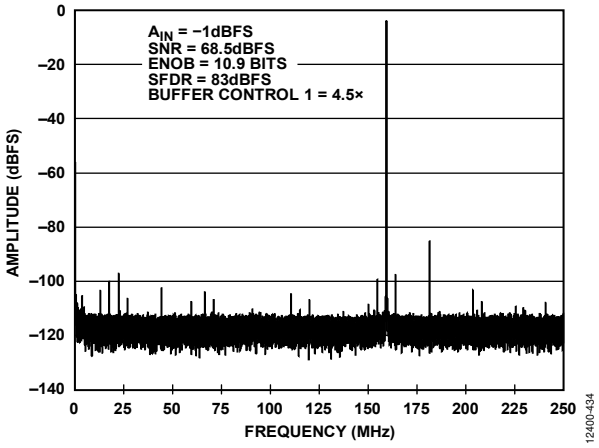

Figure 46. Single Tone FFT with f_{IN} = 340.3 MHz

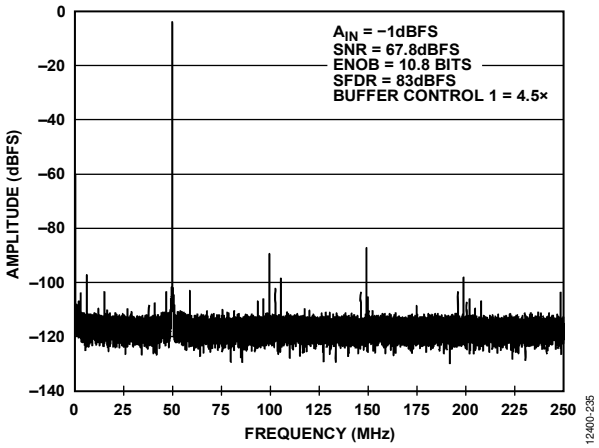

Figure 47. Single Tone FFT with f_{IN} = 450.3 MHz

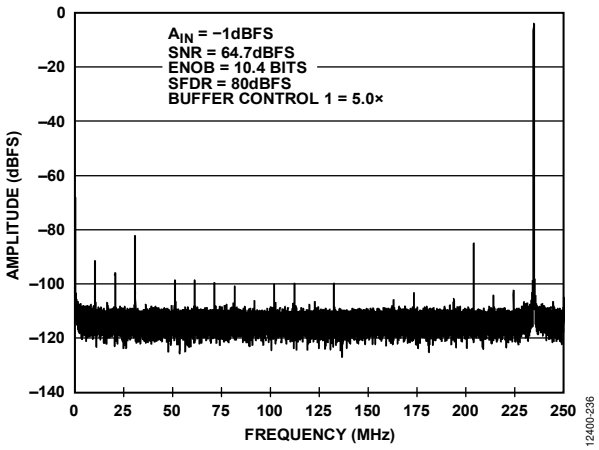

Figure 48. Single Tone FFT with f_{IN} = 765.3 MHz

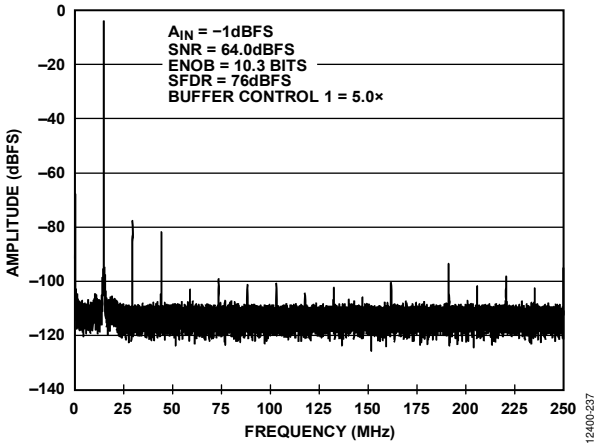

Figure 49. Single Tone FFT with f_{IN} = 985.3 MHz

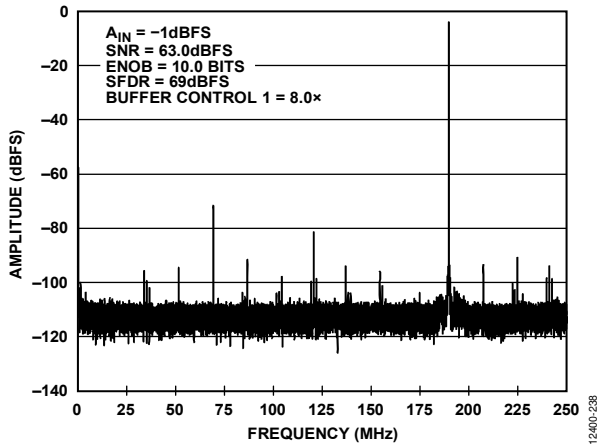

Figure 50. Single Tone FFT with f_{IN} = 1310.3 MHz

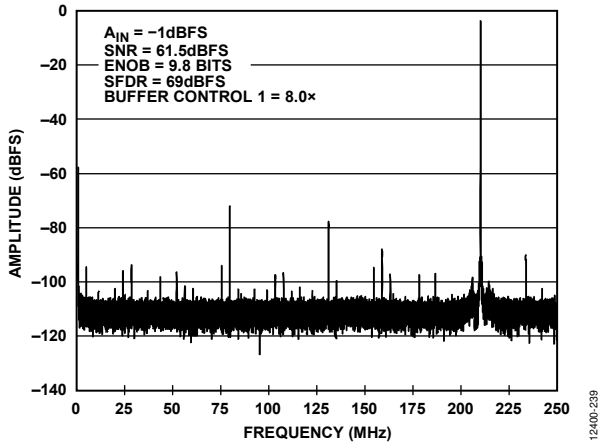

Figure 51. Single Tone FFT with f_{IN} = 1710.3 MHz

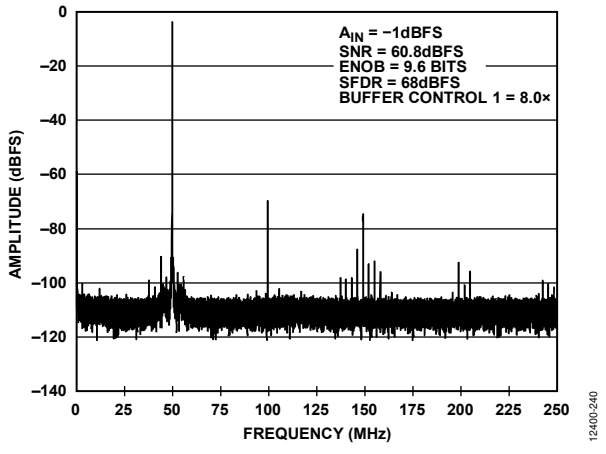

Figure 52. Single Tone FFT with f_{IN} = 1950.3 MHz

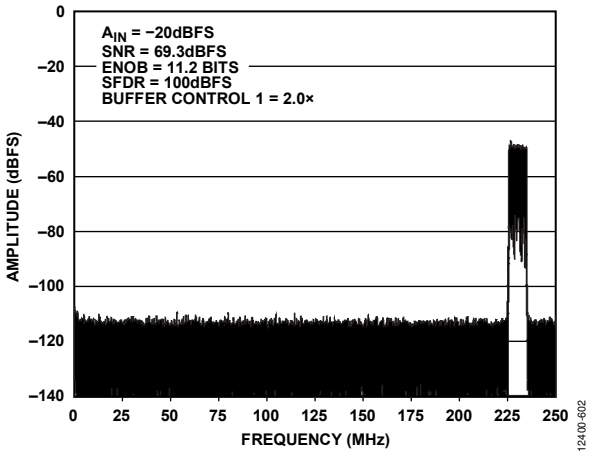

Figure 53. LTE-TDD 10 MHz Channel FFT with f_{IN} = 230 MHz

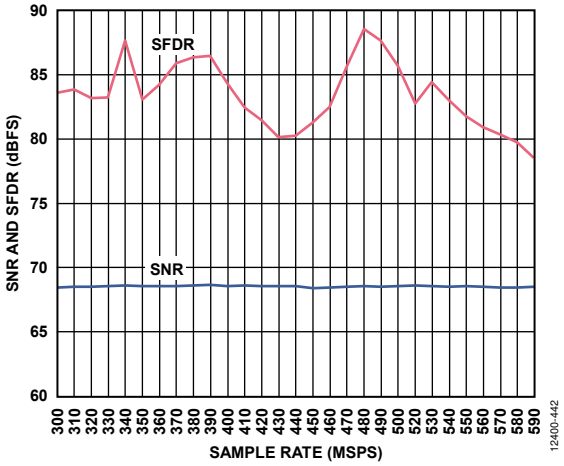

Figure 54. SNR/SFDR vs. Sample Rate (f_S), f_{IN} = 170.3 MHz; Buffer Control 1 = 2.0×

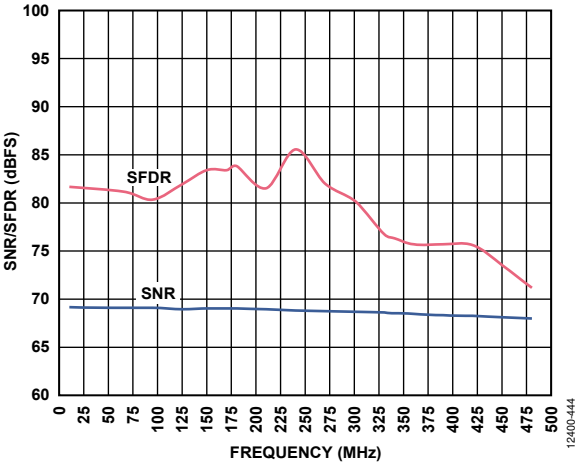

Figure 55. SNR/SFDR vs. Analog Input Frequency (f_{IN}); f_{IN} < 500 MHz; Buffer Control 1 = 3.0×

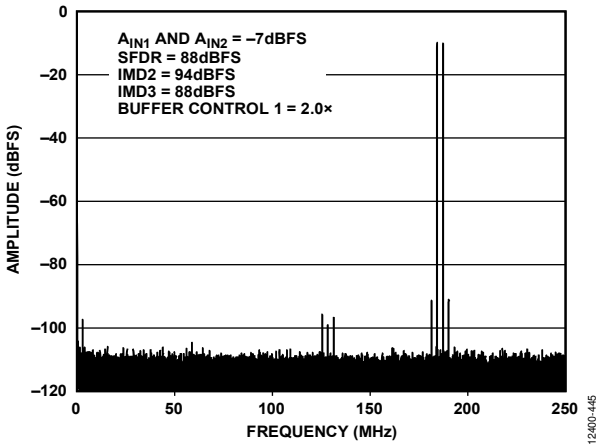

Figure 56. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

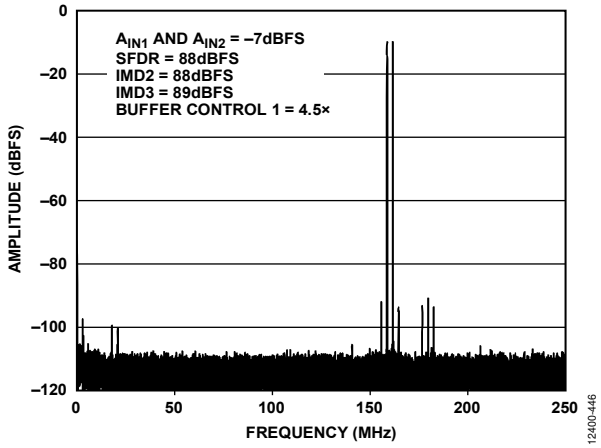

Figure 57. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

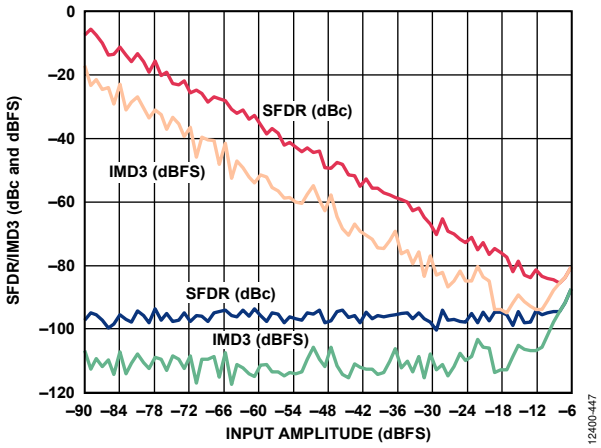

Figure 58. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

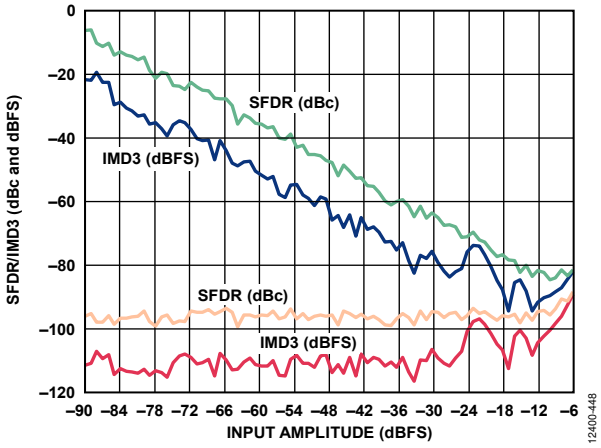

Figure 59. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz