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Wideband IF Receiver Subsystem

Data Sheet **AD6676**

FEATURES

- High instantaneous dynamic range
  - Noise figure (NF) as low as 13 dB
  - Noise spectral density (NSD) as low as −159 dBFS/Hz
  - IIP3 up to 36.9 dBm with spurious tones <−99 dBFS
- Tunable band-pass Σ-Δ analog-to-digital converter (ADC)
  - 20 MHz to 160 MHz signal bandwidth
  - 70 MHz to 450 MHz IF center frequency
  - Configurable input full-scale level of −2 dBm to −14 dBm
    - Easy to drive resistive IF input
  - Gain flatness of 1 dB with under 0.5 dB out-of-band peaking
    - Alias rejection greater than 50 dB
  - 2.0 GSPS to 3.2 GSPS ADC clock rate
    - On-chip PLL clock multiplier
  - 16-bit I/Q rate up to 266 MSPS
- On-chip digital signal processing
  - NCO and quadrature digital downconverter (QDDC)
  - Selectable decimation factor of 12, 16, 24, and 32
- Automatic gain control (AGC) support
  - On-chip attenuator with 27 dB span in 1 dB steps
  - Fast attenuator control via configurable AGC data port
  - Peak detection flags with programmable thresholds
- Single or dual lane, JESD204B capable
- Low power consumption: 1.20 W
  - 1.1 V and 2.5 V supply voltage
  - TDD power saving up to 60%
- 4.3 mm × 5.0 mm WLCSP

APPLICATIONS

- Wideband cellular infrastructure equipment and repeaters
- Point-to-point microwave equipment
- Instrumentation
  - Spectrum and communication analyzers
- Software defined radio

GENERAL DESCRIPTION

The AD6676[1] is a highly integrated IF subsystem that can digitize radio frequency (RF) bands up to 160 MHz in width centered on an intermediate frequency (IF) of 70 MHz to 450 MHz. Unlike traditional Nyquist IF sampling ADCs, the AD6676 relies on a tunable band-pass Σ-Δ ADC with a high oversampling ratio to eliminate the need for band specific IF SAW filters and gain stages, resulting in significant simplification of the wideband radio receiver architecture. On-chip quadrature digital downconversion followed by selectable decimation filters reduces the complex data rate to a manageable rate between 62.5 MSPS to 266.7 MSPS. The 16-bit complex output data is transferred to the host via a single or dual lane JESD204B interface supporting line rates of up to 5.333 Gbps.

FUNCTIONAL BLOCK DIAGRAM

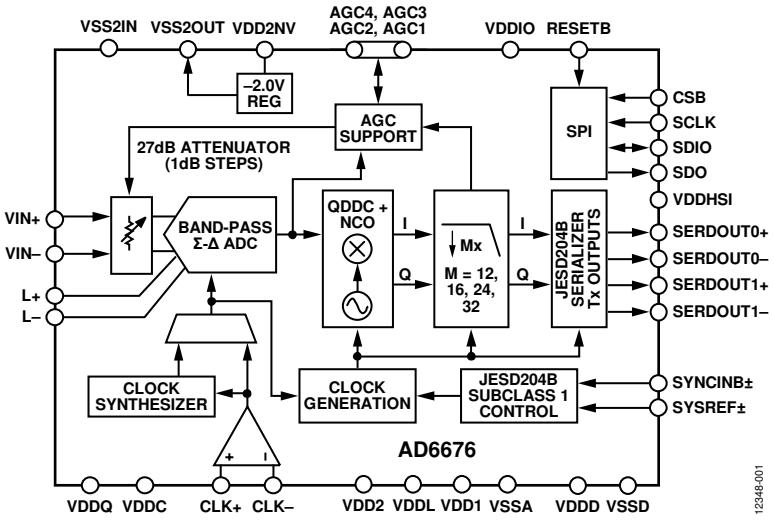

Figure 1.

[1] This product is protected by U.S. and international patents.

Rev. C Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
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AD6676* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD6676 Evaluation Board

DOCUMENTATION

Data Sheet

- AD6676: Wideband IF Receiver Subsystem Data Sheet

User Guides

- AD6676: Design Tools And Startup Guide For The Ad6676 Evaluation Board, A High Dynamic Range, Wideband Receiver

TOOLS AND SIMULATIONS

- AD6676 AMI Model

REFERENCE MATERIALS

Informational

- JESD204 Serial Interface

Press

- Wideband IF Receiver Chip Provides Industry Leading Dynamic Range in a Highly Integrated Solution

Technical Articles

- A Wideband Analog Front End Based on a Continuous Time, Δ-Σ High Speed ADC Reduces Power Consumption of High Performance Communication and Instrumentation Systems
- MS-2739: High Dynamic IF Receiver Simplifies Design of Next Generation µW Point-to-Point Modems

DESIGN RESOURCES

- AD6676 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD6676 EngineerZone Discussions.

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Added Table 123; Renumbered Sequentially 87

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9/2015—Rev. 0 to Rev. A

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10/2014—Revision 0: Initial Version

The band-pass Σ-Δ ADC of the AD6676, which operates between 2.0 GHz to 3.2 GHz, provides exceptional instantaneous dynamic range and inherent antialiasing capability. Its in-band frequency response typically maintains better than 1 dB pass band flatness with out-of-band peaking better than 0.5 dB. An integrated digital peak detector enables the instantaneous signal power to be monitored over a wide band (shortly after digitization), thus providing AGC capability to cope quickly with large in-band or out-of-band blockers.

The AD6676 includes various AGC monitoring and control features along with an internal 27 dB step attenuator in 1 dB steps. A flexible AGC port with digital input/output pins allows fast control of the AD6676 on-chip step attenuator and/or updates on the input signal via status flags. These features, along with the high instantaneous dynamic range, can significantly simplify AGC implementation compared to traditional narrow-band IF approaches that often require separate AGC capability for RF and IF protection.

In addition to reducing system complexity, the AD6676 enables significant space and power consumption savings for next generation multiple input/multiple output (MIMO) receiver architectures. The AD6676 is available in an 8 × 10 ball array WLCSP package that is approximately 4.3 mm × 5.0 mm, with a JESD204B serial interface that allows simple interfacing to the host processor.

Its low power consumption of 1.2 W compares favorably to IF sampling ADCs with similar bandwidth (BW) and dynamic range capabilities even without considering the added power savings from the elimination of an entire IF strip. The AD6676 features multichip synchronization that allows synchronization to within a fraction of an output data sample. For time-domain duplex (TDD) applications, the AD6676 features a fast power-up/power-down mode that further reduces power consumption while still maintaining multichip synchronization. Power savings of up to 60% or 42% is achievable with recovery times of 11.5 µs or 2.5 µs, depending on the device configuration.

Auxiliary blocks include an on-chip PLL clock multiplier to generate the Σ-Δ ADC clock. For applications that require better phase noise performance, an external differential RF clock source may also be used. The SPI port programs numerous parameters of the AD6676, allowing the device to be optimized for a variety of applications.

The AD6676 is available in an 80-ball WLCSP package with an optimized pinout that enables low cost printed circuit board (PCB) manufacturing. The device operates from a 1.1 V and 2.5 V supply with a total typical power consumption of 1.2 W at 3.2 GSPS operation. This product is protected by several United States patents. Contact Analog Devices, Inc., for further information.

PRODUCT HIGHLIGHTS

1. Industry leading dynamic range enables high performance, reconfigurable heterodyne (or direct sampling VHF) software defined radios with high AGC-free range.
2. Continuous time, band-pass Σ-Δ ADC supports IFs from 70 MHz to 450 MHz with IF signal bandwidths of up to 160 MHz and reduces IF filtering requirements.
3. The high instantaneous dynamic range and oversampling nature of the Σ-Δ ADC significantly reduces the IF filter complexity.
4. On-chip 27 dB digital attenuator with easy to drive resistive input simplifies interface to RF/IF components.
5. Small 4.3 mm × 5.0 mm package, simple interface, and integrated digital attenuator and clock synthesizer save PCB space.
6. Low input full-scale level of −2 dBm (or less) enables 3.3 V RF/IF component lineups at reduced P1dB and power.
7. Fast power saving mode supports TDD protocols.
8. Unique profile mode allows the AD6676 to switch between up to four different ADC IF/BW configurations in 1 µs.

SPECIFICATIONS

VDD1 = VDDL = VDDC = VDDQ = 1.1 V, VDDD = VDDHSI = 1.1 V, VDD2 = 2.5 V, VDDIO = 1.8 V, F_{IF} = 250 MHz, BW = 75 MHz, F_{ADC} = 3.2 GHz, attenuator = 0 dB, L± (inductor values) = 19 nH, maximum PIN_0dBFS setting with $IDAC1_{FS}$ = 4 mA, f_{DATA_IQ} = 200 MSPS, shuffler enabled (every clock cycle) with default threshold of 5, unless otherwise noted.

Table 1.

Parameter	Temperature	Test Conditions/Comments	Min	Typ	Max	Unit
SYSTEM DYNAMIC PERFORMANCE						
Full-Scale Input Power Level (PIN_0dBFS)[1]				−2		dBm
Maximum Continuous Wave (CW) Input Power[2]			−2	−1		dBFS
Noise Figure (NF)		No signal and measured		17		dB
Worst In-Band Noise Spectral Density	Full	Over a 5 MHz bandwidth		−155	−152.5	dBFS/Hz
Noise Figure at IF Center (NF)		No signal and measured		13		dB
In-Band Noise Spectral Density (NSD)		Over a 5 MHz bandwidth		−159		dBFS/Hz
Input Second-Order Intercept (IIP2)		−6 dBFS tones		60		dBm
Second-Order Intermodulation Distortion (IMD) (IMD2)		See Table 20		−68.3		dBc
Input Third-Order Intercept (IIP3)	Full	−8 dBFS tones		36.9		dBm
Third-Order IMD (IMD3)	Full	−8 dBFS tones		−95	−84.2	dBc
Worst In-Band Spur for Swept CW Tone	Full	−2 dBFS tone		−99	−93.5	dBFS
		−10 dBFS tone		−109.6		dBFS
In-Band Noise	Full	−2 dBFS tone		−75.5	−73.7	dBFS
	Full	No CW tone		−78.5	−76.5	dBFS
Gain Variation	Full			0.5		dB
IF INPUT (VIN±)						
Input Span		0 dBFS				
0 dB Attenuator Setting				0.48		V p-p
12 dB Attenuator Setting				1.92		V p-p
Common-Mode Input Voltage		Self biased		1.0		V
Differential Input Impedance	25°C			60||2		Ω||pF
Common-Mode Input Impedance	25°C			3.5		kΩ
Full-Scale Input Power Adjustment (PIN_0dBFS)		$IDAC1_{FS}$ span of 1 mA to 4 mA		12		dB
DIGITAL STEP ATTENUATOR (VIN±)						
Attenuation Range	Full			27		dB
Step Size	Full			1		dB
Input Return Loss	Full			20		dB
Input Return Loss Variation vs. Attenuator Setting	Full			2		dB
CLOCK INPUT (CLK±)						
Clock Synthesizer Disabled						
Frequency Range	Full		2.0		3.2	GHz
Amplitude Range	Full		0.4	0.8	2.0	V p-p
Differential Input Impedance	25°C	At 3 GHz		86||0.3		Ω||pF
Common Mode Impedance	25°C	At 3 GHz		700||0.8		Ω||pF
Input Return Loss	25°C	With 1:2 balun		15		dB
Common-Mode Voltage	25°C	Self biased		0.70		V
Clock Synthesizer Enabled						
Frequency Range[3]	Full		10		320	MHz
Amplitude Range	Full	Single-ended into CLK+	0.4	0.8	1.1	V p-p
CLK+ Input Impedance	25°C			1.4||1.0		kΩ||pF
Minimum Slew Rate				12		V/µs
Common-Mode Voltage	25°C	Self biased		0.55		V

Parameter	Temperature	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK SYNTHESIZER						
Phase Detector Frequency	Full		10		80	MHz
Minimum Charge Pump Output Current	Full			0.1		mA
Maximum Charge Pump Output Current	Full			6.4		mA
VCO Tuning Range	Full		2.94		3.2	GHz
Σ-Δ ADC AND DIGITAL DOWNCONVERTER						
Resolution	Full			16		Bits
Clock Frequency (F_{ADC})	Full		2.0		3.2	GHz
IF Center Frequency (F_{IF})	Full		70		450	MHz
IF Bandwidth		Maximum BW applies to higher F_{IF}	0.005 × F_{ADC}		0.05 × F_{ADC}	
IF Pass Band Gain Flatness	Full	F_{ADC}, F_{IF}, and BW dependent		1.0		dB
Out-of-Band Peaking		Depends on F_{ADC}, F_{IF}, and BW		0.5		dB
Alias Rejection		Regions of $F_{ADC} \pm F_{IF}$		51		dB
Fixed Decimation Factors	Full			12, 16, 24, 32		
NCO Tuning Resolution		Decimate by 12 or 24		F_{ADC}/3072		
		Decimate by 16 or 32		F_{ADC}/4096		
Out-of-Range Recovery Time	Full	Relative to ADC clock cycles		52		$1/F_{ADC}$
POWER SUPPLY AND CONSUMPTION						
Analog Supply Voltage						
VDD1, VDDL, VDDQ, VDDC	Full		1.0725	1.1	1.1275	V
VDD2, VDD2NV	Full		2.4375	2.5	2.5625	V
VSS2IN		Use on-chip regulator, tie to VSS2OUT		−2.0		V
Digital Supply Voltage (VDDD)	Full		1.0725	1.1	1.1275	V
JESD204B Supply Voltage (VDDHSI)	Full		1.0725	1.1	1.1275	V
SPI Interface Supply Voltage (VDDIO)	Full		1.7	1.8	2.5625	V
Analog Supply Current						
$I_{VDD1} + I_{VDDL}$	Full			368	397	mA
$I_{VDDC} + I_{VDDQ}$	Full	CLK synthesizer disabled		57	68	mA
I_{VDDC}[4] + I_{VDDQ}	Full	CLK synthesizer enabled		93	106	mA
$I_{VDD2} + I_{VDD2NV}$	Full			145	165	mA
Digital Supply Current (I_{VDDD})	Full			141	208	mA
JESD204B Supply Current (I_{VDDHSI})	Full			164	190	mA
SPI Interface Supply Current (I_{VDDIO})	Full			0.4	1	mA
Power Consumption	Full					
With CLK SYN Disabled				1.16	1.31	W
With CLK SYN Enabled				1.20	1.34	W
Standby[5]	Full			0.44		W
Power-Down	Full			66	177	mW
OPERATING TEMPERATURE RANGE			−40		+85	°C

[1] Extrapolated input power level is measured at the center of IF pass band that results in a 0 dBFS power level.
[2] The overload level of the Σ-Δ ADC for a CW tone is guaranteed up to −2 dBFS back off from full scale but typically exceeds −1 dBFS. Input signals that have a higher peak-to-average ratio (PAR) than a CW tone (PAR = 3 dB) must apply additional back off based on the difference in PAR.
[3] The clock synthesizer reference divider (Register 0x2BB, Bits[7:6]) must be set to divide by 4 or by 2 to ensure that its phase detector frequency remains ≤40 MHz.
[4] f_{CLK} = 200 MHz, F_{ADC} = 3.2 GHz.
[5] The AD6676 is configured for recovery time of 11.5 µs with VSS2 generator/ digital data in standby (Register 0x150 = 0x40) and low power ADC state (Register 0x250 = 0x95).

DIGITAL HIGH SPEED SERDES SPECIFICATIONS

VDD1 = VDDL = VDDC = VDDQ = 1.1 V, VDDD = VDDHSI = 1.1 V, VDD2 = 2.5 V, VDDIO = 1.8 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Temp.	Min	Typ	Max	Unit
HIGH SPEED SERIAL INPUT/OUTPUT						
Line Rate			1.6668		5.333	Gbps
Dual Lane Data Output Period or Unit Interval	UI	Full		$1/(20 \times f_{DATA\_IQ})$[1]		sec
Single Lane Data Output Period or Unit Interval	UI	Full		$1/(40 \times f_{DATA\_IQ})$[1]		sec
Data Output Duty Cycle		25°C		50		%
Data Valid Time		25°C		0.78		UI
PLL Lock Time		25°C		4		µs
Wake-Up Time (Standby)		25°C		5		µs
Wake-Up Time (Power-Down)		25°C		2.5		ms
Pipeline Delay (Latency)		Full		32.3		$1/f_{DATA\_IQ}$[1]
Deterministic Jitter		25°C		9		ps
Random Jitter at 5.333 Gbps		25°C		0.7		ps rms
Output Rise/Fall Time		25°C		45		ps
SYNCINB± Falling Edge to First K.28 Characters		25°C	4			Multiframes
CGS Phase K.28 Characters Duration		25°C	1			Multiframes
DIGITAL OUTPUTS (SERDOUT0±, SERDOUT1±)						
Logic Compliance		Full		CML		
Differential Output Voltage	VOD	Full	360		750	mV
Output Offset Voltage, ANSI Mode	VOS	Full	0.75	VDDHSI/2	1.05	V
Differential Termination Impedance		25°C		100		Ω
SYSREF INPUT (SYSREF±)						
Logic Compliance				LVDS/PECL		
Differential Input Voltage		Full	0.6	1.2	1.8	V p-p
Differential Input Impedance[2]		25°C		35/2		kΩ||pF
Input Common-Mode Voltage			0.8	0.85	2.0	V
SYNCIN INPUT (SYNCINB+, SYNCINB−)						
Logic Compliance[3]				CMOS/LVDS		
CMOS Input Voltage High	V_{IH}			$0.65 \times$ VDDIO		V
CMOS Input Voltage Low	V_{IL}			$0.35 \times$ VDDIO		V
LVDS Differential Input Voltage		Full	0.6	1.2	1.8	V p-p
LVDS Differential Input Impedance		25°C		100||1		Ω||pF
LVDS Input Common-Mode Voltage			0.8	0.85	2.0	V
LVDS Input Common-Mode Impedance		25°C		1||1		kΩ||pF
SYSREF (SYSREF±) TIMING REQUIREMENTS[4]						
Clock Synthesizer Disabled						
Setup Time	t_{SU_SR}	25°C		0.16		ns
Hold Time	t_{H_SR}	25°C		0.84		ns
Clock Synthesizer Enabled						
Setup Time	t_{SU_SR}	25°C		0.5		ns
Hold Time	t_{H_SR}	25°C		0.5		ns

[1] F_{DATA_IQ} corresponds to the complex output data rate (that is, F_{ADC}/DEC_FACTOR). Latency specification also includes ADC and digital filters delays. See Table 15
[2] The SYSREF± input requires an external differential resistor for proper termination.
[3] Set via Register 0x1E7, Bit 2, with CMOS being the default setting.
[4] SYSREF± setup and hold times are defined with respect to the rising SYSREF± edge and rising clock edge. Positive setup time leads the clock edge. Positive hold time also lags the clock rising edge. Note that the hold time takes into consideration that the internal clock signal used to sample SYSREF operates at $F_{ADC}/2$; thus, SYSREF± must remain high for at least two F_{ADC} clock cycles.

CLK± TO SYSREF± TIMING DIAGRAM

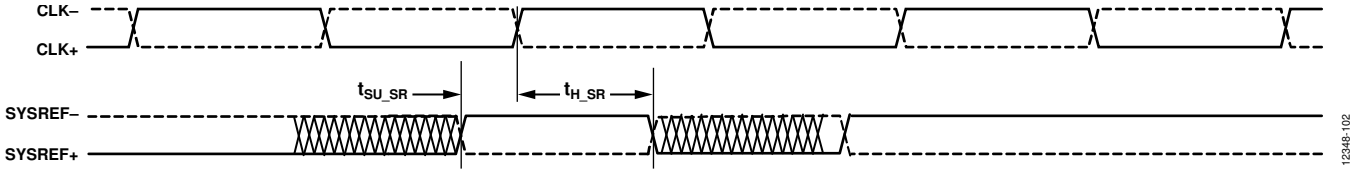

Figure 2. SERDES CLK+ to SYSREF+ Timing

DIGITAL CMOS INPUT/OUTPUT SPECIFICATIONS

VDD1 = VDDL = VDDC = VDDQ = VDDD = VDDHSI = 1.1 V, VDD2 = 2.5 V, VDDIO = 1.8 V, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT/OUTPUT LEVELS						
Input Voltage High	V_{IH}		VDDIO × 0.65			V
Input Voltage Low	V_{IL}				VDDIO × 0.35	V
Output Voltage High	V_{OH}					
SDIO/SDO		I_{OH} = 3 mA	VDDIO × 0.7			V
AGCx		I_{OH} = 0.5 mA	VDDIO × 0.7			V
Output Voltage Low	V_{OL}					
SDIO/SDO		I_{OL} = 3 mA			0.4	V
AGCx	V_{OL}	I_{OL} = 0.5 mA			0.4	V
Input Capacitance				1		pF
SPI TIMING		See Figure 148, Figure 149, and Figure 150				
SCLK Frequency	f_{SCLK}				25	MHz
SCLK Period	t_{SCLK}		40			ns
SCLK Pulse Width High	t_{HIGH}		10			ns
SCLK Pulse Width Low	t_{LOW}		10			ns
SDIO Setup Time	t_{DS}		2			ns
SDIO Hold Time	t_{DH}		2			ns
SPI_RESET Setup Time[1]	t_{SPI_RST}	Not shown in Figure 148 to Figure 150		2		ms
SCLK Falling Edge to SDO Valid Propagation Delay	t_{ACCESS}		10			ns
CSB Rising Edge to SDIO High-Z	t_Z		10			ns
CSB Fall to SCLK Rise Setup Time	t_S		2			ns
SCLK Fall to CSB Rise Hold Time	t_H		2			ns

[1] This is the time required after a software or hardware reset until SPI access is available again.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VDD1, VDDC, VDDL, VDDQ to VSSA	−0.2 V to +1.2 V
VDD2 to VSSA	−0.3 V to +3.0 V
VDD2NV to VSSA	−0.3 V to +3.0 V
VSS2IN, VSS2OUT to VSSA	−2.5 V to +0.3 V
VDDD, VDDHSI to VSSD	−0.2 V to +1.2 V
VDDIO to VSSD	−0.3 V to +3.0 V
VIN+, VIN− to VSSA	−0.3 V to VDD2 + 0.3 V
L+, L− to VSSA	−0.3 V to VDD2 + 0.3 V
CLK+, CLK− to VSSA	−0.3 V to VDDC + 0.3 V
SYSREF+, SYSREF−, SERDOUT0+, SERDOUT0−, SERDOUT1+, SERDOUT1− to VSSD	−0.3 V to VDDHSI + 0.3 V
SYNCINB+, SYNCINB− to VSSD	−0.3 V to VDDIO + 0.3 V
CSB, SDO, SDIO, SCLK, RESETB, AGC1, AGC2, AGC3, AGC4 to VSSD	−0.3 V to VDDIO + 0.3 V
Normal Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature Under Bias	125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Typical θ_{JA} is specified for a 4-layer printed circuit board (PCB) with a solid ground plane in conformance to JESD51-9 2s2p. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces the value of θ_{JA}.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	θ_{JB}	Unit
4.3 mm × 5.0 mm WLCSP	26	0.2	4.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

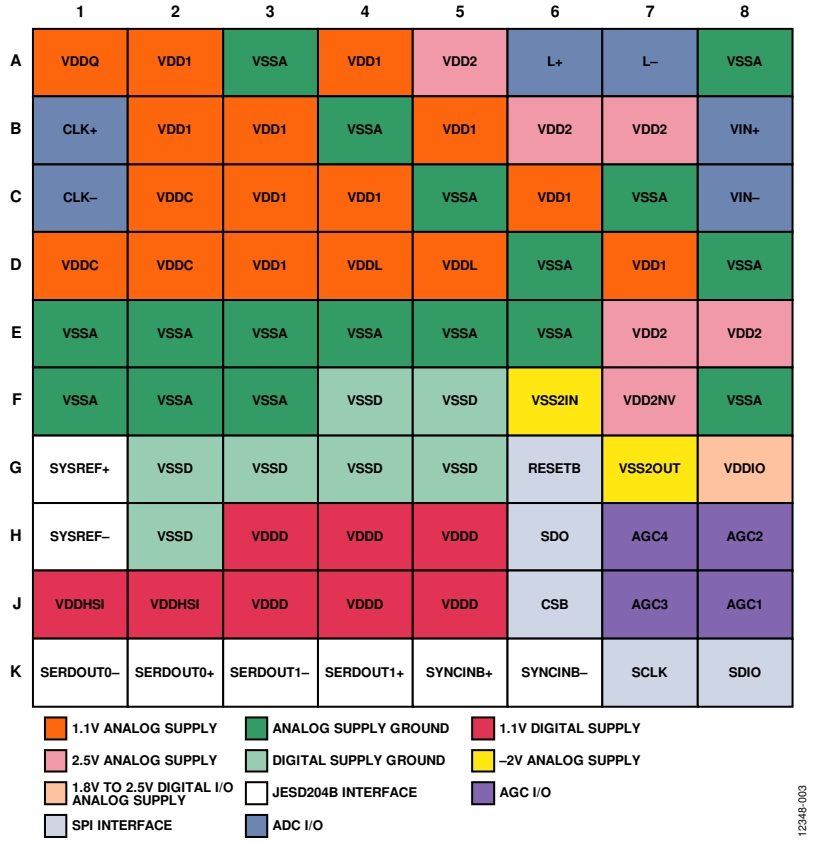

Figure 3. Pin Configuration (Top View, Not to Scale)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
Σ-Δ ADC Modulator		
B8, C8	VIN+, VIN–	Analog Inputs with Nominal 60 Ω Differential Input Termination.
A6, A7	L+, L–	Analog Outputs for External Inductor.
B1, C1	CLK+, CLK–	Clock Inputs, Nominal 100 Ω Differential Input Termination When the Clock Synthesizer is Disabled. When the clock synthesizer is enabled, each input is 1.2 kΩ; therefore, an external, 100 Ω differential termination is recommended if the clock source is LVDS or PECL. For a CMOS source driving a long trace, the addition of a series 33 Ω resistor next to the source reduces overshoot seen at CLK+ input pin.
JESD204B Interface		
K1, K2	SERDOUT0–, SERDOUT0+	Lane 0 JESD204B Digital CML Outputs.
K3, K4	SERDOUT1–, SERDOUT1+	Lane 1 JESD204B Digital CML Outputs.
G1, H1	SYSREF+, SYSREF–	JESD204B SYSREF Inputs. Note that these pins have no differential termination.
K5, K6	SYNCINB+, SYNCINB–	JESD204B CMOS or LVDS SYNC Inputs. Selectable via Register 0x1E7, Bit 2. Default CMOS mode uses the SYNCINB+ pin only. LVDS mode has a 100 Ω differential termination.

Pin No.	Mnemonic	Description
CMOS Input/Outputs		
J8, H8, J7, H7	AGC1, AGC2, AGC3, AGC4	AGC Bidirectional Inputs/Outputs. By default, AGC2 and AGC1 are inputs, whereas AGC4 and AGC3 are outputs. If the AGC2 and AGC1 pins are unused, connect them to VSSD via a 100 kΩ resistor.
J6	CSB	Serial Port Enable Input. Active low.
K8	SDIO	Serial Port Input/Output.
H6	SDO	Serial Port Output.
K7	SCLK	Serial Clock Input.
G6	RESETB	Active Low Reset Input. This pin places digital logic and SPI registers into a known default state. Leave this pin open if unused because it has an internal pull-up resistor.
Power Supplies		
G8	VDDIO	Digital Supply Input for CMOS Input/Outputs (1.8 V to 2.5 V).
J1, J2	VDDHSI	Digital 1.1 V Supply Input for the High Speed Serial Interface.
H3 to H5, J3 to J5	VDDD	Digital 1.1 V Supply Input.
F4, F5, G2 to G5, H2	VSSD	Digital Supply Return.
A1	VDDQ	Analog 1.1 V Supply Input for the CLK Synthesizer Charge Pump and Dividers.
C2, D1, D2	VDDC	Analog 1.1 V Supply Input for the CLK Synthesizer VCO.
D4, D5	VDDL	Analog 1.1 V Supply Input for the ADC.
A2, A4, B2, B3, B5, C3, C4, C6, D3, D7	VDD1	Analog 1.1 V Supply Input for the ADC.
A5, B6, B7, E7, E8	VDD2	Analog 2.5 V Supply Input.
A3, A8, B4, C5, C7, D6, D8, E1 to E6, F1 to F3, F8	VSSA	Analog Supply Return.
Negative Voltage Regulator		
F7	VDD2NV	Analog 2.5 V Supply Input.
G7	VSS2OUT	Internal −2.0 V Supply Output. Connect this pin to VSS2IN.
F6	VSS2IN	Analog −2.0 V Supply Input. Connect this pin to VSS2OUT.

TYPICAL PERFORMANCE CHARACTERISTICS

NOMINAL PERFORMANCE FOR IF = 115 MHz (DIRECT SAMPLING VHF RECEIVER)

F_{IF} = 115 MHz, BW = 20 MHz, F_{ADC} = 2.4 GHz, attenuator = 0 dB, L_{EXT} = 100 nH, maximum PIN_0dBFS setting, f_{DATA_IQ} = 75 MSPS, nominal supplies, shuffler enabled (every 4 clock cycles), with default threshold settings, unless otherwise noted.

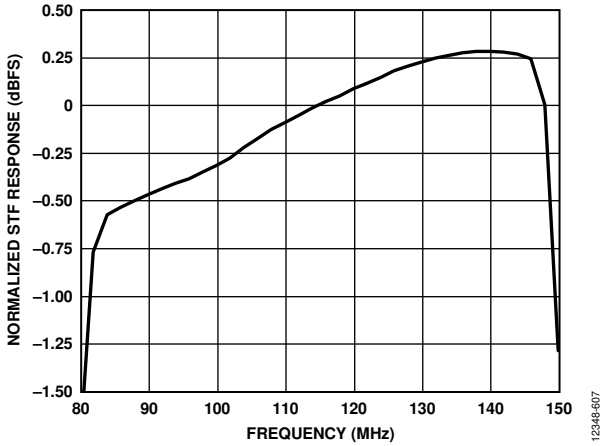

Figure 4. IF Pass Band Flatness (Includes Digital Filter)

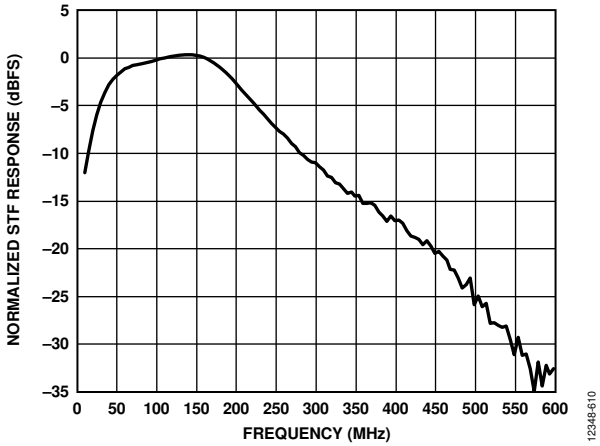

Figure 7. Wideband Frequency Response (Before Digital Filter)

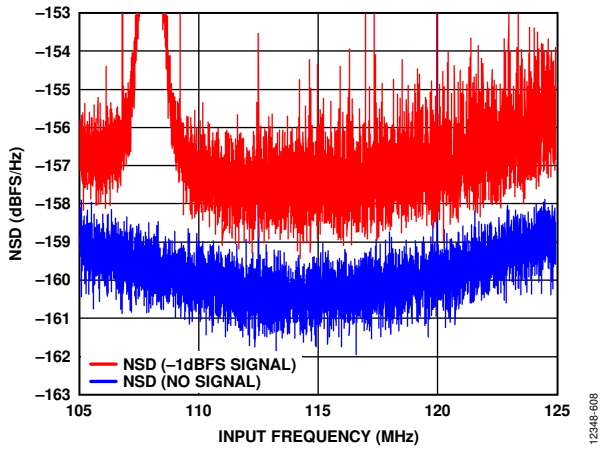

Figure 5. NSD With and Without Full-Scale CW at 108 MHz

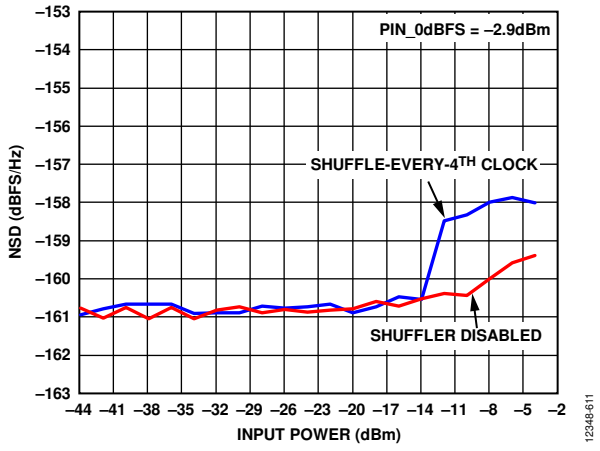

Figure 8. NSD vs. CW Input Power, CW at 108 MHz (NSD Measured at IF Center of 115 MHz)

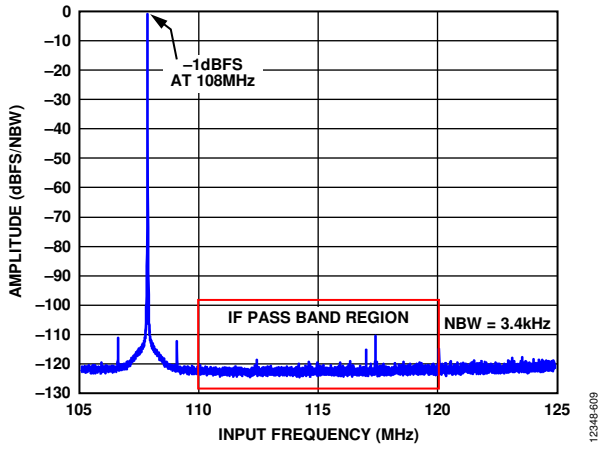

Figure 6. Spectral Plot of IF Pass Band Region with –1 dBFS CW at 108 MHz

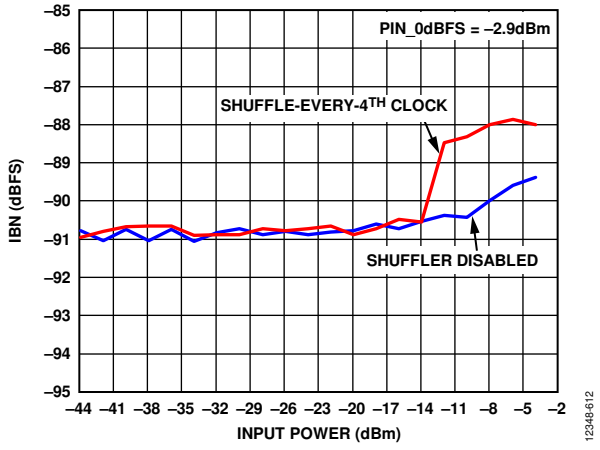

Figure 9. Integrated In-Band Noise (IBN) in IF Pass Band Region of 10 MHz vs. Swept Single Tone Input Power with CW at 130 MHz

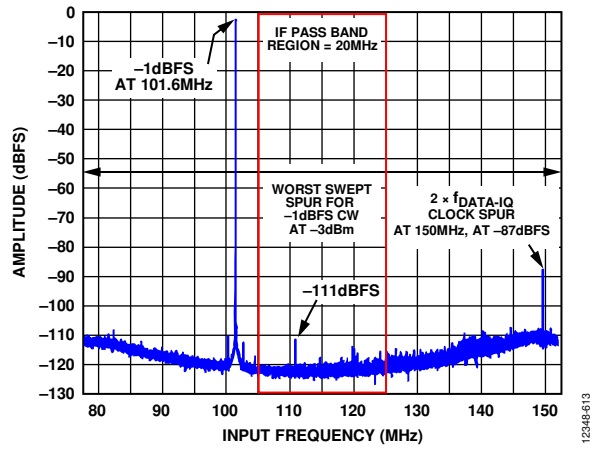

Figure 10. Worst Spur Falling in 75 MHz Pass Band for Swept CW from 77.5 MHz to 152.5 MHz

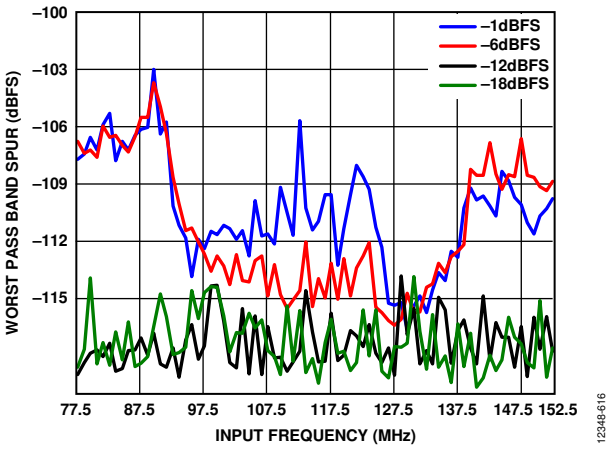

Figure 13. Worst Pass Band Spur with Swept CW from 77.5 MHz to 150 MHz, over P_{IN} = −1 dBFS, −6 dBFS, −12 dBFS, and −18 dBFS

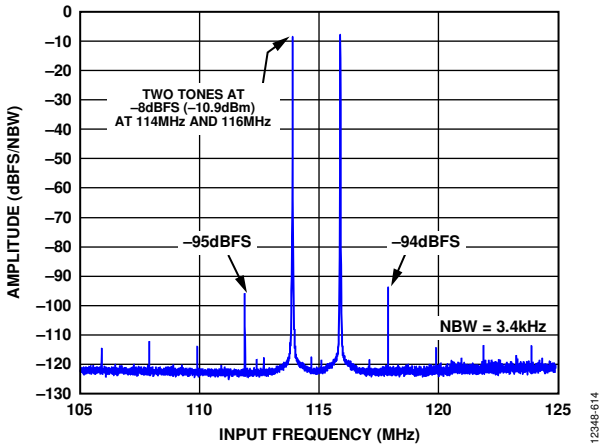

Figure 11. Two-Tone IMD Performance (f_1 = 114 MHz, f_2 = 116 MHz)

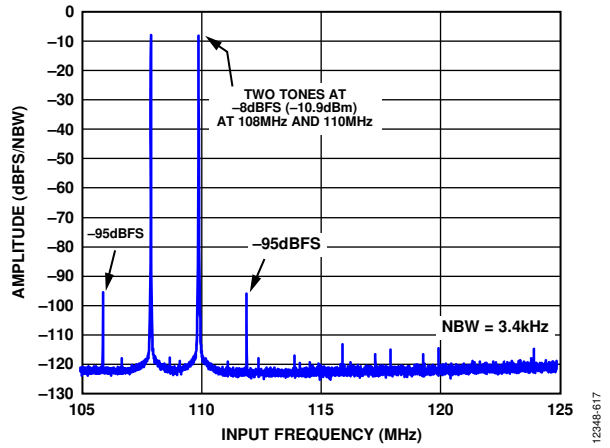

Figure 14. Two-Tone IMD Performance (f_1 = 108 MHz, f_2 = 110 MHz)

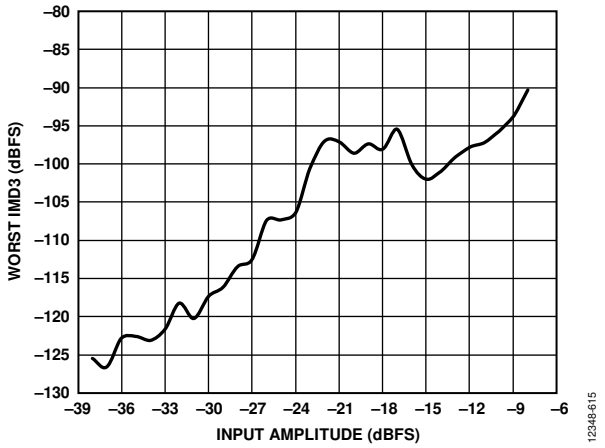

Figure 12. Swept Two-Tone Worst IMD3 vs. Tone Input Amplitude (f_1 = 113 MHz, f_2 =118 MHz)

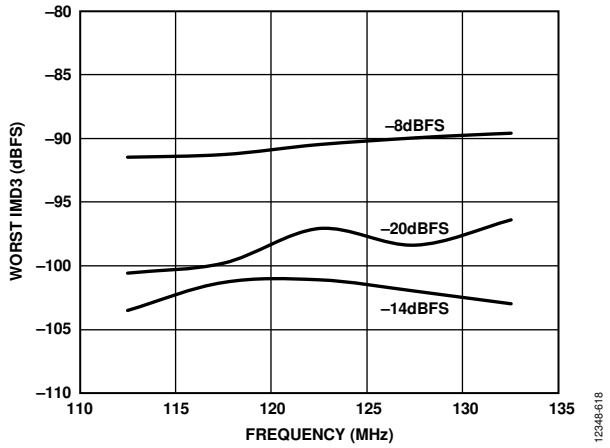

Figure 15. Swept Two Tone Worst IMD3 vs. Frequency over Pass Band (Δf = 5 MHz for Two Tones, P_{IN} = −8 dBFS, −14 dBFS, and −20 dBFS)

NOMINAL PERFORMANCE FOR IF = 140 MHz (µW POINT-TO-POINT RECEIVERS)

F_{IF} = 140 MHz, BW = 56 MHz or 112 MHz, F_{ADC} = 3.2 GHz, attenuator = 0 dB, L_{EXT} = 43 nH, maximum PIN_0dBFS setting, f_{DATA_IQ} = 200 MSPS, nominal supplies, shuffler enabled (every clock cycle), with default threshold settings, unless otherwise noted.

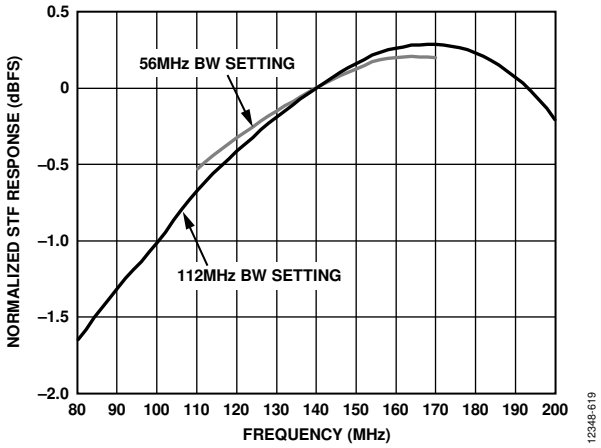

Figure 16. IF Pass Band Flatness (Includes Digital Filter)

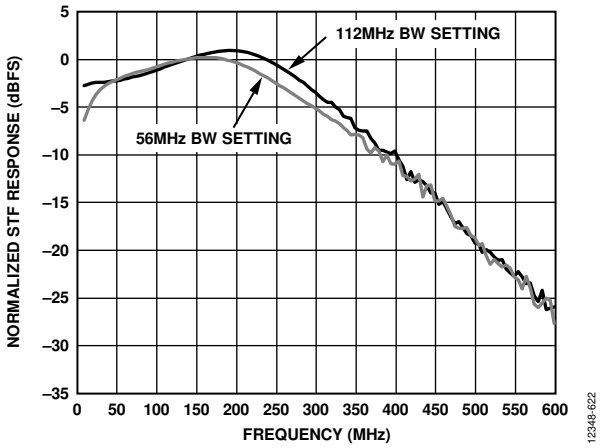

Figure 19. Wideband Frequency Response (Before Digital Filter)

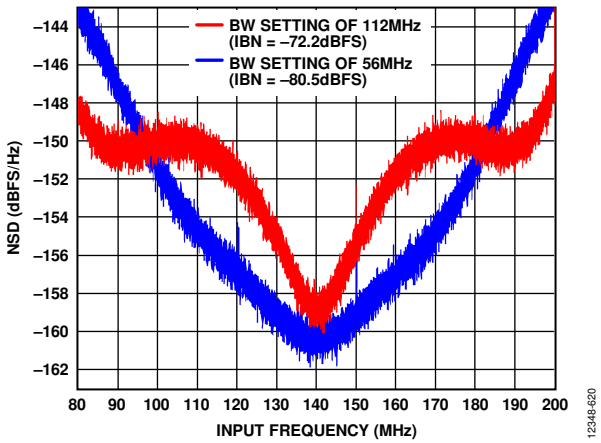

Figure 17. NSD with No Signal, IBN = 112 MHz and 56 MHz

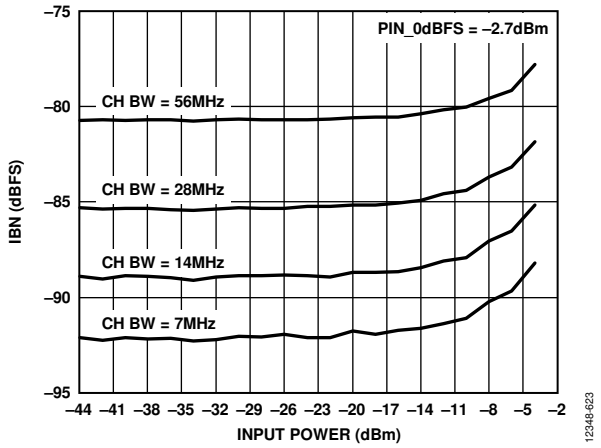

Figure 20. IBN vs. Swept Single Tone Input Power over Channel BW = 7 MHz, 14 MHz, 28 MHz, and 56 MHz, CW Blocker at 350 MHz

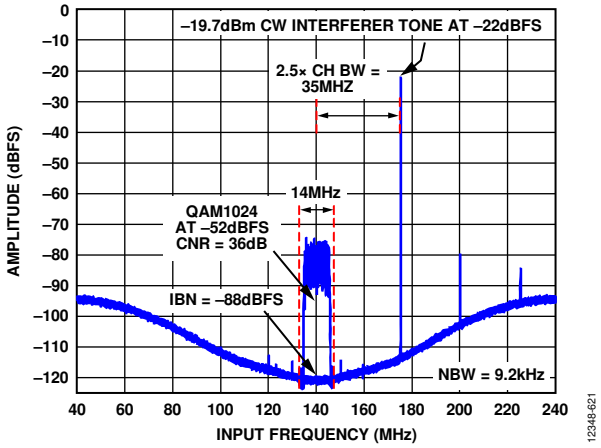

Figure 18. Spectral Plot of CW Interferer Dynamic Range for QAM1024, Channel BW = 14 MHz at Sensitivity Level with CW Interferer 30 dB Higher at 35 MHz Offset

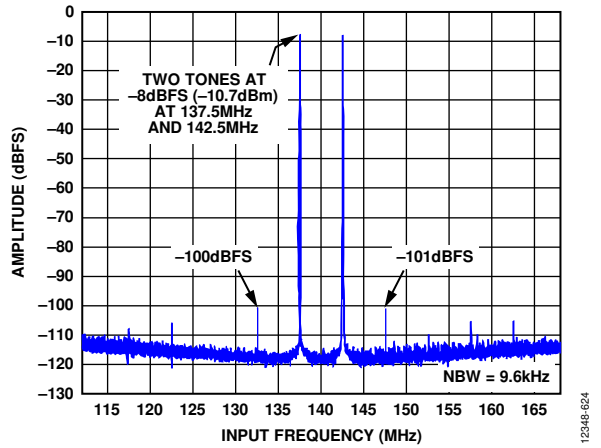

Figure 21. Two-Tone IMD Performance (f_1 = 137.5 MHz, f_2 = 142.5 MHz)

NOMINAL PERFORMANCE FOR IF = 181 MHz (WIRELESS INFRASTRUCTURE RECEIVER)

F_{IF} = 181 MHz, BW = 75 MHz, F_{ADC} = 2.94912 GHz, attenuator = 0 dB, L_{EXT} = 43 nH, maximum PIN_0dBFS setting, f_{DATA_IQ} = 122.88 MSPS, shuffler enabled (every clock cycle), with default threshold settings, unless otherwise noted.

Figure 22. IF Pass Band Flatness (Includes Digital Filter)

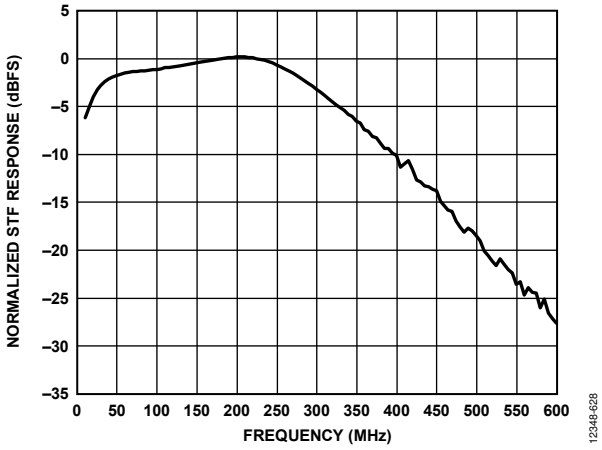

Figure 25. Wideband Frequency Response (Before Digital Filter)

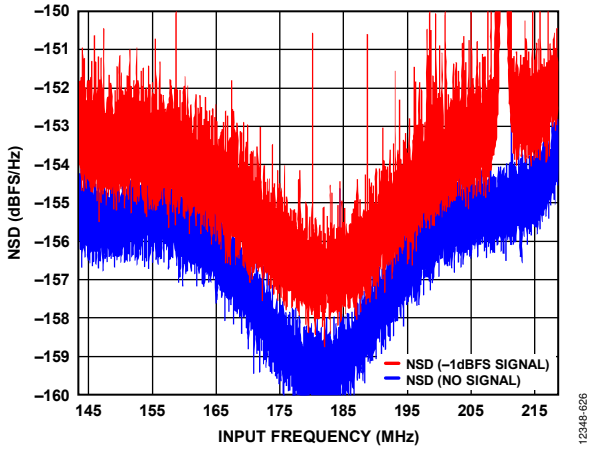

Figure 23. NSD With and Without Full-Scale CW at 210 MHz

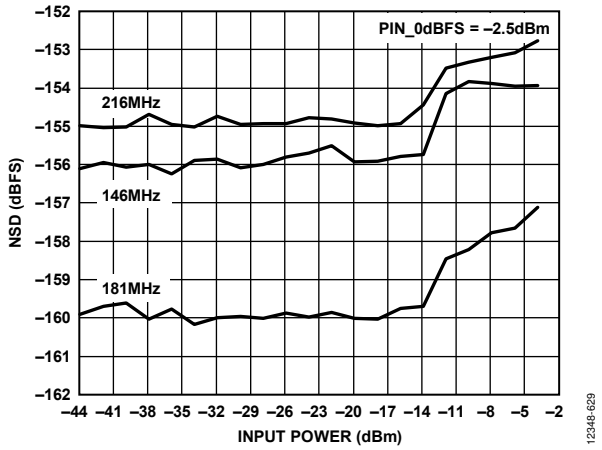

Figure 26. NSD vs. CW Input Power, CW = 210 MHz
(NSD Measured at 181 MHz as well as 146 MHz and 216 MHz Band Edges)

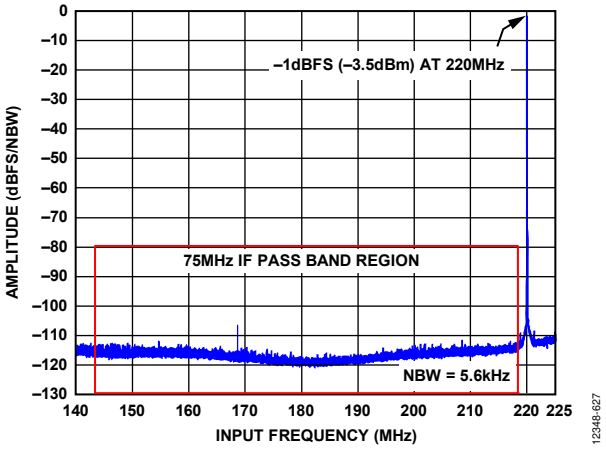

Figure 24. Spectral Plot of IF Pass Band Region with –1 dBFS CW at 220 MHz

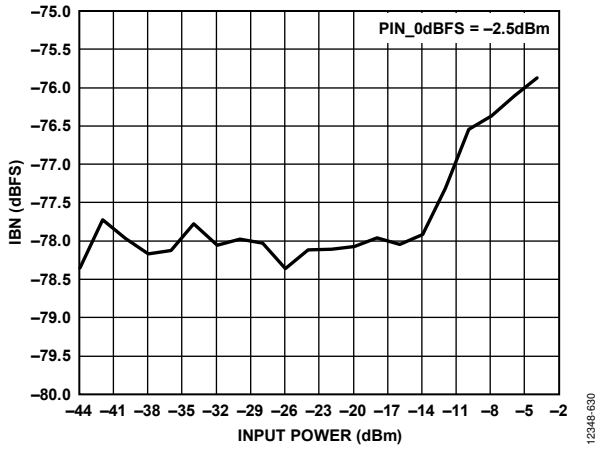

Figure 27. IBN in IF Pass Band Region (BW = 75 MHz) vs. Swept Single Tone Input Power with CW at 220 MHz

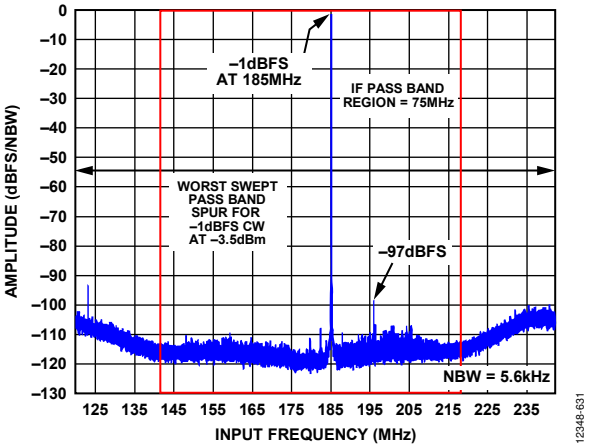

Figure 28. Worst Spur Falling in 75 MHz Pass Band for Swept CW from 122.88 MHz to 245.76 MHz

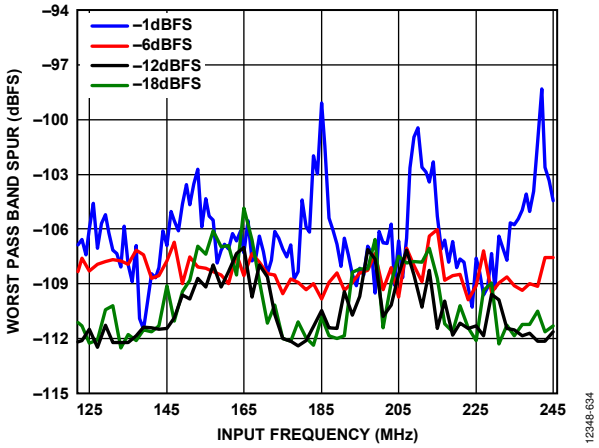

Figure 31. Swept Worst Pass Band Spur with CW Swept from 122.88 MHz to 245.76 MHz, over P_{IN} = –1 dBFS, –6 dBFS, –12 dBFS, and –18 dBFS

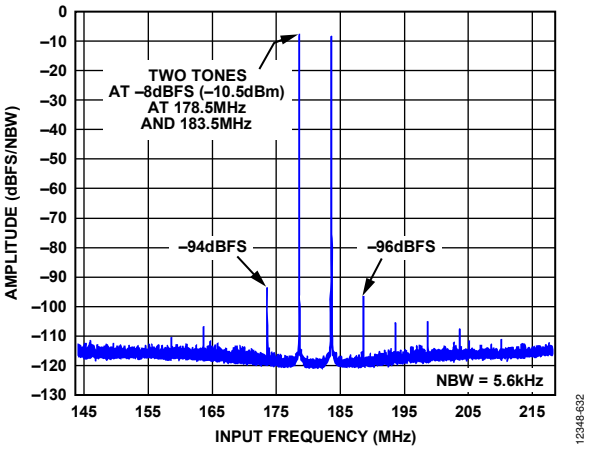

Figure 29. Two-Tone IMD Performance (f_1 = 178.5 MHz, f_2 = 183.5 MHz)

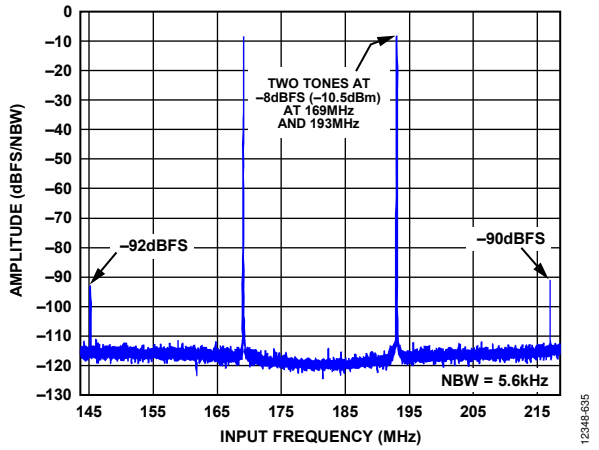

Figure 32. Two-Tone IMD Performance (f_1 = 169 MHz, f_2 = 193 MHz)

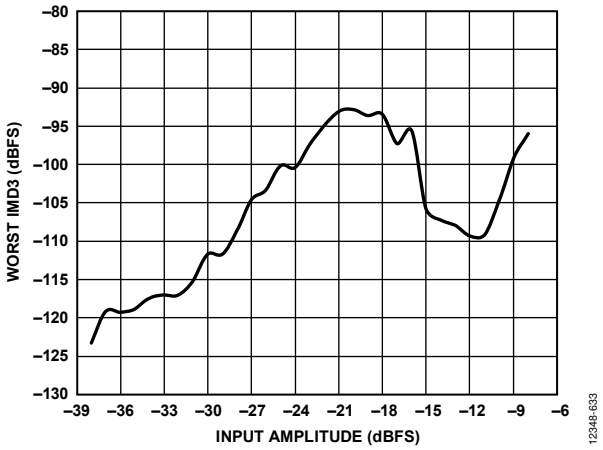

Figure 30. Swept Two-Tone Worst IMD3 vs. Tone Level (dBFS) (f_1 = 178.5 MHz, f_2 = 183.5 MHz)

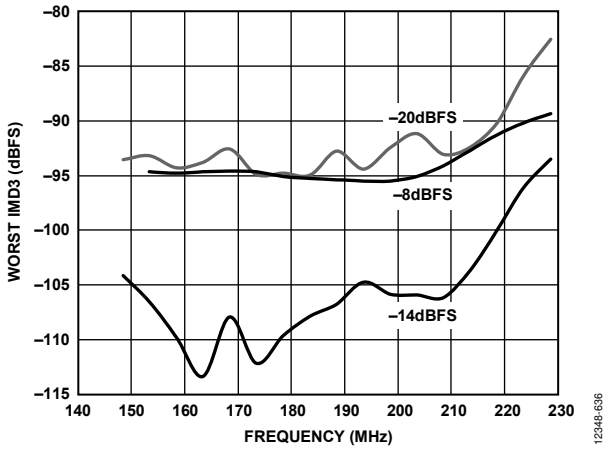

Figure 33. Swept Two-Tone Worst IMD3 vs. Frequency over Pass Band (Δf = 5 MHz for Two Tones, P_{IN} = –8 dBFS, –14 dBFS, and –20 dBFS)

NOMINAL PERFORMANCE FOR IF = 250 MHz AND BW = 75 MHz

F_{IF} = 250 MHz, BW = 75 MHz, F_{ADC} = 3.2 GHz, attenuator = 0 dB, L_{EXT} = 19 nH, maximum PIN_0dBFS setting, f_{DATA_IQ} = 200 MSPS, nominal supplies, shuffler enabled (every clock cycle), with default threshold settings, unless otherwise noted.

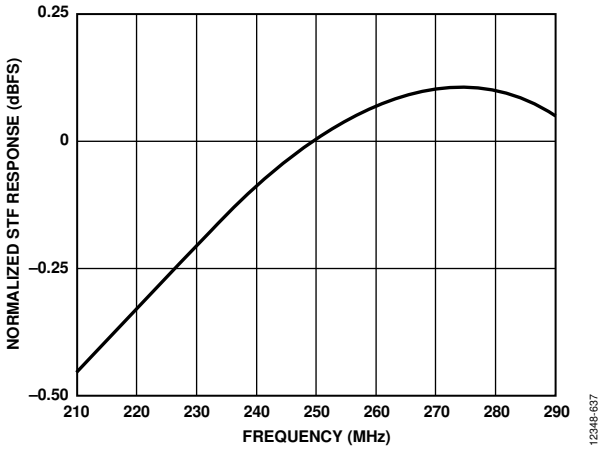

Figure 34. IF Pass Band Flatness (Includes Digital Filter)

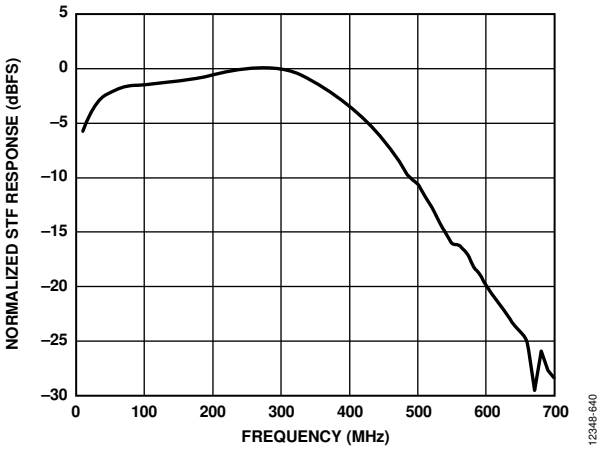

Figure 37. Wideband Frequency Response (Before Digital Filter)

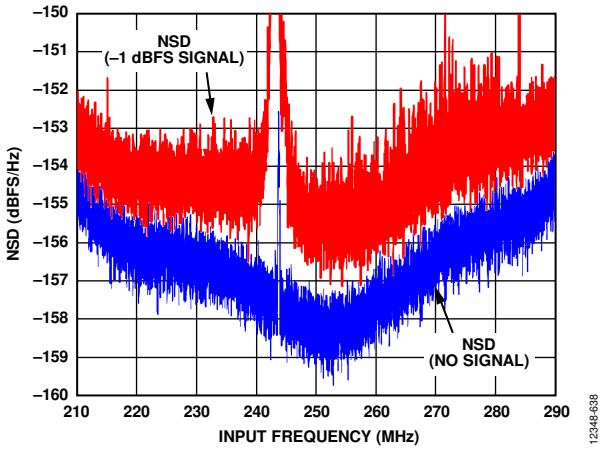

Figure 35. NSD With and Without Full-Scale CW at 243 MHz

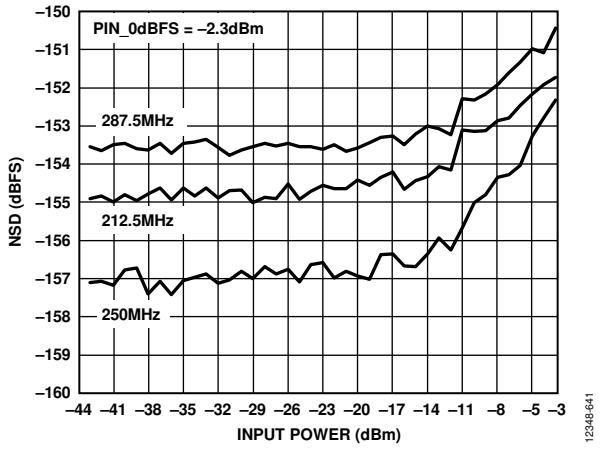

Figure 38. NSD vs. CW Input Power, CW at 243 MHz
(NSD Measured at 250 MHz as well as 212.5 MHz and 287.5 MHz Band Edges)

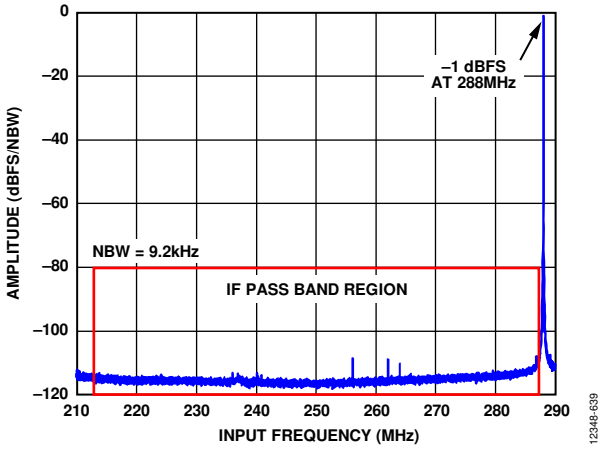

Figure 36. Spectral Plot of IF Pass Band Region with –1 dBFS CW at 288 MHz

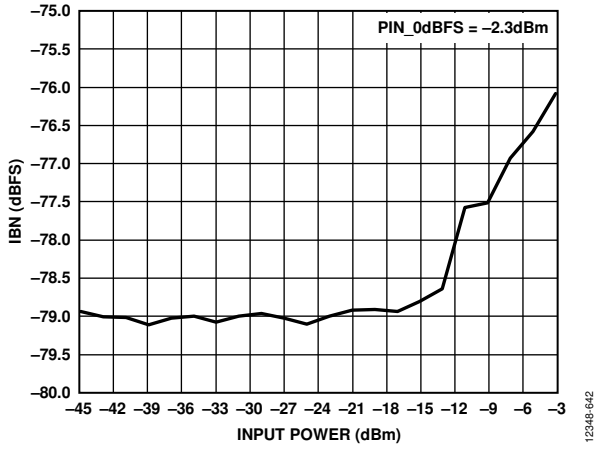

Figure 39. IBN in the Pass Band Region (BW = 75 MHz) vs. Swept Single Tone Input Power with CW at 288 MHz

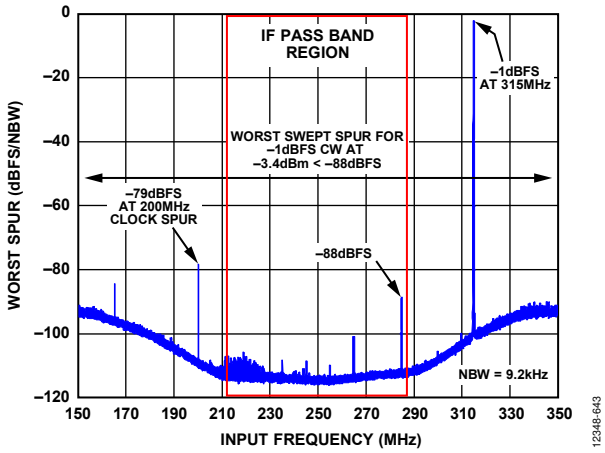

Figure 40. Worst Spur Falling in 75 MHz Pass Band for Swept CW from 150 MHz to 300 MHz

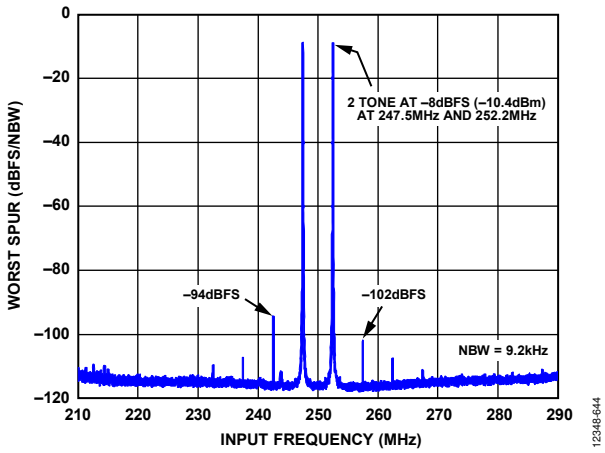

Figure 41. Two-Tone IMD Performance (f_1 = 247.5 MHz, f_2 = 252.5 MHz)

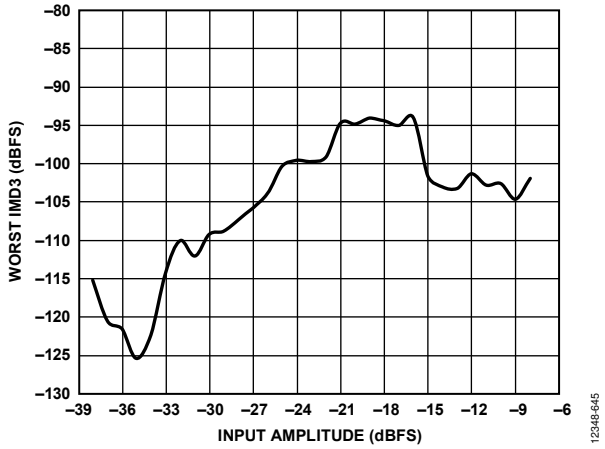

Figure 42. Swept Two-Tone Worst IMD3 vs. Tone Level (dBFS) (f_1 = 252.5 MHz, f_2 = 257.5 MHz)

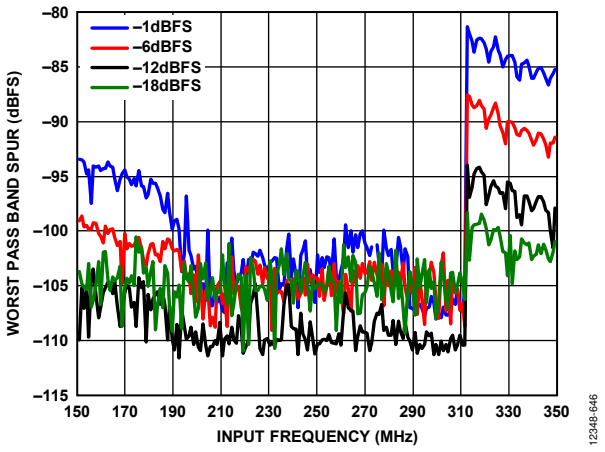

Figure 43. Swept Worst Pass Band Spur with CW Swept from 150 MHz to 300 MHz for P_{IN} = −1 dBFS, −6 dBFS, −12 dBFS, and −18 dBFS

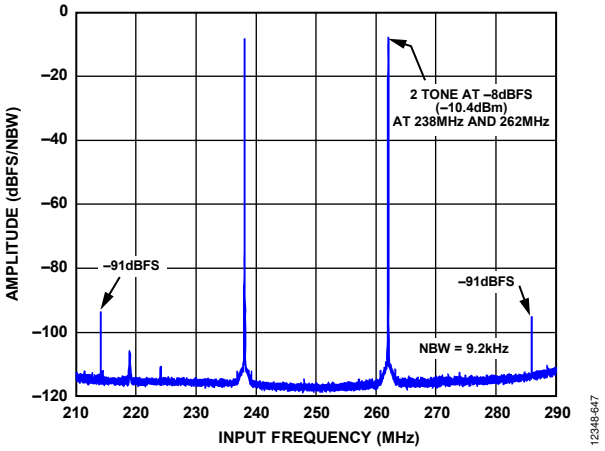

Figure 44. Two-Tone IMD Performance (f_1 = 238 MHz, f_2 = 262 MHz)

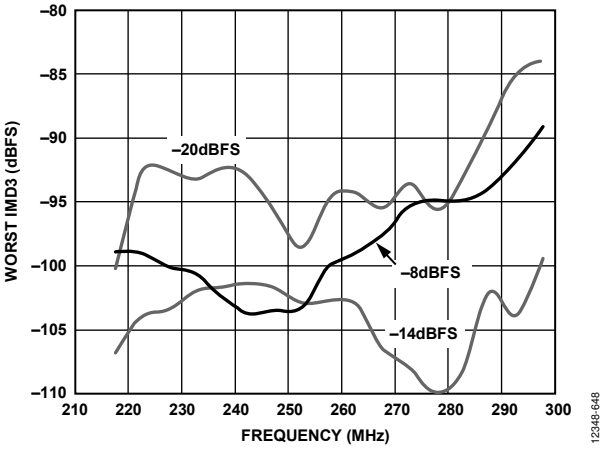

Figure 45. Swept Two-Tone Worst IMD3 vs. Frequency over Pass Band (Δf = 5 MHz for Two Tones, P_{IN} =−8 dBFS, −14 dBFS, and −20 dBFS)

NOMINAL PERFORMANCE FOR IF = 350 MHZ AND BW = 160 MHZ

F_{IF} = 350 MHz, BW = 160 MHz, F_{ADC} = 3.2 GHz, attenuator = 0 dB, L_{EXT} = 10 nH, maximum PIN_0dBFS setting, f_{DATA_IQ} = 266.7 MSPS, shuffler enabled (every clock cycle), with default threshold settings, unless otherwise noted.

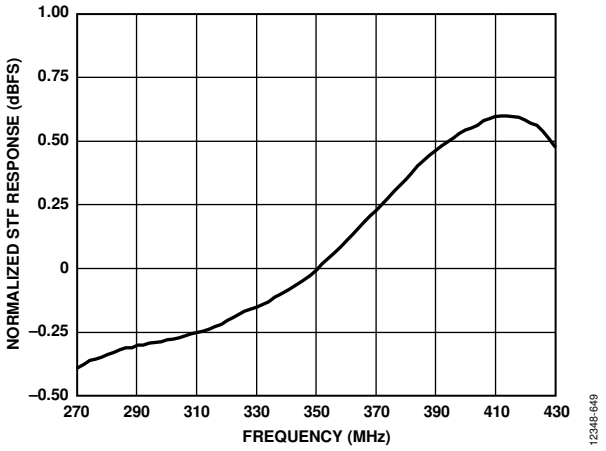

Figure 46. IF Pass Band Flatness (Includes Digital Filter)

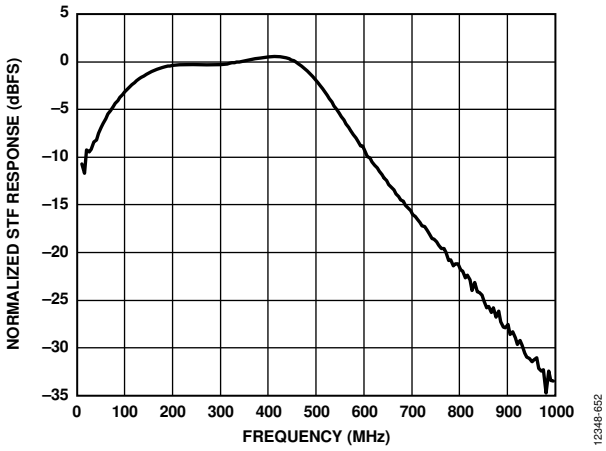

Figure 49. Wideband Frequency Response (Before Digital Filter)

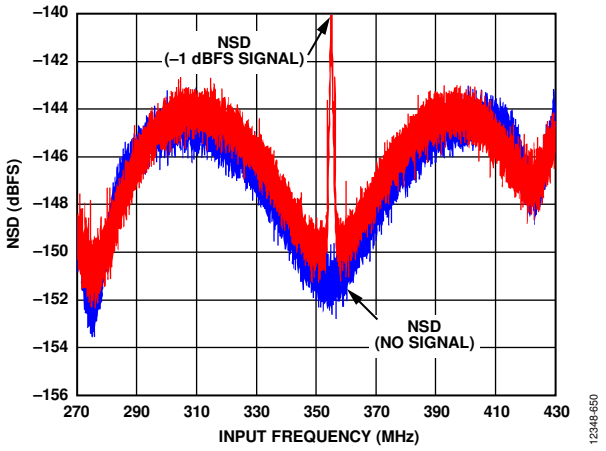

Figure 47. NSD With and Without Full-Scale CW at 355 MHz

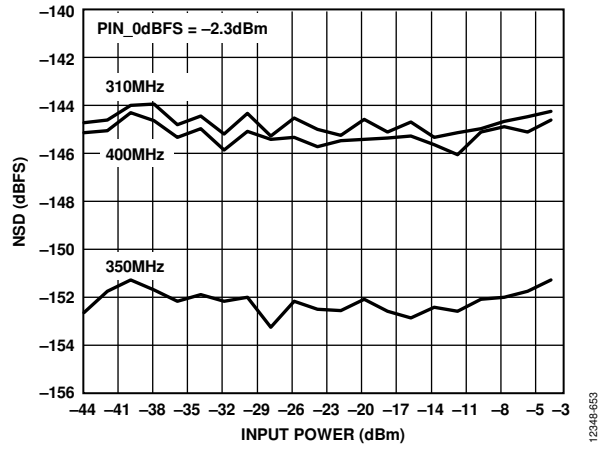

Figure 50. NSD vs. CW Input Power, CW at 355 MHz
(NSD Measured at 350 MHz as well as 350 MHz and 400 MHz Band Edges)

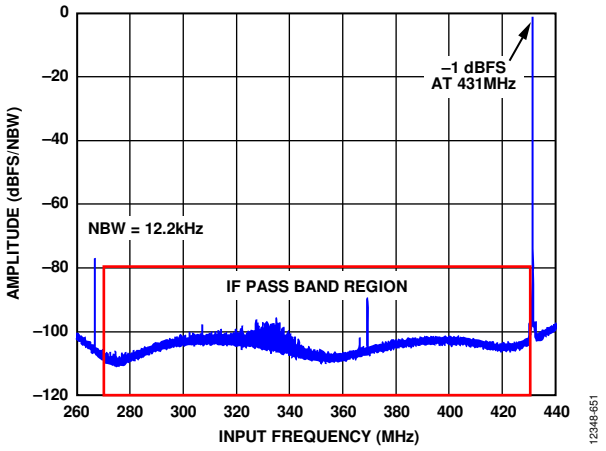

Figure 48. Spectral Plot of IF Pass Band Region with –1 dBFS CW at 431 MHz

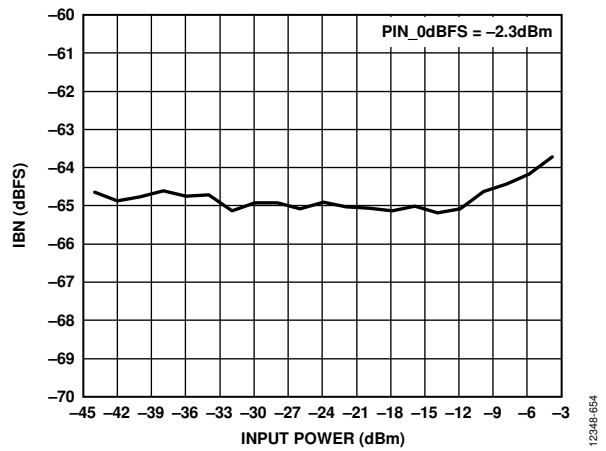

Figure 51. IBN in IF Pass Band Region (BW = 160 MHz) vs. Swept Single Tone Input Power with CW at 431 MHz

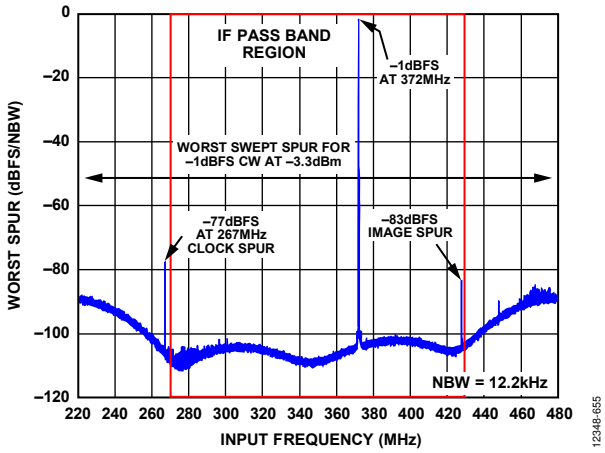

Figure 52. Worst Spur Falling in 160 MHz Pass Band for Swept CW from 217 MHz to 484 MHz

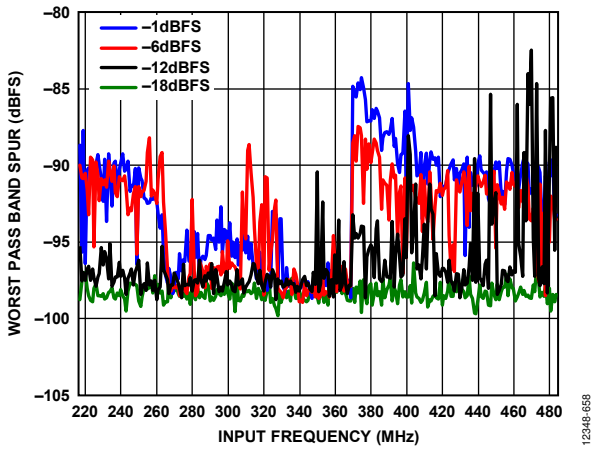

Figure 55. Swept Worst Pass Band Spur with CW Swept from 217 MHz to 484 MHz over P_{IN} = –1 dBFS, –6 dBFS, –12 dBFS, and –18 dBFS

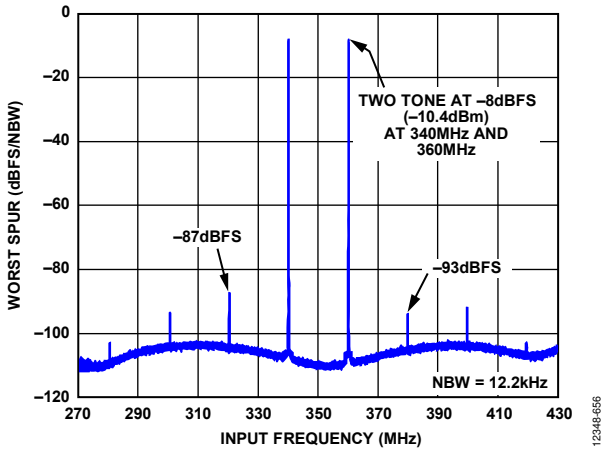

Figure 53. Two-Tone IMD Performance (f_1 = 340 MHz, f_2 = 360 MHz)

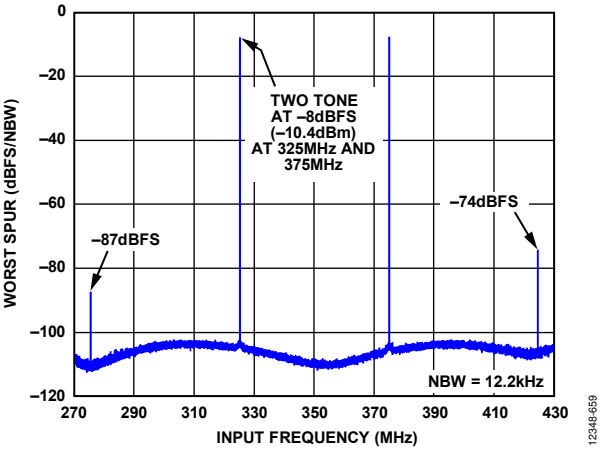

Figure 56. Two-Tone IMD Performance (f_1 = 325 MHz, f_2 = 375 MHz)

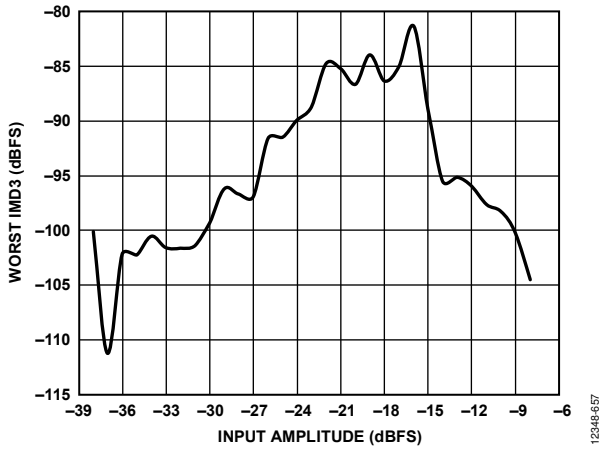

Figure 54. Swept Two-Tone Worst IMD3 vs. Tone Level (dBFS) (f_1 = 347.5 MHz, f_2 = 352.5 MHz)

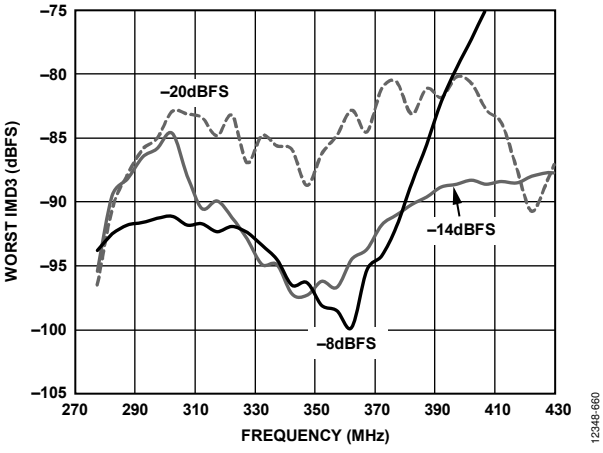

Figure 57. Swept Two-Tone Worst IMD3 vs. Frequency over Pass Band (Δf = 5 MHz for Two Tones, P_{IN} = –8 dBFS, –14 dBFS, and –20 dBFS)

EQUIVALENT CIRCUITS

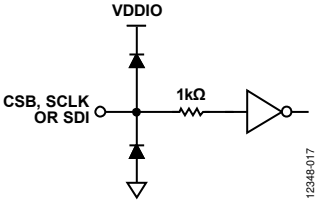

Figure 58. Equivalent CSB or SCLK Input Circuit

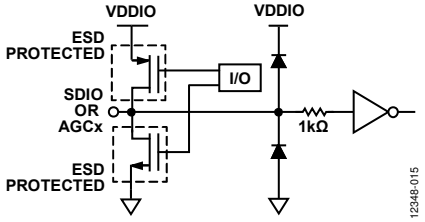

Figure 62. Equivalent SDIO or AGCx Input/Output Circuit

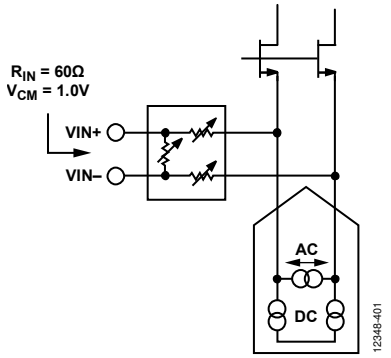

Figure 59. Equivalent Analog Input

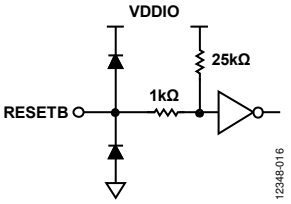

Figure 63. Equivalent RESETB Input Circuit

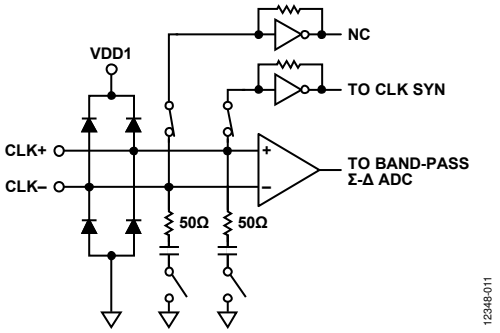

Figure 60. Equivalent Clock Input Circuit

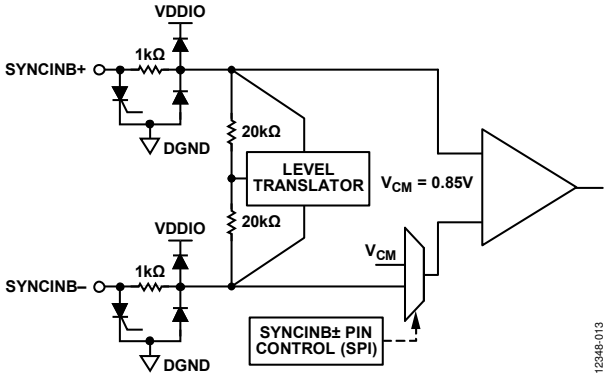

Figure 64. Equivalent SYNCINB± Input

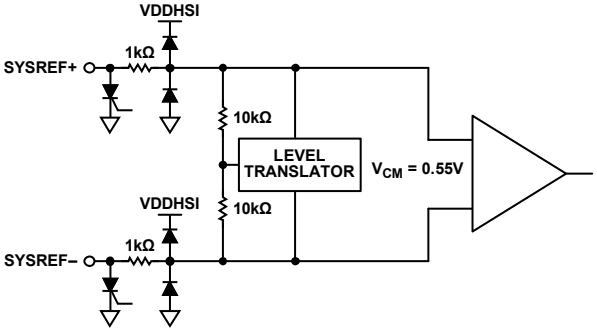

Figure 61. Equivalent SYSREF± Input

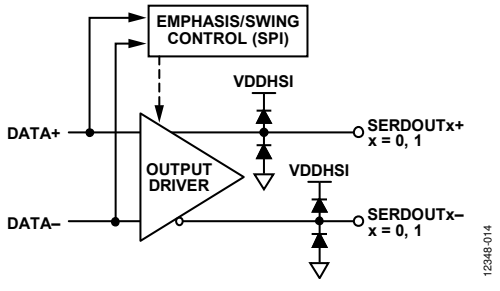

Figure 65. Digital CML Output Circuit

TERMINOLOGY

Noise Figure (NF)
NF is the degradation in SNR performance (in dB) of an input signal having a noise density of −174 dBm/Hz after it passes through a component or system. Mathematically,

$$NF = 10 \times \log(SNR_{IN}/SNR_{OUT})$$

The noise figure of the AD6676 is determined by the equation

$$NF = P_{IN} - (10 \times \log(BW)) - (-174.0 \text{ dBm/Hz}) - SNR$$

where:
P_{IN} is the input power of an unmodulated carrier.
BW is the noise measurement bandwidth.
−174.0 dBm/Hz is the thermal noise floor at 290 K.
SNR is the measured signal-to-noise ratio in dB of the AD6676.

Note that P_{IN} is set to a low level (that is, <−40 dBm) to minimize any degradation in measured SNR due to phase noise from either the input signal or Σ-Δ ADC clock source.

Noise Spectral Density (NSD)
NSD is the noise power normalized to 1 Hz bandwidth (at a particular frequency) relative to the full scale of the ADC (dBFS) and hence is given in units of dBFS/Hz. The AD6676, being a Σ-Δ ADC, displays a uneven NSD across its IF pass band. Both the worst-case NSD as well as NSD at the pass band center are reported. Note that NSD is calculated from the IBN measured over a 5 MHz bandwidth.

In-Band Noise (IBN)
IBN is the integrated noise power measured over a user defined bandwidth relative to the full scale of the ADC (dBFS). This bandwidth is typically equal to the IF pass band setting (BW) of the AD6676, unless otherwise noted.

Input Second-Order Intercept (IIP2)
IIP2 is a figure of merit used to quantify the second-order intermodulation distortion (IMD2) of a component or system. Two equal amplitude unmodulated carriers at specified frequencies (f_1 and f_2) injected into a nonlinear system exhibiting second-order nonlinearities produce IMD components at $f_1 - f_2$ and $f_1 + f_2$. For the AD6676, the two frequencies are situated at ½ the IF frequency (with a 2 MHz offset) at a power level corresponding to −6 dBFS at the IF center frequency with only the intermodulation term at $f_1 + f_2$ considered. IIP2 is the extrapolated tone power at which the intermodulation terms and the input tones have equal amplitude.

$$IIP2 = P_{IN} - IMD2$$

Input Third-Order Intercept (IIP3)
IIP3 is a figure of merit used to quantify the third-order intermodulation distortion (IMD3) of a component or system. Two equal amplitude unmodulated carriers at specified frequencies (f_1 and f_2) injected into a nonlinear system exhibiting third-order nonlinearities produce IMD components at $2f_1 - f_2$ and $2f_2 - f_1$. IIP3 is the extrapolated tone power at which the intermodulation terms and the input tones have equal amplitude.

$$IIP3 = P_{IN} - IMD3/2$$

Note that the third-order IMD performance of an ADC does not necessarily follow the 3:1 rule that is typical of RF/IF linear devices. IMD performance is dependent on the dual tone frequencies, signal input levels, and ADC clock rate.

Worst In-Band Spur (SFDR)
Worst in-band spur is the worst spur falling in the IF pass band relative to the full scale of the ADC (dBFS) when a single tone with defined power level is stepped (typically 1 MHz increments) across a user defined frequency range. Note that this worst spur can often be an image (or clock) related spur depending on the IF, BW, and IQ output data rate setting of the AD6676 and on the sweep range.

Signal Transfer Function (STF)
STF is the frequency response of the output signal of the ADC relative to a swept single tone at its input. The STF presented for different AD6676 setup conditions in the Typical Performance Characteristics section shows the STF over the IF pass band after the digital filter to highlight pass band flatness. The wideband STF response is measured before the digital filter to highlight the pass band response of the AD6676 Σ-Δ ADC.

THEORY OF OPERATION

OVERVIEW

The AD6676 is a highly integrated and flexible IF subsystem capable of digitizing IF signals. The ability to tune the IF frequency and bandwidth allows the Σ-Δ ADC to be optimized for different applications while trading off bandwidth for dynamic range. To facilitate its evaluation and design in, a software tool that is part of the AD6676EBZ development platform must be used to configure and evaluate the device. This tool saves the SPI initialization and configuration sequence to a file for later use. A screenshot of the GUI front panel (see Figure 66) shows the different user specified application parameters that configure the AD6676. The following discussion provides more insight into the device operation and how these application parameters affect performance.

Figure 66. Screenshot of AD6676 GUI Software Tool that Facilitates Device Configuration and Evaluation

A functional block diagram of the AD6676 is shown Figure 67. The focal point of the AD6676 is its continuous time, band-pass Σ-Δ ADC that operates with a clock rate between 2.0 GHz and 3.2 GHz. An on-chip controller configures the Σ-Δ ADC based on the user specified application parameters. The Σ-Δ ADC provides exceptional dynamic range and pass band flatness within the desired IF span while limiting out-of-band peaking to less than 0.5 dB. An on-chip clock synthesizer supplies a 2.94 GHz to 3.2 GHz Σ-Δ ADC clock. Alternatively, an external clock can be supplied for lower clock rates or improved phase noise performance.

On-chip digital signal processing blocks include a quadrature digital downconverter (QDDC) followed by selectable decimation filters supporting decimation factors of 12, 16, 24, or 32. The QDDC performs a complex shift of the desired IF pass band such that it is centered about dc, that is, zero IF. Cascaded decimation filters remove the inherent out-of-band noise of the ADC along with any other out-of-band signal content such that the 16-bit complex IQ data is reduced to a more manageable data rate for transfer to the host via a single or dual lane JESD204B interface supporting up to 5.333 Gbps lane rates.

The AD6676 also includes features for AGC support and/or level-planning optimization. AGC support includes the ability to monitor peak power at the Σ-Δ ADC output or rms power after the first internal decimation stage. The host can initiate fast AGC action by configuring various flags whose status are made available on the AGC4 to AGC1 pins. Flags can be set with programmable thresholds indicating whether the signal level is above or below a defined level. A 27 dB attenuator with a step size of 1 dB is available for IF AGC control or level planning optimization during initial system calibration. Alternatively, the nominal 0 dBFS full-scale input power level (PIN_0dBFS) of −2 dBm can be reduced by up to 12 dB thus further reducing the RF/IF gain requirements. The SPI programs numerous parameters of the AD6676, allowing the device to be optimized for a variety of applications.

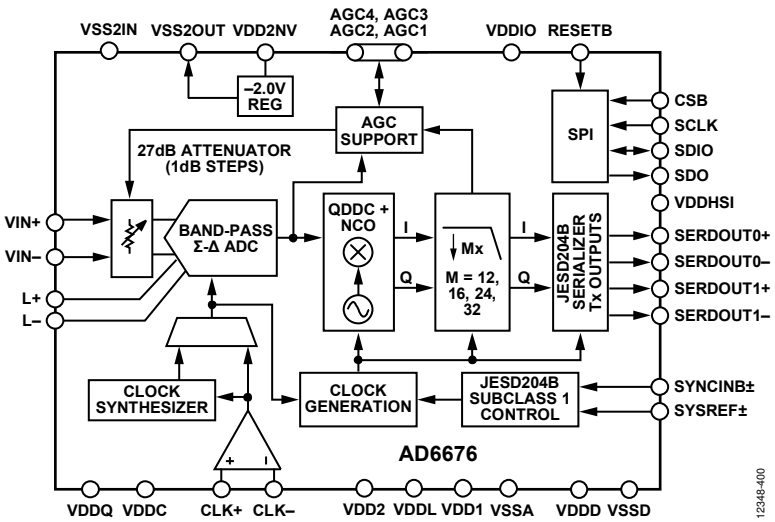

Figure 67. Functional Block Diagram

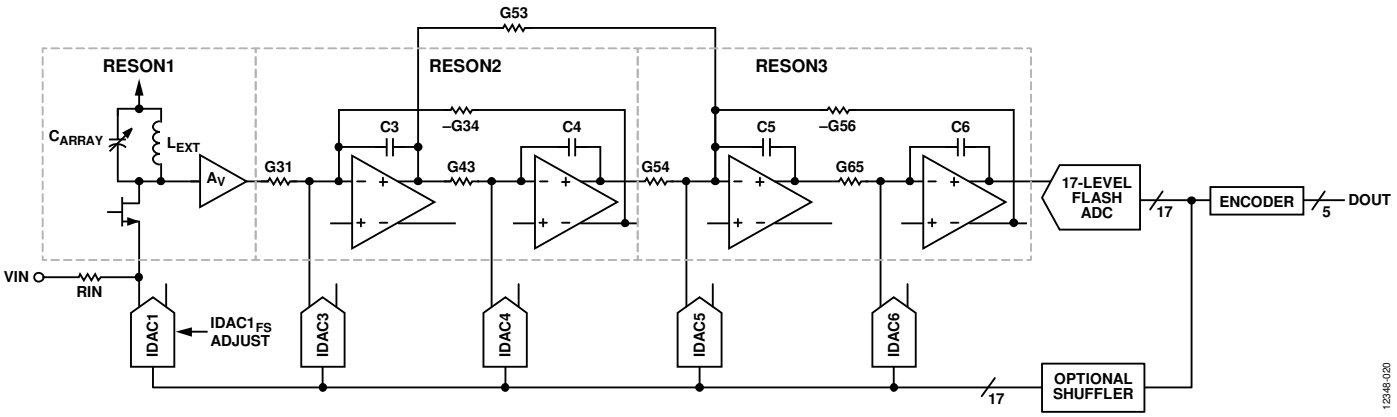

Figure 68. Simplified Single-Ended Representation of the Band-Pass Σ-Δ ADC Modulator

BAND-PASS Σ-Δ ADC ARCHITECTURE

Figure 68 shows a simplified single-ended representation of the AD6676 band-pass Σ-Δ ADC. It is a sixth-order modulator consisting of three cascaded second-order continuous-time resonators with feedback DACs and an oversampling quantizer. The first resonator (RESON1) is based on a LC tank with its resonant frequency tuned via C_{ARRAY} to the IF center while the second and third resonators (RESON2 and RESON3) are active RC-based with their resonant frequencies tuned to frequencies offset symmetrically about the IF. These resonant frequencies correspond to the zero locations of the Σ-Δ ADC quantization noise and are set according to the user defined IF frequency and bandwidth.

A 17-level flash ADC oversamples the analog output of RESON3 with the digital output of the flash ADC feeding back to each of the resonators via current mode DACs (IDACx). Note that because the ADC thermometer code output can range from −8 to +8, it is represented by five bits that are passed to the AD6676 digital path. The IDAC1 full-scale current setting ($IDAC1_{FS}$) sets the maximum full-scale input power level (PIN_0DBFS). The full-scale settings of the other IDACs set the pole location of the modulator to achieve a flat pass band response. Lastly, a programmable shuffler follows the flash ADC to improve the linearity performance of the AD6676 under large signal conditions.

The tunable nature of the Σ-Δ ADC is a result of the full-scale current of the feedback DACs, as well as the conductances (G) and capacitances (C) associated with each resonator. The value of these programmable components are calculated from the user specified application parameters listed in Table 7. The impact of each of these parameters on the performance of the AD6676 is described in subsequent sections.

Table 7. List of User Specified Application Parameters That Determine the Σ-Δ ADC Internal Settings

Application Parameter	Description	SPI Register(s)
F_{IF}	IF center frequency in MHz	0x102, 0x103
BW	IF pass band bandwidth in MHz	0x104, 0x105
F_{ADC}	Σ-Δ ADC clock rate in MHz	0x100, 0x101
L_{EXT}	External inductor value in nH	0x106
MRGN	Margin offset to set resonator frequency in MHz	0x107 to 0x109
$IDAC1_{FS}$	Full-scale current of IDAC1 that sets PIN_0dBFS level	0x10A

The on-chip controller is used only during device initialization and performs the following tasks:

- Power-up negative regulator (used by IDACs)
- Calibrate RESON1 and 17-level flash ADC
- Tune Σ-Δ ADC based on user input parameters
- Set up PLL used by JESD204B PHY

After device initialization, the on-chip controller is disabled; it is not used during normal device operation.

Signal and Noise Transfer Functions

The frequency domain response of a Σ-Δ ADC is defined by its signal and noise transfer functions (STF and NTF). Figure 69 shows a simplified feedback model of a Σ-Δ modulator with the ADC quantization error modeled as an additive noise source (E) after the loop filter (H). The STF is the frequency response of the output signal (V) relative to a swept single tone at its input (U) while the NTF is the frequency response of the ADC quantization noise (that is, V/E) that undergoes noise shaping due to of the loop filter of the ADC. Note that the ADC and DACs within the feedback loop operate at a much higher clock rate than a traditional open-loop ADC in which only the Nyquist criterion must be satisfied ($F_{ADC} = 2 \times BW$).

The oversampling ratio (OSR) is a key parameter of any Σ-Δ ADC and is defined as follows:

$$OSR = F_{ADC}/(2 \times BW) \quad (1)$$