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135 MHz BW IF Diversity Receiver

Data Sheet **AD6679**

FEATURES

- Parallel LVDS (DDR) outputs
- In-band SFDR = 82 dBFS at 340 MHz (500 MSPS)
- In-band SNR = 67.8 dBFS at 340 MHz (500 MSPS)
- 1.1 W total power per channel at 500 MSPS (default settings)
- Noise density = −153 dBFS/Hz at 500 MSPS
- 1.25 V, 2.50 V, and 3.3 V dc supply operation
- Flexible input range
  - 1.46 V p-p to 2.06 V p-p (2.06 V p-p nominal)
- 95 dB channel isolation/crosstalk
- Amplitude detect bits for efficient automatic gain control (AGC) implementation
- Noise shaping requantizer (NSR) option for main receiver function
- Variable dynamic range (VDR) option for digital predistortion (DPD) function
- 2 integrated wideband digital processors per channel
  - 12-bit numerically controlled oscillator (NCO), up to 4 cascaded half-band filters
- Differential clock inputs
- Integer clock divide by 1, 2, 4, or 8
- Energy saving power-down modes
- Small signal dither

APPLICATIONS

- Diversity multiband, multimode digital receivers
  - 3G/4G, TD-SCDMA, W-CDMA, GSM, LTE, LTE-A
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers

GENERAL DESCRIPTION

The AD6679 is a 135 MHz bandwidth mixed-signal intermediate frequency (IF) receiver. It consists of two, 14-bit, 500 MSPS analog-to-digital converters (ADCs) and various digital signal processing blocks consisting of four wideband DDCs, an NSR, and VDR monitoring. It has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed to support communications applications capable of sampling wide bandwidth analog signals of up to 2 GHz. The AD6679 is optimized for wide input bandwidth, high sampling rates, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

FUNCTIONAL BLOCK DIAGRAM

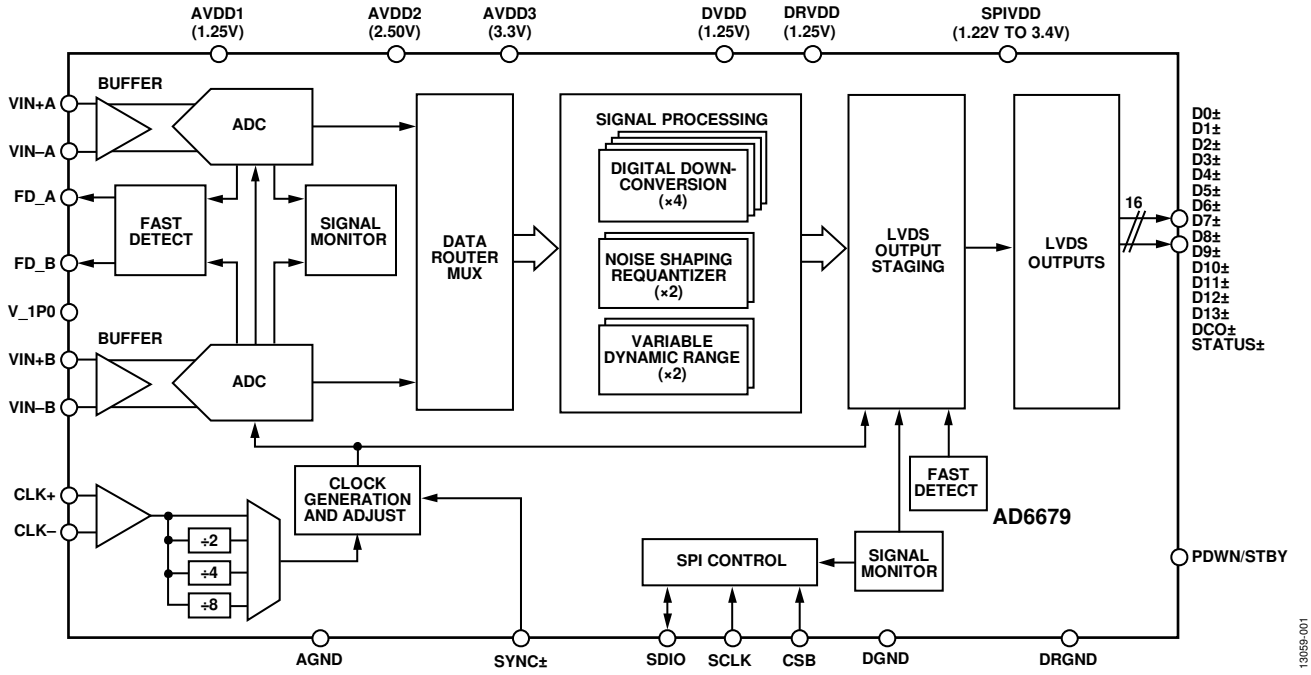

Figure 1.

Rev. B Document Feedback

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Tel: 781.329.4700
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COMPARABLE PARTS

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EVALUATION KITS

- AD6679 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1371: Variable Dynamic Range

Data Sheet

- AD6679: 135 MHz BW IF Diversity Receiver Data Sheet

DESIGN RESOURCES

- AD6679 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD6679 EngineerZone Discussions.

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5/15—Revision 0: Initial Version

The analog input and clock signals are differential inputs. The ADC data outputs are internally connected to four DDCs through a crossbar mux. Each DDC consists of up to five cascaded signal processing stages: a 12-bit frequency translator (NCO) and up to four half-band decimation filters.

Each ADC output is connected internally to an NSR block. The integrated NSR circuitry allows improved SNR performance in a smaller frequency band within the Nyquist bandwidth. The device supports two different output modes, selectable via the serial port interface (SPI). With the NSR feature enabled, the outputs of the ADCs are processed such that the AD6679 supports enhanced SNR performance within a limited portion of the Nyquist bandwidth while maintaining a 9-bit output resolution.

Each ADC output is also connected internally to a VDR block. This optional mode allows full dynamic range for defined input signals. Inputs that are within a defined mask (based on DPD applications) pass unaltered. Inputs that violate this defined mask result in the reduction of the output resolution.

With VDR, the dynamic range of the observation receiver is determined by a defined input frequency mask. For signals falling within the mask, the outputs are presented at the maximum resolution allowed. For signals exceeding defined power levels within this frequency mask, the output resolution is truncated. This mask is based on DPD applications and supports tunable real IF sampling, and zero IF or complex IF receive architectures.

Operation of the AD6679 between the DDC, NSR, and VDR modes is selectable via SPI-programmable profiles.

In addition to the DDC blocks, the AD6679 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect control bits in Register 0x245 of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly reduce the system gain to avoid an overrange condition at the ADC input. In addition to the fast detect outputs, the AD6679 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal that the ADC digitized.

The output data is routed directly to the one external 14-bit LVDS output port, supporting double data rate (DDR) formatting. An external data clock and a clock status bit are offered for data capture flexibility.

The AD6679 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 1.8 V capable 3-wire SPI.

The AD6679 is available in a Pb-free, 196-ball BGA_ED, and is specified over the −40°C to +85°C industrial temperature range.

PRODUCT HIGHLIGHTS

1. Wide full power bandwidth IF sampling of signals up to 2 GHz.
2. Buffered inputs with programmable input termination eases filter design and implementation.
3. Four integrated wideband decimation filters and NCO blocks support multiband receivers.
4. Flexible SPI controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection and signal monitoring.
6. Programmable fast overrange detection.
7. 12 mm × 12 mm, 196-ball BGA_ED.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference (V_{REF}), A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−0.3	0	+0.3	% FSR
Offset Matching	Full		0	0.3	% FSR
Gain Error	Full	−6.5	0	+6.5	% FSR
Gain Matching	Full		0	5.0	% FSR
Differential Nonlinearity (DNL)	Full	−0.6	±0.5	+0.7	LSB
Integral Nonlinearity (INL)	Full	−4.5	±2.5	+5.0	LSB
TEMPERATURE DRIFT					
Offset Error	Full		±3		ppm/°C
Gain Error	Full		−39		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Voltage	Full		1.0		V
INPUT REFERRED NOISE					
V_{REF} = 1.0 V	25°C		2.04		LSB rms
ANALOG INPUTS					
Differential Input Voltage Range (Internal V_{REF} = 1.0 V)	Full	1.46	2.06	2.06	V p-p
Common-Mode Voltage (V_{CM})	Full		2.05		V
Differential Input Capacitance[1]	Full		1.5		pF
Analog Full Power Bandwidth	Full		2		GHz
POWER SUPPLY					
AVDD1	Full	1.22	1.25	1.28	V
AVDD2	Full	2.44	2.50	2.56	V
AVDD3	Full	3.2	3.3	3.4	V
DVDD	Full	1.22	1.25	1.28	V
DRVDD	Full	1.22	1.25	1.28	V
SPIVDD	Full	1.22	1.8	3.4	V
I_{AVDD1}	Full		464	503	mA
I_{AVDD2}	Full		396	455	mA
I_{AVDD3}[2]	Full		89	100	mA
I_{DVDD} (Default SPI—NSR Mode)	Full		141	164	mA
I_{DVDD} (VDR Mode)	Full		117	138	mA
I_{DRVDD}[3]	Full		110	123	mA
I_{SPIVDD}	Full		5	6	mA
POWER CONSUMPTION					
Total Power Dissipation					
Default SPI—NSR Mode[3]	Full		2.2	2.37	W
VDR Mode[3]	Full		2.16	2.34	W
Power-Down Dissipation	Full		0.71		W
Standby[4]	Full		1.4		W

[1] Differential capacitance is measured between the VIN+x and VIN−x pins (x = A, B).
[2] AVDD3 current changes based on the Buffer Control 1 setting (see Figure 46).
[3] Parallel interleaved LVDS mode. The power dissipation on DRVDD changes with the output data mode used.
[4] Standby can be controlled by the SPI.

AC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
ANALOG INPUT FULL SCALE	Full		2.06		V p-p
NOISE DENSITY[2]	Full		−153		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[3]					
VDR Mode (Input Mask Not Triggered)					
f_{IN} = 10 MHz	25°C		68.9		dBFS
f_{IN} = 170 MHz	Full	67.5	68.6		dBFS
f_{IN} = 340 MHz	25°C		67.8		dBFS
f_{IN} = 450 MHz	25°C		67.3		dBFS
f_{IN} = 765 MHz	25°C		63.9		dBFS
f_{IN} = 985 MHz	25°C		62.8		dBFS
f_{IN} = 1950 MHz	25°C		59.0		dBFS
NSR Enabled (21% Bandwidth (BW) Mode)					
f_{IN} = 10 MHz	25°C		75.0		dBFS
f_{IN} = 170 MHz	25°C		74.8		dBFS
f_{IN} = 340 MHz	25°C		74.0		dBFS
f_{IN} = 450 MHz	25°C		73.1		dBFS
f_{IN} = 765 MHz	25°C		69.7		dBFS
f_{IN} = 985 MHz	25°C		68.1		dBFS
f_{IN} = 1950 MHz	25°C		64.6		dBFS
NSR Enabled (28% BW Mode)					
f_{IN} = 10 MHz	25°C		72.4		dBFS
f_{IN} = 170 MHz	25°C		72.3		dBFS
f_{IN} = 340 MHz	25°C		71.6		dBFS
f_{IN} = 450 MHz	25°C		71.0		dBFS
f_{IN} = 765 MHz	25°C		67.7		dBFS
f_{IN} = 985 MHz	25°C		66.8		dBFS
f_{IN} = 1950 MHz	25°C		63.1		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)[3]					
VDR Mode (Input Mask Not Triggered)					
f_{IN} = 10 MHz	25°C		68.7		dBFS
f_{IN} = 170 MHz	Full	67	68.5		dBFS
f_{IN} = 340 MHz	25°C		67.6		dBFS
f_{IN} = 450 MHz	25°C		67.2		dBFS
f_{IN} = 765 MHz	25°C		63.8		dBFS
f_{IN} = 985 MHz	25°C		62.5		dBFS
f_{IN} = 1950 MHz	25°C		58.3		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)[3]					
VDR Mode (Input Mask Not Triggered)					
f_{IN} = 10 MHz	25°C		11.1		Bits
f_{IN} = 170 MHz	Full	10.8	10.9		Bits
f_{IN} = 340 MHz	25°C		10.8		Bits
f_{IN} = 450 MHz	25°C		10.8		Bits
f_{IN} = 765 MHz	25°C		10.3		Bits
f_{IN} = 985 MHz	25°C		10.1		Bits
f_{IN} = 1950 MHz	25°C		9.5		Bits

Parameter[1]	Temperature	Min	Typ	Max	Unit
SPURIOUS FREE DYNAMIC RANGE (SFDR), SECOND OR THIRD HARMONIC[3]					
VDR Mode (Input Mask Not Triggered)					
f_{IN} = 10 MHz	25°C		83		dBFS
f_{IN} = 170 MHz	Full	76	85		dBFS
f_{IN} = 340 MHz	25°C		82		dBFS
f_{IN} = 450 MHz	25°C		86		dBFS
f_{IN} = 765 MHz	25°C		81		dBFS
f_{IN} = 985 MHz	25°C		76		dBFS
f_{IN} = 1950 MHz	25°C		69		dBFS
WORST OTHER (EXCLUDING SECOND OR THIRD HARMONIC)[3]					
VDR Mode (Input Mask Not Triggered)					
f_{IN} = 10 MHz	25°C		−93		dBFS
f_{IN} = 170 MHz	Full		−94		dBFS
f_{IN} = 340 MHz	25°C		−90		dBFS
f_{IN} = 450 MHz	25°C		−92		dBFS
f_{IN} = 765 MHz	25°C		−89		dBFS
f_{IN} = 985 MHz	25°C		−89		dBFS
f_{IN} = 1950 MHz	25°C		−85		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD)[3], A_{IN1} AND A_{IN2} = −7.0 dBFS					
f_{IN1} = 185 MHz, f_{IN2} = 188 MHz	25°C		−88		dBFS
f_{IN1} = 338 MHz, f_{IN2} = 341 MHz	25°C		−87		dBFS
CROSSTALK[4]	25°C		95		dB
FULL POWER BANDWIDTH	25°C		2		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Noise density is measured at a low analog input frequency (30 MHz).
[3] See Table 11 for the recommended settings for full-scale voltage and buffer control settings.
[4] Crosstalk is measured at 185 MHz with a −1.0 dBFS analog input on one channel and no input on the adjacent channel.

DIGITAL SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	600	1200	1800	mV p-p
Input Common-Mode Voltage	Full		0.85		V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
SYSTEM REFERENCE INPUTS (SYNC+, SYNC−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance (Differential)	Full			2.5	pF
LOGIC INPUTS (SDIO, SCLK, CSB, PDWN/STBY)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full		0.8 × SPIVDD		V
Logic 0 Voltage	Full	0	0.2 × SPIVDD		V
Input Resistance	Full		30		kΩ

Parameter	Temperature	Min	Typ	Max	Unit
LOGIC OUTPUT (SDIO)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage (I_{OH} = 800 µA)	Full		0.8 × SPIVDD		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full		0.2 × SPIVDD		V
LOGIC OUTPUTS (FD_A, FD_B)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8	SPIVDD		V
Logic 0 Voltage	Full	0	0		V
Input Resistance	Full		30		kΩ
DIGITAL OUTPUTS (D0± to D13±, A Dx/Dy± and B Dx/Dy±, DATA0± to DATA7±, DCO±, OVR±, FCO±, and STATUS±)					
Logic Compliance	Full		LVDS		
ANSI Mode					
Differential Output Voltage (V_{OD})	Full	230	350	430	mV
Output Offset Voltage (V_{OS})	Full	0.58	0.70	0.85	V
Reduced Swing Mode					
Differential Output Voltage (V_{OD})	Full	120	200	235	mV
Output Offset Voltage (V_{OS})	Full	0.59	0.70	0.83	V

SWITCHING SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, unless otherwise noted.

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK					
Clock Rate (at CLK+/CLK− Pins)	Full	0.3		4	GHz
Sample Rate					
Maximum[1]	Full	500			MSPS
Minimum[2]	Full	250			MSPS
Clock Pulse Width					
High	Full	1000			ps
Low	Full	1000			ps
LVDS DATA OUTPUT					
Data Propagation Delay (t_{PD})[3]	Full		2.225		ns
DCO± Propagation Delay (t_{DCO})[3]	Full		2.2		ns
DCO± to Data Skew—Rising Edge Data (t_{SKEWR})[3]	Full	−150	−25	+100	ps
DCO± to Data Skew—Falling Edge Data (t_{SKEWF})[3]	Full	−150	−25	+100	ps
DCO± and Data Duty Cycle	Full	44	50	56	%
FCO± Propagation Delay (t_{FCO})[4]	Full		2.2		ns
DCO± to FCO± Skew (t_{FRAME})[4]	Full	−150	−25	+100	ps
DCO Output Frequency	Full			500	MHz
Output Date Rate	Full			1000	Mbps
LATENCY					
Pipeline Latency	Full		33		Clock cycles
NSR Latency[5]	Full		8		Clock cycles
NSR HB Filter Latency[5]	Full		24		Clock cycles
VDR Latency[5]	Full		8		Clock cycles
HB1 Filter Latency[5]	Full		50		Clock cycles
HB1 + HB2 Filter Latency[5]	Full		101		Clock cycles
HB1 + HB2 + HB3 Filter Latency[5]	Full		217		Clock cycles
HB1 + HB2 + HB3 + HB4 Filter Latency[5]	Full		433		Clock cycles
Fast Detect Latency	Full		28		Clock cycles

Parameter	Temperature	Min	Typ	Max	Unit
Wake-Up Time[6]					
Standby	25°C		1		ms
Power-Down[6]	25°C			4	ms
APERTURE					
Aperture Delay (t_A)	Full		530		ps
Aperture Uncertainty (Jitter, t_J)	Full		55		fs rms
Out of Range Recovery Time	Full		1		Clock cycles

[1] The maximum sample rate is the clock rate after the divider.
[2] The minimum sample rate operates at 300 MSPS with L = 2 or L = 1.
[3] This specification is valid for parallel interleaved, channel multiplexed, and byte mode output modes.
[4] This specification is valid for byte mode output mode only.
[5] Add this value to the pipeline latency specification to achieve total latency through the AD6679.
[6] Wake-up time is defined as the time required to return to normal operation from power-down mode or standby mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK± to SYNC± TIMING REQUIREMENTS					
t_{SU_SR}	Device clock to SYNC± setup time		117		ps
t_{H_SR}	Device clock to SYNC± hold time		−96		ps
SPI TIMING REQUIREMENTS	See Figure 3				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK is in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK is in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 3)	10			ns

Timing Diagrams

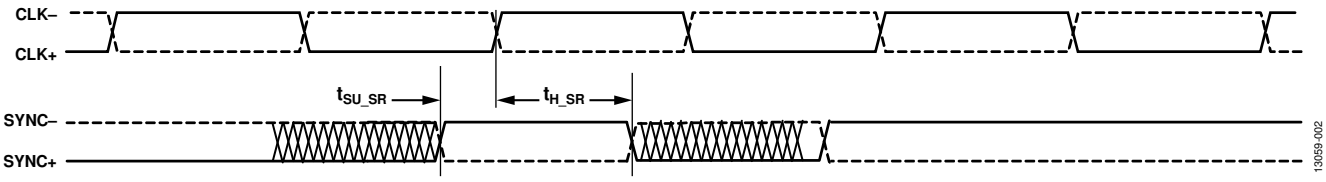


Figure 2. SYNC± Setup and Hold Timing

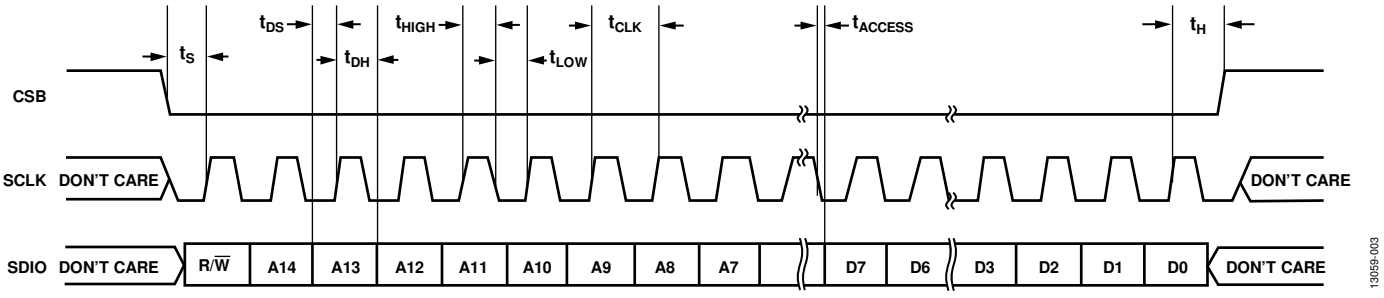
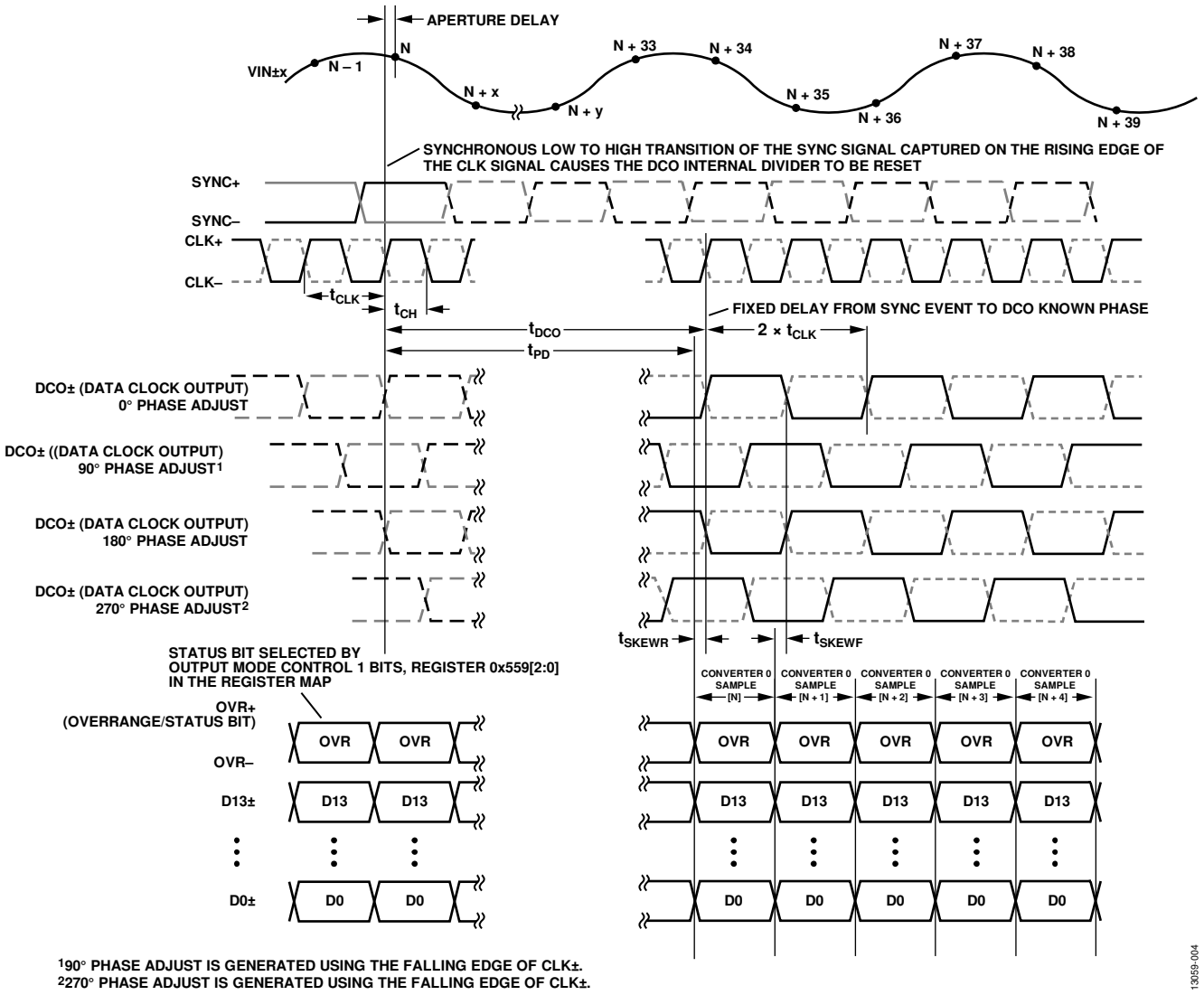


Figure 3. Serial Port Interface Timing Diagram



1 90° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
2 270° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.

Figure 4. Parallel Interleaved Mode—One Virtual Converter (Decimate by 1)

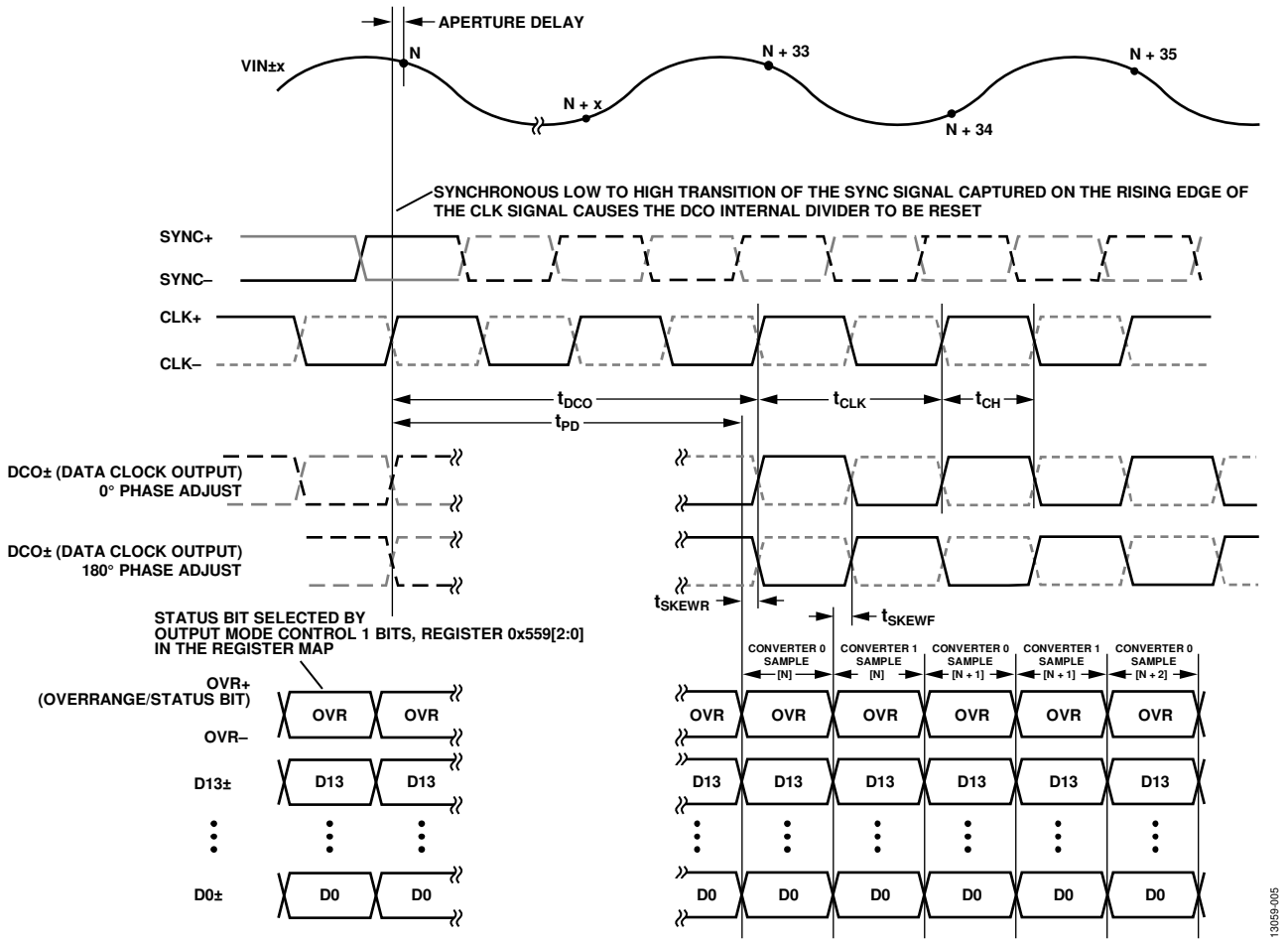


Figure 5. Parallel Interleaved Mode—Two Virtual Converters (Decimate by 1)

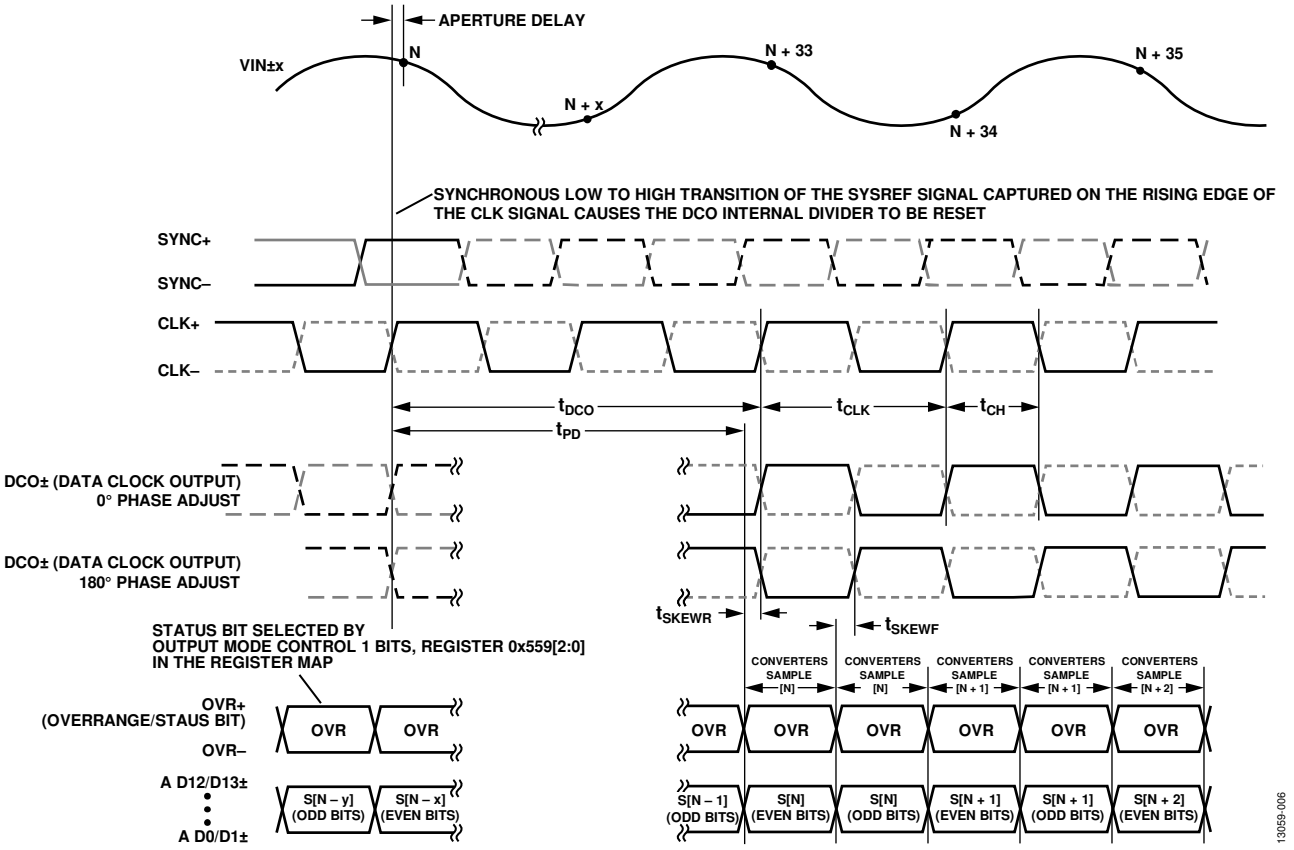


Figure 6. Channel Multiplexed (Even/Odd) Mode—One Virtual Converter (Decimate by 1)

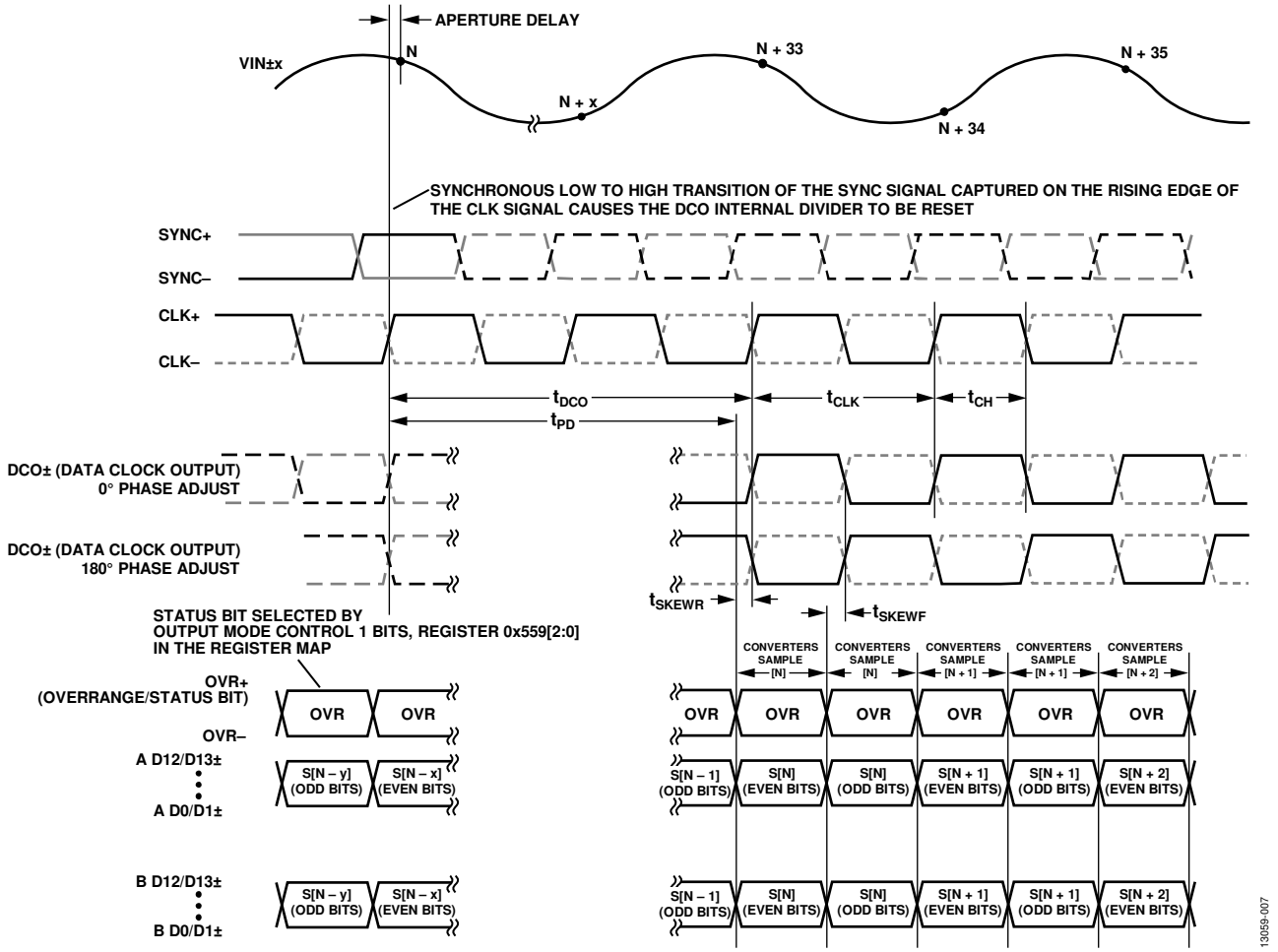
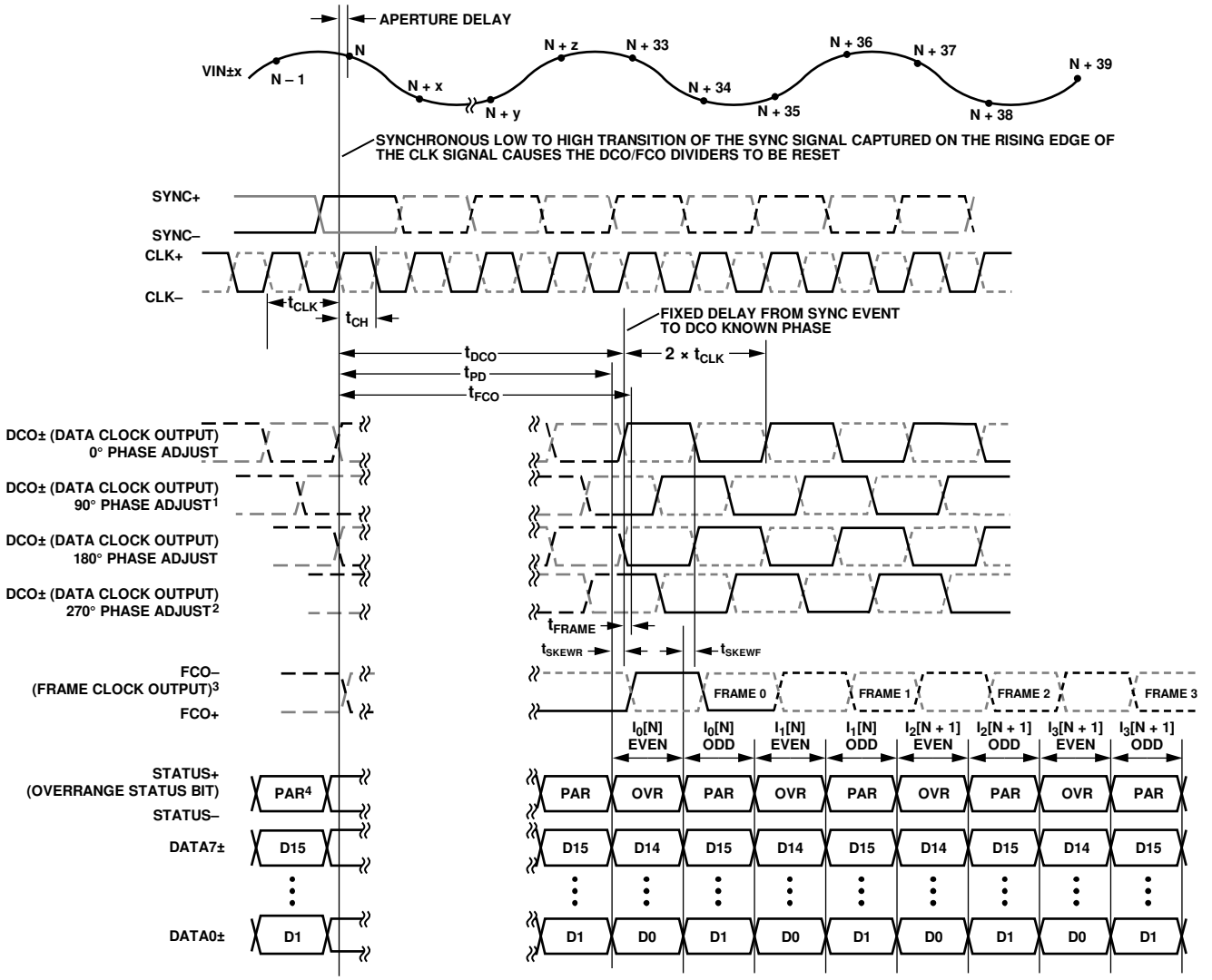
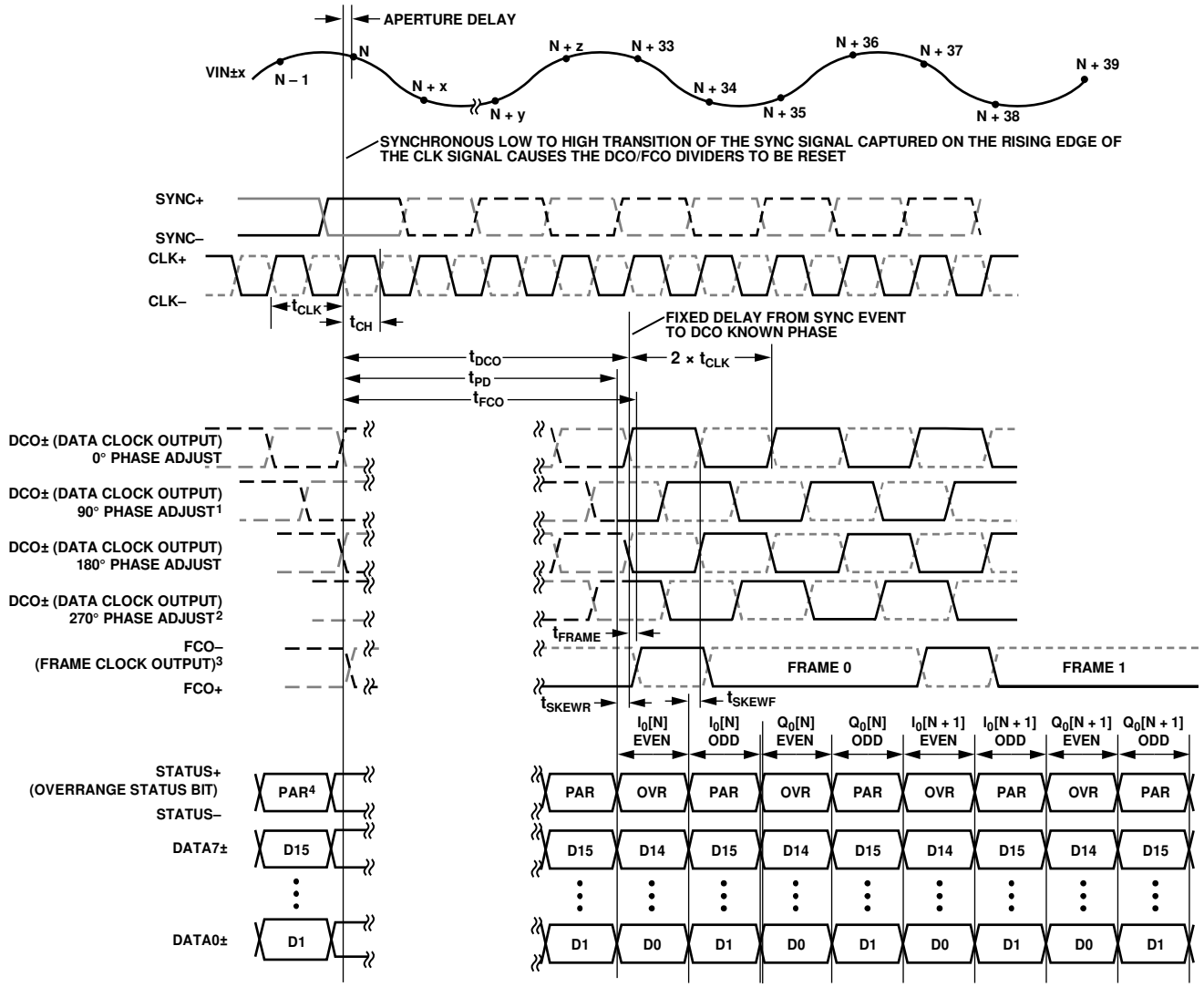


Figure 7. Channel Multiplexed (Even/Odd) Mode—Two Virtual Converters (Decimate by 1)



1 90° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
2 270° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
3 FRAME CLOCK OUTPUT SUPPORTS THREE MODES OF OPERATION:
1) ENABLED (ALWAYS ON)
2) DISABLED (ALWAYS OFF)
3) GAPPED PERIODIC (CONDITIONALLY ENABLED BASED ON PSEUDORANDOM BIT)
4 STATUS BIT SELECTED BY THE OUTPUT MODE CONTROL 1 BITS, REGISTER 0x559[2:0] IN THE REGISTER MAP.

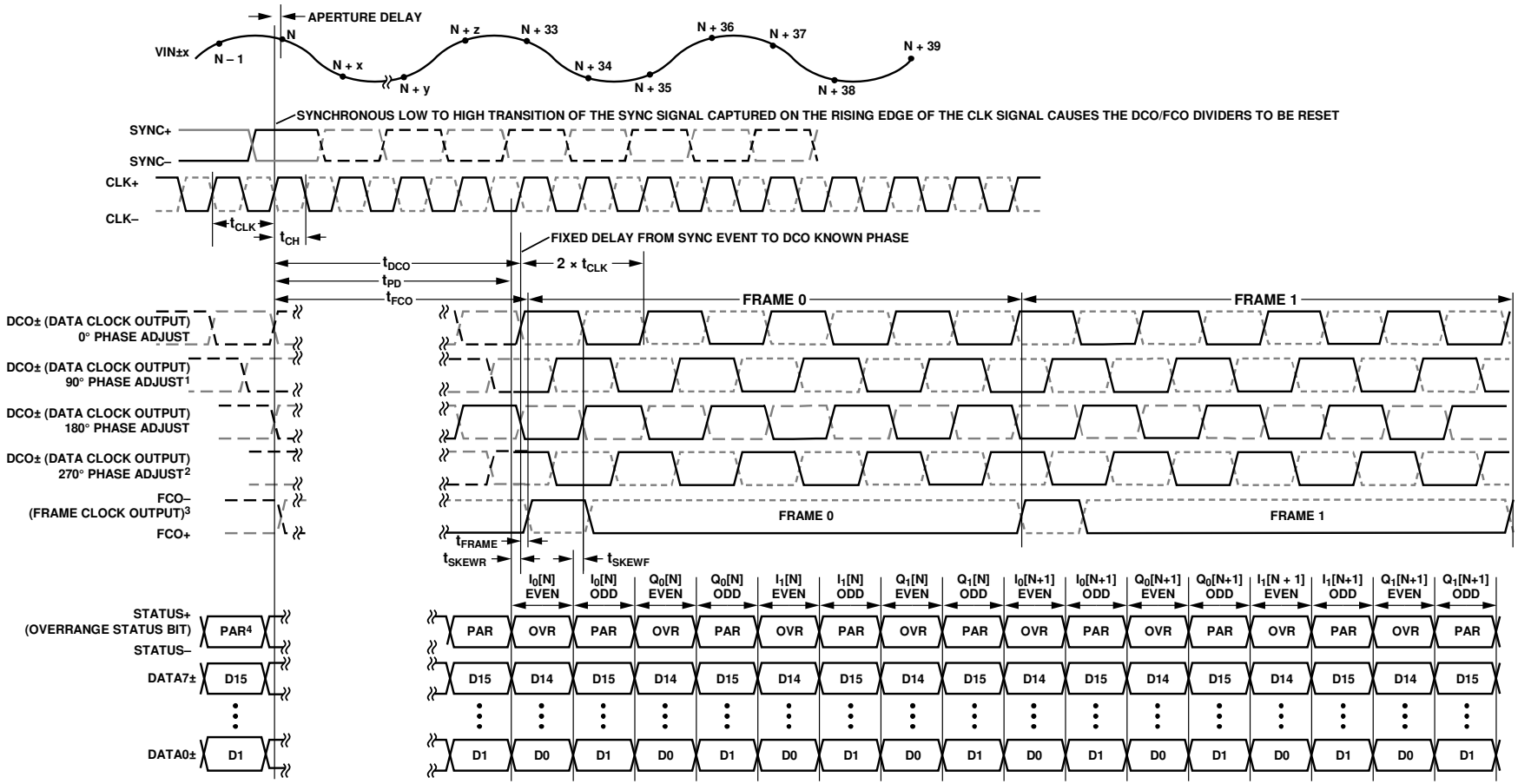
Figure 8. LVDS Byte Mode—One Virtual Converter, One DDC (I Only, Decimate by 2)



1 90° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
2 270° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
3 FRAME CLOCK OUTPUT SUPPORTS THREE MODES OF OPERATION:
1) ENABLED (ALWAYS ON)
2) DISABLED (ALWAYS OFF)
3) GAPPED PERIODIC (CONDITIONALLY ENABLED BASED ON PSEUDORANDOM BIT)
4 STATUS BIT SELECTED BY THE OUTPUT MODE CONTROL 1 BITS, REGISTER 0x559[2:0] IN THE REGISTER MAP.

13059-008

Figure 9. LVDS Byte Mode—Two Virtual Converters, One DDC (I/Q Decimate by 4)



1 90° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
2 270° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
3 FRAME CLOCK OUTPUT SUPPORTS THREE MODES OF OPERATION:
1) ENABLED (ALWAYS ON)
2) DISABLED (ALWAYS OFF)
3) GAPPED PERIODIC (CONDITIONALLY ENABLED BASED ON PSEUDO-RANDOM BIT)
4 STATUS BIT SELECTED BY OUTPUT MODE CONTROL 1 BITS, REGISTER 0x559[2:0] IN THE REGISTER MAP.

13059-009

Figure 10. LVDS Byte Mode—Four Virtual Converters, Two DDCs (I/Q Decimate by 8)

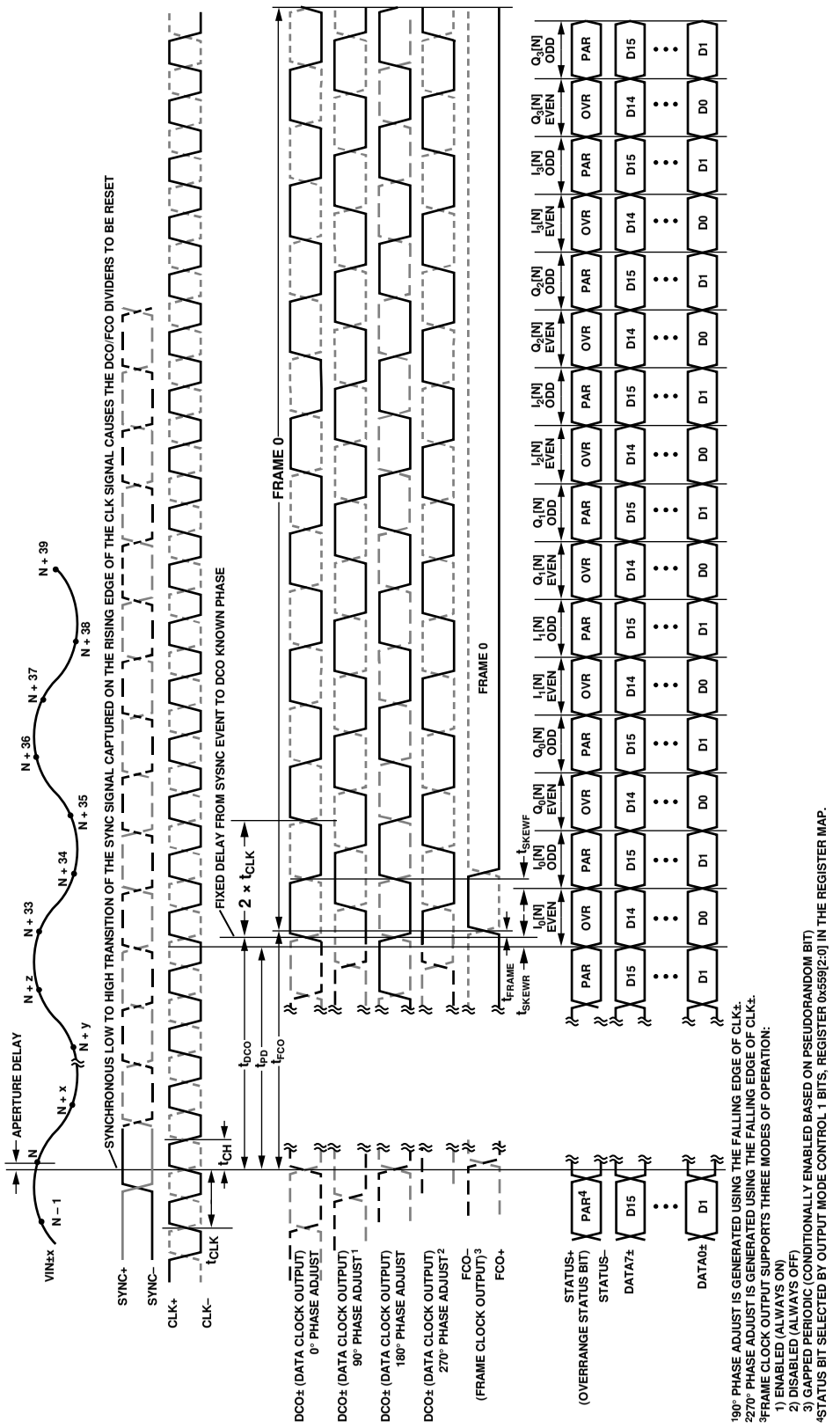


Figure 11. LVDS Byte Mode—Eight Virtual Converters, Four DDCs (I/Q Decimate by 16)

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.32 V
AVDD2 to AGND	2.75 V
AVDD3 to AGND	3.63 V
DVDD to DGND	1.32 V
DRVDD to DRGND	1.32 V
SPIVDD to AGND	3.63 V
AGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	3.2 V
SCLK, SDIO, CSB to AGND	−0.3 V to SPIVDD + 0.3 V
PDWN/STBY to AGND	−0.3 V to SPIVDD + 0.3 V
Environmental	
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature	+125°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA}, Ψ_{JB}, and Ψ_{JT} are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation, effectively reducing θ_{JA} and Ψ_{JB}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}. Thermal performance for actual applications requires careful inspection of the conditions in an application. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 6.

Table 7. Thermal Resistance

PCB Type	Airflow Velocity (m/sec)	θ_{JA}	Ψ_{JT}	Ψ_{JB}	Unit
JEDEC 2s2p Board	0.0	27.0[1, 2]	0.7[1, 3]	7.3[1, 3]	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per JEDEC JESD51-8 (still air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

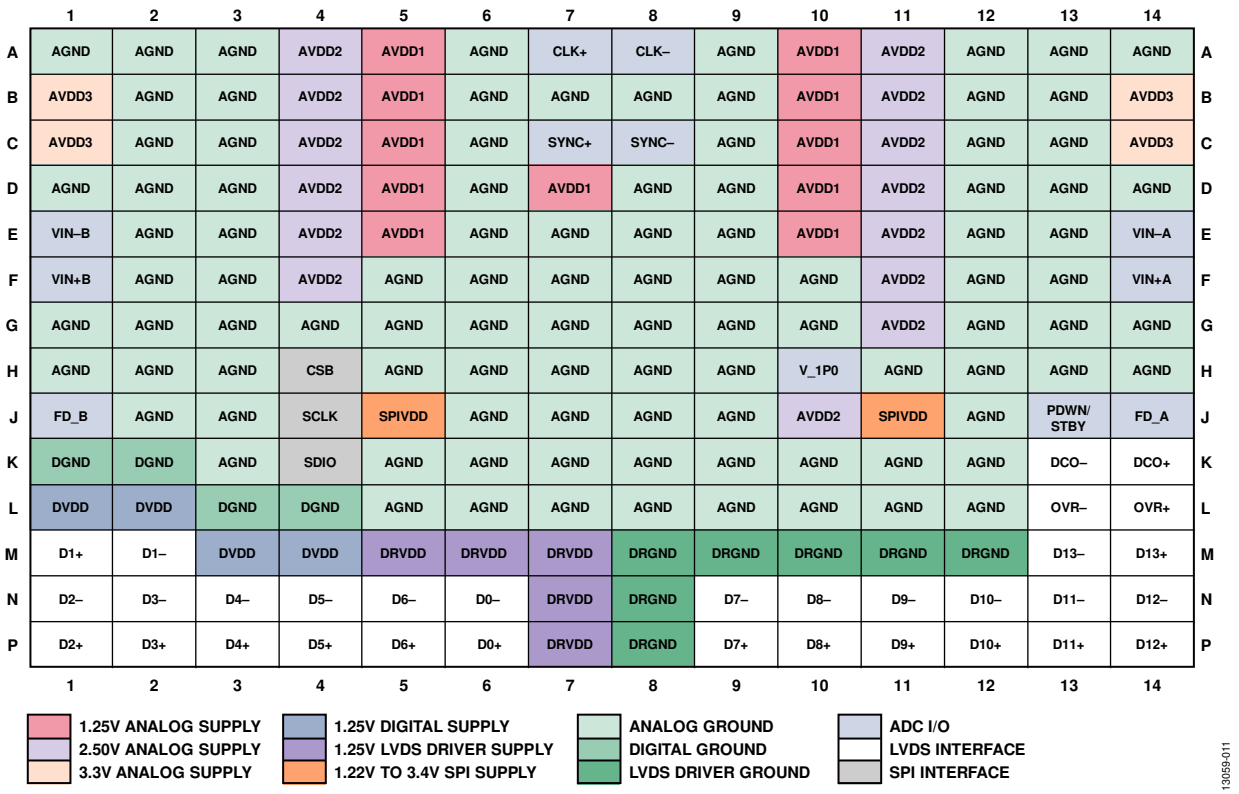


Figure 12. Pin Configuration—Parallel Interleaved LVDS Mode (Top View)

Table 8. Pin Function Descriptions—Parallel Interleaved LVDS Mode

Pin No.	Mnemonic	Type	Description
Power Supplies			
A5, A10, B5, B10, C5, C10, D5, D7, D10, E5, E10	AVDD1	Supply	Analog Power Supply (1.25 V Nominal).
A4, A11, B4, B11, C4, C11, D4, D11, E4, E11, F4, F11, G11, J10	AVDD2	Supply	Analog Power Supply (2.50 V Nominal).
B1, B14, C1, C14	AVDD3	Supply	Analog Power Supply (3.3 V Nominal)
L1, L2, M3, M4	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
M5 to M7, N7, P7	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
J5, J11	SPIVDD	Supply	Digital Power Supply for SPI (1.22 V to 3.4 V).
K1, K2, L3, L4	DGND	Ground	Ground Reference for DVDD.
M8 to M12, N8, P8	DRGND	Ground	Ground Reference for DRVDD.
A1 to A3, A6, A9, A12 to A14, B2, B3, B6 to B9, B12, B13, C2, C3, C6, C9, C12, C13, D1 to D3, D6, D8, D9, D12 to D14, E2, E3, E6 to E9, E12, E13, F2, F3, F5 to F10, F12, F13, G1 to G10, G12 to G14, H1 to H3, H5 to H9, H11 to H14, J2, J3, J6 to J9, J12, K3, K5 to K12, L5 to L12	AGND	Ground	Analog Ground.
Analog			
E14, F14	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
E1, F1	VIN−B, VIN+B	Input	ADC B Analog Input Complement/True.

Pin No.	Mnemonic	Type	Description
H10	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or as an input. Do not connect this pin if using the internal reference. This pin requires a 1.0 V reference voltage input if using an external voltage reference source.
A7, A8	CLK+, CLK−	Input	Clock Input True/Complement.
CMOS Outputs			
J14, J1	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B.
Digital Inputs			
C7, C8	SYNC+, SYNC−	Input	Active High LVDS Sync Input—True/Complement.
Data Outputs			
N6, P6	D0−, D0+	Output	LVDS Lane 0 Output Data—Complement/True.
M2, M1	D1−, D1+	Output	LVDS Lane 1 Output Data—Complement/True.
N1, P1	D2−, D2+	Output	LVDS Lane 2 Output Data—Complement/True.
N2, P2	D3−, D3+	Output	LVDS Lane 3 Output Data—Complement/True.
N3, P3	D4−, D4+	Output	LVDS Lane 4 Output Data—Complement/True.
N4, P4	D5−, D5+	Output	LVDS Lane 5 Output Data—Complement/True.
N5, P5	D6−, D6+	Output	LVDS Lane 6 Output Data—Complement/True.
N9, P9	D7−, D7+	Output	LVDS Lane 7 Output Data—Complement/True.
N10, P10	D8−, D8+	Output	LVDS Lane 8 Output Data—Complement/True.
N11, P11	D9−, D9+	Output	LVDS Lane 9 Output Data—Complement/True.
N12, P12	D10−, D10+	Output	LVDS Lane 10 Output Data—Complement/True.
N13, P13	D11−, D11+	Output	LVDS Lane 11 Output Data—Complement/True.
N14, P14	D12−, D12+	Output	LVDS Lane 12 Output Data—Complement/True.
M13, M14	D13−, D13+	Output	LVDS Lane 13 Output Data—Complement/True.
L13, L14	OVR−, OVR+	Output	LVDS Overrange Output Data—Complement/True.
K13, K14	DCO−, DCO+	Output	LVDS Digital Clock Output Data—Complement/True.
Device Under Test (DUT) Controls			
K4	SDIO	Input/output	SPI Serial Data Input/Output.
J4	SCLK	Input	SPI Serial Clock.
H4	CSB	Input	SPI Chip Select (Active Low).
J13	PDWN/STBY	Input	Power-Down Input (Active High)/Standby. The operation of this pin depends on the SPI mode and can be configured in power-down or standby mode.

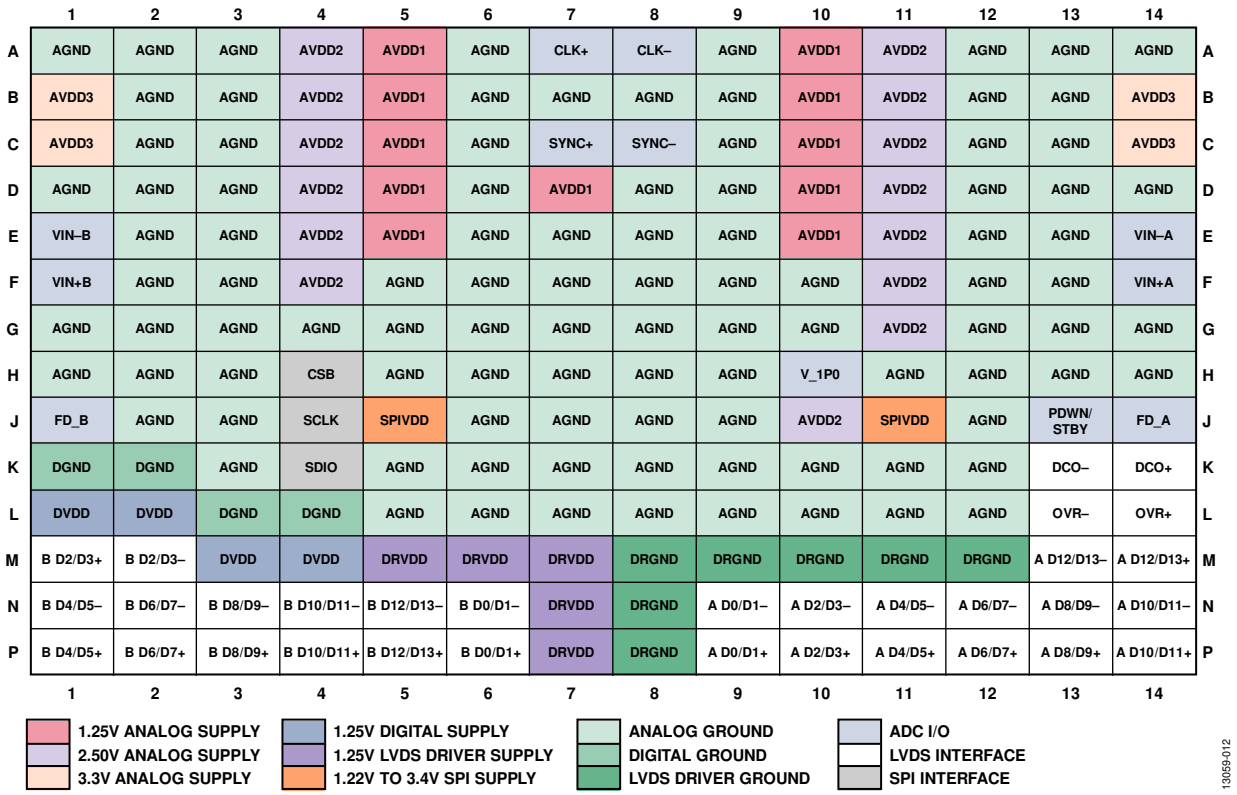


Figure 13. Pin Configuration—Channel Multiplexed (Even/Odd) LVDS Mode (Top View)

Table 9. Pin Function Descriptions—Channel Multiplexed (Even/Odd) LVDS Mode[1]

Pin No.	Mnemonic	Type	Description
Power Supplies			
A5, A10, B5, B10, C5, C10, D5, D7, D10, E5, E10	AVDD1	Supply	Analog Power Supply (1.25 V Nominal).
A4, A11, B4, B11, C4, C11, D4, D11, E4, E11, F4, F11, G11, J10	AVDD2	Supply	Analog Power Supply (2.50 V Nominal).
B1, B14, C1, C14	AVDD3	Supply	Analog Power Supply (3.3 V Nominal)
L1, L2, M3, M4	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
M5 to M7, N7, P7	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
J5, J11	SPIVDD	Supply	Digital Power Supply for SPI (1.22 V to 3.4 V).
K1, K2, L3, L4	DGND	Ground	Ground Reference for DVDD.
M8 to M12, N8, P8	DRGND	Ground	Ground Reference for DRVDD.
A1 to A3, A6, A9, A12 to A14, B2, B3, B6 to B9, B12, B13, C2, C3, C6, C9, C12, C13, D1 to D3, D6, D8, D9, D12 to D14, E2, E3, E6 to E9, E12, E13, F2, F3, F5 to F10, F12, F13, G1 to G10, G12 to G14, H1 to H3, H5 to H9, H11 to H14, J2, J3, J6 to J9, J12, K3, K5 to K12, L5 to L12	AGND	Ground	Analog Ground.
Analog			
E14, F14	VIN–A, VIN+A	Input	ADC A Analog Input Complement/True.
E1, F1	VIN–B, VIN+B	Input	ADC B Analog Input Complement/True.
H10	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or as an input. Do not connect this pin if using the internal reference. This pin requires a 1.0 V reference voltage input if using an external voltage reference source.
A7, A8	CLK+, CLK–	Input	Clock Input True/Complement.

Pin No.	Mnemonic	Type	Description
CMOS Outputs			
J14, J1	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B.
Digital Inputs			
C7, C8	SYNC+, SYNC−	Input	Active High LVDS Sync Input—True/Complement.
Data Outputs			
N9, P9	A D0/D1−, A D0/D1+	Output	LVDS Channel A Data 0/Data 1 Output Data—Complement/True.
N10, P10	A D2/D3−, A D2/D3+	Output	LVDS Channel A Data 2/Data 3 Output Data—Complement/True.
N11, P11	A D4/D5−, A D4/D5+	Output	LVDS Channel A Data 4/Data 5 Output Data—Complement/True.
N12, P12	A D6/D7−, A D6/D7+	Output	LVDS Channel A Data 6/Data 7 Output Data—Complement/True.
N13, P13	A D8/D9−, A D8/D9+	Output	LVDS Channel A Data 8/Data 9 Output Data—Complement/True.
N14, P14	A D10/D11−, A D10/D11+	Output	LVDS Channel A Data 10/Data 11 Output Data—Complement/True.
M13, M14	A D12/D13−, A D12/D13+	Output	LVDS Channel A Data 12/Data 13 Output Data—Complement/True.
N6, P6	B D0/D1−, B D0/D1+	Output	LVDS Channel B Data 0/Data 1 Output Data—Complement/True.
M2, M1	B D2/D3−, B D2/D3+	Output	LVDS Channel B Data 2/Data 3 Output Data—Complement/True.
N1, P1	B D4/D5−, B D4/D5+	Output	LVDS Channel B Data 4/Data 5 Output Data—Complement/True.
N2, P2	B D6/D7−, B D6/D7+	Output	LVDS Channel B Data 6/Data 7 Output Data—Complement/True.
N3, P3	B D8/D9−, B D8/D9+	Output	LVDS Channel B Data 8/Data 9 Output Data—Complement/True.
N4, P4	B D10/D11−, B D10/D11+	Output	LVDS Channel B Data 10/Data 11 Output Data—Complement/True.
N5, P5	B D12/D13−, B D12/D13+	Output	LVDS Channel B Data 12/Data 13 Output Data—Complement/True.
L13, L14	OVR−, OVR+	Output	LVDS Overrange Output Data—Complement/True.
K13, K14	DCO−, DCO+	Output	LVDS Digital Clock Output Data—Complement/True.
DUT Controls			
K4	SDIO	Input/output	SPI Serial Data Input/Output.
J4	SCLK	Input	SPI Serial Clock.
H4	CSB	Input	SPI Chip Select (Active Low).
J13	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured in power-down or standby mode.

[1] When using channel multiplexed (even/odd) LVDS mode for one converter, the Channel B outputs are disabled and can be left unconnected.

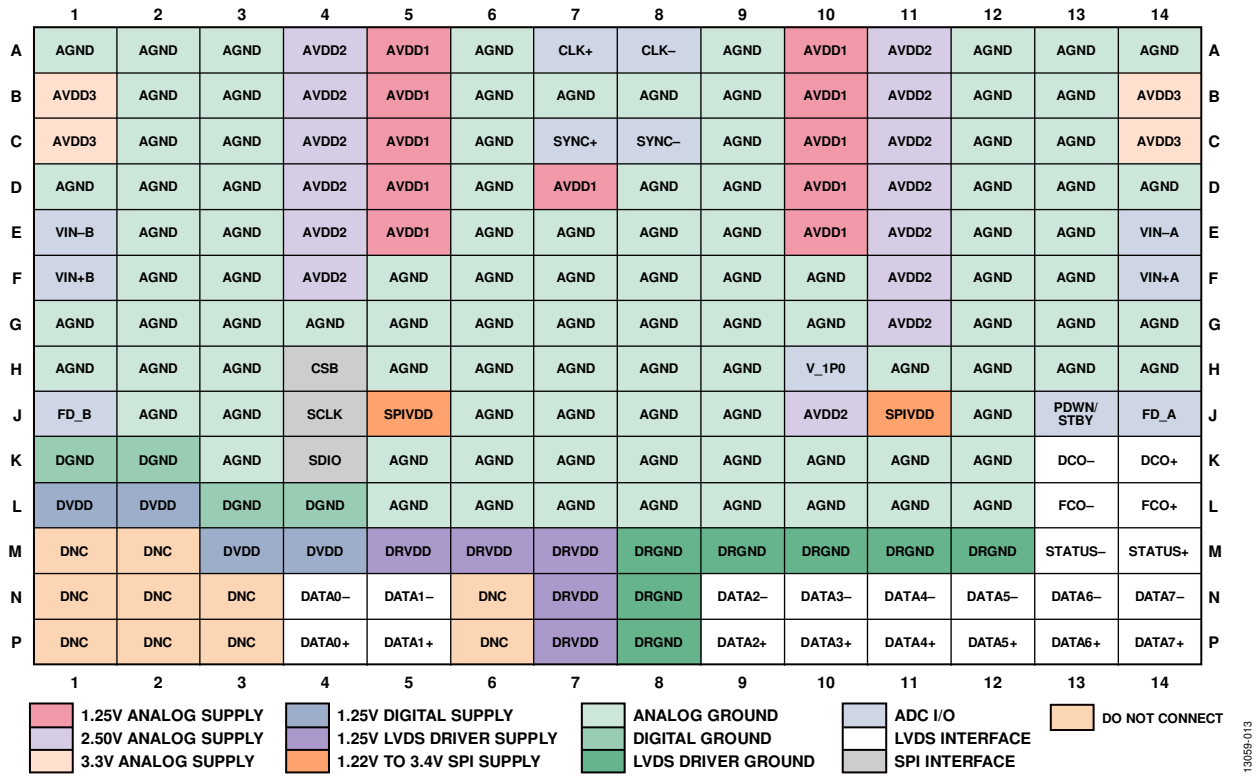


Figure 14. Pin Configuration—LVDS Byte Mode (Top View)

Table 10. Pin Function Descriptions—LVDS Byte Mode

Pin No.	Mnemonic	Type	Description
Power Supplies			
A5, A10, B5, B10, C5, C10, D5, D7, D10, E5, E10	AVDD1	Supply	Analog Power Supply (1.25 V Nominal).
A4, A11, B4, B11, C4, C11, D4, D11, E4, E11, F4, F11, G11, J10	AVDD2	Supply	Analog Power Supply (2.50 V Nominal).
B1, B14, C1, C14	AVDD3	Supply	Analog Power Supply (3.3 V Nominal)
L1, L2, M3, M4	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
M5 to M7, N7, P7	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
J5, J11	SPIVDD	Supply	Digital Power Supply for SPI (1.22 V to 3.4 V).
K1, K2, L3, L4	DGND	Ground	Ground Reference for DVDD.
M8 to M12, N8, P8	DRGND	Ground	Ground Reference for DRVDD.
A1 to A3, A6, A9, A12 to A14, B2, B3, B6 to B9, B12, B13, C2, C3, C6, C9, C12, C13, D1 to D3, D6, D8, D9, D12 to D14, E2, E3, E6 to E9, E12, E13, F2, F3, F5 to F10, F12, F13, G1 to G10, G12 to G14, H1 to H3, H5 to H9, H11 to H14, J2, J3, J6 to J9, J12, K3, K5 to K12, L5 to L12	AGND	Ground	Analog Ground.
Analog			
E14, F14	VIN–A, VIN+A	Input	ADC A Analog Input Complement/True.
E1, F1	VIN–B, VIN+B	Input	ADC B Analog Input Complement/True.
H10	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or an input. Do not connect this pin if using the internal reference. This pin requires a 1.0 V reference voltage input if using an external voltage reference source.
A7, A8	CLK+, CLK–	Input	Clock Input True/Complement.

Pin No.	Mnemonic	Type	Description
CMOS Outputs			
J14, J1	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B.
Digital Inputs			
C7, C8	SYNC+, SYNC−	Input	Active High LVDS Sync Input—True/Complement.
Data Outputs			
N4, P4	DATA0−, DATA0+	Output	LVDS Byte Data 0—Complement/True.
N5, P5	DATA1−, DATA1+	Output	LVDS Byte Data 1—Complement/True.
N9, P9	DATA2−, DATA2+	Output	LVDS Byte Data 2—Complement/True.
N10, P10	DATA3−, DATA3+	Output	LVDS Byte Data 3—Complement/True.
N11, P11	DATA4−, DATA4+	Output	LVDS Byte Data 4—Complement/True.
N12, P12	DATA5−, DATA5+	Output	LVDS Byte Data 5—Complement/True.
N13, P13	DATA6−, DATA6+	Output	LVDS Byte Data 6—Complement/True.
N14, P14	DATA7−, DATA7+	Output	LVDS Byte Data 7—Complement/True.
M13, M14	STATUS−, STATUS+	Output	LVDS Status Output Data—Complement/True.
L13, L14	FCO−, FCO+	Output	LVDS Frame Clock Output Data—Complement/True.
K13, K14	DCO−, DCO+	Output	LVDS Digital Clock Output Data—Complement/True.
DUT Controls			
K4	SDIO	Input/output	SPI Serial Data Input/Output.
J4	SCLK	Input	SPI Serial Clock.
H4	CSB	Input	SPI Chip Select (Active Low).
J13	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured in power-down or standby mode.
No Connects			
M1, M2, N1 to N3, N6, P1 to P3, P6	DNC	DNC	Do Not Connect. Do not connect to these pins.