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135 MHz Quad IF Receiver

Data Sheet

AD6684

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
  - Lane rates up to 15 Gbps
- 1.68 W total power at 500 MSPS
  - 420 mW per analog-to-digital converter (ADC) channel
- SFDR = 82 dBFS at 305 MHz (1.8 V p-p input range)
- SNR = 66.8 dBFS at 305 MHz (1.8 V p-p input range)
- Noise density = −151.5 dBFS/Hz (1.8 V p-p input range)
- Analog input buffer
- On-chip dithering to improve small signal linearity
- Flexible differential input range
  - 1.44 V p-p to 2.16 V p-p (1.80 V p-p nominal)
- 82 dB channel isolation/crosstalk
- 0.975 V, 1.8 V, and 2.5 V dc supply operation
- Noise shaping requantizer (NSR) option for main receiver
- Variable dynamic range (VDR) option for digital predistortion (DPD)
- 4 integrated wideband digital downconverters (DDCs)
  - 48-bit numerically controlled oscillator (NCO), up to 4 cascaded half-band filters
- 1.4 GHz analog input full power bandwidth
- Amplitude detect bits for efficient automatic gain control (AGC) implementation
- Differential clock input
- Integer clock divide by 1, 2, 4, or 8
- On-chip temperature diode
- Flexible JESD204B lane configurations

APPLICATIONS

- Communications
- Diversity multiband, multimode digital receivers
  - 3G/4G, W-CDMA, GSM, LTE, LTE-A
- HFC digital reverse path receivers
- Digital predistortion observation paths
- General-purpose software radios

FUNCTIONAL BLOCK DIAGRAM

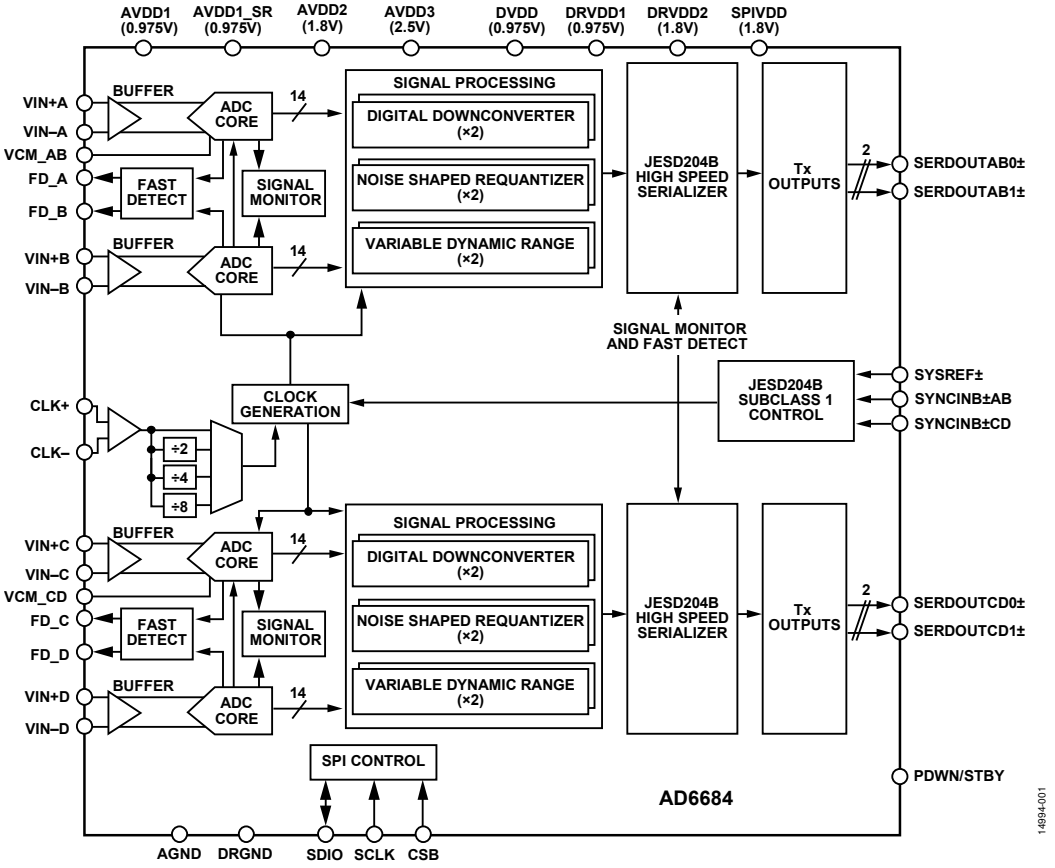

Figure 1.

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- AD6684 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1432: Practical Thermal Modeling and Measurements in High Power ICs

Data Sheet

- AD6684: 135 MHz Quad IF Receiver Data Sheet

User Guides

- Evaluating the AD6684 IF Diversity Receiver

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- AD6684 Material Declaration
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REVISION HISTORY

10/2016—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD6684 is a 135 MHz bandwidth, quad intermediate frequency (IF) receiver. It consists of four 14-bit, 500 MSPS ADCs and various digital processing blocks consisting of four wideband DDCs, an NSR, and VDR monitoring. The device has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This device is designed to support communications applications. The analog full power bandwidth of the device is 1.4 GHz.

The quad ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. The AD6684 is optimized for wide input bandwidth, excellent linearity, and low power in a small package.

The analog inputs and clock signal input are differential. Each pair of ADC data outputs are internally connected to two DDCs through a crossbar mux. Each DDC consists of up to five cascaded signal processing stages: a 48-bit frequency translator, NCO, and up to four half-band decimation filters.

Each ADC output is connected internally to an NSR block. The integrated NSR circuitry allows improved SNR performance in a smaller frequency band within the Nyquist bandwidth. The device supports two different output modes selectable via the serial port interface (SPI). With the NSR feature enabled, the outputs of the ADCs are processed such that the AD6684 supports enhanced SNR performance within a limited portion of the Nyquist bandwidth while maintaining a 9-bit output resolution.

Each ADC output is also connected internally to a VDR block. This optional mode allows full dynamic range for defined input signals. Inputs that are within a defined mask (based on DPD applications) are passed unaltered. Inputs that violate this defined mask result in the reduction of the output resolution.

With VDR, the dynamic range of the observation receiver is determined by a defined input frequency mask. For signals falling within the mask, the outputs are presented at the maximum resolution allowed. For signals exceeding defined power levels within this frequency mask, the output resolution is truncated. This mask is based on DPD applications and supports tunable real IF sampling, and zero IF or complex IF receive architectures.

Operation of the AD6684 in the DDC, NSR, and VDR modes is selectable via SPI-programmable profiles (the default mode is NSR at startup).

In addition to the DDC blocks, the AD6684 has several functions that simplify the AGC function in the communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

Users can configure each pair of IF receiver outputs onto either one or two lanes of Subclass 1 JESD204B-based high speed serialized outputs, depending on the decimation ratio and the acceptable lane rate of the receiving logic device. Multiple device synchronization is supported through the SYSREF±, SYNCINB±AB, and SYNCINB±CD input pins.

The AD6684 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using the 1.8 V capable, 3-wire SPI.

The AD6684 is available in a Pb-free, 72-lead LFCSP and is specified over the −40°C to +105°C junction temperature range.

This product may be protected by one or more U.S. or international patents

PRODUCT HIGHLIGHTS

1. Low power consumption per channel.
2. JESD204B lane rate support up to 15 Gbps.
3. Wide full power bandwidth supports IF sampling of signals up to 1.4 GHz.
4. Buffered inputs ease filter design and implementation.
5. Four integrated wideband decimation filters and NCO blocks supporting multiband receivers.
6. Programmable fast overrange detection.
7. On-chip temperature diode for system thermal management.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, specified maximum sampling rate, clock divider = 4, 1.8 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 50°C (T_A = 25°C).

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
ACCURACY				
No Missing Codes		Guaranteed		
Offset Error		0		% FSR
Offset Matching		0		% FSR
Gain Error	−5.0		+5.0	% FSR
Gain Matching		1.0		% FSR
Differential Nonlinearity (DNL)	−0.7	±0.4	+0.7	LSB
Integral Nonlinearity (INL)	−5.1	±1.0	+5.1	LSB
TEMPERATURE DRIFT				
Offset Error		8		ppm/°C
Gain Error		214		ppm/°C
INTERNAL VOLTAGE REFERENCE				
Voltage		0.5		V
INPUT REFERRED NOISE		2.6		LSB rms
ANALOG INPUTS				
Differential Input Voltage Range (Programmable)	1.44	1.80	2.16	V p-p
Common-Mode Voltage (V_{CM})		1.34		V
Differential Input Capacitance		1.75		pF
Differential Input Resistance		200		Ω
Analog Input Full Power Bandwidth		1.4		GHz
POWER SUPPLY[1]				
AVDD1	0.95	0.975	1.00	V
AVDD1_SR	0.95	0.975	1.00	V
AVDD2	1.71	1.8	1.89	V
AVDD3	2.44	2.5	2.56	V
DVDD	0.95	0.975	1.00	V
DRVDD1	0.95	0.975	1.00	V
DRVDD2	1.71	1.8	1.89	V
SPIVDD	1.71	1.8	1.89	V
I_{AVDD1}		319	482	mA
I_{AVDD1_SR}		21	53	mA
I_{AVDD2}		438	473	mA
I_{AVDD3}		87	103	mA
I_{DVDD}[2]		145	198	mA
I_{DRVDD1}		162	207	mA
I_{DRVDD2}		23	29	mA
I_{SPIVDD}		1	1.6	mA
POWER CONSUMPTION				
Total Power Dissipation (Including Output Drivers)[2]		1.68	1.94	W
Power-Down Dissipation		325		mW
Standby[3]		1.20		W

[1] Power is measured at NSR, 28% bandwidth, L, M, and F = 222.
[2] Default mode, no decimation enabled. For each link, L = 2, M = 2, and F = 2.
[3] Standby mode is controlled by the SPI.

AC SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, specified maximum sampling rate, clock divider = 4, 1.8 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, VDR mode (input mask not triggered), unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 50°C (T_A = 25°C).

Table 2.

	Analog Input Full Scale = 1.44 V p-p			Analog Input Full Scale = 1.80 V p-p			Analog Input Full Scale = 2.16 V p-p			
Parameter[1]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
ANALOG INPUT FULL SCALE		1.44			1.80			2.16		V p-p
NOISE DENSITY[2]		−149.7			−151.5			−153.0		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[3]										
VDR Mode										
f_{IN} = 10 MHz		65.4			67.1			68.4		dBFS
f_{IN} = 155 MHz		65.3		64.8	67.0			68.3		dBFS
f_{IN} = 305 MHz		65.2			66.8			68.0		dBFS
f_{IN} = 450 MHz		65.0			66.6			67.8		dBFS
f_{IN} = 765 MHz		64.8			66.5			67.5		dBFS
f_{IN} = 985 MHz		64.5			66.0			66.9		dBFS
21% Bandwidth (BW) Mode (>105 MHz at 500 MSPS)										
f_{IN} = 10 MHz		72.1			73.8			75.1		dBFS
f_{IN} = 155 MHz		71.8			73.5			74.8		dBFS
f_{IN} = 305 MHz		71.9			73.5			74.7		dBFS
f_{IN} = 450 MHz		71.6			73.2			74.4		dBFS
f_{IN} = 765 MHz		71.0			72.7			73.7		dBFS
f_{IN} = 985 MHz		70.6			72.1			73.0		dBFS
28% BW Mode (>135 MHz at 500 MSPS)										
f_{IN} = 10 MHz		69.6			71.3			72.6		dBFS
f_{IN} = 155 MHz		69.1			70.8			72.1		dBFS
f_{IN} = 305 MHz		69.1			70.7			71.9		dBFS
f_{IN} = 450 MHz		69.4			71.0			72.2		dBFS
f_{IN} = 765 MHz		68.5			70.2			71.2		dBFS
f_{IN} = 985 MHz		68.5			70.0			70.9		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)[3]										
f_{IN} = 10 MHz		65.3			67.0			68.2		dBFS
f_{IN} = 155 MHz		65.2		64.5	66.8			67.9		dBFS
f_{IN} = 305 MHz		65.1			66.6			67.6		dBFS
f_{IN} = 450 MHz		65.0			66.4			67.3		dBFS
f_{IN} = 765 MHz		64.7			66.1			66.9		dBFS
f_{IN} = 985 MHz		64.2			65.5			66.2		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)[3]										
f_{IN} = 10 MHz		10.5			10.8			11.0		Bits
f_{IN} = 155 MHz		10.5		10.4	10.8			10.9		Bits
f_{IN} = 305 MHz		10.5			10.7			10.9		Bits
f_{IN} = 450 MHz		10.5			10.7			10.8		Bits
f_{IN} = 765 MHz		10.4			10.6			10.8		Bits
f_{IN} = 985 MHz		10.3			10.6			10.7		Bits

Parameter[1]	Analog Input Full Scale = 1.44 V p-p Min	Typ	Max	Analog Input Full Scale = 1.80 V p-p Min	Typ	Max	Analog Input Full Scale = 2.16 V p-p Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)[3]										
f_{IN} = 10 MHz		89			90			80		dBFS
f_{IN} = 155 MHz		89		75	85			77		dBFS
f_{IN} = 305 MHz		82			82			78		dBFS
f_{IN} = 450 MHz		82			83			77		dBFS
f_{IN} = 765 MHz		77			75			72		dBFS
f_{IN} = 985 MHz		82			79			76		dBFS
SPURIOUS-FREE DYNAMIC RANGE (SFDR) AT −3 dBFS[3]										
f_{IN} = 10 MHz		94			94			86		dBFS
f_{IN} = 155 MHz		94			90			82		dBFS
f_{IN} = 305 MHz		89			90			83		dBFS
f_{IN} = 450 MHz		87			86			84		dBFS
f_{IN} = 765 MHz		82			80			77		dBFS
f_{IN} = 985 MHz		85			82			79		dBFS
WORST HARMONIC, SECOND OR THIRD[3]										
f_{IN} = 10 MHz		−89			−90			−80		dBFS
f_{IN} = 155 MHz		−89			−85	−75		−77		dBFS
f_{IN} = 305 MHz		−82			−82			−78		dBFS
f_{IN} = 450 MHz		−82			−83			−77		dBFS
f_{IN} = 765 MHz		−77			−75			−72		dBFS
f_{IN} = 985 MHz		−82			−79			−76		dBFS
WORST HARMONIC, SECOND OR THIRD AT −3 dBFS[3]										
f_{IN} = 10 MHz		−94			−94			−86		dBFS
f_{IN} = 155 MHz		−94			−90			−82		dBFS
f_{IN} = 305 MHz		−89			−90			−83		dBFS
f_{IN} = 450 MHz		−87			−86			−84		dBFS
f_{IN} = 765 MHz		−82			−80			−77		dBFS
f_{IN} = 985 MHz		−85			−82			−79		dBFS
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC[3]										
f_{IN} = 10 MHz		−96			−98			−99		dBFS
f_{IN} = 155 MHz		−97			−97	−86		−97		dBFS
f_{IN} = 305 MHz		−97			−98			−97		dBFS
f_{IN} = 450 MHz		−95			−96			−96		dBFS
f_{IN} = 765 MHz		−92			−91			−88		dBFS
f_{IN} = 985 MHz		−90			−89			−86		dBFS
TWO TONE INTERMODULATION DISTORTION (IMD), AIN1 AND AIN2 = −7 dBFS										
f_{IN1} = 154 MHz, f_{IN2} = 157 MHz		−93			−90			−84		dBFS
f_{IN1} = 302 MHz, f_{IN2} = 305 MHz		−90			−90			−84		dBFS
CROSSTALK[4]		82			82			82		dB
FULL POWER BANDWIDTH[5]		1.4			1.4			1.4		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Noise density is measured with no analog input signal.
[3] See Table 9 for recommended settings for full-scale voltage and buffer current setting.
[4] Crosstalk is measured at 155 MHz with a −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[5] Measured with circuit shown in Figure 58.

DIGITAL SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, specified maximum sampling rate, clock divider = 4, 1.8 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 50°C (T_A = 25°C).

Table 3.

Parameter	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1600	mV p-p
Input Common-Mode Voltage		0.69		V
Input Resistance (Differential)		32		kΩ
Input Capacitance			0.9	pF
SYSREF INPUTS (SYSREF+, SYSREF−)[1]				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage	0.6	0.69	2.2	V
Input Resistance (Differential)	18	22		kΩ
Input Capacitance (Single-Ended per Pin)		0.7		pF
LOGIC INPUTS (PDWN/STBY)				
Logic Compliance		CMOS		
Logic 1 Voltage	0.65 × SPIVDD			V
Logic 0 Voltage	0		0.35 × SPIVDD	V
Input Resistance		10		MΩ
LOGIC INPUTS (SDIO, SCLK, CSB)				
Logic Compliance		CMOS		
Logic 1 Voltage	0.65 × SPIVDD			V
Logic 0 Voltage	0		0.35 × SPIVDD	V
Input Resistance		56		kΩ
LOGIC OUTPUT (SDIO)				
Logic Compliance		CMOS		
Logic 1 Voltage (I_{OH} = 800 µA)	SPIVDD − 0.45 V			V
Logic 0 Voltage (I_{OL} = 50 µA)	0		0.45	V
SYNCIN INPUT (SYNCINB+AB, SYNCINB−AB, SYNCINB+CD, SYNCINB−CD)				
Logic Compliance		LVDS/LVPECL/CMOS		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage	0.6	0.69	2.2	V
Input Resistance (Differential)	18	22		kΩ
Input Capacitance (Single-Ended per Pin)		0.7		pF
LOGIC OUTPUTS (FD_A, FD_B)				
Logic Compliance		CMOS		
Logic 1 Voltage	0.8 × SPIVDD			V
Logic 0 Voltage	0		0.5	V
Input Resistance		56		kΩ
DIGITAL OUTPUTS (SERDOUTx±, x = AB0, AB1, CD0, and CD1)				
Logic Compliance		CML		
Differential Output Voltage		455.8		mV p-p
Short-Circuit Current ($I_{D\ SHORT}$)		15		mA
Differential Termination Impedance		100		Ω

[1] DC-coupled input only.

SWITCHING SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, specified maximum sampling rate, clock divider = 4, 1.8 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 50°C (T_A = 25°C).

Table 4.

Parameter	Min	Typ	Max	Unit
CLOCK				
Clock Rate at CLK+/CLK− Pins	0.3		2.4	GHz
Maximum Sample Rate[1]	500			MSPS
Minimum Sample Rate[2]	240			MSPS
Clock Pulse Width High	125			ps
Clock Pulse Width Low	125			ps
OUTPUT PARAMETERS				
Unit Interval (UI)[3]	62.5	100		ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)		31.25		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)		31.37		ps
Phase-Locked Loop (PLL) Lock Time		5		ms
Data Rate per Channel (NRZ)[4]	1.5625	10	15	Gbps
LATENCY[5]				
Pipeline Latency		54		Sample clock cycles
Fast Detect Latency			30	Sample clock cycles
APERTURE				
Aperture Delay (t_A)		160		ps
Aperture Uncertainty (Jitter, t_j)		44		fs rms
Out-of-Range Recovery Time		1		Sample clock cycles

[1] The maximum sample rate is the clock rate after the divider.
[2] The minimum sample rate operates at 240 MSPS with L = 2 or L = 1. Refer to SPI Register 0x011A to reduce the threshold of the clock detect circuit.
[3] Baud rate = 1/UI. A subset of this range can be supported.
[4] Default L = 2. This number can be changed based on the sample rate and decimation ratio.
[5] No DDCs used. L = 2, M = 2, F = 2 for each link.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK+ to SYSREF+ TIMING REQUIREMENTS	See Figure 3				
t_{SU_SR}	Device clock to SYSREF+ setup time		−44.8		ps
t_{H_SR}	Device clock to SYSREF+ hold time		64.4		ps
SPI TIMING REQUIREMENTS	See Figure 4				
t_{DS}	Setup time between the data and the rising edge of SCLK	4			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the CSB rising edge (not shown in Figure 4)	10			ns

Timing Diagrams

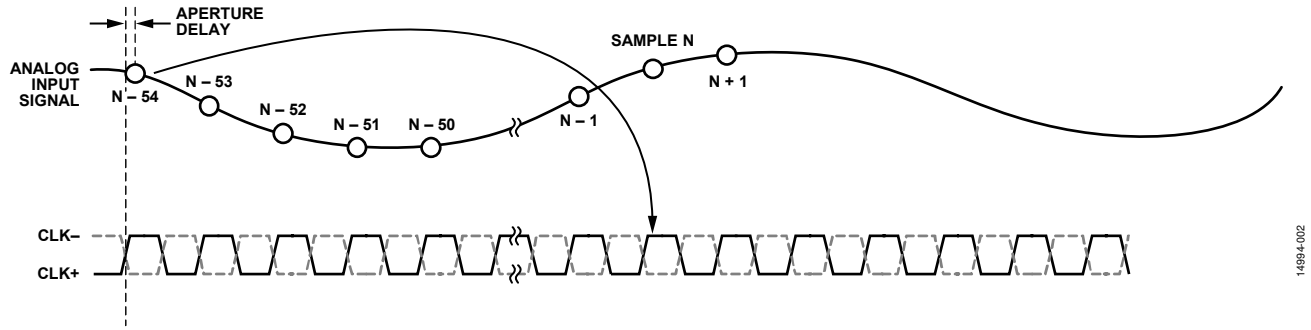


Figure 2. Data Output Timing (NSR Mode, 21%, L, M, F = 222)

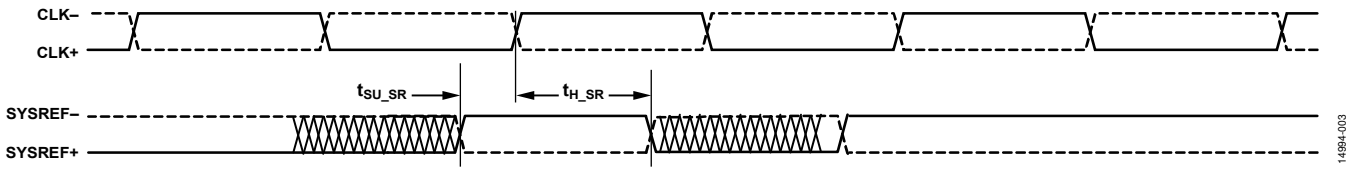


Figure 3. SYSREF± Setup and Hold Timing

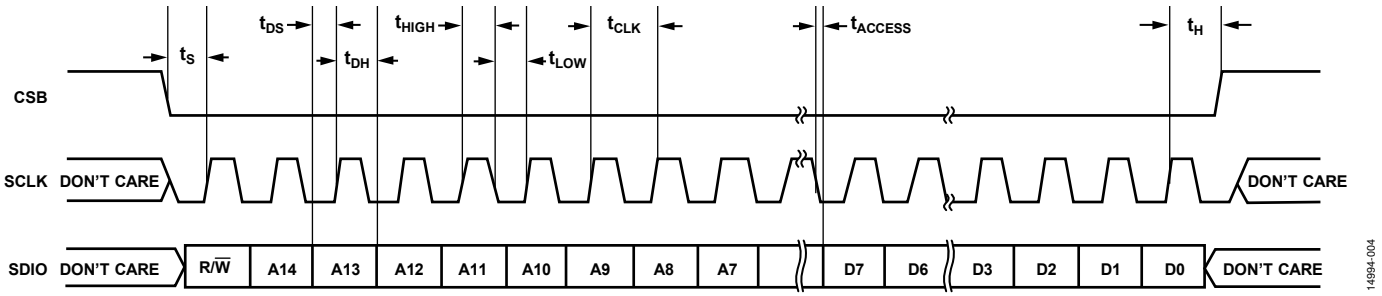


Figure 4. Serial Port Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.05 V
AVDD1_SR to AGND	1.05 V
AVDD2 to AGND	2.00 V
AVDD3 to AGND	2.70 V
DVDD to DGND	1.05 V
DRVDD1 to DRGND	1.05 V
DRVDD2 to DRGND	2.00 V
SPIVDD to AGND	2.00 V
VIN±x to AGND	−0.3 V to AVDD3 + 0.3 V
CLK± to AGND	−0.3 V to AVDD1 + 0.3 V
SCLK, SDIO, CSB to DGND	−0.3 V to SPIVDD + 0.3 V
PDWN/STBY to DGND	−0.3 V to SPIVDD + 0.3 V
SYSREF± to AGND_SR	0 V to 2.5 V
SYNCIN±AB/SYNCIN±CD to DRGND	0 V to 2.5 V
Environmental	
Operating Junction Temperature Range	−40°C to +105°C
Maximum Junction Temperature	125°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 7. Thermal Resistance

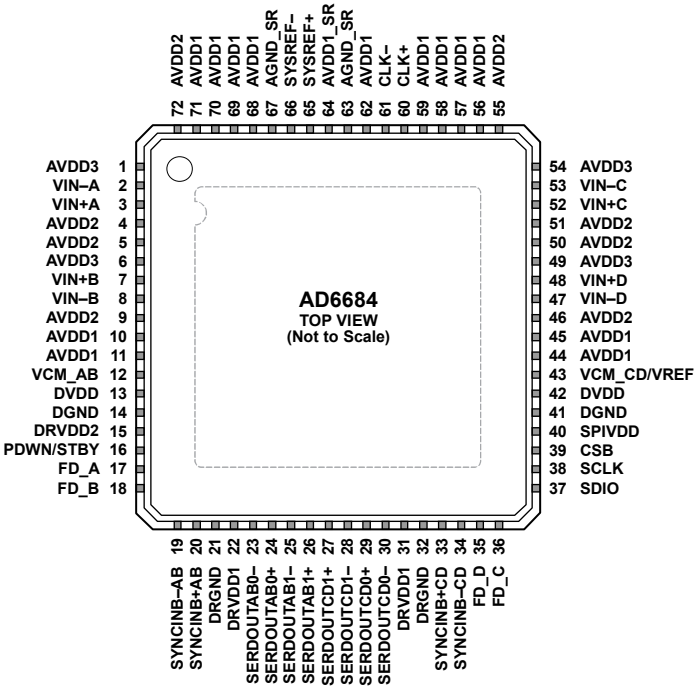
PCB Type	Airflow Velocity (m/sec)	θ_{JA}	θ_{JCB}	Unit
JEDEC 2s2p Board	0.0	21.58[1, 2]	1.95[1, 3]	°C/W
	1.0	17.94[1, 2]	N/A[4]	°C/W
	2.5	16.58[1, 2]	N/A[4]	°C/W
10-Layer Board	0.0	9.74	1.00	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-STD 883, Method 1012.1.
[4] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. ANALOG GROUND. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE GROUND REFERENCE FOR AVDDx, SPIVDD, DVDD, DRVDD1, AND DRVDD2. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

Figure 5. Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
0	AGND/EPAD	Ground	Exposed Pad. Analog Ground. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDx, SPIVDD, DVDD, DRVDD1, and DRVDD2. This exposed pad must be connected to ground for proper operation.
1, 6, 49, 54	AVDD3	Supply	Analog Power Supply (2.5 V Nominal).
2, 3	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
4, 5, 9, 46, 50, 51, 55, 72	AVDD2	Supply	Analog Power Supply (1.8 V Nominal).
7, 8	VIN+B, VIN−B	Input	ADC B Analog Input True/Complement.
10, 11, 44, 45, 56, 57, 58, 59, 62, 68, 69, 70, 71	AVDD1	Supply	Analog Power Supply (0.975 V Nominal).
12	VCM_AB	Output	Common-Mode Level Bias Output for Analog Input Channel A and Channel B
13, 42	DVDD	Supply	Digital Power Supply (0.975 V Nominal).
14, 41	DGND	Ground	Ground Reference for DVDD and SPIVDD.
15	DRVDD2	Supply	Digital Power Supply for JESD204B PLL (1.8 V Nominal).
16	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby. Requires external 10 kΩ pull-down resistor.
17, 18, 36, 35	FD_A, FD_B, FD_C, FD_D	Output	Fast Detect Outputs for Channel A, Channel B, Channel C, and Channel D.
19	SYNCINB−AB	Input	Active Low JESD204B LVDS Sync Input Complement for Channel A and Channel B.
20	SYNCINB+AB	Input	Active Low JESD204B LVDS/CMOS Sync Input True for Channel A and Channel B.
21, 32	DRGND	Ground	Ground Reference for DRVDD1 and DRVDD2.
22, 31	DRVDD1	Supply	Digital Power Supply for SERDOUT Pins (0.975 V Nominal).

Pin No.	Mnemonic	Type	Description
23, 24	SERDOUTAB0−, SERDOUTAB0+	Output	Lane 0 Output Data Complement/True for Channel A and Channel B.
25, 26	SERDOUTAB1−, SERDOUTAB1+	Output	Lane 1 Output Data Complement/True for Channel A and Channel B.
27, 28	SERDOUTCD1+, SERDOUTCD1−	Output	Lane 1 Output Data True/Complement for Channel C and Channel D.
29, 30	SERDOUTCD0+, SERDOUTCD0−	Output	Lane 0 Output Data True/Complement for Channel C and Channel D.
33	SYNCINB+CD	Input	Active Low JESD204B LVDS/CMOS Sync Input True for Channel C and Channel D.
34	SYNCINB−CD	Input	Active Low JESD204B LVDS Sync Input Complement for Channel C and Channel D.
37	SDIO	Input/output	SPI Serial Data Input/Output.
38	SCLK	Input	SPI Serial Clock.
39	CSB	Input	SPI Chip Select (Active Low).
40	SPIVDD	Supply	Digital Power Supply for SPI (1.8 V Nominal).
43	VCM_CD/VREF	Output/input	Common-Mode Level Bias Output for Analog Input Channel C and Channel D/0.5 V Reference Voltage Input. This pin is configurable through the SPI as an output or an input. Use this pin as the common-mode level bias output if using the internal reference. This pin requires a 0.5 V reference voltage input if using an external voltage reference source.
47, 48	VIN−D, VIN+D	Input	ADC D Analog Input Complement/True.
52, 53	VIN+C, VIN−C	Input	ADC C Analog Input True/Complement.
60, 61	CLK+, CLK−	Input	Clock Input True/Complement.
63, 67	AGND_SR	Ground	Ground Reference for SYSREF±.
64	AVDD1_SR	Supply	Analog Power Supply for SYSREF± (0.975 V Nominal).
65, 66	SYSREF+, SYSREF−	Input	Active Low JESD204B LVDS System Reference (SYSREF) Input True/Complement. DC-coupled input only.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, specified maximum sampling rate, clock divider = 4, 1.5 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, default SPI settings, VDR mode (input mask not triggered), unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 50°C (T_A = 25°C).

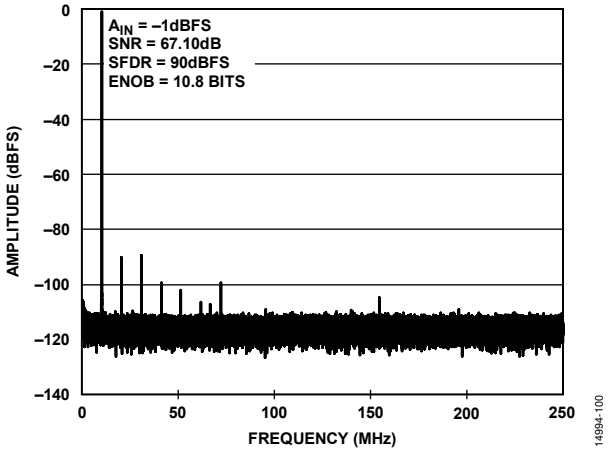


Figure 6. Single-Tone FFT with f_{IN} = 10.3 MHz

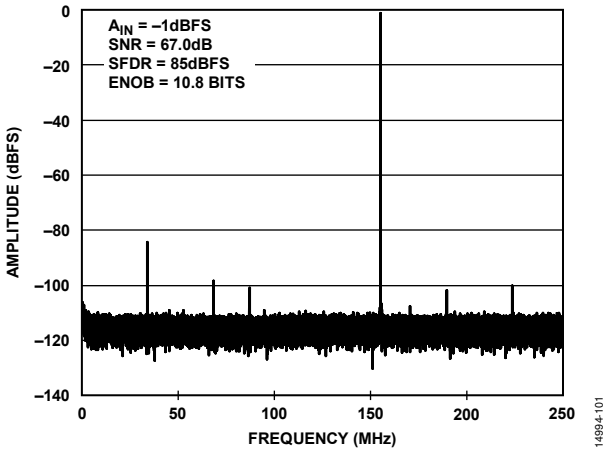


Figure 7. Single-Tone FFT with f_{IN} = 155 MHz

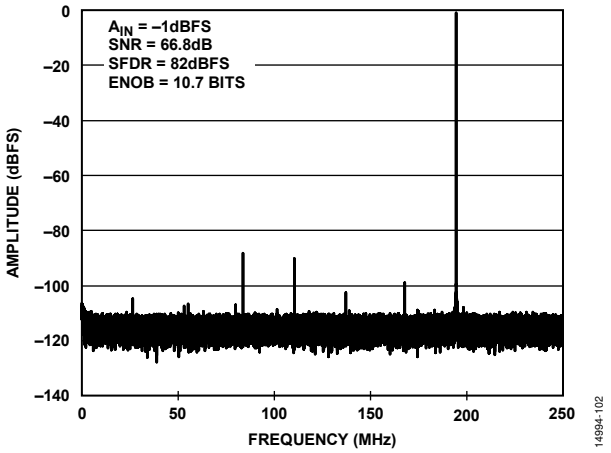


Figure 8. Single-Tone FFT with f_{IN} = 305 MHz

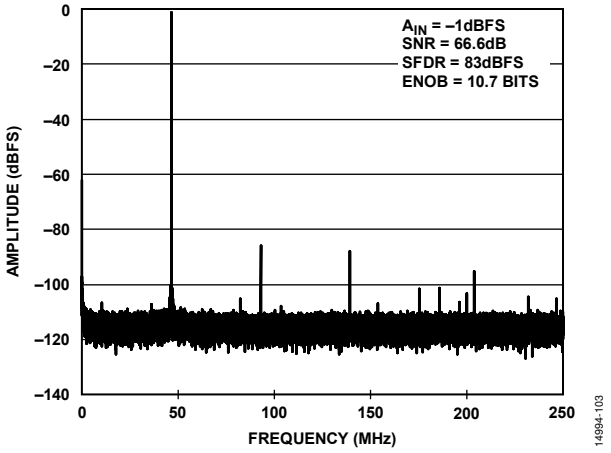


Figure 9. Single-Tone FFT with f_{IN} = 453 MHz

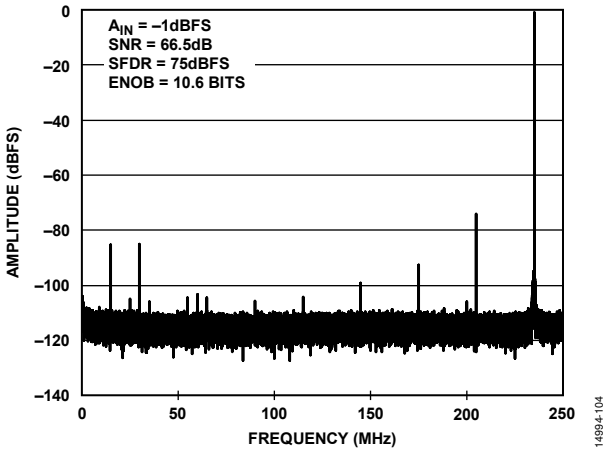


Figure 10. Single-Tone FFT with f_{IN} = 765 MHz

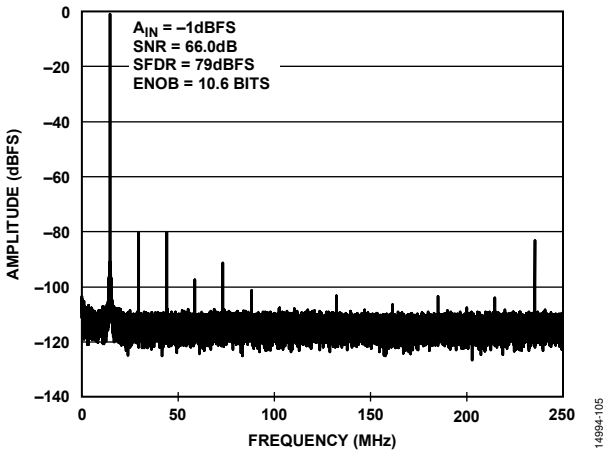


Figure 11. Single-Tone FFT with f_{IN} = 985 MHz

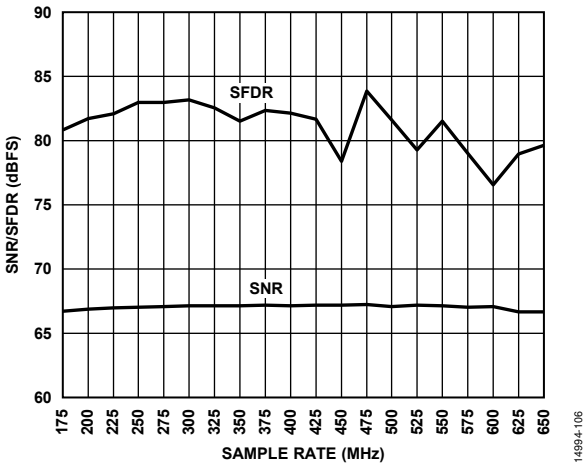


Figure 12. SNR/SFDR vs. Sample Rate (f_S), f_{IN} = 155 MHz

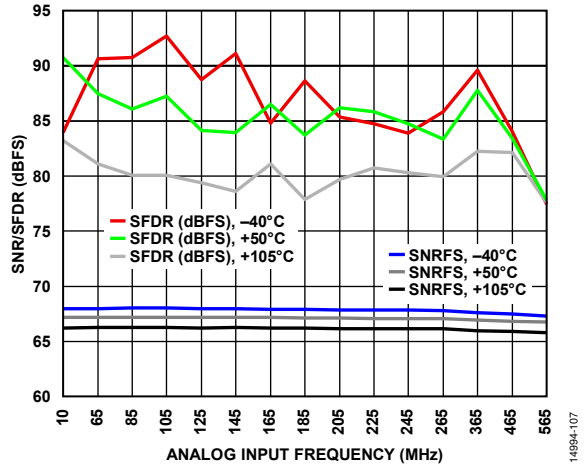


Figure 13. SNR/SFDR vs. Analog Input Frequency (f_{IN})

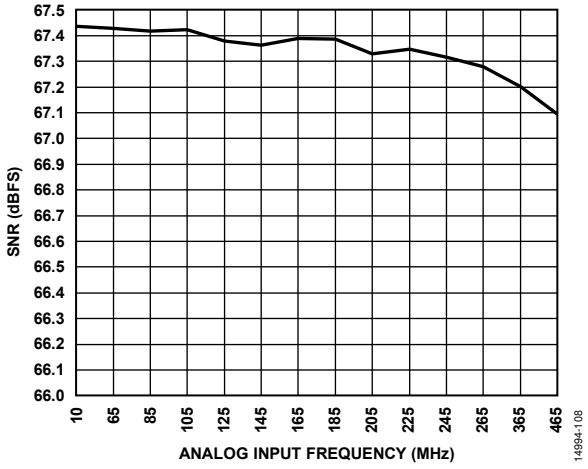


Figure 14. SNR vs. Analog Input Frequency (f_{IN}), First and Second Nyquist Zones; A_{IN} at –3 dBFS

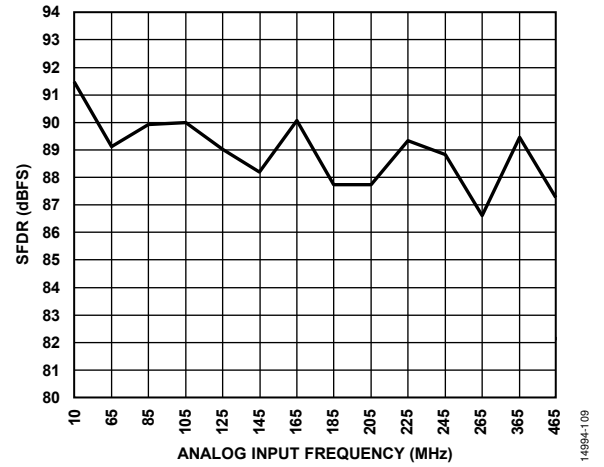


Figure 15. SFDR vs. Analog Input Frequency (f_{IN}), First and Second Nyquist Zones; A_{IN} at –3 dBFS

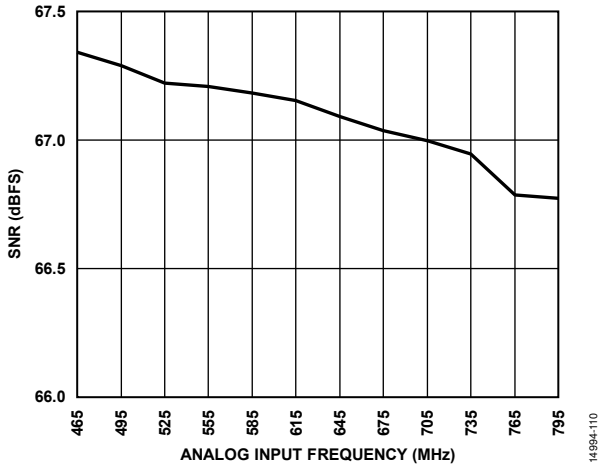


Figure 16. SNR vs. Analog Input Frequency (f_{IN}), Third Nyquist Zone A_{IN} at –3 dBFS

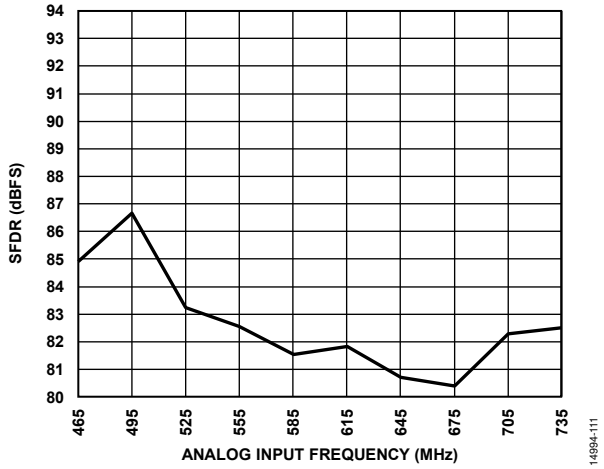


Figure 17. SFDR vs. Analog Input Frequency (f_{IN}), Third Nyquist Zone; A_{IN} at –3 dBFS

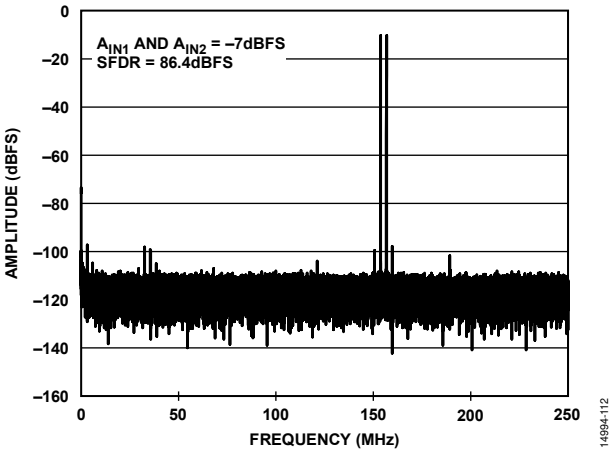


Figure 18. Two Tone FFT; f_{IN1} = 153.5 MHz, f_{IN2} = 156.5 MHz

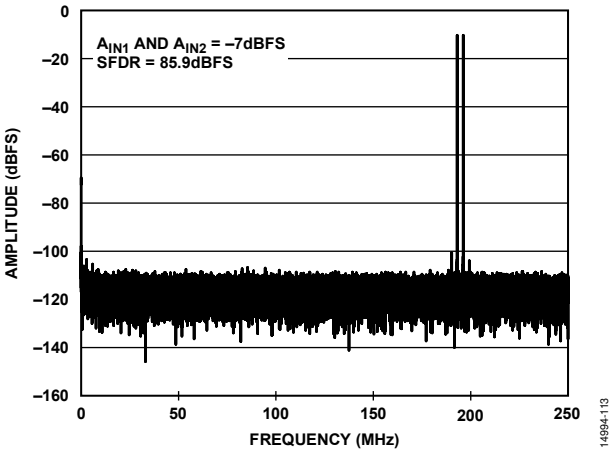


Figure 19. Two Tone FFT; f_{IN1} = 303.5 MHz, f_{IN2} = 306.5 MHz

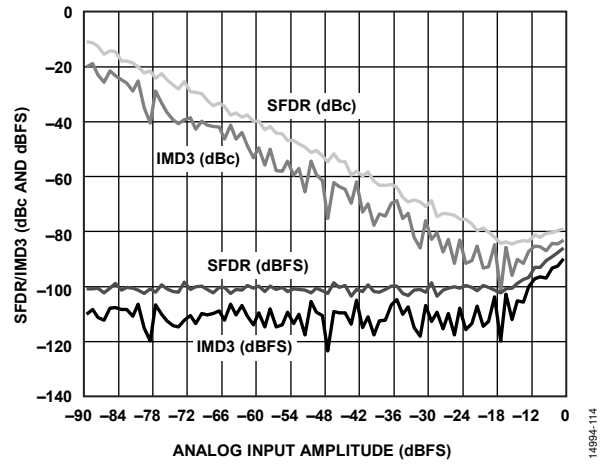


Figure 20. Two Tone SFDR/IMD3 vs. Analog Input Amplitude (A_{IN}) with f_{IN1} = 303.5 MHz and f_{IN2} = 306.5 MHz

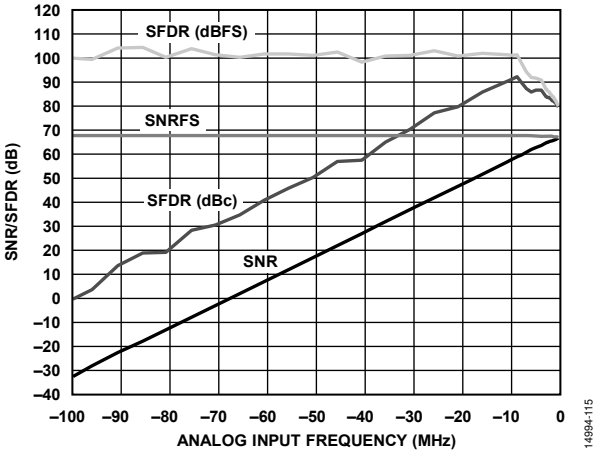


Figure 21. SNR/SFDR vs. Analog Input Frequency, f_{IN} = 155 MHz

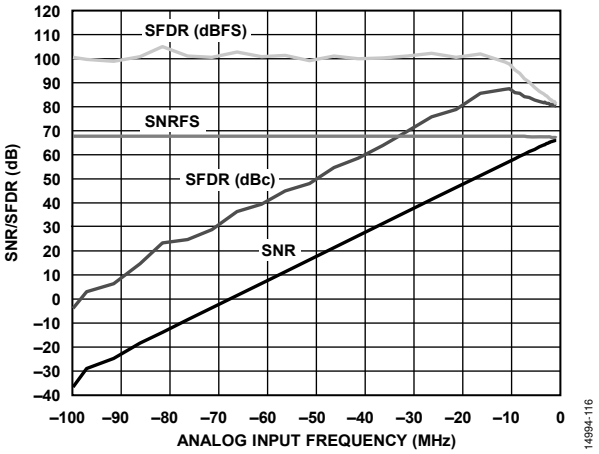


Figure 22. SNR/SFDR vs. Analog Input Frequency, f_{IN} = 305 MHz

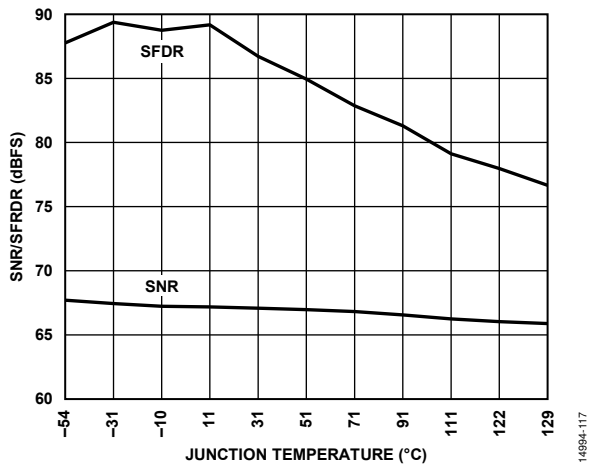


Figure 23. SNR/SFDR vs. Junction Temperature, f_{IN} = 155 MHz

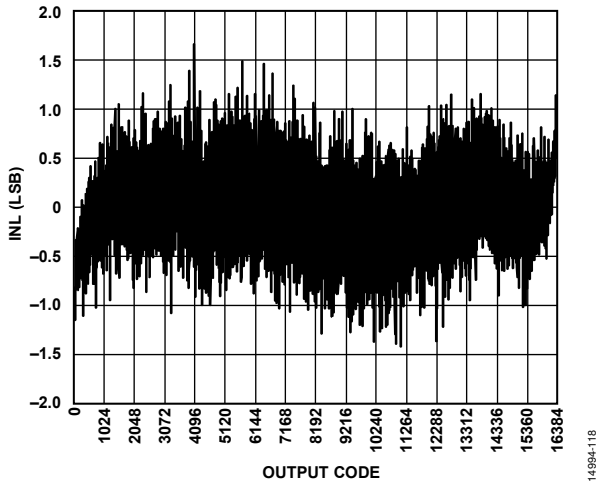


Figure 24. INL, f_{IN} = 10.3 MHz

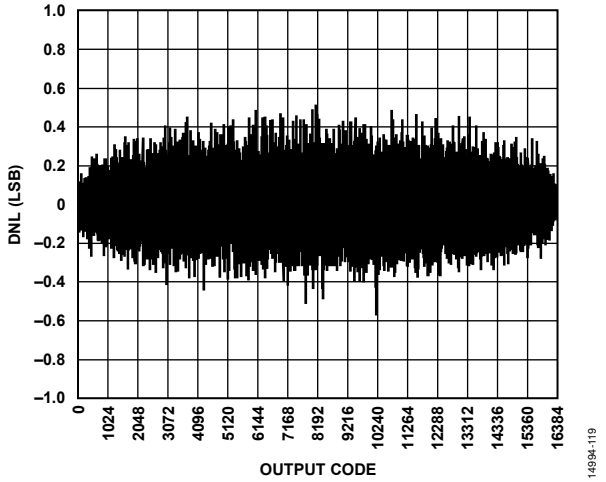


Figure 25. DNL, f_{IN} = 10.3 MHz

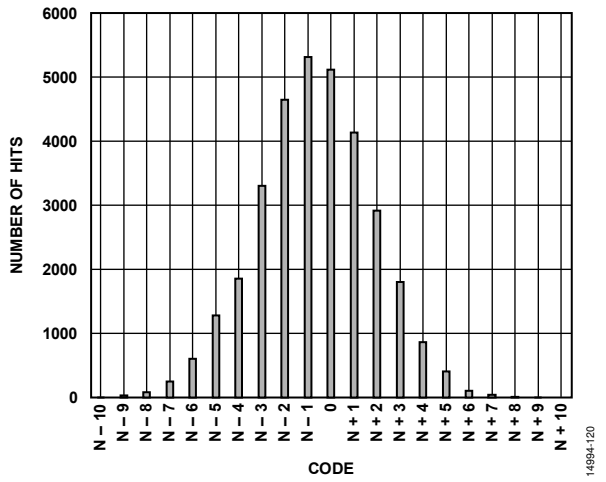


Figure 26. Input-Referred Noise Histogram

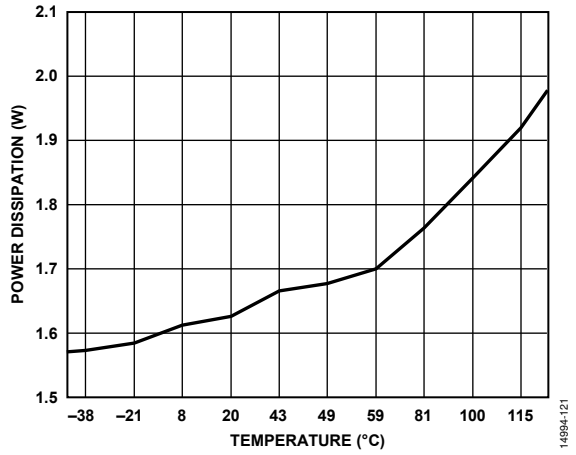


Figure 27. NSR Mode Power Dissipation vs. Junction Temperature

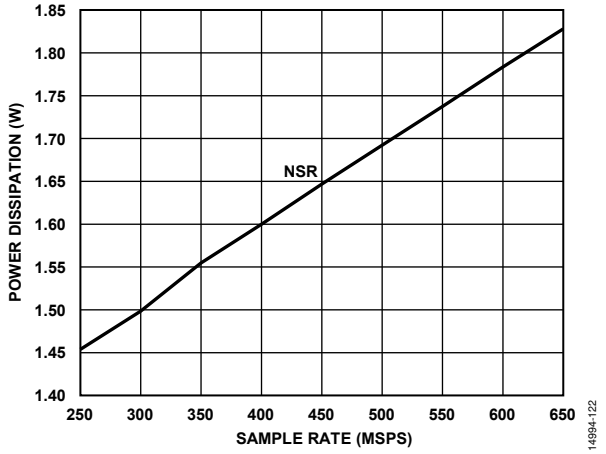


Figure 28. Power Dissipation vs. Sample Rate (f_S)

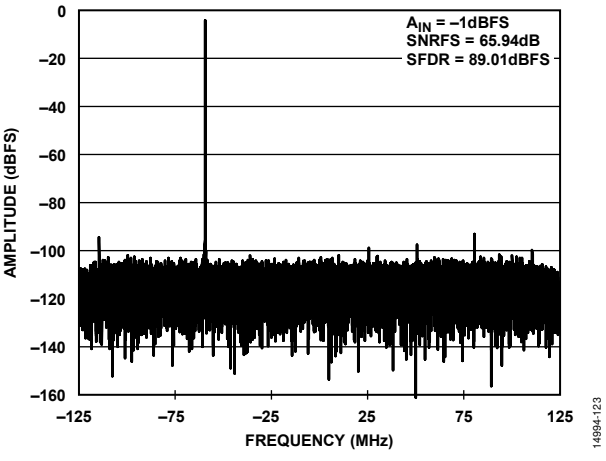


Figure 29. DDC Mode (4 DDCs, DCM2, L, M, and F = 244) with f_{IN} = 305 MHz

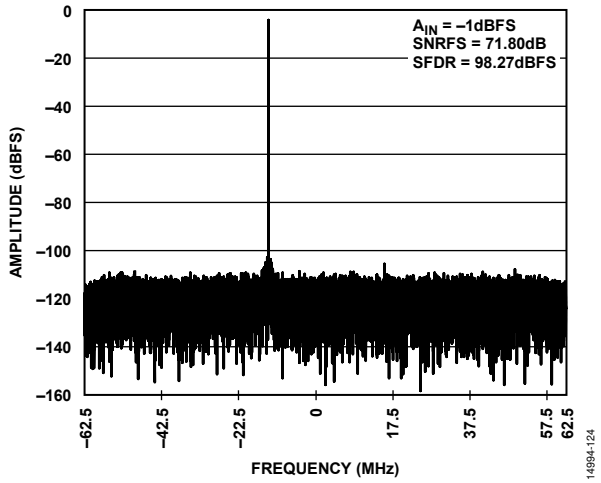


Figure 30. DDC Mode (4 DDCs, Decimate by 4, L, M, and F = 148) with f_{IN} = 305 MHz

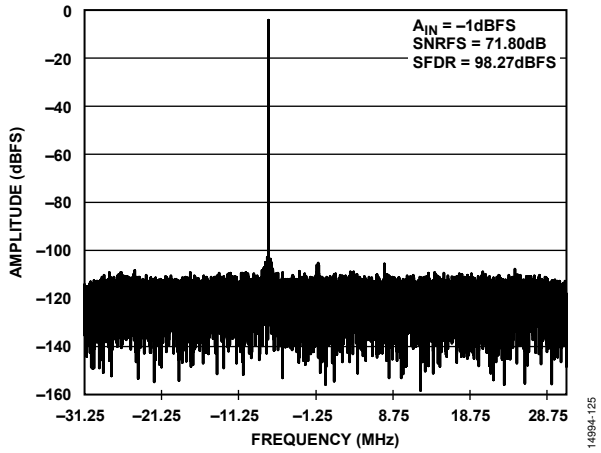


Figure 31. DDC Mode (4 DDCs, Decimate by 8, L, M, and F = 148) with f_{IN} = 305 MHz

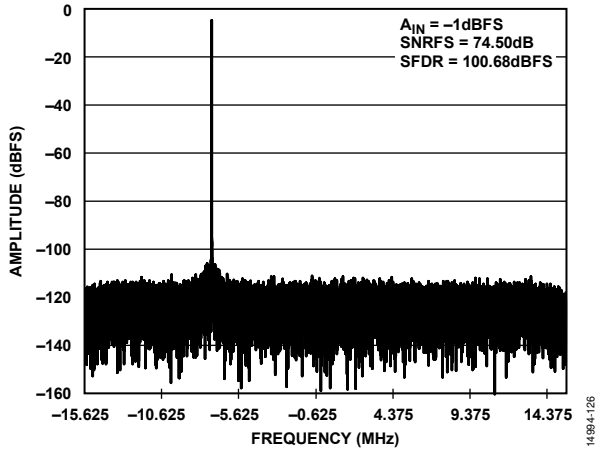


Figure 32. DDC Mode (4 DDCs, Decimate by 16, L, M, and F = 148) with f_{IN} = 305 MHz

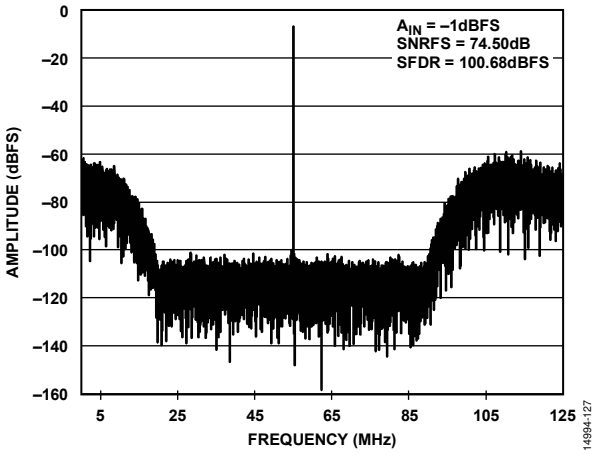


Figure 33. NSR Mode (Decimate by 2, L, M, and F = 124) with f_{IN} = 305 MHz

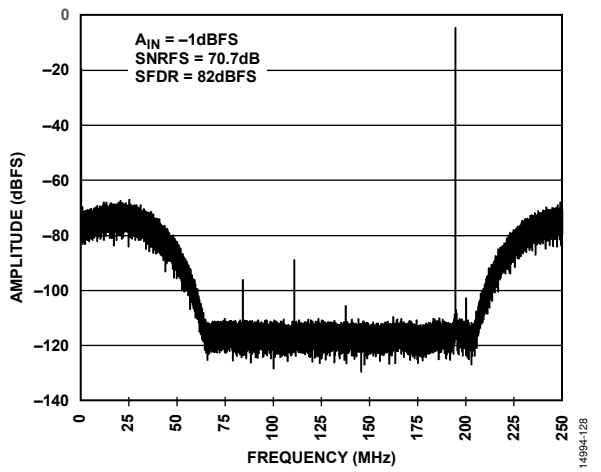


Figure 34. NSR Mode (LMF = 222) with f_{IN} = 305 MHz

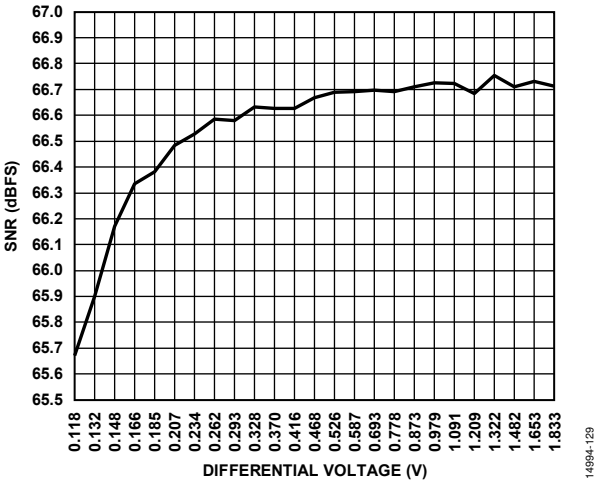


Figure 35. SNR vs. Clock Amplitude (Differential Voltage), f_{IN} = 155.3 MHz

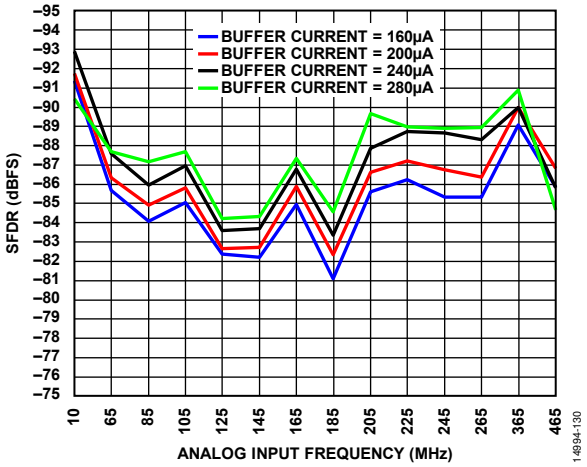


Figure 36. SFDR vs. Analog Input Frequency with Different Buffer Current Settings (First and Second Nyquist Zones)

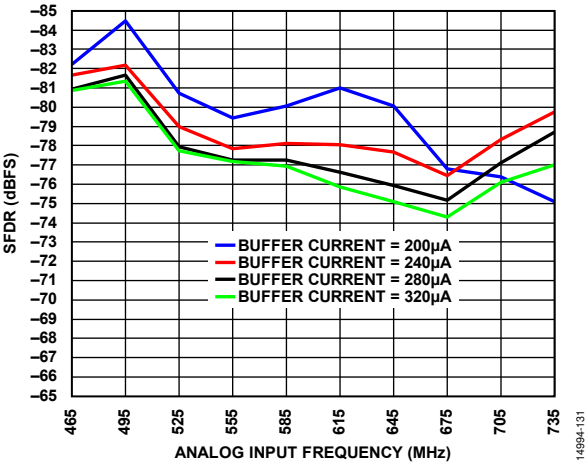


Figure 37. SFDR vs. Analog Input Frequency with Different Buffer Current Settings (Third Nyquist Zone)

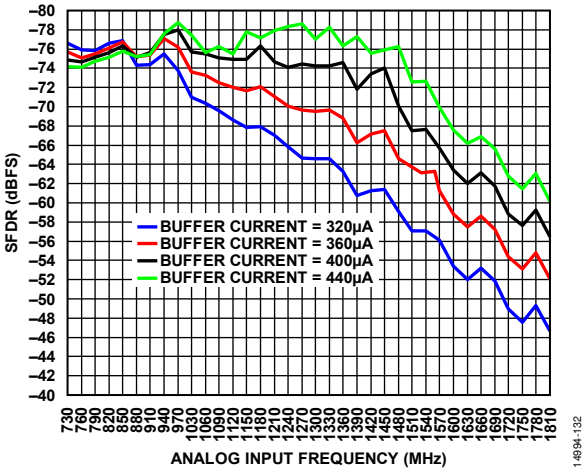


Figure 38. SFDR vs. Analog Input Frequency with Different Buffer Current Settings (Fourth Nyquist Zone)

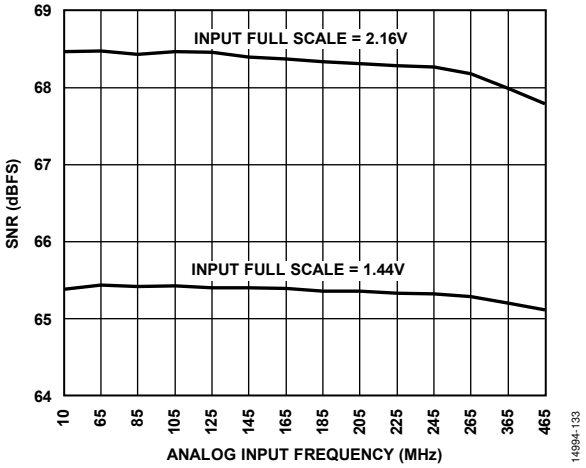


Figure 39. SNR vs. Analog Input Frequency with Different Analog Input Full Scales (First and Second Nyquist Zones)

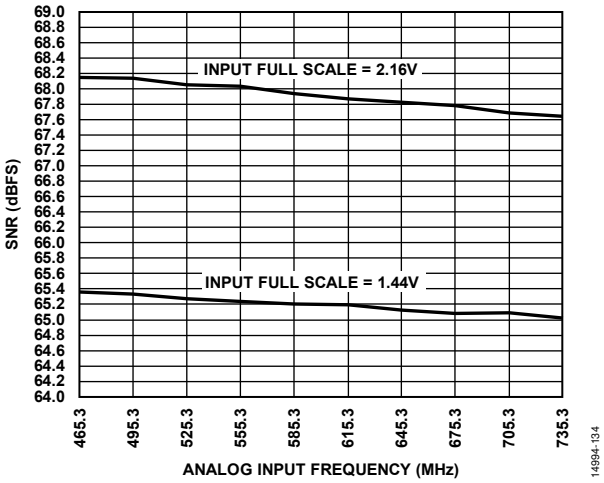


Figure 40. SNR vs. Analog Input Frequency with Different Analog Input Full Scales (Third Nyquist Zone)

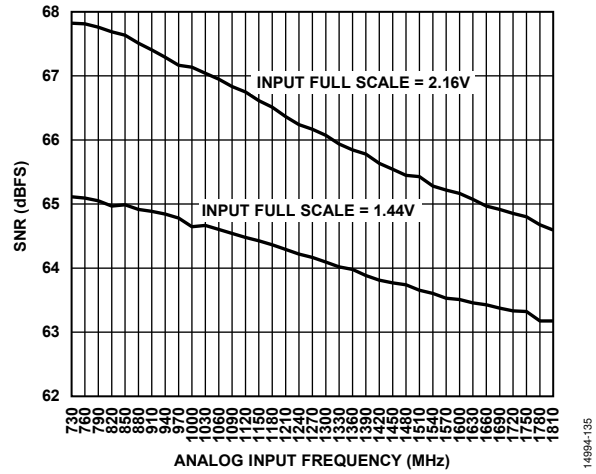


Figure 41. SNR vs. Analog Input Frequency with Different Analog Input Full Scales (Fourth Nyquist Zone)

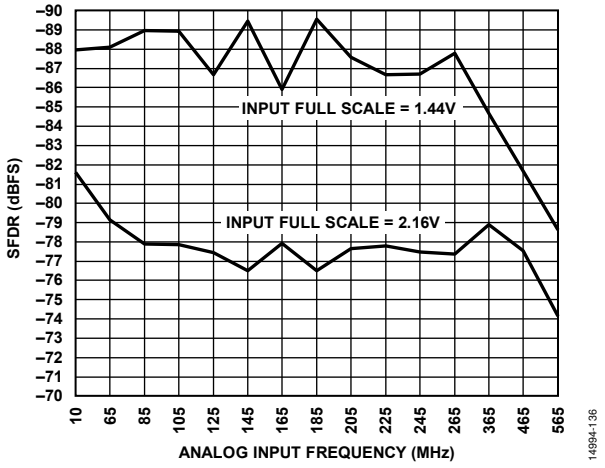


Figure 42. SFDR vs. Analog Input Frequency with Different Analog Input Full Scales (First and Second Nyquist Zones)

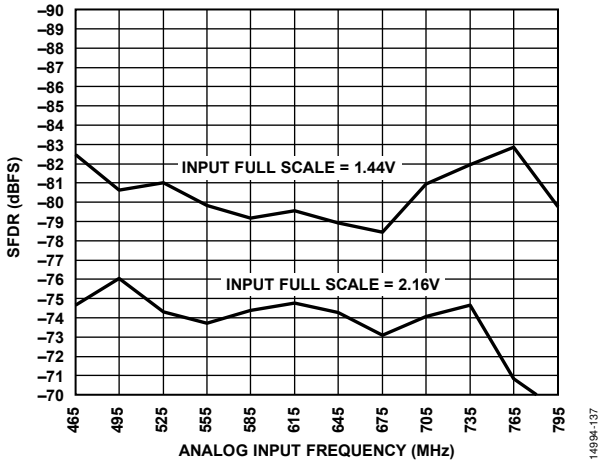


Figure 43. SFDR vs. Analog Input Frequency with Different Analog Input Full Scales (Third Nyquist Zone)

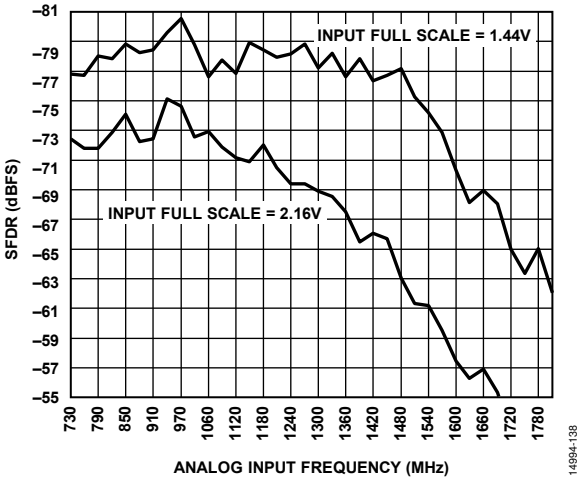


Figure 44. SFDR vs. Analog Input Frequency with Different Analog Input Full Scales (Fourth Nyquist Zone)

EQUIVALENT CIRCUITS

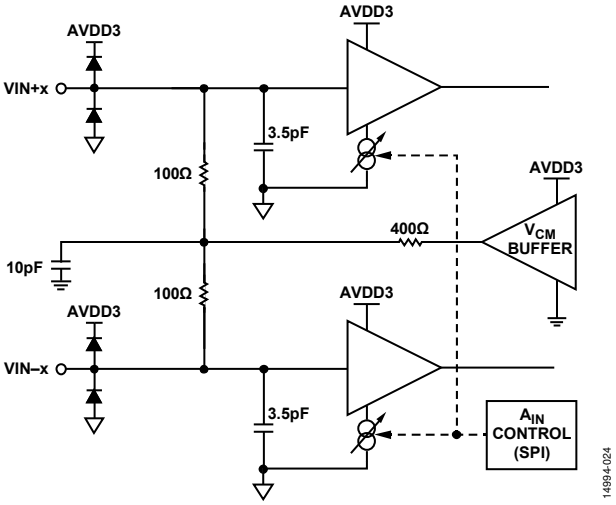


Figure 45. Analog Inputs

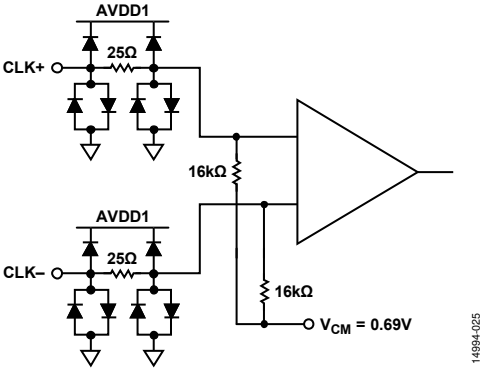


Figure 46. Clock Inputs

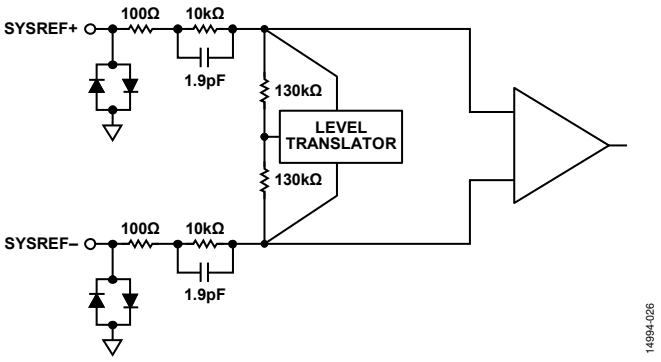


Figure 47. SYSREF± Inputs

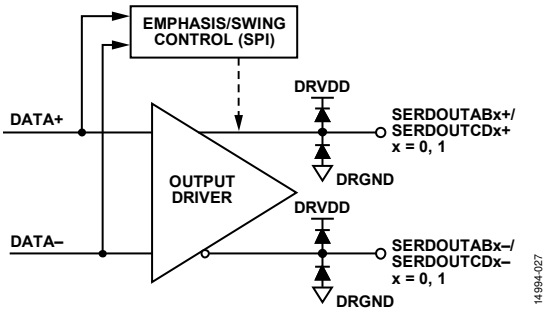


Figure 48. Digital Outputs

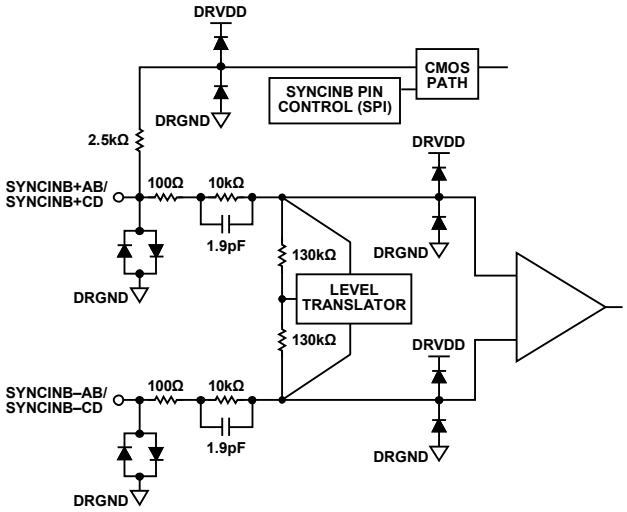


Figure 49. SYNCINB±AB, SYNCINB±CD Inputs

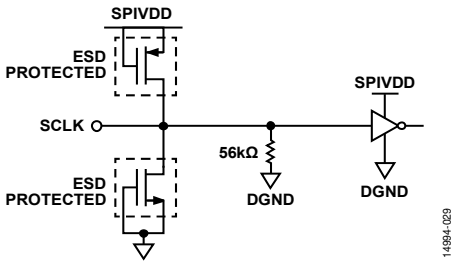


Figure 50. SCLK Input

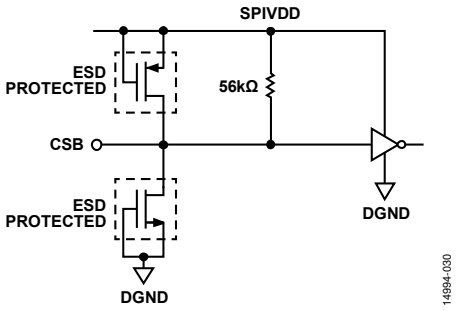


Figure 51. CSB Input

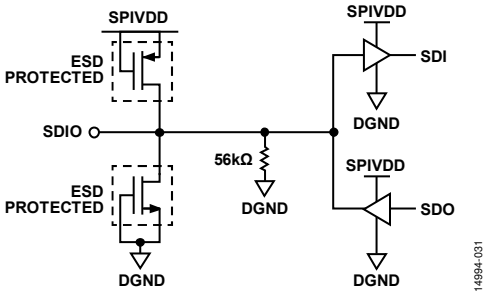


Figure 52. SDIO Input

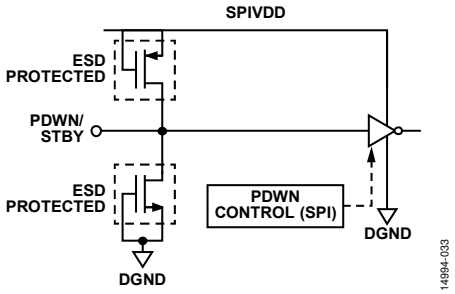


Figure 54. PDWN/STBY Input

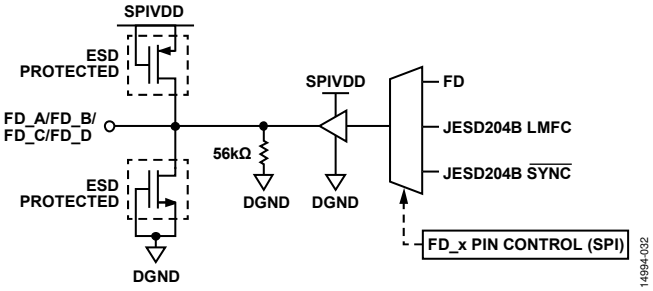


Figure 53. FD_A/FD_B/FD_C/FD_D Outputs

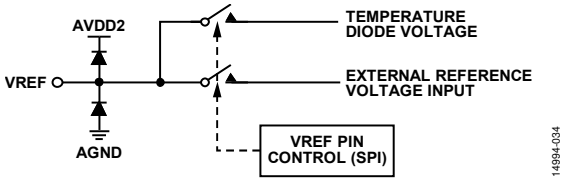


Figure 55. VREF Input/Output

THEORY OF OPERATION

ADC ARCHITECTURE

The architecture of the AD6684 consists of an input buffered pipelined ADC. The input buffer is designed to provide a 200 Ω termination impedance to the analog input signal. The equivalent circuit diagram of the analog input termination is shown in Figure 45.

The input buffer provides a linear high input impedance (for ease of drive) and reduces kickback from the ADC. The buffer is optimized for high linearity, low noise, and low power. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample while, at the same time, the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD6684 is a differential buffer with an internal common-mode voltage of 1.34 V. The clock signal alternately switches the input circuit between sample mode and hold mode. Either a differential capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This configuration ultimately creates a low-pass filter at the input, which limits unwanted broadband noise. See Figure 57 and Figure 58 for details on input network recommendations. For more information, see the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005). In general, the precise values depend on the application.

For best dynamic performance, the source impedances driving VIN+x and VIN−x must be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD6684, the available span is programmable through the SPI port from 1.44 V p-p to 2.16 V p-p differential with 1.80 V p-p differential being the default.

Dither

The AD6684 has internal on-chip dither circuitry that improves the ADC linearity and SFDR, particularly at smaller signal levels. A known but random amount of white noise is injected into the input of the AD6684. This dither improves the small signal linearity within the ADC transfer function and is precisely subtracted out digitally. The dither is turned on by default and does not reduce the ADC input dynamic range. The data sheet specifications and limits are obtained with the dither turned on. The dither can be disabled using SPI writes to Register 0x0922. Disabling the dither can slightly improve the SNR (by about 0.2 dB) at the expense of the small signal SFDR.

Differential Input Configurations

There are several ways to drive the AD6684, either actively or passively. However, optimum performance is achieved by driving the analog input differentially.

For applications where SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration (see Figure 57 and Figure 58) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD6684.

For low to midrange frequencies, a double balun or double transformer network (see Figure 57) is recommended for optimum performance of the AD6684. For higher frequencies in the second or third Nyquist zones, it is recommended to remove some of the front-end passive components to ensure wideband operation (see Figure 58).

Input Common Mode

The analog inputs of the AD6684 are internally biased to the common mode as shown in Figure 56.

For dc-coupled applications, the recommended operation procedure is to export the common-mode voltage to the VCM_CD/VREF pin using the SPI writes listed in this section. The common-mode voltage must be set by the exported value to ensure proper ADC operation. Disconnect the internal common-mode buffer from the analog input using Register 0x1908.

When performing SPI writes for dc coupling operation, use the following register settings in order:

1. Set Register 0x1908, Bit 2 to 1; this setting disconnects the internal common-mode buffer from the analog input.
2. Set Register 0x18A6 to 0x00; this setting turns off the voltage reference.
3. Set Register 0x18E6 to 0x00; this setting turns off the temperature diode export.
4. Set Register 0x18E0 to 0x04.
5. Set Register 0x18E1 to 0x1C.
6. Set Register 0x18E2 to 0x14.
7. Set Register 0x18E3, Bit 6 to 0x01; this setting turns on the VCM export.
8. Set Register 0x18E3, Bits[5:0] to the buffer current setting (copy the buffer current setting from Register 0x1A4C and Register 0x1A4D to improve the accuracy of the common-mode export).

Analog Input Controls and SFDR Optimization

The AD6684 offers flexible controls for the analog inputs, such as buffer current and input full-scale adjustment. All of the available controls are shown in Figure 56.

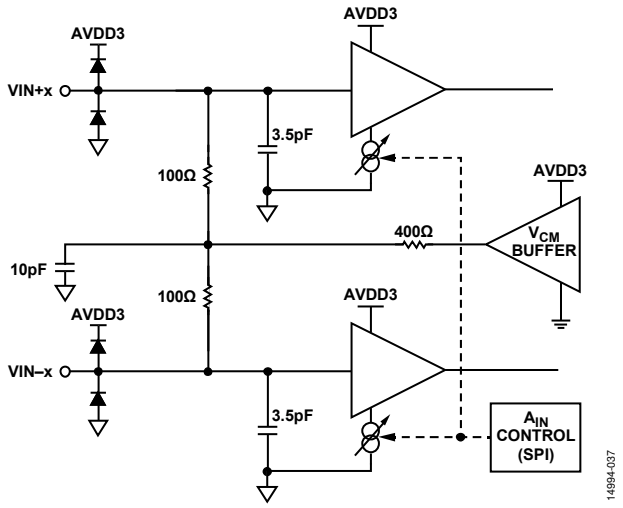


Figure 56. Analog Input Controls

Using Register 0x1A4C and Register 0x1A4D, the buffer currents on each channel can be scaled to optimize the SFDR over various input frequencies and bandwidths of interest. As the input buffer currents are set, the amount of current required by the AVDD3 supply changes. This relationship is shown in Figure 59. For a complete list of buffer current settings, see Table 46.

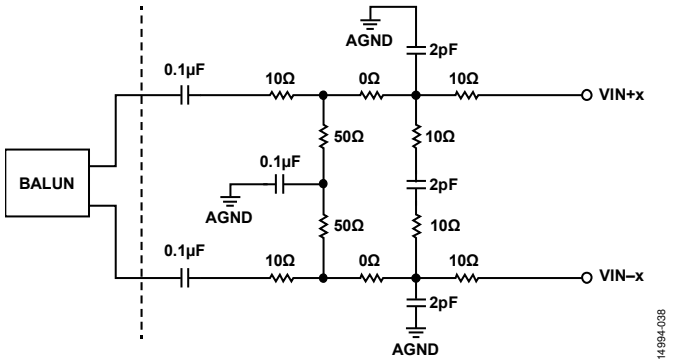


Figure 57. Differential Transformer Coupled Configuration for First and Second Nyquist Frequencies

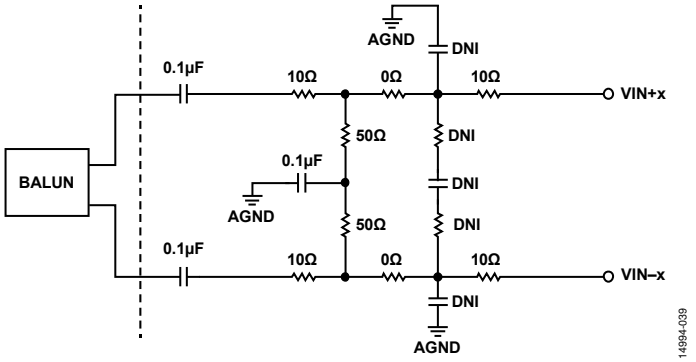


Figure 58. Differential Transformer Coupled Configuration for Third and Fourth Nyquist Zones