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RF Diversity and 1.2 GHz Bandwidth Observation Receiver

Data Sheet **AD6688**

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
  - Support for lane rates up to 16 Gbps per lane
- 1.7 W total power per channel at 3 GSPS (default settings)
- Performance at −2 dBFS amplitude, 2.6 GHz input
  - SFDR = 70 dBFS
  - NSD = −148.0 dBFS/Hz
- Performance at −9 dBFS amplitude, 2.6 GHz input
  - SFDR = 75 dBFS
  - NSD = −151.4 dBFS/Hz
- Integrated input buffer
- Noise density = −152.0 dBFS/Hz
- 0.975 V, 1.9 V, and 2.5 V dc supply operation
- 9 GHz analog input full power bandwidth (−3 dB)
- Amplitude detect bits for efficient AGC implementation
- Two Integrated wideband digital processors per channel
  - 48-bit NCO
  - 4 cascaded half band filters
- Phase coherent NCO switching
  - Up to 4 channels available
- Serial port control
  - Integer clock divide by 2 and divide by 4
  - Flexible JESD204B lane configurations
- On-chip dither

APPLICATIONS

- Diversity multiband, multimode digital receivers
- 3G/4G, TD-SCDMA, W-CDMA, GSM, LTE, LTE-A
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers

FUNCTIONAL BLOCK DIAGRAM

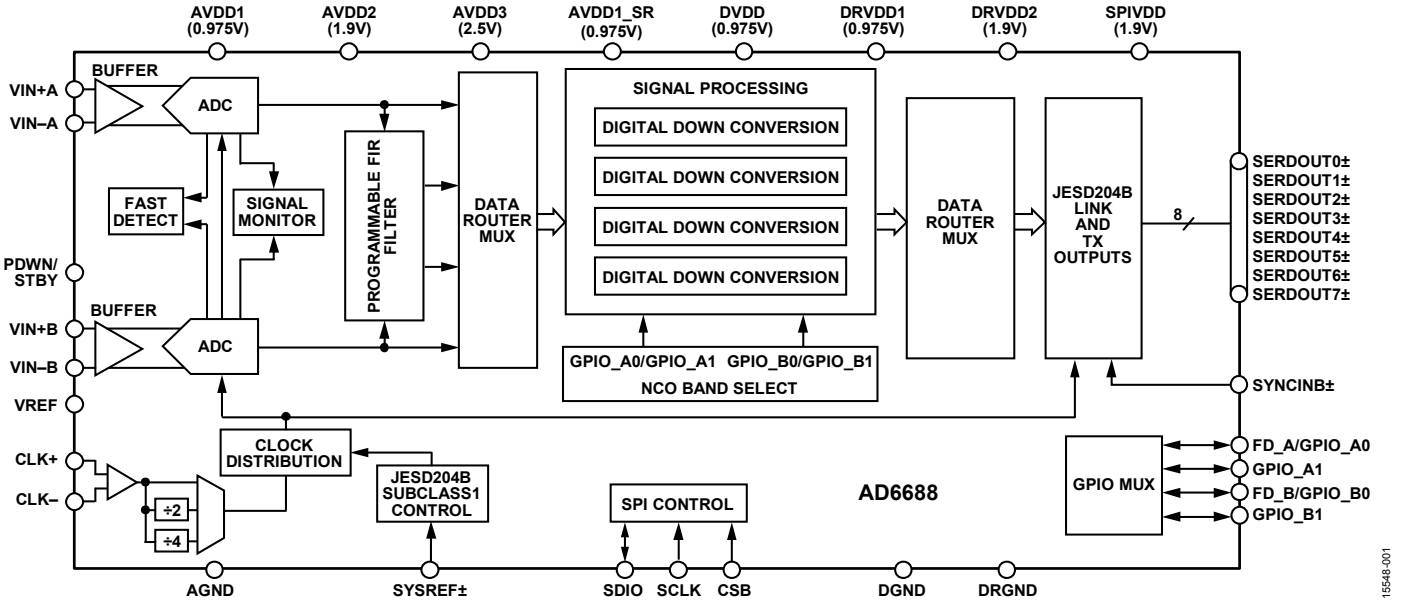

Figure 1.

Rev. 0 Document Feedback

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Technical Support www.analog.com

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REVISION HISTORY

4/2017—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD6688 is a 1.2 GHz bandwidth, mixed-signal, direct radio frequency (RF) sampling receiver. It consists of two 14-bit, 3.0 GSPS analog-to-digital converters (ADCs) and various digital signal processing blocks consisting of four wideband digital downconverters (DDCs). The AD6688 has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed to support communications applications capable of direct sampling wide bandwidth analog signals of up to 5 GHz. The 3 dB bandwidth of the ADC input is greater than 9 GHz. The AD6688 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. The analog input and clock signals are differential inputs. The ADC data outputs are internally connected to four DDCs through a crossbar mux. Each DDC consists of up to five cascaded signal processing stages: a 48-bit numerically controlled oscillator (NCO) and up to four half-band decimation filters. The NCO has the option to select preset bands over the general-purpose input/output (GPIO) pins, which enables selection of up to three bands. Operation of the AD6688 between the DDC modes is selectable via SPI-programmable profiles.

In addition to the DDC blocks, the AD6688 has several functions that simplify the automatic gain control (AGC) function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect control bits in Register 0x0245 of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input. Besides the fast detect outputs, the AD6688 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal being digitized by the ADC.

The user can configure the Subclass 1 JESD204B-based high speed serialized output in a variety of one-lane, two-lane, four-lane, six-lane, and eight-lane configurations, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multidevice synchronization is supported through the SYSREF± and SYNCINB± input pins.

The AD6688 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 3-wire serial port interface (SPI).

The AD6688 is available in a Pb-free, 196-ball BGA specified over the −40°C to +85°C ambient temperature range. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Wide full power bandwidth supports IF sampling of signals up to 9 GHz (−3 dB point).
2. Four integrated wide-band decimation filter and NCO blocks supporting multiband receivers.
3. Fast NCO switching enabled through GPIO pins.
4. Flexible SPI controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection and signal monitoring.
6. On-chip temperature diode for system thermal management.
7. 12 mm × 12 mm, 196-ball BGA.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, sampling rate = 3000 MHz, 1.7 V p-p full-scale differential input, input amplitude (A_{IN}) = −2.0 dBFS, L = 8, M = 2, F = 1, −10°C ≤ T_J ≤ +120°C[1], unless otherwise noted. Typical specifications represent performance at T_J = 70°C (T_A = 25°C).

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
ACCURACY				
No Missing Codes		Guaranteed		
Offset Error		0		%FSR
Offset Matching		0		%FSR
Gain Error	−5.89	±1	+5.89	%FSR
Gain Matching	−2.9	±0.2	+2.9	%FSR
Differential Nonlinearity (DNL)	−0.63	±0.4	+0.74	LSB
Integral Nonlinearity (INL)	−26	±6	+21	LSB
TEMPERATURE DRIFT				
Offset Error		±15		ppm/°C
Gain Error		440		ppm/°C
INTERNAL VOLTAGE REFERENCE		0.5		V
ANALOG INPUTS				
Differential Input Voltage Range		1.7		V p-p
Common-Mode Voltage (V_{CM})	1.32	1.35	1.52	V
Differential Input Resistance		200		Ω
Differential Input Capacitance		0.25		pF
Differential Input Return Loss at 2.1 GHz[2]		−7		dB
−3 dB Bandwidth		9		GHz
POWER SUPPLY				
AVDD1	0.95	0.975	1.0	V
AVDD2	1.85	1.9	1.95	V
AVDD3	2.44	2.5	2.56	V
AVDD1_SR	0.95	0.975	1.0	V
DVDD	0.95	0.975	1.0	V
DRVDD1	0.95	0.975	1.0	V
DRVDD2	1.85	1.9	1.95	V
SPIVDD	1.85	1.9	1.95	V
I_{AVDD1}		640	765	mA
I_{AVDD2}		790	885	mA
I_{AVDD3}		110	120	mA
I_{AVDD1_SR}		24	50	mA
I_{DVDD}		480	1020	mA
I_{DRVDD1}[3]		320	590	mA
I_{DRVDD2}		30	35	mA
I_{SPIVDD}		1	5	mA

Parameter	Min	Typ	Max	Unit
POWER CONSUMPTION				
Total Power Dissipation (Including Output Drivers)[4]		3.3		W
Power-Down Dissipation		300		mW
Standby[5]		1.65		mW

[1] Junction temperature (T_J) range of −10°C to +120°C translates to an ambient temperature range of −40°C to+85°C.
[2] For more information, see the Analog Input Considerations section.
[3] All lanes running. Power dissipation on DRVDD1 changes with lane rate and number of lanes used.
[4] Default mode. No DDCs used.
[5] Can be controlled by SPI.

AC SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, sampling rate = 3000 MHz, 1.7 V p-p full-scale differential input, DDC decimation ratio = 8, −10°C ≤ T_J ≤ +120°C[1], unless otherwise noted. Typical specifications represent performance at T_J = 70°C (T_A = 25°C).

Table 2.

	A_{IN} = −2 dBFS			A_{IN} = −9 dBFS			
Parameter[2]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
ANALOG INPUT FULL SCALE (DIFFERENTIAL)	1.1	1.7	2.04	1.1	1.7	2.04	V p-p
NOISE FIGURE		24.5			24.5		dB
NOISE SPECTRAL DENSITY (NSD)							
Input Frequency (f_{IN}) = 10 MHz, A_{IN} = −30 dBFS (2.04 V p-p)		−153.6			−153.6		dBFS/Hz
f_{IN} = 10 MHz, A_{IN} = −30 dBFS		−152.0			−152.0		dBFS/Hz
f_{IN} = 255 MHz		−151.5			−152.0		dBFS/Hz
f_{IN} = 950 MHz		−150.5			−151.9		dBFS/Hz
f_{IN} = 1870 MHz		−149.9			−151.9		dBFS/Hz
f_{IN} = 2170 MHz		−149.7			−151.8		dBFS/Hz
f_{IN} = 2600 MHz		−148.0	−143.9		−151.4		dBFS/Hz
IN-BAND SIGNAL-TO-NOISE RATIO (SNR)[3]							
f_{IN} = 950 MHz, NCO Tuning Frequency = 942.5 MHz		65.8			67.7		dBFS
f_{IN} = 1870 MHz, NCO Tuning Frequency = 1842.0 MHz		65.2			67.2		dBFS
f_{IN} = 2170 MHz, NCO Tuning Frequency = 2140.0 MHz		65.0			67.1		dBFS
f_{IN} = 2600 MHz, NCO Tuning Frequency = 2655.0 MHz		63.4			66.7		dBFS
IN-BAND SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)[3]							
f_{IN} = 950 MHz, NCO Tuning Frequency = 942.5 MHz		65.6			67.7		dBFS
f_{IN} = 1870 MHz, NCO Tuning Frequency = 1842.0 MHz		65.1			67.1		dBFS
f_{IN} = 2170 MHz, NCO Tuning Frequency = 2140.0 MHz		64.8			67.0		dBFS
f_{IN} = 2600 MHz, NCO Tuning Frequency = 2655.0 MHz		63.2			66.5		dBFS
SPURIOUS FREE DYNAMIC RANGE (SFDR), SECOND OR THIRD HARMONIC[4]							
f_{IN} = 950 MHz		71			78		dBFS
f_{IN} = 1870 MHz		69			76		dBFS
f_{IN} = 2170 MHz		67			73		dBFS
f_{IN} = 2600 MHz	51	70			75		dBFS
IN-BAND SPURIOUS FREE DYNAMIC RANGE (SFDR), WORST HARMONIC[5]							
f_{IN} = 950 MHz, NCO Tuning Frequency = 942.5 MHz		71			91		dBFS
f_{IN} = 1870 MHz, NCO Tuning Frequency = 1842.0 MHz		90			96		dBFS
f_{IN} = 2170 MHz, NCO Tuning Frequency = 2140.0 MHz		88			92		dBFS
f_{IN} = 2600 MHz, NCO Tuning Frequency = 2655.0 MHz		89			92		dBFS
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC[6]							
f_{IN} = 950 MHz		−86			−95		dBFS
f_{IN} = 1870 MHz		−84			−94		dBFS
f_{IN} = 2170 MHz		−83			−94		dBFS
f_{IN} = 2600 MHz		−79	−66		−90		dBFS

Parameter[2]	A_{IN} = −2 dBFS Min	Typ	Max	A_{IN} = −9 dBFS Min	Typ	Max	Unit
TWO-TONE INTERMODULATION DISTORTION (IMD), A_{IN1} AND A_{IN2} = −15.0 dBFS f_{IN1} = 1.841 GHz, f_{IN2} = 1.846 GHz; NCO Frequency = 1874.28 MHz		N/A[7]			96		dBFS
CROSSTALK[8]		>90			>90		dB
ANALOG INPUT BANDWIDTH, FULL POWER[9]		5			5		GHz

[1] Junction temperature (T_J) range of −10°C to +120°C translates to an ambient temperature range of −40°C to +85°C.
[2] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[3] In-band SNR is dependent on the DDC decimation ratio (DCM) and is calculated by |NSD| = |SNR| + 10 × log(f_S/(2 × DCM)), where f_S = ADC sample clock rate.
[4] SFDR is specified with DDCs bypassed.
[5] In-band SFDR is defined as the worst spur within the alias protected bandwidth of the DDC outputs. When DDCs are enabled, SFDR changes with DDC decimation settings, NCO frequency, and overall frequency plan.
[6] Worst other harmonic is specified with DDCs bypassed.
[7] N/A means not applicable.
[8] Crosstalk is measured at 950 MHz with a −2.0 dBFS analog input on one channel, and no input on the adjacent channel.
[9] Full power bandwidth is the bandwidth of operation in which proper ADC performance can be achieved.

DIGITAL SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, sampling rate = 3000 MHz, 1.7 V p-p full-scale differential input, A_{IN} = −2.0 dBFS, L = 8, M = 2, F = 1, −10°C ≤ T_J ≤ +120°C[1], unless otherwise noted. Typical specifications represent performance at T_J = 70°C (T_A = 25°C).

Table 3.

Parameter	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	300	800	1800	mV p-p
Input Common-Mode Voltage		0.675		V
Input Resistance (Differential)		106		Ω
Input Capacitance		0.9		pF
Differential Input Return Loss at 3 GHz[2]		−9.4		dB
SYSREF INPUTS (SYSREF+, SYSREF−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage		0.675	2.0	V
Input Resistance (Differential)		18		kΩ
Input Capacitance (Differential)		1		pF
LOGIC INPUT (SDIO, SCLK, CSB, PDWN/STBY, FD_A/GPIO_A0, FD_B/GPIO_B0, GPIO_A1, GPIO_B1)				
Logic Compliance		CMOS		
Logic 1 Voltage	0.65 × SPIVDD			V
Logic 0 Voltage	0		0.35 × SPIVDD	V
Input Resistance		30		kΩ
LOGIC OUTPUT (SDIO, FD_A, FD_B)				
Logic Compliance		CMOS		
Logic 1 Voltage (I_{OH} = 4 mA)	SPIVDD − 0.45V			V
Logic 0 Voltage (I_{OL} = 4 mA)	0		0.45	V
SYNCIN INPUT (SYNCINB+/SYNCINB−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage		0.675	2.0	V
Input Resistance (Differential)		18		kΩ
Input Capacitance		1		pF
SYNCINB+ INPUT				
Logic Compliance		CMOS		
Logic 1 Voltage	0.9 × DRVDD1		2 × DRVDD1	V
Logic 0 Voltage			0.1 × DRVDD1	V
Input Resistance		2.6		kΩ
DIGITAL OUTPUTS (SERDOUTx±, x = 0 TO 7)				
Logic Compliance		SST		
Differential Output Voltage	360	560	770	mV p-p
Differential Termination Impedance	80	100	120	Ω

[1] Junction temperature (T_J) range of −10°C to +120°C translates to an ambient temperature range of −40°C to+85°C.
[2] Reference impedance = 100 Ω.

SWITCHING SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, sampling rate = 3000 MHz, 1.7 V p-p full-scale differential input, A_{IN} = −2.0 dBFS, L = 8, M = 2, F = 1, −10°C ≤ T_J ≤ +120°C[1], unless otherwise noted. Typical specifications represent performance at T_J = 70°C (T_A = 25°C).

Table 4.

Parameter	Min	Typ	Max	Unit
CLOCK				
Clock Rate (at CLK+/CLK− Pins)		3	6	GHz
Sample Rate[2]	2500	3000	3100	MSPS
Clock Pulse Width High	161.29	166.67	192.31	ps
Clock Pulse Width Low	161.29	166.67	192.31	ps
OUTPUT PARAMETERS				
Unit Interval (UI)[3]	62.5	66.67	592.6	ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)		26		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)		26		ps
Phase-Locked Loop (PLL) Lock Time		5		ms
Data Rate per Channel (NRZ)[4]	1.6875	15	16	Gbps
LATENCY[5]				
Pipeline Latency		75		Clock cycles
Fast Detect Latency		26		Clock cycles
WAKE-UP TIME				
Standby		400		µs
Power-Down		15		ms
NCO CHANNEL SELCTION TO OUTPUT			8	Clock cycles
APERTURE				
Aperture Delay (t_A)		250		ps
Aperture Uncertainty (Jitter, t_J)		55		fs rms
Out of Range Recovery Time		1		Clock cycles

[1] Junction temperature (T_J) range of −10°C to +120°C translates to an ambient temperature range of −40°C to+85°C.
[2] The maximum sample rate is the clock rate after the divider.
[3] Baud rate = 1/UI. A subset of this range can be supported.
[4] Default L = 8. This number can be changed based on the sample rate and decimation ratio.
[5] No DDCs used. L = 8, M = 2, F = 1.

TIMING SPECIFICATIONS

Table 5.

Parameter	Description	Min	Typ	Max	Unit
CLK+ to SYSREF+ TIMING REQUIREMENTS					
t_{SU_SR}	Device clock to SYSREF+ setup time		−65		ps
t_{H_SR}	Device clock to SYSREF+ hold time		95		ps
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns

Timing Diagrams

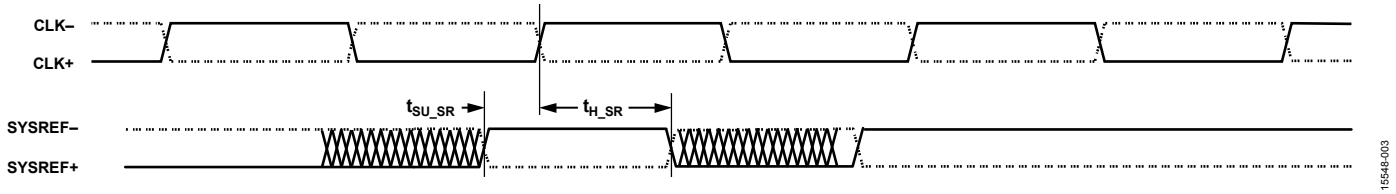

Figure 2. SYSREF± Setup and Hold Timing

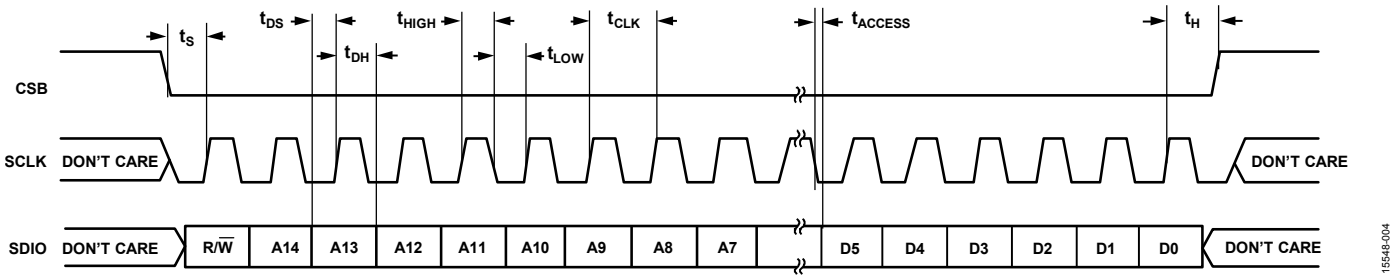

Figure 3. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.05 V
AVDD1_SR to AGND	1.05 V
AVDD2 to AGND	2.0 V
AVDD3 to AGND	2.70 V
DVDD to DGND	1.05 V
DRVDD1 to DRGND	1.05 V
DRVDD2 to DRGND	2.0 V
SPIVDD to DGND	2.0 V
AGND to DRGND	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
DGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	AGND − 0.3 V to AVDD3 + 0.3 V
CLK± to AGND	AGND − 0.3 V to AVDD1 + 0.3 V
SCLK, SDIO, CSB to DGND	DGND − 0.3 V to SPIVDD + 0.3 V
PDWN/STBY to DGND	DGND − 0.3 V to SPIVDD + 0.3 V
SYSREF± to AGND	2.5 V
SYNCINB± to DRGND	2.5 V
Junction Temperature Range (T_J)	−40°C to +125°C
Storage Temperature Range, Ambient (T_A)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC_TOP}	Ψ_{JB}	Ψ_{JT}	Unit
BP-196-4[1]	16.26	1.4	5.44	1.68	°C/W

[1] Test Condition 1: Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with 190 thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AVDD2	AVDD2	AVDD1	AVDD1[1]	AVDD1[1]	AGND[1]	CLK+	CLK–	AGND[1]	AVDD1[1]	AVDD1[1]	AVDD1	AVDD2	AVDD2
B	AVDD2	AVDD2	AVDD1	AVDD1[1]	AGND	AGND[1]	AGND[1]	AGND[1]	AGND[1]	AGND	AVDD1[1]	AVDD1	AVDD2	AVDD2
C	AVDD2	AVDD2	AVDD1	AGND	AGND	AGND[1]	AGND[1]	AGND[1]	AGND[1]	AGND	AGND	AVDD1	AVDD2	AVDD2
D	AVDD3	AGND	AGND	AGND	AGND	AGND	AGND[1]	AGND[1]	AGND	AGND	AGND	AGND	AGND	AVDD3
E	VIN–B	AGND	AGND	AGND	AGND	AGND[2]	AVDD1_SR	AGND[2]	AGND	AGND	AGND	AGND	AGND	VIN–A
F	VIN+B	AGND	AGND	AGND	AGND	AGND	SYSREF+	SYSREF–	AGND	AGND	AGND	AGND	AGND	VIN+A
G	AVDD3	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AVDD3
H	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	VREF	AGND	AGND	AGND	AGND
J	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND
K	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]
L	DGND	GPIO_B1	SPIVDD	FD_B/ GPIO_B0	CSB	SCLK	SDIO	PDWN/ STBY	FD_A/ GPIO_A0	SPIVDD	GPIO_A1	DGND	DGND	DGND
M	DGND	DGND	DRGND	DRGND	DRVDD1	DRVDD1	DRVDD1	DRVDD1	DRGND	DRGND	DRVDD1	DRGND	DRVDD2	DVDD
N	DVDD	DVDD	DRGND	SERDOUT7+	SERDOUT6+	SERDOUT5+	SERDOUT4+	SERDOUT3+	SERDOUT2+	SERDOUT1+	SERDOUT0+	DRGND	SYNCINB+	DVDD
P	DVDD	DVDD	DRGND	SERDOUT7–	SERDOUT6–	SERDOUT5–	SERDOUT4–	SERDOUT3–	SERDOUT2–	SERDOUT1–	SERDOUT0–	DRGND	SYNCINB–	DVDD

[1]DENOTES CLOCK DOMAIN.
[2]DENOTES SYSREF± DOMAIN.
[3]DENOTES ISOLATION DOMAIN.

15548-005

Figure 4. Pin Configuration (Top View)

Table 8. Pin Function Descriptions[1]

Pin No.	Mnemonic	Type	Description
Power Supplies			
A3, A12, B3, B12, C3, C12	AVDD1	Power	Analog Power Supply (0.975 V Nominal).
A4, A5, A10, A11, B4, B11	AVDD1[2]	Power	Analog Power Supply for the Clock Domain (0.975 V Nominal).
A1, A2, A13, A14, B1, B2, B13, B14, C1, C2, C13, C14	AVDD2	Power	Analog Power Supply (1.9 V Nominal).
D1, D14, G1, G14	AVDD3	Power	Analog Power Supply (2.5 V Nominal).
E7	AVDD1_SR	Power	Analog Power Supply for SYSREF± (0.975 V Nominal).
L3, L10	SPIVDD	Power	Digital Power Supply for SPI (1.9 V Nominal).
M14, N1, N2, N14, P1, P2, P14	DVDD	Power	Digital Power Supply (0.975 V Nominal).
M5 to M8, M11	DRVDD1	Power	Digital Driver Power Supply (0.975 V Nominal).
M13	DRVDD2	Power	Digital Driver Power Supply (1.9 V Nominal).
B5, B10, C4, C5, C10, C11, D2 to D6, D9 to D13, E2 to E5, E9 to E13, F2 to F6, F9 to F13, G2 to G13, H1 to H9, H11 to H14, J1 to J14	AGND	Ground	Analog Ground. These pins connect to the analog ground plane.
A6, A9, B6 to B9, C6 to C9, D7, D8	AGND[2]	Ground	Ground Reference for Clock Domain.
E6, E8	AGND[3]	Ground	Ground Reference for SYSREF±.
K1 to K14	AGND[4]	Ground	Isolation Ground.
L1, L12 to L14, M1, M2	DGND	Ground	Digital Control Ground Supply. These pins connect to the digital ground plane.
M3, M4, M9, M10, M12, N3, N12, P3, P12	DRGND	Ground	Digital Driver Ground Supply. These pins connect to the digital driver ground plane.
Analog			
E1, F1	VIN−B, VIN+B	Input	ADC B Analog Input Complement/True.
E14, F14	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
A7, A8	CLK+, CLK−	Input	Clock Input True/Complement.
H10	VREF	Input/DNC	0.50 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or an input. Do not connect this pin if using the internal reference. This pin requires a 0.50 V reference voltage input if using an external voltage reference source.
CMOS Inputs/Outputs			
L2	GPIO_B1	Input/Output	GPIO B1.
L4	FD_B/GPIO_B0	Input/Output	Fast Detect Outputs for Channel B/GPIO B0.
L9	FD_A/GPIO_A0	Input/Output	Fast Detect Outputs for Channel A/GPIO A0.
L11	GPIO_A1	Input/Output	GPIO A1.
Digital Inputs			
F7, F8	SYSREF+, SYSREF−	Input	Active High JESD204B LVDS System Reference Input True/Complement.
N13	SYNCINB+	Input	Active Low JESD204B LVDS/CMOS Sync Input True.
P13	SYNCINB−	Input	Active Low JESD204B LVDS Sync Input Complement.
Data Outputs			
N4, P4	SERDOUT7+, SERDOUT7−	Output	Lane 7 Output Data True/Complement.
N5, P5	SERDOUT6+, SERDOUT6−	Output	Lane 6 Output Data True/Complement.
N6, P6	SERDOUT5+, SERDOUT5−	Output	Lane 5 Output Data True/Complement.
N7, P7	SERDOUT4+, SERDOUT4−	Output	Lane 4 Output Data True/Complement.
N8, P8	SERDOUT3+, SERDOUT3−	Output	Lane 3 Output Data True/Complement.
N9, P9	SERDOUT2+, SERDOUT2−	Output	Lane 2 Output Data True/Complement.
N10, P10	SERDOUT1+, SERDOUT1−	Output	Lane 1 Output Data True/Complement.
N11, P11	SERDOUT0+, SERDOUT0−	Output	Lane 0 Output Data True/Complement.

Pin No.	Mnemonic	Type	Description
Digital Controls			
L8	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.
L5	CSB	Input	SPI Chip Select (Active Low).
L6	SCLK	Input	SPI Serial Clock.
L7	SDIO	Input/Output	SPI Serial Data Input/Output.

[1] See the Theory of Operation section and Applications Information section for more information on isolating the planes for optimal performance.
[2] Denotes clock domain.
[3] Denotes SYSREF± domain.
[4] Denotes isolation domain.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, sampling rate = 3000 MHz, 1.7 V p-p full-scale differential input, DDC decimation rate = 8, default buffer current settings, T_A = 25°C, 128,000 FFT sample, unless otherwise noted. See Table 10 for the recommended settings.

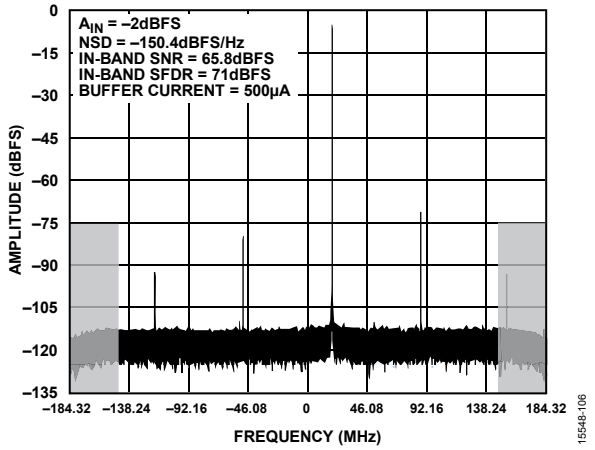

Figure 5. Single-Tone FFT at f_{IN} = 960 MHz, NCO Frequency = 942.5 MHz, A_{IN} = –2 dBFS, f_S = 2.94912 GHz

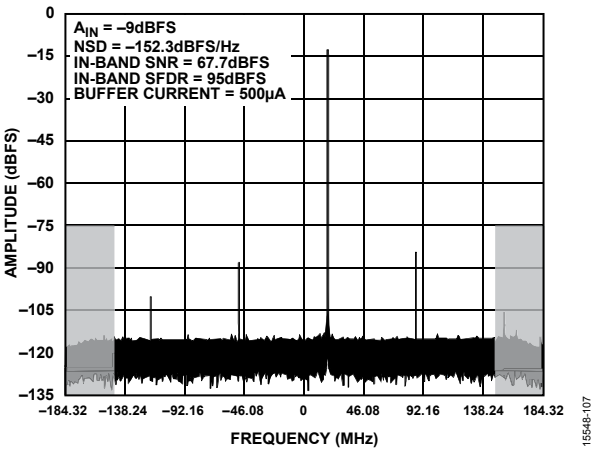

Figure 6. Single-Tone FFT at f_{IN} = 960 MHz, NCO Frequency = 942.5 MHz, A_{IN} = –9 dBFS; f_S = 2.94912 GHz

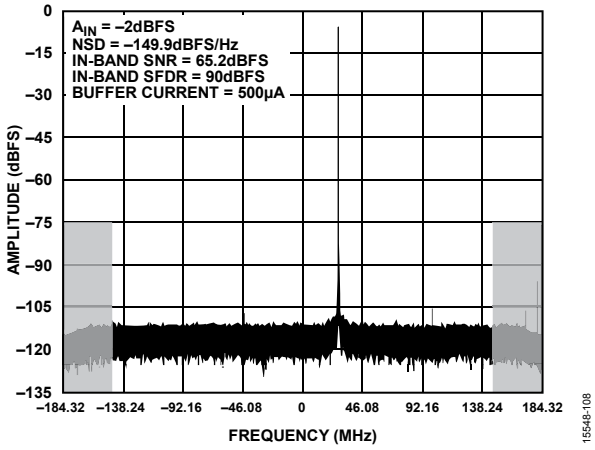

Figure 7. Single-Tone FFT at f_{IN} = 1870 MHz, NCO Frequency = 1842 MHz, A_{IN} = –2 dBFS; f_S = 2.94912 GHz

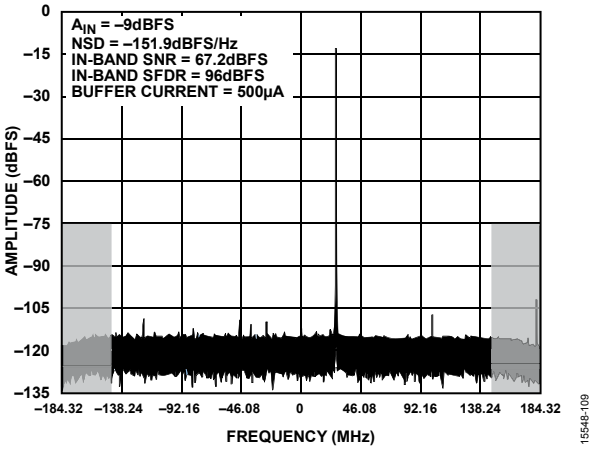

Figure 8. Single-Tone FFT at f_{IN} = 1870 MHz, NCO Frequency = 1842 MHz, A_{IN} = –9 dBFS; f_S = 2.94912 GHz

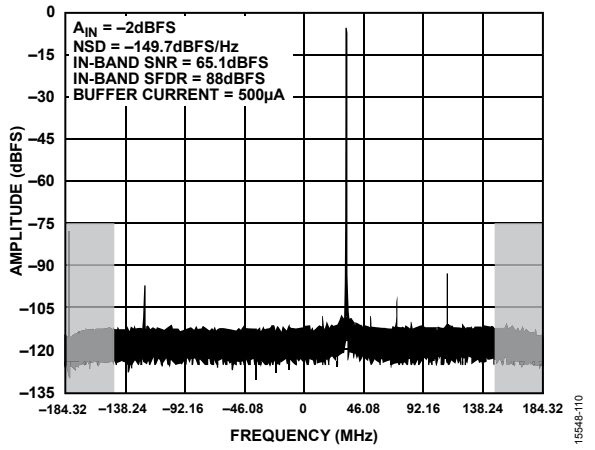

Figure 9. Single-Tone FFT at f_{IN} = 2170 MHz, NCO Frequency = 2140 MHz, A_{IN} = –2 dBFS; f_S = 2.94912 GHz

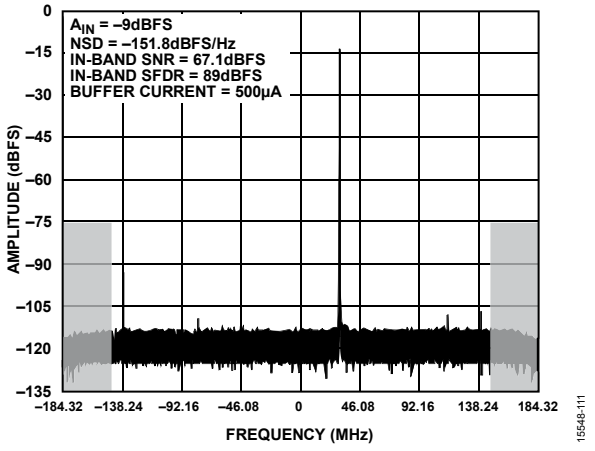

Figure 10. Single-Tone FFT at f_{IN} = 2170 MHz, NCO Frequency = 2140 MHz, A_{IN} = –9 dBFS; f_S = 2.94912 GHz

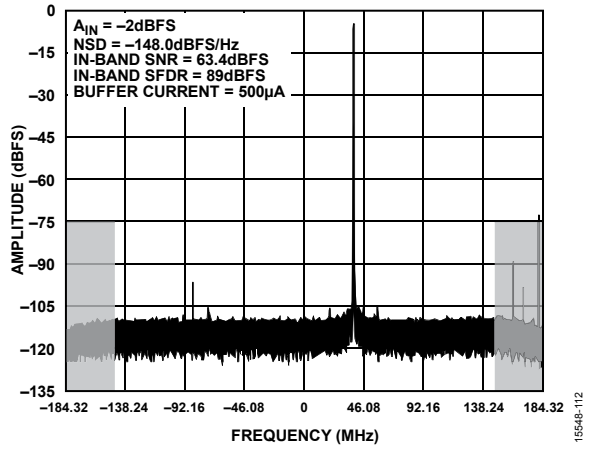

Figure 11. Single-Tone FFT at f_{IN} = 2690 MHz, NCO Frequency = 2655 MHz, A_{IN} = –2 dBFS; f_S = 2.94912 GHz

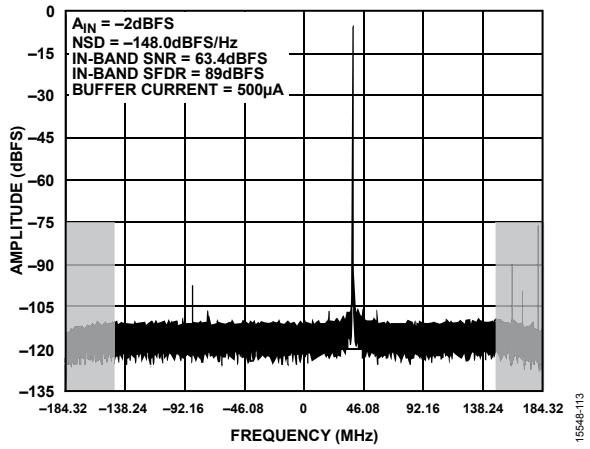

Figure 12. Single-Tone FFT at f_{IN} = 2690 MHz, NCO Frequency = 2655 MHz, A_{IN} = –2 dBFS; f_S = 2.94912 GHz

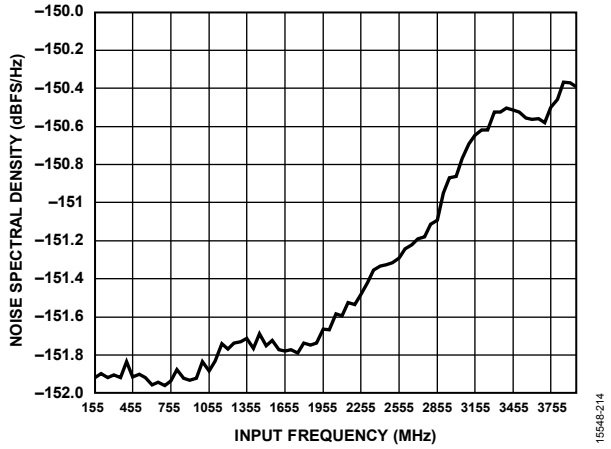

Figure 13. NSD vs. f_{IN}; A_{IN} = –9 dBFS

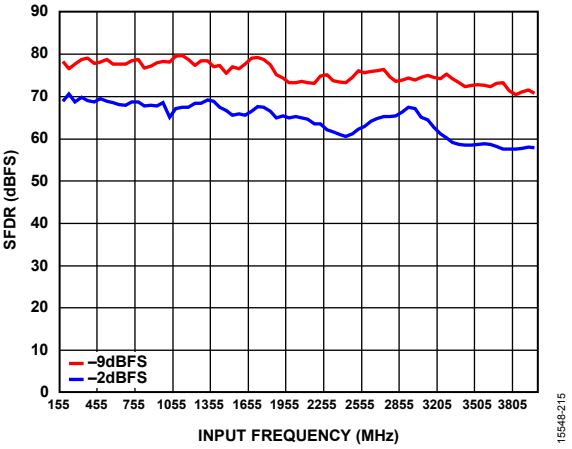

Figure 14. SFDR vs. f_{IN}; A_{IN} = –2 dBFS and –9 dBFS

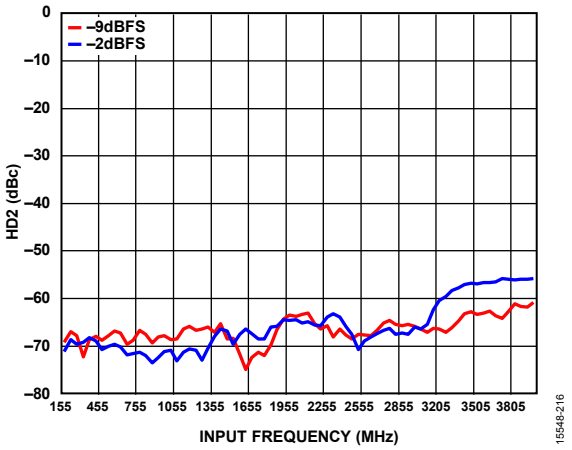

Figure 15. Second Harmonic Distortion (HD2) vs. f_{IN}; A_{IN} = –2 dBFS and –9 dBFS

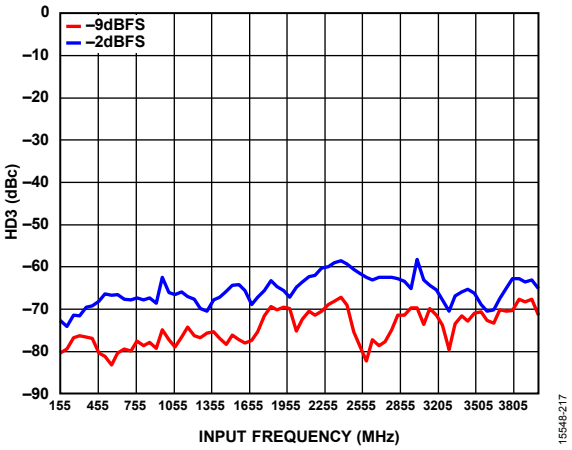

Figure 16. Third Harmonic Distortion (HD3) vs. f_{IN}; A_{IN} = –2 dBFS and –9 dBFS

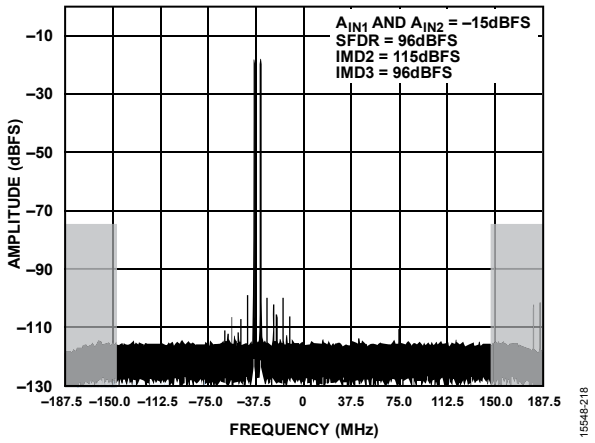

Figure 17. Two-Tone FFT; f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz; NCO Frequency = 1874.28 MHz; f_S = 3 GHz

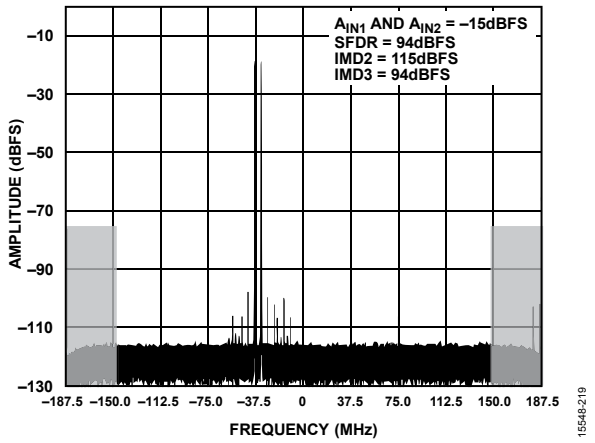

Figure 18. Two-Tone FFT; f_{IN1} = 2137.5 MHz, f_{IN2} = 2142.5 MHz NCO Frequency = 2176.92 MHz; f_S = 3 GHz

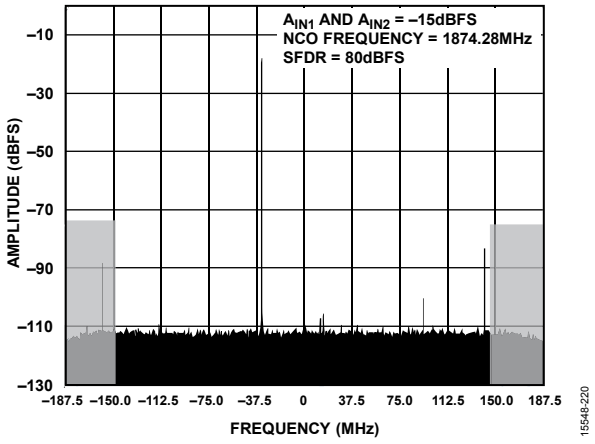

Figure 19. Two-Tone FFT; f_{IN1} = 1800 MHz, f_{IN2} = 2100 MHz NCO Frequency = 1874.28 MHz; f_S = 2.94912 GHz

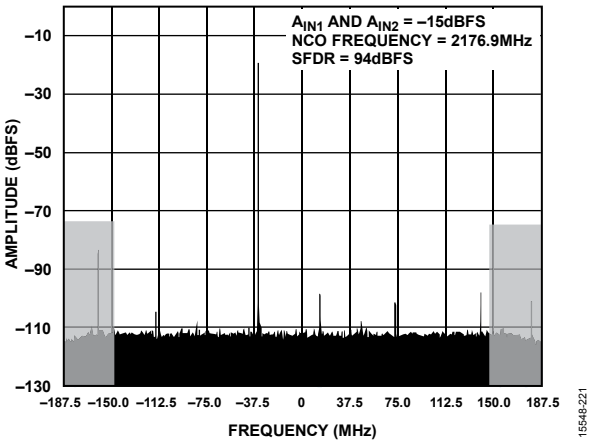

Figure 20. Two-Tone FFT; f_{IN1} = 1800 MHz, f_{IN2} = 2100 MHz NCO Frequency = 2176.92 MHz; f_S = 2.94912 GHz

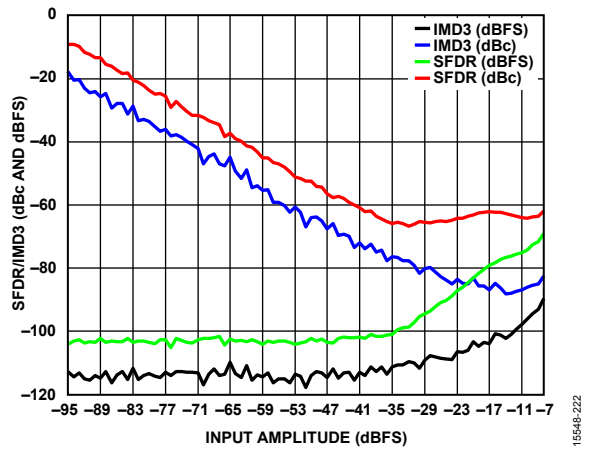

Figure 21. Two-Tone SFDR/IMD3 vs. Input Amplitude with f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz

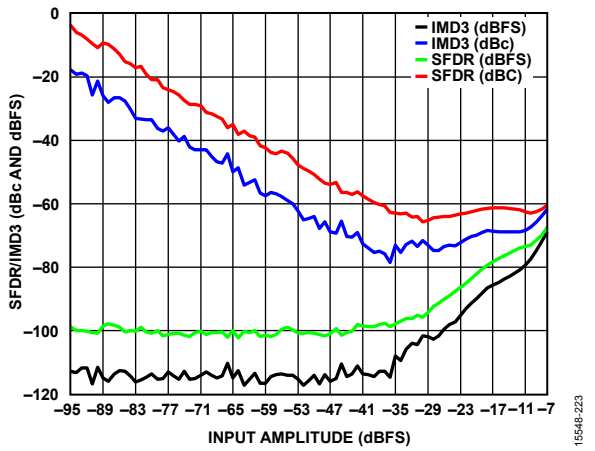

Figure 22. Two-Tone SFDR/IMD3 vs. Input Amplitude with f_{IN1} = 2137.5 MHz, f_{IN2} = 2142.5 MHz

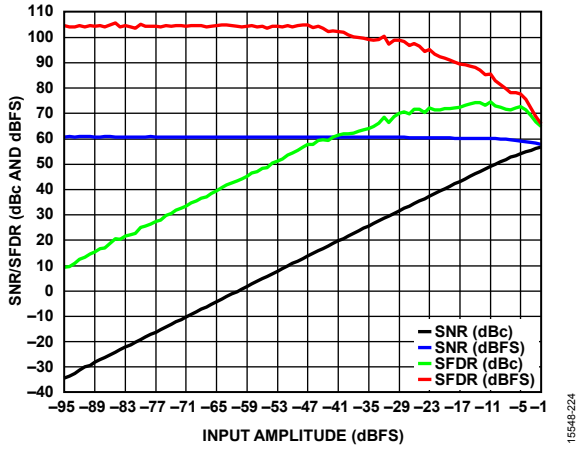

Figure 23. SNR/SFDR vs. Input Amplitude, f_{IN} = 950 MHz

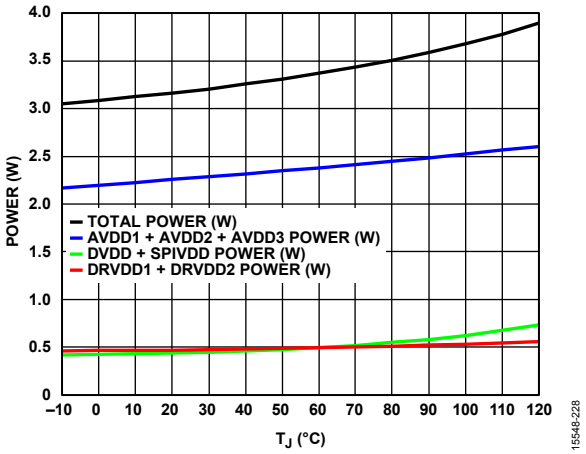

Figure 26. Power vs. Junction Temperature, f_{IN} = 950 MHz

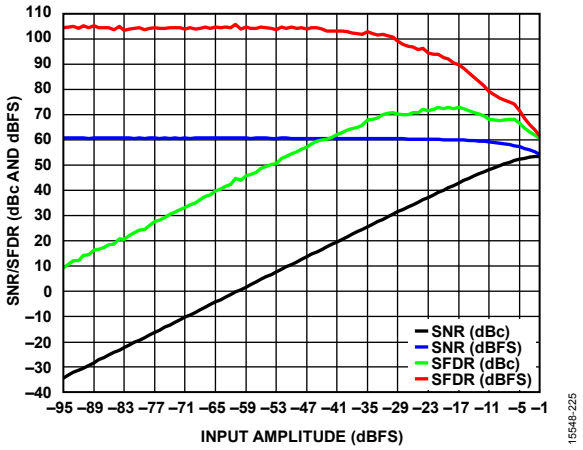

Figure 24. SNR/SFDR vs. Input Amplitude, f_{IN} = 1800 MHz

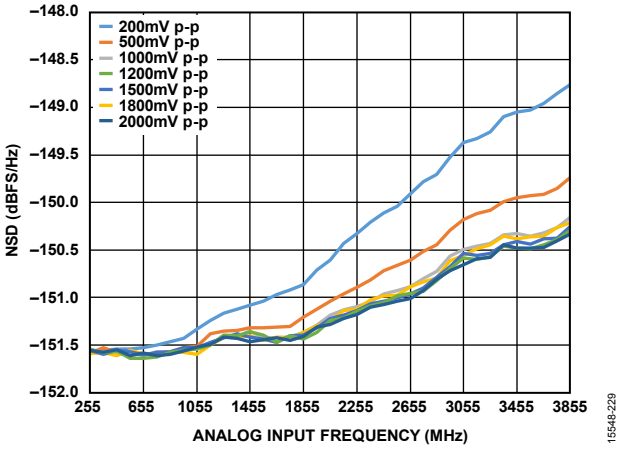

Figure 27. NSD vs. Analog Input Frequency vs. Various Clock Amplitude in Differential Voltages, A_{IN} = −9 dBFS

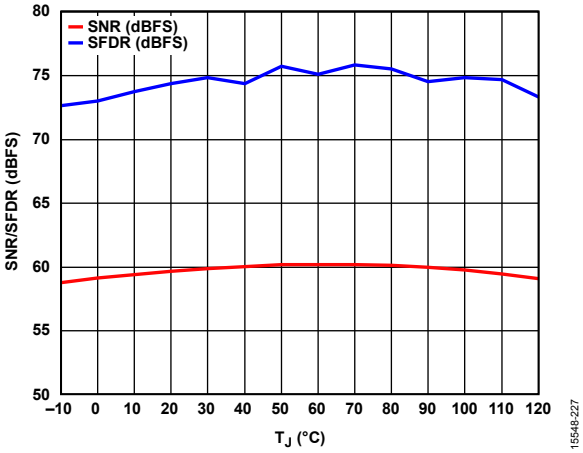

Figure 25. SNR/SFDR vs. Junction Temperature, f_{IN} = 950 MHz, A_{IN} = −9 dBFS

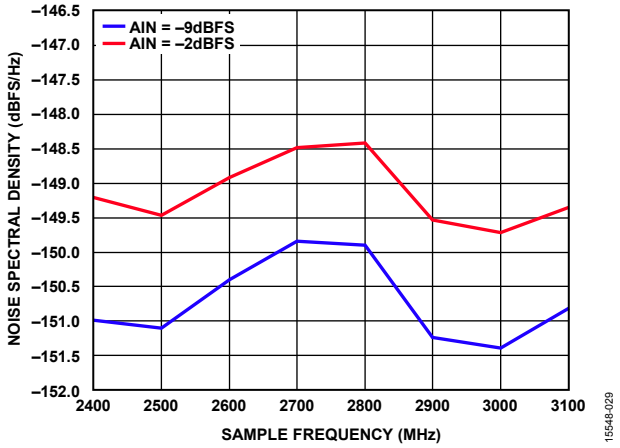

Figure 28. NSD vs. Sample Frequency (f_S)
f_{IN} = 1.8 GHz; A_{IN} = −2 dBFS

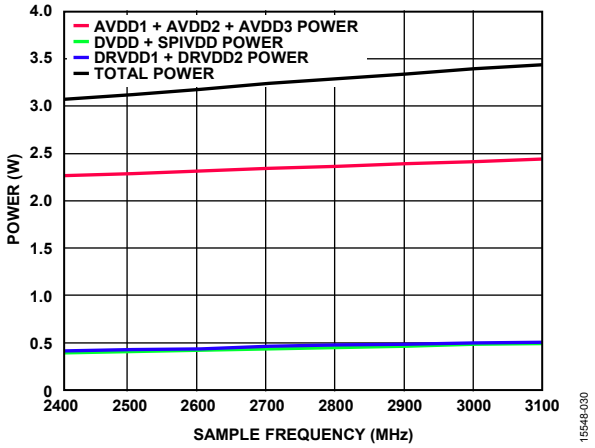

Figure 29. Power Dissipation vs. Sample Frequency (f_S)
f_{IN} = 1.8 GHz; A_{IN} = −2 dBFS

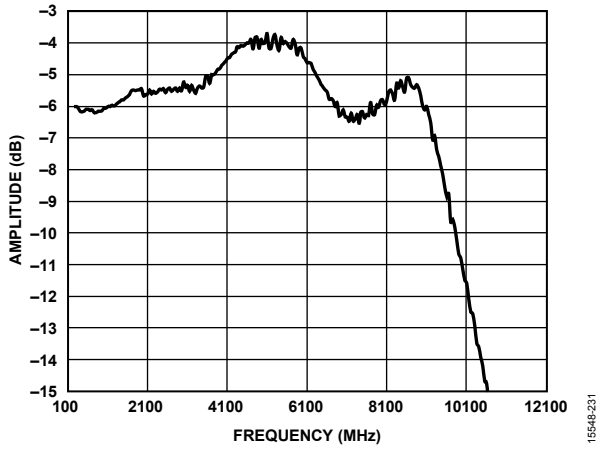

Figure 30. Input Bandwidth (see Figure 46 for Input Configuration)

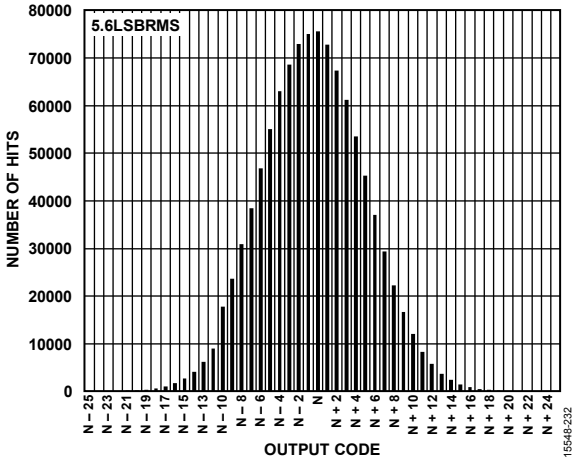

Figure 31. Input Referred Noise Histogram

EQUIVALENT CIRCUITS

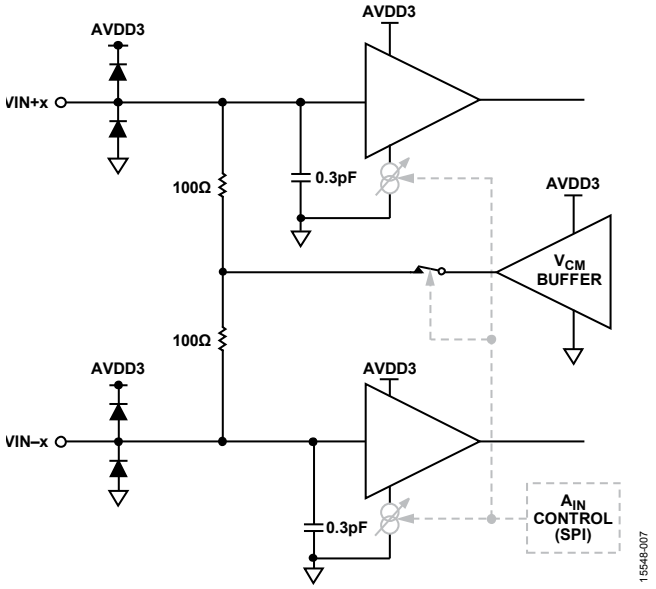

Figure 32. Analog Inputs

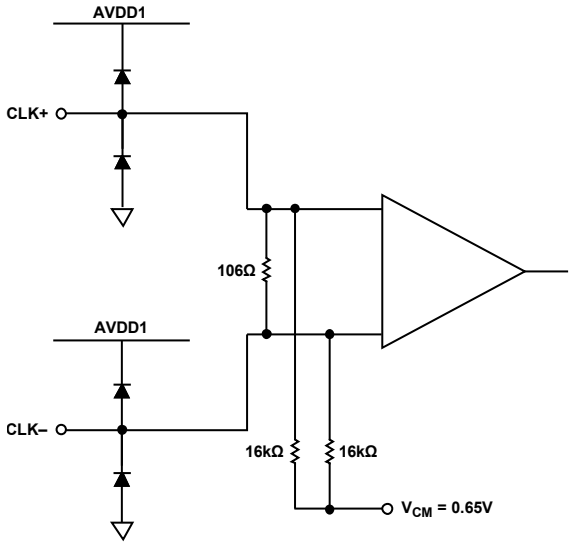

Figure 33. Clock Inputs

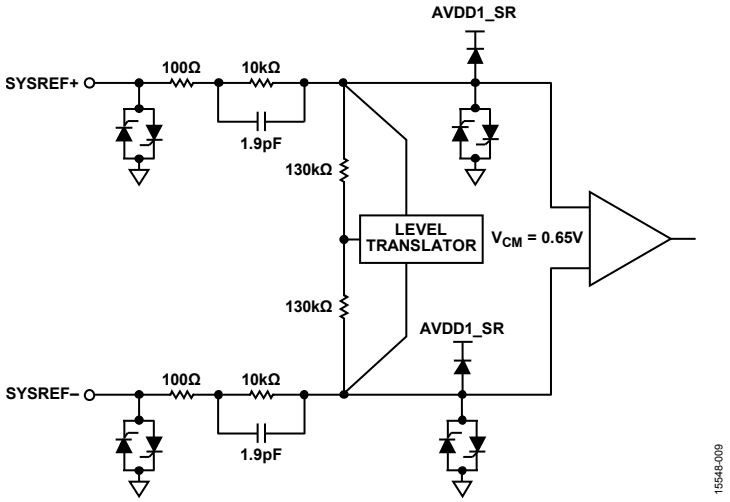

Figure 34. SYSREF± Inputs

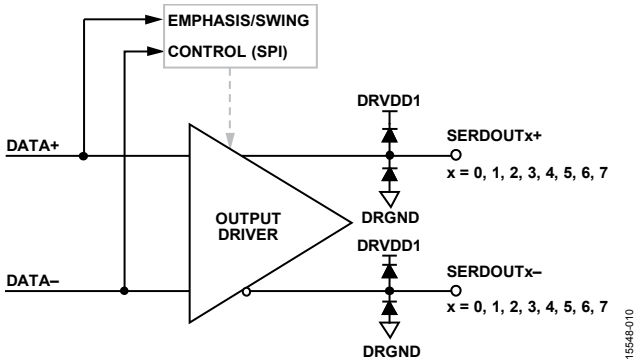

Figure 35. Digital Outputs

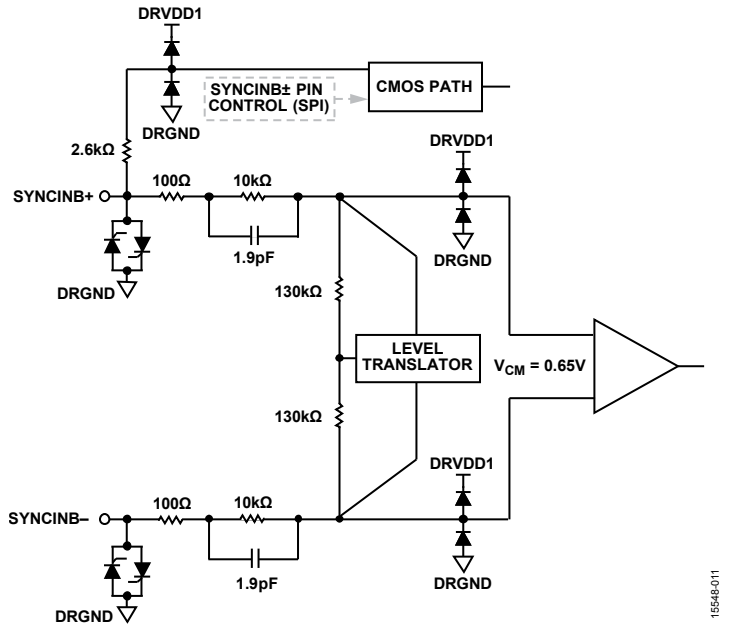

Figure 36. SYNCINB± Inputs

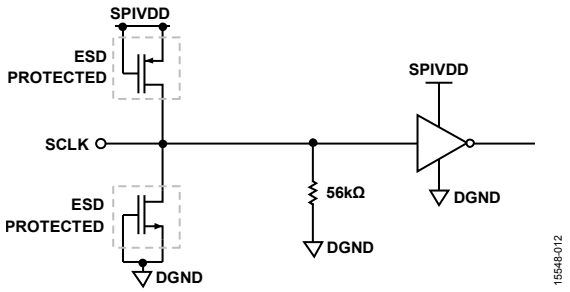

Figure 37. SCLK Input

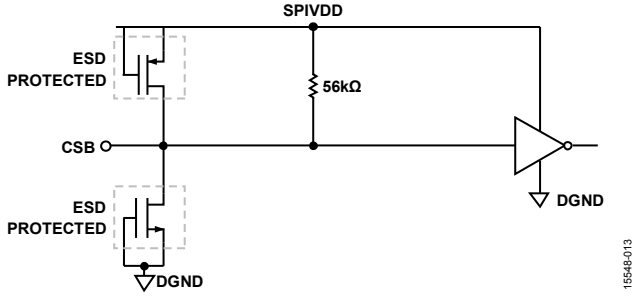

Figure 38. CSB Input

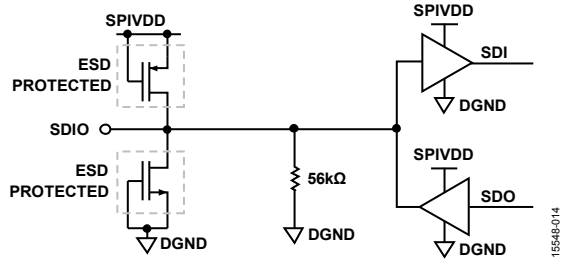

Figure 39. SDIO Input

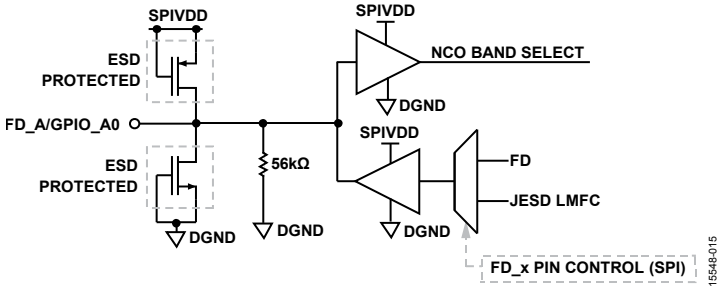

Figure 40. FD_A/GPIO_A0, FD_B/GPIO_B0, Input/Outputs

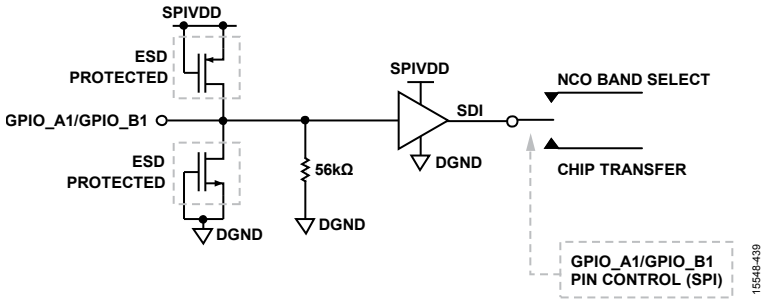

Figure 41. GPIO_A1/GPIO_B1

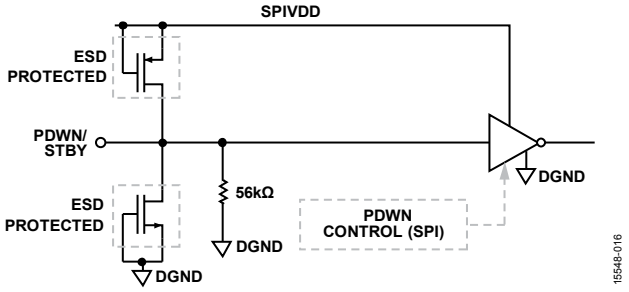

Figure 42. PDWN/STBY Input

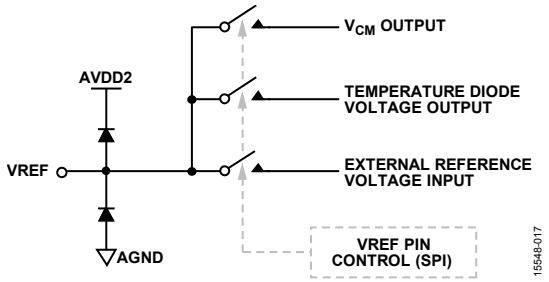

Figure 43. VREF Input/Output

THEORY OF OPERATION

The AD6688 has two analog input channels and up to eight JESD204B output lane pairs. The ADC samples wide bandwidth analog signals of up to 5 GHz. The actual 3 dB roll-off of the analog inputs is greater than 9 GHz. The AD6688 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The AD6688 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

The Subclass 1 JESD204B-based high speed serialized output data lanes can be configured in one lane (L = 1), two lane (L = 2), four lane (L = 4), and eight lane (L = 8) configurations, depending on the sample rate and the decimation ratio. Multiple device synchronization is supported through the SYSREF± and SYNCINB± input pins. The SYSREF± pin in the AD6688 can also be used as a timestamp of data as it passes through the ADC and out the JESD204B interface.

ADC ARCHITECTURE

The architecture of the AD6688 consists of an input buffered pipelined ADC. The input buffer provides a termination impedance to the analog input signal. This termination impedance is set to 200 Ω. The equivalent circuit diagram of the analog input termination is shown in Figure 32. The input buffer is optimized for high linearity, low noise, and low power across a wide bandwidth.

The input buffer provides a linear high input impedance (for ease of drive) and reduces kickback from the ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample; at the same time, the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD6688 is a differential buffer. The internal common-mode voltage of the buffer is 1.35 V. The clock signal alternately switches the input circuit between sample mode and hold mode.

Either a differential capacitor or two single-ended capacitors (or a combination of both) can be placed on the inputs to provide a matching passive network. These capacitors ultimately create a low-pass filter that limits unwanted broadband noise. For more information, refer to the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005). In general, the precise front-end network component values depend on the application.

Figure 44 shows the differential input return loss curve for the analog inputs across a frequency range of 100 MHz to 10 GHz. The reference impedance is 100 Ω.

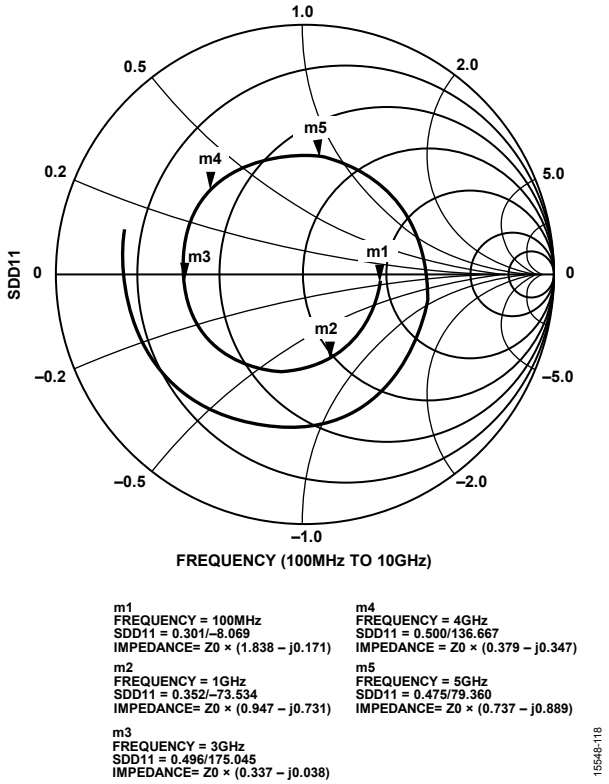

Figure 44. Differential Input Return Loss

For best dynamic performance, the source impedances driving VIN+x and VIN−x must be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. For the AD6688, the available span is programmable through the SPI port from 1.1 V p-p to 2.04 V p-p differential, with 1.7 V p-p differential being the default.