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4-Channel, Low Noise, Low Power, 24-Bit, Sigma-Delta ADC with PGA and Reference

Data Sheet **AD7124-4**

FEATURES

- 3 power modes
- RMS noise
  - Low power: 24 nV rms at 1.17 SPS, gain = 128 (255 µA typical)
  - Mid power: 20 nV rms at 2.34 SPS, gain = 128 (355 µA typical)
  - Full power: 23 nV rms at 9.4 SPS, gain = 128 (930 µA typical)
- Up to 22 noise free bits in all power modes (gain = 1)
- Output data rate
  - Full power: 9.38 SPS to 19,200 SPS
  - Mid power: 2.34 SPS to 4800 SPS
  - Low power: 1.17 SPS to 2400 SPS
- Rail-to-rail analog inputs for gains > 1
- Simultaneous 50 Hz/60 Hz rejection at 25 SPS (single cycle settling)
- Diagnostic functions (which aid safe integrity level (SIL) certification)
- Crosspoint multiplexed analog inputs
  - 4 differential/7 pseudo differential inputs
- Programmable gain (1 to 128)
- Band gap reference with 15 ppm/°C drift maximum (70 µA)
- Matched programmable excitation currents
- Internal clock oscillator
- On-chip bias voltage generator
- Low-side power switch
- General-purpose outputs
- Multiple filter options
- Internal temperature sensor
- Self and system calibration
- Sensor burnout detection
- Automatic channel sequencer
- Per channel configuration
- Power supply: 2.7 V to 3.6 V and ±1.8 V
- Independent interface power supply
- Power-down current: 5 µA maximum
- Temperature range: −40°C to +125°C
- 32-lead LFCSP/24-lead TSSOP
- 3-wire or 4-wire serial interface
  - SPI, QSPI, MICROWIRE, and DSP compatible
  - Schmitt trigger on SCLK
- ESD: 4 kV

APPLICATIONS

- Temperature measurement
- Pressure measurement
- Industrial process control
- Instrumentation
- Smart transmitters

FUNCTIONAL BLOCK DIAGRAM

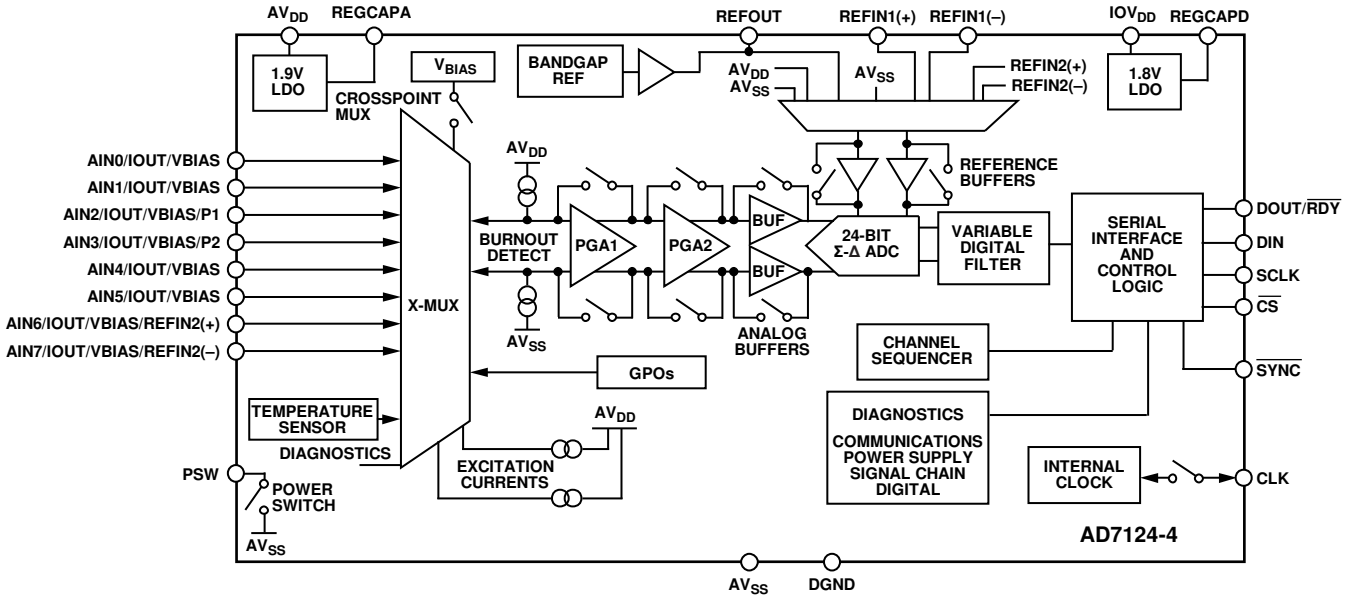

Figure 1.

Rev. C

Document Feedback

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- AD7124-4 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1392: How to Calculate Offset Errors and Input Impedance in ADC Converters with Chopped Amplifiers

Data Sheet

- AD7124-4: 4-Channel, Low Noise, Low Power, 24-Bit, Sigma-Delta ADC with PGA and Reference Data Sheet

User Guides

- UG-855: Evaluation Board for the AD7124-4 4-Channel, Low Noise, Low Power, 24-Bit, Sigma-Delta ADC with In-Amp and Reference

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD7124 No-OS Software
- AD7124-4/AD7124-8 Eval+ Software

TOOLS AND SIMULATIONS

- AD7124-4 IBIS Models

REFERENCE DESIGNS

- CN0376
- CN0381
- CN0382
- CN0383
- CN0384

REFERENCE MATERIALS

Press

- Highly Integrated Analog Front-Ends with 24-bit Converter Cores Achieve Industry's Best Combination of Low Power and Noise Performance

Technical Articles

- ADC Requirements for RTD Temperature Measurement Systems

DESIGN RESOURCES

- AD7124-4 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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5/2015—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD7124-4 is a low power, low noise, completely integrated analog front end for high precision measurement applications. The device contains a low noise, 24-bit Σ-Δ analog-to-digital converter (ADC), and can be configured to have four differential inputs or seven single-ended or pseudo differential inputs. The on-chip low gain stage ensures that signals of small amplitude can be interfaced directly to the ADC.

One of the major advantages of the AD7124-4 is that it gives the user the flexibility to employ one of three integrated power modes. The current consumption, range of output data rates, and rms noise can be tailored with the power mode selected. The device also offers a multitude of filter options, ensuring that the user has the highest degree of flexibility.

The AD7124-4 can achieve simultaneous 50 Hz and 60 Hz rejection when operating at an output data rate of 25 SPS (single cycle settling), with rejection in excess of 80 dB achieved at lower output data rates.

The AD7124-4 establishes the highest degree of signal chain integration. The device contains a precision, low noise, low drift internal band gap reference, and also accepts an external differential reference, which can be internally buffered. Other key integrated features include programmable low drift excitation current sources, burnout currents, and a bias voltage generator, which sets the common-mode voltage of a channel to $AV_{DD}/2$. The low-side power switch enables the user to power down bridge sensors between conversions, ensuring the absolute minimal power consumption of the system. The device also allows the user the option of operating with either an internal clock or an external clock.

The integrated channel sequencer allows several channels to be enabled simultaneously, and the AD7124-4 sequentially converts on each enabled channel, simplifying communication with the device. As many as 16 channels can be enabled at any time; a channel being defined as an analog input or a diagnostic such as a power supply check or a reference check. This unique feature allows diagnostics to be interleaved with conversions. The AD7124-4 also supports per channel configuration. The device allows eight configurations or setups. Each configuration consists of gain, filter type, output data rate, buffering, and reference source. The user can assign any of these setups on a channel by channel basis.

The AD7124-4 also has extensive diagnostic functionality integrated as part of its comprehensive feature set. These diagnostics include a cyclic redundancy check (CRC), signal chain checks, and serial interface checks, which lead to a more robust solution. These diagnostics reduce the need for external components to implement diagnostics, resulting in reduced board space needs, reduced design cycle times, and cost savings. The failure modes effects and diagnostic analysis (FMEDA) of a typical application has shown a safe failure fraction (SFF) greater than 90% according to IEC 61508.

The device operates with a single analog power supply from 2.7 V to 3.6 V or a dual 1.8 V power supply. The digital supply has a range of 1.65 V to 3.6 V. It is specified for a temperature range of −40°C to +125°C. The AD7124-4 is housed in a 32-lead LFCSP package and a 24-lead TSSOP package.

Note that, throughout this data sheet, multifunction pins, such as DOUT/$\overline{\text{RDY}}$, are referred to either by the entire pin name or by a single function of the pin, for example, $\overline{\text{RDY}}$, when only that function is relevant.

Table 1. AD7124-4 Overview

Parameter	Low Power Mode	Mid Power Mode	Full Power Mode
Maximum Output Data Rate	2400 SPS	4800 SPS	19,200 SPS
RMS Noise (Gain = 128)	24 nV	20 nV	23 nV
Peak-to-Peak Resolution at 1200 SPS (Gain = 1)	16.4 bits	17.1 bits	18 bits
Typical Current (ADC + PGA)	255 µA	355 µA	930 µA

SPECIFICATIONS

AV_{DD} = 2.9 V to 3.6 V (full power mode), 2.7 V to 3.6 V (mid and low power mode), IOV_{DD} = 1.65 V to 3.6 V, AV_{SS} = DGND = 0 V, REFINx(+) = 2.5 V, REFINx(−) = AV_{SS}, master clock = 614.4 kHz, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
ADC					
Output Data Rate, f_{ADC}					
Low Power Mode	1.17		2400	SPS	
Mid Power Mode	2.34		4800	SPS	
Full Power Mode	9.38		19,200	SPS	
No Missing Codes[2]	24			Bits	FS[3] > 2, sinc[4] filter
	24			Bits	FS[3] > 8, sinc[3] filter
Resolution					See the RMS Noise and Resolution section
RMS Noise and Update Rates					See the RMS Noise and Resolution section
Integral Nonlinearity (INL)	−4	±1	+4	ppm of FSR	Gain = 1[2]
	−15	±2	+15	ppm of FSR	Gain > 1[4]
Offset Error[5]					
Before Calibration		±15		µV	Gain = 1 to 8
		200/gain		µV	Gain = 16 to 128
After Internal Calibration/System Calibration		In order of noise			
Offset Error Drift vs. Temperature[6]					
Low Power Mode		10		nV/°C	Gain = 1 or gain > 16
		80		nV/°C	Gain = 2 to 8
		40		nV/°C	Gain = 16
Mid Power Mode		10		nV/°C	Gain = 1 or gain > 16
		40		nV/°C	Gain = 2 to 8
		20		nV/°C	Gain = 16
Full Power Mode		10		nV/°C	
Gain Error[5, 7]					
Before Internal Calibration	−0.0025		+0.0025	%	Gain = 1, T_A = 25°C
		−0.3		%	Gain > 1
After Internal Calibration	−0.016	+0.004	+0.016	%	Gain = 2 to 8, T_A = 25°C
		±0.025		%	Gain = 16 to 128
After System Calibration		In order of noise			
Gain Error Drift vs. Temperature		1	2	ppm/°C	
Power Supply Rejection					A_{IN} = 1 V/gain, external reference
Low Power Mode	87			dB	Gain = 2 to 16
	96			dB	Gain = 1 or gain > 16
Mid Power Mode[2]	92			dB	Gain = 2 to 16
	100			dB	Gain = 1 or gain > 16
Full Power Mode	99			dB	
Common-Mode Rejection[8]					
At DC[2]	85	90		dB	A_{IN} = 1 V, gain = 1
	105	115		dB	A_{IN} = 1 V/gain, gain 2 or 4
	102[9, 2]			dB	A_{IN} = 1 V/gain, gain 2 or 4
	115	120		dB	A_{IN} = 1 V/gain, gain ≥ 8
	105[9, 2]			dB	A_{IN} = 1 V/gain, gain ≥ 8
Sinc[3], Sinc[4] Filter[2]					
At 50 Hz, 60 Hz	120			dB	10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
At 50 Hz	120			dB	50 SPS, 50 Hz ± 1 Hz
At 60 Hz	120			dB	60 SPS, 60 Hz ± 1 Hz

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Fast Settling Filters[2]					
At 50 Hz	115			dB	First notch at 50 Hz, 50 Hz ± 1 Hz
At 60 Hz	115			dB	First notch at 60 Hz, 60 Hz ± 1 Hz
Post Filters[2]					
At 50 Hz, 60 Hz	130			dB	20 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	130			dB	25 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
Normal Mode Rejection[2]					
Sinc[4] Filter					
External Clock					
At 50 Hz, 60 Hz	120			dB	10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	80			dB	50 SPS, REJ60[10]=1, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
At 50 Hz	120			dB	50 SPS, 50 Hz ± 1 Hz
At 60 Hz	120			dB	60 SPS, 60 Hz ± 1 Hz
Internal Clock					
At 50 Hz, 60 Hz	98			dB	10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	66			dB	50 SPS, REJ60[10] = 1, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
At 50 Hz	92			dB	50 SPS, 50 Hz ± 1 Hz
At 60 Hz	92			dB	60 SPS, 60 Hz ± 1 Hz
Sinc[3] Filter					
External Clock					
At 50 Hz, 60 Hz	100			dB	10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	65			dB	50 SPS, REJ60[10] = 1, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
At 50 Hz	100			dB	50 SPS, 50 Hz ± 1 Hz
At 60 Hz	100			dB	60 SPS, 60 Hz ± 1 Hz
Internal Clock					
At 50 Hz, 60 Hz	73			dB	10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	52			dB	50 SPS, REJ60[10] = 1, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
At 50 Hz	68			dB	50 SPS, 50 Hz ± 1 Hz
At 60 Hz	68			dB	60 SPS, 60 Hz ± 1 Hz
Fast Settling Filters					
External Clock					
At 50 Hz	40			dB	First notch at 50 Hz, 50 Hz ± 0.5 Hz
At 60 Hz	40			dB	First notch at 60 Hz, 60 Hz ± 0.5 Hz
Internal Clock					
At 50 Hz	24.5			dB	First notch at 50 Hz, 50 Hz ± 0.5 Hz
At 60 Hz	24.5			dB	First notch at 60 Hz, 60 Hz ± 0.5 Hz
Post Filters					
External Clock					
At 50 Hz, 60 Hz	86			dB	20 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	62			dB	25 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
Internal Clock					
At 50 Hz, 60 Hz	67			dB	20 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	50			dB	25 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
ANALOG INPUTS[11]					
Differential Input Voltage Ranges[12]		$\pm V_{REF}$/gain		V	V_{REF} = REFINx(+) − REFINx(−), or internal reference
Absolute A_{IN} Voltage Limits[2]					
Gain = 1 (Unbuffered)	AV_{SS} − 0.05		AV_{DD} + 0.05	V	
Gain = 1 (Buffered)	AV_{SS} + 0.1		AV_{DD} − 0.1	V	
Gain > 1	AV_{SS} − 0.05		AV_{DD} + 0.05	V	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Analog Input Current					
Gain > 1 or Gain = 1 (Buffered)					
Low Power Mode					
Absolute Input Current		±1		nA	
Differential Input Current		±0.2		nA	
Analog Input Current Drift		25		pA/°C	
Mid Power Mode					
Absolute Input Current		±1.2		nA	
Differential Input Current		±0.4		nA	
Analog Input Current Drift		25		pA/°C	
Full Power Mode					
Absolute Input Current		±3.3		nA	
Differential Input Current		±1.5		nA	
Analog Input Current Drift		25		pA/°C	
Gain = 1 (Unbuffered)					Current varies with input voltage
Absolute Input Current		±2.65		µA/V	
Analog Input Current Drift		1.1		nA/V/°C	
REFERENCE INPUT					
Internal Reference					
Initial Accuracy	2.5 − 0.2%	2.5	2.5 + 0.2%	V	T_A = 25°C
Drift		2	10	ppm/°C	TSSOP
		2	15	ppm/°C	LFCSP
Output Current			10	mA	
Load Regulation		50		µV/mA	
Power Supply Rejection		85		dB	
External Reference					
External REFIN Voltage[2]	1	2.5	AV_{DD}	V	REFIN = REFINx(+) − REFINx(−)
Absolute REFIN Voltage Limits[2]	AV_{SS} − 0.05		AV_{DD} + 0.05	V	Unbuffered
	AV_{SS} + 0.1		AV_{DD} − 0.1	V	Buffered
Reference Input Current					
Buffered					
Low Power Mode					
Absolute Input Current		±0.5		nA	
Reference Input Current Drift		10		pA/°C	
Mid Power Mode					
Absolute Input Current		±1		nA	
Reference Input Current Drift		10		pA/°C	
Full Power Mode					
Absolute Input Current		±3		nA	
Reference Input Current Drift		10		pA/°C	
Unbuffered					
Absolute Input Current		±12		µA	
Reference Input Current Drift		6		nA/°C	
Normal Mode Rejection					Same as for analog inputs
Common-Mode Rejection		100		dB	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
EXCITATION CURRENT SOURCES (IOUT0/IOUT1)					Available on any analog input pin
Output Current		50/100/250/ 500/750/1000		µA	
Initial Tolerance		±4		%	T_A = 25°C
Drift		50		ppm/°C	
Current Matching		±0.5		%	Matching between IOUT0 and IOUT1, V_{OUT} = 0 V
Drift Matching[2]		5	30	ppm/°C	
Line Regulation (AV_{DD})		2		%/V	AV_{DD} = 3 V ± 5%
Load Regulation		0.2		%/V	
Output Compliance[2]	AV_{SS} − 0.05		AV_{DD} − 0.37	V	50 µA/100 µA/250 µA/500 µA current sources, 2% accuracy
	AV_{SS} − 0.05		AV_{DD} − 0.48	V	750 µA and 1000 µA current sources, 2% accuracy
BIAS VOLTAGE (V_{BIAS}) GENERATOR					Available on any analog input pin
V_{BIAS}		AV_{SS} + (AV_{DD} − AV_{SS})/2		V	
V_{BIAS} Generator Start-Up Time		6.7		µs/nF	Dependent on the capacitance connected to AINx
TEMPERATURE SENSOR					
Accuracy		±0.5		°C	
Sensitivity		13,584		Codes/°C	
LOW-SIDE POWER SWITCH					
On Resistance (R_{ON})		7	10	Ω	
Allowable Current[2]			30	mA	Continuous current
BURNOUT CURRENTS					
A_{IN} Current		0.5/2/4		µA	Analog inputs must be buffered
DIGITAL OUTPUTS (P1 AND P2)					
Output Voltage					
High, V_{OH}	AV_{DD} − 0.6			V	I_{SOURCE} = 100 µA
Low, V_{OL}			0.4	V	I_{SINK} = 100 µA
DIAGNOSTICS					
Power Supply Monitor Detect Level					
Analog Low Dropout Regulator (ALDO)			1.6	V	AV_{DD} − AV_{SS} ≥ 2.7 V
Digital LDO (DLDO)			1.55	V	IOV_{DD} ≥ 1.75 V
Reference Detect Level	0.7		1	V	REF_DET_ERR bit active if V_{REF} < 0.7 V
AINM/AINP Overvoltage Detect Level	AV_{DD} + 0.04			V	
AINM/AINP Undervoltage Detect Level			AV_{SS} − 0.04	V	
INTERNAL/EXTERNAL CLOCK					
Internal Clock					
Frequency	614.4 − 5%	614.4	614.4 + 5%	kHz	
Duty Cycle		50:50		%	
External Clock					
Frequency		2.4576		MHz	Internal divide by 4
Duty Cycle Range		45:55 to 55:45		%	
LOGIC INPUTS[2]					
Input Voltage					
Low, V_{INL}			0.3 × IOV_{DD}	V	1.65 V ≤ IOV_{DD} < 1.9 V
			0.35 × IOV_{DD}	V	1.9 V ≤ IOV_{DD} < 2.3 V
			0.7	V	2.3 V ≤ IOV_{DD} ≤ 3.6 V
High, V_{INH}	0.7 × IOV_{DD}			V	1.65 V ≤ IOV_{DD} < 1.9 V
	0.65 × IOV_{DD}			V	1.9 V ≤ IOV_{DD} < 2.3 V
	1.7			V	2.3 V ≤ IOV_{DD} < 2.7 V
	2			V	2.7 V ≤ IOV_{DD} ≤ 3.6 V
Hysteresis	0.2		0.6	V	1.65 V ≤ IOV_{DD} ≤ 3.6 V
Input Currents	−1		+1	µA	V_{IN} = IOV_{DD} or GND
Input Capacitance		10		pF	All digital inputs

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (INCLUDING CLK)					
Output Voltage[2]					
High, V_{OH}	IOV_{DD} − 0.35			V	I_{SOURCE} = 100 µA
Low, V_{OL}			0.4	V	I_{SINK} = 100 µA
Floating State Leakage Current	−1		+1	µA	
Floating State Output Capacitance		10		pF	
Data Output Coding		Offset binary			
SYSTEM CALIBRATION[2]					
Calibration Limit					
Full Scale (FS)			1.05 × FS	V	
Zero Scale	−1.05 × FS			V	
Input Span	0.8 × FS		2.1 × FS	V	
POWER SUPPLY VOLTAGES FOR ALL POWER MODES					
AV_{DD} to AV_{SS}					
Low Power Mode	2.7		3.6	V	
Mid Power Mode	2.7		3.6	V	
Full Power Mode	2.9		3.6	V	
IOV_{DD} to GND	1.65		3.6	V	
AV_{SS} to GND	−1.8		0	V	
IOV_{DD} to AV_{SS}			5.4	V	
POWER SUPPLY CURRENTS[11, 13]					
I_{AVDD}, External Reference					
Low Power Mode					
Gain = 1[2]		125	140	µA	All buffers off
Gain = 1 I_{AVDD} Increase per AINx Buffer[2]		15	25	µA	
Gain = 2 to 8		205	250	µA	
Gain = 16 to 128		235	300	µA	
I_{AVDD} Increase per Reference Buffer[2]		10	20	µA	All gains
Mid Power Mode					
Gain = 1[2]		150	170	µA	All buffers off
Gain = 1 I_{AVDD} Increase per AINx Buffer[2]		30	40	µA	
Gain = 2 to 8		275	345	µA	
Gain = 16 to 128		330	430	µA	
I_{AVDD} Increase per Reference Buffer[2]		20	30	µA	All gains
Full Power Mode					
Gain = 1[2]		315	350	µA	All buffers off
Gain = 1 I_{AVDD} Increase per AINx Buffer[2]		90	135	µA	
Gain = 2 to 8		660	830	µA	
Gain = 16 to 128		875	1200	µA	
I_{AVDD} Increase per Reference Buffer[2]		85	120	µA	All gains
I_{AVDD} Increase					
Due to Internal Reference[2]		50	70	µA	Independent of power mode; the reference buffers are not required when using this reference
Due to V_{BIAS}[2]		15	20	µA	Independent of power mode
Due to Diagnostics[2]		4	5	µA	
I_{IOVDD}					
Low Power Mode		20	35	µA	
Mid Power Mode		25	40	µA	
Full Power Mode		55	80	µA	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
POWER-DOWN CURRENTS[13]					Independent of power mode
Standby Current					
I_{AVDD}		7	15	μA	LDOs on only
I_{IOVDD}		8	20	μA	
Power-Down Current					
I_{AVDD}		1	3	μA	
I_{IOVDD}		1	2	μA	

[1] Temperature range = −40°C to +125°C.
[2] These specifications are not production tested but are supported by characterization data at the initial product release.
[3] FS is the decimal equivalent of the FS[10:0] bits in the filter registers.
[4] The integral nonlinearity is production tested in full power mode only. For other power modes, the specification is supported by characterization data at the initial product release.
[5] Following a system or internal zero-scale calibration, the offset error is in the order of the noise for the programmed gain and output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed gain and output data rate.
[6] Recalibration at any temperature removes these errors.
[7] Gain error applies to both positive and negative full-scale. A factory calibration is performed at gain = 1, T_A = 25°C.
[8] When gain > 1, the common-mode voltage is between (AV_{SS} + 0.1 + 0.5/gain) and (AV_{DD} − 0.1 − 0.5/gain).
[9] Specification is for a wider common-mode voltage between (AV_{SS} − 0.05 + 0.5/gain) and (AV_{DD} − 0.1 − 0.5/gain).
[10] REJ60 is a bit in the filter registers. When the first notch of the sinc filter is at 50 Hz, a notch is placed at 60 Hz when REJ60 is set to 1. This gives simultaneous 50 Hz and 60 Hz rejection.
[11] When the gain is greater than 1, the analog input buffers are enabled automatically. The buffers can only be disabled when the gain equals 1.
[12] When V_{REF} = (AV_{DD} − AV_{SS}), the typical differential input equals 0.92 × V_{REF}/gain for the low and mid power modes and 0.86 × V_{REF}/gain for full power mode.
[13] The digital inputs are equal to IOV_{DD} or DGND with excitation currents and bias voltage generator disabled.

TIMING CHARACTERISTICS

AV_{DD} = 2.9 V to 3.6 V (full power mode), 2.7 V to 3.6 V (mid and low power mode), IOV_{DD} = 1.65 V to 3.6 V, AV_{SS} = DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = IOV_{DD}, unless otherwise noted.

Table 3.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
t_3	100			ns	SCLK high pulse width
t_4	100			ns	SCLK low pulse width
t_{12}					Delay between consecutive read/write operations
	3/MCLK[3]			ns	Full power mode
	12/MCLK			ns	Mid power mode
	24/MCLK			ns	Low power mode
t_{13}				μs	DOUT/$\overline{RDY}$ high time if DOUT/$\overline{RDY}$ is low and the next conversion is available
		6		μs	Full power mode
		25		μs	Mid power mode
		50		μs	Low power mode
t_{14}					$\overline{SYNC}$ low pulse width
	3/MCLK			ns	Full power mode
	12/MCLK			ns	Mid power mode
	24/MCLK			ns	Low power mode
READ OPERATION					
t_1	0		80	ns	$\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time
t_2[4]	0		80	ns	SCLK active edge[5] to data valid delay
t_5[6, 7]	10		80	ns	Bus relinquish time after $\overline{CS}$ inactive edge
t_6	0			ns	SCLK inactive edge to $\overline{CS}$ inactive edge
t_7[8]					SCLK inactive edge to DOUT/$\overline{RDY}$ high
	10			ns	The DOUT_$\overline{RDY}$_DEL bit is cleared, the $\overline{CS}$_EN bit is cleared
	110			ns	The DOUT_$\overline{RDY}$_DEL bit is set, the $\overline{CS}$_EN bit is cleared
t_{7A}[7]	t_5			ns	Data valid after $\overline{CS}$ inactive edge, the $\overline{CS}$_EN bit is set

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
WRITE OPERATION					
t_8	0			ns	$\overline{CS}$ falling edge to SCLK active edge[5] setup time
t_9	30			ns	Data valid to SCLK edge setup time
t_{10}	25			ns	Data valid to SCLK edge hold time
t_{11}	0			ns	$\overline{CS}$ rising edge to SCLK edge hold time

[1] These specifications were sample tested during the initial release to ensure compliance. All input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of IOV_{DD} and timed from a voltage level of $IOV_{DD}/2$.
[2] See Figure 3, Figure 4, Figure 5, and Figure 6.
[3] MCLK is the master clock frequency.
[4] These specifications are measured with the load circuit shown in Figure 2 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[5] The SCLK active edge is the falling edge of SCLK.
[6] These specifications are derived from the measured time taken by the data output to change by 0.5 V when loaded with the circuit shown in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. The times quoted in the timing characteristics are the true bus relinquish times of the device and, therefore, are independent of external bus loading capacitances.
[7] $\overline{RDY}$ returns high after a read of the ADC. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high, although subsequent reads must not occur close to the next output update. In continuous read mode, the digital word can be read only once.
[8] When the $\overline{CS}$_EN bit is cleared, the DOUT/$\overline{RDY}$ pin changes from its DOUT function to its $\overline{RDY}$ function, following the last inactive edge of the SCLK. When $\overline{CS}$_EN is set, the DOUT pin continues to output the LSB of the data until the $\overline{CS}$ inactive edge.

Timing Diagrams

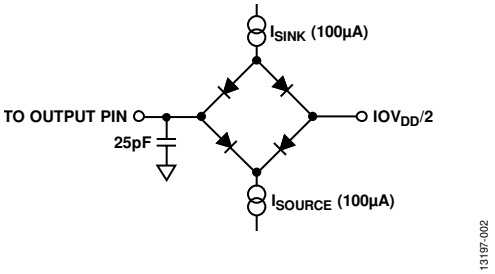

Figure 2. Load Circuit for Timing Characterization

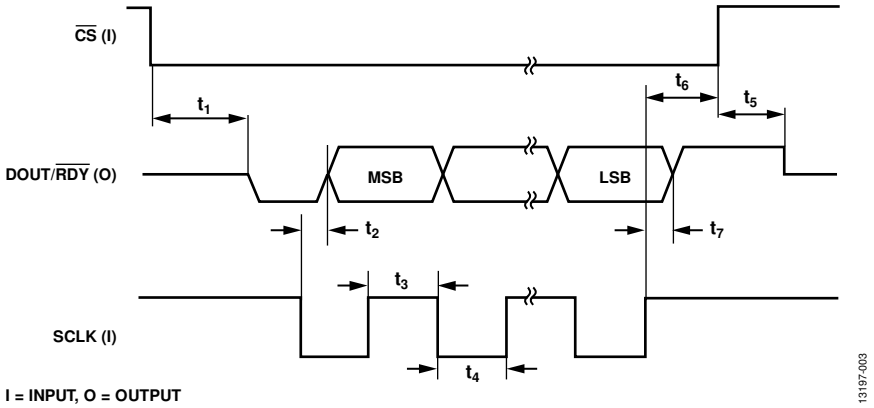

Figure 3. Read Cycle Timing Diagram ($\overline{CS}$_EN Bit Cleared)

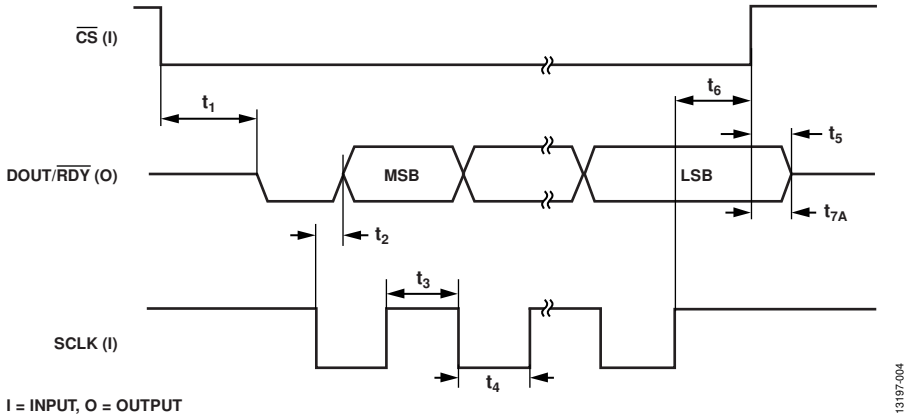

Figure 4. Read Cycle Timing Diagram (CS_EN Bit Set)

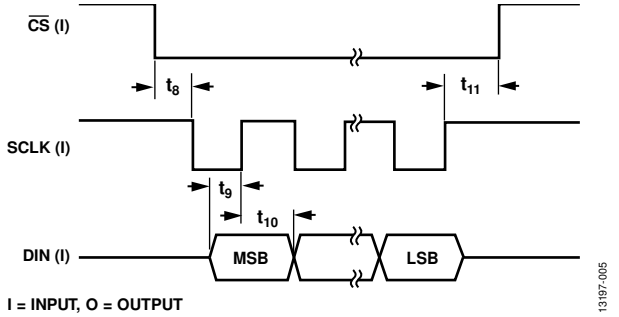

Figure 5. Write Cycle Timing Diagram

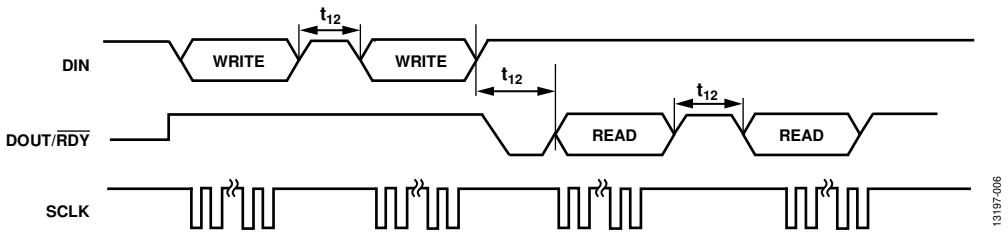

Figure 6. Delay Between Consecutive Serial Operations

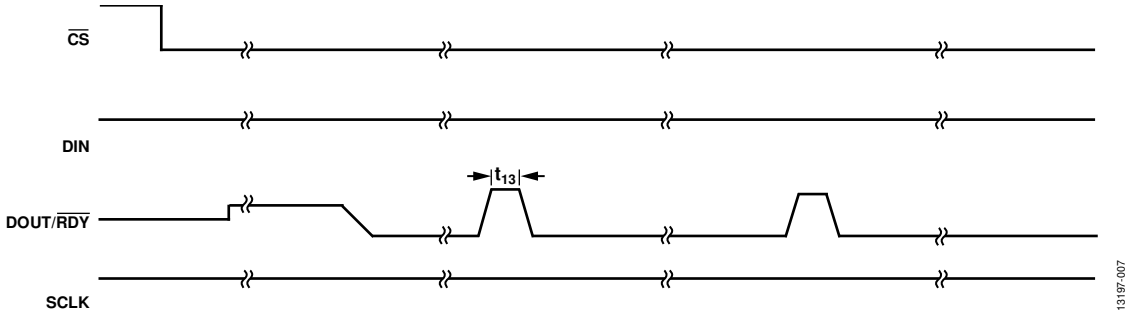

Figure 7. DOUT/RDY High Time when DOUT/RDY is Initially Low and the Next Conversion is Available

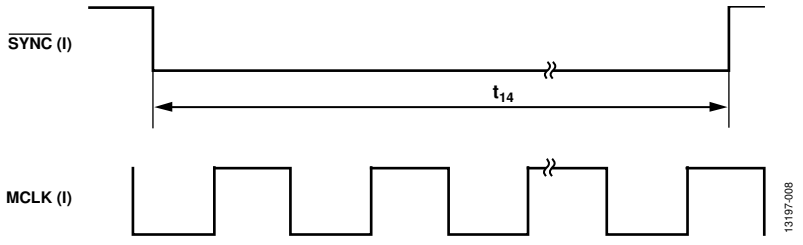

Figure 8. SYNC Pulse Width

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
AV_{DD} to AV_{SS}	−0.3 V to +3.96 V
IOV_{DD} to DGND	−0.3 V to +3.96 V
IOV_{DD} to AV_{SS}	−0.3 V to +5.94 V
AV_{SS} to DGND	−1.98 V to +0.3 V
Analog Input Voltage to AV_{SS}	−0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AV_{SS}	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to IOV_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to IOV_{DD} + 0.3 V
AINx/Digital Input Current	10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature, Soldering	
Reflow	260°C
ESD Ratings	
Human Body Model (HBM)	4 kV
Field-Induced Charged Device Model (FICDM)	1250 V
Machine Model	400 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP	32.5	32.71	°C/W
24-Lead TSSOP	128	42	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

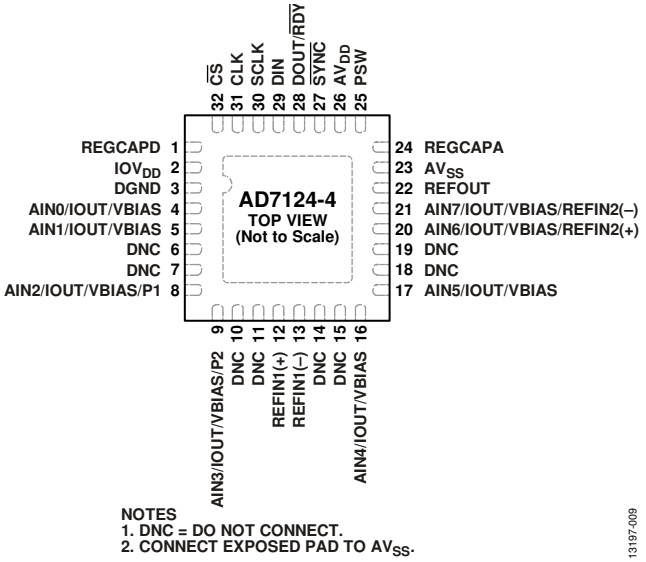

Figure 9. 32-Lead LFCSP Pin Configuration

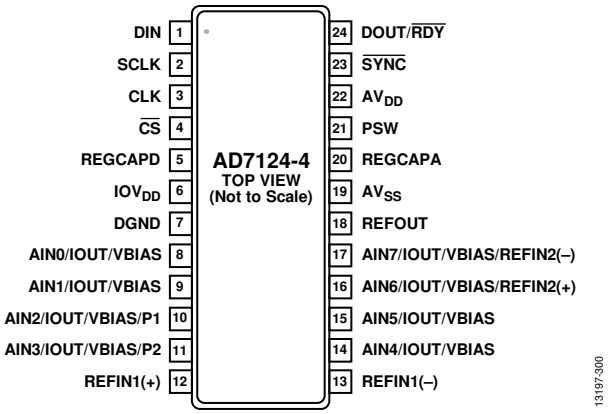

Figure 10. 24-Lead TSSOP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.			
LFCSP	**TSSOP**	**Mnemonic**	**Description**
1	5	REGCAPD	Digital LDO Regulator Output. Decouple this pin to DGND with a 0.1 µF capacitor.
2	6	IOV_{DD}	Serial Interface Supply Voltage, 1.65 V to 3.6 V. IOV_{DD} is independent of AV_{DD}. Therefore, the serial interface can operate at 1.65 V with AV_{DD} at 3.6 V, for example.
3	7	DGND	Digital Ground Reference Point.
4	8	AIN0/IOUT/VBIAS	Analog Input 0/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
5	9	AIN1/IOUT/VBIAS	Analog Input 1/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
6, 7, 10, 11, 14, 15, 18, 19	N/A[1]	DNC	Do Not Connect. Do not connect to these pins.
8	10	AIN2/IOUT/VBIAS/P1	Analog Input 2/Output of Internal Excitation Current Source/Bias Voltage/General-Purpose Output 1. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin can also be configured as a general-purpose output bit, referenced between AV_{SS} and AV_{DD}.
9	11	AIN3/IOUT/VBIAS/P2	Analog Input 3/Output of Internal Excitation Current Source/Bias Voltage/General-Purpose Output 2. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin can also be configured as a general-purpose output bit, referenced between AV_{SS} and AV_{DD}.

Pin No.			
LFCSP	TSSOP	Mnemonic	Description
12	12	REFIN1(+)	Positive Reference Input. An external reference can be applied between REFIN1(+) and REFIN1(−). REFIN1(+) can be anywhere between AV_{DD} and AV_{SS} + 1 V. The nominal reference voltage (REFIN1(+) − REFIN1(−)) is 2.5 V, but the device functions with a reference from 1 V to AV_{DD}.
13	13	REFIN1(−)	Negative Reference Input. This reference input can be anywhere between AV_{SS} and AV_{DD} − 1 V.
16	14	AIN4/IOUT/VBIAS	Analog Input 4/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
17	15	AIN5/IOUT/VBIAS	Analog Input 5/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
20	16	AIN6/IOUT/VBIAS/ REFIN2(+)	Analog Input 6/Output of Internal Excitation Current Source/Bias Voltage/Positive Reference Input. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin also functions as a positive reference input for REFIN2(±). REFIN2(+) can be anywhere between AV_{DD} and AV_{SS} + 1 V. The nominal reference voltage (REFIN2(+) to REFIN2(−)) is 2.5 V, but the device functions with a reference from 1 V to AV_{DD}.
21	17	AIN7/IOUT/VBIAS/ REFIN2(−)	Analog Input 7/Output of Internal Excitation Current Source/Bias Voltage/Negative Reference Input. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin also functions as the negative reference input for REFIN2(±). This reference input can be anywhere between AV_{SS} and AV_{DD} − 1 V.
22	18	REFOUT	Internal Reference Output. The buffered output of the internal 2.5 V voltage reference is available on this pin.
23	19	AV_{SS}	Analog Supply Voltage. The voltage on AV_{DD} is referenced to AV_{SS}. The differential between AV_{DD} and AV_{SS} must be between 2.7 V and 3.6 V in mid or low power mode and between 2.9 V and 3.6 V in full power mode. AV_{SS} can be taken below 0 V to provide a dual power supply to the AD7124-4. For example, AV_{SS} can be tied to −1.8 V and AV_{DD} can be tied to +1.8 V, providing a ±1.8 V supply to the ADC.
24	20	REGCAPA	Analog LDO Regulator Output. Decouple this pin to AV_{SS} with a 0.1 µF capacitor.
25	21	PSW	Low-Side Power Switch to AV_{SS}.
26	22	AV_{DD}	Analog Supply Voltage, Relative to AV_{SS}.
27	23	$\overline{SYNC}$	Synchronization Input. This pin is a logic input that allows synchronization of the digital filters and analog modulators when using a number of AD7124-4 devices. When $\overline{SYNC}$ is low, the nodes of the digital filter, the filter control logic, and the calibration control logic are reset, and the analog modulator is held in a reset state. $\overline{SYNC}$ does not affect the digital interface but does reset $\overline{RDY}$ to a high state if it is low.
28	24	DOUT/$\overline{RDY}$	Serial Data Output/Data Ready Output. DOUT/$\overline{RDY}$ functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/$\overline{RDY}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{RDY}$ falling edge can also be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/$\overline{RDY}$ pin. When $\overline{CS}$ is low, the data/control word information is placed on the DOUT/$\overline{RDY}$ pin on the SCLK falling edge and is valid on the SCLK rising edge.

Pin No.			
LFCSP	TSSOP	Mnemonic	Description
29	1	DIN	Serial Data Input to the Input Shift Register on the ADC. Data in the input shift register is transferred to the control registers within the ADC, with the register selection bits of the communications register identifying the appropriate register.
30	2	SCLK	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. The SCLK pin has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data.
31	3	CLK	Clock Input/Clock Output. The internal clock can be made available at this pin. Alternatively, the internal clock can be disabled, and the ADC can be driven by an external clock. This allows several ADCs to be driven from a common clock, allowing simultaneous conversions to be performed.
32	4	$\overline{CS}$	Chip Select Input. This is an active low logic input that selects the ADC. Use $\overline{CS}$ to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low if the serial peripheral interface (SPI) diagnostics are unused, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT interfacing with the device.
		EP	Exposed Pad. Connect the exposed pad to AV_{SS}.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

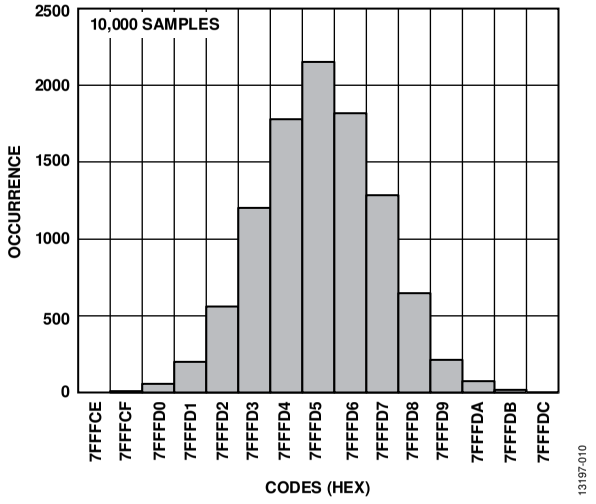

Figure 11. Noise Histogram Plot (Full Power Mode, Post Filter, Output Data Rate = 25 SPS, Gain = 1)

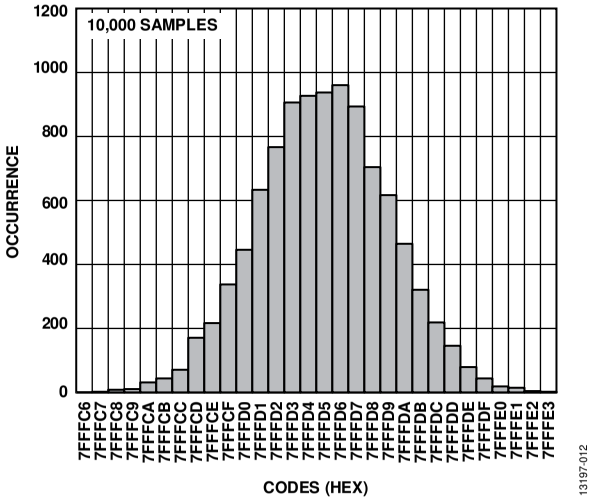

Figure 12. Noise Histogram Plot (Mid Power Mode, Post Filter, Output Data Rate = 25 SPS, Gain = 1)

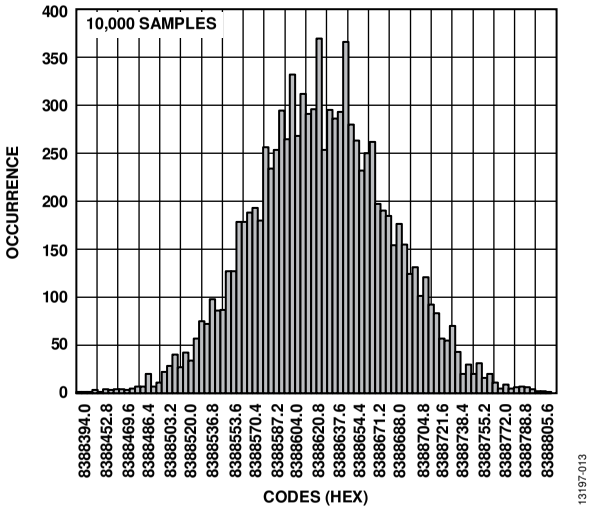

Figure 13. Noise Histogram Plot (Low Power Mode, Post Filter, Output Data Rate = 25 SPS, Gain = 1)

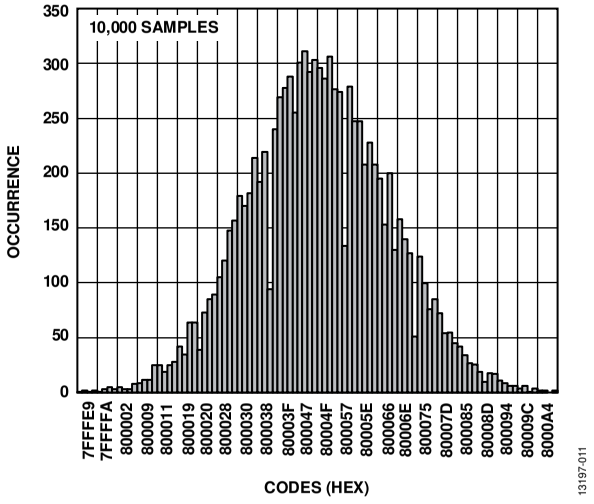

Figure 14. Noise Histogram Plot (Full Power Mode, Post Filter, Output Data Rate = 25 SPS, Gain = 128)

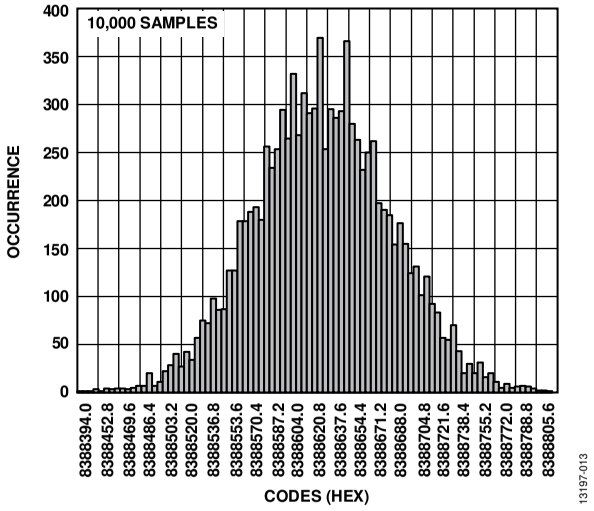

Figure 15. Noise Histogram Plot (Mid Power Mode, Post Filter, Output Data Rate = 25 SPS, Gain = 128)

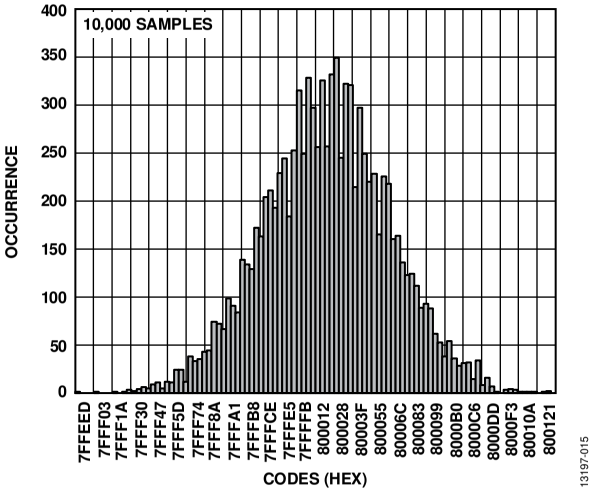

Figure 16. Noise Histogram Plot (Low Power Mode, Post Filter, Output Data Rate = 25 SPS, Gain = 128)

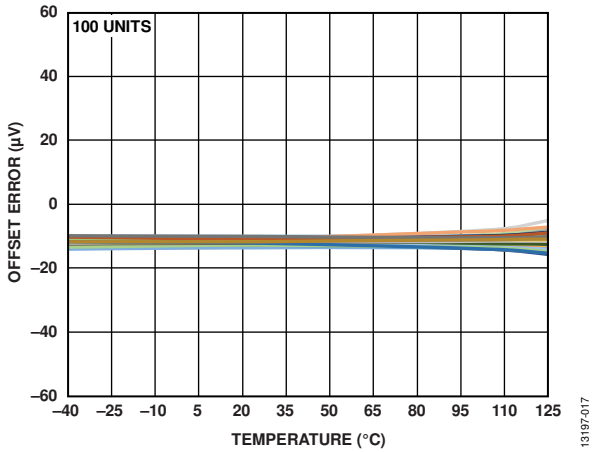

Figure 17. Input Referred Offset Error vs. Temperature (Gain = 8, Full Power Mode)

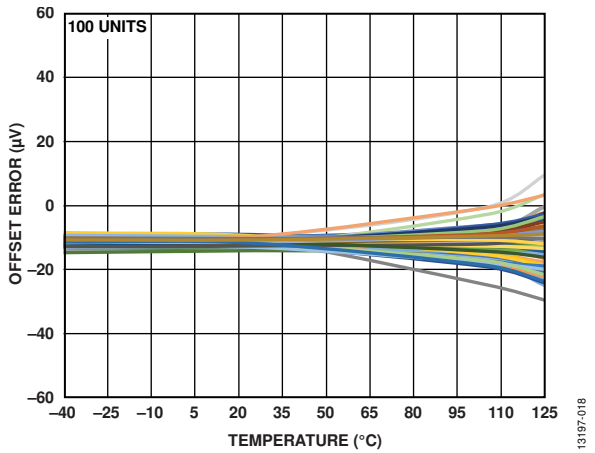

Figure 18. Input Referred Offset Error vs. Temperature (Gain = 8, Mid Power Mode)

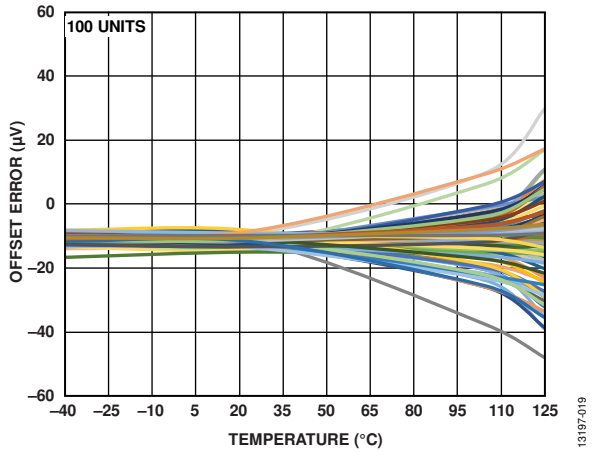

Figure 19. Input Referred Offset Error vs. Temperature (Gain = 8, Low Power Mode)

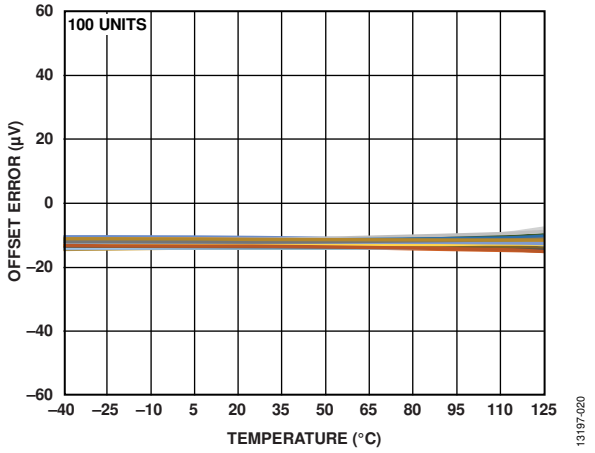

Figure 20. Input Referred Offset Error vs. Temperature (Gain = 16, Full Power Mode)

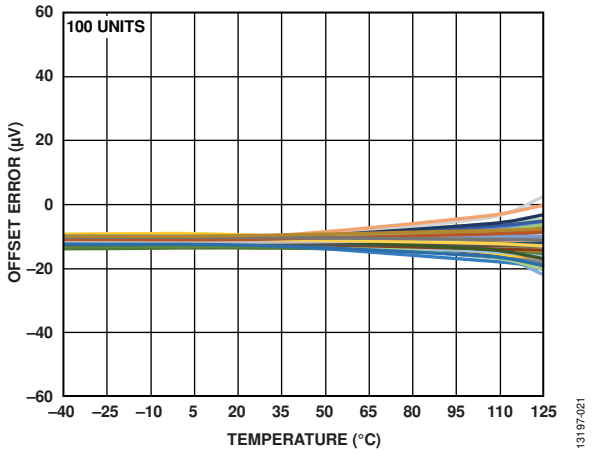

Figure 21. Input Referred Offset Error vs. Temperature (Gain = 16, Mid Power Mode)

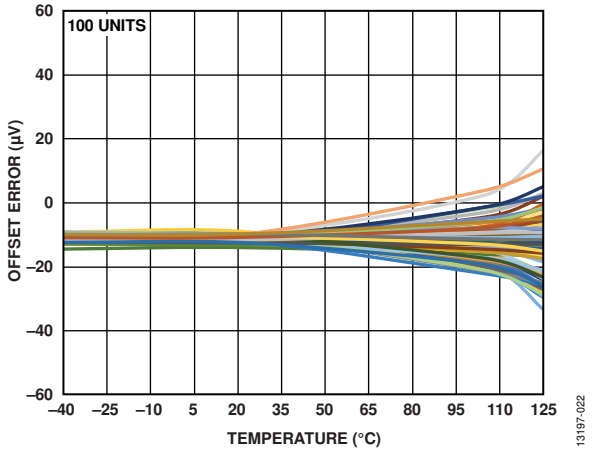

Figure 22. Input Referred Offset Error vs. Temperature (Gain = 16, Low Power Mode)

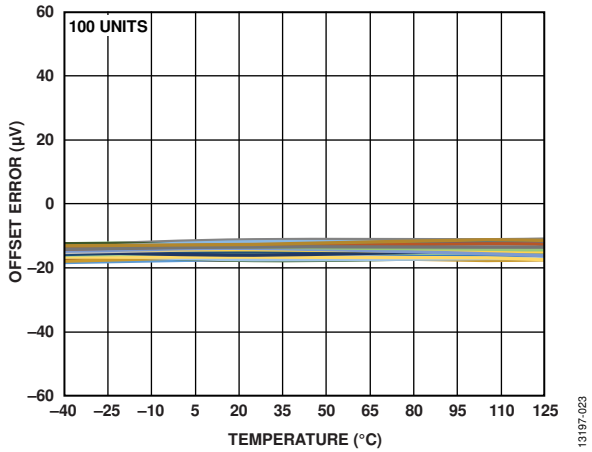

Figure 23. Input Referred Offset Error vs. Temperature (Gain = 1, Analog Input Buffers Enabled)

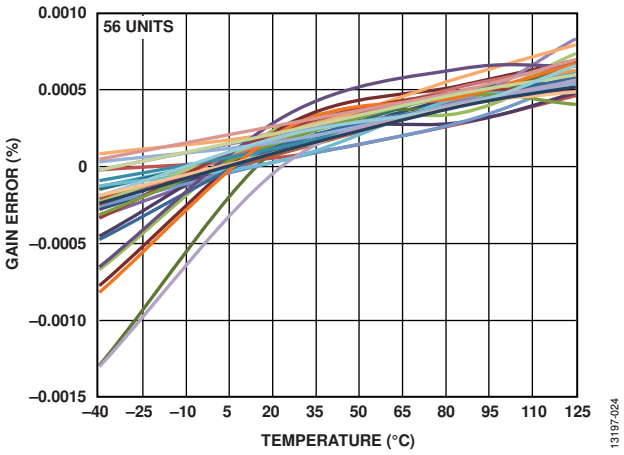

Figure 24. Input Referred Gain Error vs. Temperature (Gain = 1)

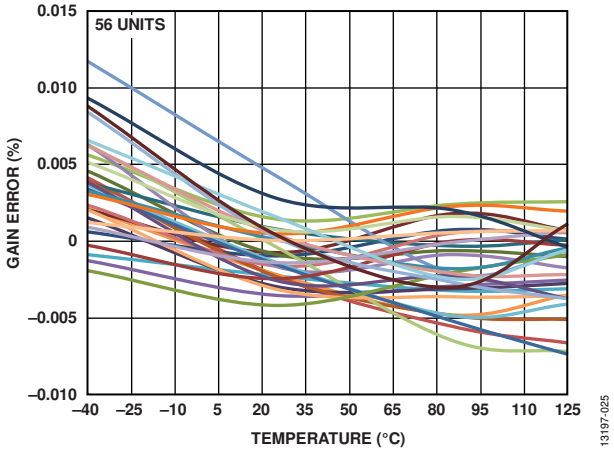

Figure 25. Input Referred Gain Error vs. Temperature (Gain = 8)

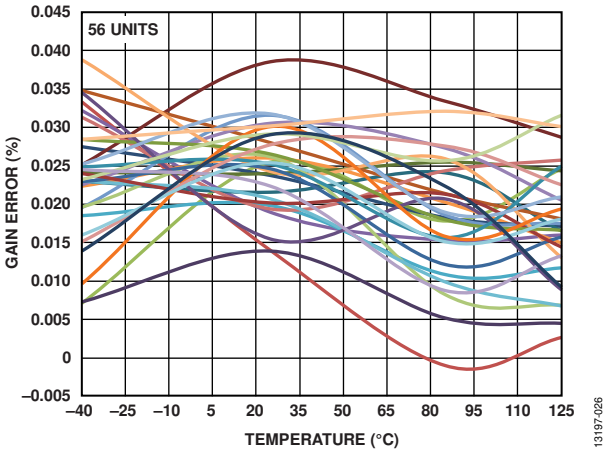

Figure 26. Input Referred Gain Error vs. Temperature (Gain = 16)

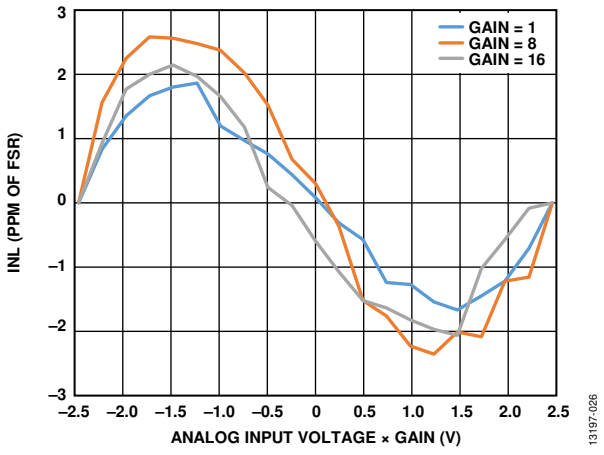

Figure 27. INL vs. Differential Input Signal (Analog Input × Gain), ODR = 50 SPS, External 2.5 V Reference

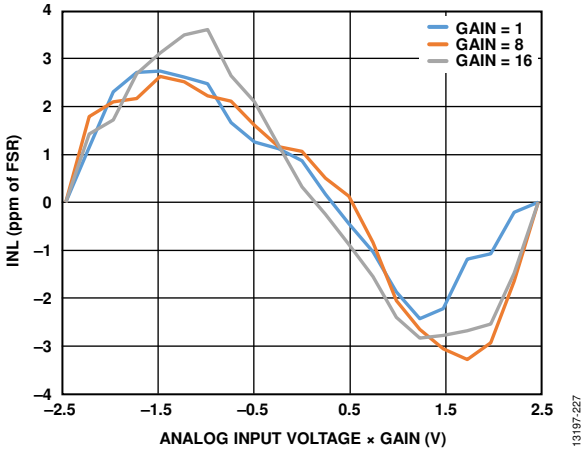

Figure 28. INL vs. Differential Input Signal (Analog Input × Gain), ODR = 50 SPS, Internal Reference

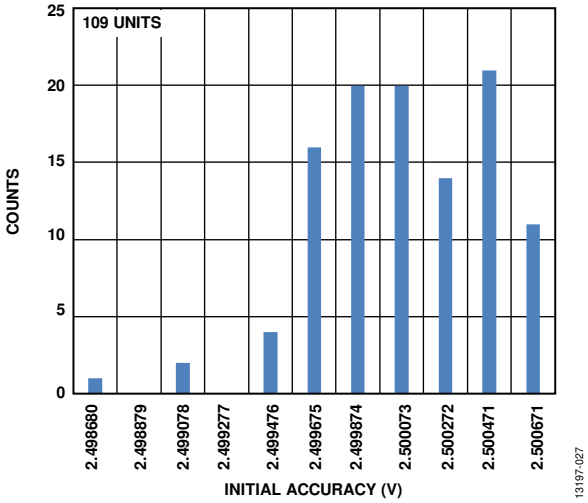

Figure 29. Internal Reference Voltage Histogram

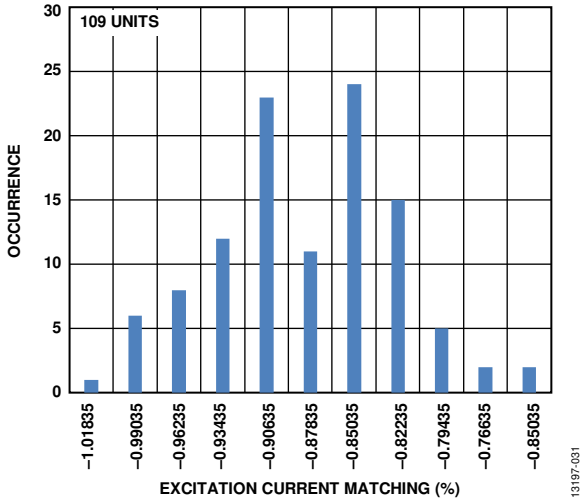

Figure 32. IOUTx Current Initial Matching Histogram (500 µA)

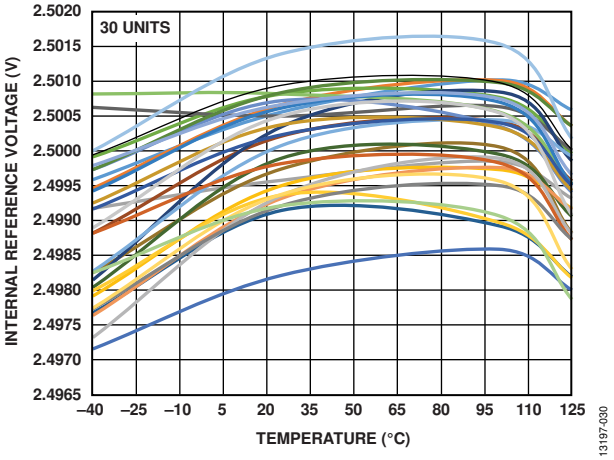

Figure 30. Internal Reference Voltage vs. Temperature

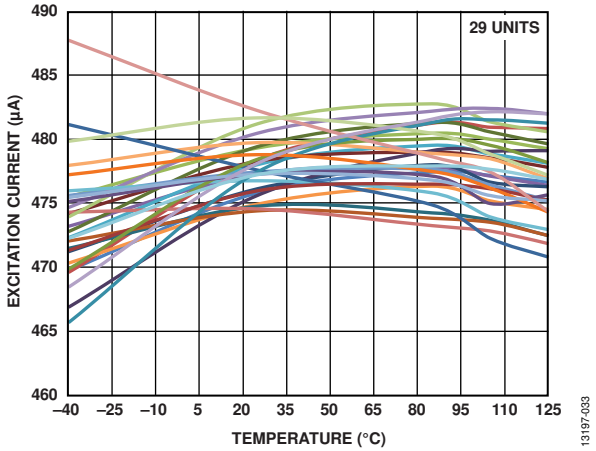

Figure 33. Excitation Current Drift (500 µA)

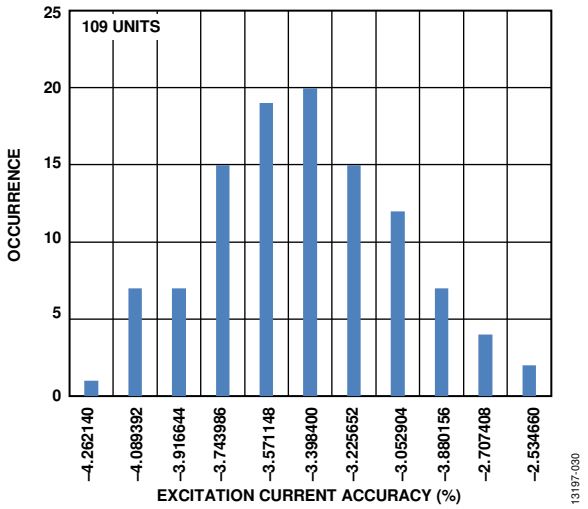

Figure 31. IOUTx Current Initial Accuracy Histogram (500 µA)

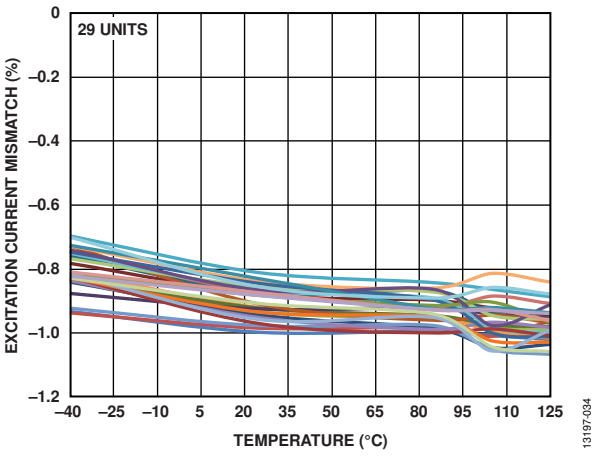

Figure 34. Excitation Current Drift Matching (500 µA)

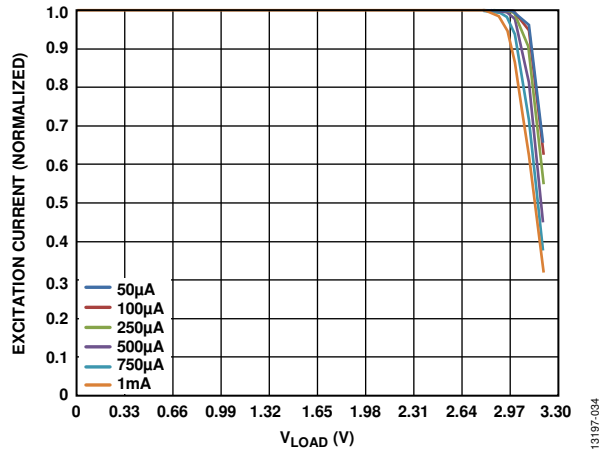

Figure 35. Output Compliance (AV_{DD} = 3.3 V)

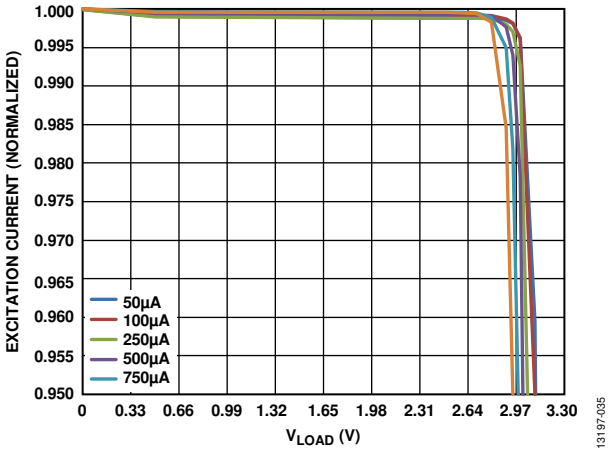

Figure 36. Output Compliance (AV_{DD} = 3.3 V)

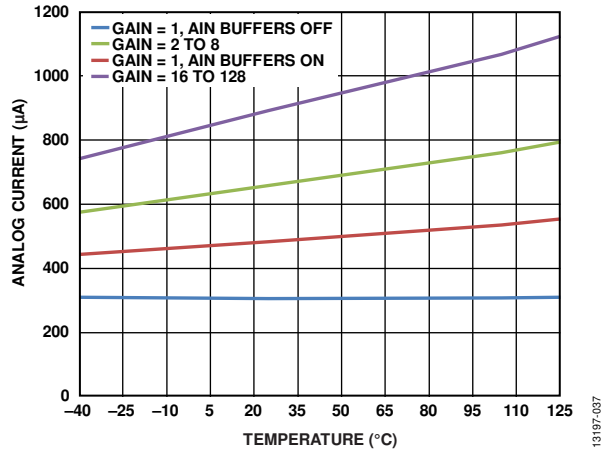

Figure 37. Analog Current vs. Temperature (Full Power Mode)

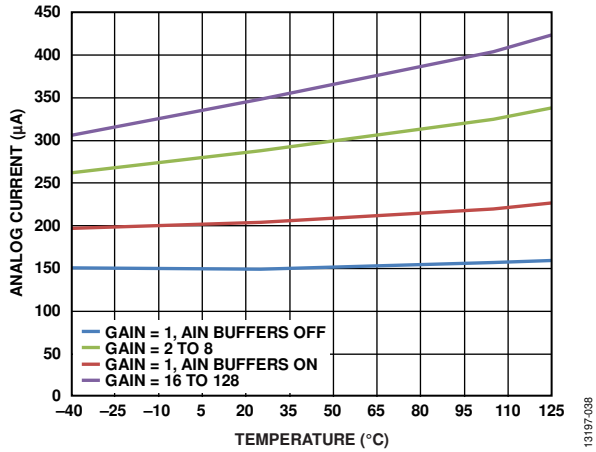

Figure 38. Analog Current vs. Temperature (Mid Power Mode)

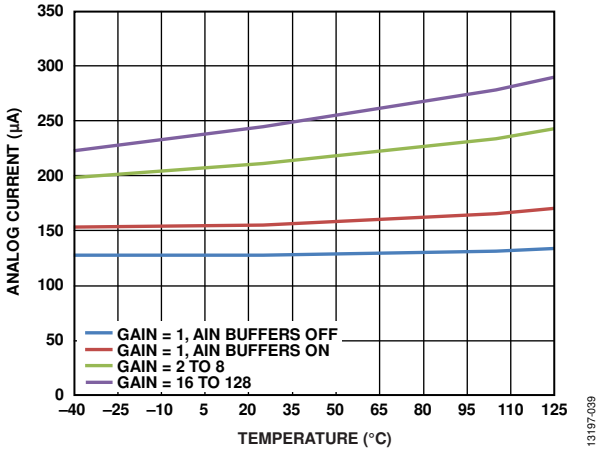

Figure 39. Analog Current vs. Temperature (Low Power Mode)

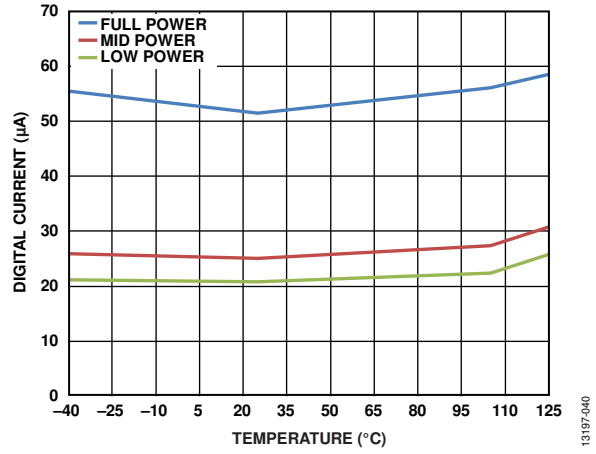

Figure 40. Digital Current vs. Temperature

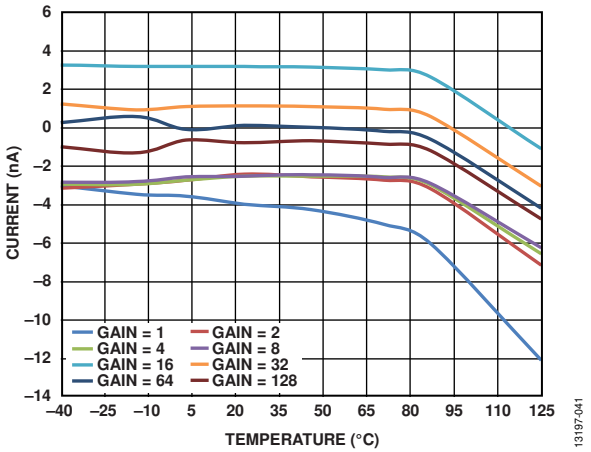

Figure 41. Absolute Analog Input Current vs. Temperature (Full Power Mode)

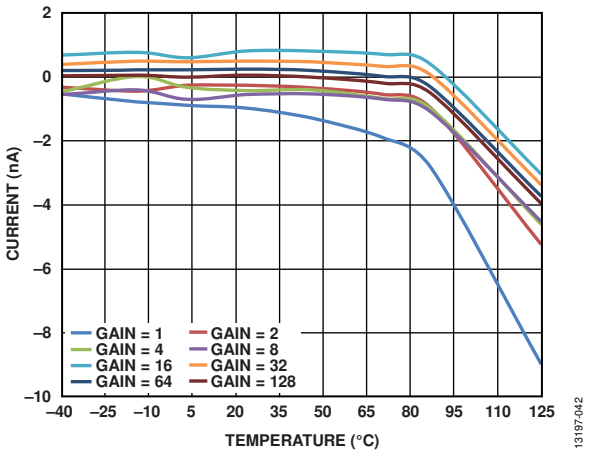

Figure 42. Absolute Analog Input Current vs. Temperature (Mid Power Mode)

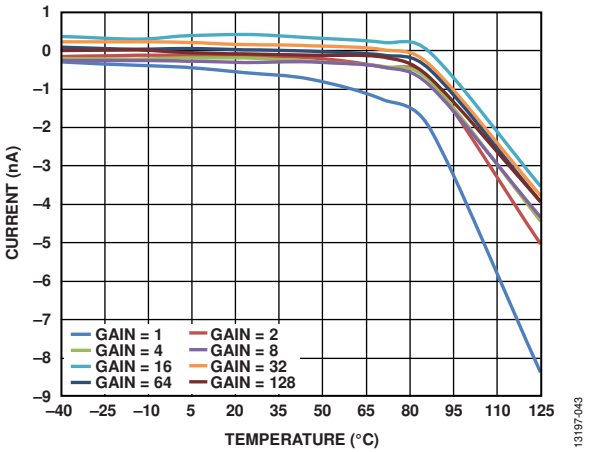

Figure 43. Absolute Analog Input Current vs. Temperature (Low Power Mode)

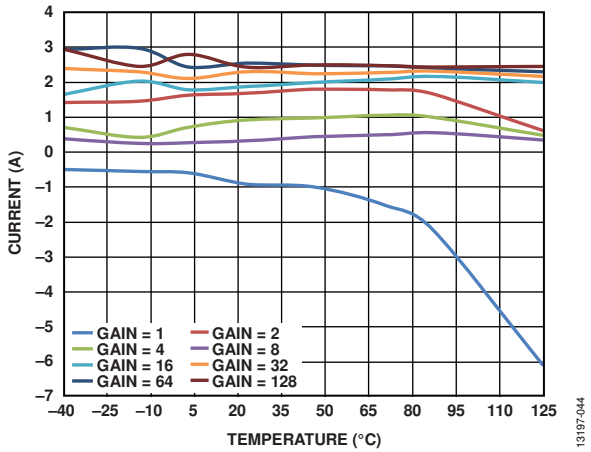

Figure 44. Differential Analog Input Current vs. Temperature (Full Power Mode)

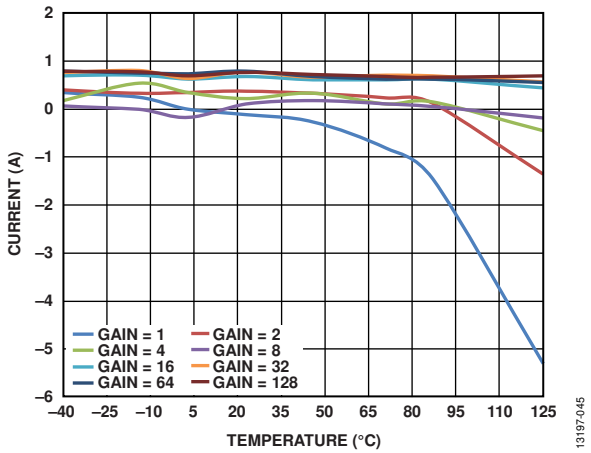

Figure 45. Differential Analog Input Current vs. Temperature (Mid Power Mode)

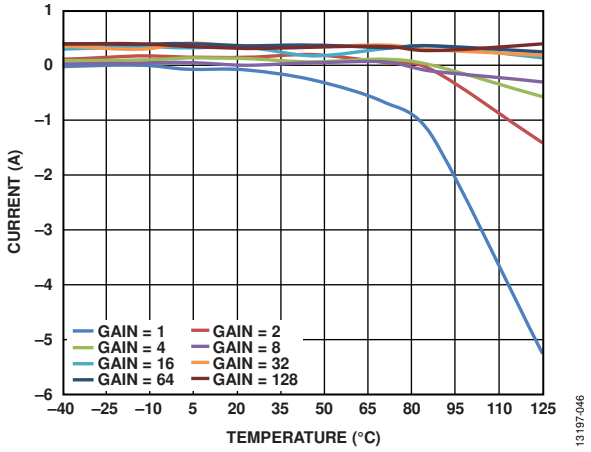

Figure 46. Differential Analog Input Current vs. Temperature (Low Power Mode)

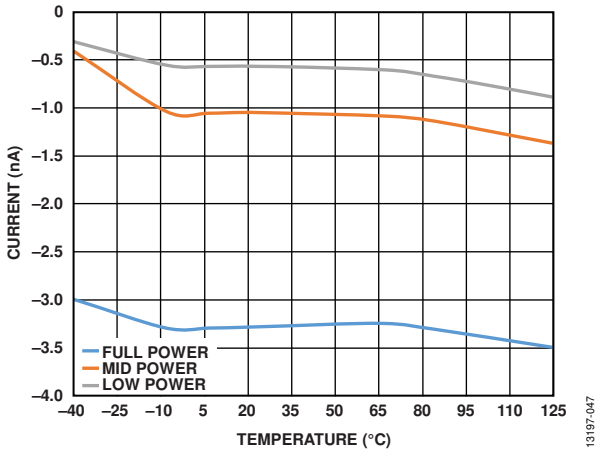

Figure 47. Reference Input Current vs. Temperature (Reference Buffers Enabled)

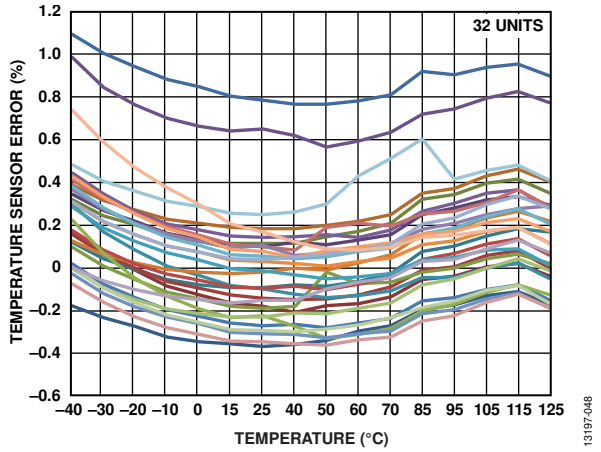

Figure 48. Temperature Sensor Accuracy

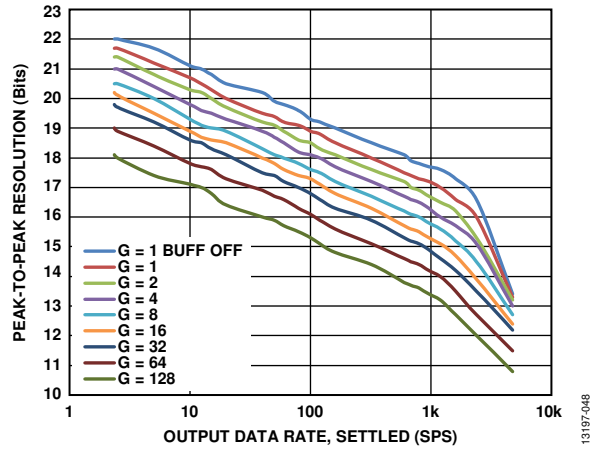

Figure 49. Peak-to-Peak Resolution vs. Output Data Rate (Settled), Sinc^4 Filter (Full Power Mode)

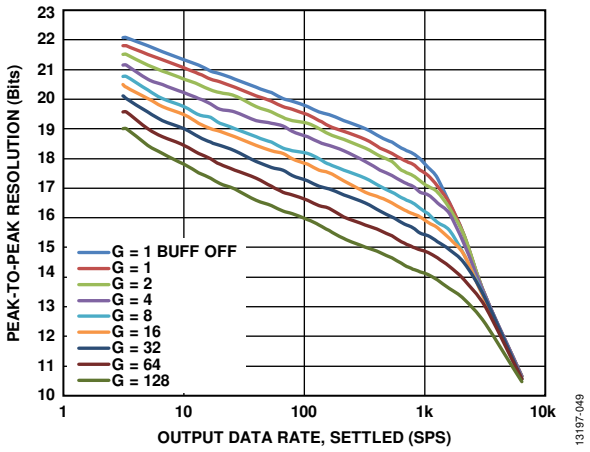

Figure 50. Peak-to-Peak Resolution vs. Output Data Rate (Settled), Sinc^3 Filter (Full Power Mode)

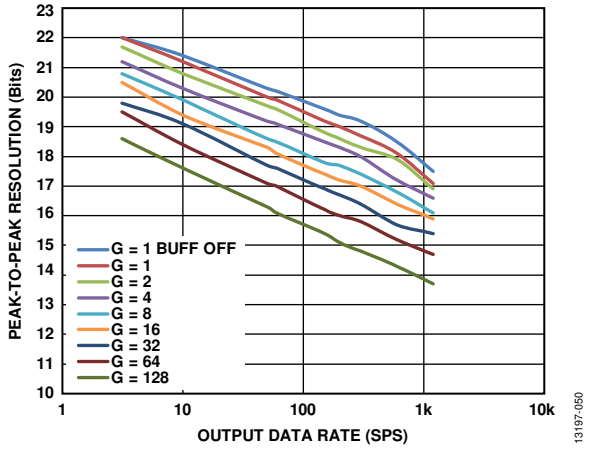

Figure 51. Peak-to-Peak Resolution vs. Output Data Rate, Sinc^4 + Sinc^1 Filter (Full Power Mode)

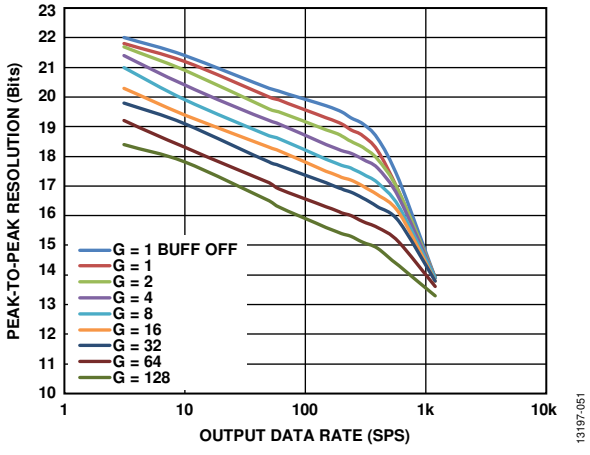

Figure 52. Peak-to-Peak Resolution vs. Output Data Rate, Sinc^3 + Sinc^1 Filter (Full Power Mode)

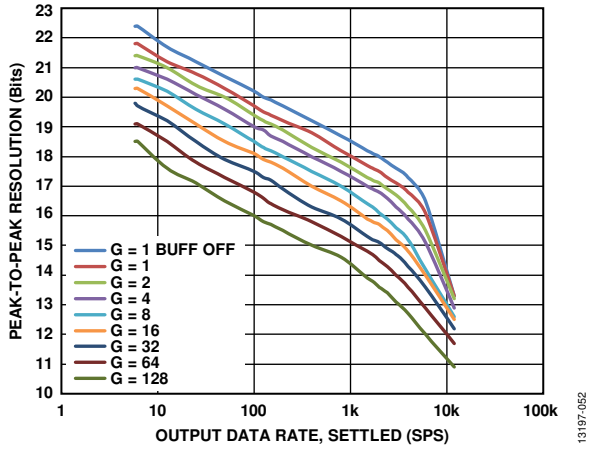

Figure 53. Peak-to-Peak Resolution vs. Output Data Rate (Settled), Sinc^4 Filter (Mid Power Mode)

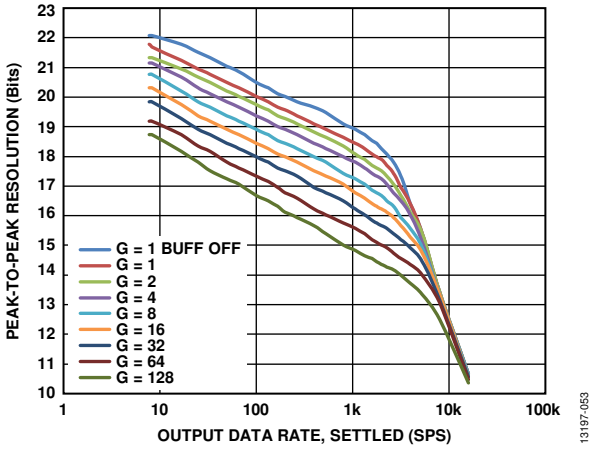

Figure 54. Peak-to-Peak Resolution vs. Output Data Rate (Settled), Sinc^3 Filter (Mid Power Mode)

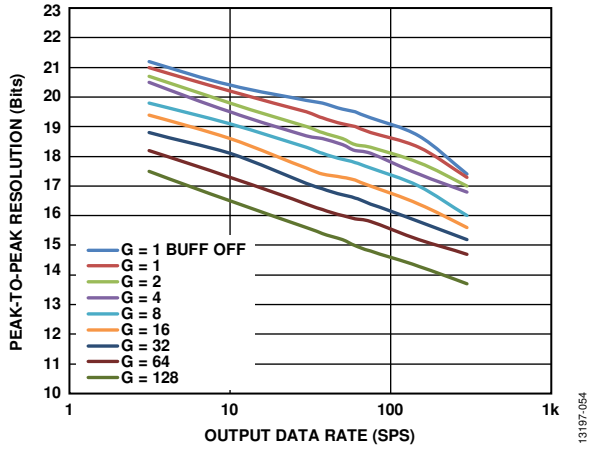

Figure 55. Peak-to-Peak Resolution vs. Output Data Rate, Sinc^4 + Sinc^1 Filter (Mid Power Mode)

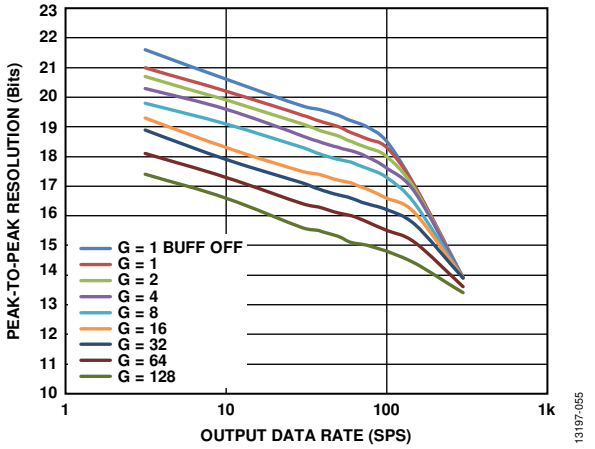

Figure 56. Peak-to-Peak Resolution vs. Output Data Rate, Sinc^3 + Sinc^1 Filter (Mid Power Mode)

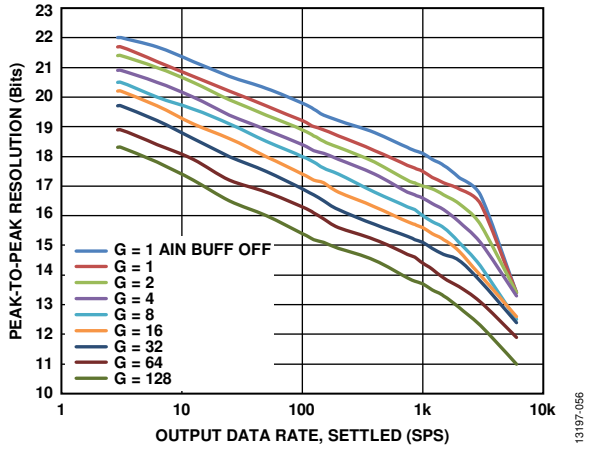

Figure 57. Peak-to-Peak Resolution vs. Output Data Rate (Settled), Sinc^4 Filter (Low Power Mode)

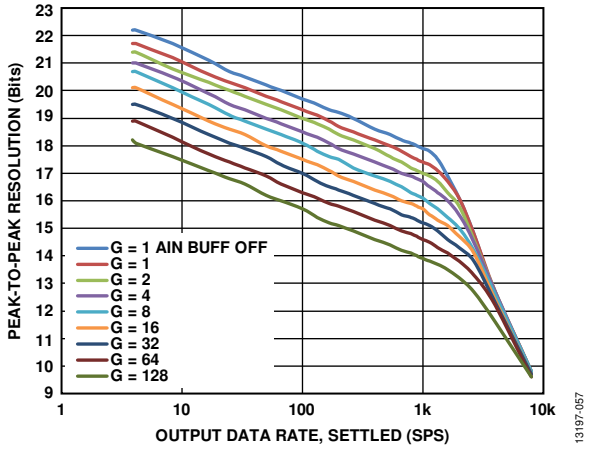

Figure 58. Peak-to-Peak Resolution vs. Output Data Rate (Settled), Sinc^3 Filter (Low Power Mode)