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Programmable Controller for Capacitance Touch Sensors

AD7142

FEATURES

- **Programmable capacitance-to-digital converter**
  - **36 ms update rate (@ maximum sequence length)**
  - **Better than 1 fF resolution**
  - **14 capacitance sensor input channels**
  - **No external RC tuning components required**
  - **Automatic conversion sequencer**
- **On-chip automatic calibration logic**
  - **Automatic compensation for environmental changes**
  - **Automatic adaptive threshold and sensitivity levels**
- **On-chip RAM to store calibration data**
- **SPI®-compatible serial interface (AD7142)**
- **I²C®-compatible serial interface (AD7142-1)**
- **Separate V_{DRIVE} level for serial interface**
- **Interrupt output and GPIO**
- **32-lead, 5 mm x 5 mm LFCSP_VQ**
- **2.6 V to 3.6 V supply voltage**
- **Low operating current**
  - **Full power mode: less than 1 mA**
  - **Low power mode: 50 µA**

APPLICATIONS

- **Personal music and multimedia players**
- **Cell phones**
- **Digital still cameras**
- **Smart hand-held devices**
- **Television, A/V, and remote controls**
- **Gaming consoles**

FUNCTIONAL BLOCK DIAGRAM

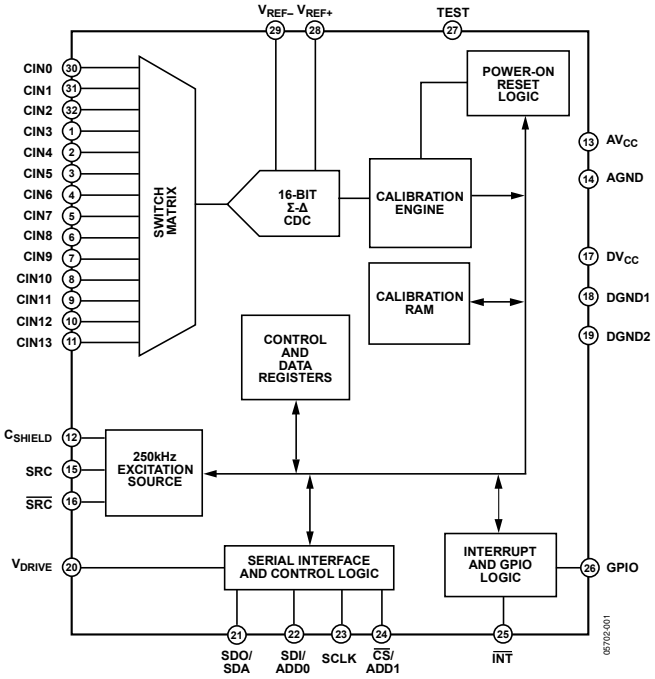

Figure 1.

GENERAL DESCRIPTION

The AD7142 and AD7142-1 are integrated capacitance-to-digital converters (CDCs) with on-chip environmental calibration for use in systems requiring a novel user input method. The AD7142 and AD7142-1 can interface to external capacitance sensors implementing functions such as capacitive buttons, scroll bars, or wheels.

The CDC has 14 inputs channeled through a switch matrix to a 16-bit, 250 kHz sigma-delta (Σ-Δ) capacitance-to-digital converter. The CDC is capable of sensing changes in the capacitance of the external sensors and uses this information to register a sensor activation. The external sensors can be arranged as a series of buttons, as a scroll bar or wheel, or as a combination of sensor types. By programming the registers, the user has full control over the CDC setup. High resolution sensors require minor software to run on the host processor.

The AD7142 and AD7142-1 have on-chip calibration logic to account for changes in the ambient environment. The calibration sequence is performed automatically and at continuous intervals, when the sensors are not touched. This ensures that there are no false or nonregistering touches on the external sensors due to a changing environment.

The AD7142 has an SPI-compatible serial interface, and the AD7142-1 has an I²C-compatible serial interface. Both parts have an interrupt output, as well as a general-purpose input/output (GPIO).

The AD7142 and AD7142-1 are available in a 32-lead, 5 mm × 5 mm LFCSP_VQ and operate from a 2.6 V to 3.6 V supply. The operating current consumption is less than 1 mA, falling to 50 µA in low power mode (conversion interval of 400 ms).

Rev. A

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AD7142* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-829: Environmental Compensation on the AD7142: The Effects of Temperature and Humidity on Capacitance Sensors
- AN-830: Factors Affecting Sensor Response
- AN-833: Using the AD7142 and a Capacitive Sensor to Develop a Single-Push Digital Shutter Button
- AN-854: Sensor PCB Design Guidelines for the AD7142 and AD7143 Capacitance-to-Digital Converters
- AN-856: AD7142 Applications Using Sensor Buttons
- AN-857: Introduction to AD7142 Host Software Requirements
- AN-858: AD7142 Sensor Board In-Line Production Test Procedure
- AN-929: Tuning the AD714x for CapTouch® Applications

Data Sheet

- AD7142: Programmable Controller for Capacitance Touch Sensors Data Sheet

Product Highlight

- Leading Inside Advertorials: Providing an Edge in Capacitive Sensor Applications

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD714X Input CapTouchÂ® Programmable Controller Linux Driver

REFERENCE MATERIALS

Technical Articles

- Building a reliable capacitive-sensor interface
- Capacitive Sensors Can Replace Mechanical Switches for Touch Control
- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD7142 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7142 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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1/07—Rev. 0 to Rev. A

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Deleted FIFO Control Section 19
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Added Slow FIFO and SLOW_FILTER_UPDATE_LVL Section 23
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6/06—Revision 0: Initial Version

SPECIFICATIONS

AV_{CC}, DV_{CC} = 2.6 V to 3.6 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CAPACITANCE-TO-DIGITAL CONVERTER					
Update Rate	35.45	36.86	38.4	ms	12 conversion stages in sequencer, decimation rate = 256
Resolution		16		Bit	
CIN Input Range[1]		±2		pF	
No Missing Codes	16			Bit	Guaranteed by design, but not production tested
CIN Input Leakage		25		nA	
Total Unadjusted Error			±20	%	
Output Noise (Peak-to-Peak)		7		Codes	Decimation rate = 128
		3		Codes	Decimation rate = 256
Output Noise (RMS)		0.8		Codes	Decimation rate = 128
		0.5		Codes	Decimation rate = 256
Parasitic Capacitance			40	pF	Parasitic capacitance to ground, per CIN input guaranteed by characterization
C_{BULK} Offset Range[1]		±20		pF	
C_{BULK} Offset Resolution		156.25		fF	
Low Power Mode Delay Accuracy			4	%	% of 200 ms, 400 ms, 600 ms, or 800 ms
EXCITATION SOURCE					
Frequency	240	250	260	kHz	
Output Voltage			AV_{CC}	V	
Short-Circuit Source Current		20		mA	
Short-Circuit Sink Current		50		mA	
Maximum Output Load		250		pF	Capacitance load on source to ground
C_{SHIELD} Output Drive		10		µA	
C_{SHIELD} Bias Level		$AV_{CC}/2$		V	
LOGIC INPUTS (SDI, SCLK, $\overline{CS}$, SDA, GPI TEST)					
V_{IH} Input High Voltage	$0.7 \times V_{DRIVE}$			V	
V_{IL} Input Low Voltage			0.4	V	
I_{IH} Input High Voltage	−1			µA	$V_{IN} = V_{DRIVE}$
I_{IL} Input Low Voltage			1	µA	V_{IN} = DGND
Hysteresis		150		mV	
OPEN-DRAIN OUTPUTS (SCLK, SDA, $\overline{INT}$)					
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = −1 mA
I_{OH} Output High Leakage Current		0.1	±1	µA	$V_{OUT} = V_{DRIVE}$
LOGIC OUTPUTS (SDO, GPO)					
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = 1 mA, V_{DRIVE} = 1.65 V to 3.6 V
V_{OH} Output High Voltage	$V_{DRIVE} - 0.6$			V	I_{SOURCE} = 1 mA, V_{DRIVE} = 1.65 V to 3.6 V
SDO Floating State Leakage Current			±1	µA	Pin three-state, leakage measured to GND and DV_{CC}
GPO Floating State Leakage Current	−5		2	µA	Pin three-state, leakage measured to GND and DV_{CC}
POWER					
AV_{CC}, DV_{CC}	2.6	3.3	3.6	V	
V_{DRIVE}	1.65		3.6	V	Serial interface operating voltage
I_{CC}		0.9	1	mA	In full power mode
			20	µA	Low power mode, converter idle, T_A = 25°C
		16	33	µA	Low power mode, converter idle
			4.5	µA	Full shutdown, T_A = 25°C
		2.25	18	µA	Full shutdown

[1] C_{IN} and C_{BULK} are defined in Figure 2.

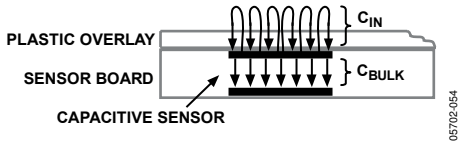


Figure 2.

Table 2. Typical Average Current in Low Power Mode, AV_{CC}, DV_{CC} = 3.6 V, T= 25°C, Load of 50 pF on SRC Pin, No Load on $\overline{SRC}$

		Number of Conversion Stages (Current Values Expressed in µA)											
Low Power Mode Delay	**Decimation Rate**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
200 ms	128	26.4	33.3	40.1	46.9	53.5	60	66.5	72.8	79.1	85.2	91.3	97.3
	256	35.6	49.1	62.2	74.9	87.3	99.3	111	122.3	133.4	144.2	154.7	164.9
400 ms	128	21.3	24.8	28.3	31.7	35.2	38.6	42	45.4	48.7	52	55.3	58.6
	256	26	32.9	39.7	46.5	53.1	59.6	66.1	72.4	78.7	84.9	91	97
600 ms	128	19.6	21.9	24.3	26.6	28.9	31.2	33.5	35.8	38.1	40.4	42.6	44.8
	256	22.7	27.4	32	36.6	41.1	45.6	50	54.4	58.8	63.1	67.4	71.6
800 ms	128	18.7	20.5	22.2	24	25.7	27.5	29.2	31	32.7	34.4	36.1	37.8
	256	21.1	24.6	28.1	31.5	35	38.4	41.8	45.2	48.5	51.8	55.1	58.4

Table 3. Maximum Average Current in Low Power Mode, AV_{CC}, DV_{CC} = 3.6 V, Load of 50 pF on SRC Pin, No Load on $\overline{SRC}$

		Number of Conversion Stages (Current Values Expressed in µA)											
Low Power Mode Delay	**Decimation Rate**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
200 ms	128	45.4	53.6	61.5	69.4	77.1	84.7	92.2	99.6	106.8	113.9	121	127.9
	256	56.2	72	87.2	102	116.3	130.2	143.7	156.8	169.5	181.8	193.8	205.5
400 ms	128	39.5	43.6	47.7	51.8	55.8	59.8	63.7	67.6	71.5	75.4	79.2	83
	256	45	53.1	61.1	68.9	76.7	84.3	91.8	99.1	106.4	113.6	120.6	127.5
600 ms	128	37.5	40.3	43	45.8	48.5	51.2	53.9	56.5	59.2	61.8	64.5	67.1
	256	41.2	46.7	52.1	57.4	62.7	67.9	73.1	78.2	83.3	88.3	93.3	98.2
800 ms	128	36.5	38.6	40.7	42.7	44.8	46.8	48.8	50.9	52.9	54.9	56.9	58.9
	256	39.3	43.4	47.5	51.5	55.6	59.5	63.5	67.4	71.3	75.2	79	82.8

SPI TIMING SPECIFICATIONS (AD7142)

T_A = −40°C to +85°C; V_{DRIVE} = 1.65 V to 3.6 V; AV_{CC}, DV_{CC} = 2.6 V to 3.6 V, unless otherwise noted. Sample tested at 25°C to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.6 V.

Table 4. SPI Timing Specifications

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK}	5	MHz max	
t_1	5	ns min	$\overline{CS}$ falling edge to first SCLK falling edge
t_2	20	ns min	SCLK high pulse width
t_3	20	ns min	SCLK low pulse width
t_4	15	ns min	SDI setup time
t_5	15	ns min	SDI hold time
t_6	20	ns max	SDO access time after SCLK falling edge
t_7	16	ns max	$\overline{CS}$ rising edge to SDO high impedance
t_8	15	ns min	SCLK rising edge to $\overline{CS}$ high

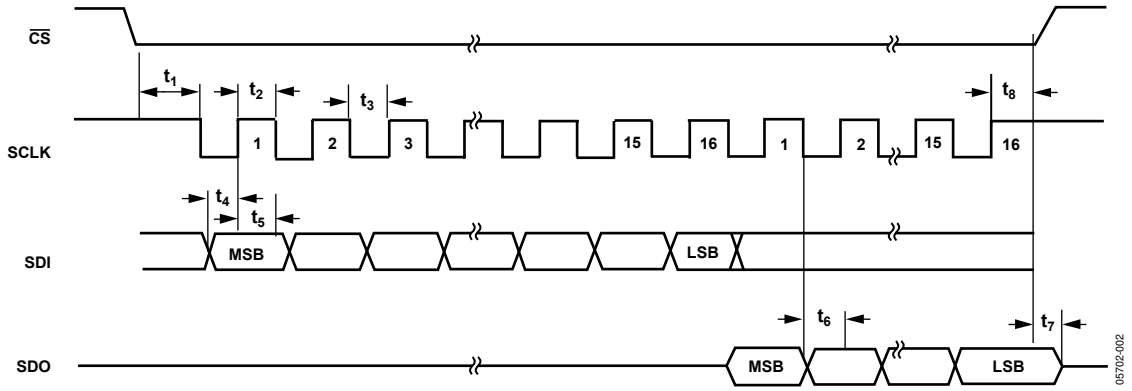


Figure 3. SPI Detailed Timing Diagram

I²C TIMING SPECIFICATIONS (AD7142-1)

T_A = −40°C to +85°C; V_{DRIVE} = 1.65 V to 3.6 V; AV_{CC}, DV_{CC} = 2.6 V to 3.6 V, unless otherwise noted. Sample tested at 25°C to ensure compliance. All input signals timed from a voltage level of 1.6 V.

Table 5. I²C Timing Specifications[1]

Parameter	Limit	Unit	Description
f_{SCLK}	400	kHz max	
t_1	0.6	µs min	Start condition hold time, $t_{HD; STA}$
t_2	1.3	µs min	Clock low period, t_{LOW}
t_3	0.6	µs min	Clock high period, t_{HIGH}
t_4	100	ns min	Data setup time, $t_{SU; DAT}$
t_5	300	ns min	Data hold time, $t_{HD; DAT}$
t_6	0.6	µs min	Stop condition setup time, $t_{SU; STO}$
t_7	0.6	µs min	Start condition setup time, $t_{SU; STA}$
t_8	1.3	µs min	Bus free time between stop and start conditions, t_{BUF}
t_R	300	ns max	Clock/data rise time
t_F	300	ns max	Clock/data fall time

[1] Guaranteed by design, not production tested.

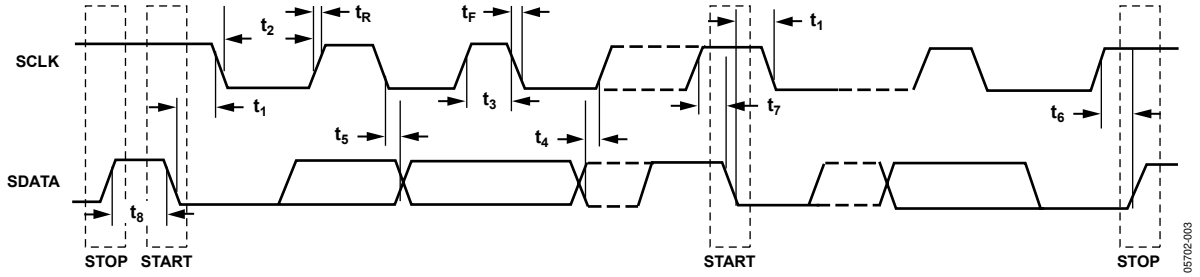


Figure 4. I²C Detailed Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AV_{CC} to AGND, DV_{CC} to DGND	−0.3 V to +3.6 V
Analog Input Voltage to AGND	−0.3 V to AV_{CC} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Input Current to Any Pin Except Supplies[1]	10 mA
ESD Rating (Human Body Model)	2.5 kV
Operating Temperature Range	−40°C to +150°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
LFCSP_VQ	
Power Dissipation	450 mW
θ_{JA} Thermal Impedance	135.7°C/W
IR Reflow Peak Temperature	260°C (±0.5°C)
Lead Temperature (Soldering 10 sec)	300°C

[1]Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

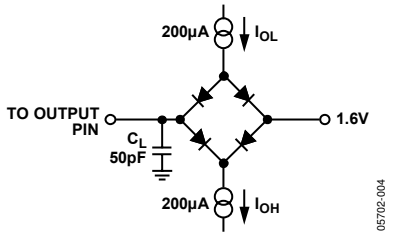


Figure 5. Load Circuit for Digital Output Timing Specifications

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

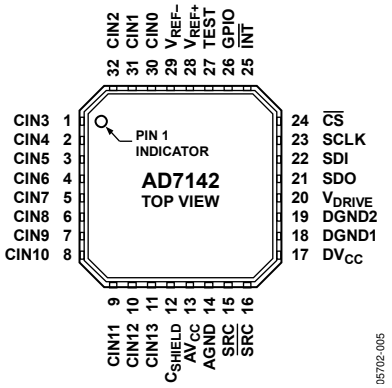


Figure 6. AD7142 Pin Configuration

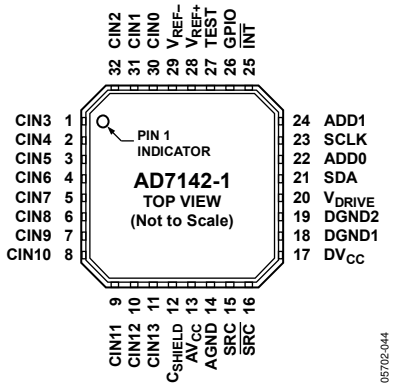


Figure 7. AD7142-1 Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CIN3	Capacitance Sensor Input.
2	CIN4	Capacitance Sensor Input.
3	CIN5	Capacitance Sensor Input.
4	CIN6	Capacitance Sensor Input.
5	CIN7	Capacitance Sensor Input.
6	CIN8	Capacitance Sensor Input.
7	CIN9	Capacitance Sensor Input.
8	CIN10	Capacitance Sensor Input.
9	CIN11	Capacitance Sensor Input.
10	CIN12	Capacitance Sensor Input.
11	CIN13	Capacitance Sensor Input.
12	C_{SHIELD}	CDC Shield Potential Output. Requires 10 nF capacitor to ground. Connect to external shield.
13	AV_{CC}	CDC Supply Voltage.
14	AGND	Analog Ground Reference Point for All CDC Circuitry. Tie to analog ground plane.
15	SRC	CDC Excitation Source Output.
16	$\overline{SRC}$	Inverted Excitation Source Output.
17	DV_{CC}	Digital Core Supply Voltage.
18	DGND1	Digital Ground.
19	DGND2	Digital Ground.
20	V_{DRIVE}	Serial Interface Operating Voltage Supply.
21	SDO	(AD7142) SPI Serial Data Output.
	SDA	(AD7142-1) I²C Serial Data Input/Output. SDA requires pull-up resistor.
22	SDI	(AD7142) SPI Serial Data Input.
	ADD0	(AD7142-1) I²C Address Bit 0.
23	SCLK	Clock Input for Serial Interface.
24	$\overline{CS}$	(AD7142) SPI Chip Select Signal.
	ADD1	(AD7142-1) I²C Address Bit 1.
25	$\overline{INT}$	General-Purpose Open-Drain Interrupt Output. Programmable polarity; requires pull-up resistor.
26	GPIO	Programmable GPIO.
27	TEST	Factory Test Pin. Tie to ground.
28	V_{REF+}	CDC Positive Reference Input. Normally tied to analog power.
29	V_{REF-}	CDC Negative Reference Input. Tie to analog ground.
30	CIN0	Capacitance Sensor Input.
31	CIN1	Capacitance Sensor Input.
32	CIN2	Capacitance Sensor Input.

TYPICAL PERFORMANCE CHARACTERISTICS

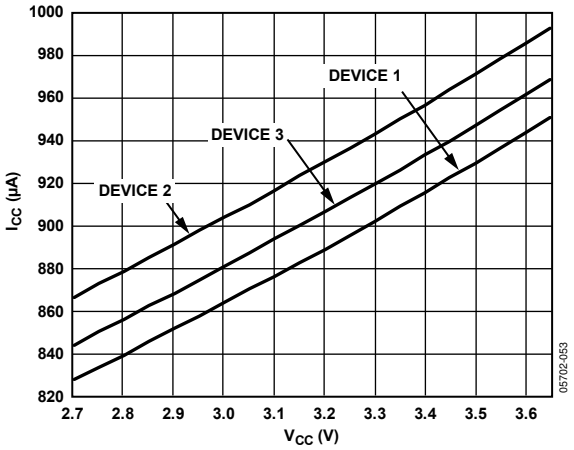


Figure 8. Supply Current vs. Supply Voltage (V_{CC} = AV_{CC} + DV_{CC}, I_{CC} = AI_{CC} + DI_{CC})

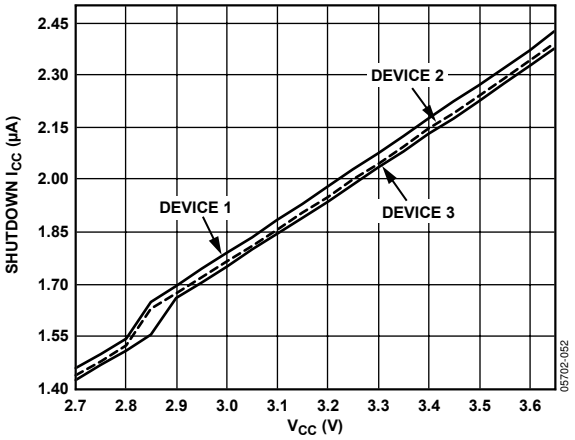


Figure 11. Shutdown Supply Current vs. Supply Voltage (V_{CC} = AV_{CC} + DV_{CC}, I_{CC} = AI_{CC} + DI_{CC})

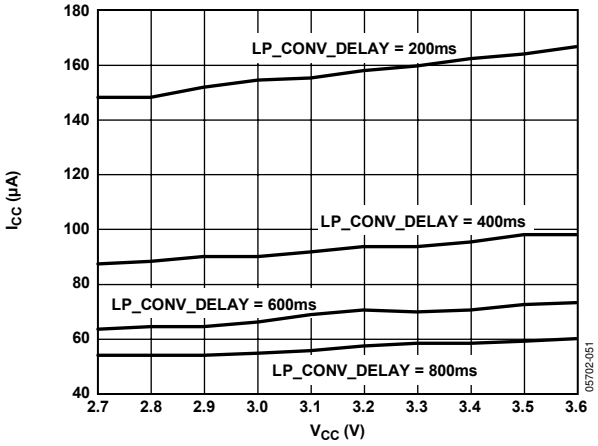


Figure 9. Low Power Supply Current vs. Supply Voltage, Decimation Rate = 256 (V_{CC} = AV_{CC} + DV_{CC}, I_{CC} = AI_{CC} + DI_{CC})

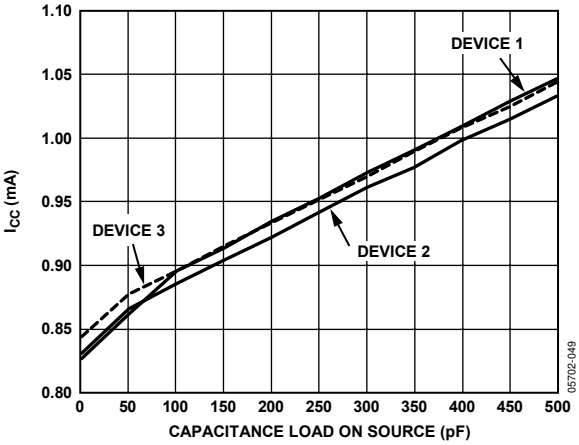


Figure 12. Supply Current vs. Capacitive Load on SRC (I_{CC} = AI_{CC} + DI_{CC})

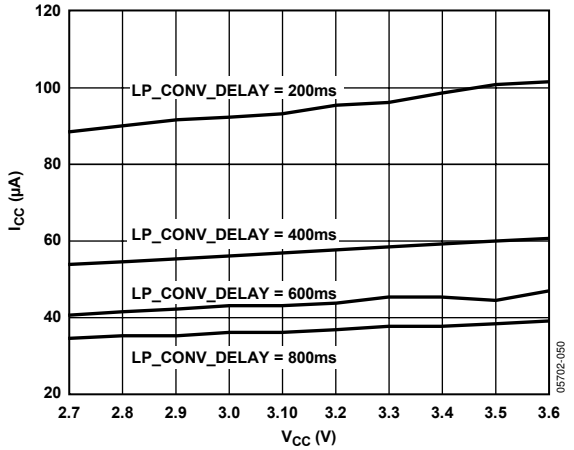


Figure 10. Low Power Supply Current vs. Supply Voltage Decimation Rate = 128 (V_{CC} = AV_{CC} + DV_{CC}, I_{CC} = AI_{CC} + DI_{CC})

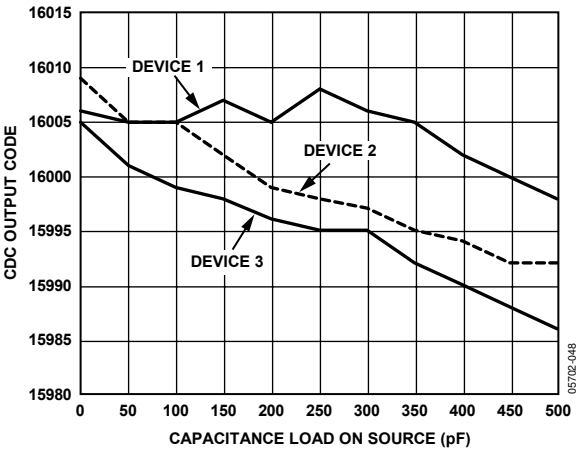


Figure 13. Output Code vs. Capacitive Load on SRC

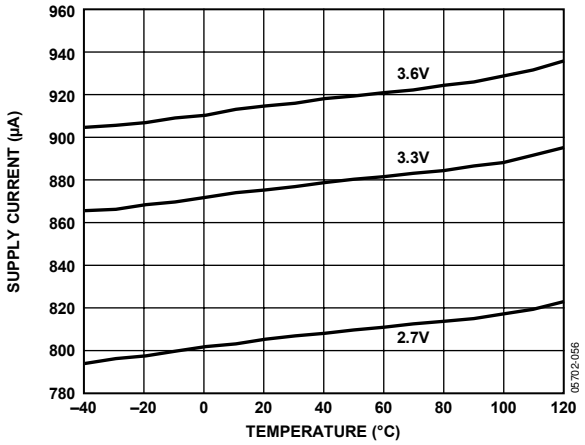


Figure 14. Supply Current vs. Temperature (Supply Current = AI_{CC} + DI_{CC})

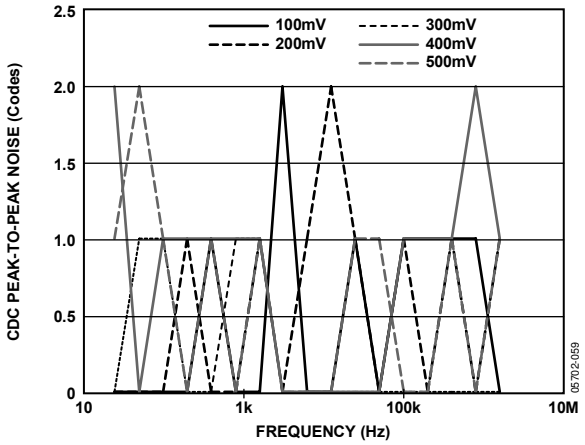


Figure 16. Power Supply Sine Wave Rejection

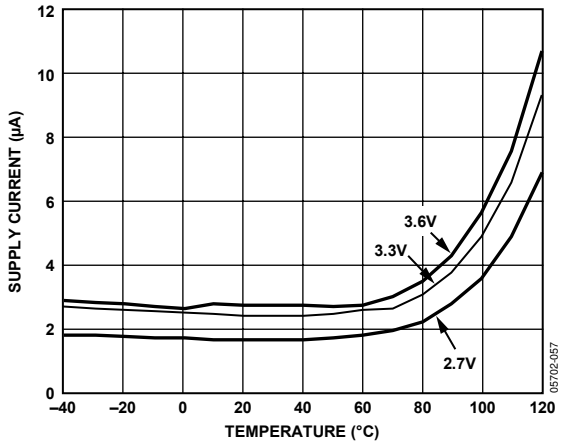


Figure 15. Shutdown Supply Current vs. Temperature (Supply Current = AI_{CC} + DI_{CC})

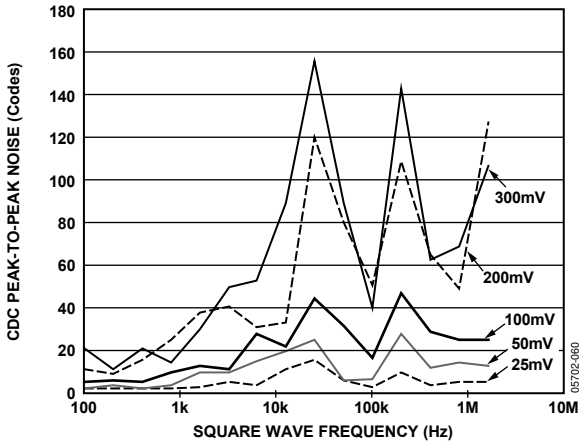


Figure 17. Power Supply Square Wave Rejection

THEORY OF OPERATION

The AD7142 and AD7142-1 are capacitance-to-digital converters (CDCs) with on-chip environmental compensation, intended for use in portable systems requiring high resolution user input. The internal circuitry consists of a 16-bit, ∑-Δ converter that converts a capacitive input signal into a digital value. There are 14 input pins on the AD7142 and AD7142-1, CIN0 to CIN13. A switch matrix routes the input signals to the CDC. The result of each capacitance-to-digital conversion is stored in on-chip registers. The host subsequently reads the results over the serial interface. The AD7142 contains an SPI interface and the AD7142-1 has an I^2C interface ensuring that the parts are compatible with a wide range of host processors. Because the AD7142 and AD7142-1 are identical parts, with the exception of the serial interface, AD7142 refers to both the AD7142 and AD7142-1 throughout this data sheet.

The AD7142 interfaces with up to 14 external capacitance sensors. These sensors can be arranged as buttons, scroll bars, wheels, or as a combination of sensor types. The external sensors consist of electrodes on a single or multiple layer PCB that interfaces directly to the AD7142.

The AD7142 can be set up to implement any set of input sensors by programming the on-chip registers. The registers can also be programmed to control features such as averaging, offsets, and gains for each of the external sensors. There is a sequencer on-chip to control how each of the capacitance inputs is polled.

The AD7142 has on-chip digital logic and 528 words of RAM that are used for environmental compensation. The effects of humidity, temperature, and other environmental factors can effect the operation of capacitance sensors. Transparent to the user, the AD7142 performs continuous calibration to compensate for these effects, allowing the AD7142 to give error-free results at all times.

The AD7142 requires some minor companion software that runs on the host or other microcontroller to implement high resolution sensor functions such as a scroll bar or wheel. However, no companion software is required to implement buttons, including 8-way button functionality. Button sensors are implemented completely in digital logic on-chip.

The AD7142 can be programmed to operate in either full power mode, or in low power automatic wake-up mode. The automatic wake-up mode is particularly suited for portable devices that require low power operation giving the user significant power savings coupled with full functionality.

The AD7142 has an interrupt output, $\overline{\text{INT}}$, to indicate when new data has been placed into the registers. $\overline{\text{INT}}$ is used to interrupt the host on sensor activation. The AD7142 operates from a 2.6 V to 3.6 V supply, and is available in a 32-lead, 5 mm × 5 mm LFCSP_VQ.

CAPACITANCE SENSING THEORY

The AD7142 uses a method of sensing capacitance known as the shunt method. Using this method, an excitation source is connected to a transmitter generating an electric field to a receiver. The field lines measured at the receiver are translated into the digital domain by a ∑-Δ converter. When a finger, or other grounded object, interferes with the electric field, some of the field lines are shunted to ground and do not reach the receiver (see Figure 18). Therefore, the total capacitance measured at the receiver decreases when an object comes close to the induced field.

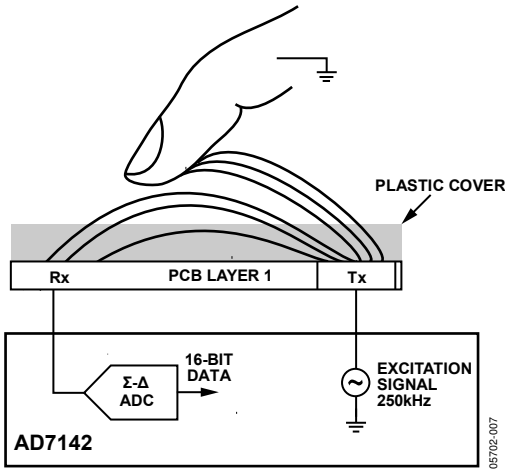


Figure 18. Sensing Capacitance Method

In practice, the excitation source and ∑-Δ ADC are implemented on the AD7142, and the transmitter and receiver are constructed on a PCB that makes up the external sensor.

Registering a Sensor Activation

When a sensor is approached, the total capacitance associated with that sensor, measured by the AD7142, changes. When the capacitance changes to such an extent that a set threshold is exceeded, the AD7142 registers this as a sensor touch.

Preprogrammed threshold levels are used to determine if a change in capacitance is due to a button being activated. If the capacitance exceeds one of the threshold limits, the AD7142 registers this as a true button activation. The same thresholds principle is used to determine if other types of sensors, such as sliders or scroll wheels, are activated.

Complete Solution for Capacitance Sensing

Analog Devices, Inc. provides a complete solution for capacitance sensing. The two main elements to the solution are the sensor PCB and the AD7142.

If the application requires high resolution sensors, such as scroll bars or wheels, software is required that runs on the host processor. (No software is required for button sensors.) The memory requirements for the host depend on the sensor, and are typically 10 kB of code and 600 bytes of data memory.

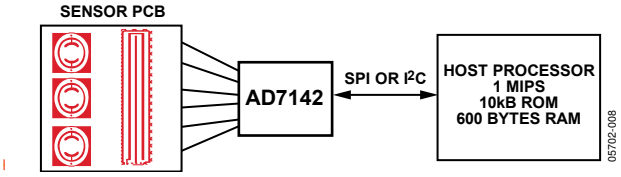


Figure 19. Three Part Capacitance Sensing Solution

Analog Devices supplies the sensor PCB footprint design libraries to the customer based on the customer's specifications, and supplies any necessary software on an open-source basis.

OPERATING MODES

The AD7142 has three operating modes. Full power mode, where the device is always fully powered, is suited for applications where power is not a concern (for example, game consoles that have an ac power supply). Low power mode, where the part automatically powers down, is tailored to give significant power savings over full power mode, and is suited for mobile applications where power must be conserved. In shutdown mode, the part shuts down completely.

The POWER_MODE bits (Bit 0 and Bit 1) of the control register set the operating mode on the AD7142. The control register is at Address 0x000. Table 8 shows the POWER_MODE settings for each operating mode. To put the AD7142 into shutdown mode, set the POWER_MODE bits to either 01 or 11.

Table 8. POWER_MODE Settings

POWER_MODE Bits	Operating Mode
00	Full power mode
01	Full shutdown mode
10	Low power mode
11	Full shutdown mode

The power-on default setting of the POWER_MODE bits is 00, full power mode.

Full Power Mode

In full power mode, all sections of the AD7142 remain fully powered at all times. When a sensor is being touched, the AD7142 processes the sensor data. If no sensor is touched, the AD7142 measures the ambient capacitance level and uses this data for the on-chip compensation routines. In full power mode, the AD7142 converts at a constant rate. See the CDC Conversion Sequence Time section for more information.

Low Power Mode

When in low power mode, the AD7142 POWER_MODE bits are set to 10 upon device initialization. If the external sensors are not touched, the AD7142 reduces its conversion frequency, thereby greatly reducing its power consumption. The part remains in a reduced power state when the sensors are not touched. Every LP_CONV_DELAY ms (200, 400, 600 or 800 ms), the AD7142 performs a conversion and uses this data to update the compensation logic. When an external sensor is touched, the AD7142 begins a conversion sequence every 36 ms to read back data from the sensors. In low power mode, the total current consumption of the AD7142 is an average of the current used during a conversion, and the current used when the AD7142 is waiting for the next conversion to begin. For example, when LP_CONV_DELAY l is 400 ms, the AD7142 typically uses 0.9 mA current for 36 ms, and 15 µA for 400 ms of the conversion interval. Note that these conversion timings can be altered through the register settings. See the CDC Conversion Sequence Time section for more information.

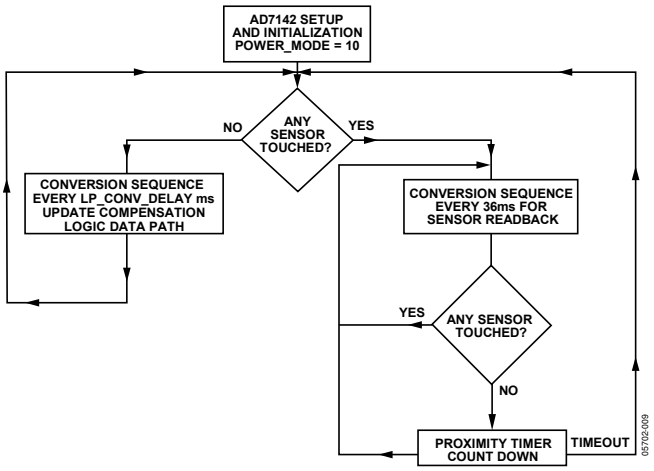


Figure 20. Low Power Mode Operation

The time taken for the AD7142 to go from a full power state to a reduced power state, once the user stops touching the external sensors, is configurable. The PWR_DWN_TIMEOUT bits, in Ambient Compensation Ctrl 0 Register, at Address 0x002, control the length of time the AD7142 takes before going into the reduced power state, once the sensors are not touched.

CAPACITANCE SENSOR INPUT CONFIGURATION

Each input connection from the external capacitance sensors to the AD7142 converter can be uniquely configured by using the registers in Table 45 and Table 46. These registers are used to configure input pin connection setups, sensor offsets, sensor sensitivities, and sensor limits for each stage. Each sensor can be individually optimized. For example, a button sensor connected to STAGE0 can have different sensitivity and offset values than a button with a different function that is connected to a different stage.

CIN INPUT MULTIPLEXER SETUP

The CIN_CONNECTION_SETUP registers in Table 45 list the different options that are provided for connecting the sensor input pin to the CDC.

The AD7142 has an on-chip multiplexer to route the input signals from each pin to the input of the converter. Each input pin can be tied to either the negative or the positive input of the CDC, or it can be left floating. Each input can also be internally connected to the C_{SHIELD} signal to help prevent cross coupling. If an input is not used, always connect it to C_{SHIELD}.

Connecting a CINx input pin to the positive CDC input results in a decrease in CDC output code when the corresponding sensor is activated. Connecting a CINx input pin to the negative CDC input results in an increase in CDC output code when the corresponding sensor is activated.

The multiplexer settings for each conversion sequence can be unique and different for each of the input pins, CIN0 to CIN13. For example, CIN0 is connected to the negative CDC input for conversion STAGE1, left floating for sequencer STAGE1, and so on for all twelve conversion stages.

Two bits in each sequence stage register control the mux setting for the input pin.

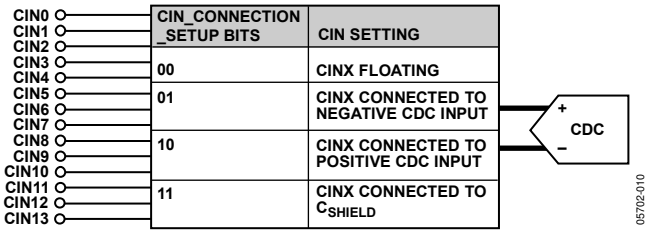


Figure 21. Input Mux Configuration Options

CAPACITANCE-TO-DIGITAL CONVERTER

The capacitance-to-digital converter on the AD7142 has a Σ-Δ architecture with 16-bit resolution. There are 14 possible inputs to the CDC that are connected to the input of the converter through a switch matrix. The sampling frequency of the CDC is 250 kHz.

OVERSAMPLING THE CDC OUTPUT

The decimation rate, or oversampling ratio, is determined by Bits[9:8] of the control register, as listed in Table 9.

Table 9. CDC Decimation Rate

Decimation Bit Value	Decimation Rate	CDC Output Rate Per Stage
00	256	3.072 ms
01	128	1.536 ms
10[1]	–	–
11[1]	–	–

[1] Do not use this setting.

The decimation process on the AD7142 is an averaging process where a number of samples are taken and the averaged result is output. Due to the architecture of the digital filter employed, the amount of samples taken (per stage) is equal to 3 times the decimation rate. So 3 × 256 or 3 × 128 samples are averaged to obtain each stage result.

The decimation process reduces the amount of noise present in the final CDC result. However, the higher the decimation rate, the lower the output rate per stage, thus, a trade-off is possible between a noise-free signal and speed of sampling.

CAPACITANCE SENSOR OFFSET CONTROL

There are two programmable DACs on board the AD7142 to null any capacitance sensor offsets. These offsets are associated with printed circuit board capacitance or capacitance due to any other source, such as connectors. In Figure 22, C_{IN} is the capacitance of the input sensors, and C_{BULK} is the capacitance between layers of the sensor PCB. C_{BULK} can be offset using the on-board DACs.

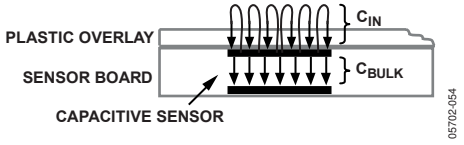


Figure 22. Capacitances Around the Sensor PCB

A simplified block diagram in Figure 23 shows how to apply the STAGE_OFFSET registers to null the offsets. The 7-bit POS_AFE_OFFSET and NEG_AFE_OFFSET registers program the offset DAC to provide 0.16 pF resolution offset adjustment over a range of ±20 pF. Apply the positive and negative offsets to either the positive or the negative CDC input using the NEG_AFE_OFFSET register and POS_AFE_OFFSET register.

This process is only required once during the initial capacitance sensor characterization.

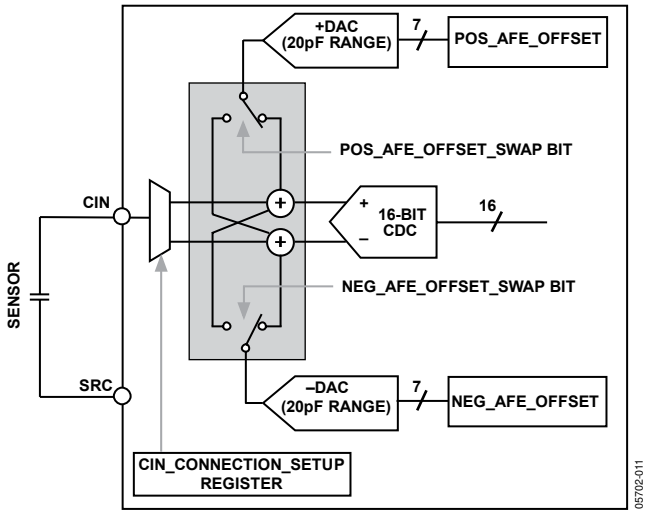


Figure 23. Analog Front-End Offset Control

CONVERSION SEQUENCER

The AD7142 has an on-chip sequencer to implement conversion control for the input channels. Up to 12 conversion stages can be performed in one sequence. Each of the 12 conversion stages can measure the input from a different sensor. By using the Bank 2 registers, each stage can be uniquely configured to support multiple capacitance sensor interface requirements. For example, a slider sensor can be assigned to STAGE1 through STAGE8, with a button sensor assigned to STAGE0.

The AD7142 on-chip sequence controller provides conversion control beginning with STAGE0. Figure 24 shows a block diagram of the CDC conversion stages and CIN inputs. A conversion sequence is defined as a sequence of CDC conversions starting at STAGE0 and ending at the stage determined by the value programmed in the SEQUENCE_STAGE_NUM register. Depending on the number and type of capacitance sensors that are used, not all conversion stages are required. Use the SEQUENCE_STAGE_NUM register to set the number of conversions in one sequence, depending on the sensor interface requirements. For example, this register would be set to 5 if the CIN inputs were mapped to only six stages. In addition, set the STAGE_CAL_EN registers according to the number of stages that are used.

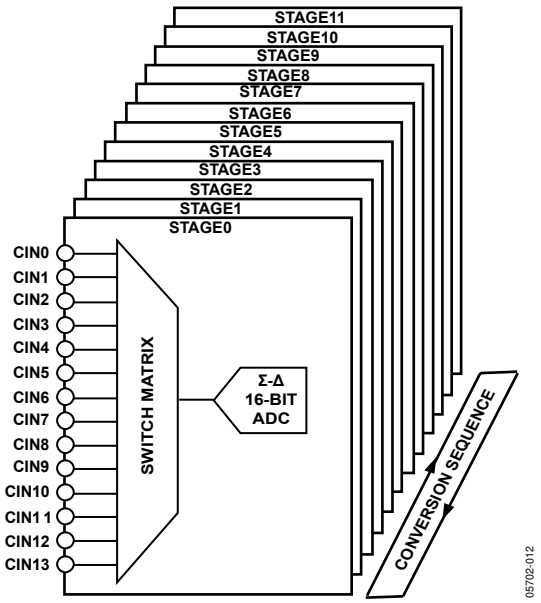


Figure 24. CDC Conversion Stages

The number of required conversion stages depends completely on the number of sensors attached to the AD7142. Figure 25 shows how many conversion stages are required for each sensor, and how many inputs each sensor requires to the AD7142.

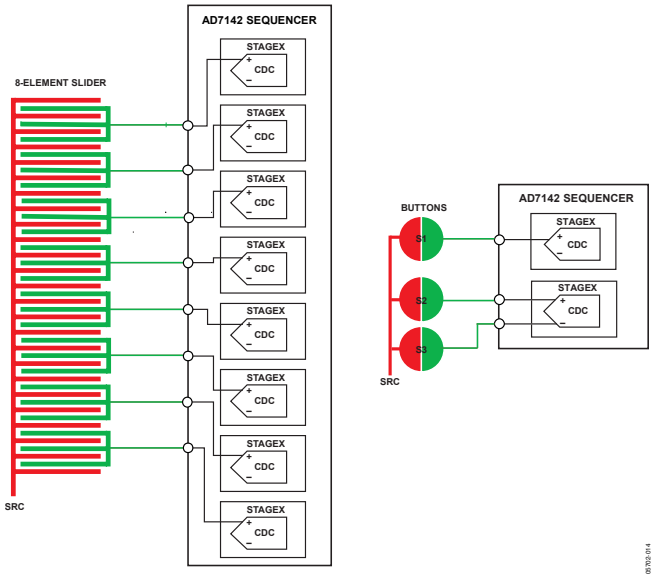


Figure 25. Sequencer Setup for Sensors

A button sensor generally requires one sequencer stage; however, it is possible to configure two button sensors to operate differentially. Only one button from the pair can be activated at a time; pressing both buttons together results in neither button being activated. This configuration requires one conversion stage, and is shown in Figure 25, B2 and B3.

A scroll bar or slider sensor requires eight stages. The result from each stage is used by the host software to determine the user's position on the scroll bar. The algorithm that performs this process is available from Analog Devices free of charge, on signing a software license. Scroll wheels also require eight stages.

The 8-way switch is made from two pairs of differential buttons. It, therefore, requires two conversion stages, one for each of the differential button pairs. It also requires a stage to measure whether the sensor is active. The buttons are orientated so that one pair makes up the top and bottom portions of the 8-way switch; the other pair makes up the left and right portions of the 8-way switch.

CDC CONVERSION SEQUENCE TIME

The time required for one complete measurement for all 12 stages by the CDC is defined as the CDC conversion sequence time. The SEQUENCE_STAGE_NUM register and DECIMATION register determine the conversion time as listed in Table 10.

Table 10. CDC Conversion Times for Full Power Mode

	Conversion Time (ms)	
SEQUENCE_STAGE_NUM	**DECIMATION = 128**	**DECIMATION = 256**
0	1.536	3.072
1	3.072	6.144
2	4.608	9.216
3	6.144	12.288
4	7.68	15.36
5	9.216	18.432
6	10.752	21.504
7	12.288	24.576
8	13.824	27.648
9	15.36	30.72
10	16.896	33.792
11	18.432	36.864

For example, operating with a decimation rate of 128, if the SEQUENCE_STAGE_NUM register is set to 5 for the conversion of six stages in a sequence, the conversion sequence time is 9.216 ms.

Full Power Mode CDC Conversion Sequence Time

The full power mode CDC conversion sequence time for all 12 stages is set by configuring the SEQUENCE_STAGE_NUM register, and DECIMATION register as outlined in Table 10.

Figure 26 shows a simplified timing diagram of the full power CDC conversion time. The full power mode CDC conversion time, t_{CONV_FP}, is set using Table 10.

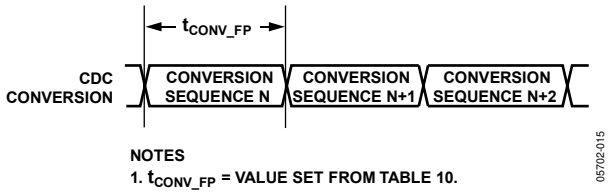


Figure 26. Full Power Mode CDC Conversion Sequence Time

Low Power Mode CDC Conversion Sequence Time with Delay

The frequency of each CDC conversion operating in the low power automatic wake-up mode is controlled by using the LP_CONV_DELAY register located at Address 0x000[3:2], in addition to the registers listed in Table 10. This feature provides some flexibility for optimizing the conversion time to meet system requirements vs. AD7142 power consumption.

For example, maximum power savings is achieved when the LP_CONV_DELAY register is set to 3. With a setting of 3, the AD7142 automatically wakes up, performing a conversion every 800 ms.

Table 11. LP_CONV_DELAY Settings

LP_CONV_DELAY Bits	Delay Between Conversions
00	200 ms
01	400 ms
10	600 ms
11	800 ms

Figure 27 shows a simplified timing example of the low power CDC conversion time. As shown, the low power CDC conversion time is set by t_{CONV_FP} and the LP_CONV_DELAY register.

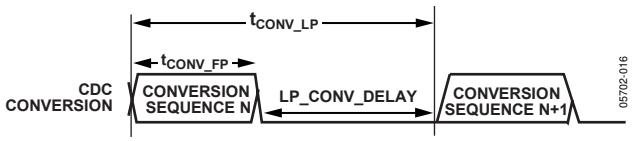


Figure 27. Low Power Mode CDC Conversion Sequence Time

CDC CONVERSION RESULTS

Certain high resolution sensors require the host to read back the CDC conversion results for processing. The registers required for host processing are located in the Bank 3 registers. The host processes the data readback from these registers using a software algorithm, to determine position information.

In addition to the results registers in the Bank 3 registers, the AD7142 provides the 16-bit CDC output data directly, starting at Address 0x00B of Bank 1. Reading back the CDC 16-bit conversion data register allows for customer-specific application data processing.

NONCONTACT PROXIMITY DETECTION

The AD7142 internal signal processing continuously monitors all capacitance sensors for noncontact proximity detection. This feature provides the ability to detect when a user is approaching a sensor, at which time all internal calibration is immediately disabled and the AD7142 is automatically configured to detect a valid contact.

The proximity control register bits are described in Table 12. The FP_PROXIMITY_CNT register bits and LP_PROXIMITY_CNT register bits control the length of the calibration disable period after the user leaves the sensor and proximity is no longer active, in full and low power modes. The calibration is disabled during this time and enabled again at the end of this period provided that the user is no longer approaching, or in contact with, the sensor. Figure 28 and Figure 29 show examples of how these registers are used to set the full and low power mode calibration disable periods.

Calibration disable period in full power mode = FP_PROXIMITY_CNT × 16 × Time taken for one conversion sequence in full power mode

Calibration disable period in low power mode = LP_PROXIMITY_CNT × 4 × Time taken for one conversion sequence in low power mode

RECALIBRATION

In certain situations, the proximity flag can be set for a long period, for example when a user hovers over a sensor for a long time. The environmental calibration on the AD7142 is suspended when proximity is detected, but changes may occur to the ambient capacitance level during the proximity event. This means the ambient value stored on the AD7142 no longer represents the actual ambient value. In this case, even when the user has left the sensor, the proximity flag may still be set. This situation could occur if the user interaction creates some moisture on the sensor causing the new sensor ambient value to be different from the expected value. In this situation, the AD7142 automatically forces a recalibration internally. This ensures that the ambient values are recalibrated regardless of how long the user hovers over a sensor. A recalibration ensures maximum AD7142 sensor performance.

The AD7142 recalibrates automatically when the measured CDC value exceeds the stored ambient value by an amount determined by PROXIMITY_RECAL_LVL, for a set period of time known as the recalibration timeout. In full power mode, the recalibration timeout is controlled by FP_PROXIMITY_RECAL, and in low power mode, by LP_PROXIMITY_RECAL.

Recalibration timeout in full power mode = FP_PROXIMITY_RECAL × Time taken for one conversion sequence in full power mode

Recalibration timeout in low power mode = LP_PROXIMITY_RECAL × Time taken for one conversion sequence in low power mode

Figure 30 and Figure 31 show examples of how the FP_PROXIMITY_RECAL and LP_PROXIMITY_RECAL register bits control the timeout period before a recalibration, operating in the full and low power modes. These figures show a user approaching a sensor followed by the user leaving the sensor and the proximity detection remains active after the user leaves the sensor. The measured CDC value exceeds the stored ambient value by the amount set in the PROXIMITY_RECAL_LVL bits, for the entire timeout period. The sensor is automatically recalibrated at the end of the timeout period. The forced recalibration takes two interrupt cycles, therefore, it should not be set again during this interval.

PROXIMITY SENSITIVITY

The fast filter in Figure 32 is used to detect when someone is close to the sensor (proximity). Two conditions set the internal proximity detection signal using Comparator 1 and Comparator 2. Comparator 1 detects when a user is approaching a sensor. The PROXIMITY_DETECTION_RATE register controls the sensitivity of Comparator 1. For example, if PROXIMITY_DETECTION_RATE is set to 4, the Proximity 1 signal is set when the absolute difference between WORD1 and WORD3 exceeds four LSB codes. Comparator 2 detects when a user hovers over a sensor or approaches a sensor very slowly. The PROXIMITY_RECAL_LVL register (Address 0x003) controls the sensitivity of Comparator 2. For example, if PROXIMITY_RECAL_LVL is set to 75, the Proximity 2 signal is set when the absolute difference between the fast filter average value and the ambient value exceeds 75 LSB codes.

Table 12. Proximity Control Registers (See Figure 32)

Register	Length	Register Address	Description
FP_PROXIMITY_CNT	4 bits	0x002 [7:4]	Calibration disable time in full power mode
LP_PROXIMITY_CNT	4 bits	0x002 [11:8]	Calibration disable time in low power mode
FP_PROXIMITY_RECAL	8 bits	0x004 [9:0]	Full power mode proximity recalibration time
LP_PROXIMITY_RECAL	6 bits	0x004 [15:10]	Low power mode proximity recalibration time
PROXIMITY_RECAL_LVL	8 bits	0x003 [13:8]	Proximity recalibration level
PROXIMITY_DETECTION_RATE	6 bits	0x003 [7:0]	Proximity detection rate

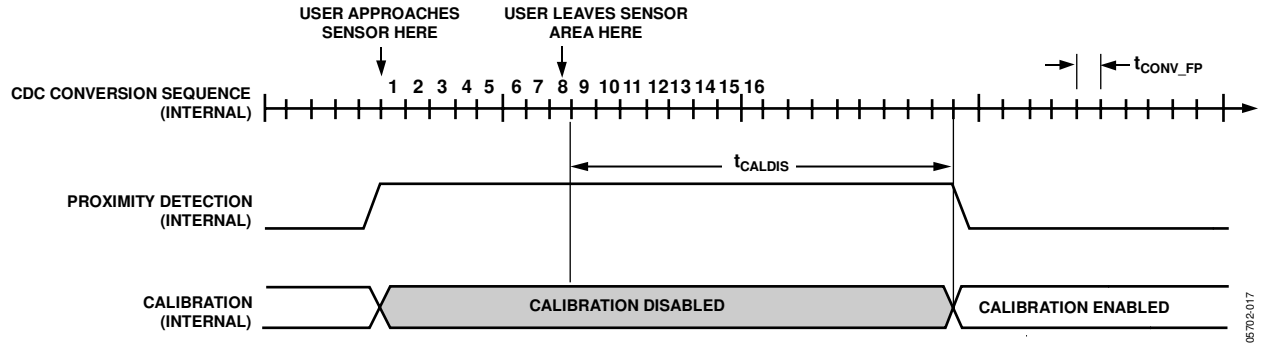


Figure 28. Full Power Mode Proximity Detection Example with FP_PROXIMITY_CNT = 1

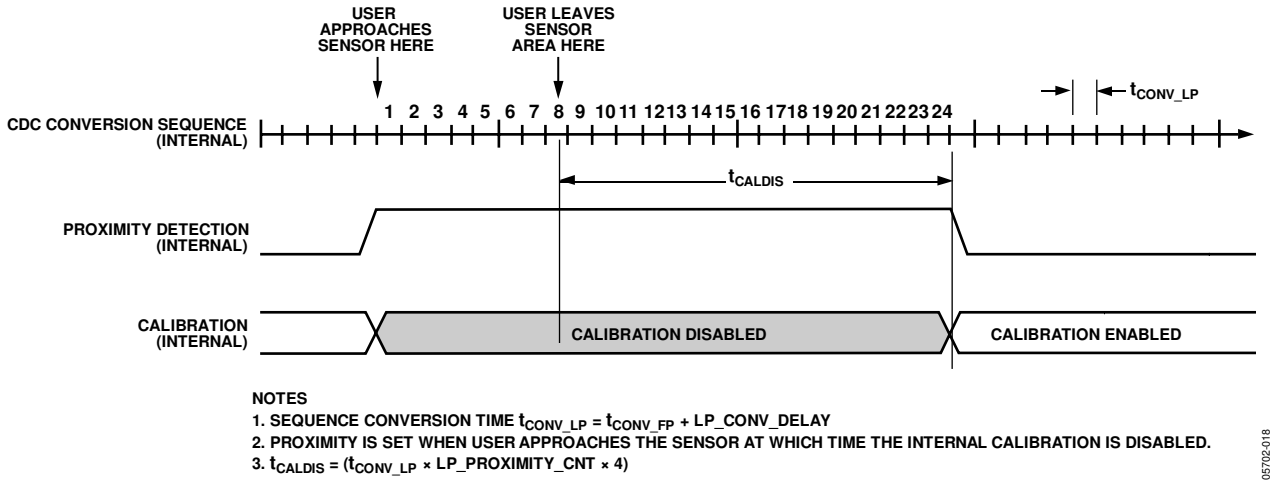


Figure 29. Low Power Mode Proximity Detection with LP_PROXIMITY_CNT = 4

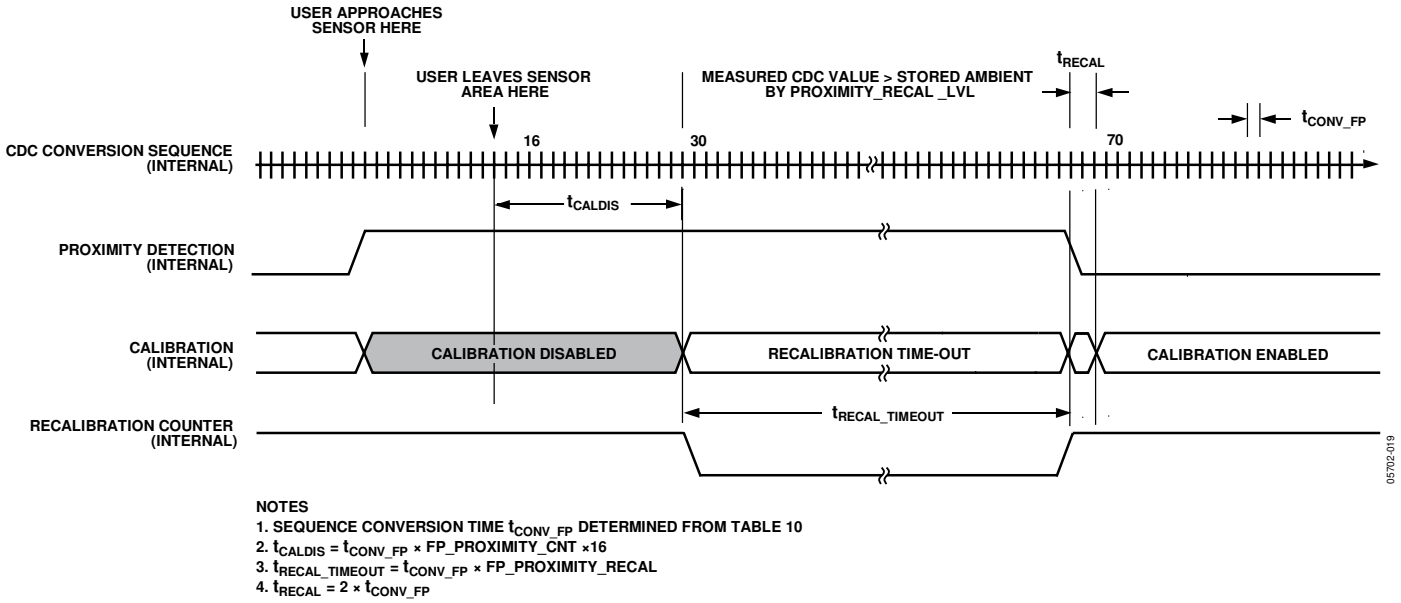


Figure 30. Full Power Mode Proximity Detection with Forced Recalibration Example with FP_PROXIMITY_CNT = 1 and FP_PROXIMITY_RECAL = 40

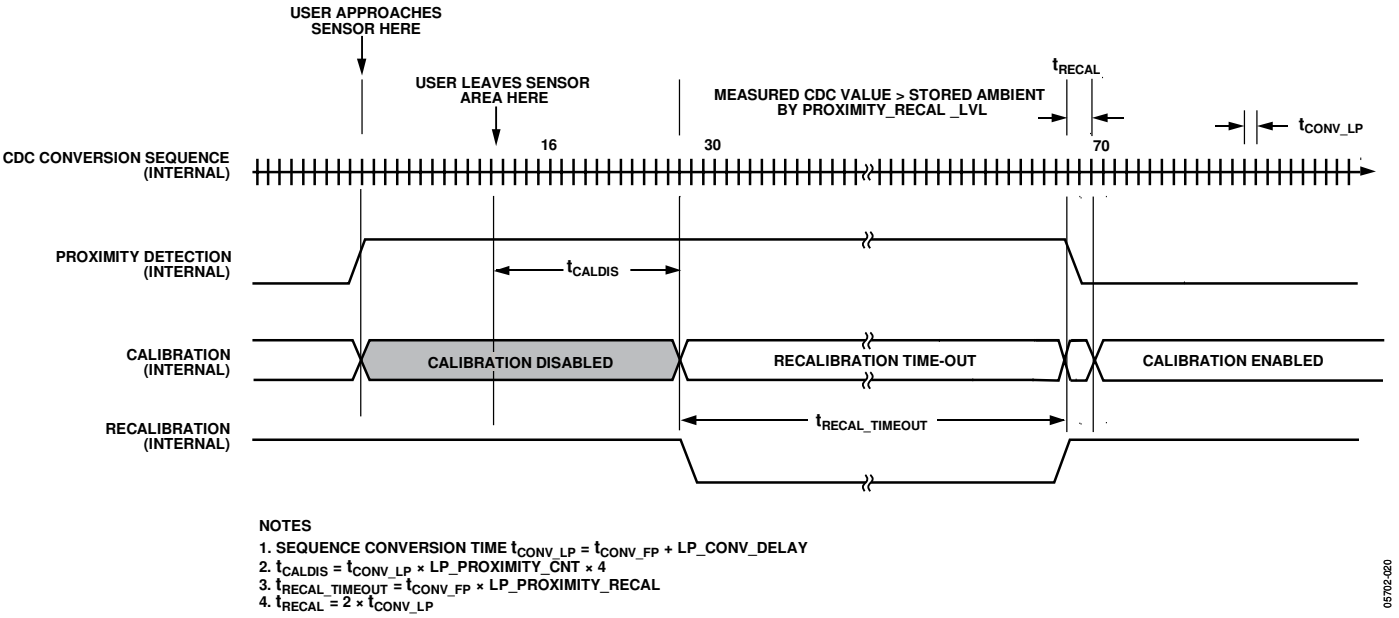


Figure 31. Low Power Mode Proximity Detection with Forced Recalibration Example with LP_PROXIMITY_CNT = 4 and LP_PROXIMITY_RECAL = 40

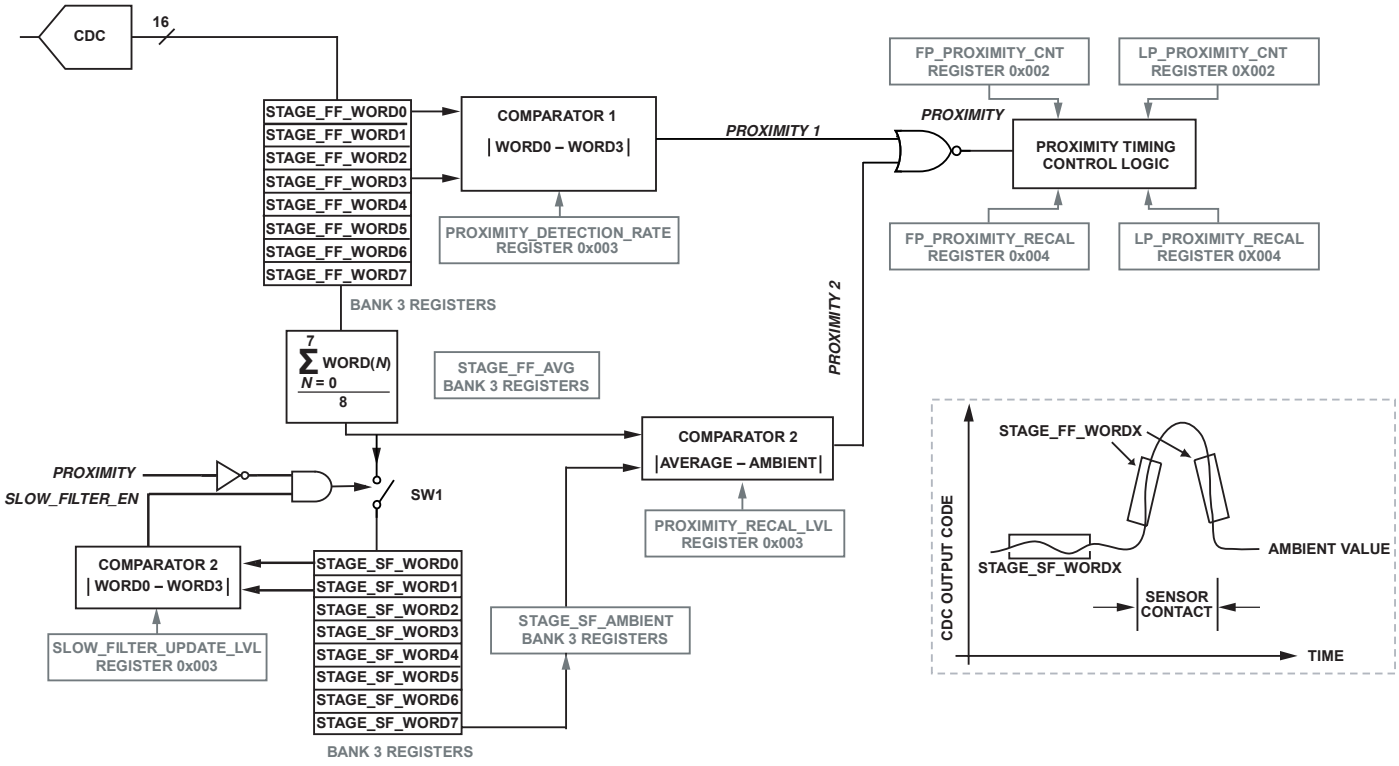
FF_SKIP_CNT

The proximity detection fast FIFO is used by the on-chip logic to determine if proximity is detected. The fast FIFO expects to receive samples from the converter at a set rate. FF_SKIP_CNT is used to normalize the frequency of the samples going into the FIFO, regardless of how many conversion stages are in a sequence. In Register 0x02, Bits[3:0] are the fast filter skip control, FF_SKIP_CNT. This value determines which CDC samples are not used (skipped) in the proximity detection fast FIFO.

Determining the FF_SKIP_CNT value is required only once during the initial setup of the capacitance sensor interface. Table 13 shows how FF_SKIP_CNT controls the update rate to the fast FIFO. Recommended value for this setting when using all 12 conversion stages on the AD7142 is FF_SKIP_CNT = 0000 = no samples skipped.

Table 13. FF_SKIP_CNT Settings

	FAST FIFO Update Rate	
FF_SKIP_CNT	**DECIMATION = 128**	**DECIMATION = 256**
0	1.536 × (SEQUENCE_STAGE_NUM + 1) ms	3.072 × (SEQUENCE_STAGE_NUM + 1) ms
1	3.072 × (SEQUENCE_STAGE_NUM + 1) ms	6.144 × (SEQUENCE_STAGE_NUM + 1) ms
2	4.608 × (SEQUENCE_STAGE_NUM + 1) ms	9.216 × (SEQUENCE_STAGE_NUM + 1) ms
3	6.144 × (SEQUENCE_STAGE_NUM + 1) ms	12.288 × (SEQUENCE_STAGE_NUM + 1) ms
4	7.68 × (SEQUENCE_STAGE_NUM + 1) ms	15.36 × (SEQUENCE_STAGE_NUM + 1) ms
5	9.216 × (SEQUENCE_STAGE_NUM + 1) ms	18.432 × (SEQUENCE_STAGE_NUM + 1) ms
6	10.752 × (SEQUENCE_STAGE_NUM + 1) ms	21.504 × (SEQUENCE_STAGE_NUM + 1) ms
7	12.288 × (SEQUENCE_STAGE_NUM + 1) ms	24.576 × (SEQUENCE_STAGE_NUM + 1) ms
8	13.824 × (SEQUENCE_STAGE_NUM + 1) ms	27.648 × (SEQUENCE_STAGE_NUM + 1) ms
9	15.36 × (SEQUENCE_STAGE_NUM + 1) ms	30.72 × (SEQUENCE_STAGE_NUM + 1) ms
10	16.896 × (SEQUENCE_STAGE_NUM + 1) ms	33.792 × (SEQUENCE_STAGE_NUM + 1) ms
11	18.432 × (SEQUENCE_STAGE_NUM + 1) ms	36.864 × (SEQUENCE_STAGE_NUM + 1) ms
12	19.968 × (SEQUENCE_STAGE_NUM + 1) ms	39.936 × (SEQUENCE_STAGE_NUM + 1) ms
13	21.504 × (SEQUENCE_STAGE_NUM + 1) ms	43.008 × (SEQUENCE_STAGE_NUM + 1) ms
14	23.04 × (SEQUENCE_STAGE_NUM + 1) ms	46.08 × (SEQUENCE_STAGE_NUM + 1) ms
15	24.576 × (SEQUENCE_STAGE_NUM + 1) ms	49.152 × (SEQUENCE_STAGE_NUM + 1) ms



NOTES
1. *SLOW FILTER EN* IS SET AND SW1 IS CLOSED WHEN |STAGE_SF_WORD 0–STAGE_SF_WORD 1| EXCEEDS THE VALUE PROGRAMMED IN THE SLOW_FILTER_UPDATE_LVL REGISTER PROVIDING *PROXIMITY* IS NOT SET.
2. *PROXIMITY 1* IS SET WHEN |STAGE_FF_WORD 0– STAGE_FF_WORD 3| EXCEEDS THE VALUE PROGRAMMED IN THE PROXIMITY_DETECTION_RATE REGISTER.
3. *PROXIMITY 2* IS SET WHEN |AVERAGE–AMBIENT| EXCEEDS THE VALUE PROGRAMMED IN THE PROXIMITY_RECAL_LVL REGISTER.
4. DESCRIPTION OF COMPARATOR FUNCTIONS:
   COMPARATOR 1: USED TO DETECT WHEN A USER IS APPROACHING OR LEAVING A SENSOR.
   COMPARATOR 2: USED TO DETECT WHEN A USER IS HOVERING OVER A SENSOR, OR APPROACHING A SENSOR VERY SLOWLY.
   ALSO USED TO DETECT IF THE SENSOR AMBIENT LEVEL HAS CHANGED AS A RESULT OF THE USER INTERACTION.
   FOR EXAMPLE, HUMIDITY OR DIRT LEFT BEHIND ON SENSOR.
   COMPARATOR 3: USED TO ENABLE THE SLOW FILTER UPDATE RATE. THE SLOW FILTER IS UPDATED WHEN *SLOW FILTER EN* IS SET AND *PROXIMITY* IS NOT SET.

Figure 32. AD7142 Proximity Detection and Environmental Calibration

ENVIRONMENTAL CALIBRATION

The AD7142 provides on-chip capacitance sensor calibration to automatically adjust for environmental conditions that have an effect on the capacitance sensor ambient levels. Capacitance sensor output levels are sensitive to temperature, humidity, and in some cases, dirt. The AD7142 achieves optimal and reliable sensor performance by continuously monitoring the CDC ambient levels and correcting for any changes by adjusting the STAGE_HIGH_THRESHOLD and STAGE_LOW_ THRESHOLD register values, as described in Equation 1 and Equation 2. The CDC ambient level is defined as the capacitance sensor output level during periods when the user is not approaching or in contact with the sensor.

The compensation logic runs automatically on every conversion after configuration when the AD7142 is not being touched. This allows the AD7142 to account for rapidly changing environmental conditions.

The ambient compensation control registers give the host access to general setup and controls for the compensation algorithm. The RAM stores the compensation data for each conversion stage, as well as setup information specific to each stage.

Figure 33 shows an example of an ideal capacitance sensor behavior where the CDC ambient level remains constant regardless of the environmental conditions. The CDC output shown is for a pair of differential button sensors, where one sensor caused an increase, and the other a decrease in measured capacitance when activated. The positive and negative sensor threshold levels are calculated as a percentage of the STAGE_OFFSET_HIGH and STAGE_OFFSET_LOW values based on the threshold sensitivity settings and the ambient value. These values are sufficient to detect a sensor contact, resulting with the AD7142 asserting the $\overline{\text{INT}}$ output when the threshold levels are exceeded.

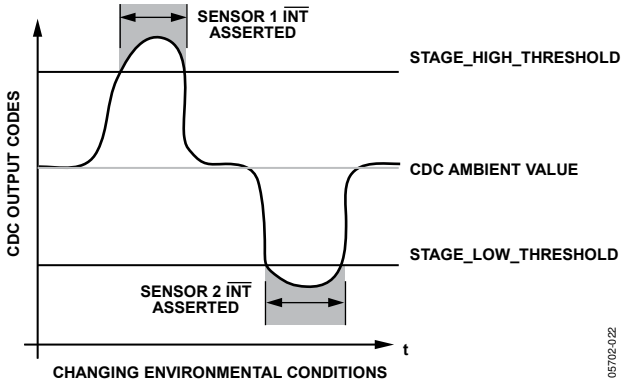


Figure 33. Ideal Sensor Behavior with a Constant Ambient Level

CAPACITANCE SENSOR BEHAVIOR WITHOUT CALIBRATION

Figure 34 shows the typical behavior of a capacitance sensor with no applied calibration. This figure shows ambient levels drifting over time as environmental conditions change. The ambient level drift has resulted in the detection of a missed user contact on Sensor 2. This is a result of the initial low offset level remaining constant when the ambient levels drifted upward beyond the detection range.

The Capacitance Sensor Behavior with Calibration section describes how the AD7142 adaptive calibration algorithm prevents errors such as this from occurring.

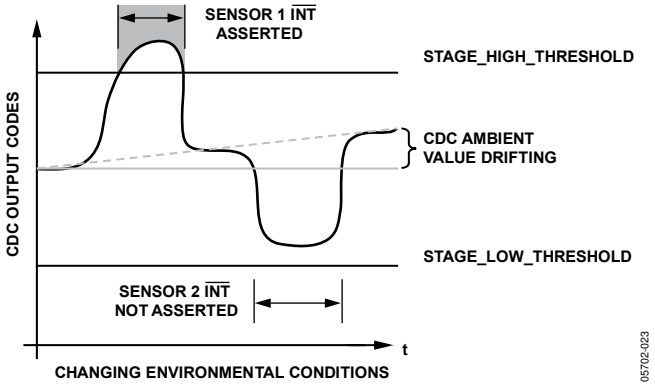


Figure 34. Typical Sensor Behavior Without Calibration Applied

CAPACITANCE SENSOR BEHAVIOR WITH CALIBRATION

The AD7142 on-chip adaptive calibration algorithm prevents sensor detection errors such as the one shown in Figure 34. This is achieved by monitoring the CDC ambient levels and readjusting the initial STAGE_OFFSET_HIGH and STAGE_OFFSET_LOW values according to the amount of ambient drift measured on each sensor. The internal STAGE_HIGH_THRESHOLD and STAGE_LOW_THRESHOLD values described in Equation 1 and Equation 2 are automatically updated based on the new STAGE_OFFSET_HIGH and STAGE_OFFSET_LOW values. This closed-loop routine ensures the reliability and repeatable operation of every sensor connected to the AD7142 under dynamic environmental conditions. Figure 35 shows a simplified example of how the AD7142 applies the adaptive calibration process resulting in no interrupt errors under changing CDC ambient levels due to environmental conditions.

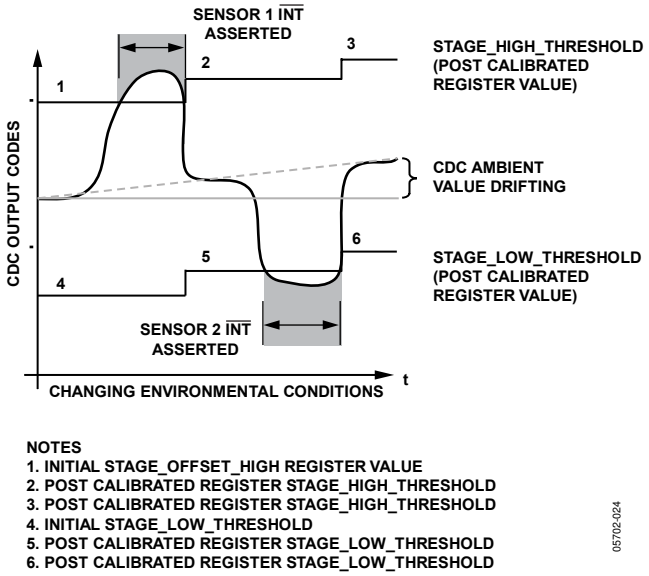


Figure 35. Typical Sensor Behavior with Calibration Applied on the Data Path

SLOW FIFO

As shown in Figure 32, there are a number of FIFOs implemented on the AD7142. These FIFOs are located in Bank 3 of the on-chip memory. The slow FIFOs are used by the on-chip logic to monitor the ambient capacitance level from each sensor.

AVG_FP_SKIP and AVG_LP_SKIP

In Register 0x001, Bits[13:12] are the slow FIFO skip control for full power mode, AVG_FP_SKIP. Bits[15:14] in the same register are the slow FIFO skip control for low power mode, AVG_LP_SKIP. These values determine which CDC samples are not used (skipped) in the slow FIFO. Changing theses values slows down or speeds up the rate at which the ambient capacitance value tracks the measured capacitance value read by the converter.

Slow FIFO update rate in full power mode = AVG_FP_SKIP × [(3 × Decimation Rate) × (SEQUENCE_STAGE_NUM +1) × (FF_SKIP_CNT +1) × 4 × 10^{-7}]

Slow FIFO update rate in low power mode = (AVG_LP_SKIP +1) × [(3 × Decimation Rate) × (SEQUENCE_STAGE_NUM +1) × (FF_SKIP_CNT +1) × 4 × 10^{-7}] / [(FF_SKIP_CNT +1) + LP_CONV_DELAY]

The slow FIFO is used by the on-chip logic to track the ambient capacitance value. The slow FIFO expects to receive samples from the converter at a rate of 33 ms to 40 ms. AVG_FP_SKIP and AVG_LP_SKIP are used to normalize the frequency of the samples going into the FIFO, regardless of how many conversion stages are in a sequence.

Determining the AVG_FP_SKIP and AVG_LP_SKIP value is only required once during the initial setup of the capacitance sensor interface. Recommended values for these settings when using all 12 conversion stages on the AD7142 are:

AVG_FP_SKIP = 00 = skip 3 samples
AVG_LP_SKIP = 00 = skip 0 samples

SLOW_FILTER_UPDATE_LVL

The SLOW_FILTER_UPDATE_LVL controls whether the most recent CDC measurement goes into the Slow FIFO (slow filter) or not. The slow filter is updated when the difference between the current CDC value and last value pushed into the slow FIFO > SLOW_FILTER_UPDATE_LVL. This variable is in Ambient Control Register 1, at Address 0x003.

$$STAGE\_HIGH\_THRESHOLD = STAGE\_SF\_AMBIENT + \left(\frac{STAGE\_OFFSET\_HIGH}{4}\right) + \left(\frac{\left(STAGE\_OFFSET\_HIGH - \frac{STAGE\_OFFSET\_HIGH}{4}\right)}{16}\right) \times POS\_THRESHOLD\_SENSITIVITY$$

Equation 1. On-Chip Logic Stage High Threshold Calculation

$$STAGE\_LOW\_THRESHOLD = STAGE\_SF\_AMBIENT + \left(\frac{STAGE\_OFFSET\_LOW}{4}\right) + \left(\frac{\left(STAGE\_OFFSET\_LOW - \frac{STAGE\_OFFSET\_LOW}{4}\right)}{16}\right) \times NEG\_THRESHOLD\_SENSITIVITY$$

Equation 2. On-Chip Logic Stage Low Threshold Calculation

ADAPTIVE THRESHOLD AND SENSITIVITY

The AD7142 provides an on-chip self-learning adaptive threshold and sensitivity algorithm. This algorithm continuously monitors the output levels of each sensor and automatically rescales the threshold levels proportionally to the sensor area covered by the user. As a result, the AD7142 maintains optimal threshold and sensitivity levels for all types of users regardless of their finger sizes.

The threshold level is always referenced from the ambient level and is defined as the CDC converter output level that must be exceeded for a valid sensor contact. The sensitivity level is defined as how sensitive the sensor is before a valid contact is registered.

Figure 36 provides an example of how the adaptive threshold and sensitivity algorithm works. The positive and negative sensor threshold levels are calculated as a percentage of the STAGE_OFFSET_HIGH and STAGE_OFFSET_LOW values based on the threshold sensitivity settings and the ambient value. On configuration, initial estimates are supplied for both STAGE_OFFSET_HIGH and STAGE_OFFSET_LOW after which the calibration engine automatically adjusts the STAGE_HIGH_THRESHOLD and STAGE_LOW_THRESHOLD values for sensor response.

The AD7142 tracks the average maximum and minimum values measured from each sensor. These values give an indication of how the user is interacting with the sensor. A large finger gives a large average maximum or minimum value, and a small finger gives smaller values. When the average maximum or minimum value changes, the threshold levels are rescaled to ensure that the threshold levels are appropriate for the current user. Figure 37 shows how the minimum and maximum sensor responses are tracked by the on-chip logic.

Reference A in Figure 36 shows an undersensitive threshold level for a small finger user, demonstrating the disadvantages of a fixed threshold level.

By enabling the adaptive threshold and sensitivity algorithm, the positive and negative threshold levels are determined by the POS_THRESHOLD_SENSITIVITY and NEG_THRESHOLD_SENSITIVITY register values and the most recent average maximum sensor output value. These registers can be used to select 16 different positive and negative sensitivity levels ranging between 25% and 95.32% of the most recent average maximum output level referenced from the ambient value. The smaller the sensitivity percentage setting, the easier it is to trigger a sensor activation. Reference B shows that the positive adaptive threshold level is set at almost mid-sensitivity with a 62.51% threshold level by setting POS_THRESHOLD_SENSITIVITY = 1000. Figure 36 also provides a similar example for the negative threshold level with NEG_THRESHOLD_SENSITIVITY = 0001.

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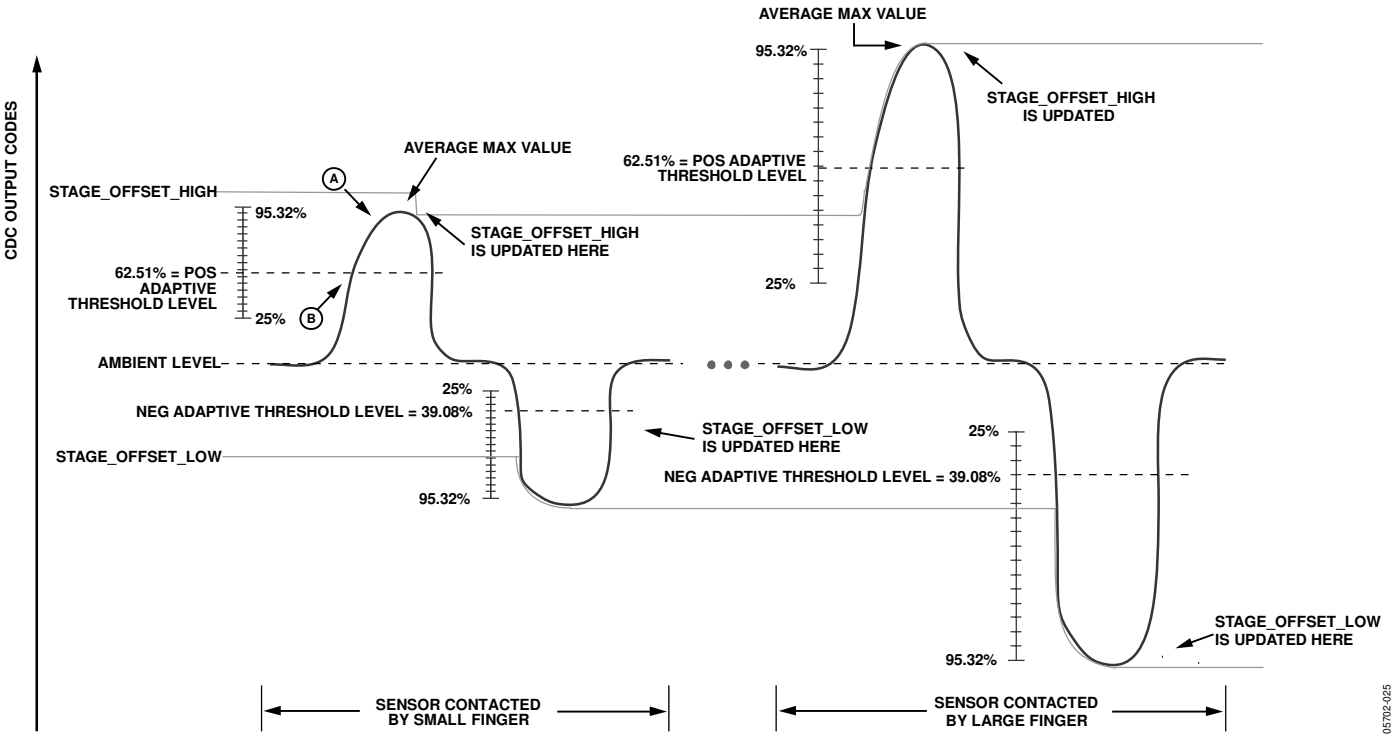

Figure 36. Threshold Sensitivity Example with POS_THRESHOLD_SENSITIVITY = 1000 and NEG_THRESHOLD_SENSITIVITY = 0011