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# CapTouch Programmable Controller for Single-Electrode Capacitance Sensors

# AD7147A

## FEATURES

- **Programmable capacitance-to-digital converter (CDC)**
  - **Femtofarad (fF) resolution**
  - **13 capacitance sensor inputs**
  - **9 ms update rate, all 13 sensor inputs**
  - **No external RC components required**
  - **Automatic conversion sequencer**
- **On-chip automatic calibration logic**
  - **Automatic compensation for environmental changes**
  - **Automatic adaptive threshold and sensitivity levels**
- **Register map is compatible with the AD714x**
- **On-chip RAM to store calibration data**
- **Serial peripheral interface (SPI) (AD7147A)**
- **I²C-compatible serial interface (AD7147A-1)**
- **Separate $V_{DRIVE}$ level for serial interface**
- **Interrupt output and general-purpose input/output (GPIO)**
- **25-ball, 2.3 mm × 2.1 mm WLCSP**
- **2.6 V to 3.6 V supply voltage**
- **Low operating current**
  - **Full power mode: 1 mA**
  - **Low power mode: 28.96 µA**

## APPLICATIONS

- **Cell phones**
- **Personal music and multimedia players**
- **Smart handheld devices**
- **Television, A/V, and remote controls**
- **Gaming consoles**
- **Digital still cameras**

## GENERAL DESCRIPTION

The AD7147A CapTouch™ controller is designed for use with capacitance sensors implementing functions such as buttons, scroll bars, and wheels. The sensors need only one PCB layer, enabling ultrathin applications.

The AD7147A is an integrated CDC with on-chip environmental calibration. The CDC has 13 inputs channeled through a switch matrix to a 16-bit, 250 kHz sigma-delta (Σ-Δ) converter. The CDC is capable of sensing changes in the capacitance of the external sensors and uses this information to register a sensor activation. By programming the registers, the user has full control over the CDC setup.

High resolution sensors require minor software to run on the host processor and may require two PCB layers.

## FUNCTIONAL BLOCK DIAGRAM

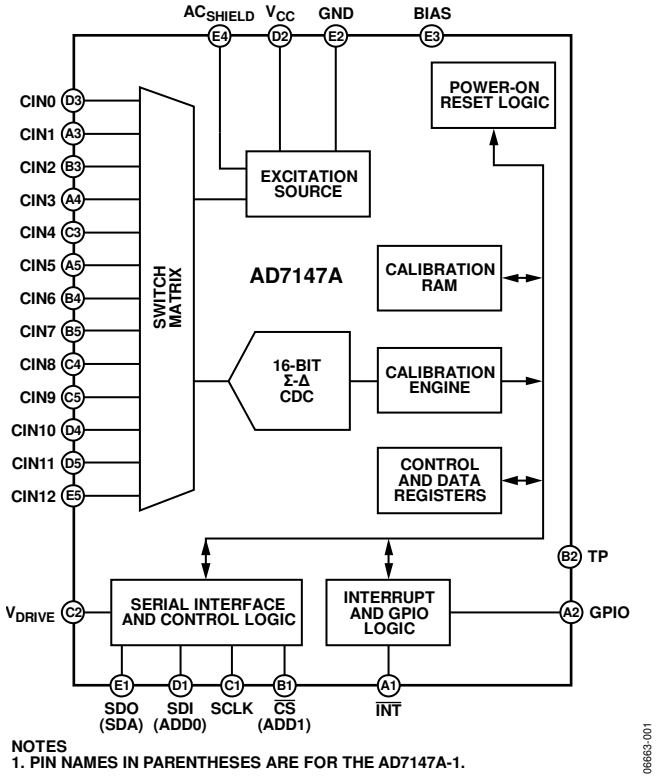


*Figure 1.*

The AD7147A is designed for single electrode capacitance sensors (grounded sensors). There is an active shield output to minimize noise pickup in the sensor.

The AD7147A has on-chip calibration logic to compensate for changes in the ambient environment. The calibration sequence is performed automatically and at continuous intervals as long as the sensors are not touched. This ensures that there are no false or nonregistering touches on the external sensors due to a changing environment.

The AD7147A has an SPI-compatible serial interface, and the AD7147A-1 has an I²C®-compatible serial interface. Both parts have an interrupt output, as well as a GPIO. There is a $V_{DRIVE}$ pin to set the voltage level for the serial interface independent of $V_{CC}$.

The AD7147A is available in a 25-ball, 2.3 mm × 2.1 mm WLCSP and operates from a 2.6 V to 3.6 V supply. The operating current consumption in low power mode is typically 28.96 µA for 13 sensors.

**Rev. B**



**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700** **www.analog.com**
**Fax: 781.461.3113** 

# AD7147A* PRODUCT PAGE QUICK LINKS

**Last Content Update: 02/23/2017**

## COMPARABLE PARTS

View a parametric search of comparable parts.

## DOCUMENTATION

**Application Notes**

- AN-925: Sensors for the AD7147 and AD7148 CapTouch® Controllers
- AN-929: Tuning the AD714x for CapTouch® Applications

**Data Sheet**

- AD7147A: CapTouch Programmable Controller for Single-Electrode Capacitance Sensors Data Sheet

## SOFTWARE AND SYSTEMS REQUIREMENTS

- AD714X Input CapTouchÂ® Programmable Controller Linux Driver

## DESIGN RESOURCES

- AD7147A Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all AD7147A EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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Changes to Ordering Guide ... 68

**3/09—Rev. 0 to Rev. A**

Changes to Ordering Guide ... 68

**1/09—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{CC}$ = 2.6 V to 3.6 V, $T_A$ = −40°C to +85°C, unless otherwise noted.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| CAPACITANCE-TO-DIGITAL CONVERTER | | | | | |
| Update Rate | 8.73 | 9 | 9.27 | ms | 12 conversion stages, decimation = 64 |
| | 17.46 | 18 | 18.54 | ms | 12 conversion stages, decimation = 128 |
| | 34.9 | 36 | 37.1 | ms | 12 conversion stages, decimation = 256 |
| Resolution | | 16 | | Bits | |
| CINx Input Range | | ±8 | | pF | |
| No Missing Codes | 16 | | | Bits | Guaranteed by design, but not production tested |
| CINx Input Leakage | | 25 | | nA | |
| Maximum Output Load | | | 20 | pF | Capacitance load on CINx to ground |
| Total Unadjusted Error | | | ±20 | % | |
| Output Noise (Peak-to-Peak) | | 12 | | Codes | Decimation rate = 64 |
| | | 7 | | Codes | Decimation rate = 128 |
| | | 3 | | Codes | Decimation rate = 256 |
| Output Noise (RMS) | | 1.1 | | Codes | Decimation rate = 64 |
| | | 0.8 | | Codes | Decimation rate = 128 |
| | | 0.5 | | Codes | Decimation rate = 256 |
| $C_{STRAY}$ Offset Range | | 20 | | pF | |
| $C_{STRAY}$ Offset Resolution | | 0.32 | | pF | |
| Low Power Mode Delay Accuracy | | | 4 | % | Percentage of 200 ms, 400 ms, 600 ms, or 800 ms |
| $AC_{SHIELD}$ | | | | | |
| Frequency | | 250 | | kHz | |
| Output Voltage | 0 | | $V_{CC}$ | V | Oscillating |
| Short-Circuit Source Current | | 10 | | mA | |
| Short-Circuit Sink Current | | 10 | | mA | |
| Maximum Output Load | | | 150 | pF | Capacitance load on $AC_{SHIELD}$ to ground |
| LOGIC INPUTS (SDI, SCLK, $\overline{CS}$, SDA, GPIO) | | | | | |
| Input High Voltage, $V_{IH}$ | 0.7 × $V_{DRIVE}$ | | | V | |
| Input Low Voltage, $V_{IL}$ | | | 0.4 | V | |
| Input High Current, $I_{IH}$ | −1 | | | µA | $V_{IN}$ = $V_{DRIVE}$ |
| Input Low Current, $I_{IL}$ | | | 1 | µA | $V_{IN}$ = GND |
| Hysteresis | | 150 | | mV | |
| OPEN-DRAIN OUTPUTS (SCLK, SDA, $\overline{INT}$) | | | | | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | $I_{SINK}$ = −1 mA |
| Output High Leakage Current, $I_{OH}$ | | ±0.1 | ±1 | µA | $V_{OUT}$ = $V_{DRIVE}$ |
| LOGIC OUTPUTS (SDO, GPIO) | | | | | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | $I_{SINK}$ = 1 mA, $V_{DRIVE}$ = 1.65 V to 3.6 V |
| Output High Voltage, $V_{OH}$ | $V_{DRIVE}$ − 0.6 | | | V | $I_{SOURCE}$ = 1 mA, $V_{DRIVE}$ = 1.65 V to 3.6 V |
| GPO, SDO Floating State Leakage Current | | | ±1 | µA | Pin three-state, leakage measured to GND and $V_{CC}$ |
| POWER | | | | | |
| $V_{CC}$ | 2.6 | 3.3 | 3.6 | V | |
| $V_{DRIVE}$ | 1.65 | | 3.6 | V | Serial interface operating voltage |
| $I_{CC}$ | | 0.8 | 1 | mA | In full power mode, $V_{CC}$ + $V_{DRIVE}$, Register 0x00, Bits[15:14] = 00 |
| | | 1.1 | 1.3 | mA | In full power mode, $V_{CC}$ + $V_{DRIVE}$, Register 0x00, Bits[15:14] = 01 |
| | | 1.2 | 1.5 | mA | In full power mode, $V_{CC}$ + $V_{DRIVE}$, Register 0x00, Bits[15:14] = 10 |
| | | 1.6 | 1.8 | mA | In full power mode, $V_{CC}$ + $V_{DRIVE}$, Register 0x00, Bits[15:14] = 11 |
| | | 15.5 | 24 | µA | Low power mode, converter idle, $V_{CC}$ + $V_{DRIVE}$, decimation = 256; Register 0x00, Bits[15:14] = 01 |
| | | 2.3 | 10 | µA | Full shutdown, $V_{CC}$ + $V_{DRIVE}$, Register 0x00, Bits[15:14] = 01 |

## AVERAGE CURRENT SPECIFICATIONS

**Table 2. Typical Average Current in Low Power Mode[1]**

| Low Power Mode Delay | Decimation Rate | Current Values of Conversion Stages (μA) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| 200 ms | 64 | 22.27 | 26.53 | 30.77 | 34.98 | 39.15 | 43.29 | 47.40 | 51.48 | 55.53 | 59.55 | 63.54 | 67.51 |
| | 128 | 27.95 | 36.37 | 44.66 | 52.84 | 60.89 | 68.82 | 76.64 | 84.34 | 91.94 | 99.42 | 106.80 | 114.08 |
| | 256 | 39.15 | 55.53 | 71.44 | 86.89 | 101.9 | 116.48 | 130.67 | 144.47 | 157.90 | 170.98 | 183.71 | 196.11 |
| 400 ms | 64 | 18.89 | 21.04 | 23.19 | 25.32 | 27.45 | 29.57 | 31.68 | 33.78. | 35.88 | 37.96 | 40.04 | 42.11 |
| | 128 | 21.76 | 26.03 | 30.27 | 34.48 | 38.66 | 42.80 | 46.92 | 51.00 | 55.05 | 59.08 | 63.07 | 67.04 |
| | 256 | 27.45 | 35.88 | 44.18 | 52.36 | 60.41 | 68.35 | 76.18 | 83.89 | 91.49 | 98.98 | 106.37 | 113.65 |
| 600 ms | 64 | 17.76 | 19.20 | 20.63 | 22.06 | 23.49 | 24.91 | 26.33 | 27.75 | 29.16 | 30.57 | 31.98 | 33.38 |
| | 128 | 19.68 | 22.54 | 25.39 | 28.22 | 31.04 | 33.85 | 36.64 | 39.42 | 42.18 | 44.93 | 47.67 | 50.39 |
| | 256 | 23.49 | 29.16 | 34.78 | 40.34 | 45.84 | 51.29 | 56.69 | 62.03 | 67.32 | 72.56 | 77.75 | 82.89 |
| 800 ms | 64 | 17.20 | 18.28 | 19.35 | 20.43 | 21.50 | 22.57 | 23.64 | 24.71 | 25.78 | 26.84 | 27.90 | 28.96 |
| | 128 | 18.63 | 20.79 | 22.93 | 25.07 | 27.20 | 29.32 | 31.43 | 33.53 | 35.63 | 37.72 | 39.80 | 41.87 |
| | 256 | 21.50 | 25.78 | 30.02 | 34.23 | 38.41 | 42.56 | 46.67 | 50.76 | 54.82 | 58.84 | 62.84 | 66.80 |

[1] $V_{CC}$ = 3.3 V, $T_A$ = 25°C, load = 50 pF.

**Table 3. Maximum Average Current in Low Power Mode[1]**

| Low Power Mode Delay | Decimation Rate | Current Values of Conversion Stages (μA) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| 200 ms | 64 | 32.62 | 38.12 | 43.58 | 48.99 | 54.35 | 59.67 | 64.95 | 70.18 | 75.37 | 80.52 | 85.63 | 90.69 |
| | 128 | 39.95 | 50.78 | 61.44 | 71.92 | 82.23 | 92.37 | 102.36 | 112.18 | 121.85 | 131.27 | 140.74 | 149.97 |
| | 256 | 54.35 | 75.37 | 95.72 | 115.42 | 134.51 | 153.02 | 170.96 | 188.38 | 205.28 | 221.70 | 237.65 | 253.15 |
| 400 ms | 64 | 28.32 | 31.10 | 33.86 | 36.61 | 39.35 | 42.08 | 44.80 | 47.50 | 50.19 | 52.88 | 55.55 | 58.21 |
| | 128 | 32.02 | 37.53 | 42.99 | 48.40 | 53.77 | 59.09 | 64.38 | 69.61 | 74.81 | 79.96 | 85.07 | 90.14 |
| | 256 | 39.35 | 50.19 | 60.86 | 71.35 | 81.67 | 91.82 | 101.82 | 111.65 | 121.33 | 130.86 | 140.24 | 149.47 |
| 600 ms | 64 | 26.88 | 28.74 | 30.59 | 32.43 | 34.27 | 36.11 | 37.94 | 39.76 | 41.58 | 43.39 | 45.20 | 47.00 |
| | 128 | 29.36 | 33.05 | 36.72 | 40.37 | 44.00 | 47.60 | 51.19 | 54.76 | 58.31 | 61.84 | 65.35 | 68.84 |
| | 256 | 34.27 | 41.58 | 48.80 | 55.95 | 63.01 | 70.00 | 76.92 | 83.76 | 90.52 | 97.21 | 103.83 | 110.39 |
| 800 ms | 64 | 26.16 | 27.56 | 28.95 | 30.33 | 31.72 | 33.10 | 34.48 | 35.85 | 37.23 | 38.60 | 39.96 | 41.33 |
| | 128 | 28.02 | 30.80 | 33.56 | 36.31 | 39.05 | 41.78 | 44.50 | 47.21 | 49.90 | 52.59 | 55.26 | 57.92 |
| | 256 | 31.72 | 37.23 | 42.69 | 48.11 | 53.48 | 58.80 | 64.09 | 69.33 | 74.53 | 79.68 | 84.80 | 89.87 |

[1] $V_{CC}$ = 3.6 V, $T_A$ = −40°C to +85°C, load = 50 pF.

## SPI TIMING SPECIFICATIONS (AD7147A)

$T_A$ = −40°C to +85°C, sample tested at 25°C to ensure compliance. $V_{DRIVE}$ = 1.65 V to 3.6 V, and $V_{CC}$ = 2.6 V to 3.6 V, unless otherwise noted. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of $V_{CC}$) and timed from a voltage level of 1.6 V.

**Table 4. SPI Timing Specifications**

| Parameter | Limit | Unit | Description |
|---|---|---|---|
| $f_{SCLK}$ | 5 | MHz max | SCLK frequency |
| $t_1$ | 5 | ns min | $\overline{CS}$ falling edge to first SCLK falling edge |
| $t_2$ | 20 | ns min | SCLK high pulse width |
| $t_3$ | 20 | ns min | SCLK low pulse width |
| $t_4$ | 15 | ns min | SDI setup time |
| $t_5$ | 15 | ns min | SDI hold time |
| $t_6$ | 20 | ns max | SDO access time after SCLK falling edge |
| $t_7$ | 16 | ns max | $\overline{CS}$ rising edge to SDO high impedance |
| $t_8$ | 15 | ns min | SCLK rising edge to $\overline{CS}$ high |

### *SPI Timing Diagram*

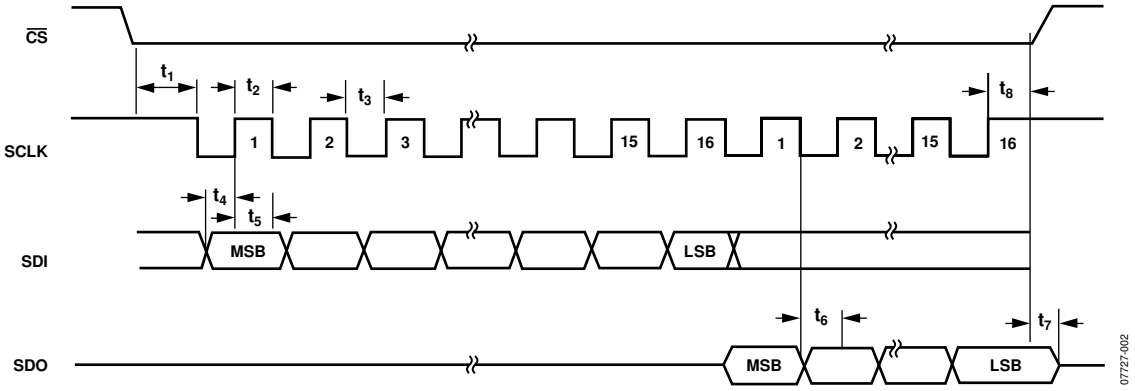



*Figure 2. SPI Detailed Timing Diagram*

## I²C TIMING SPECIFICATIONS (AD7147A-1)

$T_A$ = −40°C to +85°C, sample tested at 25°C to ensure compliance. $V_{DRIVE}$ = 1.65 V to 3.6 V, and $V_{CC}$ = 2.6 V to 3.6 V, unless otherwise noted. All input signals timed from a voltage level of 1.6 V.

**Table 5. I²C Timing Specifications**[1]

| Parameter | Limit | Unit | Description |
|---|---|---|---|
| $f_{SCLK}$ | 400 | kHz max | |
| $t_1$ | 0.6 | µs min | Start condition hold time, $t_{HD; STA}$ |
| $t_2$ | 1.3 | µs min | Clock low period, $t_{LOW}$ |
| $t_3$ | 0.6 | µs min | Clock high period, $t_{HIGH}$ |
| $t_4$ | 100 | ns min | Data setup time, $t_{SU; DAT}$ |
| $t_5$ | 300 | ns min | Data hold time, $t_{HD; DAT}$ |
| $t_6$ | 0.6 | µs min | Stop condition setup time, $t_{SU; STO}$ |
| $t_7$ | 0.6 | µs min | Start condition setup time, $t_{SU; STA}$ |
| $t_8$ | 1.3 | µs min | Bus-free time between stop and start conditions, $t_{BUF}$ |
| $t_R$ | 300 | ns max | Clock/data rise time |
| $t_F$ | 300 | ns max | Clock/data fall time |

[1] Guaranteed by design, not production tested.

### *I²C Timing Diagram*

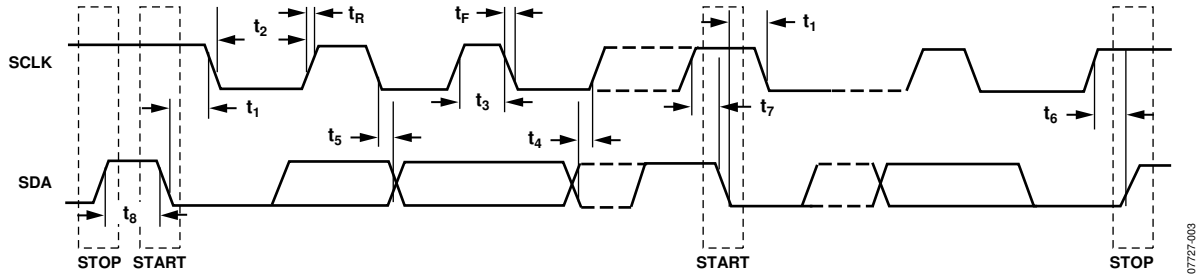



*Figure 3. I²C Detailed Timing Diagram*

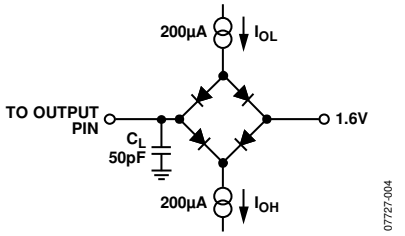



*Figure 4. Load Circuit for Digital Output Timing Specifications*

# ABSOLUTE MAXIMUM RATINGS

**Table 6.**

| Parameter | Rating |
|---|---|
| $V_{CC}$ to GND | −0.3 V to +3.6 V |
| Analog Input Voltage to GND | −0.3 V to $V_{CC}$ + 0.3 V |
| Digital Input Voltage to GND | −0.3 V to $V_{DRIVE}$ + 0.3 V |
| Digital Output Voltage to GND | −0.3 V to $V_{DRIVE}$ + 0.3 V |
| Input Current to Any Pin Except Supplies[1] | 10 mA |
| ESD Rating | |
| BIAS and $AC_{SHIELD}$ Pins (HBM Contact and Air Discharge) | 8 kV |
| All Other Pins (HBM Contact) | 2 kV |
| Operating Temperature Range | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| WLCSP | |
| Power Dissipation | 1 W |
| $\theta_{JA}$ Thermal Impedance | 65°C/W |
| IR Reflow Peak Temperature | 260°C (± 0.5°C) |
| Lead Temperature (Soldering, 10 sec) | 300°C |

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

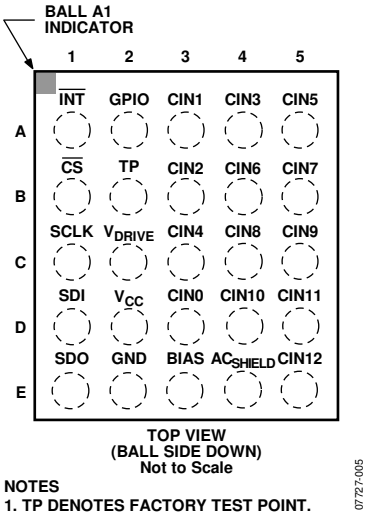



*Figure 5. AD7147A Pin Configuration*

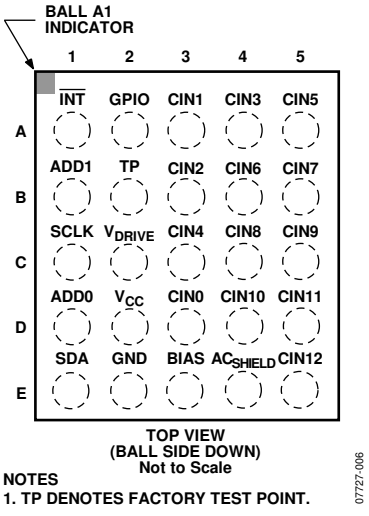



*Figure 6. AD7147A-1 Pin Configuration*

**Table 7. Pin Function Descriptions**

| Pin No. | | | |
|---|---|---|---|
| **AD7147A** | **AD7147A-1** | **Mnemonic** | **Description** |
| B4 | B4 | CIN6 | Capacitance Sensor Input. |
| B5 | B5 | CIN7 | Capacitance Sensor Input. |
| C4 | C4 | CIN8 | Capacitance Sensor Input. |
| C5 | C5 | CIN9 | Capacitance Sensor Input. |
| D4 | D4 | CIN10 | Capacitance Sensor Input. |
| D5 | D5 | CIN11 | Capacitance Sensor Input. |
| E5 | E5 | CIN12 | Capacitance Sensor Input. |
| E4 | E4 | $AC_{SHIELD}$ | CDC Active Shield Output. Connect to external shield or plane. |
| E3 | E3 | BIAS | Bias Node for Internal Circuitry. Requires 100 nF capacitor to ground. |
| E2 | E2 | GND | Ground Reference Point for All Circuitry. |
| D2 | D2 | $V_{CC}$ | Supply Voltage. |
| C2 | C2 | $V_{DRIVE}$ | Serial Interface Operating Voltage Supply. |
| E1 | N/A | SDO | SPI Serial Data Output. |
| N/A | E1 | SDA | $I^2C$ Serial Data Input/Output. SDA requires pull-up resistor. |
| D1 | N/A | SDI | SPI Serial Data Input. |
| N/A | D1 | ADD0 | $I^2C$ Address Bit 0. |
| C1 | C1 | SCLK | Clock Input for Serial Interface. |
| B1 | N/A | $\overline{CS}$ | SPI Chip Select Signal. |
| N/A | B1 | ADD1 | $I^2C$ Address Bit 1. |
| A1 | A1 | $\overline{INT}$ | General-Purpose Open-Drain Interrupt Output. Programmable polarity; requires pull-up resistor. |
| A2 | A2 | GPIO | Programmable General-Purpose Input/Output. |
| D3 | D3 | CIN0 | Capacitance Sensor Input. |
| A3 | A3 | CIN1 | Capacitance Sensor Input. |
| B3 | B3 | CIN2 | Capacitance Sensor Input. |
| A4 | A4 | CIN3 | Capacitance Sensor Input. |
| C3 | C3 | CIN4 | Capacitance Sensor Input. |
| A5 | A5 | CIN5 | Capacitance Sensor Input. |
| B2 | B2 | | Factory Test Point Only. Tie to ground. |

# TYPICAL PERFORMANCE CHARACTERISTICS

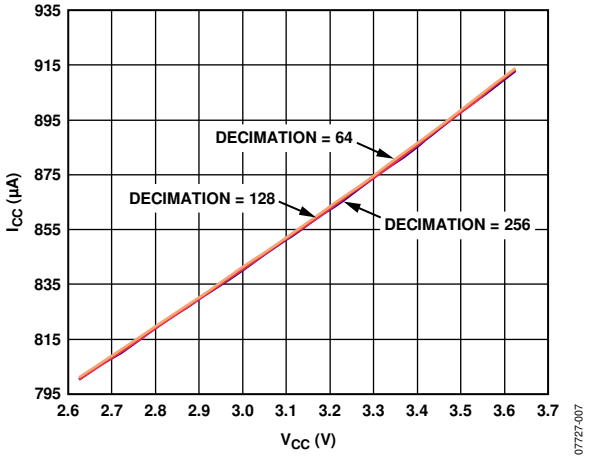



Figure 7. Supply Current vs. Supply Voltage

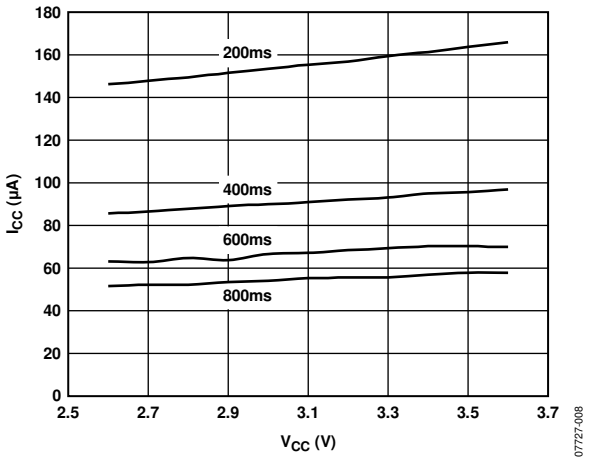



Figure 8. Low Power Supply Current vs. Supply Voltage, Decimation Rate = 256

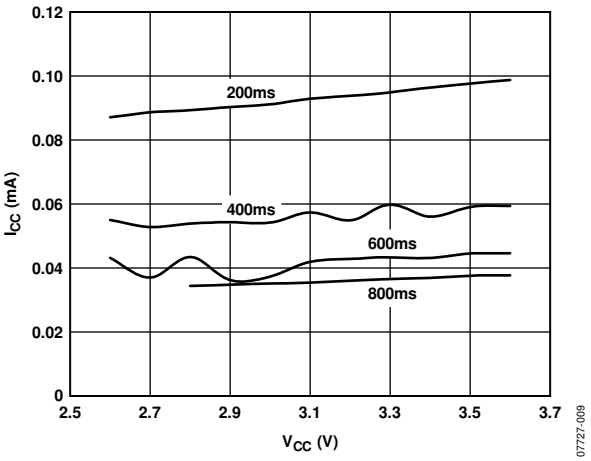



Figure 9. Low Power Supply Current vs. Supply Voltage, Decimation Rate = 128

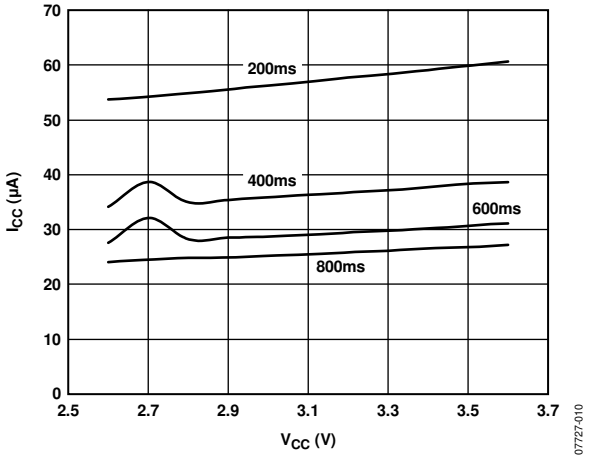



Figure 10. Low Power Supply Current vs. Supply Voltage, Decimation Rate = 64

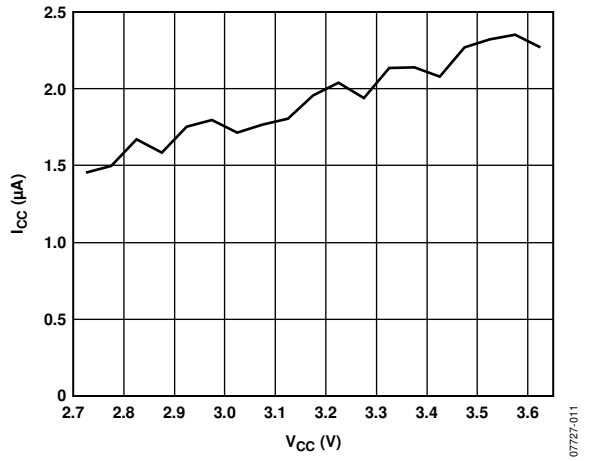



Figure 11. Shutdown Supply Current vs. Supply Voltage

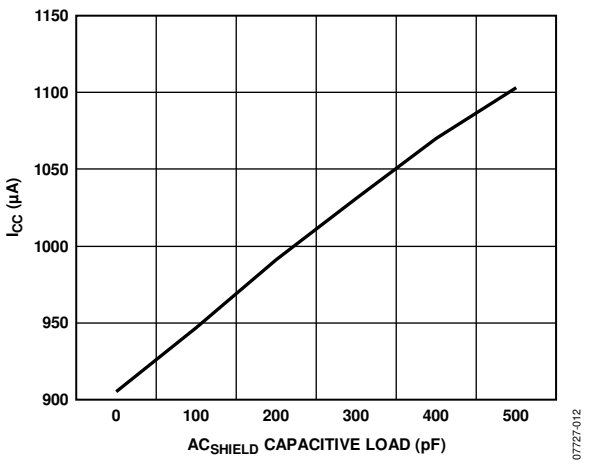



Figure 12. Supply Current vs. Capacitive Load on $AC_{SHIELD}$

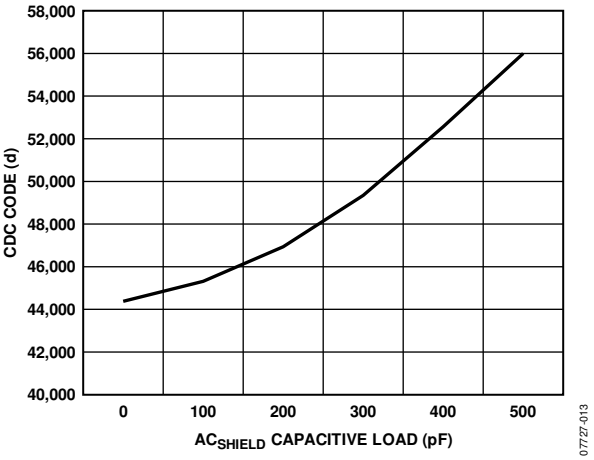



Figure 13. CDC Code vs. Capacitive Load on $AC_{SHIELD}$

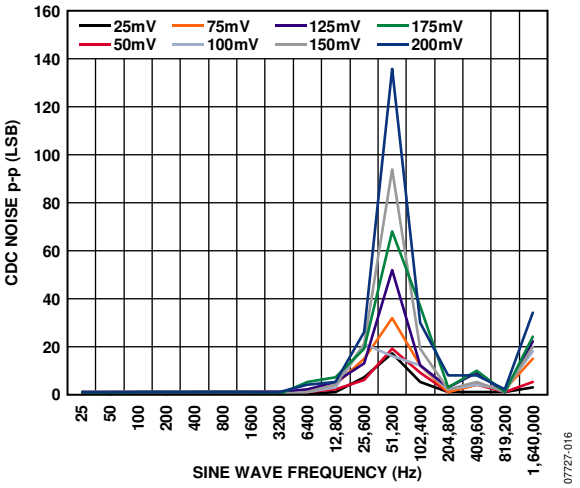



Figure 16. Power Supply Sine Wave Rejection, $V_{CC}$ = 3.6 V

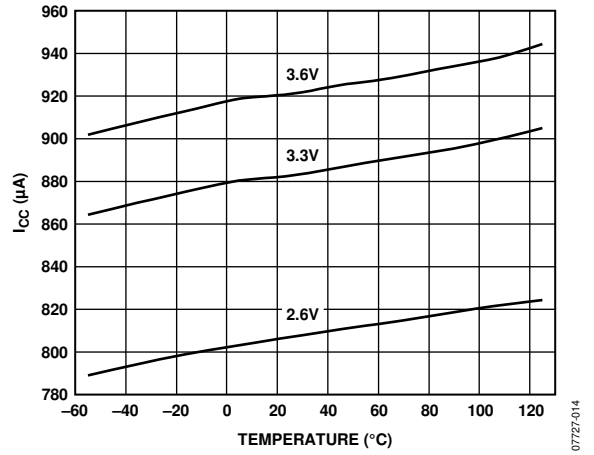



Figure 14. Supply Current vs. Temperature

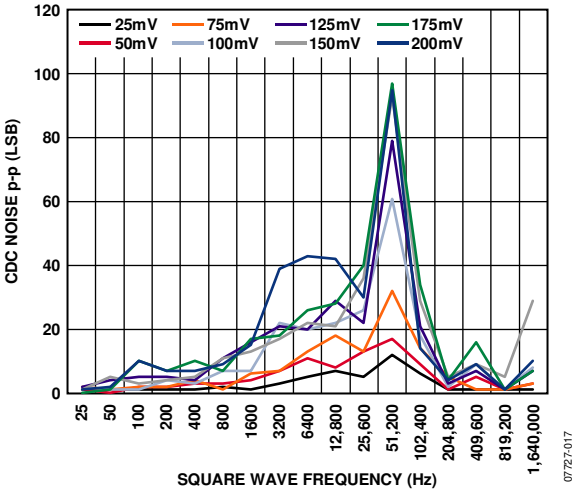



Figure 17. Power Supply Square Wave Rejection, $V_{CC}$ = 3.6 V

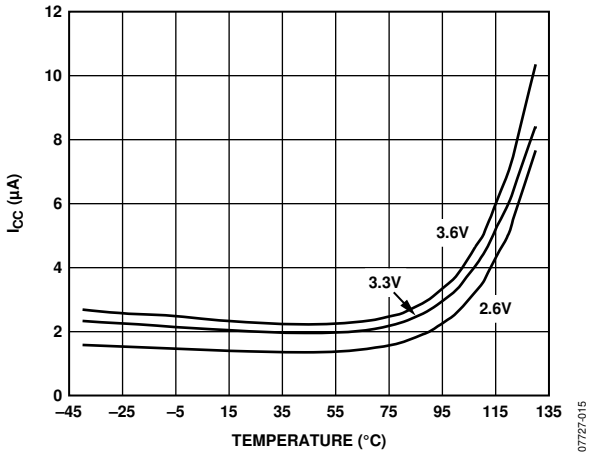



Figure 15. Shutdown Supply Current vs. Temperature

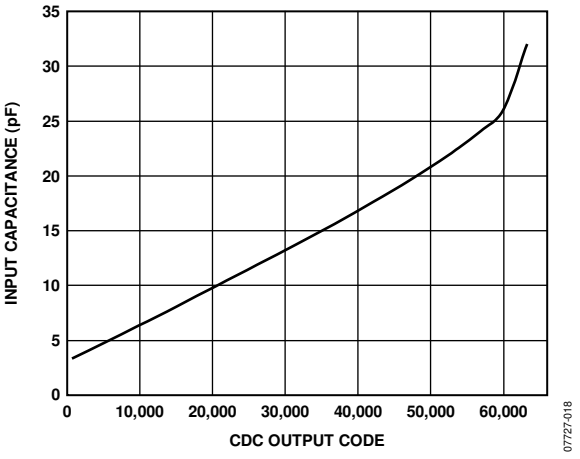



Figure 18. CDC Linearity, $V_{CC}$ = 3.3 V

# THEORY OF OPERATION

The AD7147A and AD7147A-1 are CDCs with on-chip environmental compensation. They are intended for use in portable systems requiring high resolution user input. The internal circuitry consists of a 16-bit, Σ-Δ converter that can change a capacitive input signal into a digital value. There are 13 input pins, CIN0 to CIN12. A switch matrix routes the input signals to the CDC. The result of each capacitance-to-digital conversion is stored in on-chip registers. The host subsequently reads the results over the serial interface. The AD7147A has an SPI interface, and the AD7147A-1 has an $I^2C$ interface, ensuring that the parts are compatible with a wide range of host processors. AD7147A refers to both the AD7147A and AD7147A-1, unless otherwise noted, from this point forward in this data sheet.

The AD7147A interfaces with up to 13 external capacitance sensors. These sensors can be arranged as buttons, scroll bars, or wheels, or as a combination of sensor types. The external sensors consist of an electrode on a single- or multiple-layer PCB that interfaces directly to the AD7147A.

The AD7147A can be set up to implement any set of input sensors by programming the on-chip registers. The registers can also be programmed to control features such as averaging, offsets, and gains for each of the external sensors. There is an on-chip sequencer that controls how each of the capacitance inputs is polled.

The AD7147A has on-chip digital logic and 528 words of RAM that are used for environmental compensation. The effects of humidity, temperature, and other environmental factors can affect the operation of capacitance sensors. Transparent to the user, the AD7147A performs continuous calibration to compensate for these effects, allowing the AD7147A to consistently provide error-free results.

The AD7147A requires a companion algorithm that runs on the host or another microcontroller to implement high resolution sensor functions, such as scroll bars or wheels. However, no companion algorithm is required to implement buttons. Button sensors are implemented on chip, entirely in digital logic.

The AD7147A can be programmed to operate in either full power mode or low power automatic wake-up mode. The automatic wake-up mode is particularly suited for portable devices that require low power operation to provide the user with significant power savings and full functionality.

The AD7147A has an interrupt output, $\overline{\text{INT}}$, to indicate when new data has been placed into the registers. $\overline{\text{INT}}$ is used to interrupt the host on sensor activation. The AD7147A operates from a 2.6 V to 3.6 V supply and is available in a 2.3 mm × 2.1 mm WLCSP.

## CAPACITANCE SENSING THEORY

The AD7147A measures capacitance changes from single electrode sensors. The sensor electrode on the PCB comprises one plate of a virtual capacitor. The other plate of the capacitor is the user's finger, which is grounded with respect to the sensor input.

The AD7147A first outputs an excitation signal to charge the plate of the capacitor. When the user comes close to the sensor, the virtual capacitor is formed, with the user acting as the second capacitor plate.

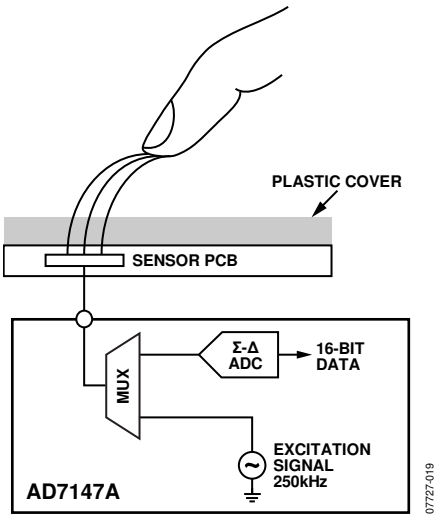



*Figure 19. Capacitance-Sensing Method*

A square wave excitation signal is applied to CINx during the conversion, and the modulator continuously samples the charge going through CINx. The output of the modulator is processed via a digital filter, and the resulting digital data is stored in the CDC_RESULT_Sx registers for each conversion stage, at Address 0x00B to Address 0x016.

### *Registering a Sensor Activation*

When a user approaches a sensor, the total capacitance associated with that sensor changes and is measured by the AD7147A. If the change causes a set threshold to be exceeded, the AD7147A interprets this as a sensor activation.

On-chip threshold limits are used to determine when a sensor activation occurs. Figure 20 shows the change in CDC_RESULT_Sx when a user activates a sensor. The sensor is deemed to be active only when the value of CDC_RESULT_Sx is either greater than the value of STAGEx_HIGH_THRESHOLD or less than the value of STAGEx_LOW_THRESHOLD.

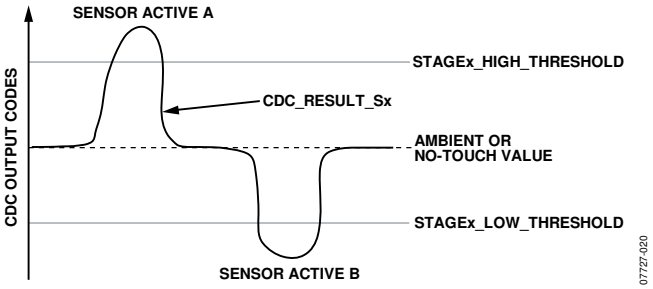



*Figure 20. Sensor Activation Thresholds*

In Figure 20, two sensor activations are shown. Sensor Active A occurs when a sensor is connected to the positive input of the converter. In this case, when a user activates the sensor, there is an increase in CDC code, and the value of CDC_RESULT_Sx exceeds that of STAGEx_HIGH_THRESHOLD. Sensor Active B occurs when the sensor is connected to the negative input of the converter. In this case, when a user activates the sensor, there is a decrease in CDC code, and the value of CDC_RESULT_Sx becomes less than the value of STAGEx_LOW_THRESHOLD.

For each conversion stage, the STAGEx_HIGH_THRESHOLD and STAGEx_LOW_THRESHOLD registers are in Bank 3. The values in these registers are updated automatically by the AD7147A due to its environmental calibration and adaptive threshold logic.

At power-up, the values in the STAGEx_HIGH_THRESHOLD and STAGEx_LOW_THRESHOLD registers are the same as those in the STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW registers in Bank 2. The user must program the STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW registers on device power-up. See the Environmental Calibration section of the data sheet for more information.

### *Complete Solution for Capacitance Sensing*

Analog Devices, Inc., provides a complete solution for capacitance sensing. The two main elements to the solution are the sensor PCB and the AD7147A.

If the application requires high resolution sensors such as scroll bars or wheels, software that runs on the host processor is required. The memory requirements for the host depend on the sensor and are typically 10 kB of code and 600 bytes of data memory, depending on the sensor type.

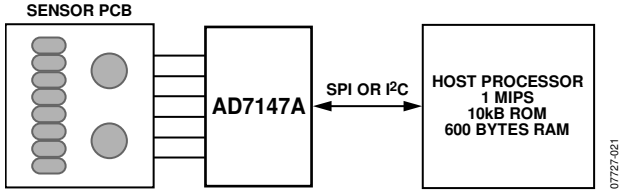



*Figure 21. Three-Part Capacitance Sensing Solution*

Analog Devices supplies the sensor PCB footprint design libraries to the customer and supplies any necessary software on an open-source basis.

## BIAS PIN

This pin is connected internally to a bias node of the AD7147A. To ensure correct operation of the AD7147A, connect a 100 nF capacitor between the BIAS pin and ground. The voltage seen at the BIAS pin is $V_{CC}/2$.

## OPERATING MODES

The AD7147A has three operating modes. Full power mode, where the device is always fully powered, is suited for applications where power is not a concern (for example, game consoles that have an ac power supply). Low power mode, where the part automatically powers down when no sensor is active, is tailored to provide significant power savings compared with full power mode and is suited for mobile applications, where power must be conserved. In shutdown mode, the part shuts down completely.

The POWER_MODE Bits[1:0] of the power control register (PWR_CONTROL, Address 0x000) set the operating mode on the AD7147A. Table 8 shows the POWER_MODE settings for each operating mode. To put the AD7147A into shutdown mode, set the POWER_MODE bits to either 01 or 11.

**Table 8. POWER_MODE Settings**

| POWER_MODE Bits | Operating Mode |
|---|---|
| 00 | Full power mode |
| 01 | Shutdown mode |
| 10 | Low power mode |
| 11 | Shutdown mode |

The power-on default setting of the POWER_MODE bits is 00, full power mode.

### Full Power Mode

In full power mode, all sections of the AD7147A remain fully powered and converting at all times. While a sensor is being touched, the AD7147A processes the sensor data. If no sensor is touched, the AD7147A measures the ambient capacitance level and uses this data for the on-chip compensation routines. In full power mode, the AD7147A converts at a constant rate. See the CDC Conversion Sequence Time section for more information.

### Low Power Mode

When AD7147A is in low power mode, the POWER_MODE bits are set to 10 upon device initialization. If the external sensors are not touched, the AD7147A reduces its conversion frequency, thereby greatly reducing its power consumption. The part remains in a reduced power state while the sensors are not touched. The AD7147A performs a conversion after a delay defined by the LP_CONV_DELAY bits, and it uses this data to update the compensation logic and check if the sensors are active. The LP_CONV_DELAY bits set the delay between conversions to 200 ms, 400 ms, 600 ms, or 800 ms.

In low power mode, the total current consumption of the AD7147A is an average of the current used during a conversion and the current used while the AD7147A is waiting for the next conversion to begin. For example, when LP_CONV_DELAY is 400 ms, the AD7147A typically uses 0.85 mA of current for 36 ms and 14 μA of current for 400 ms during the conversion interval. (Note that these conversion timings can be altered through the register settings. See the CDC Conversion Sequence Time section for more information.)

The time for the AD7147A to transition from a full power state to a reduced power state after the user stops touching the external sensors is configurable. The PWR_DOWN_TIMEOUT bits in the Ambient Compensation Control 0 register (AMB_COMP_CTRL0, Address 0x002) control the time delay before the AD7147A transitions to the reduced power state after the user stops touching the sensors.

### Low Latency from Touch to Response

In low power mode, the AD7147A remains in a low power state until proximity is detected on any one of the external sensors. When proximity is detected, the AD7147A begins a conversion sequence every 36 ms, or 18 ms, or 9 ms to read back data from the sensors. The latency between first touch and AD7147A response is greatly reduced compared to the AD7147 because the part is already in a full power state by the time the user touches the sensor.

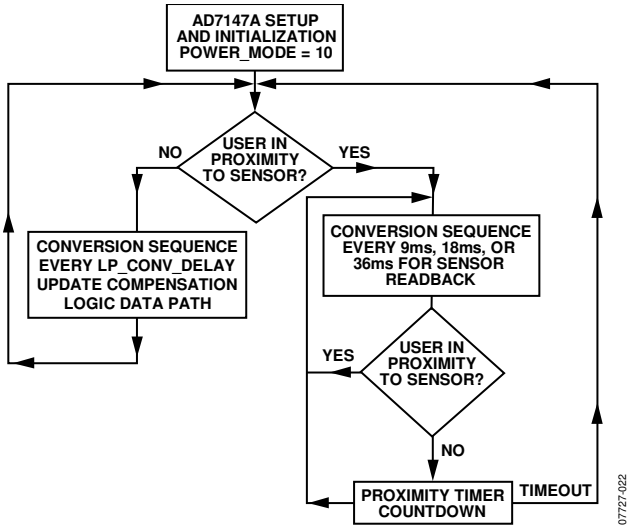



*Figure 22. Low Power Mode Operation, AD7147A*

# CAPACITANCE-TO-DIGITAL CONVERTER

The capacitance-to-digital converter on the AD7147A has a Σ-Δ architecture with 16-bit resolution. There are 13 possible inputs to the CDC that are connected to the input of the converter through a switch matrix. The sampling frequency of the CDC is 250 kHz.

## OVERSAMPLING THE CDC OUTPUT

The decimation rate, or oversampling ratio, is determined by Bits[9:8] of the power control register (PWR_CONTROL, Address 0x000), as listed in Table 9.

**Table 9. CDC Decimation Rate**

| Decimation Bits | Decimation Rate | CDC Output Rate Per Stage (ms) |
|---|---|---|
| 00 | 256 | 3.072 |
| 01 | 128 | 1.536 |
| 10 | 64 | 0.768 |
| 11 | 64 | 0.768 |

The decimation process on the AD7147A is an averaging process, where a number of samples are taken and the averaged result is output. Due to the architecture of the digital filter employed, the number of samples taken (per stage) is equal to 3× the decimation rate. So 3 × 256 or 3 × 128 samples are averaged to obtain each stage result.

The decimation process reduces the amount of noise present in the final CDC result. However, the higher the decimation rate, the lower the output rate per stage; therefore, there is a trade-off possible between the amount of noise in the signal and the speed of sampling.

## CAPACITANCE SENSOR OFFSET CONTROL

There are two programmable DACs on board the AD7147A to null the effect of any stray capacitances on the CDC measurement. These offsets are due to stray capacitance to ground.

A simplified block diagram in Figure 23 shows how to apply the STAGEx_AFE_OFFSET registers to null the offsets. The POS_AFE_OFFSET and NEG_AFE_OFFSET bits (Bits[13:8] and Bits[5:0], respectively) program the offset DACs to provide 0.32 pF resolution offset adjustment over a range of 20 pF.

The best practice is to ensure that the CDC output for any stage is approximately equal to midscale (~32,700) when all sensors are inactive. To correctly offset the stray capacitance to ground for each stage, use the following procedure:

1. Read back the CDC value from the CDC_RESULT_Sx register.
2. If this value is not close to midscale, increase the value of POS_AFE_OFFSET or NEG_AFE_OFFSET (depending on if the CINx input is connected to the positive or negative input of the converter) by 1. The CINx connections are determined by the STAGEx_CONNECTION registers.
3. If the CDC value in CDC_RESULT_Sx is now closer to midscale, repeat Step 2. If the CDC value is further from midscale, decrease the POS_AFE_OFFSET or NEG_AFE_OFFSET value by 1.

The goal is to ensure that the CDC_RESULT_Sx is as close to midscale as possible. This process is required only once during the initial capacitance sensor characterization.

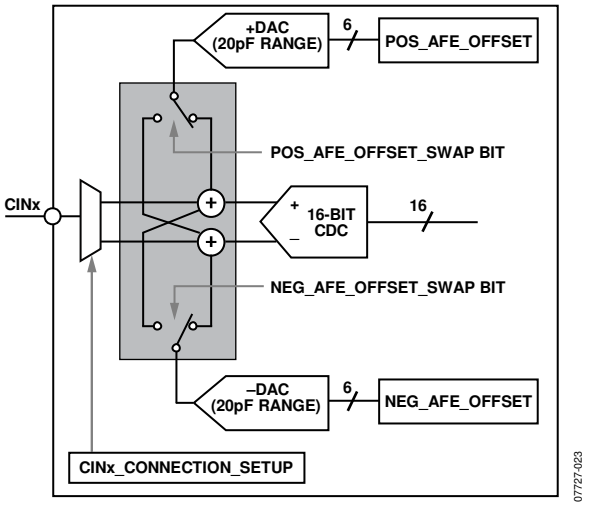



*Figure 23. Analog Front-End Offset Control*

## CONVERSION SEQUENCER

The AD7147A has an on-chip sequencer to implement conversion control for the input channels. Up to 12 conversion stages can be performed in one sequence. Each of the 12 conversions stages can measure the input from a different sensor. By using the Bank 2 registers, each stage can be uniquely configured to support multiple capacitance sensor interface requirements. For example, a slider sensor can be assigned to STAGE1 through STAGE8, with a button sensor assigned to STAGE0. For each conversion stage, the input mux that connects the CINx inputs to the converter can have a unique setting.

The AD7147A on-chip sequence controller provides conversion control, beginning with STAGE0. Figure 24 shows a block diagram of the CDC conversion stages and CINx inputs. A conversion sequence is defined as a sequence of CDC conversions starting at STAGE0 and ending at the stage determined by the value programmed in the SEQUENCE_STAGE_NUM bits (Bits[7:4], Address 0x00). Depending on the number and type of capacitance sensors that are used, not all conversion stages are required. Use the SEQUENCE_STAGE_NUM bits to set the number of conversions in one sequence. This number depends on the sensor interface requirements. For example, the register should be set to 5 if the CINx inputs are mapped to only six conversion stages. In addition, the STAGE_CAL_EN register (Address 0x001) should be set according to the number of stages that are used.

The number of required conversion stages depends solely on the number of sensors attached to the AD7147A. Figure 25 shows how many conversion stages are required for each sensor and how many inputs to the AD7147A each sensor requires.

A button sensor generally requires one sequencer stage; this is shown in Figure 25 as B1. However, it is possible to configure two button sensors to operate differentially for one conversion stage. Only one button can be activated at a time; pressing both buttons simultaneously results in neither button being activated. The configuration with two button sensors operating differentially requires one conversion stage and is shown in Figure 25, with B2 and B3 representing the differentially configured button sensors.

A wheel sensor requires eight stages, whereas a slider requires two stages. The result from each stage is used by the host software to determine the user's position on the slider or wheel. The algorithms that perform this process are available from Analog Devices and are free of charge but require signing a software license.

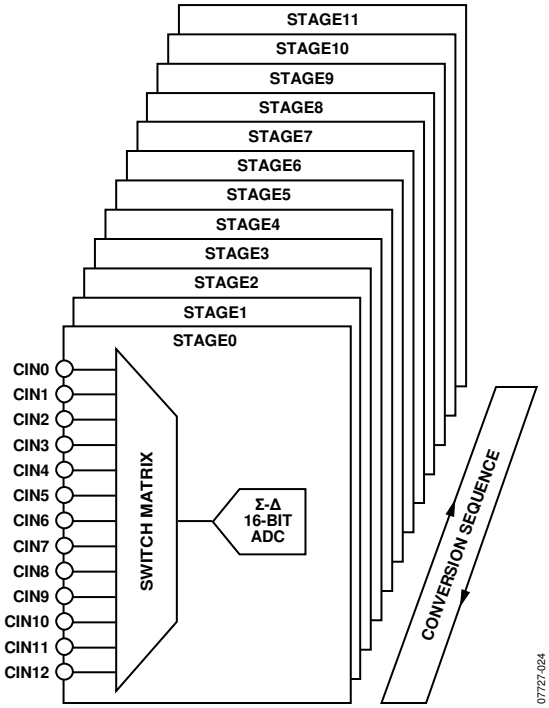



*Figure 24. CDC Conversion Stages*

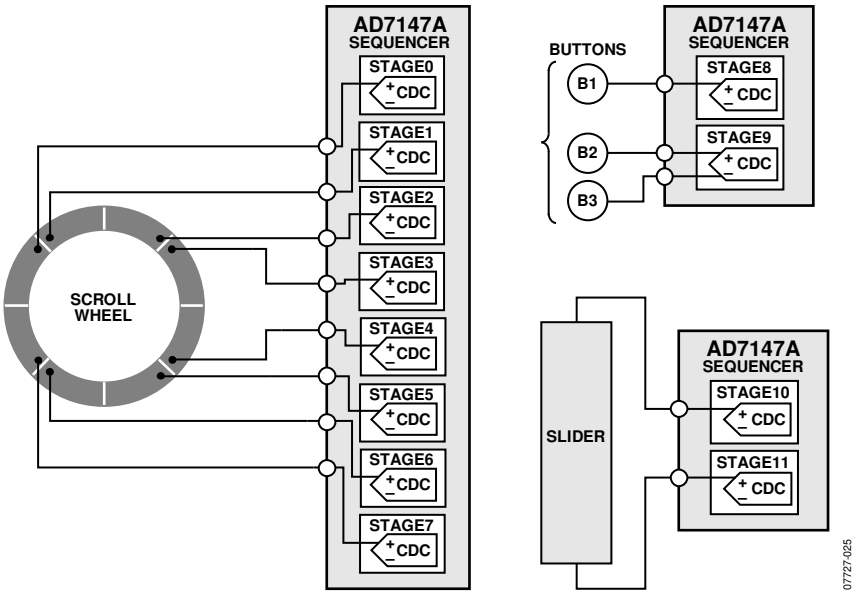



*Figure 25. Sequencer Setup for Sensors*

## CDC CONVERSION SEQUENCE TIME

**Table 10. CDC Conversion Times for Full Power Mode**

| | Conversion Time (ms) | | |
|---|---|---|---|
| **SEQUENCE_STAGE_NUM** | **Decimation = 64** | **Decimation = 128** | **Decimation = 256** |
| 0 | 0.768 | 1.536 | 3.072 |
| 1 | 1.536 | 3.072 | 6.144 |
| 2 | 2.304 | 4.608 | 9.216 |
| 3 | 3.072 | 6.144 | 12.288 |
| 4 | 3.84 | 7.68 | 15.36 |
| 5 | 4.608 | 9.216 | 18.432 |
| 6 | 5.376 | 10.752 | 21.504 |
| 7 | 6.144 | 12.288 | 24.576 |
| 8 | 6.912 | 13.824 | 27.648 |
| 9 | 7.68 | 15.36 | 30.72 |
| 10 | 8.448 | 16.896 | 33.792 |
| 11 | 9.216 | 18.432 | 36.864 |

The time required for the CDC to complete the measurement of all 12 stages is defined as the CDC conversion sequence time. The SEQUENCE_STAGE_NUM and DECIMATION bits determine the conversion time, as listed in Table 10.

For example, if the device is operated with a decimation rate of 128 and the SEQUENCE_STAGE_NUM bit is set to 5 for the conversion of six stages in a sequence, the conversion sequence time is 9.216 ms.

### *Full Power Mode CDC Conversion Sequence Time*

The full power mode CDC conversion sequence time for all 12 stages is set by configuring the SEQUENCE_STAGE_NUM and DECIMATION bits as outlined in Table 10.

Figure 26 shows a simplified timing diagram of the full power mode CDC conversion time. The full power mode CDC conversion time ($t_{CONV\_FP}$) is set using the values shown in Table 10.

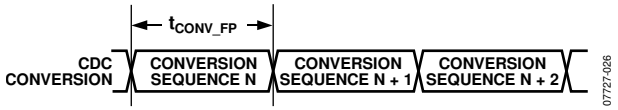



*Figure 26. Full Power Mode CDC Conversion Sequence Time*

### *Low Power Mode CDC Conversion Sequence Time with Delay*

The frequency of each CDC conversion while operating in the low power automatic wake-up mode is controlled by using the LP_CONV_DELAY Bits[3:2] located at Address 0x000 in addition to the registers listed in Table 10. This feature provides some flexibility for optimizing the trade-off between the conversion time needed to meet system requirements and the power consumption of the AD7147A.

For example, maximum power savings is achieved when the LP_CONV_DELAY bits are set to 11. With a setting of 11, the AD7147A automatically wakes up, performing a conversion every 800 ms.

**Table 11. LP_CONV_DELAY Settings**

| LP_CONV_DELAY Bits | Delay Between Conversions (ms) |
|---|---|
| 00 | 200 |
| 01 | 400 |
| 10 | 600 |
| 11 | 800 |

Figure 27 shows a simplified timing example of the low power mode CDC conversion time. As shown, the low power mode CDC conversion time is set by $t_{CONV\_FP}$ and the LP_CONV_DELAY bits.

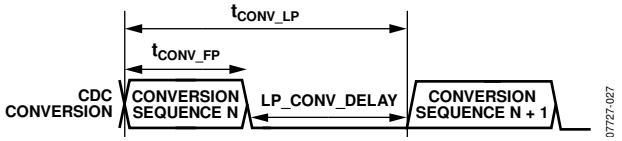



*Figure 27. Low Power Mode CDC Conversion Sequence Time*

## CDC CONVERSION RESULTS

Certain high resolution sensors require the host to read back the CDC conversion results for processing. The registers required for host processing are located in Bank 3. The host processes the data read back from these registers using a software algorithm to determine position information.

In addition to the results registers in Bank 3, the AD7147A provides the 16-bit CDC output data directly, starting at Address 0x00B of Bank 1. Reading back the CDC 16-bit conversion data register allows for customer-specific application data processing.

# CAPACITANCE SENSOR INPUT CONFIGURATION

Each input connection from the external capacitance sensors to the converter of the AD7147A can be uniquely configured by using the stage configuration registers in Bank 2 (see Table 39). These registers are used to configure the input pin connection setups, sensor offsets, sensor sensitivities, and sensor limits for each stage. Each sensor can be individually optimized. For example, a button sensor connected to STAGE0 can have different sensitivity and offset values than a button with another function that is connected to a different stage.

## CINx INPUT MULTIPLEXER SETUP

Table 35 and Table 36 list the available options for the CINx_CONNECTION_SETUP bits when the sensor input pins are connected to the CDC.

The AD7147A has an on-chip multiplexer that routes the input signals from each CINx pin to the input of the converter. Each input pin can be tied to either the negative or positive input of the CDC, or it can be left floating. Each input can also be internally connected to the BIAS signal to help prevent cross-coupling. If an input is not used, always connect it to BIAS.

Connecting a CINx input pin to the positive CDC input results in an increase in CDC output code when the corresponding sensor is activated. Connecting a CINx input pin to the negative CDC input results in a decrease in CDC output code when the corresponding sensor is activated.

The AD7147A performs a sequence of 12 conversions. The multiplexer can have different settings for each of the 12 conversions. For example, CIN0 is connected to the negative CDC input for conversion STAGE1, left floating for conversion STAGE1, and so on, for all 12 conversion stages.

For each CINx input for each conversion stage, two bits control how the input is connected to the converter, as shown in Figure 28.

### *Examples*

To connect CIN3 to the positive CDC input on Stage 0, use the following setting:

STAGE0_CONNECTION[6:0] = 0xFFBF
STAGE0_CONNECTION[12:7] = 0x2FFF

To connect CIN0 to the positive CDC input and CIN12 to the negative CIN input on STAGE5, use the following settings:

STAGE5_CONNECTION[6:0] = 0xFFFE
STAGE5_CONNECTION[12:7] = 0x37FF

## SINGLE-ENDED CONNECTIONS TO THE CDC

A single-ended connection to the CDC is defined as one CINx input connected to either the positive or negative CDC input for one conversion stage. A differential connection to the CDC is defined as one CINx input connected to the positive CDC input and a second CINx input connected to the negative input of the CDC for one conversion stage.

For any stage, if a single-ended connection to the CDC is made in that stage, the SE_CONNECTION_SETUP Bits[13:12] in the STAGEx_CONNECTION[12:7] register should be applied as described in Table 12.

**Table 12. SE_CONNECTION_SETUP Bits**

| SE_CONNECTION_SETUP | Description |
|---|---|
| 00 | Do not use. |
| 01 | Single-ended connection. For this stage, there is one CINx connected to the positive CDC input. |
| 10 | Single-ended connection. For this stage, there is one CINx connected to the negative CDC input. |
| 11 | Differential connection. For this stage, there is one CINx connected to the negative CDC input and one CINx connected to the positive CDC input. |

The SE_CONNECTION_SETUP Bits[13:12] ensure that during a single-ended connection to the CDC, the input paths to both CDC terminals are matched, which, in turn, improves the power-supply rejection of the converter measurement.

These bits should be applied in addition to setting the other bits in the STAGEx_CONNECTION registers, as outlined in the CINX Input Multiplexer Setup section.

If more than one CINx input is connected to either the positive or negative input of the converter for the same conversion, set SE_CONNECTION_SETUP to 11. For example, if CIN0 and CIN3 are connected to the positive input of the CDC, set SE_CONNECTION_SETUP to 11.

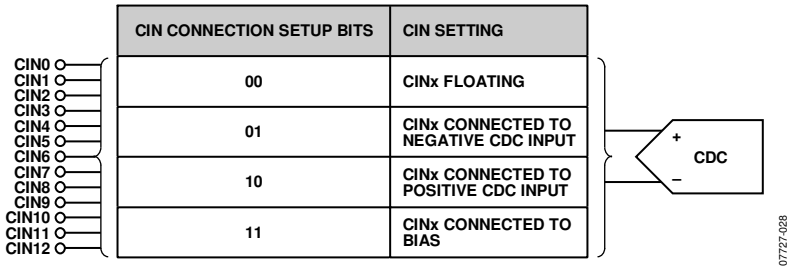



*Figure 28. Input Mux Configuration Options*

# NONCONTACT PROXIMITY DETECTION

The AD7147A internal signal processing continuously monitors all capacitance sensors for noncontact proximity detection. This feature provides the ability to detect when a user is approaching a sensor, at which time all internal calibration is immediately disabled while the AD7147 is automatically configured to detect a valid contact.

The proximity control register bits are described in Table 13. The FP_PROXIMITY_CNT and LP_PROXIMITY_CNT register bits control the length of the calibration disable period after the user stops touching the sensor and is not in close proximity to the sensor during full or low power mode. The calibration is disabled during this period and then enabled again. Figure 29 and Figure 30 show examples of how these register bits are used to set the calibration disable periods for the full and low power modes.

The calibration disable period in full power mode is the value of the FP_PROXIMITY_CNT multiplied by 16 multiplied by the time for one conversion sequence in full power mode. The calibration disable period in low power mode is the value of the LP_PROXIMITY_CNT multiplied by 4 multiplied by the time for one conversion sequence in low power mode.

## RECALIBRATION

In certain situations, for example, when a user hovers over a sensor for a long time, the proximity flag can be set for a long period. The environmental calibration on the AD7147A is suspended while proximity is detected, but changes may occur to the ambient capacitance level during the proximity event. This means that the ambient value stored on the AD7147A no longer represents the actual ambient value. In this case, even when the user is not in close proximity to the sensor, the proximity flag may still be set. This situation can occur if the user interaction creates some moisture on the sensor, causing the new sensor ambient value to be different from the expected value. In this situation, the AD7147A automatically forces a recalibration internally. This ensures that the ambient values are recalibrated, regardless of how long the user hovers over the sensor. A recalibration ensures maximum AD7147A sensor performance.

The AD7147A recalibrates automatically when the measured CDC value exceeds the stored ambient value by an amount determined by the PROXIMITY_RECAL_LVL bits for a set period of time known as the recalibration timeout. In full power mode, the recalibration timeout is controlled by FP_PROXIMITY_RECAL; in low power mode, by LP_PROXMTY_RECAL.

The recalibration timeout in full power mode is the value of FP_PROXIMITY_RECAL multiplied by the time for one conversion sequence in full power mode. The recalibration timeout in low power mode is the value of LP_PROXIMITY_RECAL multiplied by the time for one conversion sequence in low power mode.

Figure 31 and Figure 32 show examples of how the FP_PROXIMITY_RECAL and LP_PROXIMITY_RECAL register bits control the timeout period before a recalibration while operating in the full and low power modes. In these examples, a user approaches a sensor and then leaves, but the proximity detection remains active. The measured CDC value exceeds the stored ambient value by the amount set in the PROXIMITY_RECAL_LVL bits for the entire timeout period. The sensor is automatically recalibrated at the end of the timeout period.

## PROXIMITY SENSITIVITY

The fast filter in Figure 33 is used to detect when someone is close to the sensor (proximity). Two conditions, detected by Comparator 1 and Comparator 2, set the internal proximity detection signal: Comparator 1 detects when a user is approaching or leaving a sensor, and Comparator 2 detects when a user hovers over a sensor or approaches a sensor very slowly.

The sensitivity of Comparator 1 is controlled by the PROXIMITY_DETECTION_RATE bits (Address 0x003). For example, if PROXIMITY_DETECTION_RATE is set to 4, the Proximity 1 signal is set when the absolute difference between WORD1 and WORD3 exceeds (4 × 16) LSB codes.

The PROXIMITY_RECAL_LVL bits (Address 0x003) control the sensitivity of Comparator 2. For example, if PROXIMITY_RECAL_LVL is set to 75, the Proximity 2 signal is set when the absolute difference between the fast filter average value and the ambient value exceeds (75 × 16) LSB codes.

**Table 13. Proximity Control Registers (See Figure 33)**

| Bit Name | Length (Bits) | Register Address | Description |
|---|---|---|---|
| FP_PROXIMITY_CNT | 4 | 0x002[7:4] | Calibration disable time in full power mode. |
| LP_PROXIMITY_CNT | 4 | 0x002[11:8] | Calibration disable time in low power mode. |
| FP_PROXIMITY_RECAL | 10 | 0x004[9:0] | Full power mode proximity recalibration time control. |
| LP_PROXIMITY_RECAL | 6 | 0x004[15:10] | Low power mode proximity recalibration time control. |
| PROXIMITY_RECAL_LVL | 8 | 0x003[7:0] | Proximity recalibration level. This value, multiplied by 16, controls the sensitivity of Comparator 2 (see Figure 33). |
| PROXIMITY_DETECTION_RATE | 6 | 0x003[13:8] | Proximity detection rate. This value, multiplied by 16, controls the sensitivity of Comparator 1 (see Figure 33). |

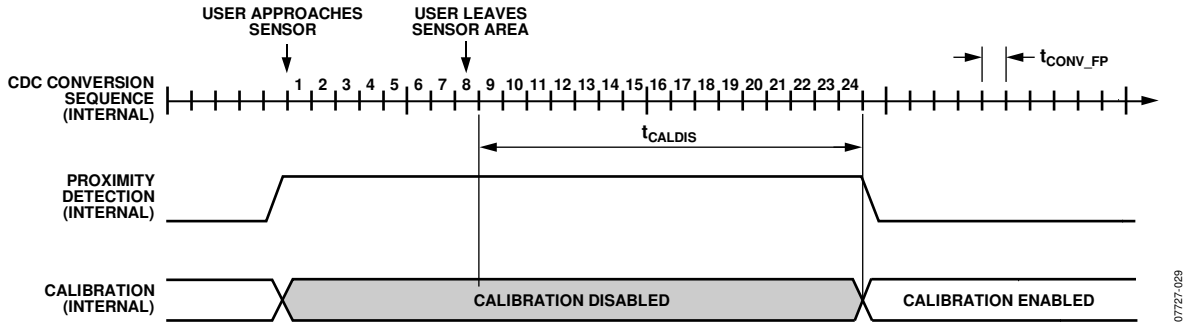



*Figure 29. Example of Full Power Mode Proximity Detection (FP_PROXIMITY_CNT = 1)*

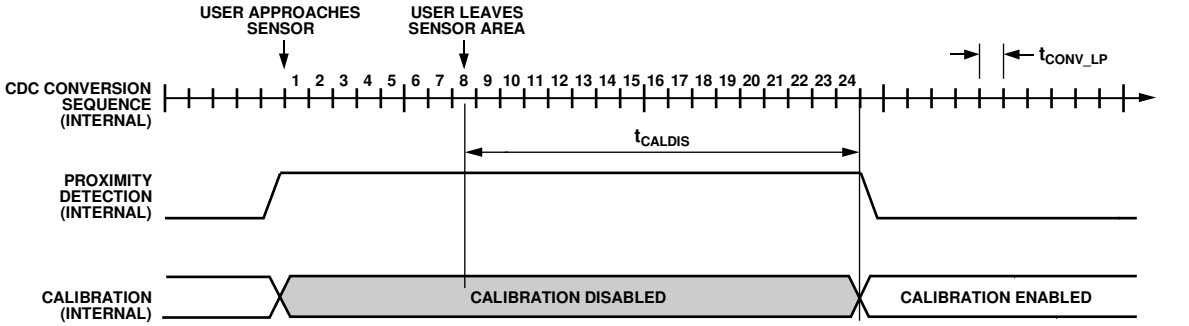



*Figure 30. Example of Low Power Mode Proximity Detection (LP_PROXIMITY_CNT = 4)*

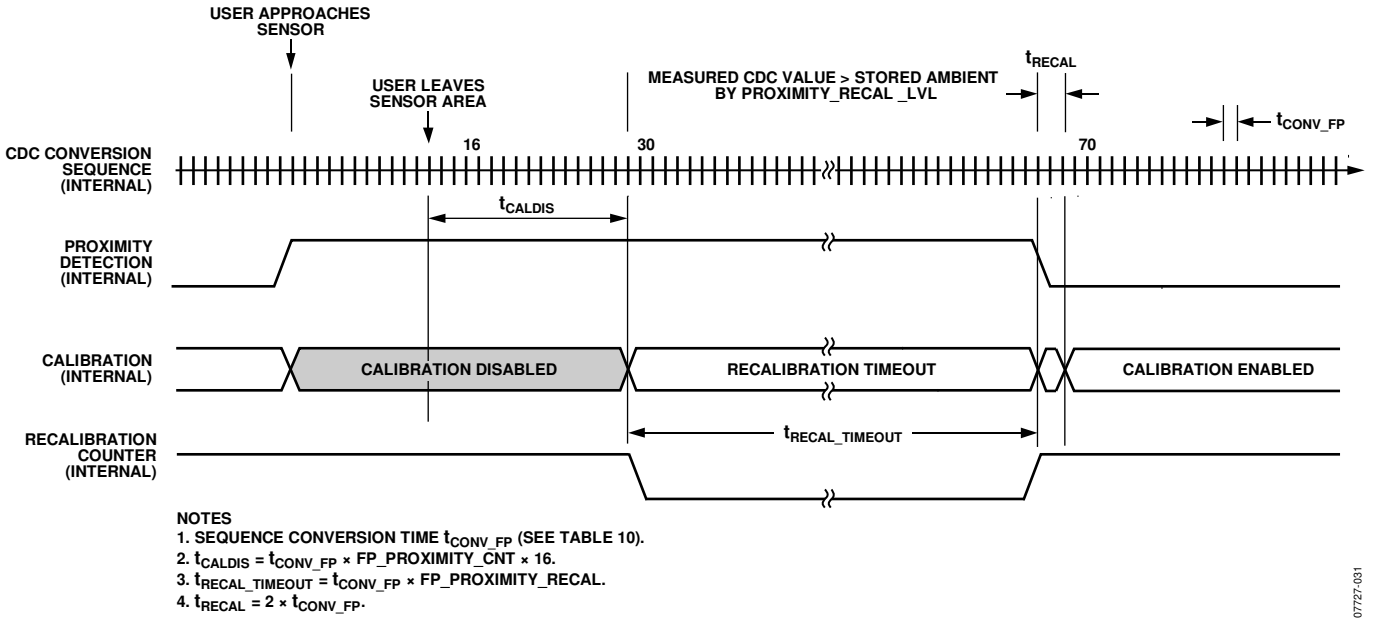



*Figure 31. Example of Full Power Mode Proximity Detection with Forced Recalibration (FP_PROXIMITY_CNT = 1 and FP_PROXIMITY_RECAL = 40)*

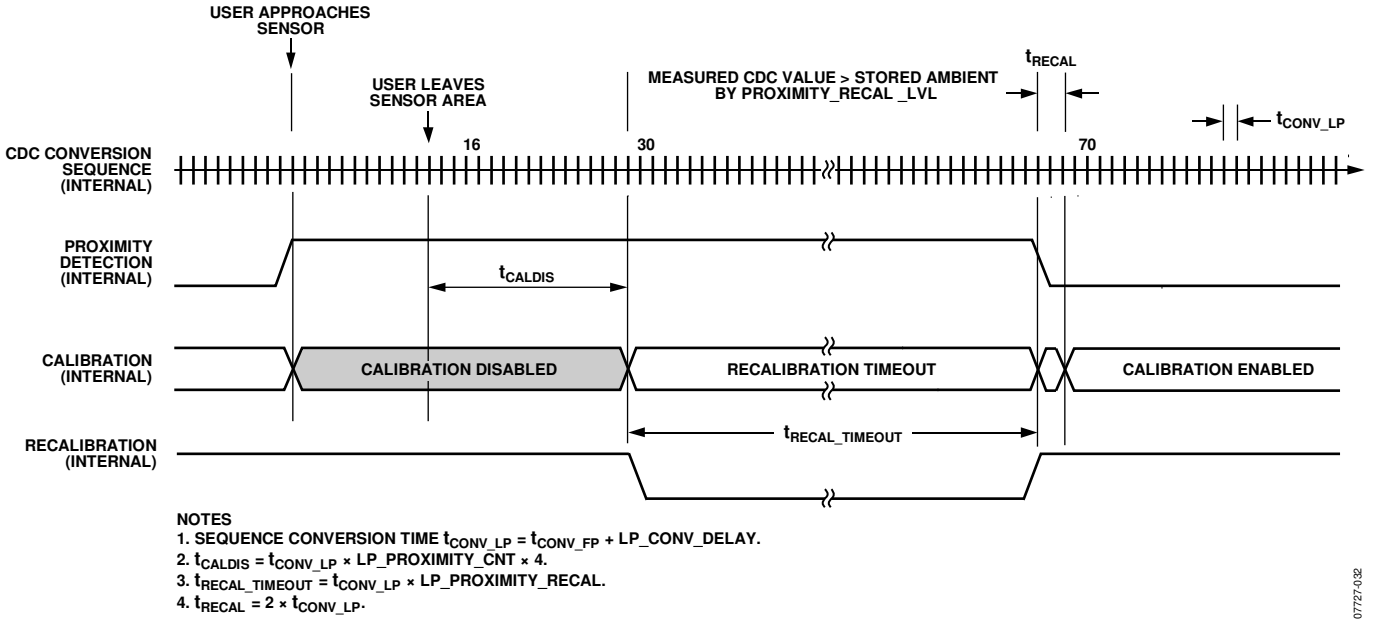



*Figure 32. Example of Low Power Mode Proximity Detection with Forced Recalibration (LP_PROXIMITY_CNT = 4 and LP_PROXIMITY_RECAL = 40)*

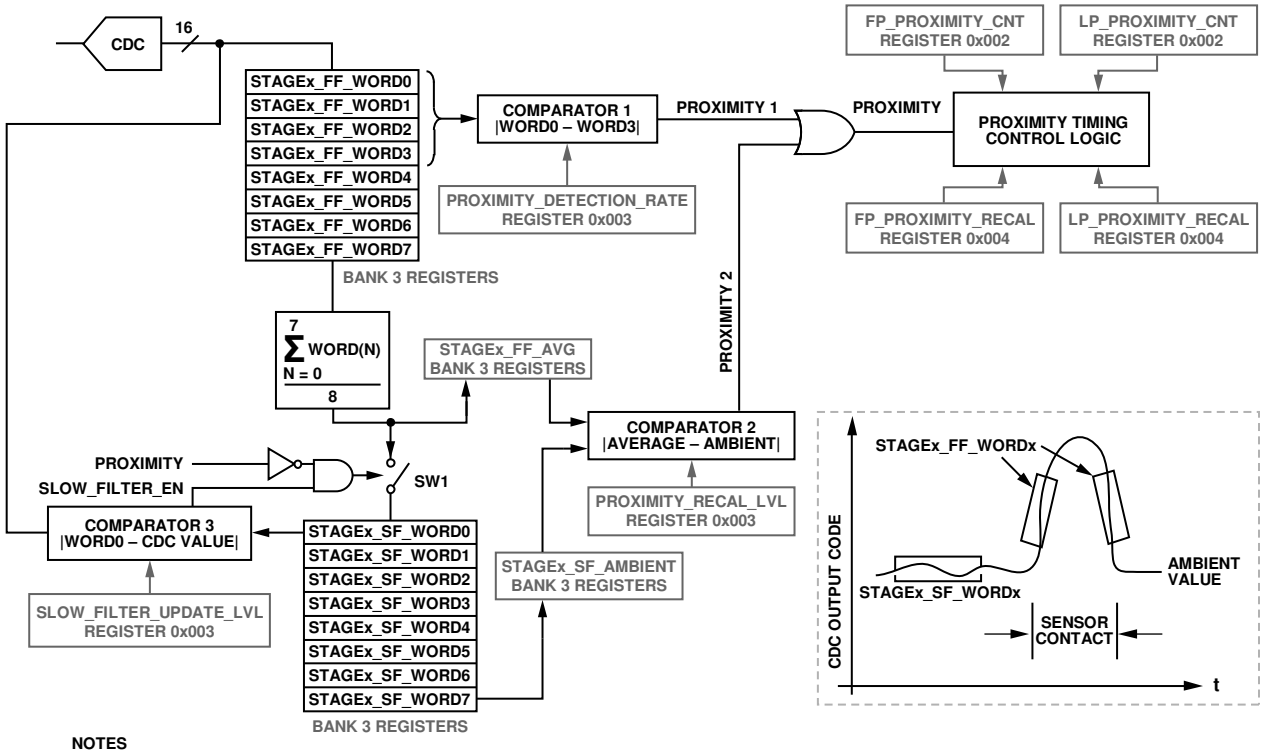
## FF_SKIP_CNT

The proximity detection fast FIFO is used by the on-chip logic to determine if proximity is detected. The fast FIFO expects to receive samples from the converter at a set rate. The fast filter skip control, FF_SKIP_CNT (Bits[3:0], Address 0x002), is used to normalize the frequency of the samples going into the FIFO, regardless of how many conversion stages are in a sequence. This value determines which CDC samples are not used (skipped) by the proximity detection fast FIFO.

Determining the FF_SKIP_CNT value is required only once during the initial setup of the capacitance sensor interface. Table 13 shows how FF_SKIP_CNT controls the update rate of the fast FIFO. The recommended value for the setting when using all 12 conversion stages on the AD7147A is 0000, or no samples skipped.

**Table 14. FF_SKIP_CNT Settings**

| FF_SKIP_CNT | FAST FIFO Update Rate | | |
|---|---|---|---|
| | **Decimation = 64** | **Decimation = 128** | **Decimation = 256** |
| 0 | 0.768 × (SEQUENCE_STAGE_NUM + 1) ms | 1.536 × (SEQUENCE_STAGE_NUM + 1) ms | 3.072 × (SEQUENCE_STAGE_NUM + 1) ms |
| 1 | 1.536 × (SEQUENCE_STAGE_NUM + 1) ms | 3.072 × (SEQUENCE_STAGE_NUM + 1) ms | 6.144 × (SEQUENCE_STAGE_NUM + 1) ms |
| 2 | 2.304 × (SEQUENCE_STAGE_NUM + 1) ms | 4.608 × (SEQUENCE_STAGE_NUM + 1) ms | 9.216 × (SEQUENCE_STAGE_NUM + 1) ms |
| 3 | 3.072 × (SEQUENCE_STAGE_NUM + 1) ms | 6.144 × (SEQUENCE_STAGE_NUM + 1) ms | 12.288 × (SEQUENCE_STAGE_NUM + 1) ms |
| 4 | 3.84 × (SEQUENCE_STAGE_NUM + 1) ms | 7.68 × (SEQUENCE_STAGE_NUM + 1) ms | 15.36 × (SEQUENCE_STAGE_NUM + 1) ms |
| 5 | 4.608 × (SEQUENCE_STAGE_NUM + 1) ms | 9.216 × (SEQUENCE_STAGE_NUM + 1) ms | 18.432 × (SEQUENCE_STAGE_NUM + 1) ms |
| 6 | 5.376 × (SEQUENCE_STAGE_NUM + 1) ms | 10.752 × (SEQUENCE_STAGE_NUM + 1) ms | 21.504 × (SEQUENCE_STAGE_NUM + 1) ms |
| 7 | 6.144 × (SEQUENCE_STAGE_NUM + 1) ms | 12.288 × (SEQUENCE_STAGE_NUM + 1) ms | 24.576 × (SEQUENCE_STAGE_NUM + 1) ms |
| 8 | 6.912 × (SEQUENCE_STAGE_NUM + 1) ms | 13.824 × (SEQUENCE_STAGE_NUM + 1) ms | 27.648 × (SEQUENCE_STAGE_NUM + 1) ms |
| 9 | 7.68 × (SEQUENCE_STAGE_NUM + 1) ms | 15.36 × (SEQUENCE_STAGE_NUM + 1) ms | 30.72 × (SEQUENCE_STAGE_NUM + 1) ms |
| 10 | 8.448 × (SEQUENCE_STAGE_NUM + 1) ms | 16.896 × (SEQUENCE_STAGE_NUM + 1) ms | 33.792 × (SEQUENCE_STAGE_NUM + 1) ms |
| 11 | 9.216 × (SEQUENCE_STAGE_NUM + 1) ms | 18.432 × (SEQUENCE_STAGE_NUM + 1) ms | 36.864 × (SEQUENCE_STAGE_NUM + 1) ms |
| 12 | 9.984 × (SEQUENCE_STAGE_NUM + 1) ms | 19.968 × (SEQUENCE_STAGE_NUM + 1) ms | 39.936 × (SEQUENCE_STAGE_NUM + 1) ms |
| 13 | 10.752 × (SEQUENCE_STAGE_NUM + 1) ms | 21.504 × (SEQUENCE_STAGE_NUM + 1) ms | 43.008 × (SEQUENCE_STAGE_NUM + 1) ms |
| 14 | 11.52 × (SEQUENCE_STAGE_NUM + 1) ms | 23.04 × (SEQUENCE_STAGE_NUM + 1) ms | 46.08 × (SEQUENCE_STAGE_NUM + 1) ms |
| 15 | 12.288 × (SEQUENCE_STAGE_NUM + 1) ms | 24.576 × (SEQUENCE_STAGE_NUM + 1) ms | 49.152 × (SEQUENCE_STAGE_NUM + 1) ms |




**NOTES**

1. SLOW_FILTER_EN, WHICH IS THE NAME OF THE OUTPUT OF COMPARATOR 3, IS SET AND SW1 IS CLOSED WHEN |STAGEx_SF_WORD0 – CDC VALUE| EXCEEDS THE VALUE PROGRAMMED IN THE SLOW_FILTER_UPDATE_LVL REGISTER PROVIDING PROXIMITY IS NOT SET.
2. PROXIMITY 1 IS SET WHEN |STAGEx_FF_WORD0 – STAGEx_FF_WORD3| EXCEEDS THE VALUE PROGRAMMED IN THE PROXIMITY_DETECTION_RATE REGISTER.
3. PROXIMITY 2 IS SET WHEN |AVERAGE – AMBIENT| EXCEEDS THE VALUE PROGRAMMED IN THE PROXIMITY_RECAL_LVL REGISTER.
4. DESCRIPTION OF COMPARATOR FUNCTIONS:
   COMPARATOR 1: USED TO DETECT WHEN A USER IS APPROACHING OR LEAVING A SENSOR.
   COMPARATOR 2: USED TO DETECT WHEN A USER IS HOVERING OVER A SENSOR OR APPROACHING A SENSOR VERY SLOWLY. ALSO USED TO DETECT IF THE SENSOR AMBIENT LEVEL HAS CHANGED AS A RESULT OF THE USER INTERACTION. FOR EXAMPLE, HUMIDITY OR DIRT LEFT BEHIND ON SENSOR.
   COMPARATOR 3: USED TO ENABLE THE SLOW FILTER UPDATE RATE. THE SLOW FILTER IS UPDATED WHEN SLOW_FILTER_EN IS SET AND PROXIMITY IS NOT SET.

*Figure 33. Proximity-Detection Logic*

# ENVIRONMENTAL CALIBRATION

The AD7147A provides on-chip capacitance sensor calibration to automatically adjust for environmental conditions that have an effect on the ambient levels of the capacitance sensor. The output levels of the capacitance sensor are sensitive to temperature, humidity, and, in some cases, dirt.

The AD7147A achieves optimal and reliable sensor performance by continuously monitoring the CDC ambient levels and compensating for any environmental changes by adjusting the values of the STAGEx_HIGH_THRESHOLD registers and the STAGEx_LOW_THRESHOLD registers as described in the Threshold Equations section. The CDC ambient level is defined as the output level of the capacitance sensor during periods when the user is not approaching or in contact with the sensor.

After the AD7147A is configured, the compensation logic runs automatically with each conversion when the AD7147A is not being touched. This allows the AD7147A to compensate for rapidly changing environmental conditions.

The ambient compensation control registers provide the host with access to general setup and controls for the compensation algorithm. On-chip RAM stores the compensation data for each conversion stage, as well as setup information specific for each stage.

Figure 34 shows an example of the ideal behavior of a capacitance sensor, where the CDC ambient level remains constant regardless of the environmental conditions. The CDC output shown is for a pair of differential button sensors, where one sensor caused an increase and the other caused a decrease in measured capacitance when activated. The positive and negative sensor threshold levels are calculated as a percentage of the STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW values, and are based on the threshold sensitivity settings and the ambient value. These values are sufficient to detect a sensor contact and result in the AD7147A asserting the $\overline{\text{INT}}$ output when the threshold levels are exceeded.

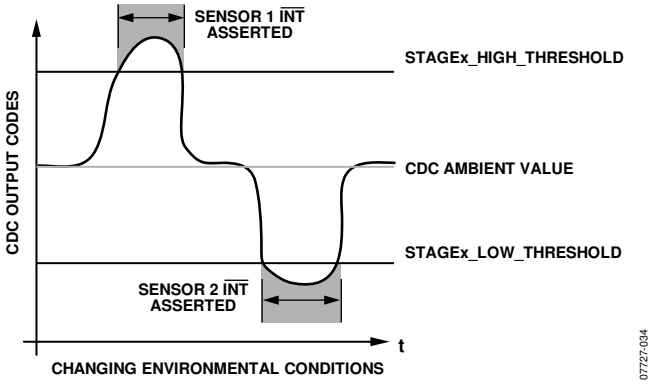



*Figure 34. Ideal Sensor Behavior with a Constant Ambient Level*

## CAPACITANCE SENSOR BEHAVIOR WITHOUT CALIBRATION

Figure 35 shows the typical behavior of a capacitance sensor when calibration is not applied and the ambient levels drifting over time as environmental conditions change. As a result of the initial threshold levels remaining constant while the ambient levels drift upward, Sensor 2 fails to detect a user contact in this example.

The Capacitance Sensor Behavior with Calibration section describes how the AD7147A adaptive calibration algorithm prevents such errors from occurring.

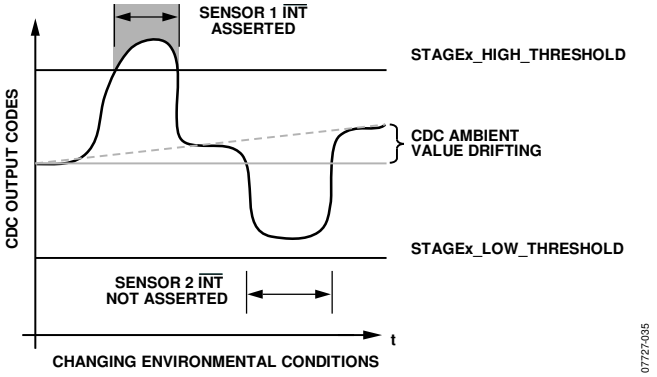



*Figure 35. Typical Sensor Behavior Without Calibration*

## THRESHOLD EQUATIONS

### *On-Chip Logic Stage High Threshold*

$$STAGEx\_HIGH\_THRESHOLD = STAGEx\_SF\_AMBIENT + \left(\frac{STAGEx\_OFFSET\_HIGH}{4}\right) + \left(\frac{\left(STAGEx\_OFFSET\_HIGH - \frac{STAGEx\_OFFSET\_HIGH}{4}\right)}{16}\right) \times POS\_THRESHOLD\_SENSITIVITY \quad (1)$$

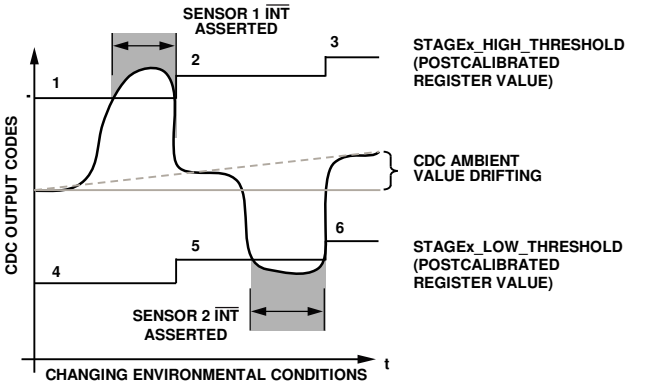
### *On-Chip Logic Stage Low Threshold*

$$STAGEx\_LOW\_THRESHOLD = STAGEx\_SF\_AMBIENT + \left(\frac{STAGEx\_OFFSET\_LOW}{4}\right) + \left(\frac{\left(STAGEx\_OFFSET\_LOW - \frac{STAGEx\_OFFSET\_LOW}{4}\right)}{16}\right) \times NEG\_THRESHOLD\_SENSITIVITY \quad (2)$$

## CAPACITANCE SENSOR BEHAVIOR WITH CALIBRATION

The AD7147A on-chip adaptive calibration algorithm prevents sensor detection errors such as the one shown in Figure 35. This is achieved by monitoring the CDC ambient levels and readjusting the initial STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW values according to the amount of ambient drift measured on each sensor. Based on the new stage offset values, the internal STAGEx_HIGH_THRESHOLD and STAGEx_LOW_THRESHOLD values described in Equation 1 and Equation 2 are automatically updated.

This closed-loop routine ensures the reliability and repeatable operation of every sensor connected to the AD7147A when they are subjected to dynamic environmental conditions. Figure 36 shows a simplified example of how the AD7147A applies the adaptive calibration process, resulting in no interrupt errors even with changing CDC ambient levels due to dynamic environmental conditions.




[1]INITIAL STAGEx_OFFSET_HIGH REGISTER VALUE.
[2]POSTCALIBRATED REGISTER STAGEx_HIGH_THRESHOLD.
[3]POSTCALIBRATED REGISTER STAGEx_HIGH_THRESHOLD.
[4]INITIAL STAGEx_LOW_THRESHOLD.
[5]POSTCALIBRATED REGISTER STAGEx_LOW_THRESHOLD.
[6]POSTCALIBRATED REGISTER STAGEx_LOW_THRESHOLD.

*Figure 36. Typical Sensor Behavior with Calibration Applied on the Data Path*

## SLOW FIFO

As shown in Figure 33, there are a number of FIFOs implemented on the AD7147A. These FIFOs are located in Bank 3 of the on-chip memory. The slow FIFOs are used by the on-chip logic to monitor the ambient capacitance level from each sensor.

### *AVG_FP_SKIP and AVG_LP_SKIP*

In Register 0x001, Bits[13:12] are the slow FIFO skip control for full power mode, AVG_FP_SKIP. Bits[15:14] in the same register are the slow FIFO skip control for low power mode, AVG_LP_SKIP, and determine which CDC samples are not used (skipped) in the slow FIFO. Changing the values of the AVG_FP_SKIP and AVG_LP_SKIP bits slows down or speeds up the rate at which the ambient capacitance value tracks the measured capacitance value read by the converter.

- Slow FIFO update rate in full power mode = AVG_FP_SKIP × [(3 × Decimation Rate) × (SEQUENCE_STAGE_NUM + 1) × (FF_SKIP_CNT + 1) × 4 × $10^{-6}$].
- Slow FIFO update rate in low power mode = ((AVG_LP_SKIP + 1) × (3 × Decimation Rate) × (SEQUENCE_STAGE_NUM + 1) × (4 × $10^{-6}$))+ LP_CONV_DELAY.

The slow FIFO is used by the on-chip logic to track the ambient capacitance value. The slow FIFO expects to receive samples from the converter at a rate between 33 ms and 40 ms. AVG_FP_SKIP and AVG_LP_SKIP are used to normalize the frequency of the samples going into the FIFO, regardless of how many conversion stages are in a sequence.

Determining the AVG_FP_SKIP and AVG_LP_SKIP values is required only once during the initial setup of the capacitance sensor interface. The recommended values for these settings when using all 12 conversion stages on the AD7147A are as follows:

- AVG_FP_SKIP = 00 = skip three samples
- AVG_LP_SKIP = 00 = skip zero samples

## SLOW_FILTER_UPDATE_LVL

SLOW_FILTER_UPDATE_LVL controls whether the most recent CDC measurement goes into the slow FIFO (slow filter). The slow filter is updated when the difference between the current CDC value and the last value of the slow FIFO is greater than the value of SLOW_FILTER_UPDATE_LVL, which is in the Ambient Control 1 register (AMB_COMP_CTRL1), Address 0x003.