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Programmable Touch Controller for Single Electrode Capacitance Sensors

Data Sheet **AD7148**

FEATURES

- Programmable capacitance-to-digital converter (CDC)
  - Femtofarad (fF) resolution
  - 8 capacitance sensor inputs
  - 25 ms update rate, all 8 sensor inputs
  - No external RC components required
  - Automatic conversion sequencer
- On-chip automatic calibration logic
  - Automatic compensation for environmental changes
  - Automatic adaptive threshold and sensitivity levels
  - Register map compatible with AD7143
- On-chip RAM to store calibration data
- I²C-compatible serial interface
- Separate V_{DRIVE} level for serial interface
- Interrupt output
- 16-lead, 4 mm × 4 mm LFCSP
- 2.6 V to 3.3 V supply voltage
- Low operating current
  - Full power mode: 1 mA
  - Low power mode: 21.5 µA

APPLICATIONS

- Cell phones
- Personal music and multimedia players
- Smart handheld devices
- Television, A/V, and remote controls
- Gaming consoles
- Digital still cameras

FUNCTIONAL BLOCK DIAGRAM

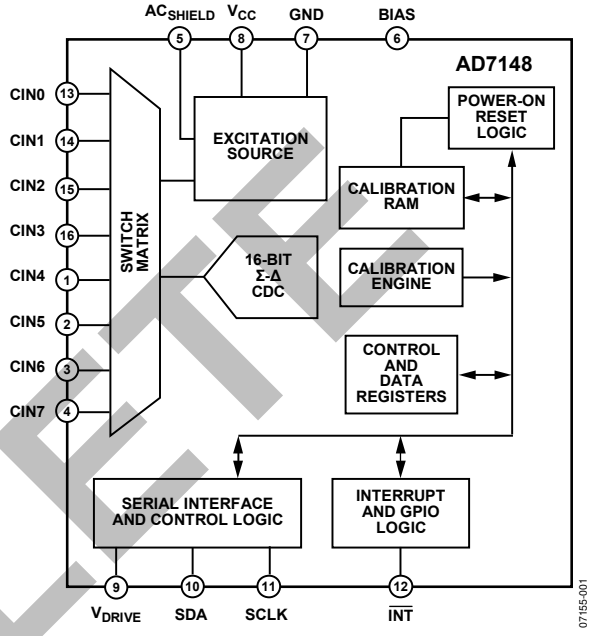

Figure 1.

GENERAL DESCRIPTION

The AD7148 is designed for use with capacitance sensors implementing functions such as buttons, scroll bars, and wheels. The sensors need only one PCB layer, enabling ultrathin applications.

The AD7148 is an integrated capacitance-to-digital converter (CDC) with on-chip environmental calibration. The CDC has eight inputs channeled through a switch matrix to a 16-bit, 250 kHz sigma-delta (Σ-Δ) converter. The CDC is capable of sensing changes in the capacitance of the external sensors and uses this information to register a sensor activation. The external sensors can be arranged as a series of buttons, as a scroll bar or wheel, or as a combination of sensor types. By programming the registers, the user has full control over the CDC setup.

High resolution sensors require minimal software to run on the host processor.

The AD7148 is designed for single electrode capacitance sensors (grounded sensors). There is an active shield output to minimize noise pickup in the sensor. For floating, or two, electrode sensors, use the AD7143.

The AD7148 has on-chip calibration logic to compensate for changes in the ambient environment. The calibration sequence is performed automatically and at continuous intervals as long as the sensors are not touched. This ensures that there are no false or nonregistering touches on the external sensors due to a changing environment.

The AD7148 has an I²C-compatible serial interface, as well as an interrupt output. There is a V_{DRIVE} pin to set the voltage level for the serial interface independent of V_{CC}.

The AD7148 is available in a 16-lead, 4 mm × 4 mm LFCSP and operates from a 2.6 V to 3.6 V supply. The operating current consumption in low power mode is typically 26 µA.

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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REVISION HISTORY

5/15—Rev. A to Rev. B

Changes to Figure 4 ... 7
Updated Outline Dimensions ... 56
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1/10—Rev. 0 to Rev. A

Changes to Figure 4 and Table 6 ... 7
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12/07—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 2.6 V to 3.6 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CAPACITANCE-TO-DIGITAL CONVERTER					
Update Rate	24.25	25	25.75	ms	8 conversion stages in sequencer; decimation rate = 256
Resolution		16		Bits	
CINx Input Range		±8		pF	
No Missing Codes	16			Bits	Guaranteed by design, not production tested
Total Unadjusted Error			±20	%	
Output Noise (Peak-to-Peak)		7		Codes	Decimation rate = 128
		3		Codes	Decimation rate = 256
Output Noise (RMS)		0.8		Codes	Decimation rate = 128
		0.5		Codes	Decimation rate = 256
C_{STRAY} Offset Range		±20		pF	6-bit DAC
C_{STRAY} Offset Resolution		0.32		pF	
Low Power Mode Delay Accuracy			4	%	% of 200 ms, 400 ms, 600 ms, or 800 ms
EXCITATION SOURCE					
Frequency		250		kHz	
Output Voltage	0		V_{CC}	V	Oscillating
AC_{SHIELD}					
Short-Circuit Source Current		10		mA	
Short-Circuit Sink Current		10		mA	
Maximum Output Load			150	pF	Capacitance load on AC_{SHIELD} to ground
LOGIC INPUTS (SCLK, SDA,)					
Input High Voltage, V_{IH}	0.7 × V_{DRIVE}			V	
Input Low Voltage, V_{IL}			0.4	V	
Input High Voltage, I_{IH}	−1			µA	V_{IN} = V_{DRIVE}
Input Low Voltage, I_{IL}			1	µA	V_{IN} = GND
Hysteresis		150		mV	
OPEN-DRAIN OUTPUTS (SCLK, SDA, $\overline{INT}$)					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = −1 mA
Output High Leakage Current, I_{OH}		+0.1	±1	µA	V_{OUT} = V_{DRIVE}
POWER					
V_{CC}	2.6	3.3	3.6	V	
V_{DRIVE}	1.65		3.6	V	Serial interface operating voltage
I_{CC}		0.9	1	mA	In full power mode, V_{CC} + V_{DRIVE}
		15.5	21.5	µA	Low power mode, converter idle, V_{CC} + V_{DRIVE}
		2.3	7.5	µA	Full shutdown, V_{CC} + V_{DRIVE}

TYPICAL AVERAGE CURRENT IN LOW POWER MODE

V_{CC} = 3.6 V, T = 25°C, load of 50 pF, unless otherwise noted.

Table 2.

		Current Values of Conversion Stages (µA)							
Low Power Mode Delay	**Decimation Rate**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
200 ms	64	20.83	24.18	27.52	30.82	34.11	37.37	40.6	43.81
	128	25.3	31.92	38.45	44.87	51.21	57.45	63.6	69.66
	256	34.11	46.99	59.51	71.66	83.47	94.94	106.1	116.96
400 ms	64	18.17	19.86	21.55	23.23	24.9	26.57	28.23	29.88
	128	20.43	23.79	27.12	30.43	33.72	36.98	40.22	43.43
	256	24.9	31.53	38.06	44.5	50.83	57.08	63.23	69.3
600 ms	64	17.28	18.41	19.54	20.67	21.79	22.91	24.03	25.14
	128	18.79	21.04	23.28	25.51	27.73	29.94	32.13	34.32
	256	21.79	26.25	30.67	35.04	39.37	43.66	47.9	52.11
800 ms	64	16.84	17.69	18.53	19.38	20.23	21.07	21.91	22.75
	128	17.97	19.66	21.35	23.03	24.7	26.37	28.03	29.69
	256	20.23	23.59	26.93	30.24	33.53	36.79	40.03	43.24

MAXIMUM AVERAGE CURRENT IN LOW POWER MODE

V_{CC} = 3.6 V, load of 50 pF, unless otherwise noted.

Table 3.

		Current Values of Conversion Stages (µA)							
Low Power Mode Delay	**Decimation Rate**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
200 ms	64	27.71	31.65	35.56	39.44	43.28	47.1	50.89	54.64
	128	32.96	40.72	48.37	55.89	63.3	70.59	77.77	84.84
	256	43.28	58.37	72.99	87.17	100.92	114.26	127.22	139.8
400 ms	64	24.61	26.6	28.58	30.55	32.51	34.47	36.42	38.36
	128	27.26	31.21	35.12	39	42.85	46.67	50.46	54.22
	256	32.51	40.29	47.94	55.47	62.88	70.18	77.36	84.44
600 ms	64	23.58	24.91	26.23	27.55	28.87	30.18	31.5	32.8
	128	25.35	27.99	30.62	33.24	35.84	38.43	41	43.56
	256	28.87	34.11	39.29	44.41	49.48	54.5	59.46	64.38
800 ms	64	23.06	24.06	25.05	26.05	27.04	28.03	29.02	30
	128	24.39	26.38	28.36	30.33	32.29	34.25	36.2	38.14
	256	27.04	30.98	34.9	38.78	42.64	46.46	50.25	54.01

I²C TIMING SPECIFICATIONS (AD7148-1)

T_A = −40°C to +85°C, V_{DRIVE} = 1.65 V to 3.6 V, V_{CC} = 2.6 V to 3.6 V, unless otherwise noted. Sample tested at 25°C to ensure compliance. All input signals timed from a voltage level of 1.6 V.

Table 4.

Parameter[1]	Limit	Unit	Description
f_{SCLK}	400	kHz max	
t_1	0.6	µs min	Start condition hold time, $t_{HD; STA}$
t_2	1.3	µs min	Clock low period, t_{LOW}
t_3	0.6	µs min	Clock high period, t_{HIGH}
t_4	100	ns min	Data setup time, $t_{SU; DAT}$
t_5	300	ns min	Data hold time, $t_{HD; DAT}$
t_6	0.6	µs min	Stop condition setup time, $t_{SU; STO}$
t_7	0.6	µs min	Start condition setup time, $t_{SU; STA}$
t_8	1.3	µs min	Bus free time between stop and start conditions, t_{BUF}
t_R	300	ns max	Clock/data rise time
t_F	300	ns max	Clock/data fall time

[1] Guaranteed by design, not production tested.

I²C Timing Diagram

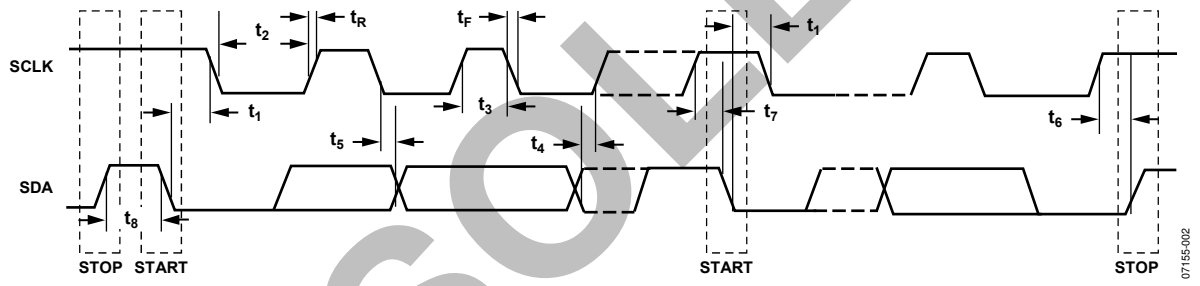


Figure 2. I²C Detailed Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_{CC} to GND	−0.3 V to +3.6 V
Analog Input Voltage to GND	−0.3 V to V_{CC} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
Input Current to Any Pin Except Supplies[1]	10 mA
ESD Rating (Human Body Model)	2.5 kV
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
LFCSP	
Power Dissipation	450 mW
θ_{JA} Thermal Impedance	135.7°C/W
IR Reflow Peak Temperature	260°C ± 0.5°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

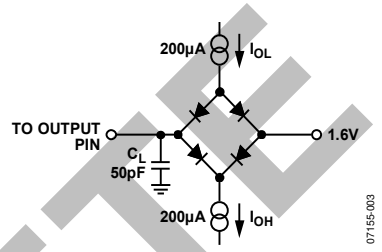
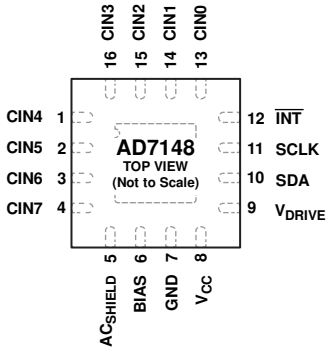


Figure 3. Load Circuit for Digital Output Timing Specifications

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD IS NOT CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINT AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE GROUND PLANE.

07155-004

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CIN4	Capacitance Sensor Input.
2	CIN5	Capacitance Sensor Input.
3	CIN6	Capacitance Sensor Input.
4	CIN7	Capacitance Sensor Input.
5	AC_{SHIELD}	CDC Active Shield Output. Connect to external shield.
6	BIAS	Bias Node for Internal Circuitry. Requires 100 nF capacitor to ground.
7	GND	Ground Reference Point for All Circuitry.
8	V_{CC}	Supply Voltage.
9	V_{DRIVE}	Serial Interface Operating Voltage Supply.
10	SDA	I^2C Serial Data Input/Output. SDA requires pull-up resistor.
11	SCLK	Clock Input for Serial Interface.
12	$\overline{INT}$	General-Purpose Open-Drain Interrupt Output. Programmable polarity; requires pull-up resistor.
13	CIN0	Capacitance Sensor Input.
14	CIN1	Capacitance Sensor Input.
15	CIN2	Capacitance Sensor Input.
16	CIN3	Capacitance Sensor Input.
17	EPAD	The exposed pad is not connected internally. For increased reliability of the solder joint and maximum thermal capability, it is recommended that the pad be soldered to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

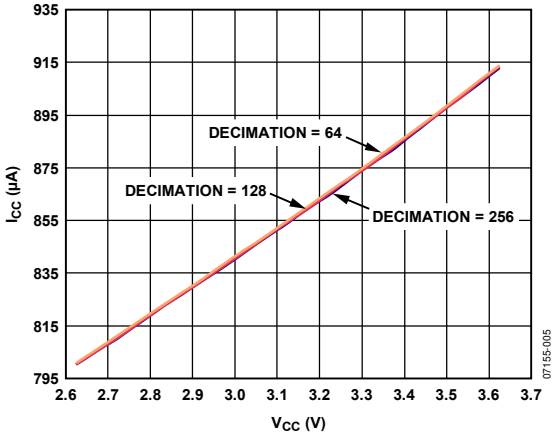


Figure 5. Supply Current vs. Supply Voltage

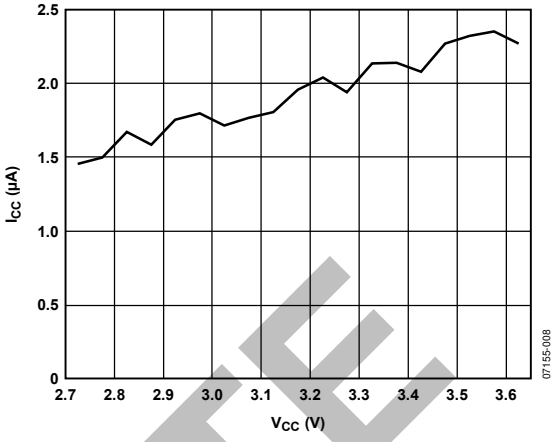


Figure 8. Shutdown Supply Current vs. Supply Voltage

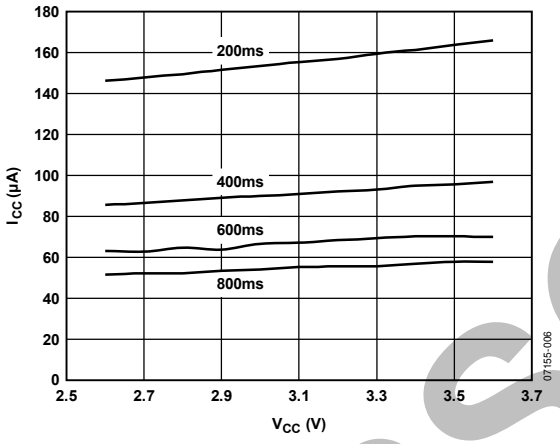


Figure 6. Low Power Supply Current vs. Supply Voltage, Decimation Rate = 256

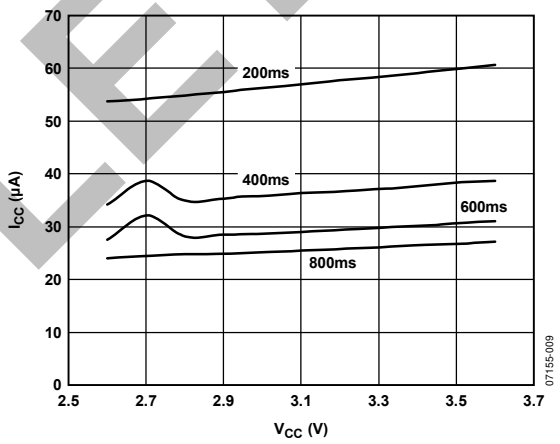


Figure 9. Low Power Supply Current vs. Supply Voltage, Decimation Rate = 64

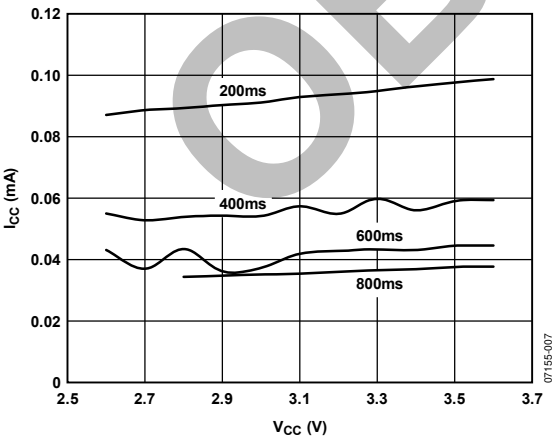


Figure 7. Low Power Supply Current vs. Supply Voltage Decimation Rate = 128

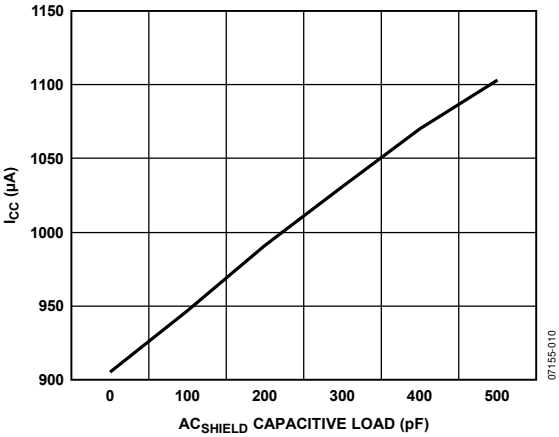


Figure 10. Supply Current vs. Capacitive Load on CIN

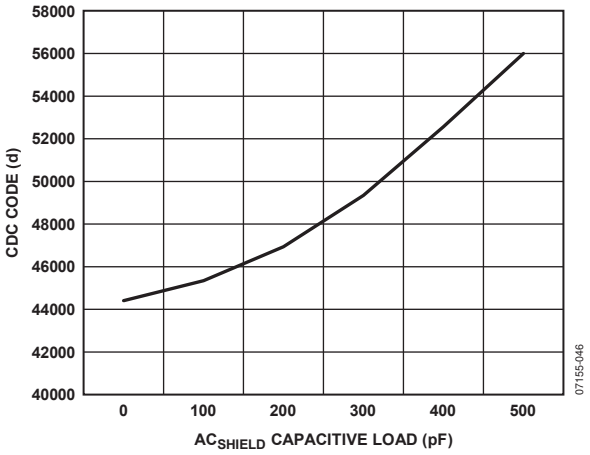


Figure 11. CDC Output Code vs. Capacitive Load on AC_{SHIELD}

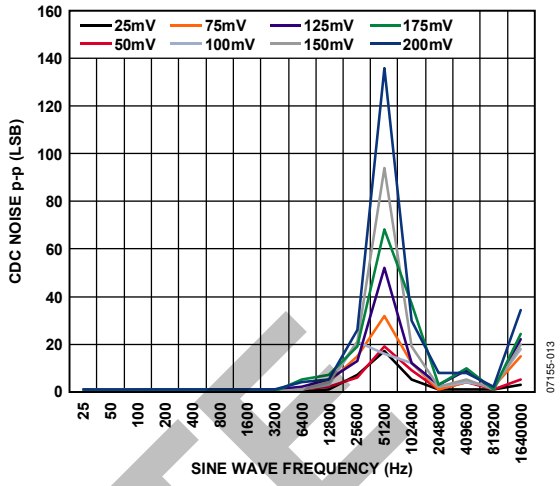


Figure 14. Power Supply Sine Wave Rejection, V_{CC} = 3.6 V

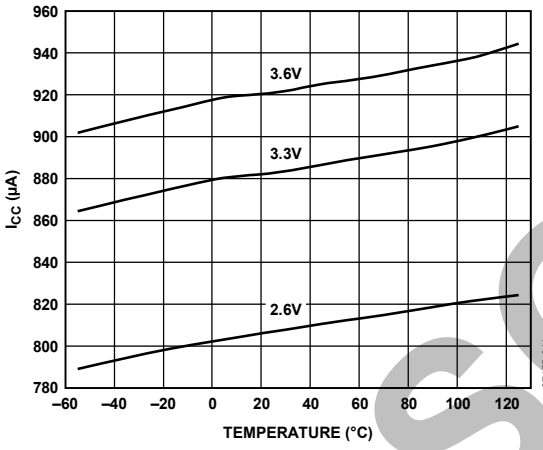


Figure 12. Supply Current vs. Temperature

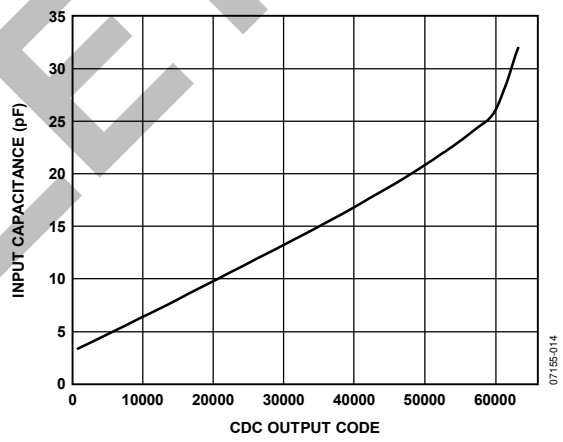


Figure 15. CDC Linearity, V_{CC} = 3.3 V

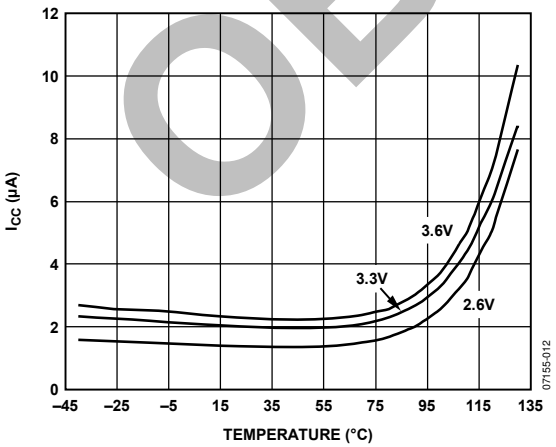


Figure 13. Shutdown Supply Current vs. Temperature

THEORY OF OPERATION

The AD7148 is a capacitance-to-digital converter (CDC) with on-chip environmental compensation, intended for use in portable systems requiring high resolution user input. The internal circuitry consists of a 16-bit, Σ-Δ converter that converts a capacitive input signal into a digital value. There are eight input pins on the AD7148: CIN0 to CIN7. A switch matrix routes the input signals to the CDC. The result of each capacitance-to-digital conversion is stored in on-chip registers. The host subsequently reads the results over the serial interface. The AD7148 has an I^2C interface, ensuring that the part is compatible with a wide range of host processors.

The AD7148 interfaces with up to eight external capacitance sensors. These sensors can be arranged as buttons, scroll bars, wheels, or as a combination of sensor types. The external sensors consist of an electrode on a single or multiple layer PCB that interfaces directly to the AD7148.

The AD7148 can be set up to implement any set of input sensors by programming the on-chip registers. The registers can also be programmed to control features such as averaging, offsets, and gains for each of the external sensors. There is an on-chip sequencer to control how each of the capacitance inputs is polled.

The AD7148 has on-chip digital logic and 528 words of RAM that are used for environmental compensation. The effects of humidity, temperature, and other environmental factors can affect the operation of capacitance sensors. Transparent to the user, the AD7148 performs continuous calibration to compensate for these effects, allowing the AD7148 to give error-free results at all times.

The AD7148 requires minimal companion software that runs on the host or other microcontroller to implement high resolution sensor functions, such as scroll bars or wheels. However, no companion software is required to implement buttons. Button sensors are implemented on chip, entirely in digital logic.

The AD7148 can be programmed to operate in either full power mode or low power, automatic wake-up mode. The automatic wake-up mode is particularly suited for portable devices that require low power operation, providing the user with significant power savings and full functionality.

The AD7148 has an interrupt output, $\overline{\text{INT}}$, to indicate when new data has been placed into the registers. $\overline{\text{INT}}$ is used to interrupt the host on sensor activation. The AD7148 operates from a 2.6 V to 3.6 V supply and is available in a 16-lead, 4 mm × 4 mm LFCSP.

CAPACITANCE SENSING THEORY

The AD7148 measures capacitance changes from sensors where one plate is connected to ground. The sensor electrode on the PCB makes up one plate of a virtual capacitor. The other plate of the capacitor is the user's finger, which is grounded with respect to the sensor input.

The AD7148 first outputs an excitation signal to charge the plate of the capacitor. When the user comes close to the sensor, the virtual capacitor is formed, with the user acting as the second capacitor plate.

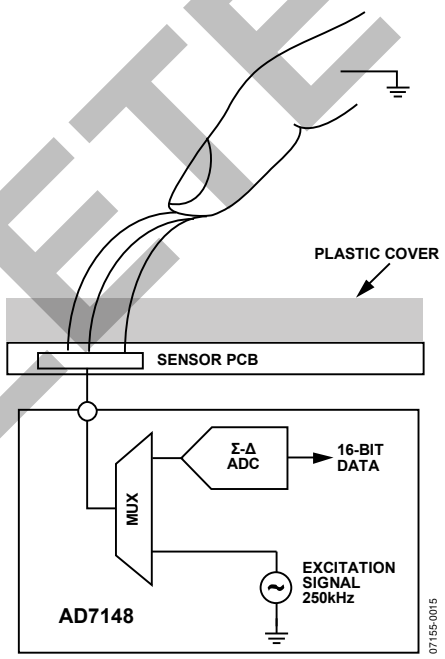


Figure 16. Capacitance Sensing Method

A square wave excitation signal is applied to the CINx input during the conversion, and the modulator continuously samples the charge going through the CINx pin. The output of the modulator is processed via a digital filter, and the resulting digital data is stored in the CDC_RESULT_Sx registers for each conversion stage, located at Address 0x00B to Address 0x012.

Registering a Sensor Activation

When a user approaches a sensor, the total capacitance associated with that sensor changes and is measured by the AD7148. When the capacitance changes to such an extent that a set threshold is exceeded, the AD7148 registers this as a sensor activation.

On-chip threshold limits are used to determine when sensor activation occurs. Figure 17 shows the change in CDC_RESULT_Sx that occurs when a user activates a sensor. The sensor is deemed to be active only when the value of CDC_RESULT_Sx is either greater than the value of STAGEx_HIGH_THRESHOLD or less than the value of STAGEx_LOW_THRESHOLD.

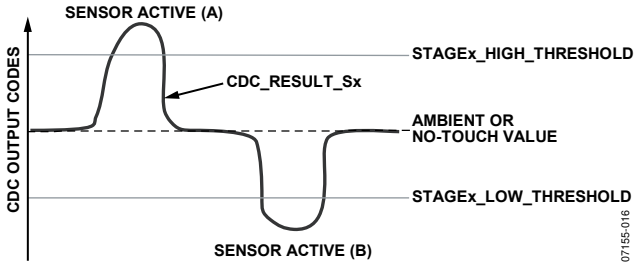


Figure 17. Sensor Activation Thresholds

In Figure 17, two different sensor activations are shown. Sensor Activate (A) occurs when a sensor is connected to the positive input of the converter. In this case, when a user activates the sensor, there is an increase in the CDC code, and the value of CDC_RESULT_Sx exceeds the value of STAGEx_HIGH_THRESHOLD. Sensor Active (B) occurs when the sensor is connected to the negative input of the converter. In this case, when a user activates the sensor, there is a decrease in the CDC code, and the value of CDC_RESULT_Sx becomes less than the value of STAGEx_LOW_THRESHOLD.

For each conversion stage, the STAGEx_HIGH_THRESHOLD and the STAGEx_LOW_THRESHOLD registers are in Register Bank 3. The values in these registers are updated automatically by the AD7148 due to its environmental calibration and adaptive threshold logic.

At power-up, the values in the STAGEx_HIGH_THRESHOLD and STAGEx_LOW_THRESHOLD registers are the same as those in the STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW registers in Register Bank 2. The user must program the STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW registers on device power-up. See the Environmental Calibration section for more information.

Complete Solution for Capacitance Sensing

Analog Devices, Inc., provides a complete solution for capacitance sensing. The two main elements of the solution are the sensor PCB and the AD7148.

If the application requires high resolution sensors such as scroll bars or wheels, software is required that runs on the host processor. No position algorithm is required for button sensors.

The memory requirements for the host depend on the sensor and are typically 10 kB of code and 600 bytes of data memory, depending on the sensor type.

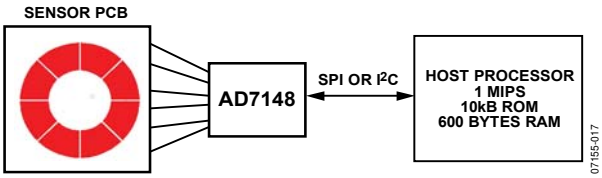


Figure 18. Three-Part Capacitance Sensing Solution

Analog Devices supplies the sensor PCB footprint design libraries to the customer and supplies any necessary software on an open-source basis.

BIAS PIN

The BIAS pin (Pin 6) is connected internally to the bias node in the AD7148. To ensure correct operation of the AD7148, connect a 100 nF capacitor between the BIAS pin and ground. The voltage at the BIAS pin is $V_{CC}/2$.

OPERATING MODES

The AD7148 has three operating modes. Full power mode, in which the device is always fully powered, is suited for applications where power is not a concern (for example, game consoles that have an ac power supply). Low power mode, in which the part automatically powers down, is tailored to give significant power savings over full power mode and is suited for mobile applications where power must be conserved. In shutdown mode, the part shuts down completely.

The POWER_MODE bits of the PWR_CONTROL register (Address 0x000[1:0]) set the operating mode on the AD7148. Table 7 shows the POWER_MODE settings for each operating mode. To put the AD7148 into shutdown mode, set the POWER_MODE bits to either 01 or 11.

Table 7. POWER_MODE Settings

POWER_MODE Bits	Operating Mode
00	Full power mode
01	Shutdown mode
10	Low power mode
11	Shutdown mode

The power-on default setting of the POWER_MODE bits is 00, full power mode.

Full Power Mode

In full power mode, all sections of the AD7148 remain fully powered and converting at all times. While a sensor is being touched, the AD7148 processes the sensor data. If no sensor is touched, the AD7148 measures the ambient capacitance level and uses this data for the on-chip compensation routines. In full power mode, the AD7148 converts at a constant rate. See the CDC Conversion Sequence Time section for more information.

Low Power Mode

When in low power mode, the POWER_MODE bits are set to 10 upon device initialization. If the external sensors are not touched, the AD7148 reduces its conversion frequency, thereby greatly reducing its power consumption. The part remains in a reduced power state while the sensors are not touched. After a delay defined by the LP_CONV_DELAY bits (200 ms, 400 ms, 600 ms or 800 ms), the AD7148 performs a conversion and uses this data to update the compensation logic.

When an external sensor is touched, the AD7148 begins a conversion sequence every 25 ms to read back data from the sensors.

In low power mode, total current consumption is an average of the current used during a conversion and the current used while the AD7148 is waiting for the next conversion to begin. For example, when LP_CONV_DELAY is 400 ms, the AD7148 typically uses 0.85 mA current for 25 ms and 14 µA for 400 ms during the conversion interval. Note that these conversion timings can be altered through the register settings. See the CDC Conversion Sequence Time section for more information.

The time required for the AD7148 to transition from a full power state to a reduced power state after the user stops touching the external sensors is configurable. The PWR_DOWN_TIMEOUT bits in the AMB_COMP_CTRL0 register (Address 0x002[13:12]) control the time delay before the AD7148 transitions to the reduced power state after the user stops touching the sensors.

Low Latency from Touch to Response

In low power mode, the AD7148 remains in a low power state until proximity is detected on any one of the external sensors. When proximity is detected, the AD7148 is automatically configured into the full power mode operation, thus converting each sequence every 36 ms. Using this method, the latency delay is minimized because the AD7148 is operating in full power mode by the time the user physically makes contact with a sensor.

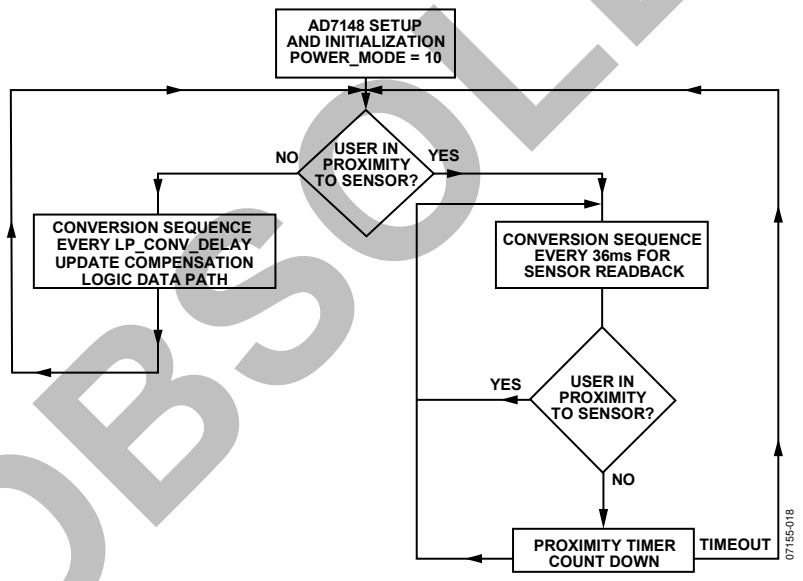


Figure 19. Low Power Mode Operation

CAPACITANCE-TO-DIGITAL CONVERTER

The capacitance-to-digital converter on the AD7148 has a Σ-Δ architecture with 16-bit resolution. There are eight possible inputs to the CDC that are connected to the input of the converter through a switch matrix. The sampling frequency of the CDC is 250 kHz.

OVERSAMPLING THE CDC OUTPUT

The decimation rate, or oversampling ratio, is determined by the DECIMATION bits of the PWR_CONTROL register (Address 0x000[9:8]), as listed in Table 8.

Table 8. CDC Decimation Rate

DECIMATION Bits	Decimation Rate	CDC Output Rate per Stage (ms)
00	256	3.072
01	128	1.536
10	64	0.768
11	64	0.768

The decimation process on the AD7148 is an averaging process, during which a number of samples are taken, and the averaged result is output. Due to the architecture of the digital filter used, the number of samples taken (per stage) is equal to 3× the decimation rate. That is, 3 × 256 samples or 3 × 128 samples are averaged to obtain each stage result.

The decimation process reduces the amount of noise present in the final CDC result. However, the higher the decimation rate, the lower the output rate per stage; thus, a trade-off is possible between a noise-free signal and speed of sampling.

CAPACITANCE SENSOR OFFSET CONTROL

There are two programmable DACs on board the AD7148 to null the effect of any stray capacitances on the CDC measurement. These offsets are due to stray capacitance to ground. Best practice is to ensure that the CDC output for any stage is approximately equal to midscale (~32,700) when no sensor is active.

The simplified block diagram in Figure 20 shows how to apply the STAGEx_OFFSET registers to null the offsets. The 6-bit POS_AFE_OFFSET and NEG_AFE_OFFSET bits program the offset DAC to provide 0.32 pF resolution offset adjustment over a range of 20 pF. Apply the positive and negative offsets to either the positive or the negative CDC input using the NEG_AFE_OFFSET and POS_AFE_OFFSET bits.

This process is required only once during the initial capacitance sensor characterization.

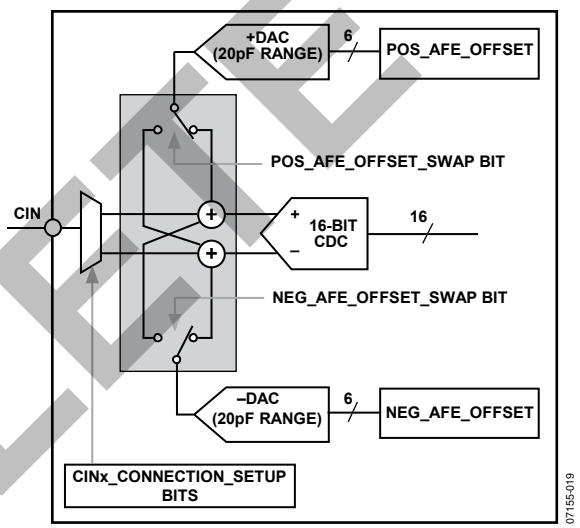


Figure 20. Analog Front-End Offset Control

CONVERSION SEQUENCER

The AD7148 has an on-chip sequencer to implement conversion control for the input channels. Up to eight conversion stages can be performed in one sequence. Each of the eight conversion stages can measure the input from a different sensor. By using the Bank 2 registers, each stage can be uniquely configured to support multiple capacitance sensor interface requirements. For example, a slider sensor can be assigned to STAGE0 through STAGE7, or a button sensor can be assigned to STAGE0. For each conversion stage, the input mux that connects the CINx inputs to the converter can have a unique setting.

The AD7148 on-chip sequence controller provides conversion control, beginning with STAGE0. Figure 21 shows a block diagram of the CDC conversion stages and CINx inputs. A conversion sequence is defined as a sequence of CDC conversions starting at STAGE0 and ending at the stage determined by the value that is programmed using the SEQUENCE_STAGE_NUM bits in the PWR_CONTROL register (Address 0x000[7:4]). Depending on the number and type of capacitance sensors that are used, not all conversion stages are required. Use the SEQUENCE_STAGE_NUM bits to set the number of conversions in one sequence, depending on the sensor interface requirements. For example, these bits are set to 0005 if the CINx inputs are mapped to only six stages. In addition, set the STAGEx_CAL_EN register according to the number of stages that are used.

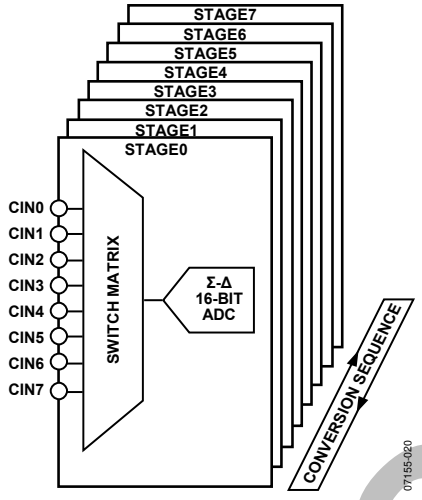


Figure 21. CDC Conversion Stages

The number of required conversion stages depends completely on the number of sensors attached to the AD7148. Figure 22 shows how many conversion stages are required for each sensor and how many inputs to the AD7148 each sensor requires.

A button sensor generally requires one sequencer stage; however, it is possible to configure two button sensors to operate differentially. Only one button from the pair can be activated at a time; pressing both buttons together results in neither button being activated. This configuration requires one conversion stage (see Figure 22, B2 and B3).

A wheel sensor requires eight stages, and a slider requires two stages. The result from each stage is used by the host software to determine user position on the slider or wheel. The algorithms that perform this process are available from Analog Devices, free of charge, on signing a software license.

CDC CONVERSION SEQUENCE TIME

The time required for one complete measurement for all eight stages by the CDC is defined as the CDC conversion sequence time. The SEQUENCE_STAGE_NUM and DECIMATION bits determine the conversion time, as shown in Table 9.

For example, while operating with a decimation rate of 128, if the SEQUENCE_STAGE_NUM bits are set to 0005 for the conversion of six stages in a sequence, the conversion sequence time is 9.216 ms.

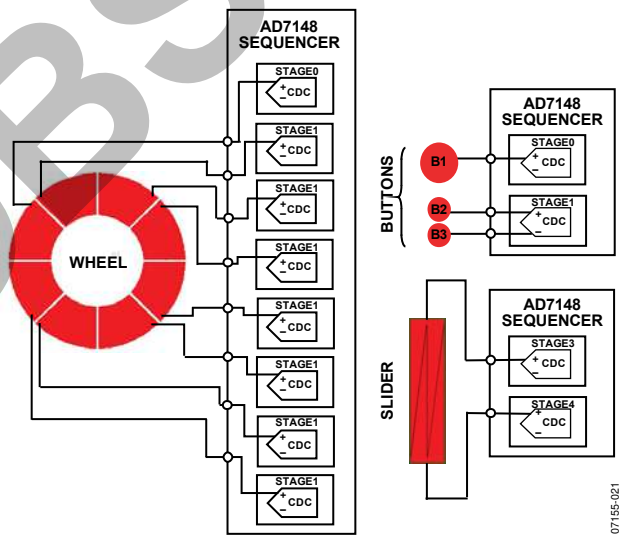


Figure 22. Sequencer Setup for Sensors

Table 9. CDC Conversion Times for Full Power Mode

	Conversion Time (ms)		
SEQUENCE_STAGE_NUM	Decimation = 64	Decimation = 128	Decimation = 256
0	0.768	1.536	3.072
1	1.536	3.072	6.144
2	2.304	4.608	9.216
3	3.072	6.144	12.288
4	3.84	7.68	15.36
5	4.608	9.216	18.432
6	5.376	10.752	21.504
7	6.144	12.288	24.576

Full Power Mode CDC Conversion Sequence Time

The full power mode CDC conversion sequence time for all eight stages is set by configuring the SEQUENCE_STAGE_NUM and DECIMATION bits, as outlined in Table 9.

Figure 23 shows a simplified timing diagram of the full power CDC conversion time. The full power mode CDC conversion time, t_{CONV_FP}, is set using Table 9.

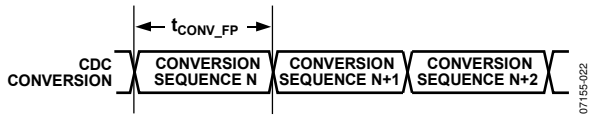


Figure 23. Full Power Mode CDC Conversion Sequence Time

Low Power Mode CDC Conversion Sequence Time with Delay

The frequency of each CDC conversion, while operating in the low power automatic wake-up mode, is controlled by using the LP_CONV_DELAY bits located at Address 0x000[3:2], in addition to the registers listed in Table 9. This feature provides some flexibility for optimizing the conversion time to meet system requirements vs. AD7148 power consumption.

For example, maximum power savings is achieved when the LP_CONV_DELAY bits (Address 0x000[3:2] are set to 11. With a setting of 11, the AD7148 automatically wakes up, performing a conversion every 800 ms.

Table 10. LP_CONV_DELAY Settings

LP_CONV_DELAY Bits	Delay Between Conversions (ms)
00	200
01	400
10	600
11	800

Figure 24 shows a simplified timing example of the low power CDC conversion time. As shown, the low power CDC conversion time is set by t_{CONV_FP} and the LP_CONV_DELAY bits.

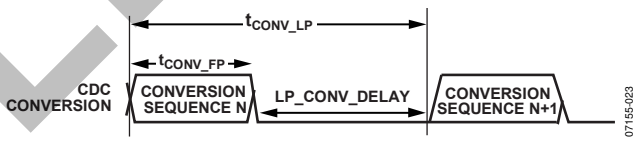


Figure 24. Low Power Mode CDC Conversion Sequence Time

CDC CONVERSION RESULTS

Certain high resolution sensors require the host to read back the CDC conversion results for processing. The registers required for host processing are located in the Bank 3 registers. The host processes the data readback from these registers using a software algorithm to determine position information.

In addition to the results registers found in the Bank 3 registers, the AD7148 provides the 16-bit CDC output data directly, starting at Address 0x00B of the Bank 1 registers. Reading back the CDC 16-bit conversion data register allows for customer-specific application data processing.

CAPACITANCE SENSOR INPUT CONFIGURATION

Each input connection from the external capacitance sensors to the AD7148 converter can be uniquely configured by using the registers in Bank 2 (see Table 39 through Table 42). These registers are used to configure input pin connection setups, sensor offsets, sensor sensitivities, and sensor limits for each stage. Each sensor can be individually optimized. For example, a button sensor connected to STAGE0 can have different sensitivity and offset values from those of a button with a different function that is connected to a different stage.

CINx INPUT MULTIPLEXER SETUP

The CINx_CONNECTION_SETUP register bits provide options for connecting the sensor input pins to the CDC (see Table 39 and Table 40).

The AD7148 has an on-chip multiplexer to route the input signals from each pin to the input of the converter. Each input pin can be tied to either the negative or the positive input of the CDC, or it can be left floating. Each input can also be internally connected to the BIAS signal to help prevent cross coupling. If an input is not used, always connect it to BIAS.

Connecting a CINx input pin to the positive CDC input results in an increase in CDC output code when the corresponding sensor is activated. Connecting a CINx input pin to the negative CDC input results in a decrease in CDC output code when the corresponding sensor is activated.

The AD7148 performs a sequence of eight conversions. The multiplexer can have different connection settings for each of the eight conversions by using the CINx_CONNECTION_SETUP bits. For example, CIN0 can be connected to the negative CDC input or left floating. The same holds true for all eight conversion stages.

Two bits in each sequence stage register control the mux setting for the input pin, as shown in Figure 25.

SINGLE-ENDED CONNECTIONS TO THE CDC

A single-ended connection to the CDC is defined as having one CINx input connected to either the positive or the negative CDC input. A differential connection to the CDC is defined as having one CINx input connected to the positive CDC input and a second CINx input connected to the negative input of the CDC.

When a single-ended connection to the CDC is made in any stage, the SE_CONNECTION_SETUP bits in the STAGEx_CONNECTION_SETUP registers should be applied. These bits ensure that, during a single-ended connection to the CDC, the input paths to both terminals are matched. This matching of input paths, in turn, improves the power supply rejection of the converter measurement.

Table 11. Application of SE_CONNECTION_SETUP Bits

Bit Values	Description
00	Do not use.
01	Single-ended connection. For this stage, there is one CINx connected to the positive CDC input.
10	Single-ended connection. For this stage, there is one CINx connected to the negative CDC input.
11	Differential connection. For this stage, there is one CINx connected to the negative CDC input and one CINx connected to the positive CDC input.

If more than one CINx input is connected to either the positive or negative input of the converter for the same conversion, set SE_CONNECTION_SETUP = 11. For example, if CIN0 and CIN3 are connected to the positive input of the CDC, SE_CONNECTION_SETUP = 11.

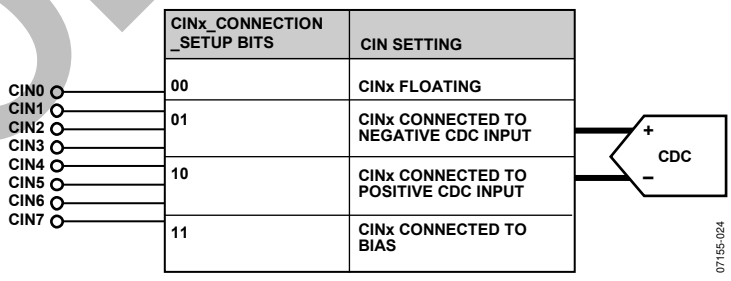


Figure 25. Input Mux Configuration Options

NONCONTACT PROXIMITY DETECTION

The AD7148 internal signal processing continuously monitors all capacitance sensors for noncontact proximity detection. This feature provides the ability to detect when a user is approaching a sensor, at which time all internal calibration is immediately disabled while the AD7148 is automatically configured to detect a valid contact.

The proximity control register bits are described in Table 12. The FP_PROXIMITY_CNT and LP_PROXIMITY_CNT register bits (Address 0x002[11:4]) control the length of the calibration disable period after the user leaves the sensor and proximity is no longer active in full and low power modes.

The calibration is disabled during this time and is enabled again at the end of this period, provided that the user is no longer approaching, or in contact with, the sensor. Figure 26 and Figure 27 show examples of how these registers are used to set the full and low power mode calibration disable periods.

The calibration disable period in full power mode is equal to FP_PROXIMITY_CNT × 16 × time taken for one conversion sequence in full power mode.

The calibration disable period in low power mode is equal to LP_PROXIMITY_CNT × 4 × time taken for one conversion sequence in low power mode.

Table 12. Proximity Control Registers (See Figure 30)

Bits	Length	Register Address	Description
FP_PROXIMITY_CNT	4 bits	0x002[7:4]	Calibration disable time in full power mode.
LP_PROXIMITY_CNT	4 bits	0x002[11:8]	Calibration disable time in low power mode.
FP_PROXIMITY_RECAL	10 bits	0x004[9:0]	Full power mode proximity recalibration time.
LP_PROXIMITY_RECAL	6 bits	0x004[15:10]	Low power mode proximity recalibration time.
PROXIMITY_RECAL_LVL	8 bits	0x003[7:0]	Proximity recalibration level. This value, multiplied by 16, controls the sensitivity of Comparator 2 in Figure 30.
PROXIMITY_DETECTION_RATE	6 bits	0x003[13:8]	Proximity detection rate. This value, multiplied by 16, controls the sensitivity of Comparator 1 in Figure 30.

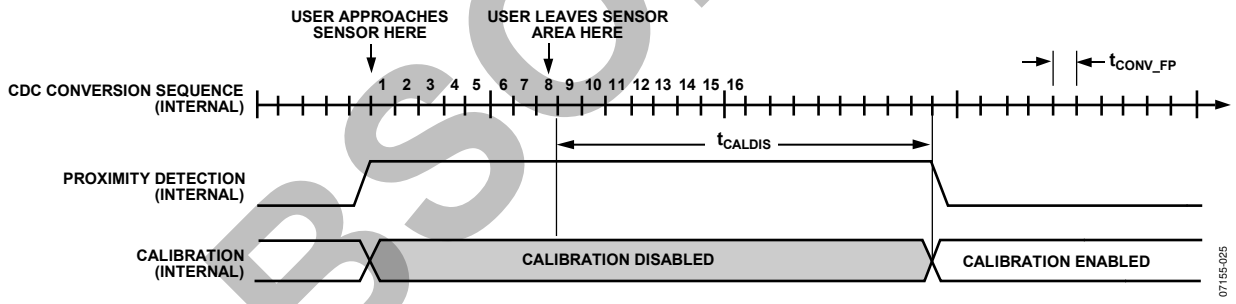


Figure 26. Full Power Mode Proximity Detection Example with FP_PROXIMITY_CNT = 1

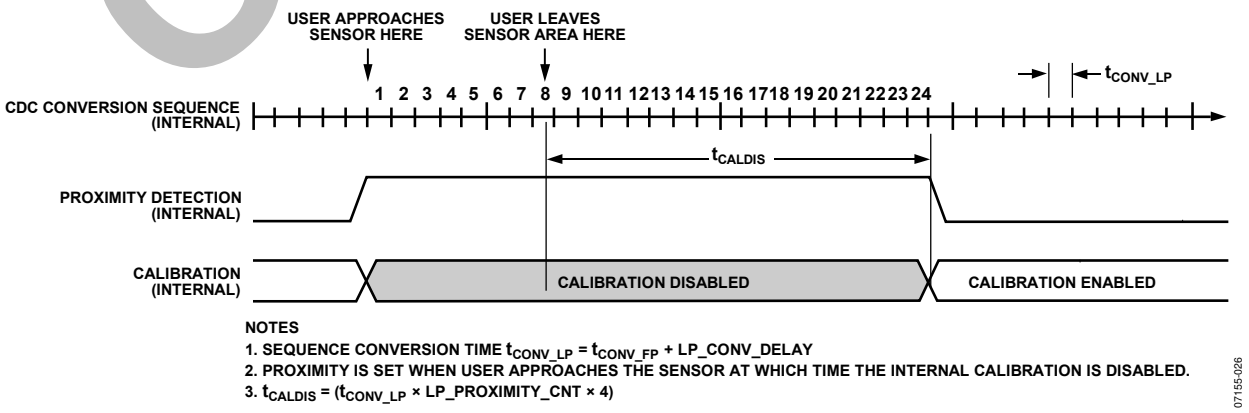


Figure 27. Low Power Mode Proximity Detection with LP_PROXIMITY_CNT = 4

RECALIBRATION

In certain situations, the proximity flag can be set for a long period: for example, when a user hovers over a sensor for a long time. The environmental calibration on the AD7148 is suspended while proximity is detected, but changes may occur to the ambient capacitance level during the proximity event. This means that the ambient value stored on the AD7148 no longer represents the actual ambient value. In this case, even when the user has left the sensor, the proximity flag may still be set. This situation could occur if user interaction creates some moisture on the sensor, causing the new sensor ambient value to be different from the expected value. In this situation, the AD7148 automatically forces an internal recalibration, ensuring that the ambient values are recalibrated, regardless of how long the user hovers over a sensor. The recalibration ensures maximum sensor performance.

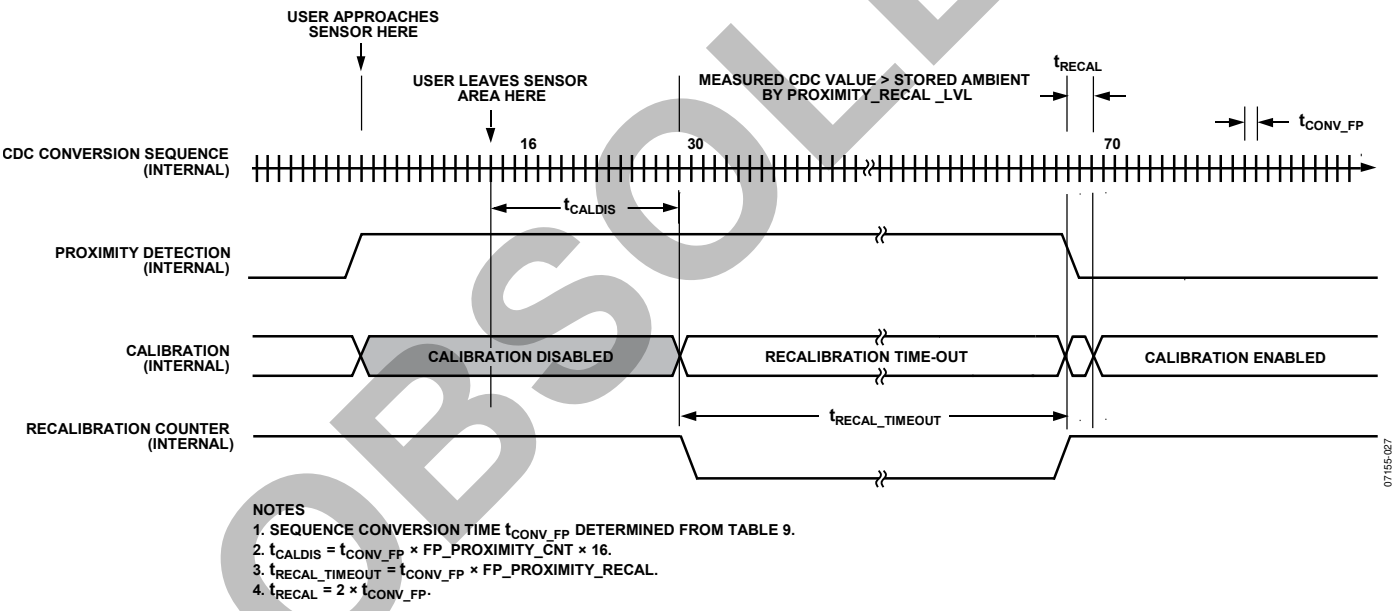
The AD7148 recalibrates automatically when the measured CDC value exceeds the stored ambient value by an amount determined by the PROXIMITY_RECAL_LVL bits (Address 0x003[7:0]) for a set period of time, known as the recalibration timeout.

In full power mode, the recalibration timeout is controlled by FP_PROXIMITY_RECAL; in low power mode, the timeout is controlled by LP_PROXIMTY_RECAL.

The recalibration timeout in full power mode is the value of the FP_PROXIMITY_RECAL multiplied by the time taken for one conversion sequence in full power mode.

The recalibration timeout in low power mode is the value of the LP_PROXIMITY_RECAL multiplied by the time taken for one conversion sequence in low power mode.

Figure 28 and Figure 29 show examples of how the FP_PROXIMITY_RECAL and LP_PROXIMITY_RECAL register bits (Address 0x004[15:0]) control the timeout period before a recalibration while operating in the full power and low power modes. These figures show a user approaching a sensor, followed by the user leaving the sensor while the proximity detection remains active after the user leaves the sensor. The measured CDC value exceeds the stored ambient value by the amount set in the PROXIMITY_RECAL_LVL bits for the entire timeout period. The sensor is automatically recalibrated at the end of the timeout period.



NOTES
1. SEQUENCE CONVERSION TIME t_{CONV_FP} DETERMINED FROM TABLE 9.
2. $t_{CALDIS} = t_{CONV\_FP} \times FP\_PROXIMITY\_CNT \times 16$.
3. $t_{RECAL\_TIMEOUT} = t_{CONV\_FP} \times FP\_PROXIMITY\_RECAL$.
4. $t_{RECAL} = 2 \times t_{CONV\_FP}$.

Figure 28. Full Power Mode Proximity Detection with Forced Recalibration Example with FP_PROXIMITY_CNT = 1 and FP_PROXIMITY_RECAL = 40

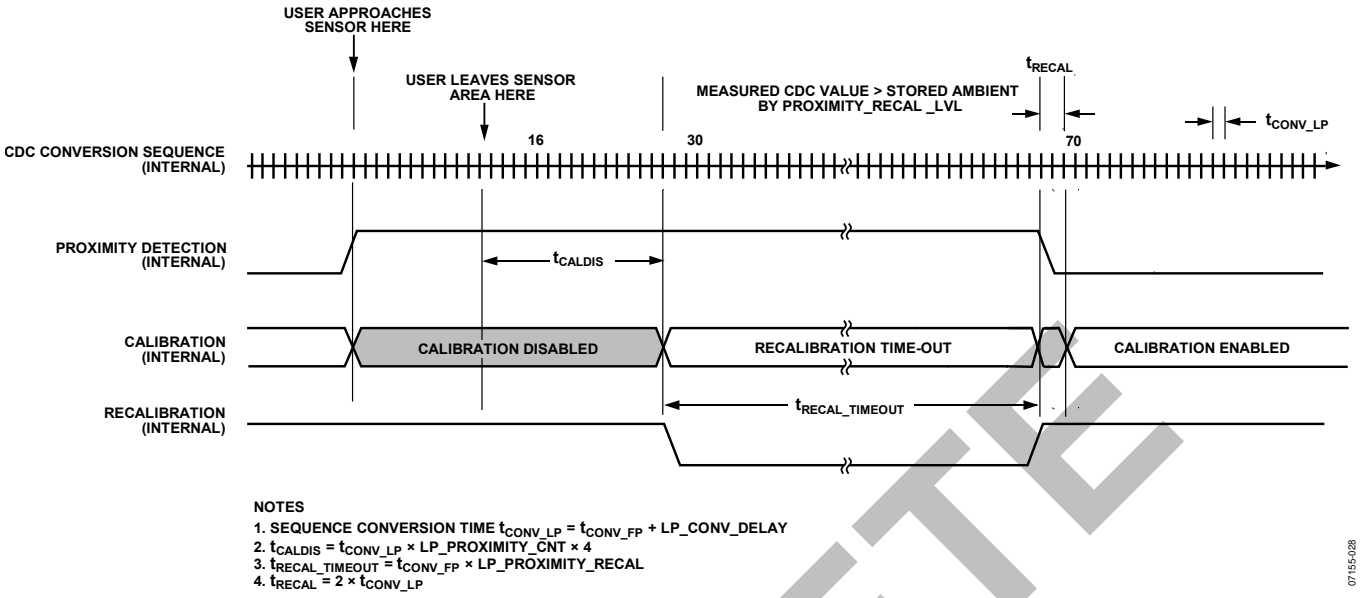


Figure 29. Low Power Mode Proximity Detection with Forced Recalibration Example with LP_PROXIMITY_CNT = 4 and LP_PROXIMITY_RECAL = 40

PROXIMITY SENSITIVITY

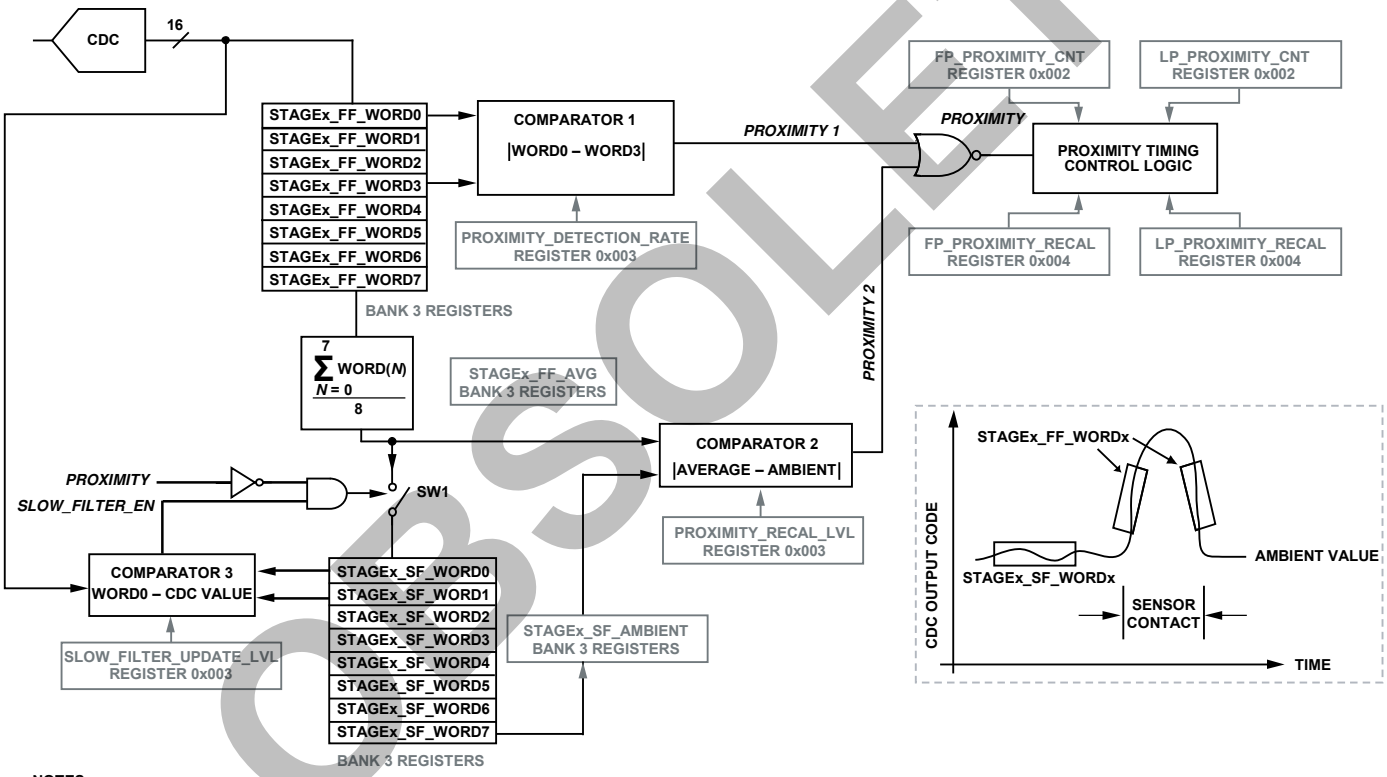
The fast filter in Figure 30 is used to detect when someone is close to the sensor (proximity). Two conditions set the internal proximity detection signal, using Comparator 1 and Comparator 2. Comparator 1 detects when a user is approaching a sensor. The PROXIMITY_DETECTION_RATE bits (Address0x003[13:8]) controls the sensitivity of Comparator 1. For example, if PROXIMITY_DETECTION_RATE is set to 4, the Proximity 1 signal is set when the absolute difference between WORD1 and WORD3 exceeds (4 × 16) LSB codes. Comparator 2 detects when a user hovers over a sensor or approaches a sensor very slowly. The PROXIMITY_RECAL_LVL bits (Address 0x003[7:0]) control the sensitivity of Comparator 2. For example, if PROXIMITY_RECAL_LVL is set to 75, the Proximity 2 signal is set when the absolute difference between the fast filter average value and the ambient value exceeds (75 × 16) LSB codes.

FF_SKIP_CNT

The proximity detection fast FIFO is used by the on-chip logic to determine if proximity is detected . The fast FIFO expects to receive samples from the converter at a set rate. FF_SKIP_CNT (Register 0x002[3:0]) is the fast filter skip control, which used to normalize the frequency of the samples going into the FIFO, regardless of how many conversion stages are in a sequence. This value determines which CDC samples are not used (skipped) in the proximity detection fast FIFO.

Determining the FF_SKIP_CNT value is required only once during the initial setup of the capacitance sensor interface. Table 13 shows how FF_SKIP_CNT controls the update rate to the fast FIFO. Recommended value for this setting, when using all eight conversion stages on the AD7148, is

FF_SKIP_CNT = 0000 = no samples skipped.



NOTES
1. *SLOW_FILTER_EN* IS SET AND SW1 IS CLOSED WHEN |STAGEx_SF_WORD0–STAGEx_SF_WORD 1| EXCEEDS THE VALUE PROGRAMMED IN THE SLOW_FILTER_UPDATE_LVL BITS PROVIDING *PROXIMITY* IS NOT SET.
2. *PROXIMITY 1* IS SET WHEN |STAGEx_FF_WORD0– STAGEx_FF_WORD3| EXCEEDS THE VALUE PROGRAMMED IN THE PROXIMITY_DETECTION_RATE BITS.
3. *PROXIMITY 2* IS SET WHEN |AVERAGE–AMBIENT| EXCEEDS THE VALUE PROGRAMMED IN THE PROXIMITY_RECAL_LVL BITS.
4. DESCRIPTION OF COMPARATOR FUNCTIONS:
   COMPARATOR 1: USED TO DETECT WHEN A USER IS APPROACHING OR LEAVING A SENSOR.
   COMPARATOR 2: USED TO DETECT WHEN A USER IS HOVERING OVER A SENSOR OR APPROACHING A SENSOR VERY SLOWLY.
   ALSO USED TO DETECT IF THE SENSOR AMBIENT LEVEL HAS CHANGED AS A RESULT OF USER INTERACTION.
   FOR EXAMPLE, HUMIDITY OR DIRT LEFT BEHIND ON SENSOR.
   COMPARATOR 3: USED TO ENABLE THE SLOW FILTER UPDATE RATE. THE SLOW FILTER IS UPDATED WHEN *SLOW_FILTER_EN* IS SET AND *PROXIMITY* IS NOT SET.

Figure 30. Proximity Detection Logic

Table 13. FF_SKIP_CNT Settings

FF_SKIP_CNT	Fast FIFO Update Rate		
	Decimation = 64	**Decimation = 128**	**Decimation = 256**
0	0.768 × (SEQUENCE_STAGE_NUM + 1) ms	1.536 × (SEQUENCE_STAGE_NUM + 1) ms	3.072 × (SEQUENCE_STAGE_NUM + 1) ms
1	1.536 × (SEQUENCE_STAGE_NUM + 1) ms	3.072 × (SEQUENCE_STAGE_NUM + 1) ms	6.144 × (SEQUENCE_STAGE_NUM + 1) ms
2	2.3 × (SEQUENCE_STAGE_NUM + 1) ms	4.608 × (SEQUENCE_STAGE_NUM + 1) ms	9.216 × (SEQUENCE_STAGE_NUM + 1) ms
3	3.072 × (SEQUENCE_STAGE_NUM + 1) ms	6.144 × (SEQUENCE_STAGE_NUM + 1) ms	12.288 × (SEQUENCE_STAGE_NUM + 1) ms
4	3.84 × (SEQUENCE_STAGE_NUM + 1) ms	7.68 × (SEQUENCE_STAGE_NUM + 1) ms	15.36 × (SEQUENCE_STAGE_NUM + 1) ms
5	4.6 × (SEQUENCE_STAGE_NUM + 1) ms	9.216 × (SEQUENCE_STAGE_NUM + 1) ms	18.432 × (SEQUENCE_STAGE_NUM + 1) ms
6	5.376 × (SEQUENCE_STAGE_NUM + 1) ms	10.752 × (SEQUENCE_STAGE_NUM + 1) ms	21.504 × (SEQUENCE_STAGE_NUM + 1) ms
7	6.144 × (SEQUENCE_STAGE_NUM + 1) ms	12.288 × (SEQUENCE_STAGE_NUM + 1) ms	24.576 × (SEQUENCE_STAGE_NUM + 1) ms
8	6.912× (SEQUENCE_STAGE_NUM + 1) ms	13.824 × (SEQUENCE_STAGE_NUM + 1) ms	27.648 × (SEQUENCE_STAGE_NUM + 1) ms
9	7.68 × (SEQUENCE_STAGE_NUM + 1) ms	15.36 × (SEQUENCE_STAGE_NUM + 1) ms	30.72 × (SEQUENCE_STAGE_NUM + 1) ms
10	8.448× (SEQUENCE_STAGE_NUM + 1) ms	16.896 × (SEQUENCE_STAGE_NUM + 1) ms	33.792 × (SEQUENCE_STAGE_NUM + 1) ms
11	9.216 × (SEQUENCE_STAGE_NUM + 1) ms	18.432 × (SEQUENCE_STAGE_NUM + 1) ms	36.864 × (SEQUENCE_STAGE_NUM + 1) ms
12	9.984 × (SEQUENCE_STAGE_NUM + 1) ms	19.968 × (SEQUENCE_STAGE_NUM + 1) ms	39.936 × (SEQUENCE_STAGE_NUM + 1) ms
13	10.752 × (SEQUENCE_STAGE_NUM + 1) ms	21.504 × (SEQUENCE_STAGE_NUM + 1) ms	43.008 × (SEQUENCE_STAGE_NUM + 1) ms
14	11.52 × (SEQUENCE_STAGE_NUM + 1) ms	23.04 × (SEQUENCE_STAGE_NUM + 1) ms	46.08 × (SEQUENCE_STAGE_NUM + 1) ms
15	12.288 × (SEQUENCE_STAGE_NUM + 1) ms	24.576 × (SEQUENCE_STAGE_NUM + 1) ms	49.152 × (SEQUENCE_STAGE_NUM + 1) ms

ENVIRONMENTAL CALIBRATION

The AD7148 provides on-chip capacitance sensor calibration to automatically adjust for environmental conditions that have an effect on the capacitance sensor ambient levels. Capacitance sensor output levels are sensitive to temperature, humidity, and in some cases, dirt. The AD7148 achieves optimal and reliable sensor performance by continuously monitoring the CDC ambient levels and correcting for any changes by adjusting the STAGEx_HIGH_THRESHOLD and STAGEx_LOW_THRESHOLD register values, as described in Equation 1 and Equation 2. The CDC ambient level is defined as the capacitance sensor output level during periods when the user is not approaching or in contact with the sensor.

The compensation logic runs automatically on every conversion after configuration when the AD7148 is not being touched, which allows the AD7148 to account for rapidly changing environmental conditions.

The ambient compensation control registers give the host access to general setup and controls for the compensation algorithm. On-chip RAM stores the compensation data for each conversion stage, as well as setup information specific to each stage.

Figure 31 shows an example of an ideal capacitance sensor behavior where the CDC ambient level remains constant, regardless of the environmental conditions. The CDC output shown is for a pair of differential button sensors, where one sensor caused an increase and the other caused a decrease in measured capacitance when activated. The positive and negative sensor threshold levels are calculated as a percentage of the STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW values based on the threshold sensitivity settings and the ambient value. These values are sufficient to detect a sensor contact, resulting in the AD7148 asserting the $\overline{\text{INT}}$ output when threshold levels are exceeded.

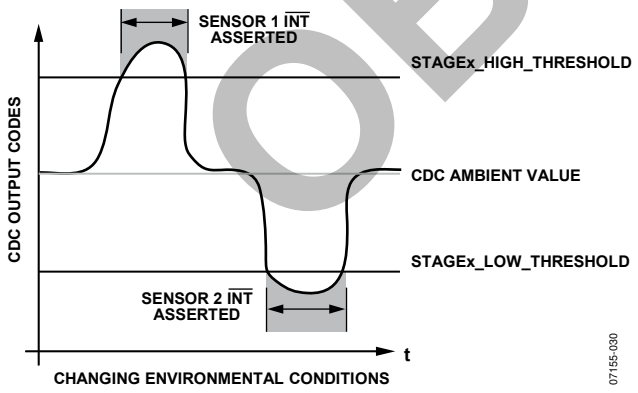


Figure 31. Ideal Sensor Behavior with a Constant Ambient Level

CAPACITANCE SENSOR BEHAVIOR WITHOUT CALIBRATION

Figure 32 shows the typical behavior of a capacitance sensor with no applied calibration. This figure shows ambient levels drifting over time as environmental conditions change. The ambient level drift results in the detection of a missed user contact on Sensor 2. This is a result of the initial low offset level remaining constant while the ambient levels drifted upward beyond the detection range.

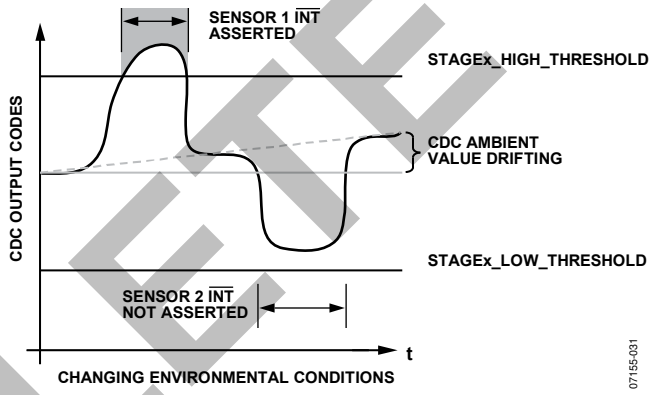


Figure 32. Typical Sensor Behavior Without Calibration Applied

The Capacitance Sensor Behavior with Calibration section describes how the AD7148 adaptive calibration algorithm prevents errors such as this from occurring.

CAPACITANCE SENSOR BEHAVIOR WITH CALIBRATION

The AD7148 on-chip adaptive calibration algorithm prevents sensor detection errors such as the one shown in Figure 32. Error prevention is accomplished by monitoring CDC ambient levels and readjusting the initial STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW values according to the amount of ambient drift measured on each sensor. The internal STAGEx_HIGH_THRESHOLD and STAGEx_LOW_THRESHOLD values described in Equation 1 and Equation 2 are automatically updated based on the new values of STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW. This closed-loop routine ensures the reliability and repeatable operation of every sensor connected to the AD7148 under dynamic environmental conditions. Figure 33 shows a simplified example of how the AD7148 applies the adaptive calibration process resulting in no interrupt errors under changing CDC ambient levels due to environmental conditions.

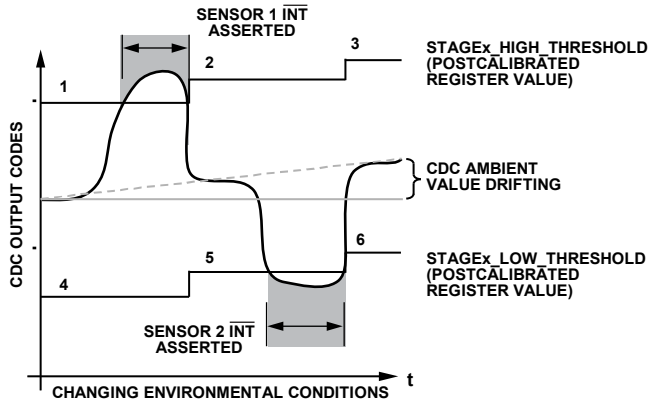


Figure 33. Typical Sensor Behavior with Calibration Applied on the Data Path

SLOW FIFO

As shown in Figure 30, there are a number of FIFOs implemented on the AD7148. These FIFOs are located in Bank 3 of the on-chip memory. The slow FIFOs are used by on-chip logic to monitor the ambient capacitance level from each sensor.

AVG_FP_SKIP and AVG_LP_SKIP

In Register 0x001, Bits[13:12]are the slow FIFO skip control for full power mode, AVG_FP_SKIP. Bits[15:14] in the same register are the slow FIFO skip control for low power mode, AVG_LP_SKIP. These values determine which CDC samples are not used (skipped) in the slow FIFO. Changing theses values slows down or speeds up the rate at which the ambient capacitance value tracks the measured capacitance value read by the converter.

Slow FIFO update rate in full power mode is equal to

AVG_FP_SKIP × [(3 × Decimation Rate) × (SEQUENCE_STAGE_NUM +1) × (FF_SKIP_CNT +1) × 4x10^{-7}]

Slow FIFO update rate in low power mode is equal to

(AVG_LP_SKIP +1) × [(3 × Decimation Rate) × (SEQUENCE_STAGE_NUM +1) × (FF_SKIP_CNT +1) × 4x10^{-7}]/[(FF_SKIP_CNT +1) + LP_CONV_DELAY]

The slow FIFO is used by the on-chip logic to track the ambient capacitance value. The slow FIFO expects to receive samples from the converter at a rate of 25 ms. AVG_FP_SKIP and AVG_LP_SKIP are used to normalize the frequency of the samples going into the FIFO, regardless of how many conversion stages are in a sequence.

Determining the AVG_FP_SKIP and AVG_LP_SKIP values is required only once during the initial setup of the capacitance sensor interface. When using all eight conversion stages, recommended values for these settings are

AVG_FP_SKIP = 00 = skip 3 samples

AVG_LP_SKIP = 00 = skip 0 samples

SLOW_FILTER_UPDATE_LVL

The SLOW_FILTER_UPDATE_LVL (Address 0x003[15:14]) controls whether the most recent CDC measurement goes into the slow FIFO (slow filter) or not. The slow filter is updated when the difference between the current CDC value and last value pushed into the slow FIFO is greater than SLOW_FILTER_UPDATE_LVL.

Equations for On-Chip Logic Stage High and Logic Stage Low Threshold Calculation

$$STAGEx\_HIGH\_THRESHOLD = STAGE\_SF\_AMBIENT + \left(\frac{STAGEx\_OFFSET\_HIGH}{4}\right) + \left(\frac{STAGEx\_OFFSET\_HIGH - \frac{STAGEx\_OFFSET\_HIGH}{4}}{16}\right) \times POS\_THRESHOLD\_SENSITIVITY \quad (1)$$

$$STAGEx\_LOW\_THRESHOLD = STAGE\_SF\_AMBIENT + \left(\frac{STAGEx\_OFFSET\_LOW}{4}\right) + \left(\frac{STAGEx\_OFFSET\_LOW - \frac{STAGEx\_OFFSET\_LOW}{4}}{16}\right) \times POS\_THRESHOLD\_SENSITIVITY \quad (2)$$

ADAPTIVE THRESHOLD AND SENSITIVITY

The AD7148 provides an on-chip self-learning adaptive threshold and sensitivity algorithm. This algorithm continuously monitors the output levels of each sensor and automatically rescales the threshold levels proportionally to the sensor area covered by the user. As a result, the AD7148 maintains optimal threshold and sensitivity levels for all types of users, regardless of finger size.

The threshold level is always referenced from the ambient level and is defined as the CDC converter output level that must be exceeded for a valid sensor contact. The sensitivity level is defined as how sensitive the sensor is before a valid contact is registered.

Figure 34 provides an example of how the adaptive threshold and sensitivity algorithm works. The positive and negative sensor threshold levels are calculated as a percentage of the STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW values, based on the threshold sensitivity settings and the ambient value. On configuration, initial estimates are supplied for both STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW, after which the calibration engine automatically adjusts the STAGEx_HIGH_THRESHOLD and STAGEx_LOW_THRESHOLD values for sensor response.

The AD7148 tracks the average maximum and minimum values measured from each sensor. These values give an indication of how the user is interacting with the sensor. A large finger gives a large average maximum or minimum value, and a small finger gives smaller values. When the average maximum or minimum value changes, the threshold levels are rescaled to ensure that the threshold levels are appropriate for the current user. Figure 35 shows how the minimum and maximum sensor responses are tracked by the on-chip logic.

Reference A in Figure 34 shows an undersensitive threshold level for a small finger user, demonstrating the disadvantages of a fixed threshold level.

By enabling the adaptive threshold and sensitivity algorithm, the positive and negative threshold levels are determined by the POS_THRESHOLD_SENSITIVITY and NEG_THRESHOLD_SENSITIVITY values and the most recent average maximum sensor output value. These bits can be used to select 16 different positive and negative sensitivity levels ranging between 25% and 95.32% of the most recent average maximum output level referenced from the ambient value. The smaller the sensitivity percentage setting, the easier it is to trigger a sensor activation. Reference B shows that the positive adaptive threshold level is set at almost mid-sensitivity with a 62.51% threshold level by setting POS_THRESHOLD_SENSITIVITY = 1000. Figure 34 also provides a similar example for the negative threshold level with NEG_THRESHOLD_SENSITIVITY = 0011.

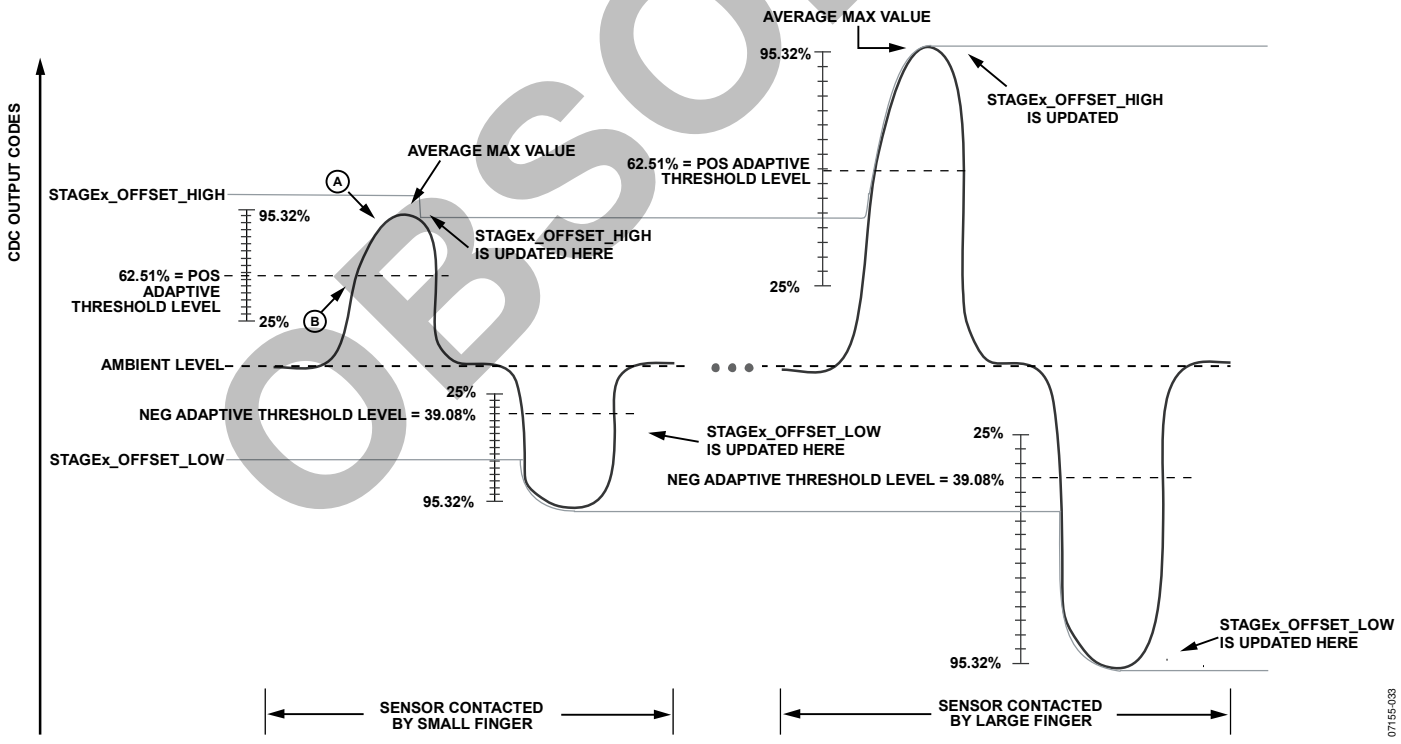


Figure 34. Threshold Sensitivity Example with POS_THRESHOLD_SENSITIVITY = 1000 and NEG_THRESHOLD_SENSITIVITY = 0011

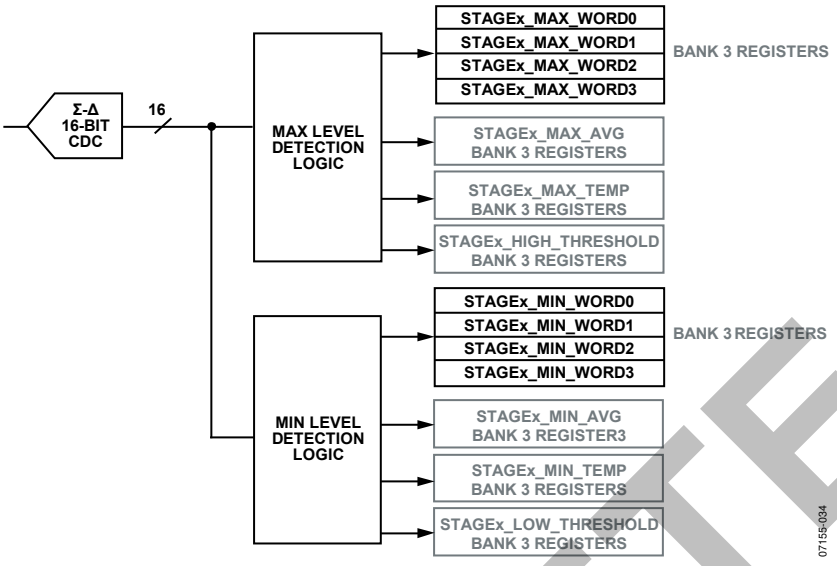


Figure 35. Tracking the Minimum and Maximum Average Sensor Values

Table 14. Additional Information About Environmental Calibration and Adaptive Threshold Registers

Bit	Register Location	Description
NEG_THRESHOLD_SENSITIVITY	Bank 2	Used in Equation 2. This value is programmed once at startup.
NEG_PEAK_DETECT	Bank 2	Used by internal adaptive threshold logic only. The NEG_PEAK_DETECT is set to a percentage of the difference between the ambient CDC value and the minimum average CDC value. If the output of the CDC gets within the NEG_PEAK_DETECT percentage of the minimum average, only then is the minimum average value updated.
POS_THRESHOLD_SENSITIVITY	Bank 2	Used in Equation 1. This value is programmed once at startup.
POS_PEAK_DETECT	Bank 2	Used by internal adaptive threshold logic only. The POS_PEAK_DETECT is set to a percentage of the difference between the ambient CDC value and the maximum average CDC value. If the output of the CDC gets within the POS_PEAK_DETECT percentage of the maximum average, only then is the maximum average value updated.
STAGEx_OFFSET_LOW	Bank 2	Used in Equation 2. An initial value (based on sensor characterization) is programmed into this register at startup. The AD7148 on-chip calibration algorithm automatically updates this register based on the amount of sensor drift due to changing ambient conditions. Set to 80% of the STAGEx_OFFSET_LOW_CLAMP value.
STAGEx_OFFSET_HIGH	Bank 2	Used in Equation 1. An initial value (based on sensor characterization) is programmed into this register at startup. The AD7148 on-chip calibration algorithm automatically updates this register based on the amount of sensor drift due to changing ambient conditions. Set to 80% of the STAGEx_OFFSET_HIGH_CLAMP value.
STAGEx_OFFSET_HIGH_CLAMP	Bank 2	Used by internal environmental calibration and adaptive threshold algorithms only. An initial value (based on sensor characterization) is programmed into this register at startup. The value in this register prevents a user from causing sensor output value to exceed the expected nominal value. Set to the maximum expected sensor response, maximum change in CDC output code.
STAGEx_OFFSET_LOW_CLAMP	Bank 2	Used by internal environmental calibration and adaptive threshold algorithms only. An initial value (based on sensor characterization) is programmed into this register at startup. The value in this register prevents a user from causing sensor output value to exceed the expected nominal value. Set to the minimum expected sensor response, minimum change in CDC output code .
STAGEx_SF_AMBIENT	Bank 3	Used in Equation 1 and Equation 2. This is the ambient sensor output, when the sensor is not touched, as calculated using the slow FIFO.
STAGEx_HIGH_THRESHOLD	Bank 3	Equation 1 value.
STAGEx_LOW_THRESHOLD	Bank 3	Equation 2 value.