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Low Power, 8-/16-Channel, 31.25 kSPS, 24-Bit, Highly Integrated Sigma-Delta ADC

Data Sheet **AD7173-8**

FEATURES

- Low power, 8-/16-channel, highly integrated multiplexed analog-to-digital converter (ADC)
- Integration
  - Precision analog input buffers and reference input buffers
  - 2.5 V precision reference (3.5 ppm/°C)
  - Cross point multiplexer (enable system diagnostic)
  - 8 full differential or 16 single-ended channels
  - Clock oscillator
  - GPIO and GPO pins with automatic external mux control
- Fast and flexible output rate: 1.25 SPS to 31.25 kSPS
- Channel scan data rate: 6.21 kSPS/channel (161 µs settling)
- Performance specifications
  - 17.5 noise free bits at 31.25 kSPS
  - 24 noise free bits at 1.25 SPS
  - INL: ±3 ppm/FSR
- 85 dB rejection of 50 Hz and 60 Hz with 50 ms settling
- Operates with either 3.3 V or5 V supply
  - Single supply
    - 3.3 V or 5 V AVDD1, 2 V to 5 V AVDD2, and 2 V to 5 V IOVDD
  - Optional split supply
    - AVDD1 and AVSS ± 2.5 V or AVDD1 and AVSS ± 1.65 V
  - Current: 1.4 mA
- 3-/4-wire serial digital interface (Schmitt trigger on SCLK)
  - CRC error checking
  - SPI, QSPI, MICROWIRE, and DSP compatible
- Package: 40-lead 6 mm × 6 mm LFCSP
- Temperature range: −40°C to +105°C

APPLICATIONS

- Process control: PLC/DCS modules
  - Voltage, current, temperature, and pressure measurement
  - Flow meters
- Medical and scientific multichannel instrumentation
- Seismic instrumentation
- Chemical analysis instrumentation: chromatography

GENERAL DESCRIPTION

Fast settling, highly accurate, low power, 8-/16-channel, multiplexed ADC for low bandwidth input signals with integrated input buffers.

Integrated precision, 2.5 V, low drift (3.5 ppm/°C), band gap reference and integrated oscillator.

Eight flexible setups with configurability for output data rate, digital filter mode, offset/gain error correction, reference selection, buffer enables and more. This per channel configurability extends to the output data rate used for each channel when using sinc5 + sinc1 filter.

Sinc5 + sinc1 filter maximizes channel scan rate, and sinc3 filter maximizes resolution and enhanced 50 Hz/60 Hz rejection, with four selectable options to maximize rejection.

Integrated diagnostic features, including CRC, register checksum, temperature sensor, crosspoint multiplexer, burnout currents, and GPIOs/GPOs.

FUNCTIONAL BLOCK DIAGRAM

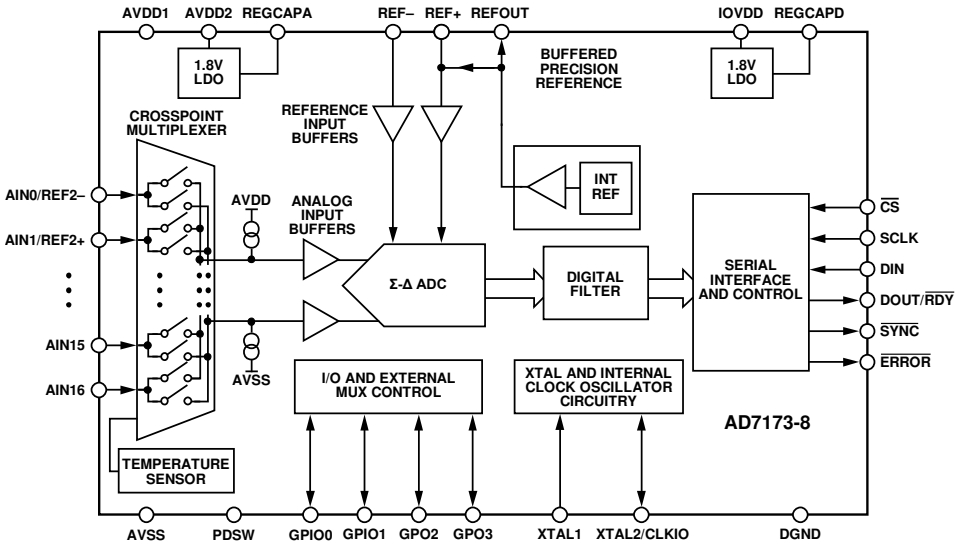

Figure 1.

Rev. A Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

AD7173-8* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7173-8SDZ Evaluation Board

DOCUMENTATION

Data Sheet

- AD7173-8: Low Power, 8-/16-Channel, 31.25 kSPS, 24-Bit, Highly Integrated Sigma-Delta ADC Data Sheet

Technical Books

- The Data Conversion Handbook, 2005

User Guides

- UG-631: Evaluating the AD7173-8 24-Bit, 31.25 kSPS, Sigma-Delta ADC with 161 µs Settling and Integrated Analog Input Buffers

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD717x Microcontroller No-OS
- AD717x Eval+ Software

TOOLS AND SIMULATIONS

- AD7173-8 Filter Model
- AD7173-8 IBIS Model

REFERENCE DESIGNS

- CN0292
- CN0364

REFERENCE MATERIALS

Technical Articles

- Flexible Bandwidth 4 mA to 20 mA Current Input with Easy HART Compatibility

Tutorials

- MT-022: ADC Architectures III: Sigma-Delta ADC Basics
- MT-023: ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications

DESIGN RESOURCES

- AD7173-8 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7173-8 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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4/14—Rev. 0 to Rev. A

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10/13—Revision 0: Initial Version

SPECIFICATIONS

AVDD1 = 3.0 V to 5.5 V, AVDD2 = 2 V to 5.5 V, IOVDD = 2 V to 5.5 V, AVSS = DGND = 0 V, REF+ = 2.5 V, REF− = AVSS, internal master clock = 2 MHz, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPEED AND PERFORMANCE					
Output Data Rate (ODR)		1.25		31250	SPS
No Missing Codes[1]	Excluding sinc3 filter at 31.25 kSPS	24			Bits
Resolution	See Table 6				
Noise	See Table 6				
Noise Free Resolution	Sinc5 + sinc1 filter (default)				
	31.25 kSPS, REF+ = 5 V		17.5		Bits
	2.6 kSPS, REF+ = 5 V		18.4		Bits
	1.25 SPS, REF+ = 5 V		24		Bits
ACCURACY					
Integral Nonlinearity (INL)	2.5 V reference		±3	±7.5	ppm/FSR
	5 V reference		±5		ppm/FSR
Offset Error[2]	Internal short		±40		µV
Offset Drift	Internal short		±350		nV/°C
Offset Drift vs. Time[3]			±450		nV/1000 hrs
Gain Error[2]	25°C, AVDD1 = 5 V		±10	±50	ppm/FSR
Gain Drift vs. Temperature[1]			±0.5	±1	ppm/FSR/°C
Gain Drift vs. Time[3]			±3		ppm/FSR/ 1000 hrs
REJECTION					
Power Supply Rejection	AVDD1 and AVDD2, V_{IN} = 1 V		90		dB
Common-Mode Rejection	V_{IN} = 0.1 V				
At DC		95			dB
At 50 Hz and 60 Hz[1]	20 SPS ODR (post filter); 50 Hz ± 1 Hz and 60 Hz ± 1 Hz	120			dB
Normal Mode Rejection[1]	50 Hz ± 1 Hz and 60 Hz ± 1 Hz				
	Internal clock, 20 SPS ODR (post filter)	71	90		dB
	External clock, 20 SPS ODR (post filter)	85	90		dB
ANALOG INPUTS					
Differential Input Voltage Range			$\pm V_{REF}$		V
Absolute AIN Voltage Limits[1]					
Buffers Disabled		AVSS − 0.05		AVDD1 + 0.05	V
Buffers Enabled		AVSS		AVDD1 − 1.1	V
Analog Input Current					
Buffers Enabled	Single cycle settling enabled (default)				
Input Current			±2		nA
Input Current Drift			±25		pA/°C
Buffers Disabled					
Input Current			±6		µA/V
Input Current Drift	External clock		±0.1		nA/V/°C
	Internal clock (±2.5% clock)		±0.5		nA/V/°C
Crosstalk	1 kHz input		−120		dB
INTERNAL REFERENCE	100 nF external capacitor on REFOUT to AVSS				
Output Voltage	REFOUT with respect to AVSS		2.5		V
Initial Accuracy[1]	T_A = 25°C[4]	−0.1		+0.1	% of V
Temperature Coefficient					
0°C to +105°C			3.5	8	ppm/°C
−40°C to +105°C			3.5	10	ppm/°C
Reference Load Current, I_{LOAD}	I_L	−10		+10	mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Power Supply Rejection (Line Regulation)	AVDD1 and AVDD2		90		dB
Load Regulation	$\Delta V_{OUT}/\Delta I_L$		140		ppm/mA
Voltage Noise	e_N, 0.1 Hz to 10 Hz		6.5		μV rms
Voltage Noise Density	e_N, 1 kHz		215		nV/√Hz
Turn-On Settling Time	100 nF capacitor		60		μs
Long-Term Stability[3]	1000 hours		460		ppm
Short Circuit	I_{SC}		25		mA
EXTERNAL REFERENCE					
Reference Input Voltage	Reference input = (REF+) − (REF−)	1	2.5	AVDD1	V
Absolute Reference Input Voltage Limits[1]					
Buffers Disabled		AVSS − 0.05		AVDD1 + 0.05	V
Buffers Enabled		AVSS		AVDD1	V
Average Reference Input Current					
Buffers Disabled			±9		μA/V
Buffers Enabled			±50		nA
Average Reference Input Current Drift	Buffers disabled				
External clock			±5		nA/V/°C
Internal clock			±6		nA/V/°C
Normal Mode Rejection[1]	See the Rejection parameter				
Common-Mode Rejection			83		dB
TEMPERATURE SENSOR					
Accuracy	After user calibration at 25°C		±2		°C
Sensitivity			477		μV/°C
BURNOUT CURRENTS					
Source/Sink Current	Analog input buffers must be enabled		±10		μA
BRIDGE POWER-DOWN SWITCH					
R_{ON}			24		Ω
Allowable Currents				16	mA
GENERAL-PURPOSE I/O (GPIO0, GPIO1, GPO2, GPO3)	With respect to AVSS				
Input Mode Leakage Current[1]		−10		+10	μA
Floating State Output Capacitance			5		pF
AVDD1 − AVSS = 5 V					
Output High Voltage, V_{OH}[1]	I_{SOURCE} = 200 μA	AVSS + 4			V
Output Low Voltage, V_{OL}[1]	I_{SINK} = 800 μA			AVSS + 0.4	V
Input High Voltage, V_{IH}[1]		AVSS + 3			V
Input Low Voltage, V_{IL}[1]				AVSS + 0.7	V
AVDD1 − AVSS = 3.3 V					
Output High Voltage, V_{OH}[1]	I_{SOURCE} = 200 μA	AVSS + 2.7			V
Output Low Voltage, V_{OL}[1]	I_{SINK} = 800 μA			AVSS + 0.27	V
Input High Voltage, V_{IH}[1]		AVSS + 2			V
Input Low Voltage, V_{IL}[1]				AVSS + 0.45	V
CLOCK					
Internal Clock					
Frequency			2		MHz
Accuracy		−2.5		+2.5	%
Duty Cycle			50:50		
Output Low Voltage, V_{OL}				0.4	V
Output High Voltage, V_{OH}		0.8 × IOVDD			V
Crystal					
Frequency		14	16	16.384	MHz
Start-Up Time			10		μs
External Clock (CLKIO)			2	2.048	MHz
Duty Cycle[1]	Typical duty cycle 50:50 (maximum:minimum)	30:70	50:50	70:30	

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS					
Input High Voltage, V_{INH}[1]	2 V ≤ IOVDD ≤ 2.3 V	0.65 × IOVDD			V
	2.3 V ≤ IOVDD ≤ 5.5 V	0.7 × IOVDD			V
Input Low Voltage, V_{INL}[1]	2 V ≤ IOVDD ≤ 2.3 V			0.35 × IOVDD	V
	2.3 V ≤ IOVDD ≤ 5.5 V			0.7	V
Hysteresis[1]	IOVDD > 2.7 V	0.08		0.25	V
	IOVDD < 2.7 V	0.04		0.2	V
Leakage Currents		−10		+10	µA
LOGIC OUTPUT (DOUT/$\overline{RDY}$)					
Output High Voltage, V_{OH}[1]	IOVDD ≥ 4.5 V, I_{SOURCE} = 1 mA	0.8 × IOVDD			V
	2.7 V ≤ IOVDD < 4.5 V, I_{SOURCE} = 500 µA	0.8 × IOVDD			V
	IOVDD < 2.7 V, I_{SOURCE} = 200 µA	0.8 × IOVDD			V
Output Low Voltage, V_{OL}[1]	IOVDD ≥ 4.5 V, I_{SINK} = 2 mA			0.4	V
	2.7 V ≤ IOVDD < 4.5 V, I_{SINK} = 1 mA			0.4	V
	IOVDD < 2.7 V, I_{SINK} = 400 µA			0.4	V
Leakage Current	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF
SYSTEM CALIBRATION[1]					
Full-Scale Calibration Limit				1.05 × FS	V
Zero-Scale Calibration Limit		−1.05 × FS			V
Input Span		0.8 × FS		2.1 × FS	V
POWER REQUIREMENTS					
Power Supply Voltage					
AVDD1 − AVSS		3.0		5.5	V
AVDD2 − AVSS		2		5.5	V
AVSS − DGND		−2.75		0	V
IOVDD − DGND		2		5.5	V
IOVDD − AVSS	For AVSS < DGND			6.35	V
POWER SUPPLY CURRENTS	All outputs unloaded				
Full Operating Mode					
AVDD1 Current					
AVDD1 = 5 V Typical, 5.5 V Maximum	AIN± and REF± buffers disabled; external reference		0.23	0.27	mA
	AIN± and REF± buffers disabled; internal reference		0.42	0.49	mA
	AIN± and REF± buffers enabled; external reference		2.12	2.71	mA
	Each enabled buffered pair: AIN+, AIN− and REF+, REF−		0.945	1.22	mA
AVDD1 = 3.3 V Typical, 3.6 V Maximum[1]	AIN± and REF± buffers disabled; external reference		0.16	0.19	mA
	AIN± and REF± buffers disabled; internal reference		0.34	0.4	mA
	AIN± and REF± buffers enabled; external reference		1.9	2.45	mA
	Each enabled buffered pair: AIN+, AIN− and REF+, REF−		0.87	1.13	mA
AVDD2 Current	External reference		1	1.15	mA
	Internal reference		1.25	1.4	mA
IOVDD Current	External clock		0.24	0.39	mA
	Internal clock		0.52	0.76	mA
	External crystal		0.9		mA
Standby Mode					
Standby (LDO on)	Reference off, total current consumption		25		µA
	Reference on, total current consumption		400		µA
Power-Down Mode	Full power-down, LDO, REF±		2	10	µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER DISSIPATION					
Full Operating Mode	Unbuffered, external clock and reference; AVDD1 = 3.3 V, AVDD2 = 2 V, IOVDD = 2 V		3		mW
	Unbuffered, external clock and reference; all supplies = 5 V		7.35		mW
	Unbuffered, external clock and reference; all supplies = 5.5 V			9.96	mW
	Fully buffered, internal clock and reference (note that REFOUT has no load); AVDD1 = 3.3 V, AVDD2 = 2 V, IOVDD = 2 V		10.4		mW
	Fully buffered, internal clock and reference (note that REFOUT has no load); all supplies = 5 V		20.4		mW
	Fully buffered, internal clock and reference (note that REFOUT has no load); all supplies = 5.5 V			28	mW
Standby Mode	Reference off, all supplies = 5 V		125		µW
	Reference on, all supplies = 5 V		2		mW
Power-Down Mode	Full power-down, all supplies = 5 V		10		µW
	Full power-down, all supplies = 5.5 V			55	µW

[1] Specification is not production tested but is supported by characterization data at the initial product release.
[2] Following a system or internal zero-scale calibration, the offset error is in the order of the noise for the programmed output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed output data rate.
[3] This specification is noncumulative and includes MSL preconditioning effects.
[4] This specification includes MSL preconditioning effects.

TIMING CHARACTERISTICS

IOVDD = 2 V to 5.5 V, DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = IOVDD, C_{LOAD} = 20 pF, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Test Conditions/Comments[1, 2]
SCLK PULSE WIDTH			
t_3	25	ns min	SCLK high pulse width
t_4	25	ns min	SCLK low pulse width
READ OPERATION			
t_1	0	ns min	$\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time
	15	ns max	IOVDD = 4.5 V to 5.5 V
	40	ns max	IOVDD = 2 V to 3.6 V
t_2[3]	0	ns min	SCLK active edge to data valid delay[4]
	12	ns max	IOVDD = 4.5 V to 5.5 V
	25	ns max	IOVDD = 2 V to 3.6 V
t_5[5]	2.5	ns min	Bus relinquish time after $\overline{CS}$ inactive edge
	20	ns max	
t_6	0	ns min	SCLK inactive edge to $\overline{CS}$ inactive edge
t_7	10	ns min	SCLK inactive edge to DOUT/$\overline{RDY}$ high/low
WRITE OPERATION			
t_8	0	ns min	$\overline{CS}$ falling edge to SCLK active edge setup time[4]
t_9	8	ns min	Data valid to SCLK edge setup time
t_{10}	8	ns min	Data valid to SCLK edge hold time
t_{11}	5	ns min	$\overline{CS}$ rising edge to SCLK edge hold time

[1] Sample tested during initial release to ensure compliance.
[2] See Figure 2 and Figure 3.
[3] The time required for the output to cross the V_{OL} or V_{OH} limits.
[4] The SCLK active edge is the falling edge of SCLK.
[5] $\overline{RDY}$ returns high after a read of the data register. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high. It is important to ensure that subsequent reads do not occur close to the next output update. If the continuous read feature is enabled, the digital word can be read only once.

Timing Diagrams

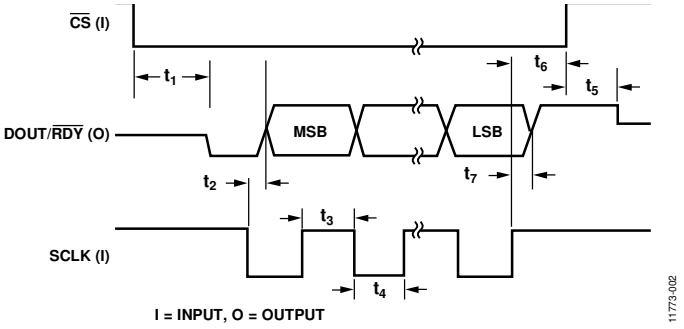


Figure 2. Read Cycle Timing Diagram

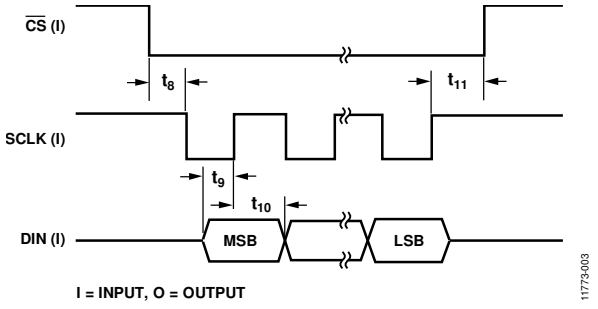


Figure 3. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AVDD1, AVDD2 to AVSS	−0.3 V to +6.5 V
AVDD1 to DGND	−0.3 V to +6.5 V
IOVDD to DGND	−0.3 V to +6.5 V
IOVDD to AVSS	−0.3 V to +7.5 V
AVSS to DGND	−3.25 V to +0.3 V
Analog Input Voltage to AVSS	−0.3 V to AVDD1 + 0.3 V
Reference Input Voltage to AVSS	−0.3 V to AVDD1 + 0.3 V
Digital Input Voltage to DGND	−0.3 V to IOVDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to IOVDD + 0.3 V
AIN[16:0] or Digital Input Current	10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Soldering, Reflow Temperature	260°C
ESD Rating (HBM)	4 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device soldered on a JEDEC test board for surface-mount packages. The values listed in Table 4 are based on simulated data.

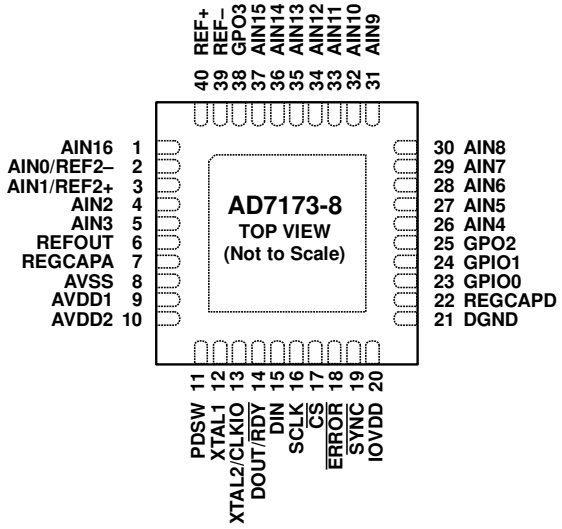
Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
40-Lead, 6 mm × 6 mm LFCSP		
1-Layer JEDEC Board	114	°C/W
4-Layer JEDEC Board	54	°C/W
4-Layer JEDEC Board with 16 Thermal Vias	34	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD SHOULD BE SOLDERED TO A SIMILAR PAD ON THE PCB UNDER THE EXPOSED PAD TO CONFER MECHANICAL STRENGTH AND FOR HEAT DISSIPATION. THE EXPOSED PAD MUST BE CONNECTED TO AVSS THROUGH THIS PAD ON THE PCB.

11773-004

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	AIN16	AI	Analog Input 16. Selectable through cross point mux.
2	AIN0/REF2–	AI	Analog Input 0 (AIN0)/Reference 2, Negative Input (REF2–). An external reference can be applied between REF2+ and REF2–. REF2– can span from AVSS to AVDD1 − 1 V. Analog Input 0 is selectable through cross point mux. Reference 2 can be selected through the REFSEL bits in the setup configuration register.
3	AIN1/REF2+	AI	Analog Input 1 (AIN0)/Reference 2, Positive Input (REF2+). An external reference can be applied between REF2+ and REF2–. REF2+ can span from AVDD1 to AVSS + 1 V. Analog Input 1 is selectable through cross point mux. Reference 2 can be selected through the REFSEL bits in the setup configuration register.
4	AIN2	AI	Analog Input 2. Selectable through cross point mux.
5	AIN3	AI	Analog Input 3. Selectable through cross point mux.
6	REFOUT	AO	Buffered Output of Internal Reference. The output is 2.5 V with respect to AVSS.
7	REGCAPA	AO	Analog LDO Regulator Output. Decouple this pin to AVSS using a 1 µF capacitor.
8	AVSS	P	Negative Analog Supply. This supply ranges from 0 V to −2.75 V and is nominally set to 0 V.
9	AVDD1	P	Analog Supply Voltage 1. This voltage ranges from 3.0 V minimum to 5.5 V maximum with respect to AVSS.
10	AVDD2	P	Analog Supply Voltage 2. This voltage ranges from 2 V to AVDD1 with respect to AVSS.
11	PDSW	AO	Power-Down Switch Connected to AVSS. This pin is controlled by the PDSW bit in the GPIOCON register.
12	XTAL1	AI	Input 1 for Crystal.
13	XTAL2/CLKIO	AI/DI	Input 2 for Crystal (XTAL2)/Clock Input or Output (CLKIO). See the CLOCKSEL bit settings in the ADCMODE register (Table 25) for more information.
14	DOUT/$\overline{\text{RDY}}$	DO	Serial Data Output (DOUT)/Data Ready Output ($\overline{\text{RDY}}$). This pin serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. The data-word/control word information is placed on the DOUT/$\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. When $\overline{\text{CS}}$ is high, the DOUT/$\overline{\text{RDY}}$ output is tristated. When $\overline{\text{CS}}$ is low, and a register is not being read, DOUT/$\overline{\text{RDY}}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available.

Pin No.	Mnemonic	Type[1]	Description
15	DIN	DI	Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers in the ADC, with the register address (RA) bits of the communications register identifying the appropriate register. Data is clocked in on the rising edge of SCLK.
16	SCLK	DI	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. SCLK has a Schmitt trigger input, making the interface suitable for opto-isolated applications.
17	$\overline{CS}$	DI	Chip Select Input. This is an active low logic input used to select the ADC. $\overline{CS}$ can be used to select the ADC in systems with more than one device on the serial bus. $\overline{CS}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device. When $\overline{CS}$ is high, the DOUT/$\overline{RDY}$ output is tristated.
18	$\overline{ERROR}$	DI/O	This pin can be used in one of the following three modes: Active low error input mode. This mode sets the ADC_ERROR bit in the STATUS register. Active low, open-drain error output mode. The STATUS register error bits are mapped to the $\overline{ERROR}$ pin. The $\overline{ERROR}$ pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed. General-purpose output mode. The status of the pin is controlled by the ERR_DAT bit in the GPIOCON register. The pin is referenced between IOVDD and DGND, as opposed to the AVDD1 and AVSS levels used by the GPIO1 and GPIO2 pins. The $\overline{ERROR}$ pin has an active pull-up in this case.
19	$\overline{SYNC}$	DI	Synchronization Input. Allows synchronization of the digital filters and analog modulators when using multiple AD7173-8 devices.
20	IOVDD	P	Digital I/O Supply Voltage. IOVDD voltage ranges from 2 V to 5 V. IOVDD is independent of AVDD1 and AVDD2. For example, IOVDD can be operated at 3.3 V when AVDD1 or AVDD2 equals 5 V, or vice versa. If AVSS is set to −2.5 V, the voltage on IOVDD must not exceed 3.6 V.
21	DGND	P	Digital Ground.
22	REGCAPD	AO	Digital LDO Regulator Output. This pin is for decoupling purposes only. Decouple this pin to DGND using a 1 µF capacitor.
23	GPIO0	DI/O	General-Purpose Input/Output. Logic input/output on this this pin is referred to the AVDD1 and AVSS supplies.
24	GPIO1	DI/O	General-Purpose Input/Output. Logic input/output on this this pin is referred to the AVDD1 and AVSS supplies.
25	GPO2	DO	General-Purpose Output. Logic output on this this pin is referred to the AVDD1 and AVSS supplies.
26	AIN4	AI	Analog Input 4. Selectable through cross point mux.
27	AIN5	AI	Analog Input 5. Selectable through cross point mux.
28	AIN6	AI	Analog Input 6. Selectable through cross point mux.
29	AIN7	AI	Analog Input 7. Selectable through cross point mux.
30	AIN8	AI	Analog Input 8. Selectable through cross point mux.
31	AIN9	AI	Analog Input 9. Selectable through cross point mux.
32	AIN10	AI	Analog Input 10. Selectable through cross point mux.
33	AIN11	AI	Analog Input 11. Selectable through cross point mux.
34	AIN12	AI	Analog Input 12. Selectable through cross point mux.
35	AIN13	AI	Analog Input 13. Selectable through cross point mux.
36	AIN14	AI	Analog Input 14. Selectable through cross point mux.
37	AIN15	AI	Analog Input 15. Selectable through cross point mux.
38	GPO3	DO	General-Purpose Output. Logic output on this this pin is referred to the AVDD1 and AVSS supplies.
39	REF−	AI	Reference 1 Input Negative Terminal. REF− can span from AVSS to AVDD1 − 1 V. Reference 1 can be selected through the REFSEL bits in the SETUP CONFIGURATION register.
40	REF+	AI	Reference 1 Input Positive Terminal. An external reference can be applied between REF+ and REF−. REF+ can span from AVDD1 to AVSS + 1 V. Reference 1 can be selected through the REFSEL bits in the SETUP CONFIGURATION register.
	EP	P	Exposed Pad. The exposed pad should be soldered to a similar pad on the PCB under the exposed paddle to confer mechanical strength to the package and for heat dissipation. The exposed pad must be connected to AVSS through this pad on the PCB.

[1] AI = analog input, AO = analog output, DI/O = bidirectional digital input/output, DO = digital output, DI = digital input, P = power supply.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 5 V, AVDD2 = 5 V, IOVDD = 3.3 V, unless otherwise noted.

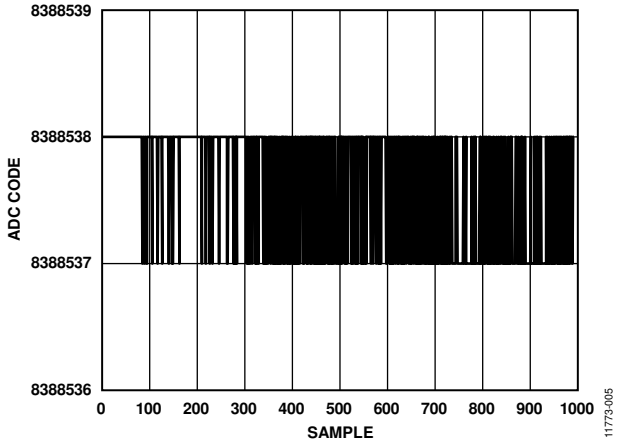


Figure 5. Noise
(Output Data Rate = 1.25 SPS, Analog Input Buffers Disabled)

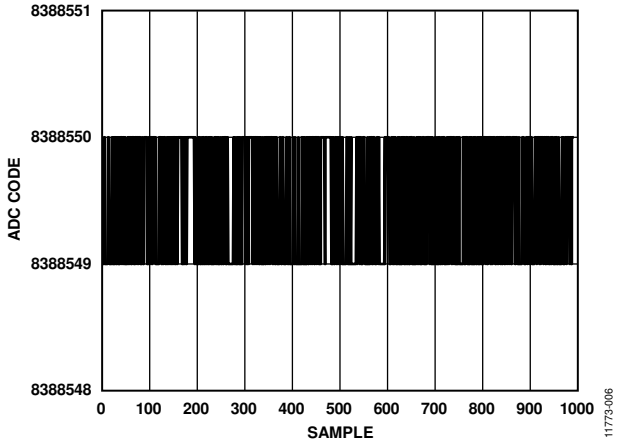


Figure 6. Noise
(Output Data Rate = 1.25 SPS, Analog Input Buffers Enabled)

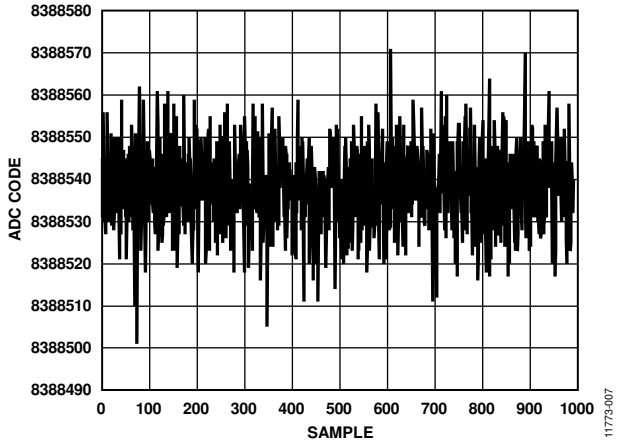


Figure 7. Noise
(Output Data Rate = 10 kSPS, Analog Input Buffers Disabled)

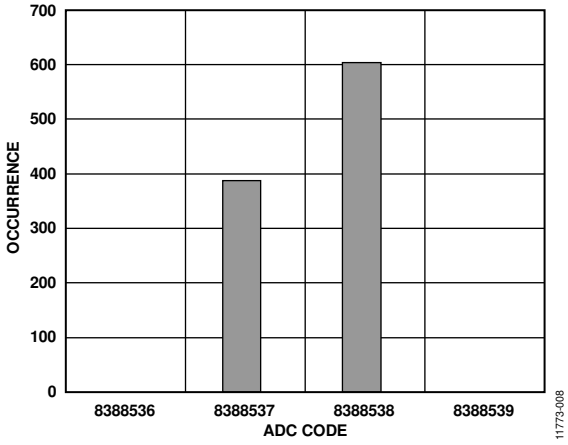


Figure 8. Noise Distribution Histogram
(Output Data Rate = 1.25 SPS, Analog Input Buffers Disabled))

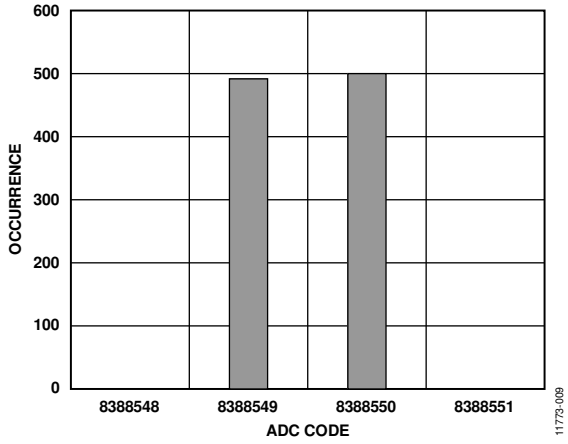


Figure 9. Noise Distribution Histogram
(Output Data Rate = 1.25 SPS, Analog Input Buffers Enabled)

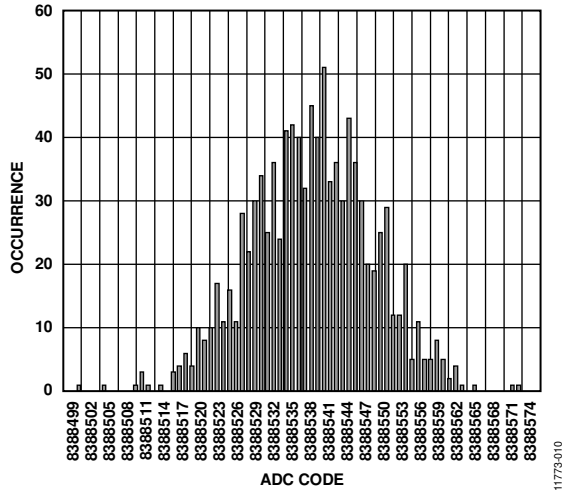


Figure 10. Noise Distribution Histogram
(Output Data Rate = 10 kSPS, Analog Input Buffers Disabled))

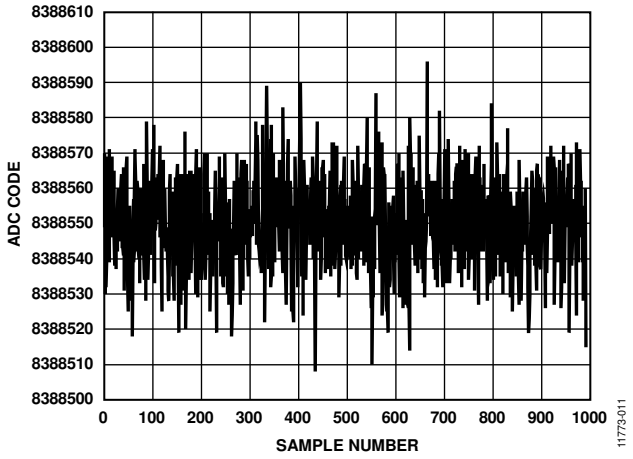


Figure 11. Noise
(Output Data Rate = 10 kSPS, Analog Input Buffers Enabled)

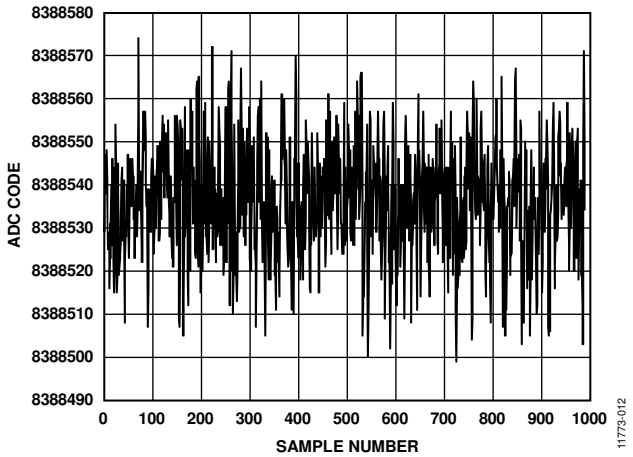


Figure 12. Noise
(Output Data Rate = 31.25 kSPS, Analog Input Buffers Disabled)

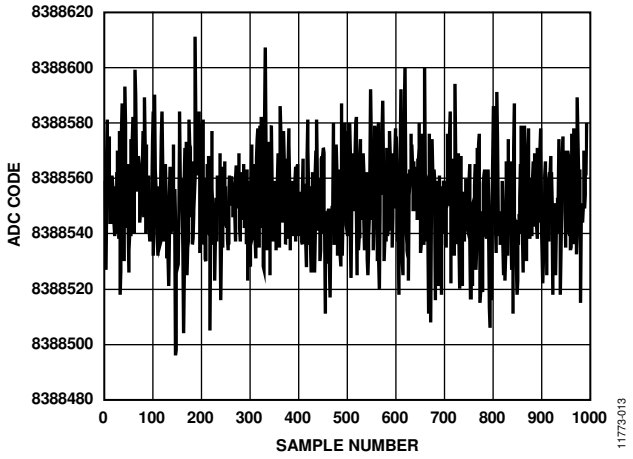


Figure 13. Noise
(Output Data Rate = 31.25 kSPS, Analog Input Buffers Enabled)

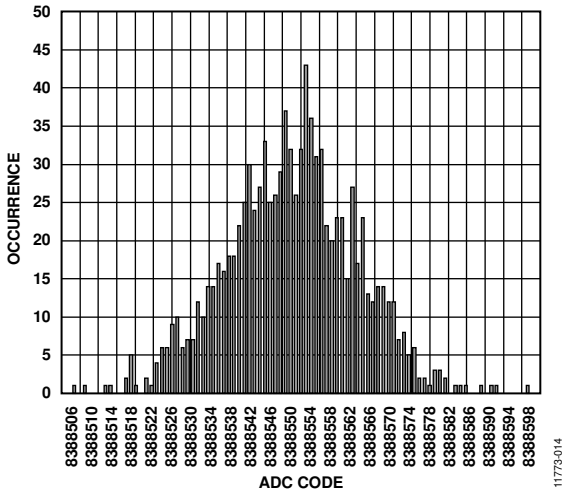


Figure 14. Noise Distribution Histogram
(Output Data Rate = 10 kSPS, Analog Input Buffers Enabled))

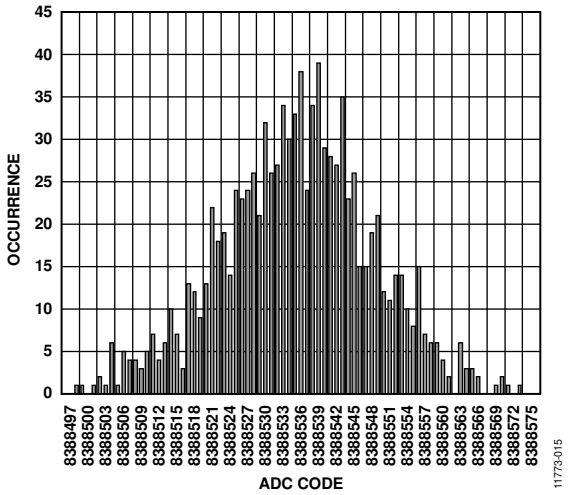


Figure 15. Noise Distribution Histogram
(Output Data Rate = 31.25 kSPS, Analog Input Buffers Disabled)

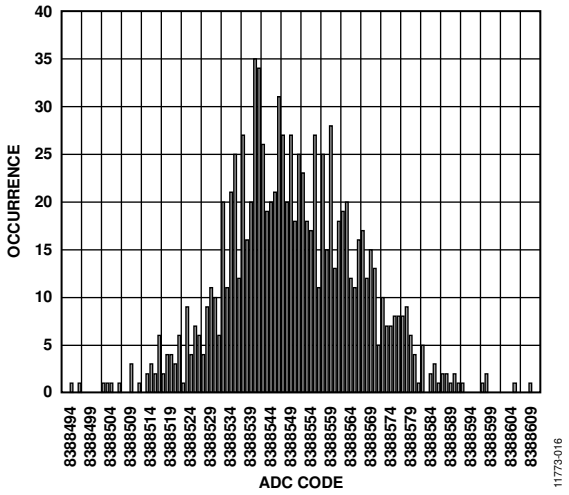


Figure 16. Noise Distribution Histogram
(Output Data Rate = 31.25 kSPS, Analog Input Buffers Enabled)

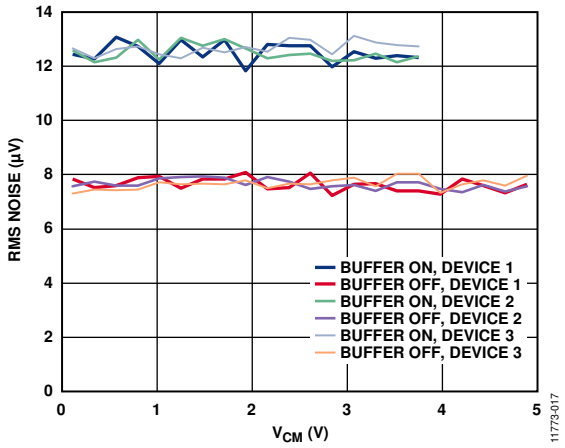


Figure 17. RMS Noise vs. Common-Mode Input Voltage

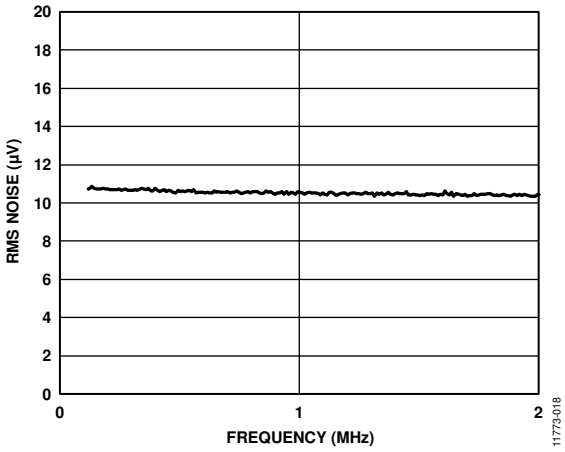


Figure 18. RMS Noise vs. Master Clock Frequency (Output Data Rate = 31.25 kSPS, Analog Input Buffers Enabled)

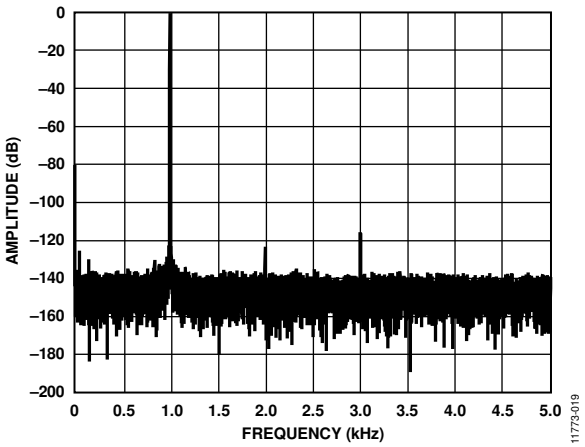


Figure 19. ADC Output FFT; 1 kHz Input Tone, −0.5 dBFS Input FFT (Output Data Rate = 10 kSPS, External Reference, External Clock, Buffers Enabled)

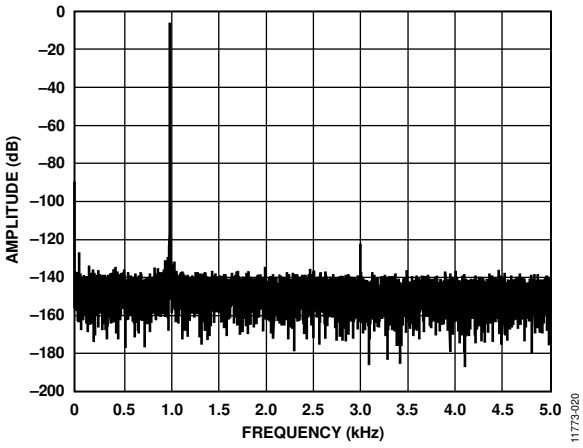


Figure 20. ADC Output FFT; 1 kHz Input Tone, −6 dBFS Input FFT (Output Data Rate = 10 kSPS, External Reference, External Clock, Buffers Enabled)

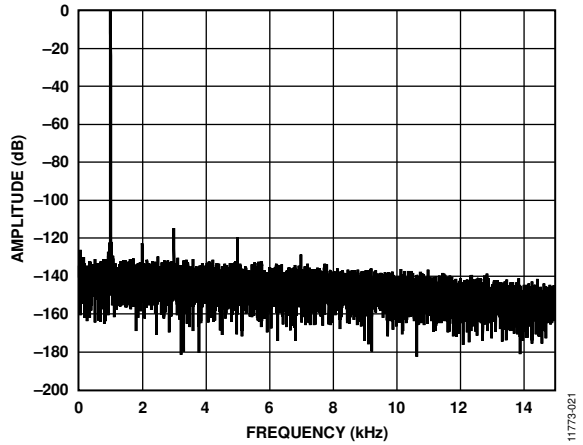


Figure 21. ADC Output FFT; 1 kHz Input Tone, −0.5 dBFS Input FFT (Output Data Rate = 31.25 kSPS, External Reference, External Clock, Buffers Enabled)

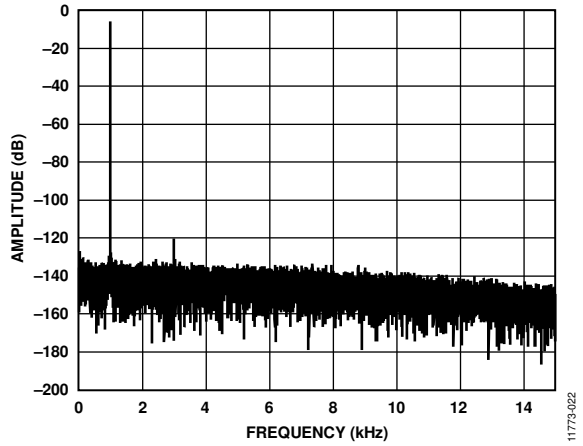


Figure 22. ADC Output FFT; 1 kHz Input Tone, −6 dBFS Input FFT (Output Data Rate = 31.25 kSPS, External Reference, External Clock, Buffers Enabled)

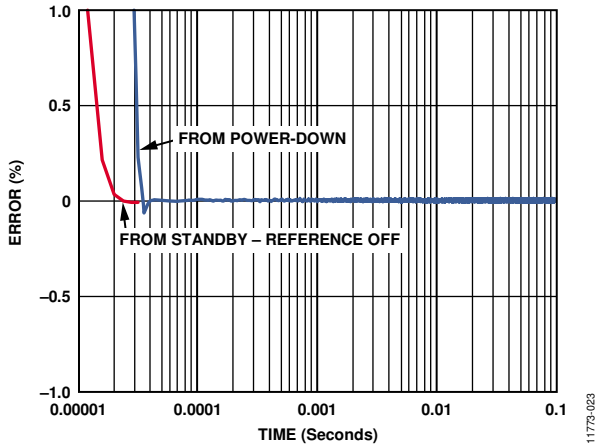


Figure 23. Internal Reference Settling Time

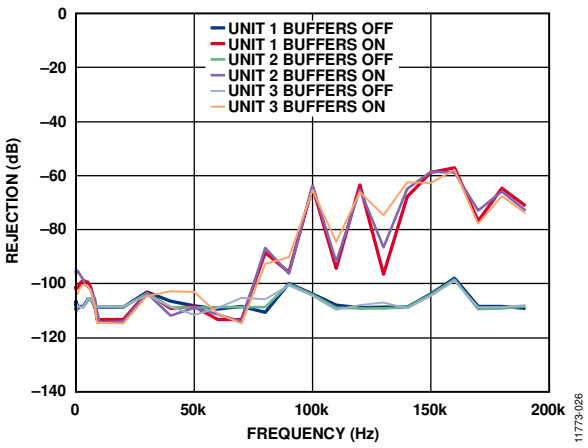


Figure 26. Common-Mode Rejection Ratio vs. Frequency (Output Data Rate = 31.25 kSPS)

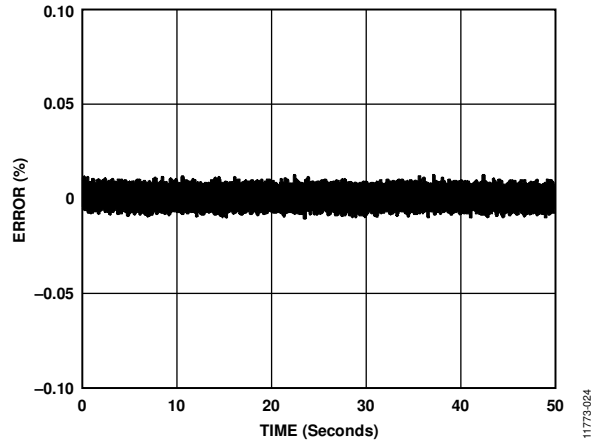


Figure 24. Internal Reference Settling Time (Extended)

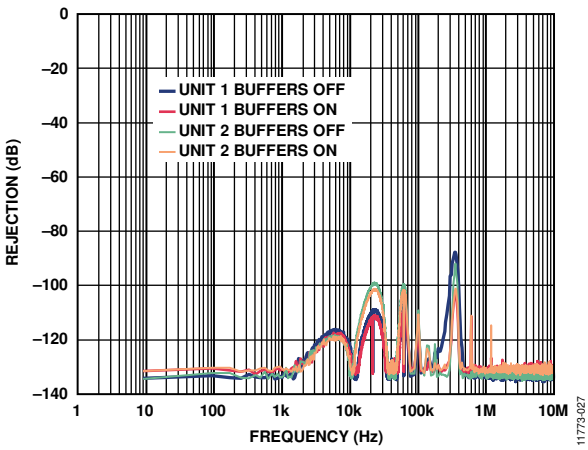


Figure 27. Power Supply Rejection Ratio vs. Frequency

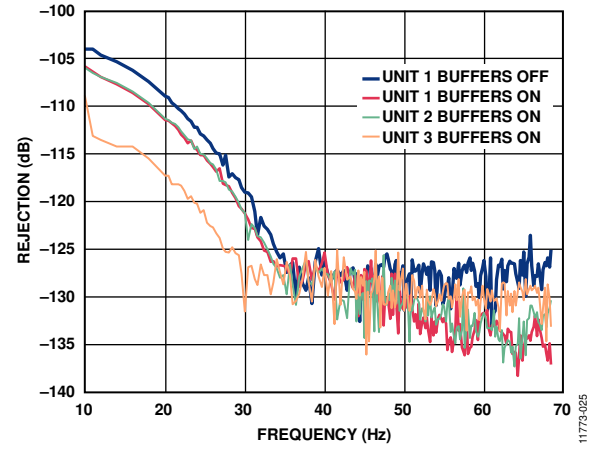


Figure 25. Common-Mode Rejection Ratio (10 Hz to 70 Hz) vs. Frequency (20 SPS Enhanced Filter)

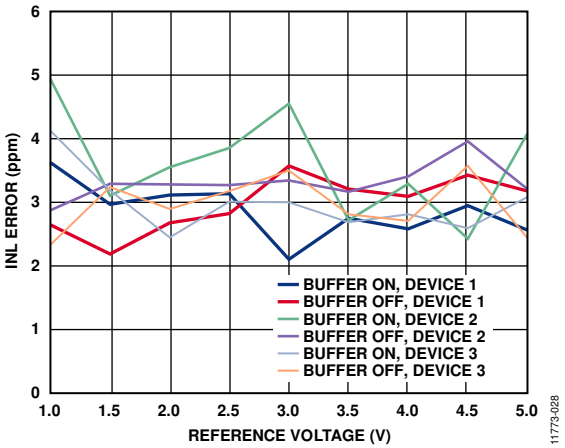


Figure 28. Integral Nonlinearity (INL) Error vs. Reference Voltage (Differential Input, External Reference)

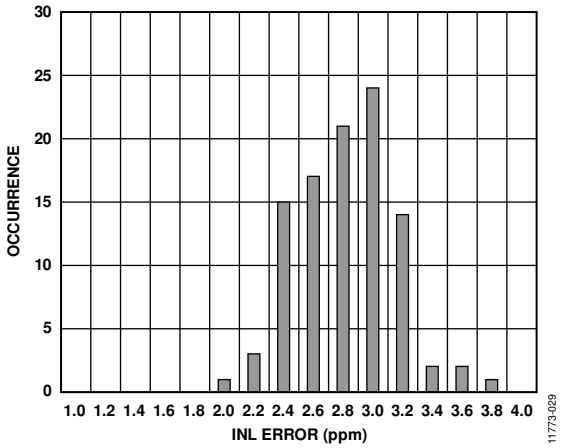


Figure 29. Integral Nonlinearity (INL) Distribution Histogram (Differential Input, V_{REF} = 2.5 V External)

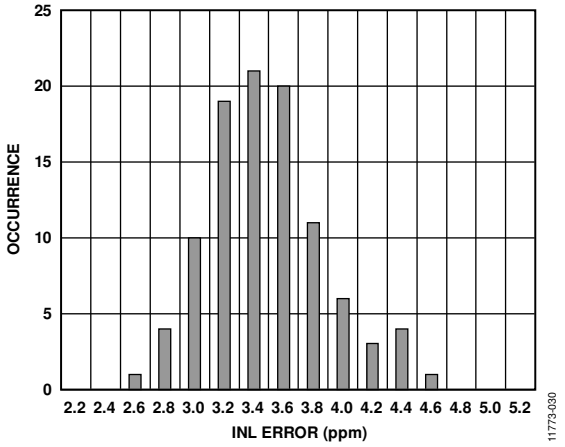


Figure 30. Integral Nonlinearity (INL) Distribution Histogram (Differential Input, V_{REF} = 5 V External)

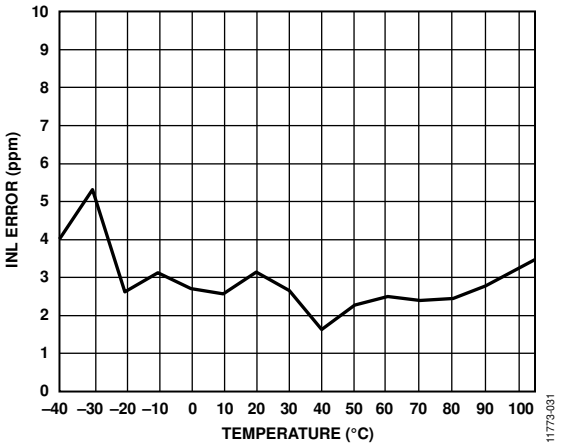


Figure 31. Integral Nonlinearity (INL) Error vs. Temperature (Differential Input, V_{REF} = 2.5 V)

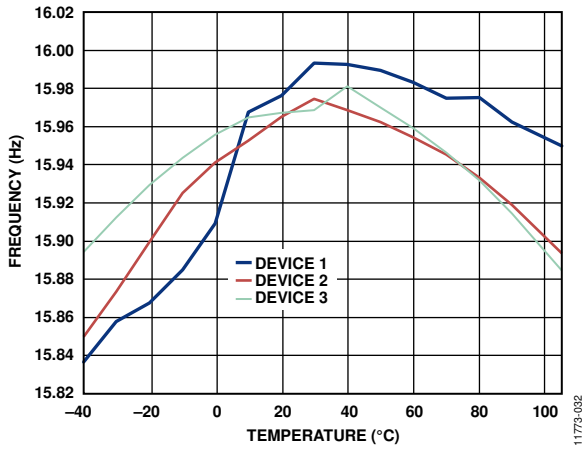


Figure 32. Internal Oscillator Frequency vs. Temperature

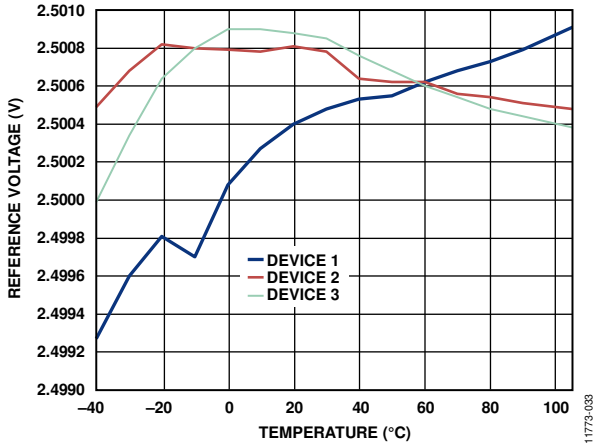


Figure 33. Internal Reference Voltage vs. Temperature

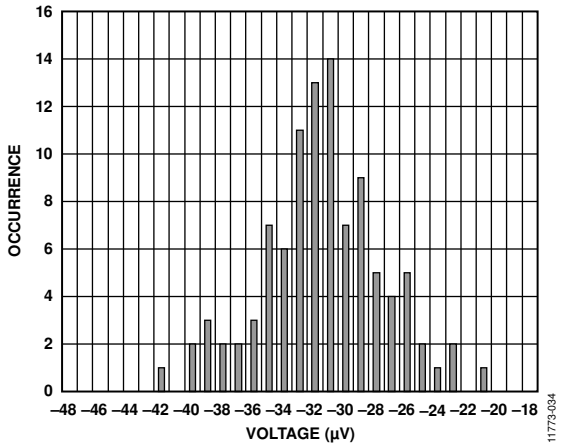


Figure 34. Offset Error Distribution Histogram (Internal Short)

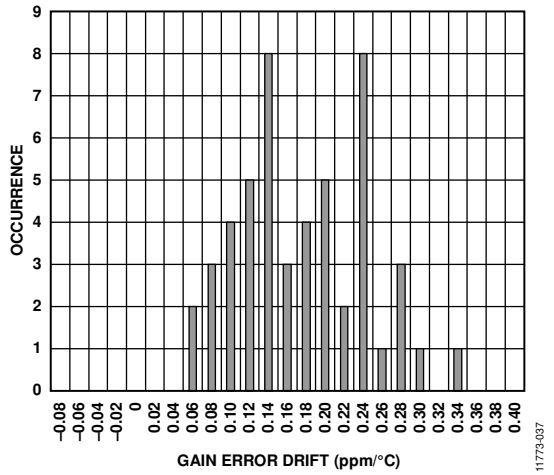


Figure 37. Gain Error Drift Distribution Histogram

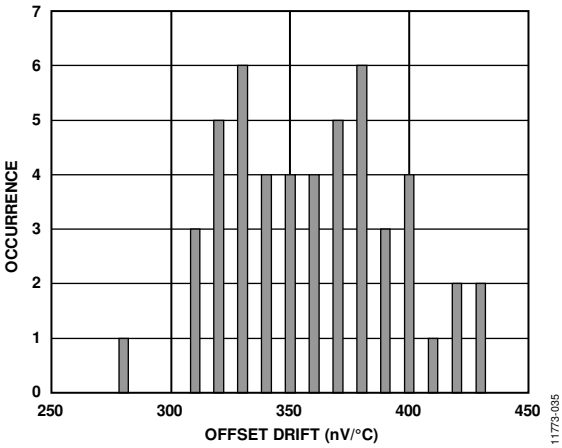


Figure 35. Offset Error Drift Distribution Histogram (Internal Short)

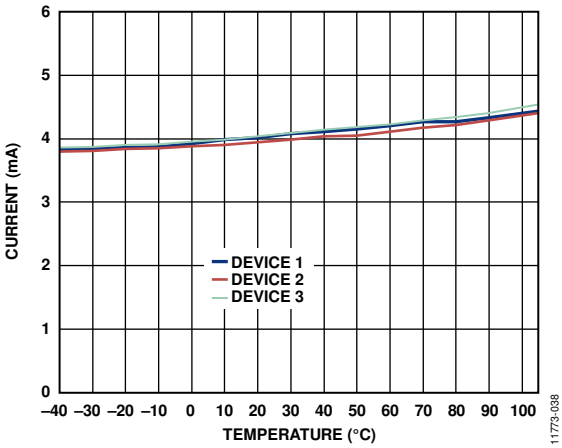


Figure 38. Current Consumption vs. Temperature (Continuous Conversion Mode, Buffers Enabled, Internal Reference, Internal Clock)

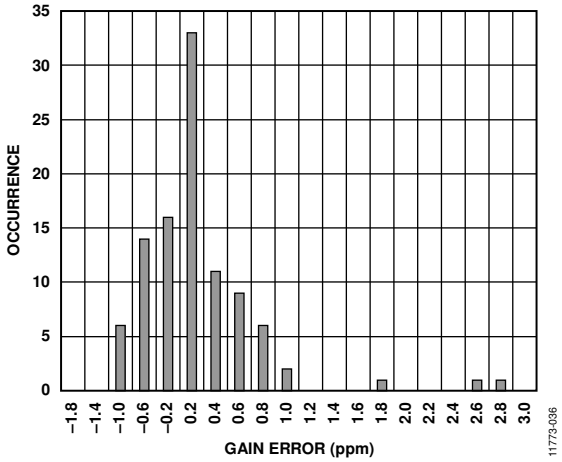


Figure 36. Gain Error Distribution Histogram

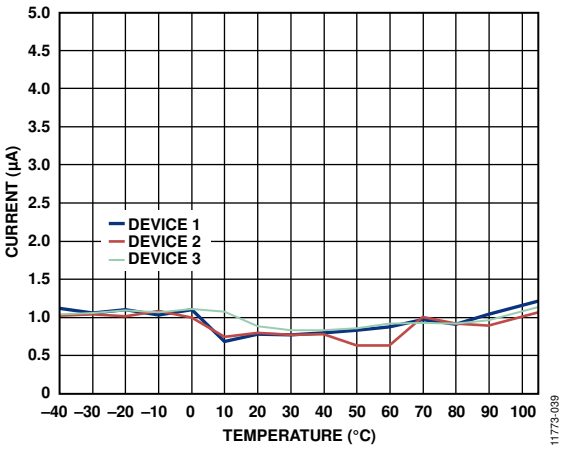


Figure 39. Current Consumption vs. Temperature (Power-Down Mode)

NOISE PERFORMANCE AND RESOLUTION

Table 6 shows the rms noise, peak-to-peak noise, effective resolution, and the noise free (peak-to-peak) resolution of the AD7173-8 for various output data rates and filters. The values listed are for the bipolar input range with an external 5 V reference.

These values are typical and are generated with a differential input voltage of 0 V when the ADC is continuously converting on a single channel. It is important to note that the peak-to-peak resolution is calculated based on the peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no code flicker. Using the sinc3 filter at the fastest rate results in the noise being quantization limited. This limitation degrades the noise specification at this rate and does not give a result of 24 bits, no missing codes.

Table 6. RMS Noise and Peak-to-Peak Resolution vs. Output Data Rate using Sinc5 + Sinc1 Filter (Default)[1]

	Sinc5 + Sinc1 Filter (Default)			
Output Data Rate (SPS)	**RMS Noise (µV rms)**	**Effective Resolution (Bits)**	**Peak-to-Peak Noise (µV rms)**	**Peak-to-Peak Resolution (Bits)**
31,250	8.0	20.2	67	17.5
5208	4.5	21.1	30	18.3
1007	2.2	22.2	15	19.3
381	1.3	22.9	8.9	20.1
100.5	0.71	23.8	5.1	21
20.01	0.32	24	1.7	22.2
5	0.15	24	0.75	23.4
1.25	0.07	24	0.32	24

[1] Selected rates only; 1000 samples.

Table 7. RMS Noise and Peak-to-Peak Resolution vs. Output Data Rate using Sinc3 Filter[1]

	Sinc3 Filter			
Output Data Rate (SPS)	**RMS Noise (µV rms)**	**Effective Resolution (Bits)**	**Peak-to-Peak Noise (µV rms)**	**Peak-to-Peak Resolution (Bits)**
31,250	210	15.5	1665	12.8
5208	3.6	21.4	28	18.7
1008	1.5	22.7	12	19.9
400.6	1	23.3	6.6	20.5
100.5	0.55	24	3.5	21.4
20.01	0.25	24	1.2	22.4
5	0.11	24	0.56	23.4
1.25	0.07	24	0.27	24

[1] Selected rates only; 1000 samples.

GETTING STARTED

The AD7173-8 offers the user a fast settling, high resolution, multiplexed ADC with high levels of configurability.

- Eight fully differential or 16 single-ended analog inputs.
- Cross point mux. Selects any analog input combination as a pairing to be converted. The signals are routed to the input buffers and onto the modulator positive or negative input.
- ADC input. Selectable as a fully differential input or as a single-ended input.
- Per setup configurability. Up to eight different setups can be defined. A separate setup can be mapped to each of the channels. Each setup allows the user to configure the following:
  - Output data rate when using sinc5 + sinc1 filter
  - Digital filter mode
  - Offset/gain error correction
  - Reference source selection (internal/external)
  - Analog and reference input buffer enables
  - Digital output coding

The AD7173-8 includes a precision 2.5 V low drift (3.5 ppm/°C) band gap internal reference. This reference can be selected to be used for the ADC conversions, reducing the external component count. When enabled, the internal reference is output to the REFOUT pin and can be used as a low noise biasing voltage for the external circuitry. An example of this is using the REFOUT signal to set the input common mode for an external single-ended to differential amplifier.

The AD7173-8 includes two separate linear regulator blocks for both the analog and digital circuitry. The analog LDO regulates the AVDD2 supply to 1.8 V, supplying the ADC core. The user can tie the AVDD1 and AVDD2 supplies together for easiest connection. If a clean analog supply rail is in the system in the range of 2 V to 5.5 V (minimum to maximum), the user can also choose to connect this supply rail to the AVDD2 input, allowing for lower power dissipation.

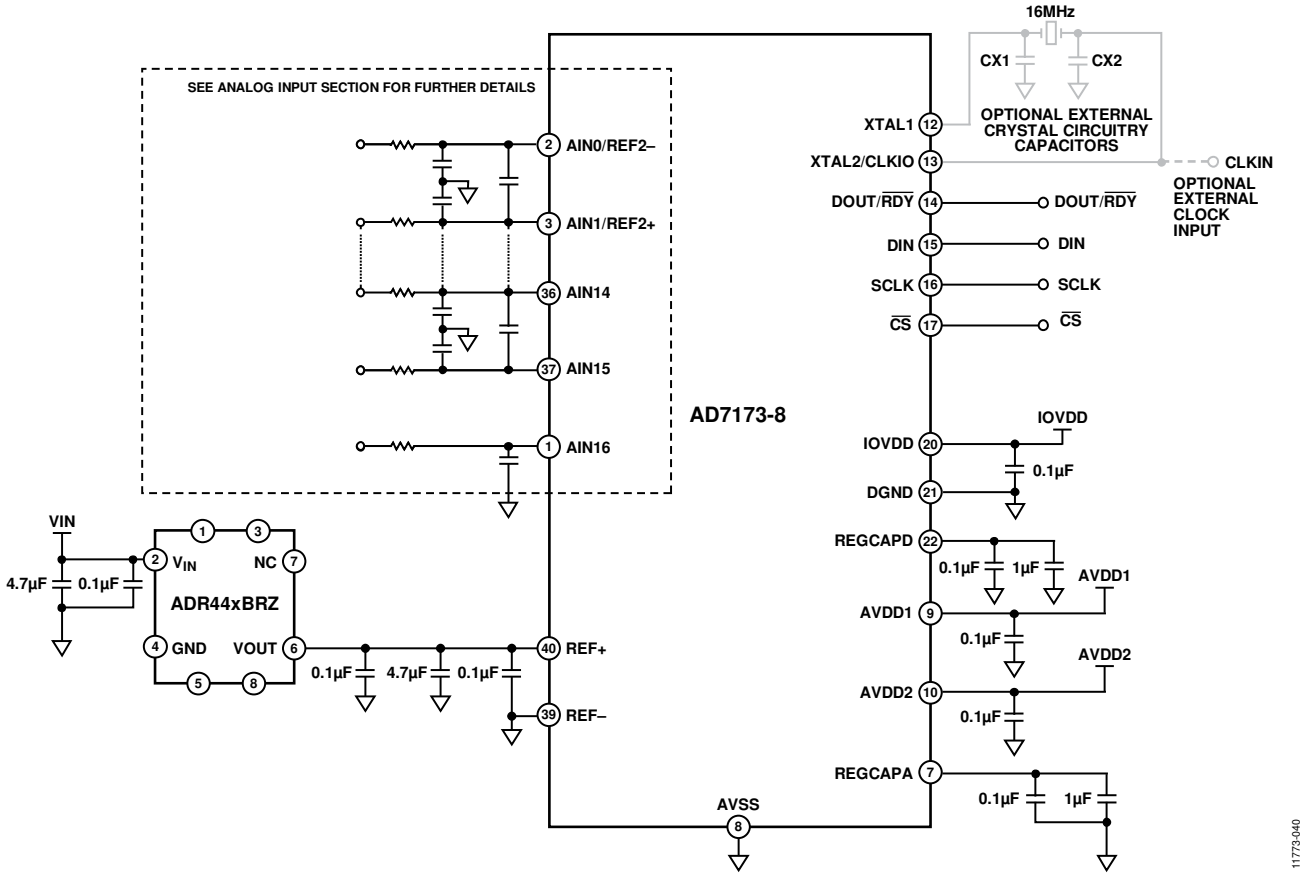


Figure 40. Typical Connection Diagram

The linear regulator for the digital IOVDD supply performs a similar function, regulating the input voltage applied at the IOVDD pin to 1.8 V for the internal digital filtering. The serial interface signals always operate from the IOVDD supply seen at the pin. This means that if 3.3 V is applied to the IOVDD pin, the interface logic inputs and outputs operate at this level.

The AD7173-8 can be used across a wide variety of applications, providing high resolution and accuracy. A sample of these scenarios follows:

- Fast scanning of analog input channels using the internal mux
- Fast scanning of analog input channels using an external mux
- High resolution at lower speeds in either multichannel or ADC per channel applications
- Single ADC per channel; the fast low latency output allows further application specific filtering in an external micro-controller, DSP, or FPGA

POWER SUPPLIES

The AD7173-8 can run from either a 3.3 V or 5 V supply voltage.

The device has three independent power supply pins: AVDD1, AVDD2, and IOVDD.

- AVDD1 and AVDD2 are referred to AVSS.
- AVDD2 powers the internal regulator supplying the ADC.
- AVDD1 and AVDD2 can be tied together for convenience.
- IOVDD is referred to DGND. The supply sets the interface logic levels on the SPI interface and powers an internal regulator for operation of the digital processing.

Single Supply Operation (AVSS = DGND)

When the AD7173-8 is powered from a single supply that is connected to AVDD1, the supply can be either 3.3 V or 5 V. In this configuration, AVSS and DGND can be shorted together on one single ground plane. With this setup, an external level shifting circuit is required to use fully differential inputs to shift the common-mode voltage.

AVDD2 is the input to the internal voltage regulator. Connect AVDD2 to AVDD1 for convenience. Otherwise, if a separate supply is available in the system, a voltage from 2 V to 5.5 V can be applied. IOVDD can range from 2 V to 5.5 V in this unipolar input configuration.

Split Supply Operation (AVSS ≠ DGND)

The AD7173-8 device has the ability to operate with AVSS set to a negative voltage, allowing true bipolar inputs to be applied. This allows for a fully differential input signal centered around 0 V and eliminates the need for an external level shifting circuit. For example, with a 5 V split supply, AVDD1 = 2.5 V and AVSS = −2.5 V. In this use case, the AD7173-8 internally level shifts the signals, allowing the digital output to function between DGND (nominally 0 V) and IOVDD.

When using a split supply for AVDD1 and AVSS, the absolute maximum ratings must be considered (refer to the Absolute Maximum Ratings section). Ensure that IOVDD is set below 3.6 V to stay within the absolute maximum rating for the device.

DIGITAL COMMUNICATION

The AD7173-8 has a 3-wire or 4-wire SPI interface that is compatible with QSPI™, MICROWIRE®, and DSPs. The interface operates in SPI Mode 3 and can be operated with $\overline{CS}$ tied low. In SPI Mode 3, SCLK idles high, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge. This means that data is clocked out on the falling/drive edge and data is clocked in on the rising/sample edge.

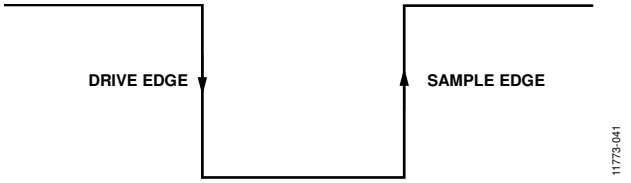


Figure 41. SPI Mode 3 SCLK Edges

Accessing the ADC Register Map

The communications register controls access to the full register map of the ADC. This register is an 8-bit write only register. On power-up or after a reset, the digital interface defaults to a state where it is expecting a write to the communications register; therefore, all communication begins by writing to the communications register.

The data written to the communications register determines which register is being accessed and if the next operation is a read or write. The register address bits (RA[5:0]) determine the specific register to which the read or write operation applies.

When the read or write operation to the selected register is complete, the interface returns to its default state, where it expects a write operation to the communications register.

In situations where interface synchronization is lost, a write operation of at least 64 serial clock cycles with DIN high returns the ADC to its default state by resetting the entire part, including the register contents. Alternatively, if $\overline{CS}$ is being used with the digital interface, returning $\overline{CS}$ high resets the digital interface to its default state and aborts any current operation.

Figure 42 and Figure 43 illustrate writing to and reading from a register by first writing the 8-bit command to the communications register followed by the data for the addressed register.

Reading the ID register is the recommended method for verifying correct communication with the part. The ID register is a read only register and contains the value 0x30DX for the AD7173-8. The communication register and ID register details are described in Table 8 and Table 9.

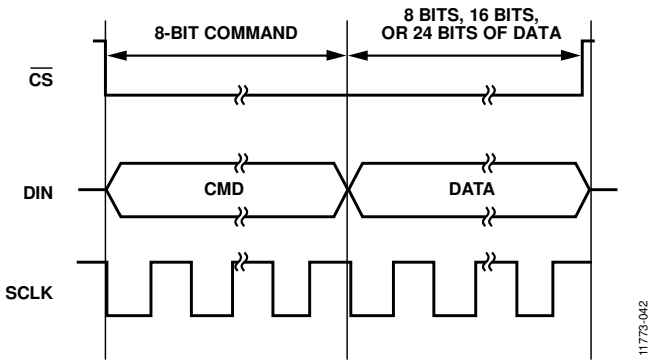


Figure 42. Writing to a Register
(8-Bit Command with Register Address Followed by Data of 8, 16, or 24 Bits; Data Length Is Dependent on the Register Selected)

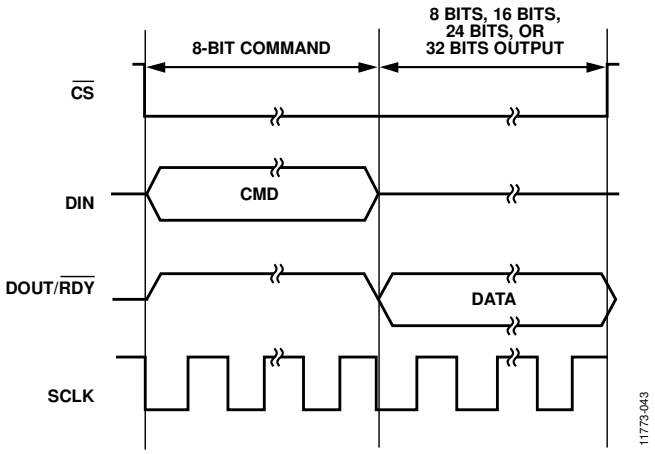


Figure 43. Reading from a Register
(8-Bit Command with Register Address Followed by Data of 8, 16, or 24 Bits; Data Length on DOUT Is Dependent on the Register Selected)

Table 8. Communications Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	COMMS	[7:0]	$\overline{WEN}$	R/$\overline{W}$	RA						0x00	W

Table 9. ID Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x07	ID	[15:8]	ID[15:8]								0x30DX[1]	R
		[7:0]	ID[7:0]									

[1] X = don't care.

CONFIGURATION OVERVIEW

After power on-or reset, the AD7173-8 default configuration is as follows:

- Channel configuration. CH0 is enabled, AIN0 is selected as the positive input, and AIN1 is selected as the negative input. Setup 0 is selected.
- Setup configuration. The input buffers are disabled, and the external reference is selected.
- ADC mode. Continuous conversion mode, the internal oscillator, and single cycle settling are enabled.
- Interface mode. CRC is disabled, and data + status output is disabled.

Note that only a few of the register setting options are shown; this list is just an example. For full register information, see the Register Details section.

Figure 44 shows an overview of the suggested flow for changing the ADC configuration, divided into the following three blocks:

- Channel configuration (see Box A in Figure 44)
- Setup configuration (see Box B in Figure 44)
- ADC mode and interface mode configuration (see Box C in Figure 44)

Channel Configuration

The AD7173-8 has 16 independent channels and eight independent setups. The user can select any of the analog input pairs on any channel, as well as any of the eight setups for any channel, giving the user full flexibility in the channel configuration. This also allows per channel configuration when using eight differential inputs because each channel can have its own dedicated setup.

Channel Registers

The channel registers are used to select which of the 17 analog input pins (AIN0 to AIN16) are used as either the positive analog input or the negative analog input for that channel. This register also contains a channel enable/disable bit and the setup selection bits, which are used to pick which of the eight available setups are used for this channel.

When the AD7173-8 is operating with more than one channel enabled, the channel sequencer cycles through the enabled channels in sequential order, from Channel 0 to Channel 15. If a channel is disabled, it is skipped by the sequencer. Details of the channel register for Channel 0 are shown in Table 10.

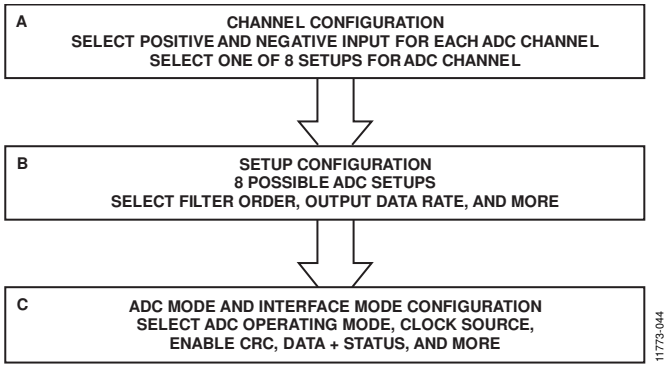


Figure 44. Suggested ADC Configuration Flow

Table 10. Channel 0 Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x10	CH0	[15:8]	CH_EN0	SETUP_SEL[2:0]			RESERVED		AINPOS0[4:3]		0x8001	RW
		[7:0]	AINPOS0[2:0]			AINNEG0						

ADC Setups

The AD7173-8 has eight independent setups. Each setup consists of the following four registers:

- Setup configuration register
- Filter configuration register
- Offset register
- Gain register

For example, Setup 0 consists of Setup Configuration Register 0, Filter Configuration Register 0, Offset Register 0, and Gain Register 0. Figure 45 shows the grouping of these registers The setup is selectable from the channel registers detailed in the Channel Configuration section. This allows each channel to be assigned to one of 8 separate setups. Table 11 through Table 14 show the four registers that are associated with Setup 0. This structure is repeated for Setup 1 to Setup 7.

Setup Configuration Registers

The setup configuration registers allow the user to select the output coding of the ADC by selecting between bipolar and unipolar. In bipolar mode, the ADC accepts negative differential input voltages, and the output coding is offset binary. In unipolar mode, the ADC accepts only positive differential voltages, and the coding is straight binary. In either case, the input voltage must be within the AVDD1/AVSS supply voltages. The user can also select the reference source using this register. Four options are available: an internal 2.5 V reference, an external reference connected between the REF+ and REF− pins, an external reference connected between AIN0/REF2− and AIN1/REF2+, or AVDD1 − AVSS. The analog input buffers and reference input buffers for the setup can also be enabled using this register.

Filter Configuration Registers

The filter configuration register selects which digital filter is used at the output of the ADC modulator. The order of the filter and the output data rate is selected by setting the bits in this register. For more information, see the Digital Filters section.

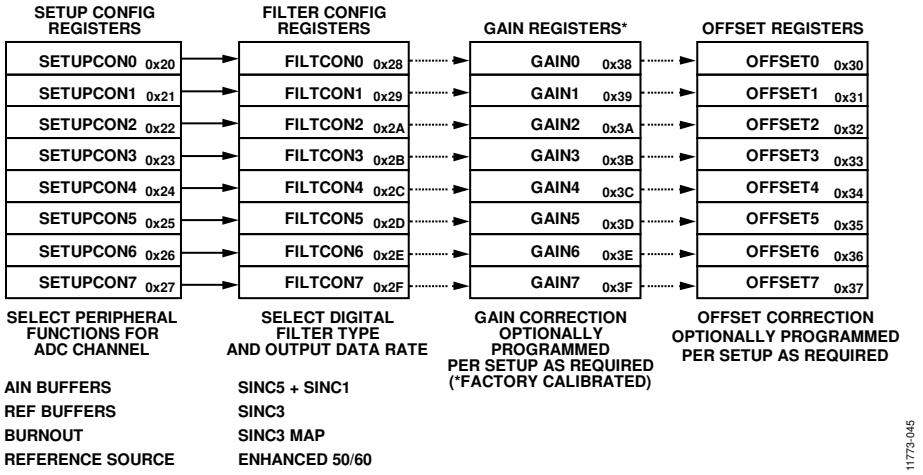


Figure 45. ADC Setup Register Grouping

Table 11. Setup Configuration 0 Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x20	SETUPCON0	[15:8]	RESERVED			BI_UNIPOLAR0	REF_BUF 0[1:0]		AIN_BUF 0[1:0]		0x1000	RW
		[7:0]	BURNOUT_EN0	BUFCHOPMAX0	REF_SEL0		RESERVED					

Table 12. Filter Configuration 0 Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x28	FILTCON0		SINC3_MAP0	RESERVED			ENHFILTEN0	ENHFILT0			0x0000	RW
				ORDER0		ODR0						

Table 13. Offset Configuration 0 Register Bit Map

Reg	Name	Bits	Bit[23:0]	Reset	RW
0x30	OFFSET0	[23:0]	OFFSET0[23:0]	0x800000	RW

Table 14. Gain Configuration 0 Register Bit Map

Reg	Name	Bits	Bit[23:0]	Reset	RW
0x38	GAIN0	[23:0]	GAIN0[23:0]	0x5XXXX0	RW

Offset Registers

The offset register holds the offset calibration coefficient for the ADC. The power-on reset value of the offset register is 0x800000. The offset register is a 24-bit read/write register. The power-on reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user or if the offset register is written to by the user.

Gain Registers

The gain register is a 24-bit register that holds the gain calibration coefficient for the ADC. The gain registers are read/write registers. These registers are configured at power-on with factory calibrated coefficients. Therefore, every device has different default coefficients. The default value is automatically overwritten if a system full-scale calibration is initiated by the user or if the gain register is written to by the user. For more information on calibration, see the Operating Modes section.

ADC Mode and Interface Mode Configuration

The ADC mode register and the interface mode register configure the core peripherals for use by the AD7173-8 and the mode for the digital interface.

ADC Mode Register

The ADC mode register is used primarily to set the conversion mode of the ADC to either continuous or single conversion. The user can also select the standby and power-down modes, as well as any of the calibration modes. In addition, this register contains the clock source select bits and the internal reference enable bits. The reference select bits are contained in the setup configuration registers (see the ADC Setups section for more information).

Interface Mode Register

The interface mode register configures the digital interface operation. This register allows the user to control data-word length, CRC enable, data + status read and continuous read mode.

The details of both registers are shown in Table 15 and Table 16. For more information, see the Digital Interface section.

Table 15. ADC Mode Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x01	ADCMODE	[15:8]	REF_EN	RESERVED	SING_CYC	RESERVED		DELAY			0x2000	RW
		[7:0]	RESERVED	MODE			CLOCKSEL		RESERVED			

Table 16. Interface Mode Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x02	IFMODE	[15:8]	RESERVED			ALT_SYNC	IOSTRENGTH	$\overline{\text{HIDE\_DELAY}}$	RESERVED	DOUT_RESET	0x0000	RW
		[7:0]	CONTREAD	DATA_STAT	REG_CHECK	RESERVED	CRC_EN		RESERVED	WL16		