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# 24-Bit, 250 kSPS, Sigma-Delta ADC with 20 µs Settling and True Rail-to-Rail Buffers

Data Sheet **AD7175-2**

## FEATURES

- Fast and flexible output rate: 5 SPS to 250 kSPS
- Channel scan data rate of 50 kSPS/channel (20 µs settling)
- Performance specifications
  - 17.2 noise free bits at 250 kSPS
  - 20 noise free bits at 2.5 kSPS
  - 24 noise free bits at 20 SPS
  - INL: ±1 ppm of FSR
- 85 dB rejection of 50 Hz and 60 Hz with 50 ms settling
- User configurable input channels
  - 2 fully differential channels or 4 single-ended channels
  - Crosspoint multiplexer
- On-chip 2.5 V reference (±2 ppm/°C drift)
- True rail-to-rail analog and reference input buffers
- Internal or external clock
- Power supply: AVDD1 = 5 V, AVDD2 = IOVDD = 2 V to 5 V
  - Split supply with AVDD1/AVSS at ±2.5 V
- ADC current: 8.4 mA
- Temperature range: −40°C to +105°C
- 3- or 4-wire serial digital interface (Schmitt trigger on SCLK)
  - Serial port interface (SPI), QSPI, MICROWIRE, and DSP compatible

## APPLICATIONS

- Process control: PLC/DCS modules
- Temperature and pressure measurement
- Medical and scientific multichannel instrumentation
- Chromatography

## GENERAL DESCRIPTION

The AD7175-2 is a low noise, fast settling, multiplexed, 2-/4-channel (fully/pseudo differential) Σ-Δ analog-to-digital converter (ADC) for low bandwidth inputs. It has a maximum channel scan rate of 50 kSPS (20 µs) for fully settled data. The output data rates range from 5 SPS to 250 kSPS.

The AD7175-2 integrates key analog and digital signal conditioning blocks to allow users to configure an individual setup for each analog input channel in use. Each feature can be user selected on a per channel basis. Integrated true rail-to-rail buffers on the analog inputs and external reference inputs provide easy to drive high impedance inputs. The precision 2.5 V low drift (2 ppm/°C) band gap internal reference (with output reference buffer) adds embedded functionality to reduce external component count.

The digital filter allows simultaneous 50 Hz/60 Hz rejection at 27.27 SPS output data rate. The user can switch between different filter options according to the demands of each channel in the application. The ADC automatically switches through each selected channel. Further digital processing functions include offset and gain calibration registers, configurable on a per channel basis.

The device operates with a 5 V AVDD1, or ±2.5 V AVDD1/AVSS, and 2 V to 5 V AVDD2 and IOVDD supplies. The specified operating temperature range is −40°C to +105°C. The AD7175-2 is in a 24-lead TSSOP package.

Note that, throughout this data sheet, the dual function pin names are referenced by the relevant function only.

## FUNCTIONAL BLOCK DIAGRAM

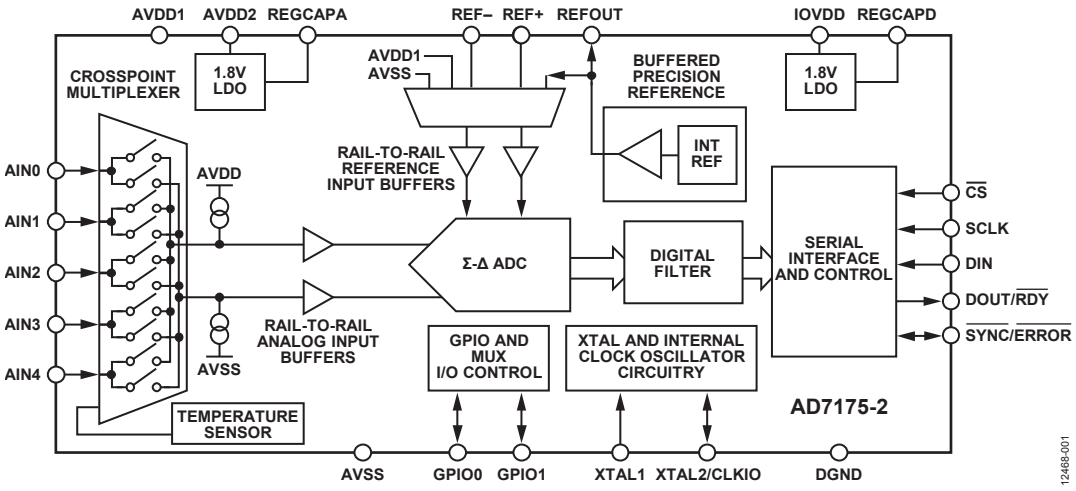


*Figure 1.*

**Rev. B** Document Feedback



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# AD7175-2* PRODUCT PAGE QUICK LINKS

**Last Content Update: 02/23/2017**

## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- AD7175-2 Evaluation Board

## DOCUMENTATION

**Data Sheet**

- AD7175-2: 24-Bit, 250 kSPS, Sigma-Delta ADC with 20 µs Settling and True Rail-to-Rail Buffers Data Sheet

**Technical Books**

- The Data Conversion Handbook, 2005

**User Guides**

- UG-741: Evaluating the AD7175-2 24-Bit, 250 kSPS, Sigma-Delta ADC with 20 µs Settling and Integrated Analog Input Buffer

## SOFTWARE AND SYSTEMS REQUIREMENTS

- AD7175 Microcontroller Renesas Driver
- AD7176-2 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design
- AD717x Microcontroller No-OS
- AD717x Eval+ Software

## TOOLS AND SIMULATIONS

- AD7175-2 Digital Filter Frequency Response Model
- AD7175-2 IBIS Model

## REFERENCE DESIGNS

- CN0292
- CN0363
- CN0364

## REFERENCE MATERIALS

**Press**

- Analog Devices Introduces Industry's First 24-Bit Sigma Delta A/D Converter with Rail-to-Rail Analog and Reference Input Buffers On-chip

**Technical Articles**

- Fundamental Principles Behind the Sigma-Delta ADC Topology: Part 1
- Fundamental Principles Behind the Sigma-Delta ADC Topology: Part 2

**Tutorials**

- MT-022: ADC Architectures III: Sigma-Delta ADC Basics
- MT-023: ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications

## DESIGN RESOURCES

- AD7175-2 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all AD7175-2 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

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**5/2016—Rev. A to Rev. B**

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**9/2014—Rev. 0 to Rev. A**

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**7/2014—Revision 0: Initial Version**

# SPECIFICATIONS

AVDD1 = 4.5 V to 5.5 V, AVDD2 = 2 V to 5.5 V, IOVDD = 2 V to 5.5 V, AVSS = DGND = 0 V, REF+ = 2.5 V, REF− = AVSS, MCLK = internal master clock = 16 MHz, $T_A = T_{MIN}$ to $T_{MAX}$ (−40°C to +105°C), unless otherwise noted.

**Table 1.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ADC SPEED AND PERFORMANCE | | | | | |
| Output Data Rate (ODR) | | 5 | | 250,000 | SPS |
| No Missing Codes[1] | Excluding sinc3 filter ≥ 125 kSPS | 24 | | | Bits |
| Resolution | See Table 6 and Table 7 | | | | |
| Noise | See Table 6 and Table 7 | | | | |
| ACCURACY | | | | | |
| Integral Nonlinearity (INL) | Analog input buffers enabled | | ±3.5 | ±7.8 | ppm of FSR |
| | Analog input buffers disabled | | ±1 | ±3.5 | ppm of FSR |
| Offset Error[2] | Internal short | | ±40 | | µV |
| Offset Drift | Internal short | | ±80 | | nV/°C |
| Gain Error[2] | | | ±35 | ±85 | ppm of FSR |
| Gain Drift | | | ±0.4 | ±0.75 | ppm/°C |
| REJECTION | | | | | |
| Power Supply Rejection | AVDD1, AVDD2, $V_{IN}$ = 1 V | | 95 | | dB |
| Common-Mode Rejection | $V_{IN}$ = 0.1 V | | | | |
| At DC | | 95 | | | dB |
| At 50 Hz, 60 Hz[1] | 20 Hz output data rate (post filter), 50 Hz ± 1 Hz and 60 Hz ± 1 Hz | 120 | | | dB |
| Normal Mode Rejection[1] | 50 Hz ± 1 Hz and 60 Hz ± 1 Hz | | | | |
| | Internal clock, 20 SPS ODR (postfilter) | 71 | 90 | | dB |
| | External clock, 20 SPS ODR (postfilter) | 85 | 90 | | dB |
| ANALOG INPUTS | | | | | |
| Differential Input Range | $V_{REF}$ = (REF+) − (REF−) | | ±$V_{REF}$ | | V |
| Absolute Voltage Limits[1] | | | | | |
| Input Buffers Disabled | | AVSS − 0.05 | | AVDD1 + 0.05 | V |
| Input Buffers Enabled | | AVSS | | AVDD1 | V |
| Analog Input Current | | | | | |
| Input Buffers Disabled | | | | | |
| Input Current | | | ±48 | | µA/V |
| Input Current Drift | External clock | | ±0.75 | | nA/V/°C |
| | Internal clock (±2.5% clock) | | ±4 | | nA/V/°C |
| Input Buffers Enabled | | | | | |
| Input Current | | | ±30 | | nA |
| Input Current Drift | AVDD1 − 0.2 V to AVSS + 0.2 V | | ±75 | | pA/°C |
| | AVDD1 to AVSS | | ±1 | | nA/°C |
| Crosstalk | 1 kHz input | | −120 | | dB |
| INTERNAL REFERENCE | 100 nF external capacitor to AVSS | | | | |
| Output Voltage | REFOUT, with respect to AVSS | | 2.5 | | V |
| Initial Accuracy[3] | REFOUT, $T_A$ = 25°C | −0.12 | | +0.12 | % of V |
| Temperature Coefficient | | | | | |
| 0°C to 105°C[1] | | | ±2 | ±5 | ppm/°C |
| −40°C to +105°C[1] | | | ±3 | ±10 | ppm/°C |
| Reference Load Current, $I_{LOAD}$ | | −10 | | +10 | mA |
| Power Supply Rejection | AVDD1, AVDD2, (line regulation) | | 90 | | dB |
| Load Regulation | $\Delta V_{OUT}/\Delta I_{LOAD}$ | | 32 | | ppm/mA |
| Voltage Noise | $e_N$, 0.1 Hz to 10 Hz, 2.5 V reference | | 4.5 | | µV rms |
| Voltage Noise Density | $e_N$, 1 kHz, 2.5 V reference | | 215 | | nV/√Hz |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Turn-On Settling Time | 100 nF REFOUT capacitor | | 200 | | µs |
| Short-Circuit Current, $I_{SC}$ | | | 25 | | mA |
| EXTERNAL REFERENCE INPUTS | | | | | |
| Differential Input Range | $V_{REF}$ = (REF+) − (REF−) | 1 | 2.5 | AVDD1 | V |
| Absolute Voltage Limits[1] | | | | | |
| Input Buffers Disabled | | AVSS − 0.05 | | AVDD1 + 0.05 | V |
| Input Buffers Enabled | | AVSS | | AVDD1 | V |
| REFIN Input Current | | | | | |
| Input Buffers Disabled | | | | | |
| Input Current | | | ±72 | | µA/V |
| Input Current Drift | External clock | | ±1.2 | | nA/V/°C |
| | Internal clock | | ±6 | | nA/V/°C |
| Input Buffers Enabled | | | | | |
| Input Current | | | ±800 | | nA |
| Input Current Drift | | | 1.25 | | nA/°C |
| Normal Mode Rejection[1] | See the Rejection parameter | | | | |
| Common-Mode Rejection | | | 95 | | dB |
| TEMPERATURE SENSOR | | | | | |
| Accuracy | After user calibration at 25°C | | ±2 | | °C |
| Sensitivity | | | 470 | | µV/K |
| BURNOUT CURRENTS | | | | | |
| Source/Sink Current | Analog input buffers must be enabled | | ±10 | | µA |
| GENERAL-PURPOSE INPUT/ OUTPUT (GPIO0, GPIO1) | With respect to AVSS | | | | |
| Input Mode Leakage Current[1] | | −10 | | +10 | µA |
| Floating State Output Capacitance | | | 5 | | pF |
| Output High Voltage, $V_{OH}$[1] | $I_{SOURCE}$ = 200 µA | AVSS + 4 | | | V |
| Output Low Voltage, $V_{OL}$[1] | $I_{SINK}$ = 800 µA | | | AVSS + 0.4 | V |
| Input High Voltage, $V_{IH}$[1] | | AVSS + 3 | | | V |
| Input Low Voltage, $V_{IL}$[1] | | | | AVSS + 0.7 | V |
| CLOCK | | | | | |
| Internal Clock | | | | | |
| Frequency | | | 16 | | MHz |
| Accuracy | | −2.5% | | +2.5% | % |
| Duty Cycle | | | 50 | | % |
| Output Low Voltage, $V_{OL}$ | | | | 0.4 | V |
| Output High Voltage, $V_{OH}$ | | 0.8 × IOVDD | | | V |
| Crystal | | | | | |
| Frequency | | 14 | 16 | 16.384 | MHz |
| Startup Time | | | 10 | | µs |
| External Clock (CLKIO) | | | 16 | 16.384 | MHz |
| Duty Cycle[1] | | 30 | 50 | 70 | % |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LOGIC INPUTS | | | | | |
| Input High Voltage, $V_{INH}$[1] | 2 V ≤ IOVDD < 2.3 V | 0.65 × IOVDD | | | V |
| | 2.3 V ≤ IOVDD ≤ 5.5 V | 0.7 × IOVDD | | | V |
| Input Low Voltage, $V_{INL}$[1] | 2 V ≤ IOVDD < 2.3 V | | | 0.35 × IOVDD | V |
| | 2.3 V ≤ IOVDD ≤ 5.5 V | | | 0.7 | V |
| Hysteresis[1] | IOVDD ≥ 2.7 V | 0.08 | | 0.25 | V |
| | IOVDD < 2.7 V | 0.04 | | 0.2 | V |
| Leakage Currents | | −10 | | +10 | µA |
| LOGIC OUTPUT (DOUT/$\overline{RDY}$) | | | | | |
| Output High Voltage, $V_{OH}$[1] | IOVDD ≥ 4.5 V, $I_{SOURCE}$ = 1 mA | 0.8 × IOVDD | | | V |
| | 2.7 V ≤ IOVDD < 4.5 V, $I_{SOURCE}$ = 500 µA | 0.8 × IOVDD | | | V |
| | IOVDD < 2.7 V, $I_{SOURCE}$ = 200 µA | 0.8 × IOVDD | | | V |
| Output Low Voltage, $V_{OL}$[1] | IOVDD ≥ 4.5 V, $I_{SINK}$ = 2 mA | | | 0.4 | V |
| | 2.7 V ≤ IOVDD < 4.5 V, $I_{SINK}$ = 1 mA | | | 0.4 | V |
| | IOVDD < 2.7 V, $I_{SINK}$ = 400 µA | | | 0.4 | V |
| Leakage Current | Floating state | −10 | | +10 | µA |
| Output Capacitance | Floating state | | 10 | | pF |
| SYSTEM CALIBRATION[1] | | | | | |
| Full-Scale (FS) Calibration Limit | | | | 1.05 × FS | V |
| Zero-Scale Calibration Limit | | −1.05 × FS | | | V |
| Input Span | | 0.8 × FS | | 2.1 × FS | V |
| POWER REQUIREMENTS | | | | | |
| Power Supply Voltage | | | | | |
| AVDD1 to AVSS | | 4.5 | | 5.5 | V |
| AVDD2 to AVSS | | 2 | | 5.5 | V |
| AVSS to DGND | | −2.75 | | 0 | V |
| IOVDD to DGND | | 2 | | 5.5 | V |
| IOVDD to AVSS | For AVSS < DGND | | | 6.35 | V |
| POWER SUPPLY CURRENTS[4] | All outputs unloaded, digital inputs connected to IOVDD or DGND | | | | |
| Full Operating Mode | | | | | |
| AVDD1 Current | Analog input and reference input buffers disabled, external reference | | 1.4 | 1.65 | mA |
| | Analog input and reference input buffers disabled, internal reference | | 1.75 | 2 | mA |
| | Analog input and reference input buffers enabled, external reference | | 13 | 16 | mA |
| | Each buffer: AIN+, AIN−, REF+, REF− | | 2.9 | | mA |
| AVDD2 Current | External reference | | 4.5 | 5 | mA |
| | Internal reference | | 4.75 | 5.2 | mA |
| IOVDD Current | External clock | | 2.5 | 2.8 | mA |
| | Internal clock | | 2.75 | 3.1 | mA |
| | External crystal | | 3 | | mA |
| Standby Mode (LDO On) | Internal reference off, total current consumption | | 25 | | µA |
| | Internal reference on, total current consumption | | 425 | | µA |
| Power-Down Mode | Full power-down (including LDO and internal reference) | | 5 | 10 | µA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER DISSIPATION[4] | | | | | |
| Full Operating Mode | All buffers disabled, external clock and reference, AVDD2 = 2 V, IOVDD = 2 V | | 21 | | mW |
| | All buffers disabled, external clock and reference, all supplies = 5 V | | 42 | | mW |
| | All buffers disabled, external clock and reference, all supplies = 5.5 V | | | 52 | mW |
| | All buffers enabled, internal clock and reference, AVDD2 = 2 V, IOVDD = 2 V | | 82 | | mW |
| | All buffers enabled, internal clock and reference, all supplies = 5 V | | 105 | | mW |
| | All buffers enabled, internal clock and reference, all supplies = 5.5 V | | | 136 | mW |
| Standby Mode | Internal reference off, all supplies = 5 V | | 125 | | µW |
| | Internal reference on, all supplies = 5 V | | 2.2 | | mW |
| Power-Down Mode | Full power-down, all supplies = 5 V | | 25 | 50 | µW |

[1] Specification is not production tested but is supported by characterization data at initial product release.
[2] Following a system or internal zero-scale calibration, the offset error is in the order of the noise for the programmed output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed output data rate.
[3] This specification includes moisture sensitivity level (MSL) preconditioning effects.
[4] This specification is with no load on the REFOUT and digital output pins.

## TIMING CHARACTERISTICS

IOVDD = 2 V to 5.5 V, DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = IOVDD, $C_{LOAD}$ = 20 pF, unless otherwise noted.

**Table 2.**

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ | Unit | Test Conditions/Comments[1, 2] |
|---|---|---|---|
| SCLK | | | |
| $t_3$ | 25 | ns min | SCLK high pulse width |
| $t_4$ | 25 | ns min | SCLK low pulse width |
| READ OPERATION | | | |
| $t_1$ | 0 | ns min | $\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time |
| | 15 | ns max | IOVDD = 4.75 V to 5.5 V |
| | 40 | ns max | IOVDD = 2 V to 3.6 V |
| $t_2$[3] | 0 | ns min | SCLK active edge to data valid delay[4] |
| | 12.5 | ns max | IOVDD = 4.75 V to 5.5 V |
| | 25 | ns max | IOVDD = 2 V to 3.6 V |
| $t_5$[5] | 2.5 | ns min | Bus relinquish time after $\overline{CS}$ inactive edge |
| | 20 | ns max | |
| $t_6$ | 0 | ns min | SCLK inactive edge to $\overline{CS}$ inactive edge |
| $t_7$ | 10 | ns min | SCLK inactive edge to DOUT/$\overline{RDY}$ high/low |
| WRITE OPERATION | | | |
| $t_8$ | 0 | ns min | $\overline{CS}$ falling edge to SCLK active edge setup time[4] |
| $t_9$ | 8 | ns min | Data valid to SCLK edge setup time |
| $t_{10}$ | 8 | ns min | Data valid to SCLK edge hold time |
| $t_{11}$ | 5 | ns min | $\overline{CS}$ rising edge to SCLK edge hold time |

[1] Sample tested during initial release to ensure compliance.
[2] See Figure 2 and Figure 3.
[3] This parameter is defined as the time required for the output to cross the $V_{OL}$ or $V_{OH}$ limits.
[4] The SCLK active edge is the falling edge of SCLK.
[5] DOUT/$\overline{RDY}$ returns high after a read of the data register. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while DOUT/$\overline{RDY}$ is high, although care must be taken to ensure that subsequent reads do not occur close to the next output update. If the continuous read feature is enabled, the digital word can be read only once.

## TIMING DIAGRAMS

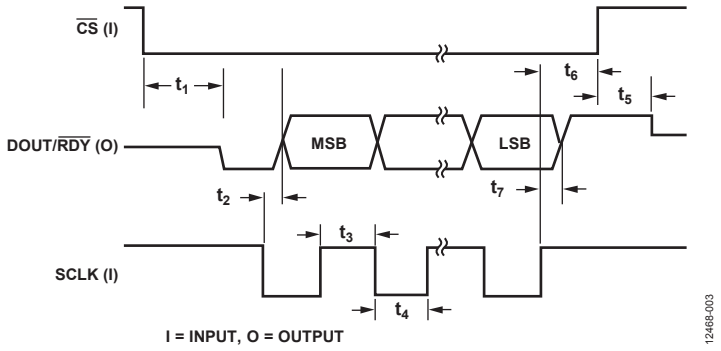


*Figure 2. Read Cycle Timing Diagram*

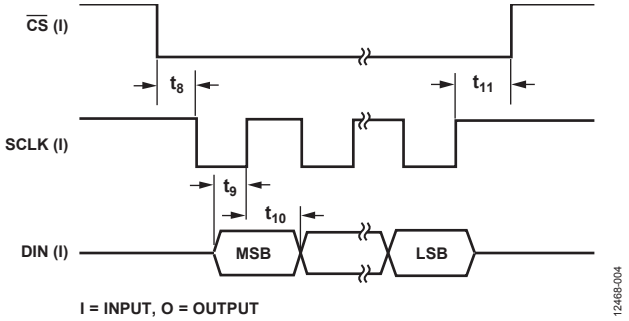


*Figure 3. Write Cycle Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 3.**

| Parameter | Rating |
|---|---|
| AVDD1, AVDD2 to AVSS | −0.3 V to +6.5 V |
| AVDD1 to DGND | −0.3 V to +6.5 V |
| IOVDD to DGND | −0.3 V to +6.5 V |
| IOVDD to AVSS | −0.3 V to +7.5 V |
| AVSS to DGND | −3.25 V to +0.3 V |
| Analog Input Voltage to AVSS | −0.3 V to AVDD1 + 0.3 V |
| Reference Input Voltage to AVSS | −0.3 V to AVDD1 + 0.3 V |
| Digital Input Voltage to DGND | −0.3 V to IOVDD + 0.3 V |
| Digital Output Voltage to DGND | −0.3 V to IOVDD + 0.3 V |
| Analog Input/Digital Input Current | 10 mA |
| Operating Temperature Range | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Maximum Junction Temperature | 150°C |
| Lead Soldering, Reflow Temperature | 260°C |
| ESD Rating (HBM) | 4 kV |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for a device soldered on a JEDEC test board for surface-mount packages.

**Table 4. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| 24-Lead TSSOP | | |
| JEDEC 1-Layer Board | 149 | °C/W |
| JEDEC 2-Layer Board | 81 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

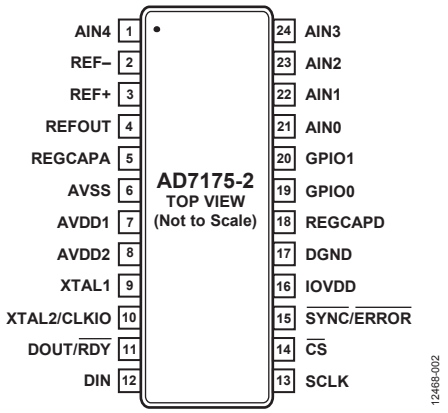


*Figure 4. Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 1 | AIN4 | AI | Analog Input 4. Selectable through crosspoint multiplexer. |
| 2 | REF− | AI | Reference Input Negative Terminal. REF− can span from AVSS to AVDD1 − 1 V. |
| 3 | REF+ | AI | Reference Input Positive Terminal. An external reference can be applied between REF+ and REF−. REF+ can span from AVSS + 1 V to AVDD1.The device functions with a reference magnitude from 1 V to AVDD1. |
| 4 | REFOUT | AO | Buffered Output of Internal Reference. The output is 2.5 V with respect to AVSS. |
| 5 | REGCAPA | AO | Analog LDO Regulator Output. Decouple this pin to AVSS using a 1 µF and a 0.1 µF capacitor. |
| 6 | AVSS | P | Negative Analog Supply. This supply ranges from −2.75 V to 0 V and is nominally set to 0 V. |
| 7 | AVDD1 | P | Analog Supply Voltage 1. This voltage is 5 V ± 10% with respect to AVSS. |
| 8 | AVDD2 | P | Analog Supply Voltage 2. This voltage ranges from 2 V to 5 V with respect to AVSS. |
| 9 | XTAL1 | AI | Input 1 for Crystal. |
| 10 | XTAL2/CLKIO | AI/DI | Input 2 for Crystal/Clock Input or Output. Based on the CLOCKSEL bits in the ADCMODE register. There are four options available for selecting the MCLK source:<br>Internal oscillator: no output.<br>Internal oscillator: output to XTAL2/CLKIO. Operates at IOVDD logic level.<br>External clock: input to XTAL2/CLKIO. Input must be at IOVDD logic level.<br>External crystal: connected between XTAL1 and XTAL2/CLKIO. |
| 11 | DOUT/$\overline{\text{RDY}}$ | DO | Serial Data Output/Data Ready Output. DOUT/$\overline{\text{RDY}}$ is a dual purpose pin. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. The data-word/control word information is placed on the DOUT/$\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. When $\overline{\text{CS}}$ is high, the DOUT/$\overline{\text{RDY}}$ output is three-stated. When $\overline{\text{CS}}$ is low, DOUT/$\overline{\text{RDY}}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available. |
| 12 | DIN | DI | Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers in the ADC, with the register address (RA) bits of the communications register identifying the appropriate register. Data is clocked in on the rising edge of SCLK. |
| 13 | SCLK | DI | Serial Clock Input. This serial clock input is for data transfers to and from the ADC. The SCLK has a Schmitt triggered input, making the interface suitable for opto-isolated applications. |
| 14 | $\overline{\text{CS}}$ | DI | Chip Select Input. This is an active low logic input selects the ADC. $\overline{\text{CS}}$ can select the ADC in systems with more than one device on the serial bus. $\overline{\text{CS}}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device. When $\overline{\text{CS}}$ is high, the DOUT/$\overline{\text{RDY}}$ output is three-stated. |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 15 | $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ | DI/O | Synchronization Input/Error Input/Output. This pin can be switched between a logic input and a logic output in the GPIOCON register. When synchronization input ($\overline{\text{SYNC}}$) is enabled, this pin allows synchronization of the digital filters and analog modulators when using multiple AD7175-2 devices. For more information, see the Synchronization section. When the synchronization input is disabled, this pin can be used in one of three modes:<br>Active low error input mode: this mode sets the ADC_ERROR bit in the status register.<br>Active low, open-drain error output mode: the status register error bits are mapped to the $\overline{\text{ERROR}}$ output. The $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed.<br>General-purpose output mode: the status of the pin is controlled by the ERR_DAT bit in the GPIOCON register. The pin is referenced between IOVDD and DGND, as opposed to the AVDD1 and AVSS levels used by the GPIOx pins. The pin has an active pull-up in this case. |
| 16 | IOVDD | P | Digital Input/Output Supply Voltage. The IOVDD voltage ranges from 2 V to 5 V. IOVDD is independent of AVDD2. For example, IOVDD can be operated at 3 V when AVDD2 equals 5 V, or vice versa. If AVSS is set to −2.5 V, the voltage on IOVDD must not exceed 3.6 V. |
| 17 | DGND | P | Digital Ground. |
| 18 | REGCAPD | AO | Digital LDO Regulator Output. This pin is for decoupling purposes only. Decouple this pin to DGND using a 1 µF and a 0.1 µF capacitor. |
| 19 | GPIO0 | DI/O | General-Purpose Input/Output 0. The pin is referenced between AVDD1 and AVSS levels. |
| 20 | GPIO1 | DI/O | General-Purpose Input/Output 1. The pin is referenced between AVDD1 and AVSS levels. |
| 21 | AIN0 | AI | Analog Input 0. Selectable through the crosspoint multiplexer. |
| 22 | AIN1 | AI | Analog Input 1. Selectable through the crosspoint multiplexer. |
| 23 | AIN2 | AI | Analog Input 2. Selectable through the crosspoint multiplexer. |
| 24 | AIN3 | AI | Analog Input 3. Selectable through the crosspoint multiplexer. |

[1] AI is analog input, AO is analog output, DI/O is bidirectional digital input/output, DO is digital output, DI is digital input, and P is power supply.

# TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 5 V, AVDD2 = 5 V, IOVDD = 3.3 V, $T_A$ = 25°C, unless otherwise noted.

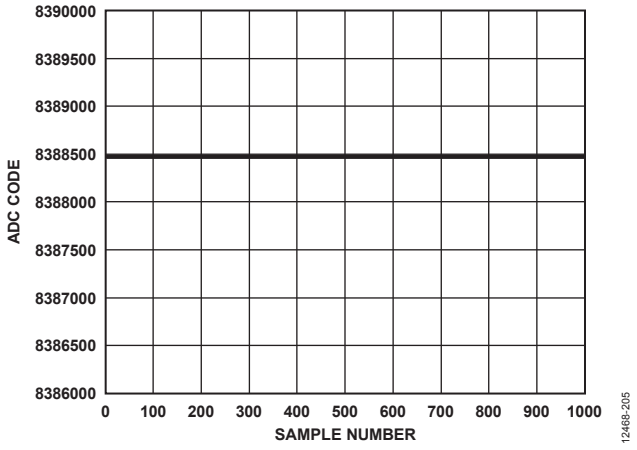


*Figure 5. Noise (Analog Input Buffers Disabled, $V_{REF}$ = 5 V, Output Data Rate = 5 SPS)*

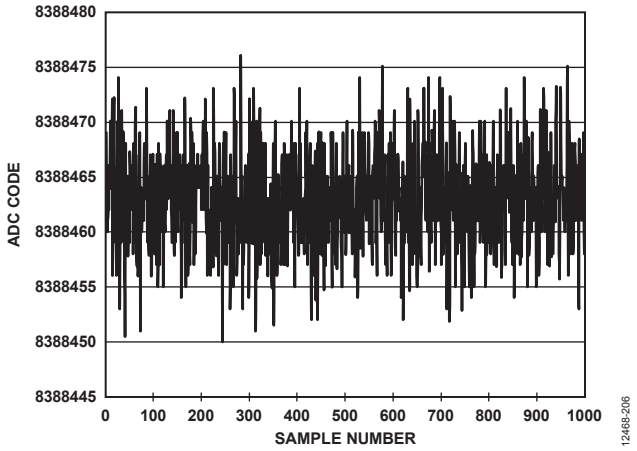


*Figure 6. Noise (Analog Input Buffers Disabled, $V_{REF}$ = 5 V, Output Data Rate = 10 kSPS)*

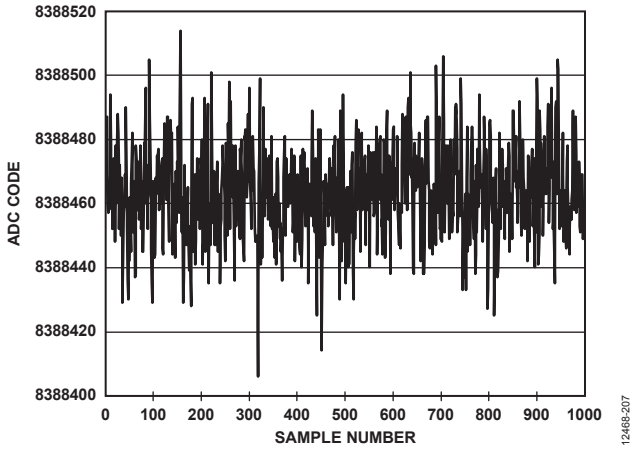


*Figure 7. Noise (Analog Input Buffers Disabled, $V_{REF}$ = 5 V, Output Data Rate = 250 kSPS)*

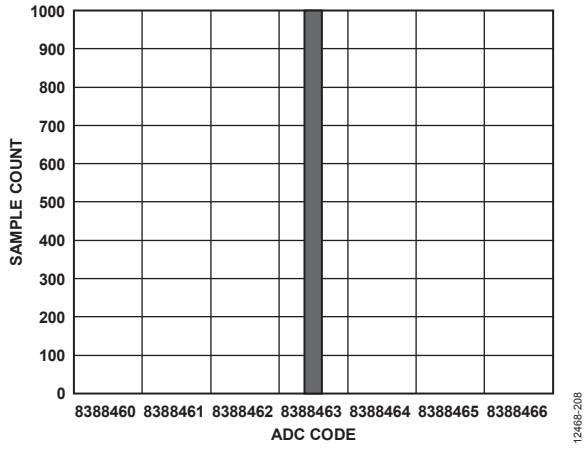


*Figure 8. Histogram (Analog Input Buffers Disabled, $V_{REF}$ = 5 V, Output Data Rate = 5 SPS)*

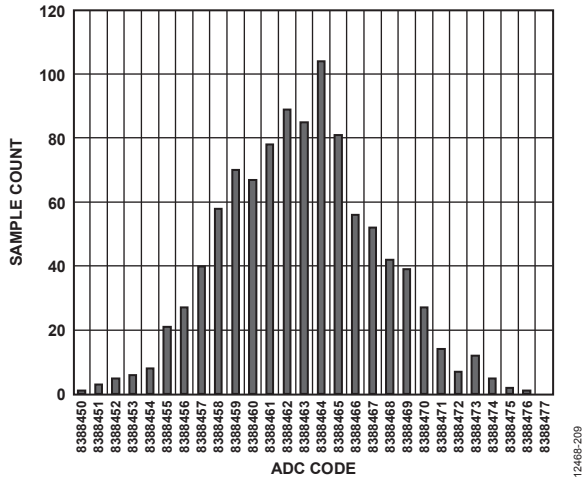


*Figure 9. Histogram (Analog Input Buffers Disabled, $V_{REF}$ = 5 V, Output Data Rate = 10 kSPS)*

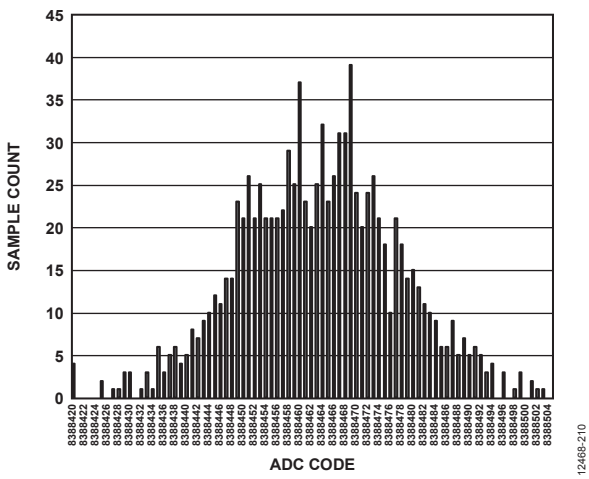


*Figure 10. Histogram (Analog Input Buffers Disabled, $V_{REF}$ = 5 V, Output Data Rate = 250 kSPS)*

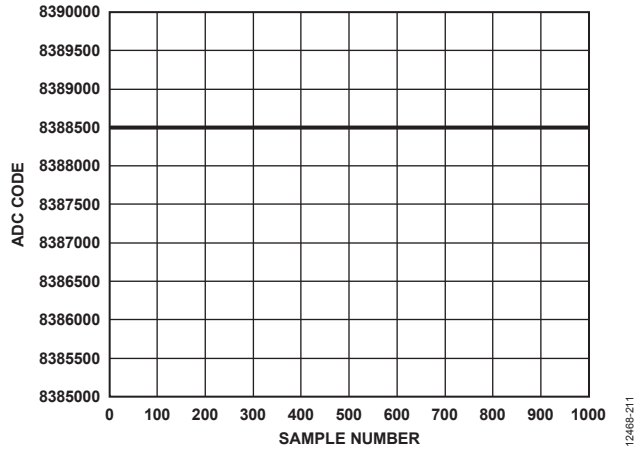


*Figure 11. Noise (Analog Input Buffers Enabled, $V_{REF}$ = 5 V, Output Data Rate = 5 SPS)*

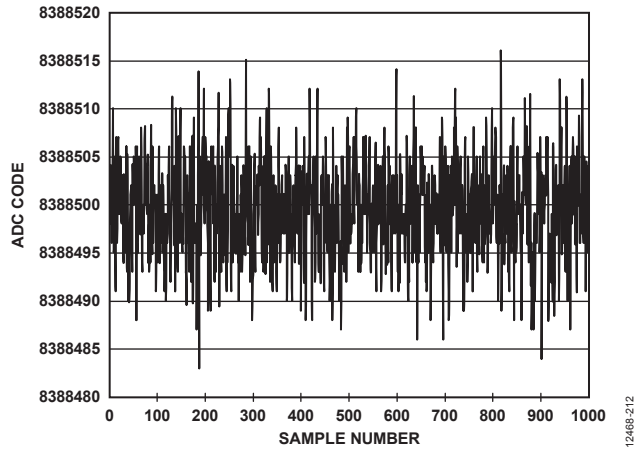


*Figure 12. Noise (Analog Input Buffers Enabled, $V_{REF}$ = 5 V, Output Data Rate = 10 kSPS)*

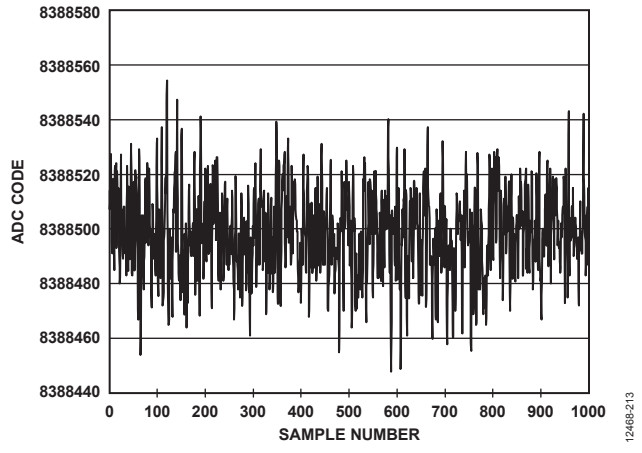


*Figure 13. Noise (Analog Input Buffers Enabled, $V_{REF}$ = 5 V, Output Data Rate = 250 kSPS)*

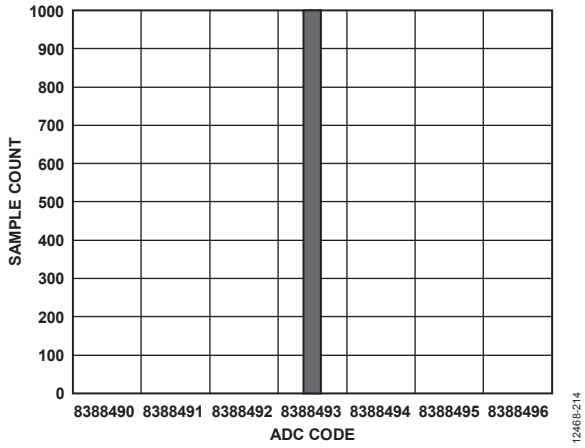


*Figure 14. Histogram (Analog Input Buffers Enabled, $V_{REF}$ = 5 V, Output Data Rate = 5 SPS)*

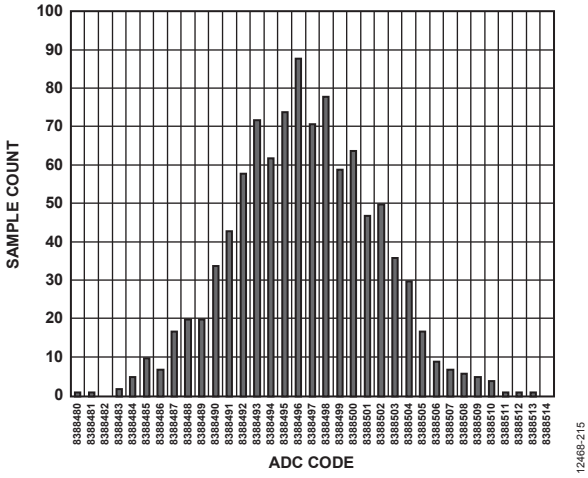


*Figure 15. Histogram (Analog Input Buffers Enabled, $V_{REF}$ = 5 V, Output Data Rate = 10 kSPS)*

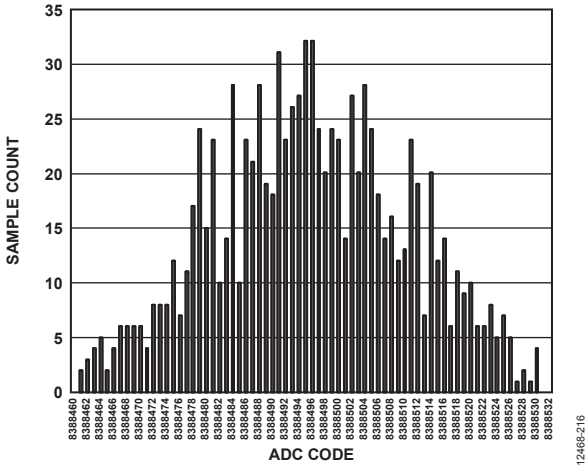


*Figure 16. Histogram (Analog Input Buffers Enabled, $V_{REF}$ = 5 V, Output Data Rate = 250 kSPS)*

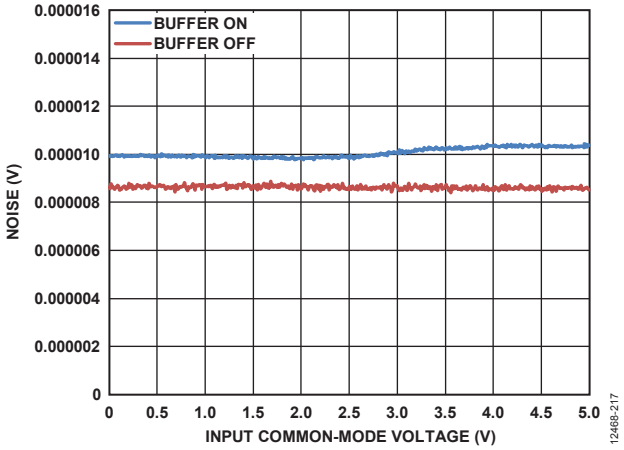


Figure 17. Noise vs. Input Common-Mode Voltage, Analog Input Buffers On and Off

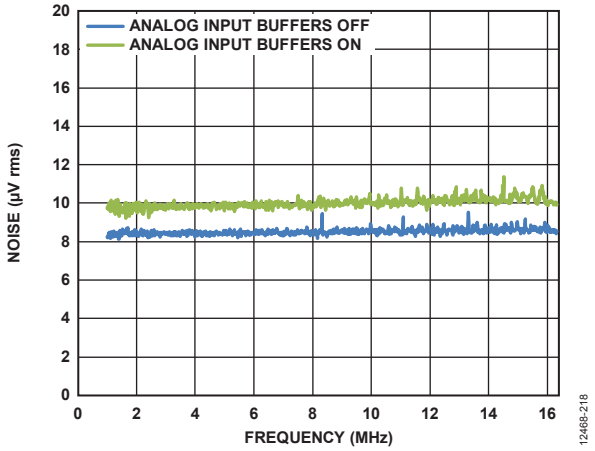


Figure 18. Noise vs. External Master Clock Frequency, Analog Input Buffers On and Off

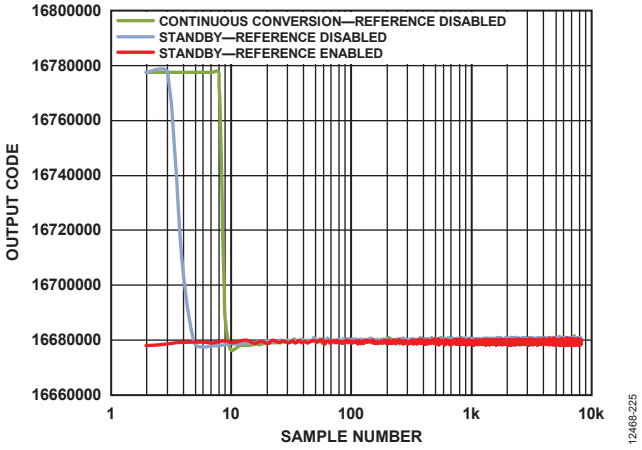


Figure 19. Internal Reference Settling Time

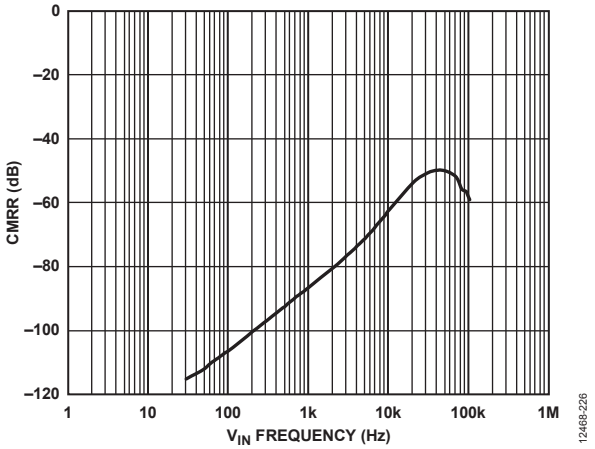


Figure 20. Common-Mode Rejection Ratio (CMRR) vs. $V_{IN}$ Frequency ($V_{IN}$ = 0.1 V, Output Data Rate = 250 kSPS)

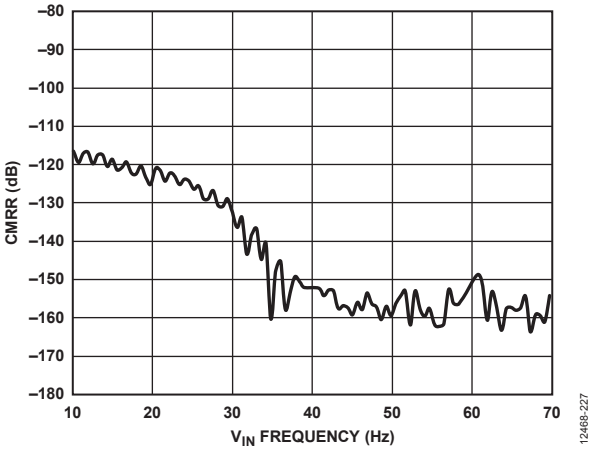


Figure 21. Common-Mode Rejection Ratio (CMRR) vs. $V_{IN}$ Frequency ($V_{IN}$ = 0.1 V, 10 Hz to 70 Hz, Output Data Rate = 20 SPS Enhanced Filter)

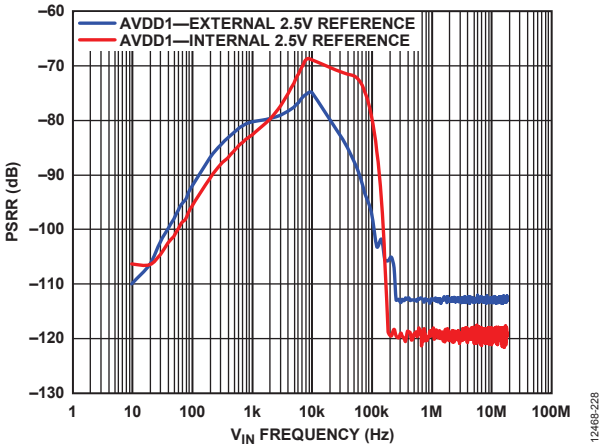


Figure 22. Power Supply Rejection Ratio (PSRR) vs. $V_{IN}$ Frequency

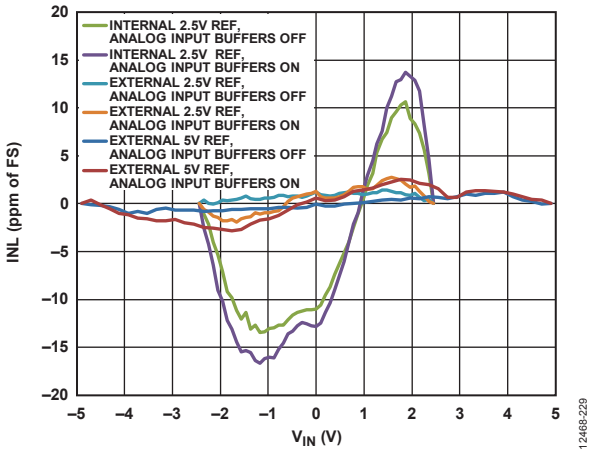


Figure 23. Integral Nonlinearity (INL) vs. $V_{IN}$ (Differential Input)

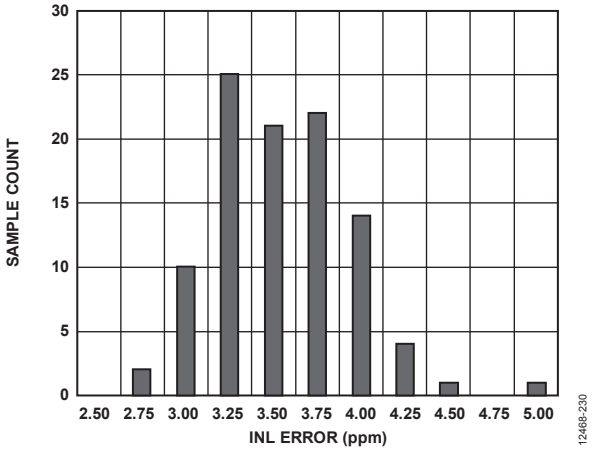


Figure 24. Integral Nonlinearity (INL) Distribution Histogram (Differential Input, Analog Input Buffers Enabled, $V_{REF}$ = 2.5 V External, 100 Units)

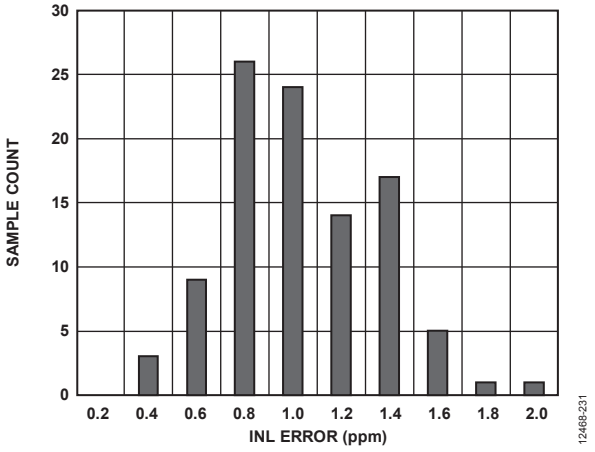


Figure 25. Integral Nonlinearity (INL) Distribution Histogram (Differential Input, Analog Input Buffers Disabled, $V_{REF}$ = 2.5 V External, 100 Units)

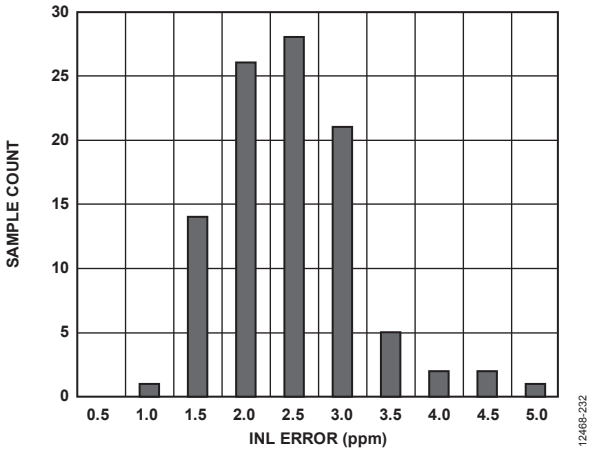


Figure 26. Integral Nonlinearity (INL) Distribution Histogram (Analog Input Buffers Enabled, Differential Input, $V_{REF}$ = 5 V External, 100 Units)

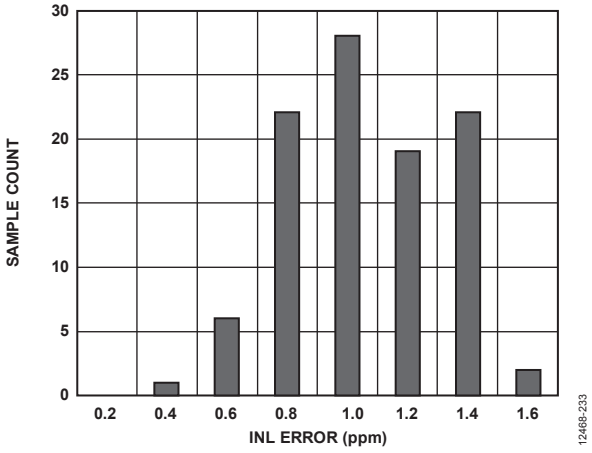


Figure 27. Integral Nonlinearity (INL) Distribution Histogram (Analog Input Buffers Disabled, Differential Input, $V_{REF}$ = 5 V External, 100 Units)

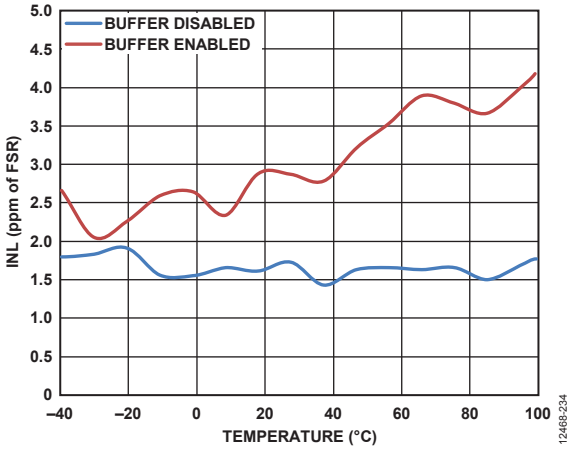


Figure 28. Integral Nonlinearity (INL) vs. Temperature (Differential Input, $V_{REF}$ = 2.5 V External)

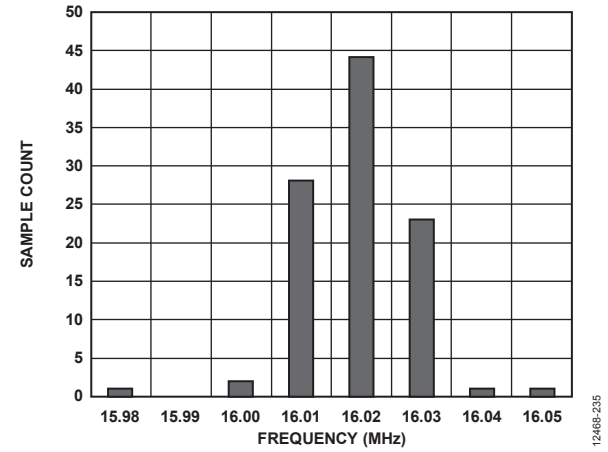


Figure 29. Internal Oscillator Frequency/Accuracy Distribution Histogram (100 Units)

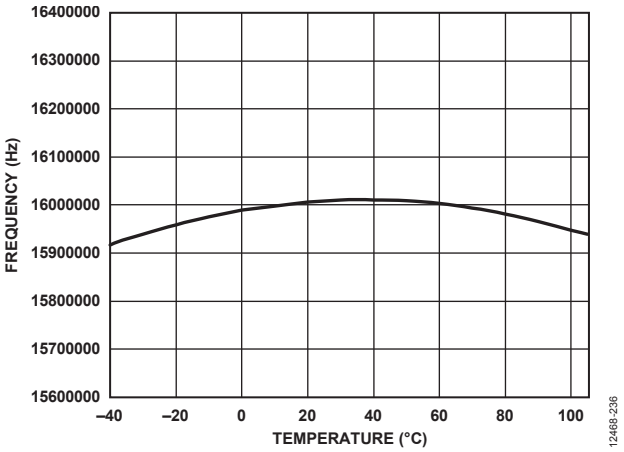


Figure 30. Internal Oscillator Frequency vs. Temperature

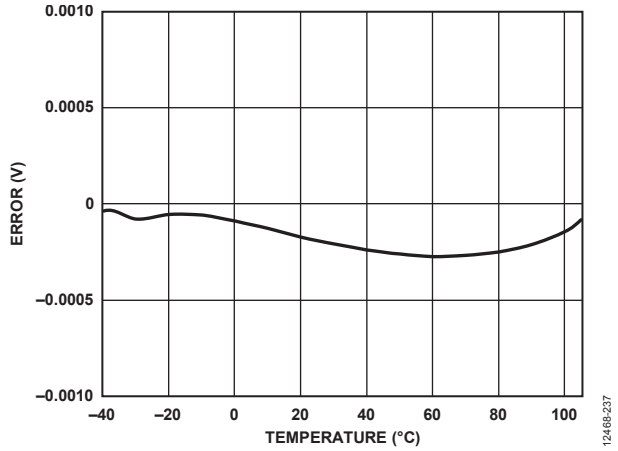


Figure 31. Absolute Reference Error vs. Temperature

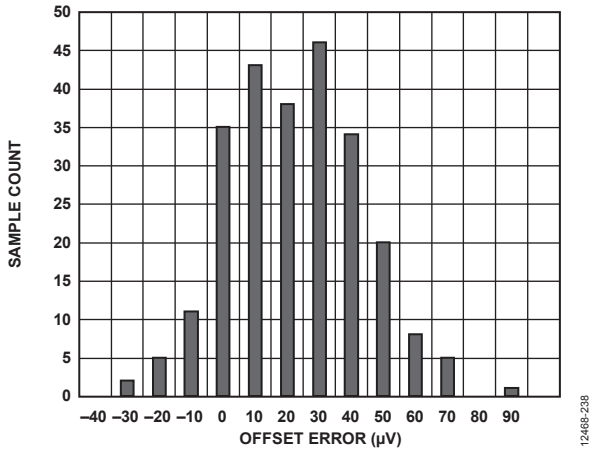


Figure 32. Offset Error Distribution Histogram (Internal Short) (248 Units)

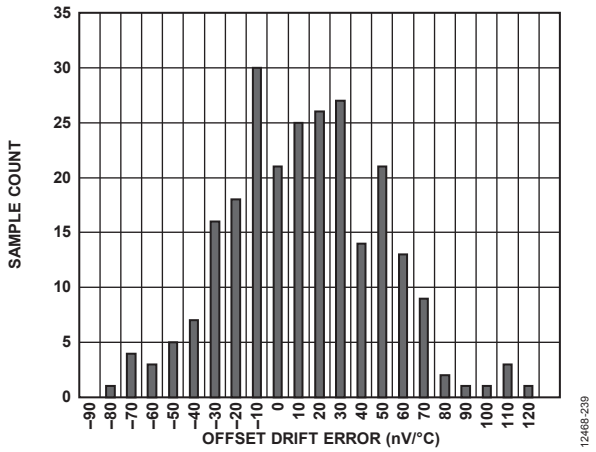


Figure 33. Offset Error Drift Distribution Histogram (Internal Short) (248 Units)

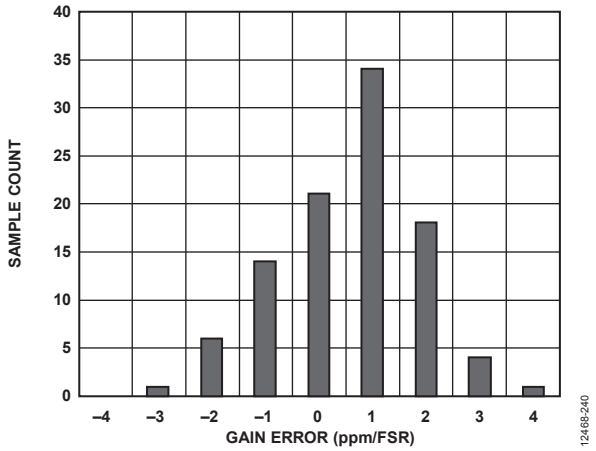


Figure 34. Gain Error Distribution Histogram (Analog Input Buffers Enabled) (100 Units)

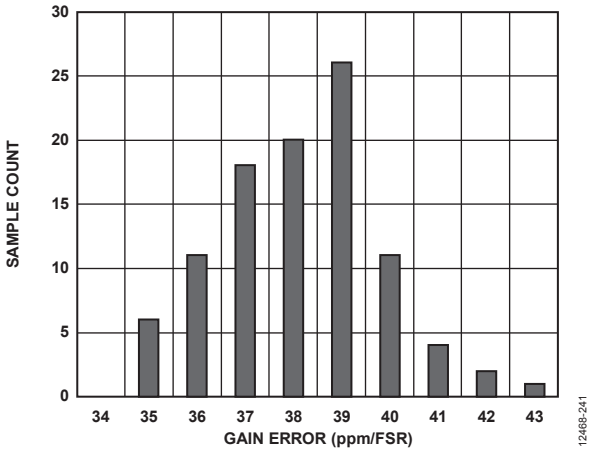


Figure 35. Gain Error Distribution Histogram
(Analog Input Buffers Disabled, 100 Units)

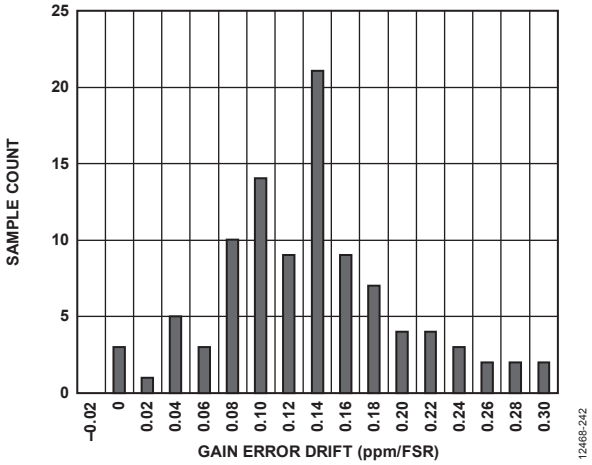


Figure 36. Gain Error Drift Distribution Histogram
(Analog Input Buffers Enabled, 100 Units)

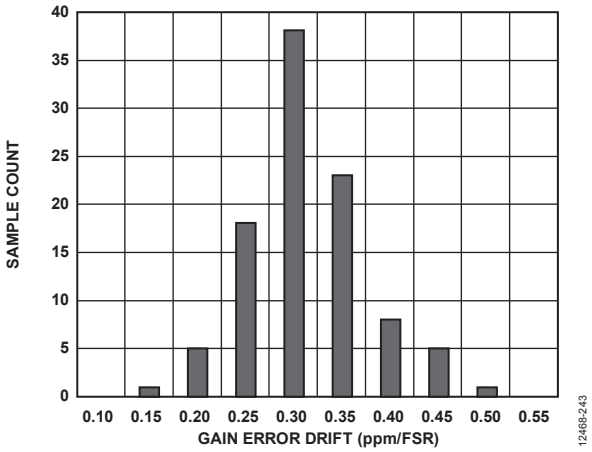


Figure 37. Gain Error Drift Distribution Histogram
(Analog Input Buffers Disabled, 100 Units)

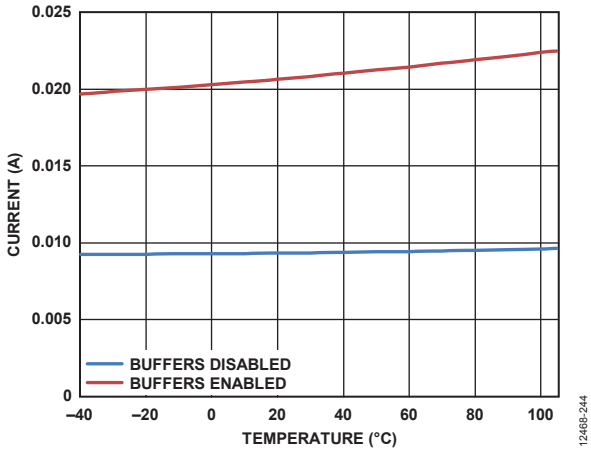


Figure 38. Current Consumption vs. Temperature
(Continuous Conversion Mode)

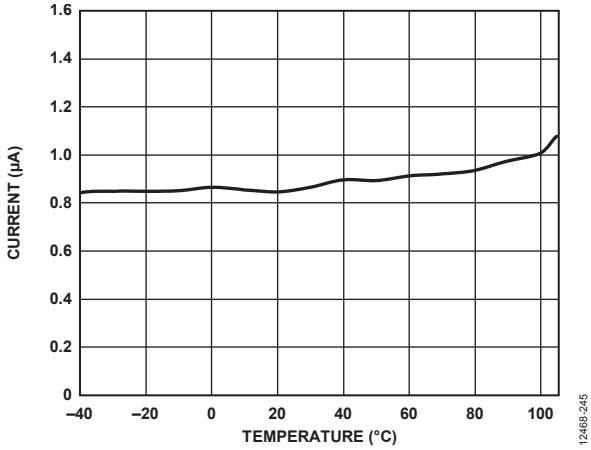


Figure 39. Current Consumption vs. Temperature (Power-Down Mode)

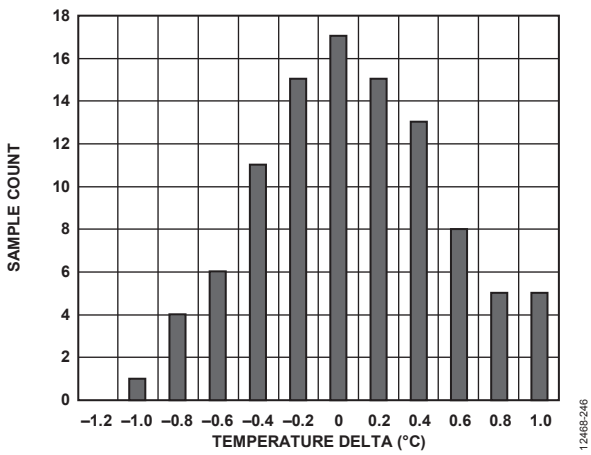


Figure 40. Temperature Sensor Distribution Histogram
(Uncalibrated, 100 Units)

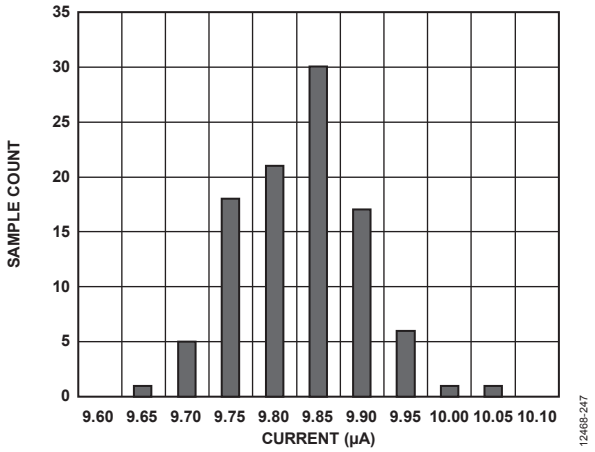


Figure 41. Burnout Current Distribution Histogram (100 Units)

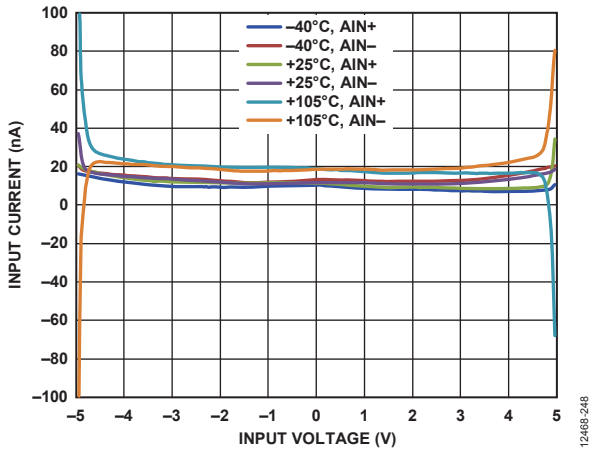


Figure 42. Analog Input Current vs. Input Voltage ($V_{CM}$ = 2.5 V)

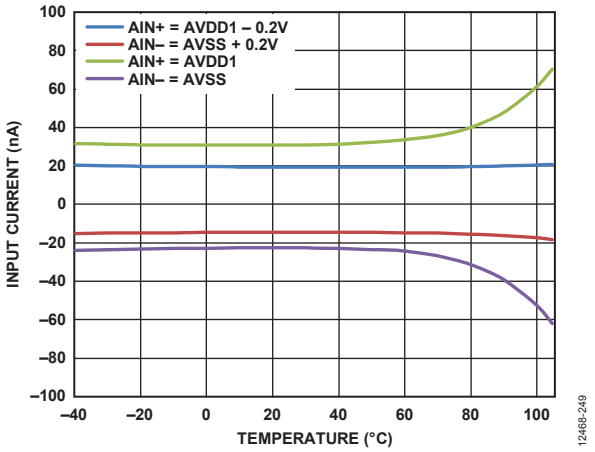


Figure 43. Analog Input Current vs. Temperature

# NOISE PERFORMANCE AND RESOLUTION

Table 6 and Table 7 show the rms noise, peak-to-peak noise, effective resolution and the noise free (peak-to-peak) resolution of the AD7175-2 for various output data rates and filters. The numbers given are for the bipolar input range with an external 5 V reference.

These numbers are typical and are generated with a differential input voltage of 0 V when the ADC is continuously converting on a single channel. It is important to note that the peak-to-peak resolution is calculated based on the peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no code flicker.

**Table 6. RMS Noise and Peak-to-Peak Resolution vs. Output Data Rate using Sinc5 + Sinc1 Filter (Default)[1]**

| Output Data Rate (SPS) | RMS Noise (μV rms) | Effective Resolution (Bits) | Peak-to-Peak Noise (μV p-p) | Peak-to-Peak Resolution (Bits) |
|---|---|---|---|---|
| Input Buffers Disabled | | | | |
| 250,000 | 8.7 | 20.1 | 65 | 17.2 |
| 62,500 | 5.5 | 20.8 | 43 | 17.8 |
| 10,000 | 2.5 | 21.9 | 18.3 | 19.1 |
| 1000 | 0.77 | 23.6 | 5.2 | 20.9 |
| 59.92 | 0.19 | 24 | 1.1 | 23.1 |
| 49.96 | 0.18 | 24 | 0.95 | 23.3 |
| 16.66 | 0.1 | 24 | 0.45 | 24 |
| 5 | 0.07 | 24 | 0.34 | 24 |
| Input Buffers Enabled | | | | |
| 250,000 | 9.8 | 20 | 85 | 16.8 |
| 62,500 | 6.4 | 20.6 | 55 | 17.5 |
| 10,000 | 3 | 21.7 | 23 | 18.7 |
| 1000 | 0.92 | 23.4 | 5.7 | 20.7 |
| 59.98 | 0.23 | 24 | 1.2 | 23.0 |
| 49.96 | 0.2 | 24 | 1 | 23.3 |
| 16.66 | 0.13 | 24 | 0.66 | 23.9 |
| 5 | 0.07 | 24 | 0.32 | 24 |

[1] Selected rates only, 1000 samples.

**Table 7. RMS Noise and Peak-to-Peak Resolution vs. Output Data Rate using Sinc3 Filter[1]**

| Output Data Rate (SPS) | RMS Noise (μV rms) | Effective Resolution (Bits) | Peak-to-Peak Noise (μV p-p) | Peak-to-Peak Resolution (Bits) |
|---|---|---|---|---|
| Input Buffers Disabled | | | | |
| 250,000 | 210 | 15.5 | 1600 | 12.6 |
| 62,500 | 5.2 | 20.9 | 40 | 17.9 |
| 10,000 | 1.8 | 22.4 | 14 | 19.4 |
| 1000 | 0.56 | 24 | 3.9 | 21.3 |
| 60 | 0.13 | 24 | 0.8 | 23.6 |
| 50 | 0.13 | 24 | 0.7 | 23.8 |
| 16.66 | 0.07 | 24 | 0.37 | 24 |
| 5 | 0.05 | 24 | 0.21 | 24 |
| Input Buffers Enabled | | | | |
| 250,000 | 210 | 15.5 | 1600 | 12.6 |
| 62,500 | 5.8 | 20.7 | 48 | 17.7 |
| 10,000 | 2.1 | 22.2 | 16 | 19.3 |
| 1000 | 0.71 | 23.7 | 4.5 | 21.1 |
| 60 | 0.17 | 24 | 1.1 | 23.1 |
| 50 | 0.15 | 24 | 0.83 | 23.5 |
| 16.66 | 0.12 | 24 | 0.6 | 24 |
| 5 | 0.08 | 24 | 0.35 | 24 |

[1] Selected rates only, 1000 samples.

# GETTING STARTED

The AD7175-2 offers the user a fast settling, high resolution, multiplexed ADC with high levels of configurability.

- Two fully differential or four single-ended analog inputs.
- Crosspoint multiplexer selects any analog input combination as the input signals to be converted, routing them to the modulator positive or negative input.
- True rail-to-rail buffered analog and reference inputs.
- Fully differential input or single-ended input relative to any analog input.
- Per channel configurability—up to four different setups can be defined. A separate setup can be mapped to each of the channels. Each setup allows the user to configure whether the buffers are enabled or disabled, gain and offset correction, filter type, output data rate, and reference source selection (internal/external).

The AD7175-2 includes a precision 2.5 V low drift (±2 ppm/°C) band gap internal reference. This reference can used for the ADC conversions, reducing the external component count. Alternatively, the reference can be output to the REFOUT pin to be used as a low noise biasing voltage for external circuitry. An example of this is using the REFOUT signal to set the input common mode for an external amplifier.

The AD7175-2 includes two separate linear regulator blocks for both the analog and digital circuitry. The analog LDO regulates the AVDD2 supply to 1.8 V, supplying the ADC core. The user can tie the AVDD1 and AVDD2 supplies together for easiest connection. If there is already a clean analog supply rail in the system in the range of 2 V (minimum) to 5.5 V (maximum), the user can also choose to connect this to the AVDD2 input, allowing lower power dissipation.

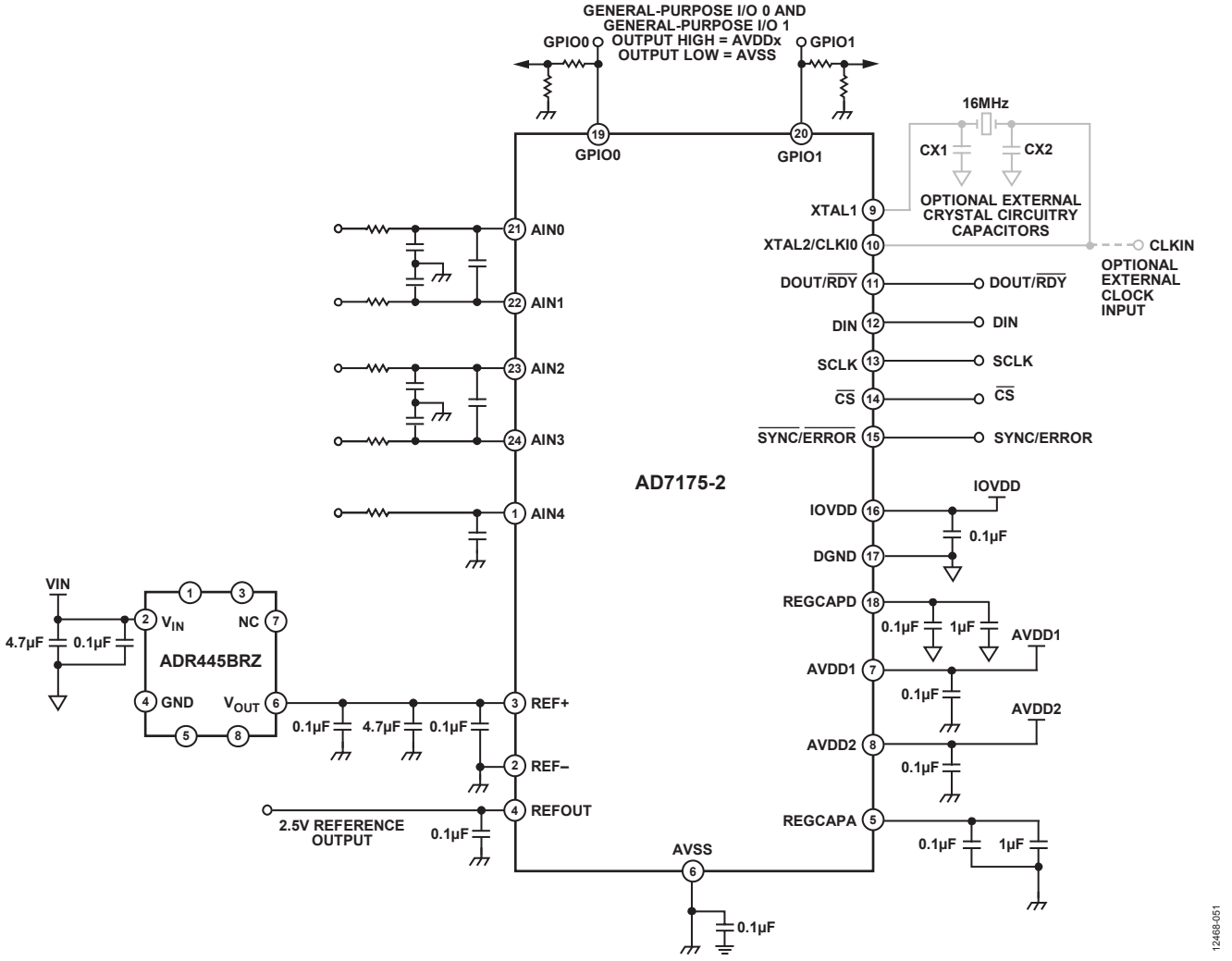


*Figure 44. Typical Connection Diagram*

The linear regulator for the digital IOVDD supply performs a similar function, regulating the input voltage applied at the IOVDD pin to 1.8 V for the internal digital filtering. The serial interface signals always operate from the IOVDD supply seen at the pin. This means that if 3.3 V is applied to the IOVDD pin, the interface logic inputs and outputs operate at this level.

The AD7175-2 can be used across a wide variety of applications, providing high resolution and accuracy. A sample of these scenarios is as follows:

- Fast scanning of analog input channels using the internal multiplexer
- Fast scanning of analog input channels using an external multiplexer with automatic control from the GPIOs.
- High resolution at lower speeds in either channel scanning or ADC per channel applications
- Single ADC per channel: the fast low latency output allows further application specific filtering in an external micro-controller, DSP, or FPGA

## POWER SUPPLIES

The AD7175-2 has three independent power supply pins: AVDD1, AVDD2, and IOVDD.

AVDD1 powers the crosspoint multiplexer and integrated analog and reference input buffers. AVDD1 is referenced to AVSS, and AVDD1 − AVSS = 5 V only. This can be a single 5 V supply or a ±2.5 V split supply. The split supply operation allows true bipolar inputs. When using split supplies, consider the absolute maximum ratings (see the Absolute Maximum Ratings section).

AVDD2 powers the internal 1.8 V analog LDO regulator. This regulator powers the ADC core. AVDD2 is referenced to AVSS, and AVDD2 − AVSS can range from 5.5 V (maximum) to 2 V (minimum).

IOVDD powers the internal 1.8 V digital LDO regulator. This regulator powers the digital logic of the ADC. IOVDD sets the voltage levels for the SPI interface of the ADC. IOVDD is referenced to DGND, and IOVDD − DGND can vary from 5.5 V (maximum) to 2 V (minimum).

There is no specific requirement for a power supply sequence on the AD7175-2. When all power supplies are stable, a device reset is required; see the AD7175-2 Reset section for details on how to reset the device.

## DIGITAL COMMUNICATION

The AD7175-2 has a 3- or 4-wire SPI interface that is compatible with QSPI™, MICROWIRE®, and DSPs. The interface operates in SPI Mode 3 and can be operated with $\overline{CS}$ tied low. In SPI Mode 3, the SCLK idles high, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge. This means that data is clocked out on the falling/drive edge and data is clocked in on the rising/sample edge.

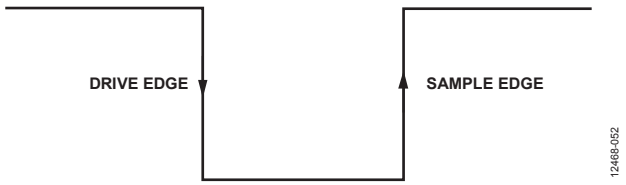


*Figure 45. SPI Mode 3 SCLK Edges*

### *Accessing the ADC Register Map*

The communications register controls access to the full register map of the ADC. This register is an 8-bit write only register. On power-up or after a reset, the digital interface defaults to a state where it is expecting a write to the communications register; therefore, all communication begins by writing to the communications register.

The data written to the communications register determines which register is being accessed and if the next operation is a read or write. The register address bits (RA[5:0]) determine the specific register to which the read or write operation applies.

When the read or write operation to the selected register is complete, the interface returns to the default state, where it expects a write operation to the communications register.

Figure 46 and Figure 47 illustrate writing to and reading from a register by first writing the 8-bit command to the communications register, followed by the data for that register.

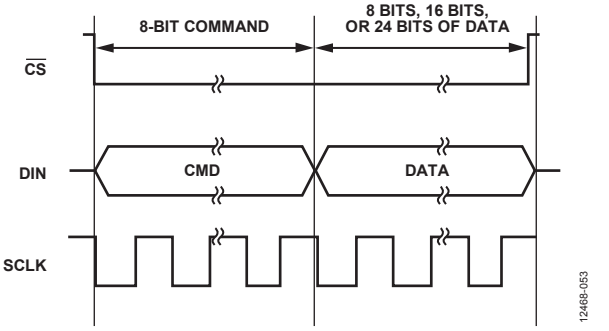


*Figure 46. Writing to a Register*
*(8-Bit Command with Register Address Followed by Data of 8, 16, or 24 Bits; Data Length on DIN Is Dependent on the Register Selected)*

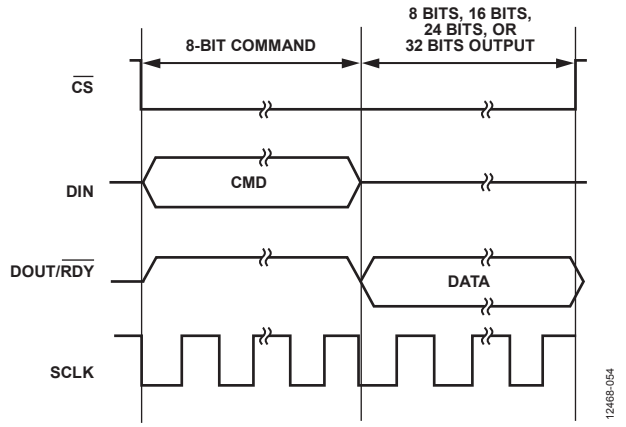


*Figure 47. Reading from a Register*
*(8-Bit Command with Register Address Followed by Data of 8, 16, or 24 Bits; Data Length on DOUT Is Dependent on the Register Selected)*

Reading the ID register is the recommended method for verifying correct communication with the device. The ID register is a read only register and contains the value 0x0CDX for the AD7175-2. The communications register and the ID register details are described in Table 8 and Table 9.

## AD7175-2 RESET

In situations where interface synchronization is lost, a write operation of at least 64 serial clock cycles with DIN high returns the ADC to the default state by resetting the entire device, including the register contents. Alternatively, if $\overline{CS}$ is being used with the digital interface, returning $\overline{CS}$ high sets the digital interface to the default state and halts any serial interface operation.

## CONFIGURATION OVERVIEW

After power-on or reset, the AD7175-2 default configuration is as follows:

- Channel configuration. CH0 is enabled, AIN0 is selected as the positive input, and AIN1 is selected as the negative input. Setup 0 is selected.
- Setup configuration. The internal reference and the analog input buffers are enabled. The reference input buffers are disabled.
- Filter configuration. The sinc5 + sinc 1 filter is selected and the maximum output data rate of 250 kSPS is selected.
- ADC mode. Continuous conversion mode and the internal oscillator are enabled.
- Interface mode. CRC and data + status output are disabled.

Note that only a few of the register setting options are shown; this list is just an example. For full register information, see the Register Details section.

Figure 48 shows an overview of the suggested flow for changing the ADC configuration, divided into the following three blocks:

- Channel configuration (see Box A in Figure 48)
- Setup configuration (see Box B in Figure 48)
- ADC mode and interface mode configuration (see Box C in Figure 48)

### *Channel Configuration*

The AD7175-2 has four independent channels and four independent setups. The user can select any of the analog input pairs on any channel, as well as any of the four setups for any channel, giving the user full flexibility in the channel configuration. This also allows per channel configuration when using differential inputs and single-ended inputs because each channel can have a dedicated setup.

#### Channel Registers

The channel registers select which of the five analog input pins (AIN0 to AIN4) are used as either the positive analog input (AIN+) or the negative analog input (AIN−) for that channel. This register also contains a channel enable/disable bit and the setup selection bits, which pick which of the four available setups to use for this channel.

When the AD7175-2 is operating with more than one channel enabled, the channel sequencer cycles through the enabled channels in sequential order, from Channel 0 to Channel 3. If a channel is disabled, it is skipped by the sequencer. Details of the channel register for Channel 0 are shown in Table 10.

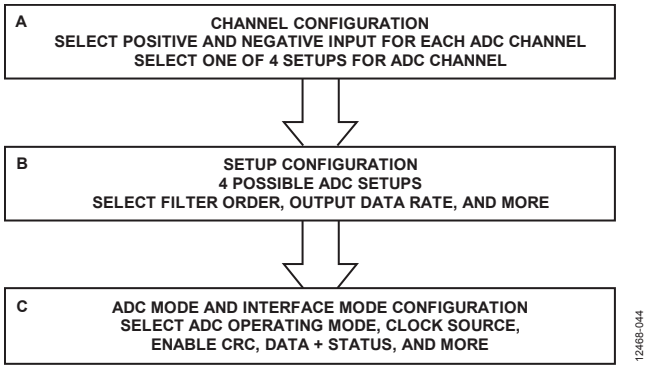


*Figure 48. Suggested ADC Configuration Flow*

**Table 8. Communications Register**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | COMMS | [7:0] | $\overline{WEN}$ | R/$\overline{W}$ | RA | | | | | | 0x00 | W |

**Table 9. ID Register**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x07 | ID | [15:8] | ID[15:8] | | | | | | | | 0x0CDX | R |
| | | [7:0] | ID[7:0] | | | | | | | | | |

**Table 10. Channel 0 Register**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x10 | CH0 | [15:8] | CH_EN0 | Reserved | SETUP_SEL[2:0] | | Reserved | | AINPOS0[4:3] | | 0x8001 | RW |
| | | [7:0] | AINPOS0[2:0] | | | AINNEG0 | | | | | | |

### *ADC Setups*

The AD7175-2 has four independent setups. Each setup consists of the following four registers:

- Setup configuration register
- Filter configuration register
- Offset register
- Gain register

For example, Setup 0 consists of Setup Configuration Register 0, Filter Configuration Register 0, Gain Register 0, and Offset Register 0. Figure 49 shows the grouping of these registers The setup is selectable from the channel registers (see the Channel Configuration section), which allows each channel to be assigned to one of four separate setups. Table 11 through Table 14 show the four registers that are associated with Setup 0. This structure is repeated for Setup 1 to Setup 3.

### Setup Configuration Registers

The setup configuration registers allow the user to select the output coding of the ADC by selecting between bipolar and unipolar. In bipolar mode, the ADC accepts negative differential input voltages, and the output coding is offset binary. In unipolar mode, the ADC accepts only positive differential voltages, and the coding is straight binary. In either case, the input voltage must be within the AVDD1/AVSS supply voltages. The user can select the reference source using this register. Three options are available: an internal 2.5 V reference, an external reference connected between the REF+ and REF− pins, or AVDD1 − AVSS. The analog input and reference input buffers can also be enabled or disabled using this register.

### Filter Configuration Registers

The filter configuration register selects which digital filter is used at the output of the ADC modulator. The order of the filter and the output data rate is selected by setting the bits in this register. For more information, see the Digital Filters section.

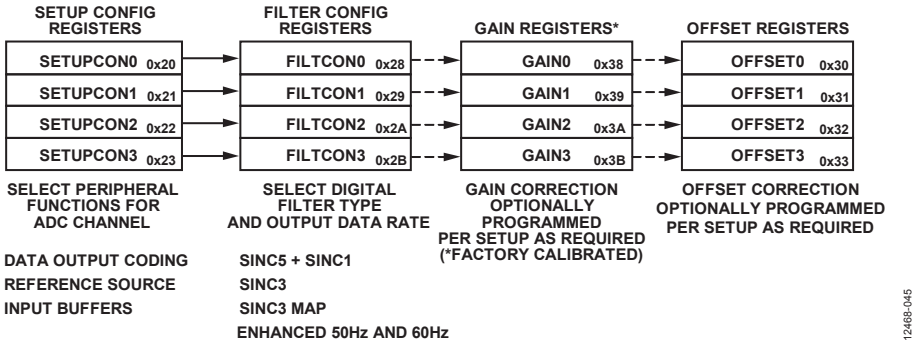


*Figure 49. ADC Setup Register Grouping*

**Table 11. Setup Configuration 0 Register**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x20 | SETUPCON0 | [15:8] | Reserved | | | BI_UNIPOLAR0 | REFBUF0+ | REFBUF0− | AINBUF0+ | AINBUF0− | 0x1320 | RW |
| | | [7:0] | BURNOUT_EN0 | Reserved | REF_SEL0 | | Reserved | | | | | |

**Table 12. Filter Configuration 0 Register**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x28 | FILTCON0 | [15:8] | SINC3_MAP0 | Reserved | | | ENHFILTEN0 | ENHFILT0 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER0 | | ODR0 | | | | | | |

**Table 13. Gain Configuration 0 Register**

| Reg. | Name | Bits | Bit[23:0] | Reset | RW |
|---|---|---|---|---|---|
| 0x38 | GAIN0 | [23:0] | GAIN0[23:0] | 0x5XXXX0 | RW |

**Table 14. Offset Configuration 0 Register**

| Reg. | Name | Bits | Bit[23:0] | Reset | RW |
|---|---|---|---|---|---|
| 0x30 | OFFSET0 | [23:0] | OFFSET0[23:0] | 0x800000 | RW |