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4.8 kHz, Ultralow Noise, 24-Bit Sigma-Delta ADC with PGA and AC Excitation

AD7195

FEATURES

AC or DC sensor excitation
RMS noise: 8.5 nV at 4.7 Hz (gain = 128)
16 noise-free bits at 2.4 kHz (gain = 128)
Up to 22.5 noise-free bits (gain = 1)
Offset drift: 5 nV/°C
Gain drift: 1 ppm/°C
Specified drift over time
2 differential/4 pseudo differential input channels
Automatic channel sequencer
Programmable gain (1 to 128)
Output data rate: 4.7 Hz to 4.8 kHz
Internal or external clock
Simultaneous 50 Hz/60 Hz rejection
Power supply
  AV_{DD}: 4.75 V to 5.25 V
  DV_{DD}: 2.7 V to 5.25 V
Current: 6 mA
Temperature range: −40°C to +105°C
Package: 32-lead LFCSP

INTERFACE

3-wire serial
SPI, QSPI™, MICROWIRE™, and DSP compatible
Schmitt trigger on SCLK

APPLICATIONS

Weigh scales
Strain gage transducers
Pressure measurement
Temperature measurement
Chromatography
PLC/DCS analog input modules
Data acquisition
Medical and scientific instrumentation

GENERAL DESCRIPTION

The AD7195 is a low noise, complete analog front end for high precision measurement applications. It contains a low noise, 24-bit sigma-delta (Σ-Δ) analog-to-digital converter (ADC). The on-chip low noise gain stage means that signals of small amplitude can be interfaced directly to the ADC. The AD7195 contains ac excitation, which is used to remove dc-induced offsets from bridge sensors.

The device can be configured to have two differential inputs or four pseudo differential inputs. The on-chip channel sequencer allows several channels to be enabled, and the AD7195 sequentially converts on each enabled channel. This simplifies communication with the part. The on-chip 4.92 MHz clock can be used as the clock source to the ADC or, alternatively, an external clock or crystal can be used. The output data rate from the part can be varied from 4.7 Hz to 4.8 kHz.

The device has two digital filter options. The choice of filter affects the rms noise/noise-free resolution at the programmed output data rate, the settling time, and the 50 Hz/60 Hz rejection. For applications that require all conversions to be settled, the AD7195 includes a zero latency feature.

The part operates with a 5 V analog power supply and a digital power supply from 2.7 V to 5.25 V. It consumes a current of 6 mA. It is housed in a 32-lead LFCSP package.

FUNCTIONAL BLOCK DIAGRAM

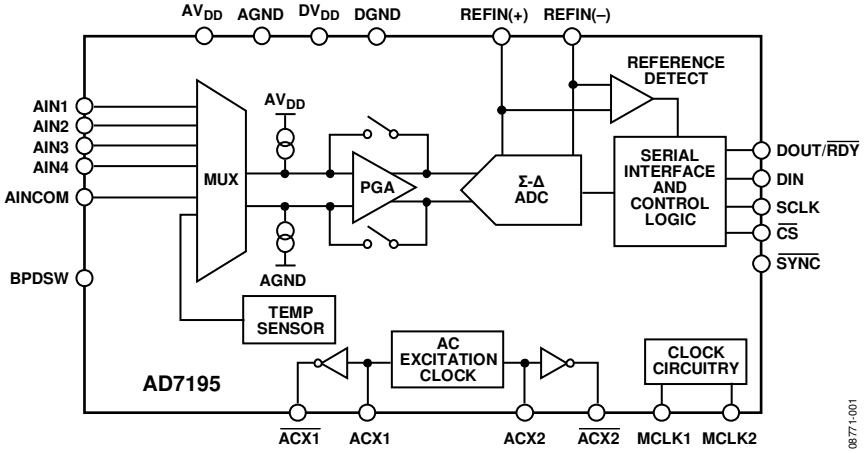

Figure 1.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

AD7195* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7195 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1069: Zero Latency for the AD7190, AD7192, AD7193, AD7194, and AD7195
- AN-1084: Channel Switching: AD7190, AD7192, AD7193, AD7194, AD7195
- AN-1131: Chopping on the AD7190, AD7192, AD7193, AD7194, and AD7195
- AN-1264: Precision Signal Conditioning for High Resolution Industrial Applications

Data Sheet

- AD7195: 4.8 kHz, Ultralow Noise, 24-Bit Sigma-Delta ADC with PGA and AC Excitation

User Guides

- UG-257: Evaluation Board for the AD7195, 4.8 kHz, Ultralow Noise, 24-Bit Sigma-Delta ADC

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD7190 - Microcontroller No-OS Driver
- AD7192 IIO High Precision ADC Linux Driver

TOOLS AND SIMULATIONS

- Download the Active Functional Model to evaluate and debug AD719x

REFERENCE MATERIALS

Tutorials

- Tutorial on Technical and Performance Benefits of AD719x Family

DESIGN RESOURCES

- AD7195 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7195 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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TABLE OF CONTENTS

REVISION HISTORY

1/10—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 5.25 V, AGND = DGND = 0 V; REFIN(+) = AV_{DD}, REFIN(−) = AGND, MCLK = 4.92 MHz, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments[1]
ADC					
Output Data Rate	4.7		4800	Hz	Chop disabled
	1.17		1200	Hz	Chop enabled, sinc[4] filter
	1.56		1600	Hz	Chop enabled, sinc[3] filter
No Missing Codes[2]	24			Bits	FS > 1, sinc[4] filter[3]
	24			Bits	FS > 4, sinc[3] filter[3]
Resolution					See the RMS Noise and Resolution section
RMS Noise and Output Data Rates					See the RMS Noise and Resolution section
Integral Nonlinearity					
Gain = 1[2]		±1	±5	ppm of FSR	
Gain > 1		±5	±15	ppm of FSR	
Offset Error[4, 5]		±75/gain		μV	Chop disabled
		±0.5		μV	Chop enabled
Offset Error Drift vs. Temperature		±100/gain		nV/°C	Gain = 1 to 16; chop disabled
		±5		nV/°C	Gain = 32 to 128; chop disabled
		±5		nV/°C	Chop enabled
Offset Error Drift vs. Time		25		nV/1000 hours	Gain ≥ 32
Gain Error[4]		±0.001	±0.005	% max	AV_{DD} = 5 V, gain = 1, T_A = 25°C (factory calibration conditions)
		±0.006		%	Gain > 1, post internal full-scale calibration
Gain Drift vs. Temperature		±1		ppm/°C	
Gain Drift vs. Time		10		ppm/1000 hours	Gain = 1
Power Supply Rejection		95		dB	Gain = 1, V_{IN} = 1 V
	98	103			Gain = 8, V_{IN} = 1 V/gain
	100	110		dB	Gain > 8, V_{IN} = 1 V/gain
Common-Mode Rejection					
@ DC[2]	100	115		dB min	Gain = 1, V_{IN} = 1 V
@ DC	115	140		dB min	Gain > 1, V_{IN} = 1 V/gain
@ 50 Hz, 60 Hz[2]	120			dB	10 Hz output data rate, 50 ± 1 Hz, 60 ± 1 Hz
@ 50 Hz, 60 Hz[2]	120			dB	50 ± 1 Hz (50 Hz output data rate), 60 ± 1 Hz (60 Hz output data rate)
Normal Mode Rejection[2]					
Sinc[4] Filter					
Internal Clock					
@ 50 Hz, 60 Hz	100			dB	10 Hz output data rate, 50 ± 1 Hz, 60 ± 1 Hz
	74			dB	50 Hz output data rate, REJ60[6] = 1, 50 ± 1 Hz, 60 ± 1 Hz
@ 50 Hz	96			dB	50 Hz output data rate, 50 ± 1 Hz
@ 60 Hz	97			dB	60 Hz output data rate, 60 ± 1 Hz
External Clock					
@ 50 Hz, 60 Hz	120			dB	10 Hz output data rate, 50 ± 1 Hz, 60 ± 1 Hz
	82			dB	50 Hz output data rate, REJ60[6] = 1, 50 ± 1 Hz, 60 ± 1 Hz
@ 50 Hz	120			dB	50 Hz output data rate, 50 ± 1 Hz
@ 60 Hz	120			dB	60 Hz output data rate, 60 ± 1 Hz
Sinc[3] Filter					
Internal Clock					
@ 50 Hz, 60 Hz	75			dB	10 Hz output data rate, 50 ± 1 Hz, 60 ± 1 Hz
	60			dB	50 Hz output data rate, REJ60[6] = 1, 50 ± 1 Hz, 60 ± 1 Hz
@ 50 Hz	70			dB	50 Hz output data rate, 50 ± 1 Hz
@ 60 Hz	70			dB	60 Hz output data rate, 60 ± 1 Hz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments[1]
External Clock					
@ 50 Hz, 60 Hz	100			dB	10 Hz output data rate, 50 ± 1 Hz, 60 ± 1 Hz
	67			dB	50 Hz output data rate, REJ60[6] = 1, 50 ± 1 Hz, 60 ± 1 Hz
@ 50 Hz	95			dB	50 Hz output data rate, 50 ± 1 Hz
@ 60 Hz	95			dB	60 Hz output data rate, 60 ± 1 Hz
ANALOG INPUTS					
Differential Input Voltage Ranges		$\pm V_{REF}$/gain		V	VREF = REFIN(+) − REFIN(−), gain = 1 to 128
	$-(AV_{DD} - 1.25\ V)$/gain		$+(AV_{DD} - 1.25\ V)$/gain	V	Gain > 1
Absolute AIN Voltage Limits[2]					
Unbuffered Mode	AGND − 0.05		AV_{DD} + 0.05	V	
Buffered Mode	AGND + 0.25		AV_{DD} − 0.25	V	
Analog Input Current					
Buffered Mode					
Input Current[2]	−2		+2	nA	Gain = 1
	−4.5		+4.5	nA	Gain > 1
Input Current Drift		±5		pA/°C	
Unbuffered Mode					
Input Current		±5		µA/V	Gain = 1, input current varies with input voltage
		±1		µA/V	Gain > 1
Input Current Drift		±0.05		nA/V/°C	External clock
		±1.6		nA/V/°C	Internal clock
REFERENCE INPUT					
REFIN Voltage	1	AV_{DD}	AV_{DD}	V	REFIN = REFIN(+) − REFIN(−). The differential input must be limited to $\pm(AV_{DD} - 1.25\ V)$/gain when gain > 1
Absolute REFIN Voltage Limits[2]	GND − 0.05		AV_{DD} + 0.05	V	
Average Reference Input Current		7		µA/V	
Average Reference Input Current Drift		±0.03		nA/V/°C	External clock
		±1.3		nA/V/°C	Internal clock
Normal Mode Rejection[2]		Same as for analog inputs			
Common-Mode Rejection		95		dB	
Reference Detect Levels	0.3		0.6	V	
TEMPERATURE SENSOR					
Accuracy		±2		°C	Applies after user calibration at 25°C
Sensitivity		2815		Codes/°C	Bipolar mode
BRIDGE POWER-DOWN SWITCH					
R_{ON}			10	Ω	
Allowable Current[2]			30	mA	Continuous current
BURNOUT CURRENTS					
AIN Current		500		nA	Analog inputs must be buffered and chop disabled
DIGITAL OUTPUTS (ACXx, $\overline{ACXx}$)					
Output High Voltage, V_{OH}[2]	4			V	AV_{DD} = 5 V, I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}[2]			0.4	V	AV_{DD} = 5 V, I_{SINK} = 800 µA
INTERNAL/EXTERNAL CLOCK					
Internal Clock					
Frequency	4.72		5.12	MHz	
Duty Cycle		50:50		%	
External Clock/Crystal[2]					
Frequency	2.4576	4.9152	5.12	MHz	
Input Low Voltage V_{INL}			0.8	V	DV_{DD} = 5 V
			0.4	V	DV_{DD} = 3 V
Input High Voltage, V_{INH}	2.5			V	DV_{DD} = 3 V
	3.5			V	DV_{DD} = 5 V
Input Current	−10		+10	µA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments[1]
LOGIC INPUTS					
Input High Voltage, V_{INH}[2]	2			V	
Input Low Voltage, V_{INL}[2]			0.8	V	
Hysteresis[2]	0.1		0.25	V	
Input Currents	−10		+10	μA	
LOGIC OUTPUT (DOUT/$\overline{RDY}$)					
Output High Voltage, V_{OH}[2]	DV_{DD} − 0.6			V	DV_{DD} = 3 V, I_{SOURCE} = 100 μA
Output Low Voltage, V_{OL}[2]			0.4	V	DV_{DD} = 3 V, I_{SINK} = 100 μA
Output High Voltage, V_{OH}[2]	4			V	DV_{DD} = 5 V, I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}[2]			0.4	V	DV_{DD} = 5 V, I_{SINK} = 1.6 mA
Floating-State Leakage Current	−10		+10	μA	
Floating-State Output Capacitance		10		pF	
Data Output Coding		Offset binary			
SYSTEM CALIBRATION[2]					
Full-Scale Calibration Limit			1.05 × FS	V	
Zero-Scale Calibration Limit	−1.05 × FS			V	
Input Span	0.8 × FS		2.1 × FS	V	
POWER REQUIREMENTS[7]					
Power Supply Voltage					
AV_{DD} − AGND	4.75		5.25	V	
DV_{DD} − DGND	2.7		5.25	V	
Power Supply Currents					
AI_{DD} Current		0.85	1	mA	gain = 1, buffer off
		1.1	1.3	mA	gain = 1, buffer on
		3.5	4.5	mA	gain = 8, buffer off
		4	5	mA	gain = 8, buffer on
		5	6.4	mA	gain = 16 to 128, buffer off
		5.5	6.9	mA	gain = 16 to 128, buffer on
DI_{DD} Current		0.35	0.4	mA	DV_{DD} = 3 V
		0.5	0.6	mA	DV_{DD} = 5 V
		1.5		mA	External crystal used
I_{DD} (Power-Down Mode)			2	μA	

[1] Temperature range: −40°C to +105°C.
[2] Specification is not production tested, but is supported by characterization data at initial product release.
[3] FS is the decimal equivalent of Bit FS9 to Bit FS0 in the mode register.
[4] Following a system or internal zero-scale calibration, the offset error is in the order of the noise for the programmed gain and output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed gain and output data rate.
[5] The analog inputs are configured for differential mode.
[6] REJ60 is a bit in the mode register. When the output data rate is set to 50 Hz, setting REJ60 to 1 places a notch at 60 Hz, allowing simultaneous 50 Hz/60 Hz rejection.
[7] Digital inputs equal to DV_{DD} or DGND.

TIMING CHARACTERISTICS

AV_{DD} = 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 5.25 V, AGND = DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = DV_{DD}, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Unit	Conditions/Comments[1, 2]
READ AND WRITE OPERATIONS			
t_3	100	ns min	SCLK high pulse width
t_4	100	ns min	SCLK low pulse width
READ OPERATION			
t_1	0	ns min	$\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time
	60	ns max	DV_{DD} = 4.75 V to 5.25 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_2[3]	0	ns min	SCLK active edge to data valid delay[4]
	60	ns max	DV_{DD} = 4.75 V to 5.25 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_5[5, 6]	10	ns min	Bus relinquish time after $\overline{CS}$ inactive edge
	80	ns max	
t_6	0	ns min	SCLK inactive edge to $\overline{CS}$ inactive edge
t_7	10	ns min	SCLK inactive edge to DOUT/$\overline{RDY}$ high
WRITE OPERATION			
t_8	0	ns min	$\overline{CS}$ falling edge to SCLK active edge setup time[4]
t_9	30	ns min	Data valid to SCLK edge setup time
t_{10}	25	ns min	Data valid to SCLK edge hold time
t_{11}	0	ns min	$\overline{CS}$ rising edge to SCLK edge hold time

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.
[2] See Figure 3 and Figure 4.
[3] These numbers are measured with the load circuit shown in Figure 2 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[4] The SCLK active edge is the falling edge of SCLK.
[5] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit shown in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.
[6] $\overline{RDY}$ returns high after a read of the data register. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high, although care should be taken to ensure that subsequent reads do not occur close to the next output update. If the continuous read feature is enabled, the digital word can be read only once.

Circuit and Timing Diagram

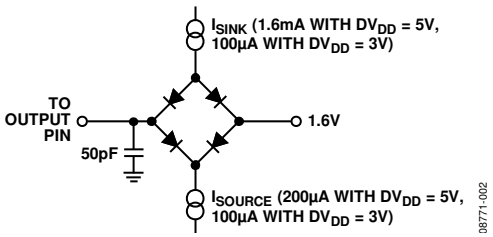

Figure 2. Load Circuit for Timing Characterization

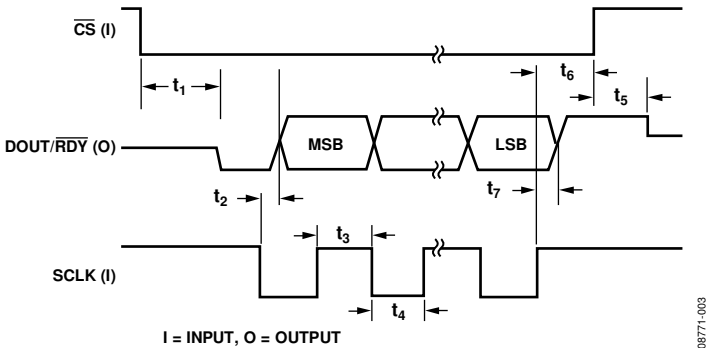

Figure 3. Read Cycle Timing Diagram

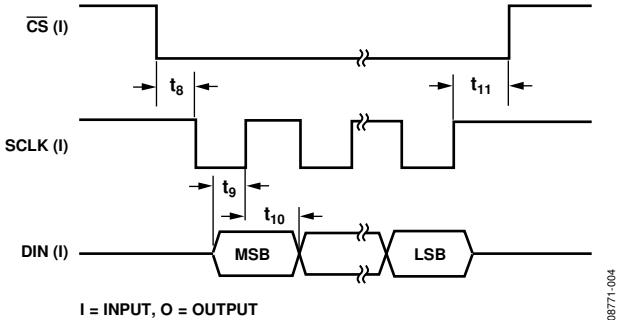

Figure 4. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +6.5 V
DV_{DD} to AGND	−0.3 V to +6.5 V
AGND to DGND	−0.3 V to +0.3 V
Analog Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
AIN/Digital Input Current	10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature, Soldering Reflow	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP_WQ	32.5	32.71	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

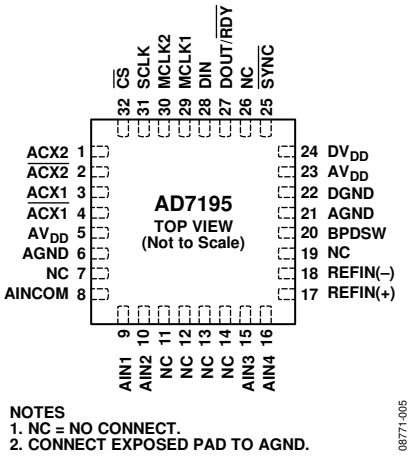

Figure 5.Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	ACX2	Digital Output. Provides a signal that can be used to control the reversing of the bridge excitation in ac excited bridge applications. In ac mode, ACX2 toggles in anti-phase with ACX1. If the ACX bit equals zero (ac excitation turned off), the ACX2 output remains low. When toggling, it is guaranteed to be nonoverlapping with ACX1. The nonoverlap interval between ACX1 and ACX2 is 1/(master clock) which is equal to 200 ns when a 4.92 MHz clock is used.
2	$\overline{\text{ACX2}}$	Digital Output. Provides a signal that can be used to control the reversing of the bridge excitation in ac excited bridge applications. This output is the inverse of ACX2. If the ACX bit equals zero (ac excitation turned off), the $\overline{\text{ACX2}}$ output remains high.
3	ACX1	Digital Output. Provides a signal that can be used to control the reversing of the bridge excitation in ac excited bridge applications. When ACX1 is high, the bridge excitation is taken as normal and when ACX1 is low, the bridge excitation is reversed (chopped). If the Bit ACX equals zero (ac excitation turned off), the ACX1 output remains high.
4	$\overline{\text{ACX1}}$	Digital Output. Provides a signal that can be used to control the reversing of the bridge excitation in ac excited bridge applications. This output is the inverse of ACX1. When $\overline{\text{ACX1}}$ is low, the bridge excitation is taken as normal and when $\overline{\text{ACX1}}$ is high, the bridge excitation is reversed (chopped). If the ACX bit equals zero (ac excitation turned off), the $\overline{\text{ACX1}}$ output remains low.
5	AV_{DD}	Analog Supply Voltage, 4.75 V to 5.25 V. AV_{DD} is independent of DV_{DD}.
6	AGND	Analog Ground Reference Point.
7	NC	No Connect. This pin should be tied to AGND.
8	AINCOM	Analog inputs AIN1 to AIN4 are referenced to this input when configured for pseudo differential operation.
9	AIN1	Analog Input. This pin can be configured as the positive input of a fully differential input pair when used with AIN2 or as a pseudo differential input when used with AINCOM.
10	AIN2	Analog Input. This pin can be configured as the negative input of a fully differential input pair when used with AIN1 or as a pseudo differential input when used with AINCOM.
11	NC	No Connect. This pin should be tied to AGND.
12	NC	No Connect. This pin should be tied to AGND.
13	NC	No Connect. This pin should be tied to AGND.
14	NC	No Connect. This pin should be tied to AGND.
15	AIN3	Analog Input. This pin can be configured as the positive input of a fully differential input pair when used with AIN4 or as a pseudo differential input when used with AINCOM.
16	AIN4	Analog Input. This pin can be configured as the negative input of a fully differential input pair when used with AIN3 or as a pseudo differential input when used with AINCOM.
17	REFIN(+)	Positive Reference Input. An external reference can be applied between REFIN(+) and REFIN(–). REFIN(+) can lie anywhere between AV_{DD} and AGND + 1 V. The nominal reference voltage, (REFIN(+) − REFIN(–)), is AV_{DD}, but the part functions with a reference from 1 V to AV_{DD}.
18	REFIN(–)	Negative Reference Input. This reference input can lie anywhere between AGND and AV_{DD} − 1 V.
19	NC	No Connect. This pin should be tied to AGND.

Pin No.	Mnemonic	Description
20	BPDSW	Bridge Power-Down Switch to AGND.
21	AGND	Analog Ground Reference Point.
22	DGND	Digital Ground Reference Point.
23	AV_{DD}	Analog Supply Voltage, 4.75 V to 5.25 V. AV_{DD} is independent of DV_{DD}.
24	DV_{DD}	Digital Supply Voltage, 2.7 V to 5.25 V. DV_{DD} is independent of AV_{DD}.
25	$\overline{SYNC}$	Logic input that allows for synchronization of the digital filters and analog modulators when using a number of AD7195 devices. While $\overline{SYNC}$ is low, the nodes of the digital filter, the filter control logic, and the calibration control logic are reset, and the analog modulator is also held in its reset state. $\overline{SYNC}$ does not affect the digital interface but does reset $\overline{RDY}$ to a high state if it is low. $\overline{SYNC}$ has a pull-up resistor internally to DV_{DD}.
26	NC	No Connect. This pin should be tied to AGND.
27	DOUT/$\overline{RDY}$	Serial Data Output/Data Ready Output. DOUT/$\overline{RDY}$ serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/$\overline{RDY}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{RDY}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/$\overline{RDY}$ pin. With $\overline{CS}$ low, the data-/control-word information is placed on the DOUT/$\overline{RDY}$ pin on the SCLK falling edge and is valid on the SCLK rising edge.
28	DIN	Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers in the ADC, with the register selection bits of the communications register identifying the appropriate register.
29	MCLK1	When the master clock for the device is provided externally by a crystal, the crystal is connected between MCLK1 and MCLK2.
30	MCLK2	Master Clock Signal for the Device. The AD7195 has an internal 4.92 MHz clock. This internal clock can be made available on the MCLK2 pin. The clock for the AD7195 can be provided externally also in the form of a crystal or external clock. A crystal can be tied across the MCLK1 and MCLK2 pins. Alternatively, the MCLK2 pin can be driven with a CMOS-compatible clock and the MCLK1 pin left unconnected.
31	SCLK	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information transmitted to or from the ADC in smaller batches of data.
32	$\overline{CS}$	Chip Select Input. This is an active low logic input used to select the ADC. $\overline{CS}$ can be used to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device.

TYPICAL PERFORMANCE CHARACTERISTICS

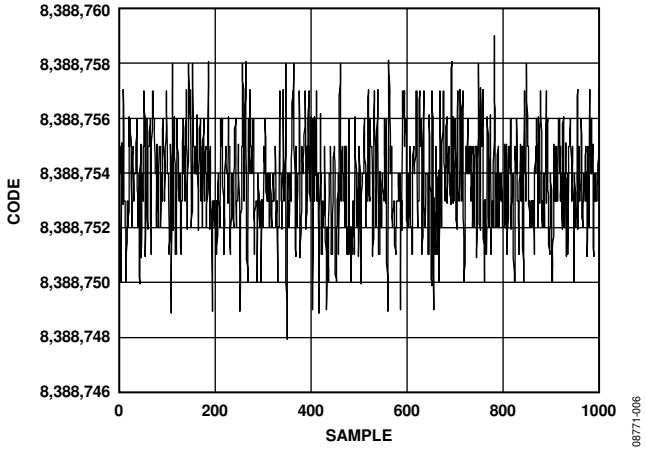

Figure 6. Noise (V_{REF} = 5 V, Output Data Rate = 4.7 Hz, Gain = 128, Chop Disabled, Sinc^4 Filter)

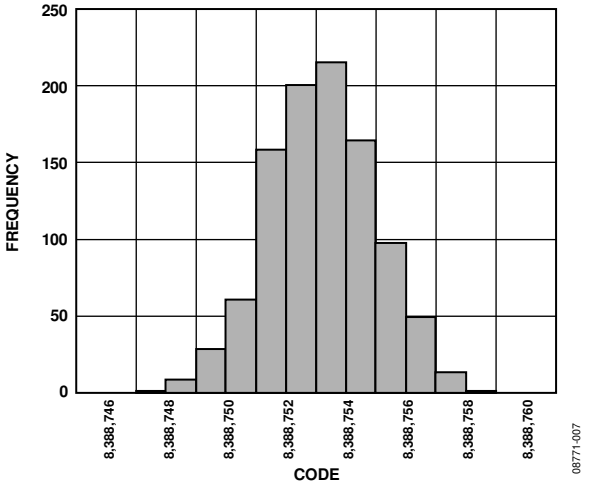

Figure 7. Noise Distribution Histogram (V_{REF} = 5 V, Output Data Rate = 4.7 Hz, Gain = 128, Chop Disabled, Sinc^4 Filter)

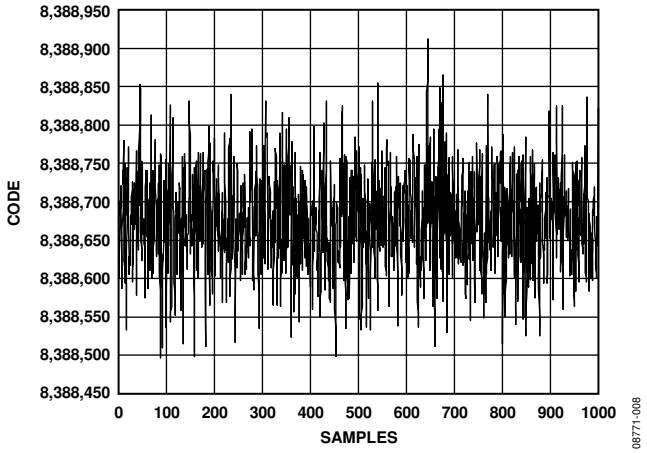

Figure 8. Noise (V_{REF} = 5 V, Output Data Rate = 4800 Hz, Gain = 128, Chop Disabled, Sinc^4 Filter)

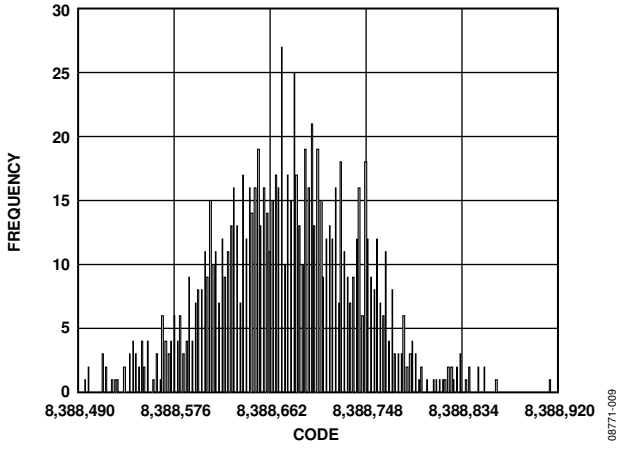

Figure 9. Noise Distribution Histogram (V_{REF} = 5 V, Output Data Rate = 4800 Hz, Gain = 128, Chop Disabled, Sinc^4 Filter)

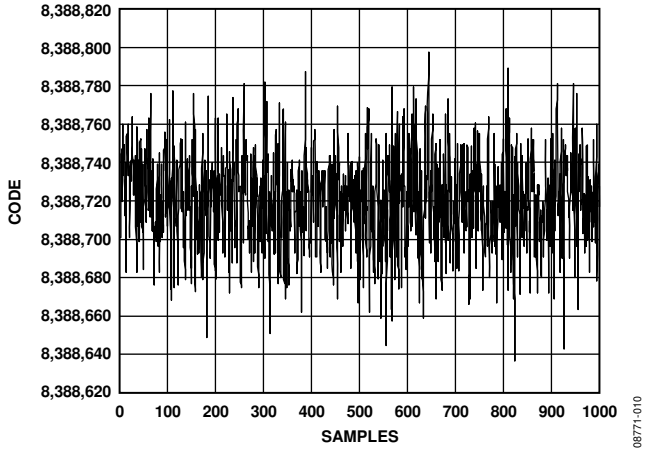

Figure 10. Noise (V_{REF} = 5 V, Output Data Rate = 4800 Hz, Gain = 1, Chop Disabled, Sinc^4 Filter)

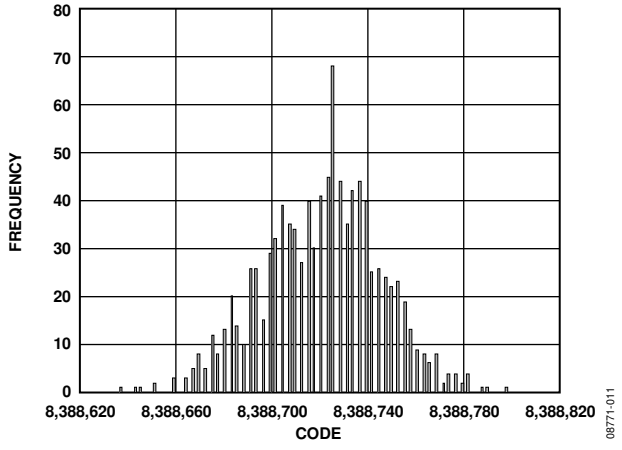

Figure 11. Noise Distribution Histogram (V_{REF} = 5 V, Output Data Rate = 4800 Hz, Gain = 1, Chop Disabled, Sinc^4 Filter)

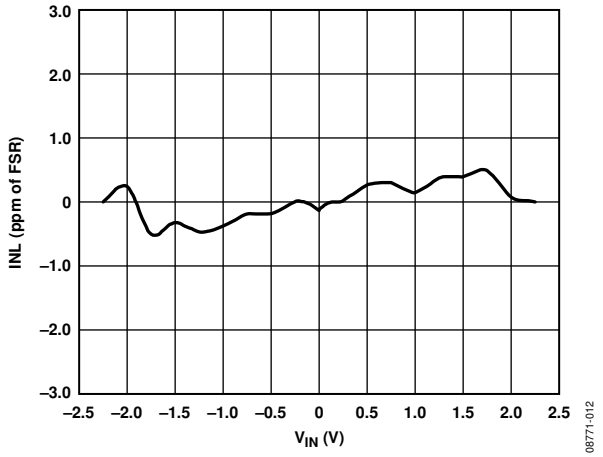

Figure 12. INL (Gain = 1)

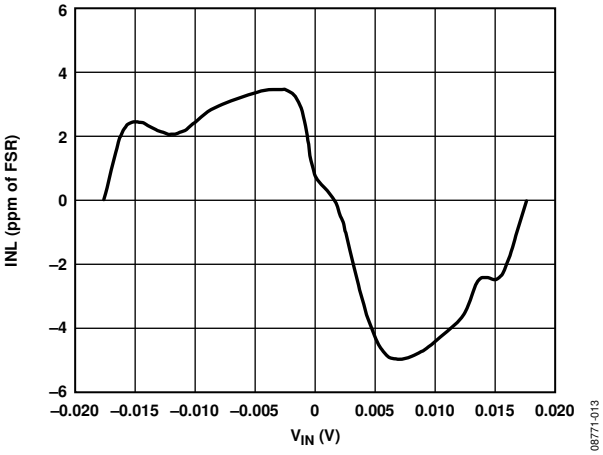

Figure 13. INL (Gain = 128)

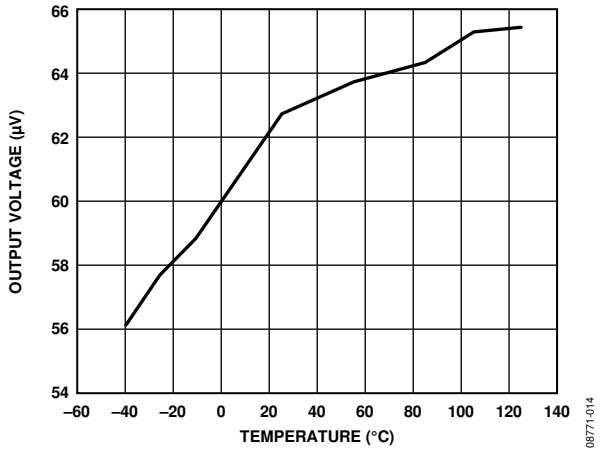

Figure 14. Offset Error (Gain = 1, Chop Disabled)

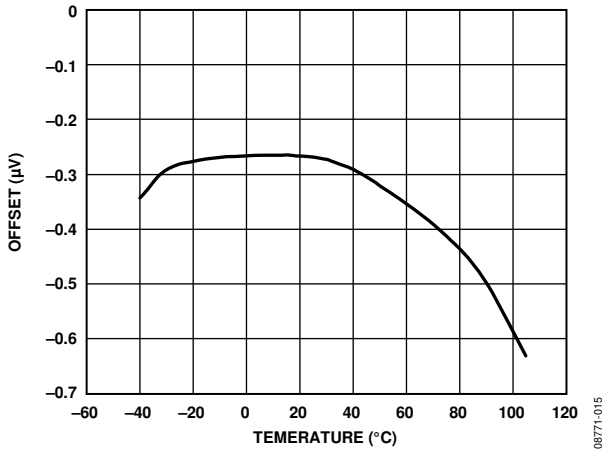

Figure 15. Offset Error (Gain = 128, Chop Disabled)

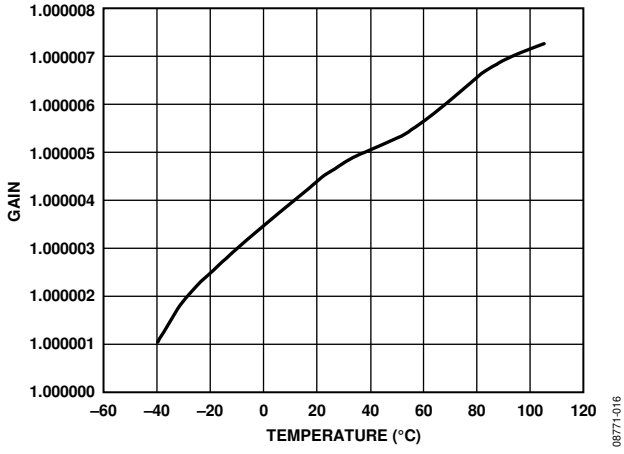

Figure 16. Gain Error (Gain = 1, Chop Disabled)

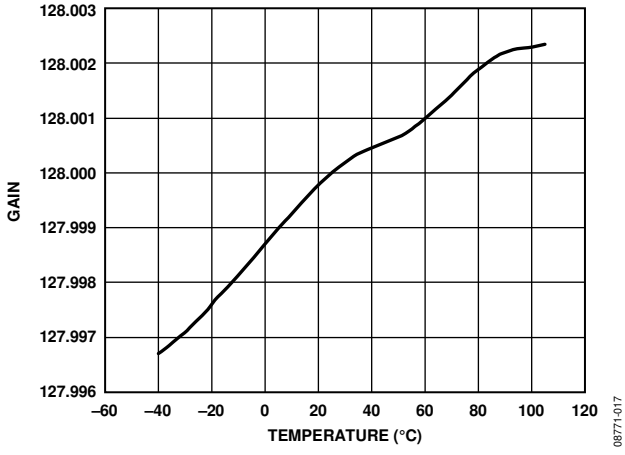

Figure 17. Gain Error (Gain = 128, Chop Disabled)

RMS NOISE AND RESOLUTION

The tables in this section show the rms noise, peak-to-peak noise, effective resolution, and noise-free (peak-to-peak) resolution of the AD7195 for various output data rates and gain settings, with chop disabled and chop enabled for the sinc[4] and sinc[3] filters. The numbers given are for the bipolar input range with the external 5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V when the ADC is continuously converting on a single channel. It is important to note that the effective resolution is calculated using the rms noise, whereas the peak-to-peak resolution is calculated based on peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no code flicker.

SINC[4] CHOP DISABLED

Table 6. RMS Noise (nV) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	4.7	852.5	280	96	50	22	10	8.5
640	7.5	533	390	120	54	28	12	10.5
480	10	400	470	130	56	31	14	11.5
96	50	80	1000	150	78	45	33	28
80	60	66.7	1100	170	88	52	36	31
32	150	26.7	1460	220	125	75	55	48
16	300	13.3	1900	285	170	100	75	67
5	960	4.17	3000	480	280	175	140	121
2	2400	1.67	5000	780	440	280	220	198
1	4800	0.83	14,300	1920	1000	550	380	295

Table 7. Peak-to-Peak Noise (nV) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	4.7	852.5	1600	500	250	130	65	56
640	7.5	533	2200	650	290	150	80	65
480	10	400	3000	670	300	190	100	70
96	50	80	6000	900	450	280	180	170
80	60	66.7	7200	1100	480	300	220	190
32	150	26.7	8300	1500	750	410	340	310
16	300	13.3	11,000	1700	1000	600	440	430
5	960	4.17	20,000	3000	1800	1100	810	710
2	2400	1.67	32,000	5100	2800	1700	1400	1200
1	4800	0.83	86,000	13,000	6000	3500	2400	1900

Table 8. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1[1]	Gain of 8[1]	Gain of 16[1]	Gain of 32[1]	Gain of 64[1]	Gain of 128[1]
1023	4.7	852.5	24 (22.6)	23.6 (21.3)	23.6 (21.3)	23.6 (21.2)	23.6 (21.2)	23.1 (20.4)
640	7.5	533	24 (22.1)	23.4 (20.9)	23.4 (20.9)	23.4 (20.9)	23.4 (20.9)	22.8 (20.2)
480	10	400	24 (21.7)	23.3 (20.8)	23.3 (20.8)	23.3 (20.8)	23.3 (20.6)	22.7 (20.1)
96	50	80	23.3 (20.7)	23 (20.4)	22.9 (20.4)	22.7 (20.1)	22.2 (19.7)	21.4 (18.8)
80	60	66.7	23.1 (20.4)	22.8 (20.1)	22.8 (20)	22.5 (20)	22.1 (19.4)	21.3 (18.6)
32	150	26.7	22.7 (20.2)	22.4 (19.7)	22.3 (19.7)	22 (19.5)	21.5 (18.8)	20.6 (17.9)
16	300	13.3	22.3 (19.8)	22.1 (19.5)	21.8 (19.3)	21.6 (19)	21 (18.4)	20.1 (17.5)
5	960	4.17	21.7 (18.9)	21.3 (18.7)	21.1 (18.4)	20.8 (18.1)	20.2 (17.6)	19.3 (16.7)
2	2400	1.67	20.9 (18.3)	20.6 (17.9)	20.4 (17.7)	20.1 (17.5)	19.5 (16.8)	18.6 (16)
1	4800	0.83	19.4 (16.8)	19.3 (16.6)	19.3 (16.4)	19.1 (16.4)	18.8 (16)	18 (15.3)

[1] The output peak-to-peak (p-p) resolution is listed in parentheses.

SINC³ CHOP DISABLED

Table 9. RMS Noise (nV) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	4.7	639.4	290	125	53	24	10.5	9
640	7.5	400	470	135	56	29	13	11.5
480	10	300	610	145	58	32	16	12.5
96	50	60	1100	160	86	50	35	29
80	60	50	1200	170	95	55	40	32
32	150	20	1500	230	130	80	58	50
16	300	10	1950	308	175	110	83	73
5	960	3.13	4000	590	330	200	150	133
2	2400	1.25	56,600	7000	3500	1800	900	490
1	4800	0.625	442,000	55,000	28,000	14,000	7000	3450

Table 10. Peak-to-Peak Noise (nV) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	4.7	639.4	1700	750	260	140	65	56
640	7.5	400	2400	800	340	150	84	60
480	10	300	3000	900	360	200	100	70
96	50	60	6600	1000	480	290	200	180
80	60	50	6800	1100	600	300	240	200
32	150	20	8900	1400	710	470	360	310
16	300	10	13,000	2000	1000	670	470	500
5	960	3.13	25,000	3400	2200	1200	850	800
2	2400	1.25	310,000	41,000	22,000	12,000	5600	3100
1	4800	0.625	2,600,000	300,000	170,000	79,000	41,000	24,000

Table 11. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1[1]	Gain of 8[1]	Gain of 16[1]	Gain of 32[1]	Gain of 64[1]	Gain of 128[1]
1023	4.7	639.4	24 (22.5)	23.5 (21)	23.5 (21)	23.5 (21)	23.5 (21)	23 (20.4)
640	7.5	400	24 (22)	23.3 (20.8)	23.3 (20.8)	23.3 (20.8)	23.3 (20.8)	22.7 (20.3)
480	10	300	24 (22)	23.2 (20.5)	23.2 (20.5)	23.2 (20.5)	23.2 (20.5)	22.6 (20.1)
96	50	60	23.1 (20.5)	22.9 (20.3)	22.8 (20.3)	22.6 (20)	22.1 (19.6)	21.4 (18.7)
80	60	50	23 (20.5)	22.8 (20.1)	22.6 (20)	22.4 (20)	21.9 (19.3)	21.2 (18.6)
32	150	20	22.7 (20)	22.4 (19.8)	22.2 (19.7)	21.9 (19.3)	21.4 (18.7)	20.6 (17.9)
16	300	10	22.3 (19.5)	22 (19.3)	21.8 (19.3)	21.4 (18.8)	20.8 (18.3)	20 (17.3)
5	960	3.13	21.3 (18.5)	21 (18.5)	20.9 (18.1)	20.6 (18)	20 (17.5)	19.2 (16.6)
2	2400	1.25	17.4 (14.9)	17.4 (14.9)	17.4 (14.8)	17.4 (14.7)	17.4 (14.7)	17.3 (14.6)
1	4800	0.625	14.5 (11.9)	14.5 (11.9)	14.4 (11.8)	14.4 (11.8)	14.4 (11.8)	14.4 (11.7)

[1] The output peak-to-peak (p-p) resolution is listed in parentheses.

SINC^4 CHOP ENABLED

Table 12. RMS Noise (nV) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	1.175	1702	198	85	41	18	7	6
640	1.875	1067	276	92	45	22	8.5	7
480	2.5	800	332	99	46	23	10	8
96	12.5	160	707	127	61	34	23	18
80	15	133	778	141	62	35	24	21
32	37.5	53.3	990	156	85	51	38	33
16	75	26.7	1344	191	106	67	51	45
5	240	8.33	2192	325	184	120	92	78
2	600	3.33	3606	523	297	191	148	134
1	1200	1.67	9900	1345	680	368	248	200

Table 13. Peak-to-Peak Noise (nV) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	1.175	1702	1131	474	212	92	46	40
640	1.875	1067	1556	495	248	106	57	46
480	2.5	800	2121	530	255	134	71	50
96	12.5	160	4243	707	368	198	127	120
80	15	133	5091	849	424	212	156	134
32	37.5	53.3	5870	1061	530	290	240	219
16	75	26.7	7780	1202	707	424	311	304
5	240	8.33	14,142	2121	1273	778	573	502
2	600	3.33	22,627	3606	1980	1202	990	850
1	1200	1.67	60,800	9192	4950	2475	1697	1345

Table 14. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1[1]	Gain of 8[1]	Gain of 16[1]	Gain of 32[1]	Gain of 64[1]	Gain of 128[1]
1023	1.175	1702	24 (23.1)	24 (21.8)	24 (21.8)	24 (21.7)	24 (21.7)	23.6 (20.9)
640	1.875	1067	24 (22.6)	23.9 (21.4)	23.9 (21.4)	23.9 (21.4)	23.9 (21.4)	23.3 (20.7)
480	2.5	800	24 (22.2)	23.8 (21.3)	23.8 (21.3)	23.8 (21.3)	23.8 (21.1)	23.2 (20.6)
96	12.5	160	23.8 (21.2)	23.5 (20.9)	23.4 (20.9)	23.2 (20.6)	22.7 (20.2)	21.9 (19.3)
80	15	133	23.6 (20.9)	23.3 (20.6)	23.3 (20.5)	23 (20.5)	22.6 (19.9)	21.8 (19.1)
32	37.5	53.3	23.2 (20.7)	22.9 (20.2)	22.8 (20.2)	22.5 (20)	22 (19.3)	21.1 (18.4)
16	75	26.7	22.8 (20.3)	22.6 (20)	22.3 (19.8)	22.1 (19.5)	21.5 (18.9)	20.6 (18)
5	240	8.33	22.2 (19.4)	21.8 (19.2)	21.6 (18.9)	21.3 (18.6)	20.7 (18.1)	19.8 (17.2)
2	600	3.33	21.4 (18.8)	21.1 (18.4)	20.9 (18.2)	20.6 (18)	20 (17.3)	19.1 (16.5)
1	1200	1.67	19.9 (17.3)	19.8 (17.1)	19.8 (16.9)	19.6 (16.9)	19.3 (16.5)	18.5 (15.8)

[1] The output peak-to-peak (p-p) resolution is listed in parentheses.

When ac excitation is enabled, the rms noise and resolution is the same as for chop enabled mode.

SINC³ CHOP ENABLED

Table 15. RMS Noise (nV) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	1.56	1282	205	88	37	17	7.5	6.5
640	2.5	800	332	95	40	21	9	8
480	3.33	600	431	103	41	23	11.5	9
96	16.6	120	778	113	61	35	25	21
80	20	100	849	120	67	39	28	23
32	50	40	1061	163	92	57	41	35
16	100	20	1379	218	124	78	59	52
5	320	6.25	2828	417	233	141	106	94
2	800	2.5	40,022	4950	2475	1273	636	346
1	1600	1.25	312,540	38,890	19,800	9900	4950	2440

Table 16. Peak-to-Peak Noise (nV) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	1.56	1282	1202	530	184	92	46	40
640	2.5	800	1697	566	240	120	59	42
480	3.33	600	2121	636	255	141	71	49
96	16.6	120	4667	686	318	198	141	127
80	20	100	4808	707	424	205	170	141
32	50	40	6293	990	474	382	255	219
16	100	20	9192	1414	707	474	332	354
5	320	6.25	17,680	2404	1556	849	601	566
2	800	2.5	219,200	29,000	15,560	8485	3960	2192
1	1600	1.25	1,838,500	212,200	120,200	55,870	29,000	16,970

Table 17. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1[1]	Gain of 8[1]	Gain of 16[1]	Gain of 32[1]	Gain of 64[1]	Gain of 128[1]
1023	1.56	1282	24 (23)	24 (21.5)	24 (21.5)	24 (21.5)	24 (21.5)	23.5 (20.9)
640	2.5	800	24 (22.5)	23.8 (21.3)	23.8 (21.3)	23.8 (21.3)	23.8 (21.3)	23.2 (20.8)
480	3.33	600	24 (22.5)	23.7 (21)	23.7 (21)	23.7 (21)	23.7 (21)	23.1 (20.6)
96	16.6	120	23.6 (21)	23.4 (20.8)	23.3 (20.8)	23.1 (20.5)	22.6 (20.1)	21.9 (19.2)
80	20	100	23.5 (21)	23.3 (20.6)	23.1 (20.5)	22.9 (20.5)	22.4 (19.8)	21.7 (19.1)
32	320	40	23.2 (20.5)	22.9 (20.3)	22.7 (20.2)	22.4 (19.8)	21.9 (19.2)	21.1 (18.4)
16	100	20	22.8 (20)	22.5 (19.8)	22.3 (19.8)	21.9 (19.3)	21.3 (18.8)	20.5 (17.8)
5	320	6.25	21.8 (19)	21.5 (19)	21.4 (18.6)	21.1 (18.5)	20.5 (18)	19.7 (17.1)
2	800	2.5	17.9 (15.4)	17.9 (15.4)	17.9 (15.3)	17.9 (15.2)	17.9 (15.2)	17.8 (15.1)
1	1600	1.25	15 (12.4)	15 (12.4)	14.9 (12.3)	14.9 (12.3)	14.9 (12.3)	14.9 (12.2)

[1] The output peak-to-peak (p-p) resolution is listed in parentheses.

When ac excitation is enabled, the rms noise and resolution is the same as for chop enabled mode.

ON-CHIP REGISTERS

The ADC is controlled and configured via a number of on-chip registers described on the following pages. In the following descriptions, the term set implies a Logic 1 state and cleared implies a Logic 0 state, unless otherwise noted.

Table 18. Register Summary

Register	Addr.	Dir.	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Communications	00	W	00	$\overline{WEN}$	R/$\overline{W}$	Register address			CREAD	0	0
Status	00	R	80	$\overline{RDY}$	ERR	NOREF	PARITY	0	CHD2	CHD1	CHD0
Mode	01	R/W	080060	Mode select			DAT_STA	CLK1	CLK0	0	0
				SINC3	0	ENPAR	0	SINGLE	REJ60	FS9	FS8
				FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0 (LSB)
Configuration	02	R/W	000117	Chop (MSB)	ACX	0	0	0	0	0	0
				CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
				BURN	REFDET	0	BUF	U/$\overline{B}$	G2	G1	G0 (LSB)
Data	03	R	000000	D23 (MSB)	D22	D21	D20	D19	D18	D17	D16
				D15	D14	D13	D12	D11	D10	D9	D8
				D7	D6	D5	D4	D3	D2	D1	D0 (LSB)
ID	04	R	A6	1	0	1	0	0	1	1	0
GPOCON	05	R/W	00	0	BPDSW	0	0	0	0	0	0
Offset	06	R/W	800000	OF23 (MSB)	OF22	OF21	OF20	OF19	OF18	OF17	OF16
				OF15	OF14	OF13	OF12	OF11	OF10	OF9	OF8
				OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0 (LSB)
Full Scale	07	R/W	5XXXX0	FS23 (MSB)	FS22	FS21	FS20	FS19	FS18	FS17	FS16
				FS15	FS14	FS13	FS12	FS11	FS10	FS9	FS8
				FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0 (LSB)

COMMUNICATIONS REGISTER

(RS2, RS1, RS0 = 0, 0, 0)

The communications register is an 8-bit write-only register. All communications to the part must start with a write operation to the communications register. The data written to the communications register determines whether the next operation is a read or a write operation and in which register this operation takes place. For read or write operations, when the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the communications register. This is the default state of the interface and, on power-up or after a reset, the ADC is in this default state waiting for a write operation to the communications register. In situations where the interface sequence is lost, a write operation of at least 40 serial clock cycles with DIN high returns the ADC to this default state by resetting the entire part. Table 19 outlines the bit designations for the communications register. CR0 through CR7 indicate the bit location, CR denoting that the bits are in the communications register. CR7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}$(0)	R/$\overline{\text{W}}$(0)	RS2(0)	RS1(0)	RS0(0)	CREAD(0)	0	0

Table 19. Communications Register Bit Designations

Bit Location	Bit Name	Description
CR7	$\overline{\text{WEN}}$	Write enable bit. For a write to the communications register to occur, 0 must be written to this bit. If a 1 is the first bit written, the part does not clock on to subsequent bits in the register; rather, it stays at this bit location until a 0 is written to this bit. After a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits are loaded to the communications register. Idling the DIN pin high between data transfers minimizes the effects of spurious SCLK pulses on the serial interface.
CR6	R/$\overline{\text{W}}$	A 0 in this bit location indicates that the next operation is a write to a specified register. A 1 in this position indicates that the next operation is a read from the designated register.
CR5 to CR3	RS2 to RS0	Register address bits. These address bits are used to select which registers of the ADC are selected during the serial interface communication (see Table 20).
CR2	CREAD	Continuous read of the data register. When this bit is set to 1 (and the data register is selected), the serial interface is configured so that the data register can be continuously read; that is, the contents of the data register are automatically placed on the DOUT pin when the SCLK pulses are applied after the $\overline{\text{RDY}}$ pin goes low to indicate that a conversion is complete. The communications register does not have to be written to for subsequent data reads. To enable continuous read, the Instruction 01011100 must be written to the communications register. To disable continuous read, the Instruction 01011000 must be written to the communications register while the $\overline{\text{RDY}}$ pin is low. While continuous read is enabled, the ADC monitors activity on the DIN line so that it can receive the instruction to disable continuous read. Additionally, a reset occurs if 40 consecutive 1s are seen on DIN. Therefore, hold DIN low until an instruction is written to the device.
CR1 to CR0	0	These bits must be programmed to Logic 0 for correct operation.

Table 20. Register Selection

RS2	RS1	RS0	Register	Register Size
0	0	0	Communications register during a write operation	8 bits
0	0	0	Status register during a read operation	8 bits
0	0	1	Mode register	24 bits
0	1	0	Configuration register	24 bits
0	1	1	Data register/data register plus status information	24 bits/32 bits
1	0	0	ID register	8 bits
1	0	1	GPOCON register	8 bits
1	1	0	Offset register	24 bits
1	1	1	Full-scale register	24 bits

STATUS REGISTER

(RS2, RS1, RS0 = 0, 0, 0; Power-On/Reset = 0x80)

The status register is an 8-bit read-only register. To access the ADC status register, the user must write to the communications register, select the next operation to be a read, and load Bit RS2, Bit RS1, and Bit RS0 with 0. Table 21 outlines the bit designations for the status register. SR0 through SR7 indicate the bit locations, SR denoting that the bits are in the status register. SR7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

SR7	**SR6**	**SR5**	**SR4**	**SR3**	**SR2**	**SR1**	**SR0**
$\overline{\text{RDY}}$(1)	ERR(0)	NOREF(0)	PARITY(0)	0	CHD2(0)	CHD1(0)	CHD0(0)

Table 21. Status Register Bit Designations

Bit Location	Bit Name	Description
SR7	$\overline{\text{RDY}}$	Ready bit for the ADC. This bit is cleared when data is written to the ADC data register. The $\overline{\text{RDY}}$ bit is set automatically after the ADC data register is read, or a period of time before the data register is updated, with a new conversion result to indicate to the user that the conversion data should not be read. It is also set when the part is placed in power-down mode or idle mode or when $\overline{\text{SYNC}}$ is taken low. The end of a conversion is also indicated by the DOUT/$\overline{\text{RDY}}$ pin. This pin can be used as an alternative to the status register for monitoring the ADC for conversion data.
SR6	ERR	ADC error bit. This bit is written to at the same time as the $\overline{\text{RDY}}$ bit. This bit is set to indicate that the result written to the ADC data register is clamped to all 0s or all 1s. Error sources include overrange or under-range, or the absence of a reference voltage. This bit is cleared when the result written to the data register is within the allowed analog input range again.
SR5	NOREF	No external reference bit. This bit is set to indicate that the reference is at a voltage that is below a specified threshold. When set, conversion results are clamped to all 1s. This bit is cleared to indicate that a valid reference is applied to the selected reference pins. The NOREF bit is enabled by setting the REFDET bit in the configuration register to 1.
SR4	PARITY	Parity check of the data register. If the ENPAR bit in the mode register is set, the PARITY bit is set if there is an odd number of 1s in the data register. It is cleared if there is an even number of 1s in the data register. The DAT_STA bit in the mode register should be set when the parity check is used. When the DAT_STA bit is set, the contents of the status register are transmitted along with the data for each data register read.
SR3	0	This bit is set to 0.
SR2 to SR0	CHD2 to CHD0	These bits indicate which channel corresponds to the data register contents. They do not indicate which channel is presently being converted but indicate which channel was selected when the conversion contained in the data register was generated.

MODE REGISTER

(RS2, RS1, RS0 = 0, 0, 1; Power-On/Reset = 0x080060)

The mode register is a 24-bit register from which data can be read or to which data can be written. This register is used to select the operating mode, the output data rate, and the clock source. Table 22 outlines the bit designations for the mode register. MR0 through MR23 indicate the bit locations, MR denoting that the bits are in the mode register. MR23 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit. Any write to the mode register resets the modulator and filter and sets the $\overline{\text{RDY}}$ bit.

MR23	**MR22**	**MR21**	**MR20**	**MR19**	**MR18**	**MR17**	**MR16**
MD2(0)	MD1(0)	MD0(0)	DAT_STA(0)	CLK1(1)	CLK0(0)	0	0
MR15	**MR14**	**MR13**	**MR12**	**MR11**	**MR10**	**MR9**	**MR8**
SINC3(0)	0	ENPAR(0)	0	SINGLE(0)	REJ60(0)	FS9(0)	FS8(0)
MR7	**MR6**	**MR5**	**MR4**	**MR3**	**MR2**	**MR1**	**MR0**
FS7(0)	FS6(1)	FS5(1)	FS4(0)	FS3(0)	FS2(0)	FS1(0)	FS0(0)

Table 22. Mode Register Bit Designations

Bit Location	Bit Name	Description		
MR23 to MR21	MD2 to MD0	Mode select bits. These bits select the operating mode of the AD7195 (see Table 23).		
MR20	DAT_STA	This bit enables the transmission of status register contents after each data register read. When DAT_STA is set, the contents of the status register are transmitted along with each data register read. This function is useful when several channels are selected because the status register identifies the channel to which the data register value corresponds.		
MR19, MR18	CLK1, CLK0	These bits select the clock source for the AD7195. Either the on-chip 4.92 MHz clock or an external clock can be used. The ability to use an external clock allows several AD7195 devices to be synchronized. Also, 50 Hz/60 Hz rejection is improved when an accurate external clock drives the AD7195.		
		CLK1	**CLK0**	**ADC Clock Source**
		0	0	External crystal. The external crystal is connected from MCLK1 to MCLK2.
		0	1	External clock. The external clock is applied to the MCLK2 pin.
		1	0	Internal 4.92 MHz clock. Pin MCLK2 is tristated.
		1	1	Internal 4.92 MHz clock. The internal clock is available on MCLK2.
MR17, MR16	0	These bits must be programmed with a Logic 0 for correct operation.		
MR15	SINC3	Sinc^3 filter select bit. When this bit is cleared, the sinc^4 filter is used (default value). When this bit is set, the sinc^3 filter is used. The benefit of the sinc^3 filter compared to the sinc^4 filter is its lower settling time. For a given output data rate, f_{ADC}, the sinc^3 filter has a settling time of $3/f_{ADC}$ while the sinc^4 filter has a settling time of $4/f_{ADC}$ when chop is disabled. The sinc^4 filter, due to its deeper notches, gives better 50 Hz/60 Hz rejection. At low output data rates, both filters give similar rms noise and similar no missing codes for a given output data rate. At higher output data rates (FS values less than 5), the sinc^4 filter gives better performance than the sinc^3 filter for rms noise and no missing codes.		
MR14	0	This bit must be programmed with a Logic 0 for correct operation.		
MR13	ENPAR	Enable parity bit. When ENPAR is set, parity checking on the data register is enabled. The DAT_STA bit in the mode register should be set when the parity check is used. When the DAT_STA bit is set, the contents of the status register are transmitted along with the data for each data register read.		
MR12	0	This bit must be programmed with a Logic 0 for correct operation.		
MR11	SINGLE	Single cycle conversion enable bit. When this bit is set, the AD7195 settles in one conversion cycle so that it functions as a zero-latency ADC. This bit has no effect when multiple analog input channels are enabled or when the single conversion mode is selected.		
MR10	REJ60	This bit enables a notch at 60 Hz when the first notch of the sinc filter is at 50 Hz. When REJ60 is set, a filter notch is placed at 60 Hz when the sinc filter first notch is at 50 Hz. This allows simultaneous 50 Hz/60 Hz rejection.		
MR9 to MR0	FS9 to FS0	Filter output data rate select bits. The 10 bits of data programmed into these bits determine the filter cut-off frequency, the position of the first notch of the filter, and the output data rate for the part. In association with the gain selection, they also determine the output noise (and, therefore, the effective resolution) of the device (see Table 6 through Table 17). When chop is disabled and continuous conversion mode is selected, *Output Data Rate* = (*MCLK*/1024)/*FS* where *FS* is the decimal equivalent of the code in Bit FS0 to Bit FS9 and is in the range 1 to 1023, and *MCLK* is the master clock frequency. With a nominal MCLK of 4.92 MHz, this results in an output data rate from 4.69 Hz to 4.8 kHz. With chop disabled, the first notch frequency is equal to the output data rate when converting on a single channel. When chop is enabled, *Output Data Rate* = (*MCLK*/1024)/(*N* × *FS*) where *FS* is the decimal equivalent of the code in Bit FS0 to Bit FS9 and is in the range 1 to 1023, and *MCLK* is the master clock frequency. With a nominal MCLK of 4.92 MHz, this results in a conversion rate from 4.69/N Hz to 4.8/N kHz, where N is the order of the sinc filter. The sinc filter's first notch frequency is equal to N × output data rate. The chopping introduces notches at odd integer multiples of (output data rate/2).		

Table 23. Operating Modes

MD2	MD1	MD0	Mode
0	0	0	Continuous conversion mode (default). In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register. The DOUT/RDY pin and the RDY bit in the status register go low when a conversion is complete. The user can read these conversions by setting the CREAD bit in the communications register to 1, which enables continuous read. When continuous read is enabled, the conversions are automatically placed on the DOUT line when SCLK pulses are applied. Alternatively, the user can instruct the ADC to output each conversion by writing to the communications register. After power-on, a reset, or a reconfiguration of the ADC, the complete settling time of the filter is required to generate the first valid conversion. Subsequent conversions are available at the selected output data rate, which is dependent on filter choice.
0	0	1	Single conversion mode. When single conversion mode is selected, the ADC powers up and performs a single conversion on the selected channel. The internal clock requires up to 1 ms to power up and settle. The ADC then performs the conversion, which requires the complete settling time of the filter. The conversion result is placed in the data register. RDY goes low, and the ADC returns to power-down mode. The conversion remains in the data register until another conversion is performed. RDY remains active (low) until the data is read or another conversion is performed.
0	1	0	Idle mode. In idle mode, the ADC filter and modulator are held in a reset state even though the modulator clocks are still provided.
0	1	1	Power-down mode. In power-down mode, all AD7195 circuitry, except the bridge power-down switch, is powered down. The bridge power-down switch remains active because the user may need to power up the sensor prior to powering up the AD7195 for settling reasons. The external crystal, if selected, remains active.
1	0	0	Internal zero-scale calibration. An internal short is automatically connected to the input. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel.
1	0	1	Internal full-scale calibration. A full-scale input voltage is automatically connected to the input for this calibration. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. A full-scale calibration is required each time the gain of a channel is changed to minimize the full-scale error.
1	1	0	System zero-scale calibration. The user should connect the system zero-scale input to the channel input pins as selected by the CH7 to CH0 bits in the configuration register. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel. A system zero-scale calibration is required each time the gain of a channel is changed.
1	1	1	System full-scale calibration. The user should connect the system full-scale input to the channel input pins as selected by the CH7 to CH0 bits in the configuration register. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. A full-scale calibration is required each time the gain of a channel is changed.

CONFIGURATION REGISTER

(RS2, RS1, RS0 = 0, 1, 0; Power-On/Reset = 0x000117)

The configuration register is a 24-bit register from which data can be read or to which data can be written. This register is used to configure the ADC for unipolar or bipolar mode, to enable or disable the buffer, to enable or disable the burnout currents, to select the gain, and to select the analog input channel. Table 24 outlines the bit designations for the filter register. CON0 through CON23 indicate the bit locations. CON denotes that the bits are in the configuration register. CON23 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

CON23	**CON22**	**CON21**	**CON20**	**CON19**	**CON18**	**CON17**	**CON16**
CHOP(0)	ACX(0)	0	0	0	0	0	0
CON15	**CON14**	**CON13**	**CON12**	**CON11**	**CON10**	**CON9**	**CON8**
CH7(0)	CH6(0)	CH5(0)	CH4(0)	CH3(0)	CH2(0)	CH1(0)	CH0(1)
CON7	**CON6**	**CON5**	**CON4**	**CON3**	**CON2**	**CON1**	**CON0**
BURN(0)	REFDET(0)	0	BUF(1)	U/$\overline{B}$ (0)	G2(1)	G1(1)	G0(1)

Table 24. Configuration Register Bit Designations

Bit Location	Bit Name	Description				
CON23	CHOP	Chop enable bit. When the CHOP bit is cleared, chop is disabled. When the CHOP bit is set, chop is enabled. When chop is enabled, the offset and offset drift of the ADC are continuously removed. However, this increases the conversion time and settling time of the ADC. For example, when FS = 96 decimal and the sinc^4 filter is selected, the conversion time with chop enabled equals 80 ms and the settling time equals 160 ms. With chop disabled, higher conversion rates are allowed. For an FS word of 96 decimal and the sinc^4 filter selected, the conversion time is 20 ms and the settling time is 80 ms. However, at low gains, periodic calibrations may be required to remove the offset and offset drift. When ax excitation is enabled, chop must be enabled also.				
CON22	ACX	AC excitation enable bit. If the signal source to the AD7195 is ac excited, this bit must be set to 1. For dc-excited inputs, this bit must be 0. With the ACX bit at 1, the AD7195 assumes that the voltage at the AIN(+)/AIN(–) and REFIN(+)/REFIN(–) input terminals are reversed on alternate input sampling cycles (that is, chopped). Note that when the AD7195 is performing internal zero-scale or full-scale calibrations, the ACX bit is treated as a 0, that is, the device performs these self-calibrations with dc excitation. TheBitCHOP must be set to 1 when ac excitation is enabled.				
CON21 to CON16	0	These bits must be programmed with a Logic 0 for correct operation.				
CON15 to CON8	CH7 to CH0	Channel select bits. These bits are used to select which channels are enabled on the AD7195 (see Table 25). Several channels can be selected, and the AD7195 automatically sequences them. The conversion on each channel requires the complete settling time. When performing calibrations or when accessing the calibration registers, only one channel can be selected.				
CON7	BURN	When this bit is set to 1, the 500 nA current sources in the signal path are enabled. When BURN = 0, the burnout currents are disabled. The burnout currents can be enabled only when the buffer is active and when chop is disabled.				
CON6	REFDET	Enables the reference detect function. When set, the NOREF bit in the status register indicates when the external reference being used by the ADC is open circuit or less than 0.6 V maximum. The reference detect circuitry operates only when the ADC is active.				
CON5	0	This bit must be programmed with a Logic 0 for correct operation.				
CON4	BUF	Enables the buffer on the analog inputs. If cleared, the analog inputs are unbuffered, lowering the power consumption of the device. If this bit is set, the analog inputs are buffered, allowing the user to place source impedances on the front end without contributing gain errors to the system. With the buffer disabled, the voltage on the analog input pins can be from 50 mV below AGND to 50 mV above AV_{DD}. When the buffer is enabled, it requires some headroom; therefore, the voltage on any input pin must be limited to 250 mV within the power supply rails.				
CON3	U/$\overline{B}$	Polarity select bit. When this bit is set, unipolar operation is selected. When this bit is cleared, bipolar operation is selected.				
CON2 to CON0	G2 to G0	Gain select bits. These bits are written by the user to select the ADC input range as follows:				
		G2	**G1**	**G0**	**Gain**	**ADC Input Range (5 V Reference)**
		0	0	0	1	±5 V
		0	0	1	Reserved	
		0	1	0	Reserved	
		0	1	1	8	±625 mV
		1	0	0	16	±312.5 mV
		1	0	1	32	±156.2 mV
		1	1	0	64	±78.125 mV
		1	1	1	128	±39.06 mV

Table 25. Channel Selection

Channel Enable Bits in the Configuration Register								Channel Enabled			
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0	Positive Input AIN(+)	Negative Input AIN(−)	Status Register Bits CHD[2:0]	Calibration Register Pair
							1	AIN1	AIN2	000	0
						1		AIN3	AIN4	001	1
					1			Temperature sensor		010	None
				1				AIN2	AIN2	011	0
			1					AIN1	AINCOM	100	0
		1						AIN2	AINCOM	101	1
	1							AIN3	AINCOM	110	2
1								AIN4	AINCOM	111	3

DATA REGISTER

(RS2, RS1, RS0 = 0, 1, 1; Power-On/Reset = 0x000000)

The conversion result from the ADC is stored in this data register. This is a read-only, 24-bit register. On completion of a read operation from this register, the $\overline{RDY}$ pin/bit is set. When the DAT_STA bit in the mode register is set to 1, the contents of the status register are appended to each 24-bit conversion. This is advisable when several analog input channels are enabled because the three LSBs of the status register (CHD2 to CHD0) identify the channel from which the conversion originated.

ID REGISTER

(RS2, RS1, RS0 = 1, 0, 0; Power-On/Reset = 0xA6)

The identification number for the AD7195 is stored in the ID register. This is a read-only register.

GPOCON REGISTER

(RS2, RS1, RS0 = 1, 0, 1; Power-On/Reset = 0x00)

The GPOCON register is an 8-bit register from which data can be read or to which data can be written. This register is used to enable the general-purpose digital outputs.

Table 26 outlines the bit designations for the GPOCON register. GP0 through GP7 indicate the bit locations. GP denotes that the bits are in the GPOCON register. GP7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
0	BPDSW(0)	0	0	0	0	0	0

Table 26. Register Bit Designations

Bit Location	Bit Name	Description
GP7	0	This bit must be programmed with a Logic 0 for correct operation.
GP 6	BPDSW	Bridge power-down switch control bit. This bit is set by the user to close the bridge power-down switch BPDSW to AGND. The switch can sink up to 30 mA. The bit is cleared by the user to open the bridge power-down switch. When the ADC is placed in power-down mode, the bridge power-down switch remains active.
GP5 to GP0	0	These bits must be programmed with a Logic 0 for correct operation.

OFFSET REGISTER

(RS2, RS1, RS0 = 1, 1, 0; Power-On/Reset = 0x800000)

The offset register holds the offset calibration coefficient for the ADC. The power-on reset value of the offset register is 0x800000. The AD7195 has four offset registers; therefore, each channel has a dedicated offset register (see Table 25). Each of these registers is a 24-bit read/write register. This register is used in conjunction with its associated full-scale register to form a register pair. The power-on reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user. The AD7195 must be placed in power-down mode or idle mode when writing to the offset register.

FULL-SCALE REGISTER

(RS2, RS1, RS0 = 1, 1, 1; Power-On/Reset = 0x5XXXX0)

The full-scale register is a 24-bit register that holds the full-scale calibration coefficient for the ADC. The AD7195 has four full-scale registers; therefore, each channel has a dedicated full-scale register (see Table 25). The full-scale registers are read/write registers. However, when writing to the full-scale registers, the ADC must be placed in power-down mode or idle mode. These registers are configured at power-on with factory-calibrated full-scale calibration coefficients, the calibration being performed at gain = 1. Therefore, every device has different default coefficients. The default value is automatically overwritten if an internal or system full-scale calibration is initiated by the user or if the full-scale register is written to.