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Lithium Ion Battery Monitoring System

AD7280A

FEATURES

12-bit ADC, 1 µs per channel conversion time
6 analog input channels, common-mode range 0.5 V to 27.5 V
6 auxiliary ADC inputs
±1.6 mV cell voltage accuracy
On-chip voltage regulator
Cell balancing interface
Daisy-chain interface
Internal reference: ±3 ppm/°C
1.8 µA power-down current
High input impedance
Serial interface with alert function
1 SPI interface for up to 48 channels
CRC protection on read and write commands
On-chip registers for channel sequencing
V_{DD} operating range: 8 V to 30 V
Temperature range: −40°C to +105°C
48-lead LQFP
Qualified for automotive applications

APPLICATIONS

Lithium ion battery monitoring
Electric and hybrid electric vehicles
Power supply backup
Power tools

FUNCTIONAL BLOCK DIAGRAM

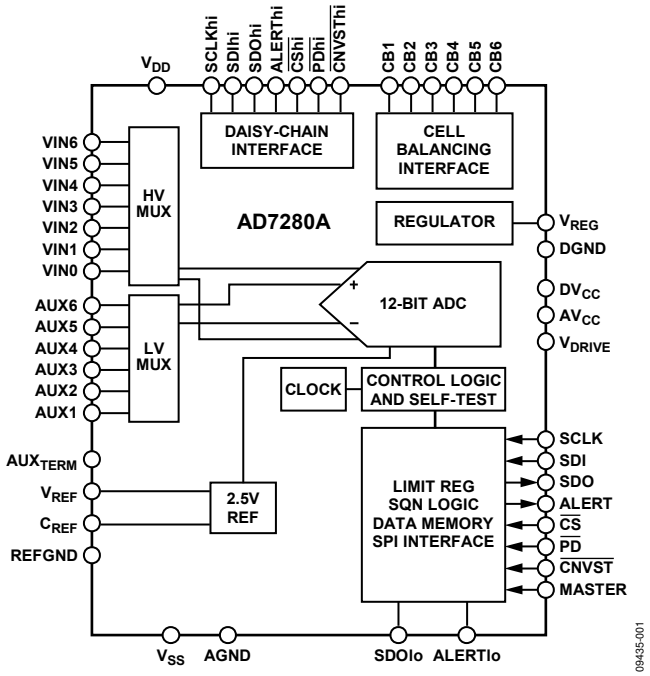

Figure 1.

GENERAL DESCRIPTION

The AD7280A[1] contains all the functions required for general-purpose monitoring of stacked lithium ion batteries as used in hybrid electric vehicles, battery backup applications, and power tools. The part has multiplexed cell voltage and auxiliary ADC measurement channels for up to six cells of battery management. An internal ±3 ppm/°C reference is provided that allows a cell voltage accuracy of ±1.6 mV. The ADC resolution is 12 bits and allows conversion of up to 48 cells within 7 µs.

The AD7280A operates from a single V_{DD} supply that has a range of 8 V to 30 V (with an absolute maximum rating of 33 V). The part provides six differential analog input channels to accommodate large common-mode signals across the full V_{DD} range. Each channel allows an input signal range, VIN(+) − VIN(−), of 1 V to 5 V. The input pins assume a series stack of six cells. In addition, the part includes six auxiliary ADC input channels that can be used for temperature measurement or system diagnostics.

The AD7280A includes on-chip registers that allow a sequence of channel measurements to be programmed to suit the application requirements.

The AD7280A also includes a dynamic alert function that can detect whether the cell voltages or auxiliary ADC inputs exceed an upper or lower limit defined by the user. The AD7280A has cell balancing interface outputs designed to control external FET transistors to allow discharging of individual cells.

The AD7280A includes a built-in self-test feature that internally applies a known voltage to the ADC inputs.

A daisy-chain interface allows up to eight parts to be stacked without the need for individual device isolation.

The AD7280A requires only one supply pin that accepts 6.9 mA under normal operation while converting at 1 MSPS.

All this functionality is provided in a 48-lead LQFP package operating over a temperature range of −40°C to +105°C.

[1] Patents pending.

Rev. 0

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Last Content Update: 02/23/2017

COMPARABLE PARTS

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EVALUATION KITS

- AD7280A Evaluation Board

DOCUMENTATION

Data Sheet

- AD7280A: Lithium Ion Battery Monitoring System Data Sheet

User Guides

- UG-252: Evaluation Board for the AD7280A Lithium Ion Battery Monitoring System

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD7280A IIO Lithium Ion Battery Monitoring System Linux Driver

REFERENCE DESIGNS

- CN0197
- CN0235

DESIGN RESOURCES

- AD7280A Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

4/11—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 8 V to 30 V, V_{SS} = 0 V, DV_{CC} = AV_{CC} = V_{REG}, V_{DRIVE} = 2.7 V to 5.5 V, T_A = −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC ACCURACY (VIN0 TO VIN6)[1]					
Resolution	12			Bits	No missing codes
Integral Nonlinearity		±1		LSB	
Differential Nonlinearity		±0.8		LSB	
Offset Error		±1		LSB	
Offset Error Match		1		LSB	
Gain Error		±1		LSB	
Gain Error Match		1		LSB	
ADC Unadjusted Error[2, 3]		±1.2		mV	
Total Unadjusted Error[4, 5]			±9	mV	V_{IN} range[6] = 1 V to 4.1 V, −10°C to +85°C
			±10	mV	V_{IN} range[6] = 1 V to 4.1 V, −40°C to +85°C
		±1.6	±14.5	mV	V_{IN} range[6] = 1 V to 4.1 V, −40°C to +105°C
CELL VOLTAGE INPUTS (VIN0 TO VIN6)					
Pseudo Differential Input Voltage					
VIN(x) − VIN(x − 1)	1		2 × V_{REF}	V	
Absolute Input Voltage	V_{CM} − V_{REF}		V_{CM} + V_{REF}	V	
Common-Mode Input Voltage	0.5		27.5	V	
Static Leakage Current[7]		±5	±70	nA	
Dynamic Leakage Current[7]			±3	nA	$\overline{\text{CNVST}}$ pulse every 100 ms
Input Capacitance		15		pF	
DC ACCURACY (AUX1 TO AUX6)[1, 8]					
Resolution	12			Bits	No missing codes
Integral Nonlinearity		±1		LSB	
Differential Nonlinearity		±0.8		LSB	
Offset Error		±2		LSB	
Offset Error Match		2		LSB	
Gain Error		±2		LSB	
Gain Error Match		2		LSB	
ADC Unadjusted Error[9]		±1.2		mV	
Total Unadjusted Error[10]			±20	mV	−40°C to +85°C
		±1.6	±22	mV	−40°C to +105°C
AUXILIARY ADC INPUTS (AUX1 TO AUX6)					
Input Voltage Range	0		2 × V_{REF}	V	
Static Leakage Current[7]		±15		nA	
Dynamic Leakage Current[7]			±3	nA	$\overline{\text{CNVST}}$ pulse every 100 ms
Input Capacitance		15		pF	
REFERENCE					
Reference Voltage	2.494	2.5	2.506	V	−40°C to +85°C
	2.494	2.5	2.509	V	−40°C to +105°C
Reference Voltage Temperature Coefficient		±3	±15	ppm/°C	−40°C to +85°C
		±11		ppm/°C	−40°C to +105°C
Output Voltage Hysteresis		50		ppm	−40°C to +105°C
Long-Term Drift		150		ppm/1000 hours	
Line Regulation		±5		ppm/V	
Turn-On Settling Time[11, 12]		5.5	10	ms	V_{REG} = 1 µF, V_{REF} = 1 µF, C_{REF} = 100 nF

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REGULATOR OUTPUT (V_{REG})					
Input Voltage Range	8		30	V	
Output Voltage, V_{REG}[13]	4.9	5.2	5.5	V	5 mA external load
Output Current[14]			5	mA	
Line Regulation		0.5		mV/V	
Load Regulation		2.5		mV/mA	
Internal Short Protection Limit		25		mA	For a 10 Ω short
CELL BALANCING OUTPUTS[15]					
Output High Voltage, V_{OH}	V_{REG} − 1	5	V_{REG} + 0.2	V	I_{SOURCE} = 415 nA
Output Low Voltage, V_{OL}	0			V	
CB1 Output Ramp-Up Time[16]		30		µs	For an 80 pF load
CB1 Output Ramp-Down Time[17]		30		µs	For an 80 pF load
CB2 to CB6 Output Ramp-Up Time[16]		380		µs	For an 80 pF load
CB2 to CB6 Output Ramp-Down Time[17]		30		µs	For an 80 pF load
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.4	V	
Input Current, I_{IN}			±10	µA	
Input Capacitance, C_{IN}		5		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} × 0.9			V	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Floating State Leakage Current			±10	µA	
Floating State Output Capacitance		5		pF	
Output Coding		Straight binary			

[1] For dc accuracy specifications, the LSB size for cell voltage measurements is (2 × V_{REF} − 1 V)/4096. The LSB size for auxiliary ADC input voltage measurements is (2 × V_{REF})/4096.
[2] ADC unadjusted error includes the INL of the ADC and the gain and offset errors of the VIN0 to VIN6 input channels.
[3] The conversion accuracy during cell balancing is decreased due to the activation of the cell balance circuitry. The ADC unadjusted error increases by a factor of 4.
[4] Total unadjusted error includes the INL of the ADC and the gain and offset errors of the VIN0 to VIN6 input channels, as well as the reference error, that is, the difference between the ideal and actual reference voltage and the temperature coefficient of the 2.5 V reference.
[5] The conversion accuracy during cell balancing is decreased due to the activation of the cell balance circuitry. The total unadjusted error increases by a factor of 4.
[6] For the full analog input range, that is, 1 V to 2 × V_{REF}, the total unadjusted error increases by 20%.
[7] The total current measured on the input pins while converting is the sum of the static and dynamic leakage currents. See the Terminology section.
[8] Bit D3 of the control register is set to 0 (thermistor termination resistor function is not in use).
[9] ADC unadjusted error includes the INL of the ADC and the gain and offset errors of the AUXx input channels.
[10] Total unadjusted error includes the INL of the ADC and the gain and offset errors of the AUXx input channels, as well as the reference error, that is, the difference between the ideal and actual reference voltage and the temperature coefficient of the 2.5 V reference.
[11] The turn-on settling time is the time from the rising edge of the $\overline{PD}$ signal until the conversion result settles to the specified accuracy. This includes the time required to power up the regulator and the reference. Note that a rising edge on the $\overline{CNVST}$ input is also required to power up the reference. This rising edge should occur after the rising edge on $\overline{PD}$.
[12] Sample tested during initial release to ensure compliance.
[13] The regulator output voltage is specified with an external 5 mA load in addition to the current required to drive the AV_{CC}, DV_{CC}, and V_{DRIVE} supplies of the AD7280A.
[14] This specification refers to the maximum regulator output current that is available for external use.
[15] The CBx outputs can be set to 0 V or V_{REG} with respect to the negative terminal of the cell being balanced.
[16] The CB1 to CB6 output ramp-up times are defined from the rising edge of the $\overline{CS}$ command until the CB output exceeds V_{REG} − 1 V with respect to the negative terminal of the cell being balanced.
[17] The CB1 to CB6 output ramp-down times are defined from the rising edge of the $\overline{CS}$ command until the CB output falls below 50 mV with respect to the negative terminal of the cell being balanced.

POWER SPECIFICATIONS

V_{DD} = 8 V to 30 V, V_{SS} = 0 V, DV_{CC} = AV_{CC} = V_{REG}, V_{DRIVE} = 2.7 V to 5.5 V, T_A = −40°C to +105°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD}	8		30	V	
Master Device					
I_{DD} During Conversion		5.6	7.3	mA	
I_{DD} During Data Readback		5.3	7.0	mA	
I_{DD} During Cell Balancing		5.1	6.8	mA	
I_{DD} Software Power-Down		2.5	2.9	mA	
I_{DD} Full Power-Down Mode		1.8	5	µA	
Slave Device					
I_{DD} During Conversion		6.9	8.7	mA	
I_{DD} During Data Readback		6.5	8.2	mA	
I_{DD} During Cell Balancing		6.4	8.0	mA	
I_{DD} Software Power-Down		3.8	4.2	mA	
I_{DD} Full Power-Down Mode		1.8	5	µA	
POWER DISSIPATION					
Master Device					V_{DD} = 30 V
During Conversion		170	220	mW	
During Data Readback		160	210	mW	
During Cell Balancing		155	205	mW	
Software Power-Down		75	90	mW	
Full Power-Down Mode		54	150	µW	
Slave Device					V_{DD} = 30 V
During Conversion		210	265	mW	
During Data Readback		195	250	mW	
During Cell Balancing		192	240	mW	
Software Power-Down		115	130	mW	
Full Power-Down Mode		54	150	µW	

TIMING SPECIFICATIONS

V_{DD} = 8 V to 30 V, V_{SS} = 0 V, DV_{CC} = AV_{CC} = V_{REG}, V_{DRIVE} = 2.7 V to 5.5 V, T_A = −40°C to +105°C, unless otherwise noted.

Table 3.

Parameter[1]	Min	Typ	Max	Unit	Description
t_{CONV}					ADC conversion time
	425	560	695	ns	−40°C to +85°C
	425		720	ns	−40°C to +105°C
t_{ACQ}					ADC acquisition time, Bits[D6:D5] of the control register set to 00
	340	400	465	ns	−40°C to +85°C
	340		470	ns	−40°C to +105°C
t_{ACQ}					ADC acquisition time, Bits[D6:D5] of the control register set to 01
	665	800	1010	ns	−40°C to +85°C
	665		1030	ns	−40°C to +105°C
t_{ACQ}					ADC acquisition time, Bits[D6:D5] of the control register set to 10
	1005	1200	1460	ns	−40°C to +85°C
	1005		1510	ns	−40°C to +105°C
t_{ACQ}					ADC acquisition time, Bits[D6:D5] of the control register set to 11
	1340	1600	1890	ns	−40°C to +85°C
	1340		1945	ns	−40°C to +105°C
t_{DELAY}		200	250	ns	Propagation delay between the falling edges of $\overline{CNVST}$ of adjacent parts in the daisy chain
t_{WAIT}	5			µs	Time required between the end of conversions and the beginning of readback of the conversion results
f_{SCLK}			1	MHz	Frequency of serial read clock
t_{QUIET}	200			ns	Minimum quiet time required between the end of a serial read and the start of the next conversion
t_1[2]	0.4		50	µs	$\overline{CNVST}$ low pulse
t_2	10			ns	$\overline{CS}$ falling edge to SCLK rising edge
t_3			20	ns	Delay from $\overline{CS}$ falling edge until SDO is three-state disabled
t_4	5			ns	SDI setup time prior to SCLK falling edge
t_5	4			ns	SDI hold time after SCLK falling edge
t_6[3]			28	ns	Data access time after SCLK rising edge
t_7	20			ns	SCLK to data valid hold time
t_8	0.45 × t_{SCLK}			ns	SCLK high pulse width
t_9	0.45 × t_{SCLK}			ns	SCLK low pulse width
t_{10}[4]	100			ns	$\overline{CS}$ rising edge to SCLK rising edge
t_{11}			10	ns	$\overline{CS}$ rising edge to SDO high impedance
t_{12}	3			µs	$\overline{CS}$ high time required between each 32-bit write/read command

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V. All timing specifications given are with a 25 pF load capacitance.
[2] Maximum allowed $\overline{CNVST}$ low pulse time to ensure that a software power-down state is not entered when the $\overline{CNVST}$ pin is not gated.
[3] Time required for the output to cross 0.4 V or 2.4 V.
[4] t_{10} applies when using a continuous SCLK. Guaranteed by design.

Timing Diagram

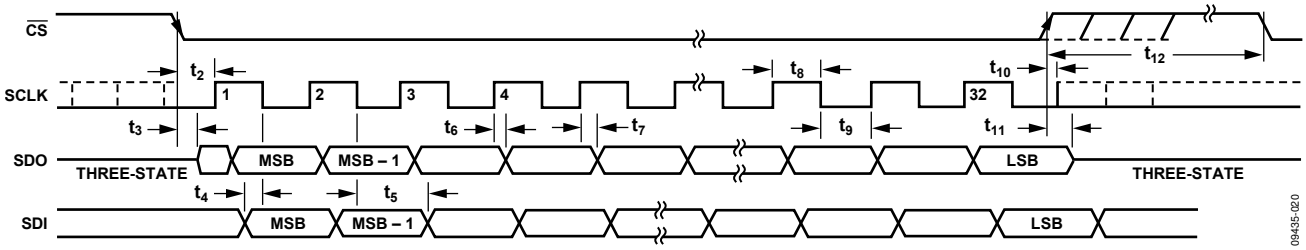

Figure 2. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to V_{SS}, AGND	−0.3 V to +33 V
V_{SS} to AGND, DGND	−0.3 V to +0.3 V
VIN0 to VIN5 Voltage to V_{SS}, AGND	V_{SS} − 0.3 V to V_{DD} + 0.3 V
VIN6 Voltage to V_{SS}, AGND	V_{DD} − 0.3 V to V_{DD} + 1 V
CB1 Output to V_{SS}, AGND	−0.3 V to DV_{CC} + 0.3 V
CBx Output to VIN(x − 1)[1]	−0.3 V to VIN(x − 1)[1] + 7 V
AUX1 to AUX6 Voltage to V_{SS}, AGND	−0.3 V to AV_{CC} + 0.3 V
AUX_{TERM} Voltage to V_{SS}, AGND	−0.3 V to AV_{CC} + 0.3 V
AV_{CC} to V_{SS}, AGND, DGND	−0.3 V to +7 V
DV_{CC} to AV_{CC}	−0.3 V to +0.3 V
DV_{CC} to V_{SS}, DGND	−0.3 V to +7 V
V_{DRIVE} to V_{SS}, AGND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
Digital Input Voltage to V_{SS}, DGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to V_{SS}, DGND	−0.3 V to V_{DRIVE} + 0.3 V
Input Current to Any Pin Except Supply Pins[2]	±10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Pb-Free Temperature, Soldering Reflow	260(+0)°C
ESD	2 kV

[1] x = 2 to 6.
[2] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

To conform with IPC 2221 industrial standards, it is advisable to use conformal coating on the high voltage pins.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
48-Lead LQFP (ST-48)	76.2	17	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

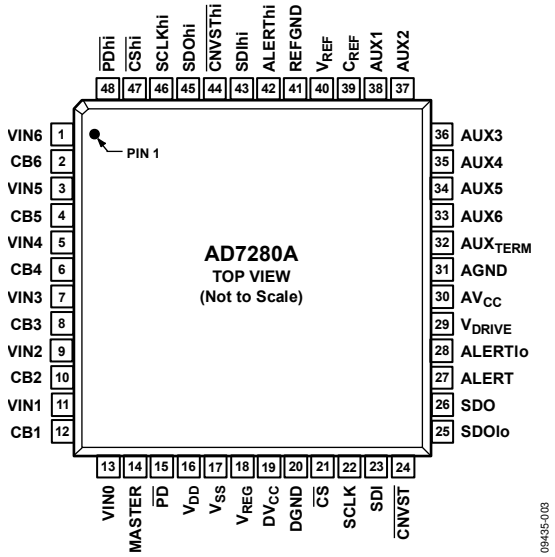

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 5, 7, 9, 11, 13	VIN6 to VIN0	Analog Input 6 to Analog Input 0. VIN0 should be connected to the base of the series-connected battery cells. VIN1 should be connected to the top of Cell 1, VIN2 should be connected to the top of Cell 2, and so on (see Figure 28 and Figure 29).
2, 4, 6, 8, 10, 12	CB6 to CB1	Cell Balance Output 6 to Cell Balance Output 1. These pins provide a voltage output that can be used to supply the gate drive of an external cell balancing transistor. Each CBx output provides a 0 V or 5 V voltage output referenced to the absolute amplitude of the negative terminal of the battery cell that is being balanced.
14	MASTER	Voltage Input. Connect the MASTER pin of the AD7280A that is connected directly to the DSP/microprocessor to the V_{DD} supply pin through a 10 kΩ resistor. In an application with two or more AD7280As in a daisy chain, the MASTER pins of the remaining AD7280As in the daisy chain should be tied to their respective V_{SS} supply pins through 10 kΩ resistors.
15	$\overline{PD}$	Power-Down Input. This input is used to power down the AD7280A. When the AD7280A acts as a master, the $\overline{PD}$ input is supplied from the DSP/microprocessor. When the AD7280A acts as a slave in a daisy chain, the $\overline{PD}$ input should be connected to the $\overline{PDhi}$ output of the AD7280A immediately below it in potential in the daisy chain.
16	V_{DD}	Positive Power Supply Voltage for the High Voltage Analog Input Structure of the AD7280A. The supply must be greater than the minimum voltage of 8 V. V_{DD} can be supplied directly from the cell with the highest potential of the four, five, or six cell battery stacks that the AD7280A is monitoring. The maximum voltage that should be applied between V_{DD} and V_{SS} is 30 V. Place 10 µF and 100 nF decoupling capacitors on the V_{DD} pin.
17	V_{SS}	Negative Power Supply Voltage for the High Voltage Analog Input Structure of the AD7280A. This input should be at the same potential as the AGND/DGND voltage.
18	V_{REG}	Analog Voltage Output, 5.2 V. The internally generated V_{REG} voltage, which provides the supply voltage for the ADC core, is available on this pin for use external to the AD7280A. Place 1 µF and 100 nF decoupling capacitors on the V_{REG} pin.
19	DV_{CC}	Digital Supply Voltage, 4.9 V to 5.5 V. The DV_{CC} and AV_{CC} voltages should ideally be at the same potential. For best performance, it is recommended that the DV_{CC} and AV_{CC} pins be shorted together to ensure that the voltage difference between them never exceeds 0.3 V, even on a transient basis. This supply should be decoupled to DGND. Place 100 nF decoupling capacitors on the DV_{CC} pin. The DV_{CC} supply pin should be connected to the V_{REG} output.
20	DGND	Digital Ground. Ground reference point for all digital circuitry on the AD7280A. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.

Pin No.	Mnemonic	Description
21	$\overline{CS}$	Chip Select Input. The $\overline{CS}$ input is used to frame the input and output data on the SPI and daisy-chain interfaces. On the master AD7280A device, the $\overline{CS}$ input is supplied from the DSP/microprocessor. When the AD7280A acts as a slave in a daisy chain, this input should be connected to the $\overline{CS}$hi output of the AD7280A immediately below it in potential in the daisy chain.
22	SCLK	Serial Clock Input. On the master AD7280A device, the SCLK input is supplied from the DSP/microprocessor. When the AD7280A acts as a slave in a daisy chain, this input should be connected to the SCLKhi output of the AD7280A immediately below it in potential in the daisy chain.
23	SDI	Serial Data Input. Data to be written to the on-chip registers is provided on this input and is clocked into the AD7280A on the falling edge of the SCLK input. On the master AD7280A device, SDI is the data input of the SPI interface. When the AD7280A acts as a slave in a daisy chain, this input accepts data from the SDOhi output of the AD7280A immediately below it in potential in the daisy chain.
24	$\overline{CNVST}$	Convert Start Input. The conversion is initiated on the falling edge of $\overline{CNVST}$. On the master AD7280A, the $\overline{CNVST}$ pulse is supplied from the DSP/microprocessor; this input can also be tied to DV_{CC} and the conversion initiated through the serial interface. When the AD7280A acts as a slave in a daisy chain, this input should be connected to the $\overline{CNVST}$hi output of the AD7280A immediately below it in potential in the daisy chain.
25	SDOlo	Serial Data Output in Daisy-Chain Mode. On the master AD7280A device, this output should be connected to V_{SS} either directly or through a pull-down, 1 kΩ resistor. When the AD7280A acts as a slave in a daisy chain, this output should be connected to the SDIhi input of the AD7280A immediately below it in potential in the daisy chain.
26	SDO	Serial Data Output. The conversion output data or the register output data is supplied to this pin as a serial data stream. The bits are clocked out on the rising edge of the SCLK input; 32 SCLKs are required to access the data. On the master AD7280A device, the SDO output should be connected to the DSP/microprocessor. The SDO outputs of the remaining AD7280As in the daisy chain should be connected to V_{SS} either directly or through a pull-down, 1 kΩ resistor.
27	ALERT	Digital Output. This flag indicates cell or auxiliary ADC input overvoltage or undervoltage. The ALERT output of the master AD7280A should be connected to the DSP/microprocessor. The ALERT outputs of the remaining AD7280As in the daisy chain should be connected to V_{SS} either directly or through a pull-down, 1 kΩ resistor.
28	ALERTlo	Alert Output in Daisy-Chain Mode. On the master AD7280A, this output should be connected to V_{SS} either directly or through a pull-down, 1 kΩ resistor. When the AD7280A acts as a slave in a daisy chain, this output should be connected to the ALERThi input of the AD7280A immediately below it in potential in the daisy chain.
29	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines the voltage at which the SPI interface operates. This pin should be decoupled to DGND. On the master AD7280A device, the voltage range on this pin is 2.7 V to 5.5 V. The V_{DRIVE} voltage can be different from the voltage at AV_{CC} and DV_{CC}, but it should never exceed either by more than 0.3 V. The V_{DRIVE} pin of the remaining AD7280As in the daisy chain should be connected to V_{REG}.
30	AV_{CC}	Analog Supply Voltage for the ADC Core, 4.9 V to 5.5 V. The AV_{CC} and DV_{CC} voltages should ideally be at the same potential. For best performance, it is recommended that the AV_{CC} and DV_{CC} pins be shorted together to ensure that the voltage difference between them never exceeds 0.3 V, even on a transient basis. This supply should be decoupled to AGND. Place 100 nF decoupling capacitors on the AV_{CC} pin. The AV_{CC} supply pin should be connected to the V_{REG} output.
31	AGND	Analog Ground. This pin is the ground reference point for all analog circuitry on the AD7280A. This input should be at the same potential as the base of the series-connected battery cells. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
32	AUX_{TERM}	Thermistor Termination Resistor Input. If this function is not required in the application, it is recommended that this pin be connected to V_{REG} through a 10 kΩ resistor.
33 to 38	AUX6 to AUX1	Auxiliary, Single-Ended 5 V ADC Inputs. If any of these inputs is not required in the application, it is recommended that the pin be connected to V_{REG} through a 10 kΩ resistor.
39	C_{REF}	Reference Capacitor. A 100 nF decoupling capacitor to REFGND should be placed on this pin.
40	V_{REF}	Reference Output, 2.5 V. The on-chip reference is available on this pin for use external to the AD7280A. A 1 µF decoupling capacitor to REFGND is recommended on this pin.
41	REFGND	Reference Ground. This pin is the ground reference point for the internal band gap reference circuitry on the AD7280A. The REFGND voltage should be at the same potential as the AGND voltage.
42	ALERThi	Alert Input in Daisy-Chain Mode. The alert signal from each AD7280A in the daisy chain is passed through the ALERTlo output and the ALERThi input of each AD7280A in the chain and is supplied to the DSP/microprocessor through the ALERT output of the master AD7280A. This input should be connected to the ALERTlo output of the AD7280A immediately above it in potential in the daisy chain. The AD7280A at the highest potential in the stack does not require an alert input; in this case, the pin should be connected to V_{DD} through a 1 kΩ resistor.

Pin No.	Mnemonic	Description
43	SDIhi	Serial Data Input in Daisy-Chain Mode. The data from each AD7280A in the daisy chain is passed through the SDOlo output and the SDIhi input of each AD7280A in the chain and is supplied to the DSP/microprocessor through the SDO output of the master AD7280A. This input should be connected to the SDOlo output of the AD7280A immediately above it in potential in the daisy chain. The AD7280A at the highest potential in the stack does not require a serial data input in daisy-chain mode; in this case, the pin should be connected to V_{DD} through a 1 kΩ resistor.
44	$\overline{\text{CNVSThi}}$	Conversion Start Output in Daisy-Chain Mode. The convert start signal from the DSP/microprocessor supplied to the $\overline{\text{CNVST}}$ input of the master AD7280A is passed through each AD7280A by means of the $\overline{\text{CNVST}}$ input and the $\overline{\text{CNVSThi}}$ output. This output should be connected to the $\overline{\text{CNVST}}$ pin of the AD7280A immediately above it in potential in the daisy chain. The AD7280A at the highest potential in the stack does not require a daisy-chain conversion start output; in this case, the pin should be connected to V_{DD}.
45	SDOhi	Serial Data Output in Daisy-Chain Mode. The serial data input from the DSP/microprocessor supplied to the SDI input of the master AD7280A is passed through each AD7280A by means of the SDI input and the SDOhi output. This output should be connected to the SDI input of the AD7280A immediately above it in potential in the daisy chain. The AD7280A at the highest potential in the stack does not require a daisy-chain serial data output; in this case, the pin should be connected to V_{DD}.
46	SCLKhi	Serial Clock Output in Daisy-Chain Mode. The clock signal from the DSP/microprocessor supplied to the SCLK input of the master AD7280A is passed through each AD7280A by means of the SCLK input and the SCLKhi output. This output should be connected to the SCLK input of the AD7280A immediately above it in potential in the daisy chain. The AD7280A at the highest potential in the stack does not require a daisy-chain serial clock output; in this case, the pin should be connected to V_{DD}.
47	$\overline{\text{CShi}}$	Chip Select Output in Daisy-Chain Mode. The chip select signal from the DSP/microprocessor supplied to the $\overline{\text{CS}}$ input of the master AD7280A is passed through each AD7280A by means of the $\overline{\text{CS}}$ input and the $\overline{\text{CShi}}$ output. This output should be connected to the $\overline{\text{CS}}$ input of the AD7280A immediately above it in potential in the daisy chain. The AD7280A at the highest potential in the stack does not require a daisy-chain chip select output; in this case, the pin should be connected to V_{DD}.
48	$\overline{\text{PDhi}}$	Power-Down Output in Daisy-Chain Mode. The power-down signal from the DSP/microprocessor supplied to the $\overline{\text{PD}}$ input of the master AD7280A is passed through each AD7280A by means of the $\overline{\text{PD}}$ input and the $\overline{\text{PDhi}}$ output. This output should be connected to the $\overline{\text{PD}}$ input of the AD7280A immediately above it in potential in the daisy chain. The AD7280A at the highest potential in the stack does not require a daisy-chain power-down output; in this case, the pin should be connected to V_{DD}.

TYPICAL PERFORMANCE CHARACTERISTICS

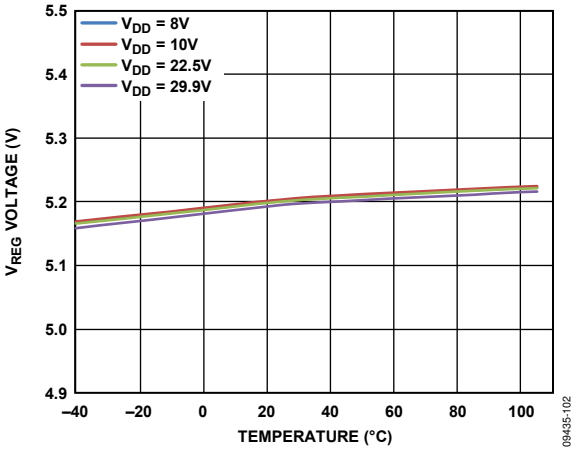

Figure 4. V_{REG} vs. Temperature for Different Supply Voltages, V_{REG} Connected to AV_{CC} and DV_{CC}

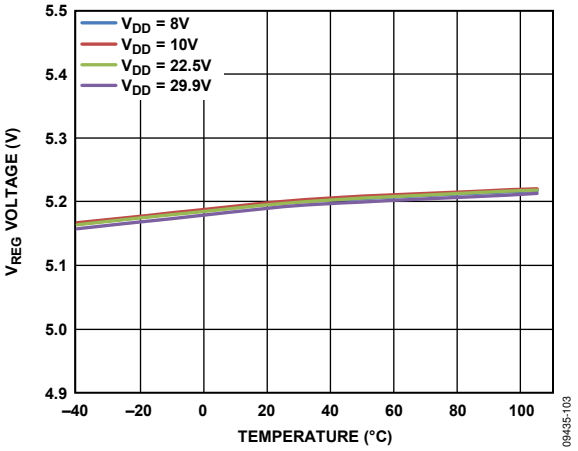

Figure 5. V_{REG} vs. Temperature for Different Supply Voltages, V_{REG} Connected to AV_{CC} and DV_{CC}, 5 mA External Load

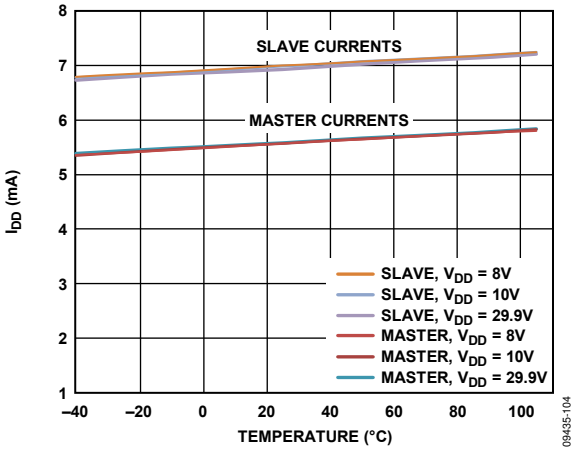

Figure 6. I_{DD} During Conversion vs. Temperature for Different Supply Voltages

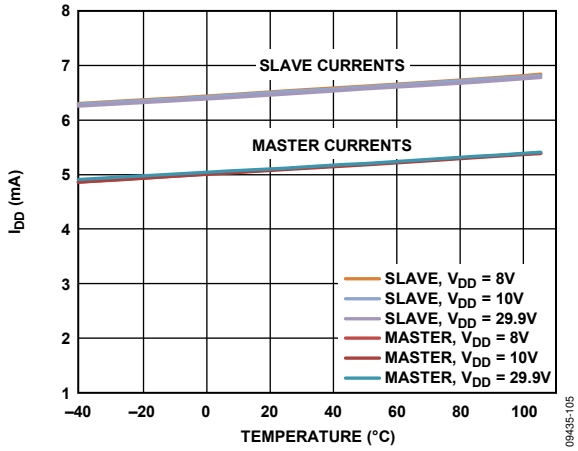

Figure 7. I_{DD} During Cell Balancing vs. Temperature for Different Supply Voltages

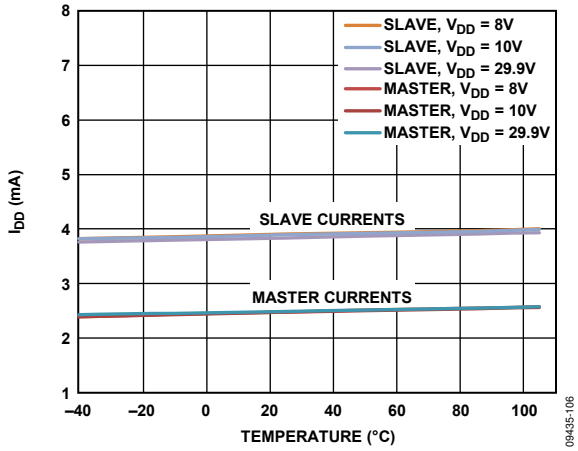

Figure 8. I_{DD} During Software Power-Down vs. Temperature for Different Supply Voltages

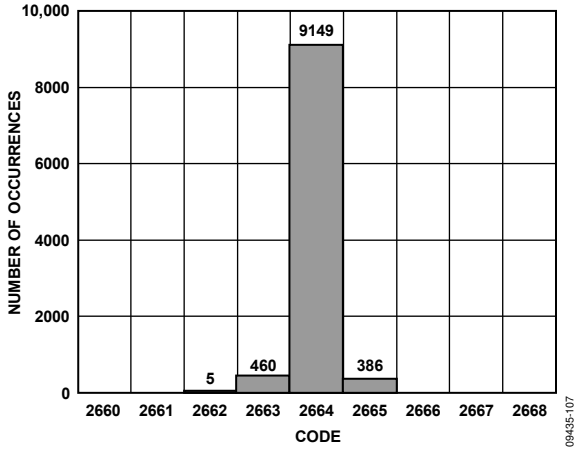

Figure 9. Histogram of Codes for 10,000 Samples, Odd Cell Voltage Channels

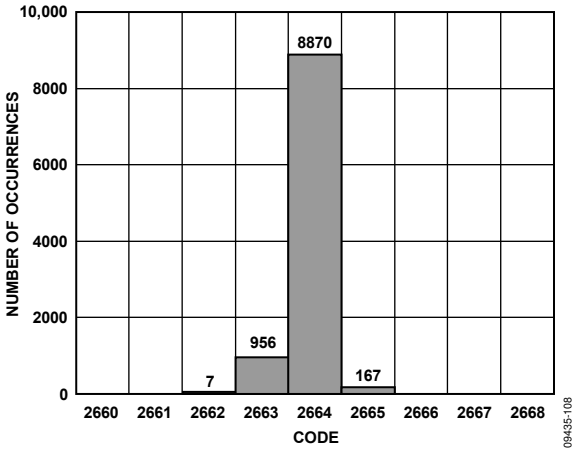

Figure 10. Histogram of Codes for 10,000 Samples, Even Cell Voltage Channels

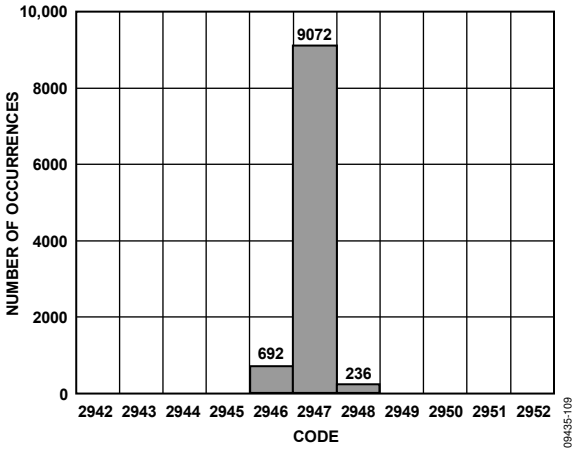

Figure 11. Histogram of Codes for 10,000 Samples, Auxiliary Channels

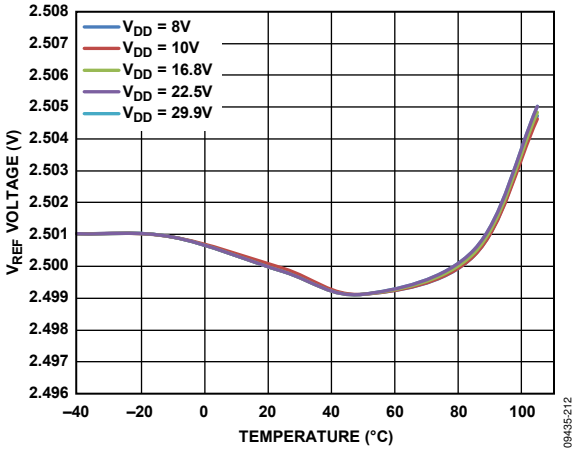

Figure 12. V_{REF} vs. Temperature for Different Supply Voltages

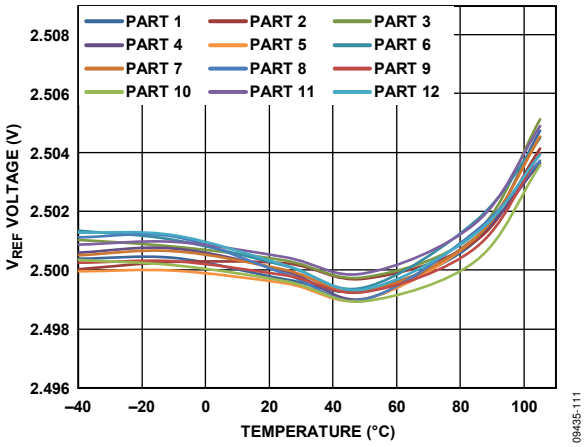

Figure 13. V_{REF} vs. Temperature for Different Parts

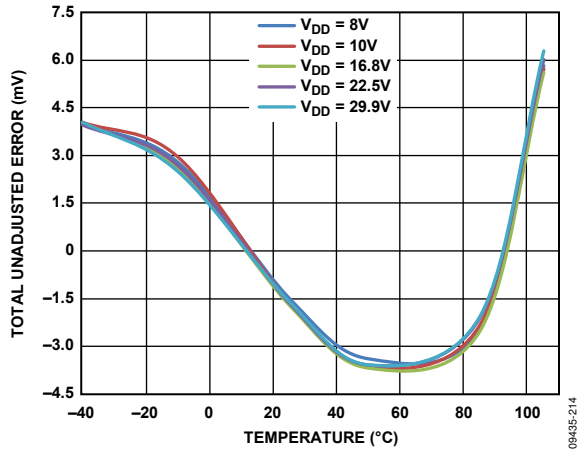

Figure 14. Total Unadjusted Error for Even Cell Voltage Channels (Absolute Value) vs. Temperature for Different Supply Voltages

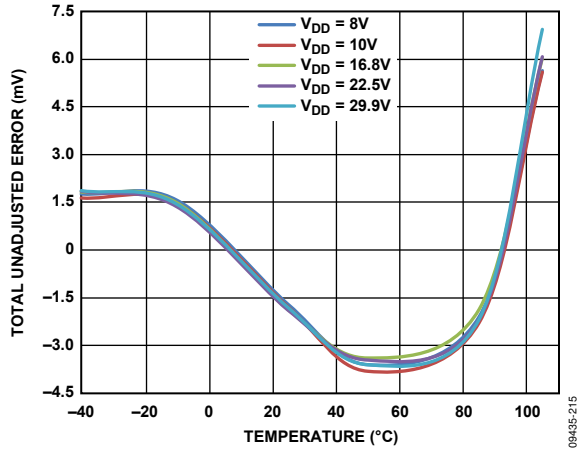

Figure 15. Total Unadjusted Error for Odd Cell Voltage Channels (Absolute Value) vs. Temperature for Different Supply Voltages

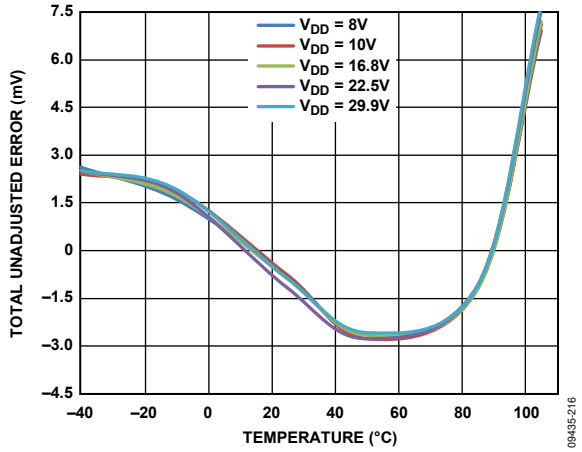

Figure 16. Total Unadjusted Error for Auxiliary Channels (Absolute Value) vs. Temperature for Different Supply Voltages

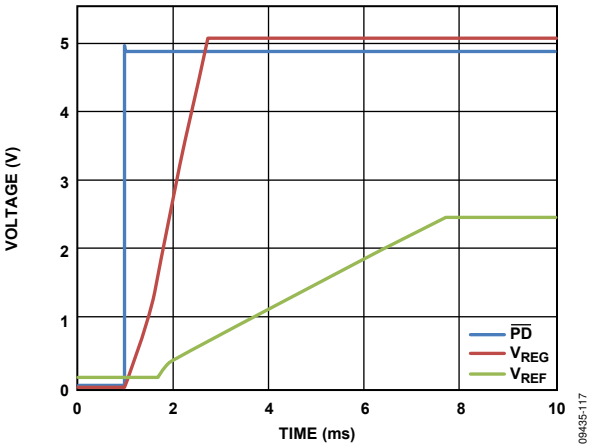

Figure 19. Power-Up Time, 10 µF Capacitor on the V_{REF} and V_{REG} Pins

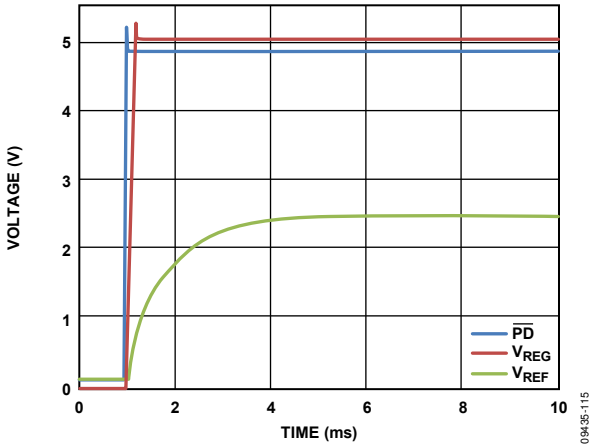

Figure 17. Power-Up Time, 1 µF Capacitor on the V_{REF} and V_{REG} Pins

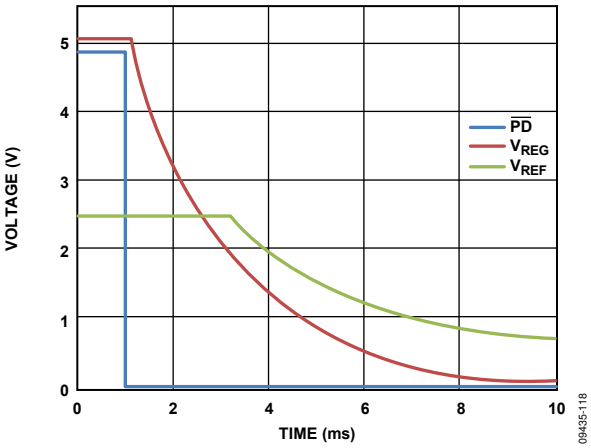

Figure 20. Power-Down Time, 10 µF Capacitor on the V_{REF} and V_{REG} Pins

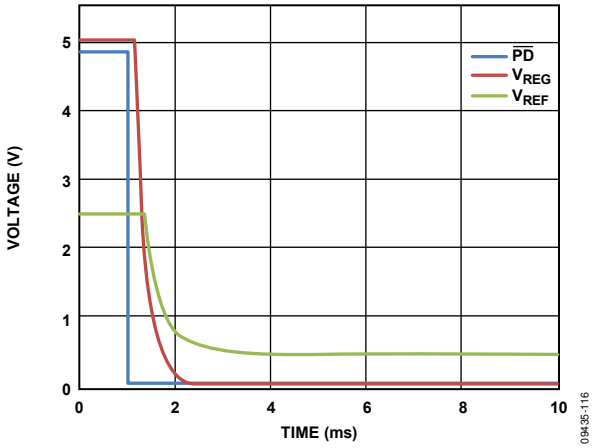

Figure 18. Power-Down Time, 1 µF Capacitor on the V_{REF} and V_{REG} Pins

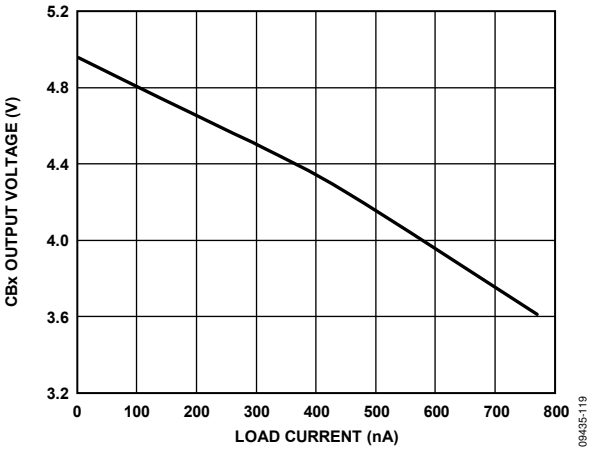

Figure 21. CBx Output Voltage vs. Load Current

TERMINOLOGY

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (a point 1 LSB below the first code transition) and full scale (a point 1 LSB above the last code transition).

Offset Error
Offset error applies to straight binary output coding. It is the deviation of the first code transition (000 ... 000) to (000 ... 001) from the ideal, that is, AGND + 1 LSB for AUX1 to AUX6 and 1 V + AGND + 1 LSB for VIN0 to VIN6.

Offset Error Match
Offset error match is the difference in zero code error across all six channels.

Gain Error
Gain error applies to straight binary output coding. It is the deviation of the last code transition (111 ... 110) to (111 ... 111) from the ideal (that is, 2 × V_{REF} − 1 LSB) after adjusting for the offset error.

Gain Error Match
Gain error match is the difference in gain error across all six channels.

ADC Unadjusted Error
ADC unadjusted error includes the INL error and the offset and gain errors of the ADC and measurement channel.

Total Unadjusted Error (TUE)
TUE is the maximum deviation of the output code from the ideal. Total unadjusted error includes the INL error, the offset and gain errors, and the reference errors. Reference errors include the difference between the actual and ideal reference voltage (that is, 2.5 V) and the reference voltage temperature coefficient.

Reference Voltage Temperature Coefficient
The reference voltage temperature coefficient is derived from the maximum and minimum reference output voltage (V_{REF}) measured between T_{MIN} and T_{MAX}. It is expressed in ppm/°C using the following equation:

$$TCV_{REF}\,(\text{ppm}/^\circ\text{C}) = \left(\frac{V_{REF}(Max) - V_{REF}(Min)}{2.5\,\text{V} \times (T_{MAX} - T_{MIN})}\right) \times 10^6$$

where:
$V_{REF}(Max)$ is the maximum V_{REF} between T_{MIN} and T_{MAX}.
$V_{REF}(Min)$ is the minimum V_{REF} between T_{MIN} and T_{MAX}.
T_{MAX} = +85°C or +105°C.
T_{MIN} = −40°C.

Output Voltage Hysteresis
Output voltage hysteresis, or thermal hysteresis, is defined as the absolute maximum change of reference output voltage after the device is cycled through temperature from either T_HYS+ or T_HYS−, where:

T_HYS+ = +25°C to T_{MAX} to +25°C
T_HYS− = +25°C to T_{MIN} to +25°C

Output voltage hysteresis is expressed in ppm using the following equation:

$$V_{HYS}\,(\text{ppm}) = \left(\frac{V_{REF}(25^\circ\text{C}) - V_{REF}(T\_HYS)}{V_{REF}(25^\circ\text{C})}\right) \times 10^6$$

where:
V_{REF}(25°C) = V_{REF} at 25°C.
$V_{REF}(T\_HYS)$ is the maximum change of V_{REF} at T_HYS+ or T_HYS−.

Static Leakage Current
Static leakage current is the current measured on the cell voltage and/or the auxiliary ADC inputs when the device is static, that is, not converting.

Dynamic Leakage Current
Dynamic leakage current is the current measured on the cell voltage and/or the auxiliary ADC inputs when the device is converting, with the static leakage current subtracted. Dynamic leakage current is specified with a convert start pulse frequency of 10 Hz, that is, every 100 ms. The dynamic leakage current for a different conversion rate can be calculated using the following equation:

$$I_{DYN(B)} = \left(\frac{I_{DYN(A)} \times f_{CNVST(B)}}{f_{CNVST(A)}}\right)$$

where:
$I_{DYN(A)}$ is the dynamic leakage current at the convert start frequency, $f_{CNVST(A)}$ (see Table 1).
$I_{DYN(B)}$ is the dynamic leakage current at the desired convert start frequency, $f_{CNVST(B)}$.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7280A is a lithium ion (Li-Ion) battery monitoring chip that can monitor the voltage and temperature of four, five, or six series-connected Li-Ion battery cells. The AD7280A also provides an interface that can be used to control external transistors for cell balancing.

The V_{DD} and V_{SS} supplies required by the AD7280A should be taken from battery cells being monitored by the part. An internal V_{REG} rail is generated to provide power for the ADC and the internal interface circuitry. This V_{REG} voltage is available on an output pin for use external to the AD7280A.

The AD7280A consists of a high voltage input multiplexer, a low voltage input multiplexer, and a SAR ADC. The high voltage multiplexer allows four, five, or six series-connected Li-Ion battery cells to be measured. The low voltage multiplexer provides the user with six single-ended ADC inputs that can be used in combination with external thermistors to measure the temperature of each battery cell. The auxiliary ADC inputs can also be used for external diagnostics in the application. Initiating conversions on all 12 channels, that is, the six cell voltage channels and the six auxiliary ADC channels, requires only a single $\overline{\text{CNVST}}$ pulse. Alternatively, the conversion can be initiated through the rising edge of $\overline{\text{CS}}$. Each conversion result is stored in an individual result register (see Table 13).

Each individual cell voltage and auxiliary ADC measurement requires a minimum of 1 µs to acquire and complete a conversion. Depending on the external components connected to the analog inputs of the AD7280A, additional acquisition time may be required. A higher acquisition time can be selected through the control register. The AD7280A also provides a conversion averaging option that can be selected through the control register. This option allows the user to complete two, four, or eight averages on each cell voltage and auxiliary ADC measurement. The averaged conversion results are stored in the result registers. On power-up, the default combined acquisition and conversion time is 1 µs, with the averaging register set to 0, that is, a single conversion per channel.

The results of the cell voltage and auxiliary ADC conversions are read back via the 4-wire serial peripheral interface (SPI). The SPI is also used to write to and read from the internal registers.

The AD7280A features an alert function that can be triggered if the voltage conversion results or the auxiliary ADC conversion results exceed the maximum and minimum voltage thresholds selected by the user. The alert modes and threshold levels are selected by writing to internal registers.

The AD7280A provides six analog output voltages that can be used to control external transistors as part of a cell balancing circuit. Each cell balance output provides a 0 V or 5 V voltage, with respect to the potential on the base of each individual cell, that can be applied to the gate of the external cell balancing transistors.

The AD7280A features a daisy-chain interface. Individual AD7280A devices can monitor the cell voltages and temperatures of six cells. A chain of AD7280As can be used to monitor the cell voltages and temperatures of a larger number of cells. The conversion data from each AD7280A in the chain passes to the system controller via a single SPI interface. Control data can similarly be passed via the SPI up the chain to each individual AD7280A.

The AD7280A includes an on-chip 2.5 V reference. The reference voltage is available for use external to the AD7280A.

The AD7280A also has a V_{DRIVE} feature to control the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, in the recommended configuration, the AD7280A is operated with a supply of 5 V; however, the V_{DRIVE} pin can be powered from a 3 V supply, allowing a large dynamic range with low voltage digital processors.

CONVERTER OPERATION

The conversion paths of the AD7280A consist of a high voltage input multiplexer or a low voltage input multiplexer and a SAR ADC. The high voltage multiplexer selects the pair of analog inputs, VIN0 to VIN6, that is to be converted. The voltage of each individual cell is measured by converting the difference between adjacent analog inputs, that is, VIN1 − VIN0, VIN2 − VIN1, and so on (see Figure 22 and Figure 23). The low voltage multiplexer selects the auxiliary ADC input, AUX1 to AUX6, that is to be converted. The conversion results for each cell voltage and auxiliary ADC input can be accessed t_{WAIT} after the programmed conversion sequence is completed.

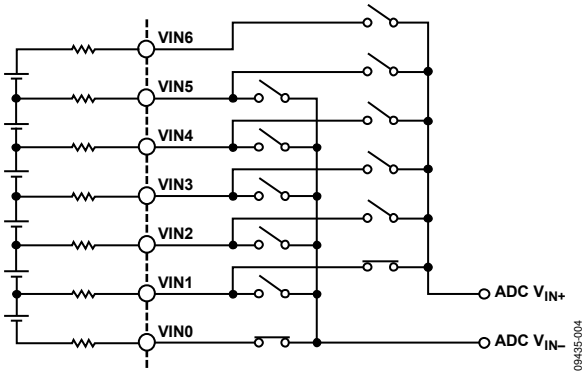

Figure 22. Mux Configuration During VIN1 to VIN0 Sampling

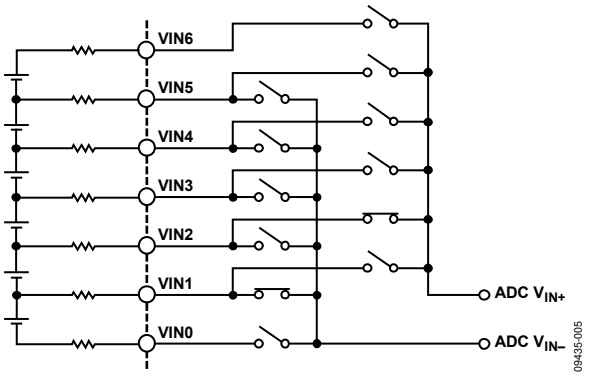

Figure 23. Mux Configuration During VIN2 to VIN1 Sampling

The ADC is a successive approximation register analog-to-digital converter (SAR ADC). The converter is composed of a comparator, a SAR, control logic, and two capacitive DACs. Figure 24 shows a simplified schematic of the converter. During the acquisition phase, the SW1, SW2, and SW3 switches are closed. The sampling capacitor array acquires the signal on the input during this phase.

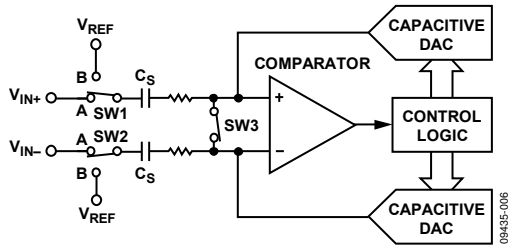

Figure 24. ADC Configuration During Acquisition Phase

When the ADC starts a conversion, SW3 opens, and SW1 and SW2 move to Position B, causing the comparator to become unbalanced (see Figure 25). The control logic and capacitive DACs are used to add and subtract fixed amounts of charge to return the comparator to a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. This output code is then stored in the appropriate register for the input that has been converted.

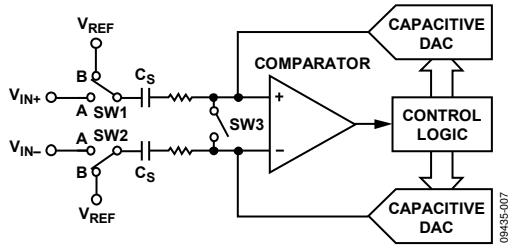

Figure 25. ADC Configuration During Conversion Phase

ANALOG INPUT STRUCTURE

Figure 26 shows the equivalent circuit of the analog input structure of the AD7280A. The diodes provide ESD protection. The resistors are lumped components made up of the on resistance of the input multiplexer, internal track resistance, and other internal switches. The value of these resistors is approximately 300 Ω typical. Capacitor C1 is also a lumped component made up of pin capacitance, ESD diodes, and switch capacitance, whereas Capacitor C2 is the sampling capacitor of the ADC. The total lumped capacitance of C1 and C2 is approximately 15 pF.

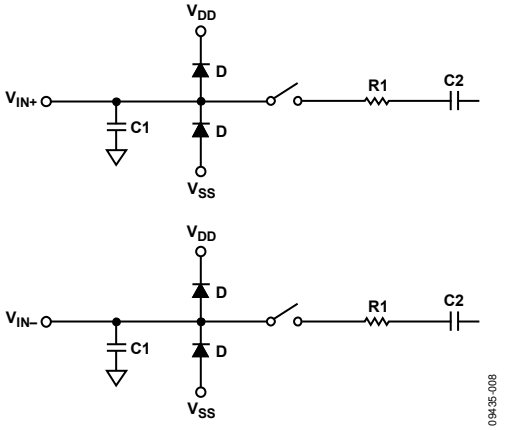

Figure 26. Equivalent Analog Input Circuit

TRANSFER FUNCTION

The output coding of the AD7280A is straight binary. The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSBs, and so on). The LSB size is dependent on whether the cell voltage or the auxiliary ADC inputs are being measured. The analog input range of the voltage inputs is 1 V to 5 V, and the analog input range of the auxiliary ADC inputs is 0 V to 5 V. The ideal transfer characteristic is shown in Figure 27.

Table 7. LSB Sizes for Each Analog Input Range

Selected Inputs	Input Range	Full-Scale Range	LSB Size
Cell Voltage	1 V to 5 V	4 V/4096	976 µV
Auxiliary ADC Inputs	0 V to 5 V	5 V/4096	1.22 mV

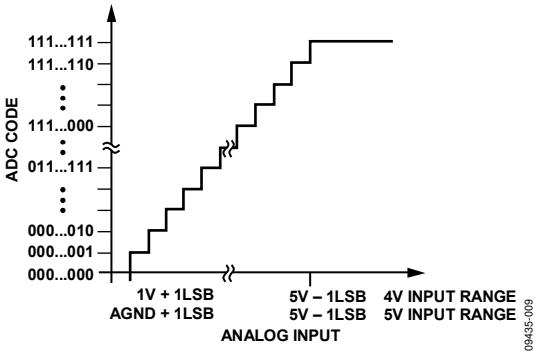

Figure 27. Ideal Transfer Characteristic

TYPICAL CONNECTION DIAGRAMS

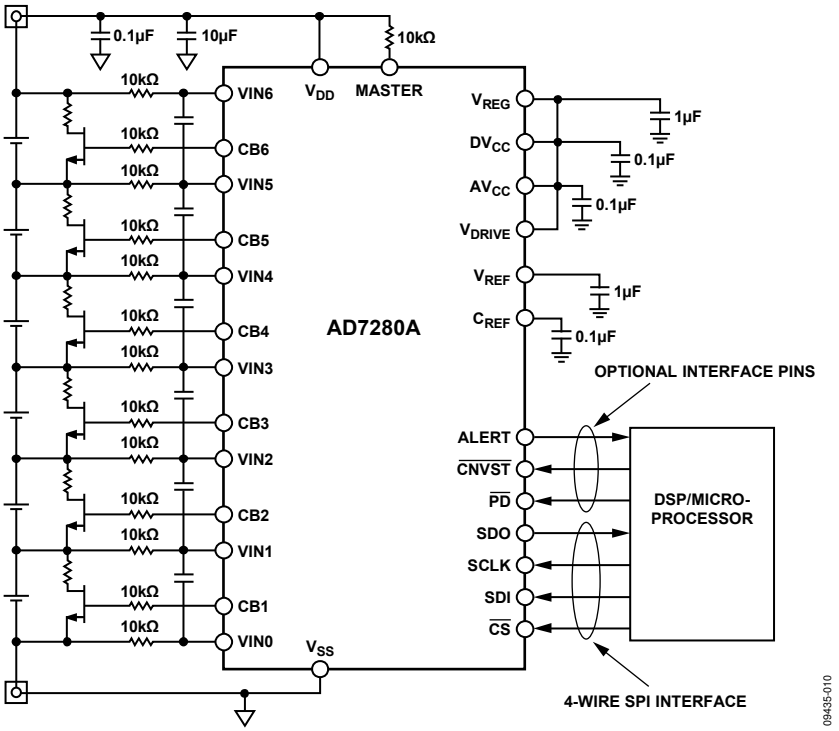

Figure 28. AD7280A Configuration Diagram for Six Battery Cells

The AD7280A can be used to monitor four, five, or six battery cells connected in series. A typical configuration for a six-cell battery monitoring application is shown in Figure 28. However, lithium ion battery applications require a significant number of individual cells to provide the required output voltage. Figure 29 shows the recommended configuration of a chain of AD7280As monitoring a larger battery stack. The daisy-chain interface of the AD7280A allows each individual AD7280A to communicate with the AD7280A immediately above and below it. The daisy-chain interface allows the AD7280As to be electrically connected to the battery management chip without the need for individual isolation devices between each AD7280A.

As shown in Figure 29, it is recommended that a Zener diode be placed across the supplies of each AD7280A. This prevents an overvoltage across the supplies of each AD7280A during the initial connection of the daisy chain of AD7280As to the battery stack. A voltage rating of 30 V is suggested for this Zener diode, but lower values can also be used to suit the application.

The 10 kΩ resistor in series with the inputs combined with a 100 nF capacitor across the adjacent differential inputs acts as a low-pass filter. The 10 kΩ resistors provide protection for the analog inputs in the event of an overvoltage or undervoltage on those inputs, for example, if any of the cell voltage inputs is incorrectly shorted to V_{DD} or V_{SS}. The resistors also provide protection during the initial connection of the daisy chain of AD7280As to the battery stack. For more information about the daisy-chain interface, see the Daisy-Chain Interface section.

In an application that includes a safety mechanism designed to open circuit the battery stack, additional isolation is required between the AD7280A above the break point and the battery management chip.

A suggested configuration for the external cell balancing circuit is shown in Figure 28. This configuration also includes 10 kΩ resistors in series with the cell balance outputs. These resistors provide protection for the cell balance outputs in the event of an overvoltage or undervoltage on those inputs. See the Cell Balancing Outputs section for more information.

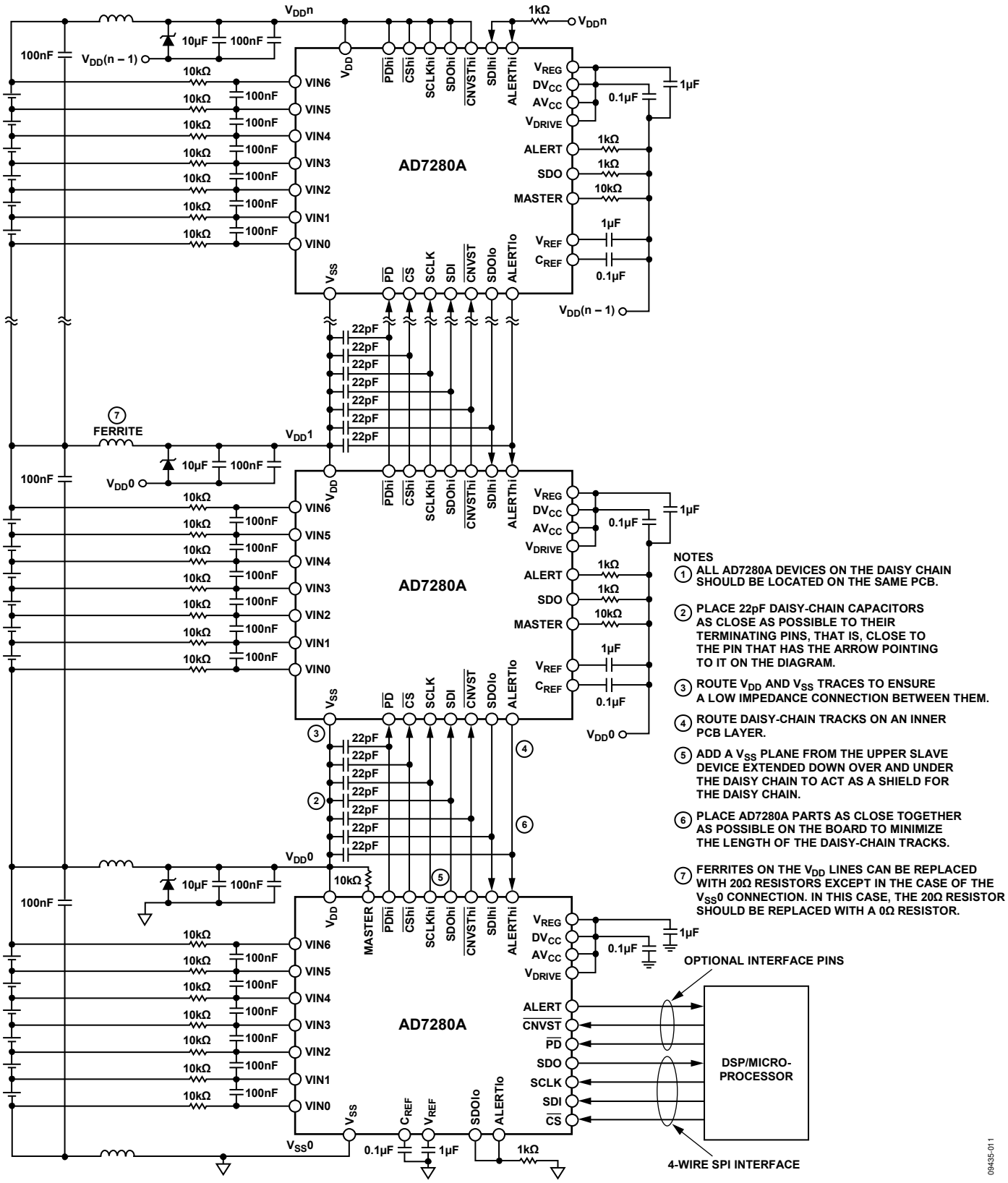

Figure 29. AD7280A Daisy-Chain Configuration

REFERENCE

The internal reference is temperature compensated to 2.5 V. The reference is trimmed to provide a typical drift of ±3 ppm/°C. As shown in Figure 30, the internal reference circuitry consists of a 1.2 V band gap reference and a reference buffer. The 2.5 V reference is available at the V_{REF} pin. The V_{REF} pin should be decoupled to REFGND using a 1 µF or greater ceramic capacitor. The C_{REF} pin should be decoupled to REFGND using a 0.1 µF or greater ceramic capacitor. The 2.5 V reference is capable of driving an external load of up to 10 kΩ.

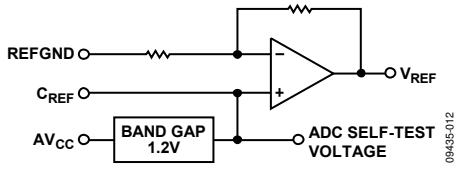

Figure 30. AD7280A Internal Reference

CONVERTING CELL VOLTAGES AND AUXILIARY ADC INPUTS

A conversion can be initiated on the AD7280A using either the $\overline{\text{CNVST}}$ input or the serial interface (see the Conversion Start Format section). A single conversion command initiates conversions on all selected channels of the AD7280A. As described in the Converter Operation section, the voltage of each individual battery cell is measured by converting the difference between adjacent analog inputs. The first cell to be converted following a convert start command is Cell 6, which is the difference between VIN6 and VIN5. At the end of the first conversion, the AD7280A generates an internal end-of-conversion (EOC) signal. This internal EOC selects the next cell voltage inputs for measurement through the multiplexer, that is, the difference between VIN5 and VIN4. The new input is acquired, and a second internal convert start signal is generated, which initiates the conversion. This process is repeated until all the selected voltage and auxiliary ADC inputs have been converted.

The conversion sequence—that is, the order in which the cell voltages and auxiliary ADC inputs are converted—is shown in Figure 31 and Figure 32. The cell voltage inputs are converted in reverse order, that is, Cell 6 is followed by Cell 5, and so on. However, the auxiliary ADC inputs are converted in increasing numerical order, that is, AUX1 is followed by AUX2, and so on. For example, when all 12 inputs are selected for conversion, the conversion of Cell 1, that is, VIN1 to VIN0, is followed by the conversion of the AUX1 input.

When all selected conversions are completed, the VIN6 and VIN5 voltage inputs are again selected through the multiplexer, and the voltage across Cell 6 is acquired in preparation for the next conversion request. This is the default state for the multiplexer.

Bits[D15:D14] of the control register select the cell voltage and auxiliary ADC inputs to be converted. There are four options available (see Table 8).

Table 8. Cell Voltage and Auxiliary ADC Input Selection

Bits[D15:D14]	Voltage Inputs	Auxiliary ADC Inputs
00	6 to 1	1 to 6
01	6 to 1	1, 3, and 5
10	6 to 1	None
11	ADC self-test	None

Each voltage and auxiliary ADC input conversion requires a minimum of 1 µs to acquire and convert the cell voltage or auxiliary ADC input voltage. For example, when Bits[D15:D14] are set to 00, the falling edge of $\overline{\text{CNVST}}$ triggers a series of 12 conversions. This requires a minimum of 12 µs to convert all selected measurements on a single AD7280A. If no auxiliary ADC input conversions are required, Bits[D15:D14] are set to 10. In this case, the conversion request triggers a series of six conversions, requiring a minimum of 6 µs.

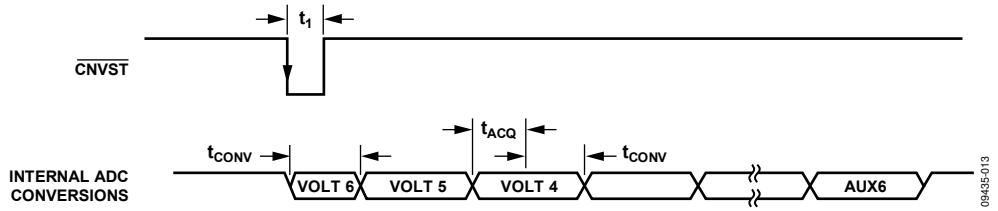

Figure 31. ADC Conversions on the AD7280A

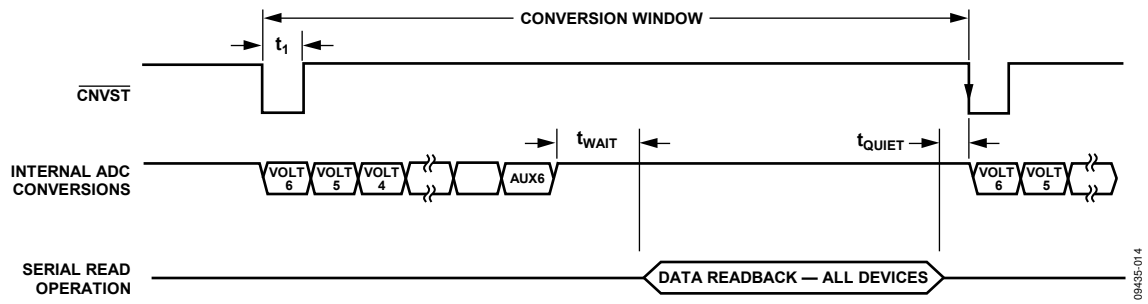

Figure 32. ADC Conversions and Readback on the AD7280A

Note that 90 µs should be allowed before initiating any conversions following any change to Bits[D15:D14]. This time should be allowed between writing to the control register to change the selected conversions and initiating the first conversion. Conversions that are initiated by the rising edge of the $\overline{CS}$ pin require two separate write commands to the control register. The first command configures the AD7280A for the required acquisition time; the second command, following a delay of 90 µs, initiates the conversion on the rising edge of $\overline{CS}$.

After the completion of all requested conversions, the results can be read back from either a single device or from all devices in a daisy chain by using the SPI and daisy-chain interfaces. For more information, see the Serial Interface section and the Daisy-Chain Interface section.

As shown in Figure 32, a wait time, t_{WAIT}, is required between the completion of conversions and the start of readback. This time is required to synchronize the high speed conversion clock and the lower speed clock used for all other AD7280A operations. The minimum value of t_{WAIT} is 5 µs.

Acquisition Time

The time required to acquire an input signal depends on how quickly the sampling capacitor is charged. This, in turn, depends on the input impedance and any external components placed on the analog inputs. The default acquisition time of the AD7280A on initial power-up is 400 ns. This time can be increased in steps of 400 ns up to 1.6 µs to provide flexibility in selecting external components on the analog inputs. The acquisition time is selected by writing to Bits[D6:D5] in the control register (see Table 9).

Table 9. Analog Input Acquisition Time

Bits[D6:D5]	Acquisition Time
00	400 ns
01	800 ns
10	1.2 µs
11	1.6 µs

The acquisition time required is calculated using the following formula:

$$t_{ACQ} = 10 \times ((R_{SOURCE} + R) \times C)$$

where:

R_{SOURCE} should include any extra source impedance on the analog input between the external capacitors (100 nF) and the input pins. It does not include any extra source impedance, for example, the 10 kΩ series resistors, which are between the battery cells and the external capacitors.

R is the resistance seen by the track-and-hold amplifier looking at the input, 300 Ω.

C is the sampling capacitance, that is, the value of the sampling capacitor, 15 pF.

Conversion Averaging

The AD7280A includes an option where the acquisition and conversion of each cell input can be repeated with an averaged conversion result being stored in the individual register. The averaged conversion result can then be read back through the SPI interface in the same manner as a standard conversion result. The AD7280A can be programmed, through Bits[D10:D9] of the control register, to complete one, two, four, or eight conversions. The default on power-up is a single conversion per channel, that is, no averaging.

Selection of the two, four, or eight average options through the control register causes the control sequence of both the high voltage and low voltage input multiplexers to be reconfigured to allow the additional acquisitions and conversions to be completed. In each case, the requested number of conversions is completed on each channel before beginning the acquisition and conversion of the next channel in sequence. For example, if an average of two conversions is requested, the new sequence is Voltage Channel 6, Voltage Channel 6, Voltage Channel 5, Voltage Channel 5, Voltage Channel 4, and so on.

It should also be noted that when the high voltage multiplexer is reconfigured, 90 µs should be allowed before initiating any conversions. This time should be allowed between writing to the control register to select averaging and initiating the first conversion. Conversions that are being initiated by the rising edge of the $\overline{CS}$ pin require two separate write commands to the control register. The first command configures the AD7280A for the required averaging, and the second command, after a delay of 90 µs, initiates the conversion on the rising edge of $\overline{CS}$.

Suggested External Component Configuration on Analog Inputs

As described in the Acquisition Time section, the acquisition time of the AD7280A is selected by the status of Bits[D6:D5] in the control register. This provides flexibility in selecting external components on the analog inputs. A suggested configuration for placing external components on the analog inputs to the AD7280A is shown in Figure 33.

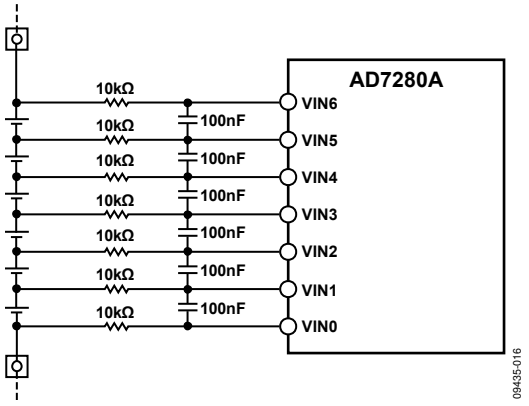

Figure 33. External Series Resistance and Shunt Capacitance

The 10 kΩ resistors in series with the inputs provide protection for the analog inputs in the event of an overvoltage or undervoltage on those inputs. The 100 nF capacitor across the differential inputs acts as a low-pass filter in conjunction with the 10 kΩ resistor. The cutoff frequency of the low-pass filter is 80 Hz. Using these external components, the default acquisition time of 400 ns can be used, which allows a combined acquisition and conversion time of 1 µs.

CONVERTING CELL VOLTAGES AND AUXILIARY ADC INPUTS IN A CHAIN OF AD7280As

The AD7280A provides a daisy-chain interface that allows up to eight parts to be stacked without the need for individual isolation. One feature of the daisy-chain interface is the ability to initiate conversions on all parts in the daisy-chain stack with a single convert start command. The convert start command is transferred up the daisy chain, from the master device to each AD7280A in turn. The delay time between each AD7280A is t_{DELAY}, as shown in Figure 34. The maximum delay between the start of conversions on the master AD7280A and the last AD7280A device in the chain can be determined by multiplying t_{DELAY} by the number of slave AD7280As in the daisy chain. The total conversion time for all cell voltage and auxiliary ADC input conversions can be calculated using the following equation:

$$Total\ Conversion\ Time = ((t_{ACQ} + t_{CONV}) \times (Number\ of\ Conversions\ per\ Part)) - t_{ACQ} + ((N - 1) \times t_{DELAY})$$

where:

t_{ACQ} is the analog input acquisition time of the AD7280A (see Table 9).

t_{CONV} is the conversion time of the AD7280A, as specified in Table 3.

Number of Conversions per Part is the number of inputs selected for conversion (6, 9, or 12, as listed in Table 8), multiplied by the number of averages selected for each input (1, 2, 4, or 8).

N is the number of AD7280As in the daisy chain.

t_{DELAY} is the delay time when transferring the convert start command between adjacent AD7280A devices, as specified in Table 3.

The total conversion times calculated for three possible configurations of the AD7280A are included in Table 10.

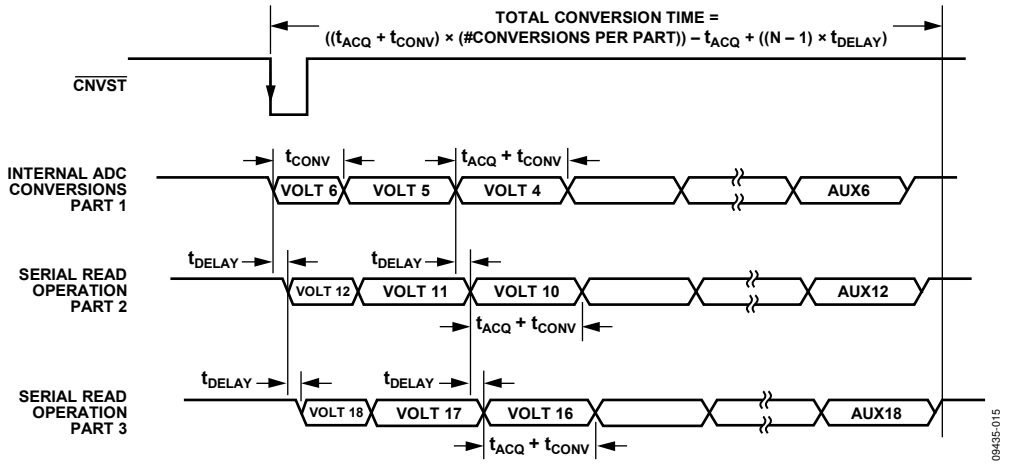

Figure 34. ADC Conversions and Readback on a Chain of Three AD7280As

Table 10. Calculated Conversion Times for Three Example AD7280A Configurations, T_A = −40°C to +85°C

Bits [D15:D14]	Bits [D10:D9]	Bits [D6:D5]	Configuration	Conversion Time per Part	Total Conversion Time per 48 Channel Stack
00	00	00	12 channels; t_{CONV} = 695 ns; t_{ACQ} = 465 ns; average = 0	13.46 µs	15.2 µs
		01	12 channels; t_{CONV} = 695 ns; t_{ACQ} = 1.01 µs; average = 0	19.45 µs	21.2 µs
		10	12 channels; t_{CONV} = 695 ns; t_{ACQ} = 1.46 µs; average = 0	24.4 µs	26.15 µs
		11	12 channels; t_{CONV} = 695 ns; t_{ACQ} = 1.89 µs; average = 0	29.13 µs	30.9 µs
10	00	00	6 channels; t_{CONV} = 695 ns; t_{ACQ} = 465 ns; average = 0	6.5 µs	8.23 µs
		01	6 channels; t_{CONV} = 695 ns; t_{ACQ} = 1.01 µs; average = 0	9.22 µs	10.97 µs
		10	6 channels; t_{CONV} = 695 ns; t_{ACQ} = 1.46 µs; average = 0	11.47 µs	13.22 µs
		11	6 channels; t_{CONV} = 695 ns; t_{ACQ} = 1.89 µs; average = 0	13.62 µs	15.37 µs
00	11	00	12 channels; t_{CONV} = 695 ns; t_{ACQ} = 465 ns; average = 8	110.9 µs	112.65 µs
		01	12 channels; t_{CONV} = 695 ns; t_{ACQ} = 1.01 µs; average = 8	162.67 µs	164.42 µs
		10	12 channels; t_{CONV} = 695 ns; t_{ACQ} = 1.46 µs; average = 8	205.42 µs	207.17 µs
		11	12 channels; t_{CONV} = 695 ns; t_{ACQ} = 1.89 µs; average = 8	246.27 µs	248.02 µs

CONVERSION WINDOW

As described in the Converting Cell Voltages and Auxiliary ADC Inputs section, the AD7280A converts the selected cell voltage and auxiliary ADC inputs in a defined sequence (see Figure 31). As described in the Circuit Information section, the AD7280A consists primarily of a high voltage input multiplexer, a low voltage input multiplexer, and a SAR ADC. The six cell voltage channels are presented to the ADC in turn by the high voltage multiplexer. Control is then handed to the low voltage multiplexer that allows the six auxiliary ADC channels to be converted. Following completion of all selected conversions, control is handed back to the high voltage multiplexer, and the AD7280A is ready to receive the next valid convert start command.

The conversion window of the AD7280A includes the actual conversion time for the selected channels (see Table 10), as well as the additional time required to return control to the high voltage multiplexer and configure it to start acquiring the cell voltage between VIN6 and VIN5. The conversion window defines the minimum time that should be allowed between successive convert start commands.

The conversion window for the AD7280A can be calculated using the following equation:

$$Conversion\ Window = Total\ Conversion\ Time + 80\ \mu s$$

where *Total Conversion Time* can be calculated for either a single device or for a chain of devices, as described in the Converting Cell Voltages and Auxiliary ADC Inputs section.

SELF-TEST CONVERSION

A self-test conversion can be initiated on the AD7280A, which allows the operation of the ADC and reference buffer to be verified. The self-test conversion is completed on the internal 1.2 V band gap reference voltage, and the voltage range for the conversion is 0 V to 5 V. The self-test conversion can be initiated on either a single AD7280A or on all AD7280As in the daisy chain simultaneously.

The conversion results can be read back though the read protocols defined in the Serial Interface section. The self-test conversion result typically varies between Code 970 and Code 990.

The self-test conversion can also be used to verify the operation of the alert outputs, as described in the Alert Output section.

CONNECTION OF FEWER THAN SIX VOLTAGE CELLS

The AD7280A provides six input channels for battery cell voltage measurement. The AD7280A can also be used in applications that require fewer than six voltage measurements. In these applications, care should be taken to ensure that the sum of the individual cell voltages still exceeds the minimum V_{DD} supply voltage. For this reason, the recommended minimum number of battery cells connected to each AD7280A is 4. Care should also be taken to ensure that the voltage on the VIN6 input is always greater than or equal to the voltage on the V_{DD} supply pin. For example, in an application with five battery cells connected to the AD7280A, the cell voltage on Cell 5 should be applied across VIN6 and VIN5, and the VIN4 and VIN5 inputs should be shorted together. Figure 35 shows an example of the battery connections to the AD7280A in a four-cell battery monitoring application.

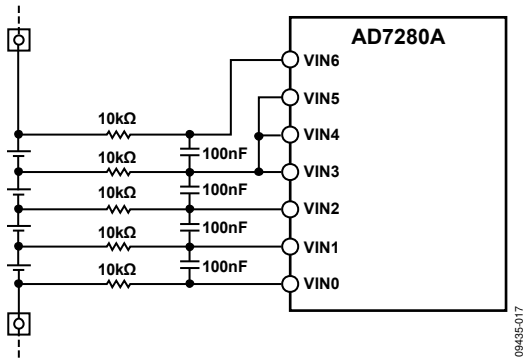

Figure 35. Typical Connections for a Four-Cell Application

Regardless of how many cell voltage measurements are required in the user application, the AD7280A acquires and converts the voltages on all six cell voltage input channels. The conversion data on all six voltage channels is supplied to the DSP/microprocessor using the SPI/daisy-chain interfaces. Users should ignore the conversion data that is not required in their application.

It is also possible to read back a single cell voltage conversion result from each device in the daisy chain. This can be done by programming the read register on each device to read back the required conversion result (see Example 4 in the Examples of Interfacing with the AD7280A section). However, as previously described, all six cell voltage channels are converted. When using the device in this mode, the overall conversion sample rate should be limited by the conversion window required for the number of channels selected by Bits[D15:D14] of the control register.

When using the alert function, the user should program the alert register to ensure that the shorted channels do not incorrectly trigger an alert output (see the Alert Output section).

AUXILIARY ADC INPUTS

The AD7280A provides six single-ended analog inputs to the ADC—AUX1 to AUX6—which can be used to convert the voltage output of a thermistor temperature measurement circuit. In the event that no temperature measurements are required or that individual cell temperature measurements are not required, the auxiliary ADC inputs can be used to convert any other 0 V to 5 V input signal.

The AD7280A can be programmed to complete conversions on all six auxiliary ADC channels, on three auxiliary ADC channels (AUX1, AUX3, and AUX5), or on none of the auxiliary ADC input channels. The number of conversions is programmed through Bits[D15:D14] of the control register. The number of conversion results supplied by the AD7280A for readback by the DSP/microprocessor is programmed through Bits[D13:D12] of the control register. It is also possible to read back a single auxiliary ADC conversion result from each device in the daisy chain. This can be done by programming the read register on each device to read back the required conversion result (see Example 4 in the Examples of Interfacing with the AD7280A section). If the device is used in this mode, the overall conversion sample rate should be limited by the conversion window required for the number of channels selected by Bits[D15:D14] of the control register.

In an application where the alert function is used but only one or two auxiliary ADC inputs are required, the AD7280A should first be programmed to complete and read back only three auxiliary ADC conversions by setting Bits[D15:D12] of the control register to 0101. Channel AUX5 and Channel AUX3 can be removed from the alert detection by writing to Bits[D1:D0] of the alert register (see Table 12 in the Alert Output section).

Thermistor Termination Input

If thermistor circuits are used to measure each individual cell temperature, the thermistor termination pin, AUX_{TERM}, can be used to terminate the thermistor inputs for each auxiliary ADC input measurement. This reduces the termination resistor requirement from six resistors to one. Bit D3 in the control register should be set to 1 when using the AUX_{TERM} input.

Note that, due to settling time requirements, the thermistor termination resistor option should only be used when the acquisition time of the AD7280A is set to its highest value (1.6 µs). The acquisition time is configured by setting Bits[D6:D5] of the control register (see Table 9).

In Figure 36, the termination resistor is placed between V_{SS} and AUX_{TERM}. The AUX_{TERM} input can be used to terminate the thermistor inputs to the high or low voltage of the thermistor circuit.

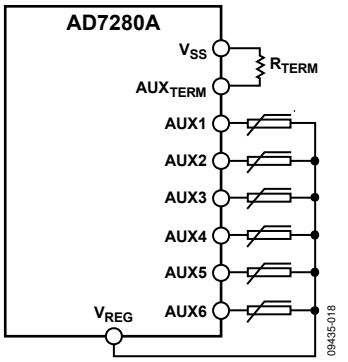

Figure 36. Typical Circuit Using the Thermistor Termination Resistor

POWER REQUIREMENTS

The current consumed by the AD7280A in normal operation, that is, when not in power-down mode, is dependent on the mode in which the part is being operated. The three distinct modes of operation can be described as follows:

- Voltage and auxiliary ADC input conversion
- AD7280A configuration and data readback
- Cell balancing

The AD7280A consumes its highest level of current while converting voltage and/or auxiliary ADC inputs to digital outputs. Depending on the configuration of the AD7280A, the conversion time can be as little as 6 µs. The typical current required by the AD7280A during conversion is 6.9 mA (see Table 2).

When configuring a chain of AD7280As or when reading back the voltage and/or auxiliary ADC conversion results from a chain of AD7280As, the current required for each AD7280A is typically 6.5 mA (see Table 2). The time required to read back the voltage conversions results from 48 lithium ion cells depends on the speed of the interface clock used, that is, SCLK, but it can be as low as 1.54 ms.

The typical current consumed by the AD7280A when the cell balance outputs are switched on is 6.4 mA (see Table 2). The length of time for which the cell balance outputs are switched on is defined by the user.

When the AD7280A is not being used in any of the aforementioned modes of operation, it is recommended that the device be powered down, as described in the Power-Down section. This significantly reduces the current drawn by each AD7280A in the chain, which avoids unnecessary draining of the lithium ion cells and aids in current matching between devices across the full battery stack.

POWER-DOWN

The AD7280A provides two power-down options.

- Full power-down (hardware)
- Software power-down

Full Power-Down (Hardware)

The AD7280A can be placed into full power-down mode, which requires only 5 µA maximum current, by taking the $\overline{PD}$ pin low. The falling edge of the $\overline{PD}$ pin powers down all analog and digital circuitry.

The AD7280A includes a digital delay filter on the $\overline{PD}$ pin, which protects against a power-down being initiated by noise or glitches on the hardware $\overline{PD}$ pin. A hardware power-down is not initiated until the $\overline{PD}$ pin is held low for approximately 130 µs. Similarly, the AD7280A is not taken out of power-down mode until the $\overline{PD}$ pin is held high for approximately 130 µs. The digital delay filter does not apply on initial power-up. The power-on request is accepted by the AD7280A approximately 5 µs after the rising edge of $\overline{PD}$.

When placing the AD7280A into full power-down mode, AV_{CC} and DV_{CC} must fall to 0 V and must not be held high by any external means. AV_{CC} and DV_{CC} can be held high unintentionally if the auxiliary ADC inputs are greater than the forward bias on the internal ESD protection diodes. For this reason, it is recommended that the auxiliary ADC inputs return to 0 V when the part is placed in full power-down mode.

In addition, all digital inputs on the AD7280A master device must return to 0 V when the part is placed in full power-down mode (see Figure 37). However, if an external V_{DRIVE} supply is used—that is, V_{DRIVE} is not connected to V_{REG}—then only the $\overline{CNVST}$ line must return low (see Figure 38).

When the AD7280A is placed into full power-down mode, the device must be left in full power-down for a minimum of 2 ms when the V_{REG} and V_{REF} pins are decoupled with 1 µF capacitors. This ensures that the charge on the V_{REG} and V_{REF} decoupling capacitors dissipates sufficiently to allow the internal power-on reset circuit to activate when powering the AD7280A back up.

This time is measured from the falling edge of the $\overline{PD}$ pin. Figure 18 shows a plot of the voltage on the V_{REG} and V_{REF} pins as the AD7280A is powering down with 1 µF decoupling capacitors on the pins. Figure 20 shows a similar plot but with 10 µF decoupling capacitors on the V_{REG} and V_{REF} pins.

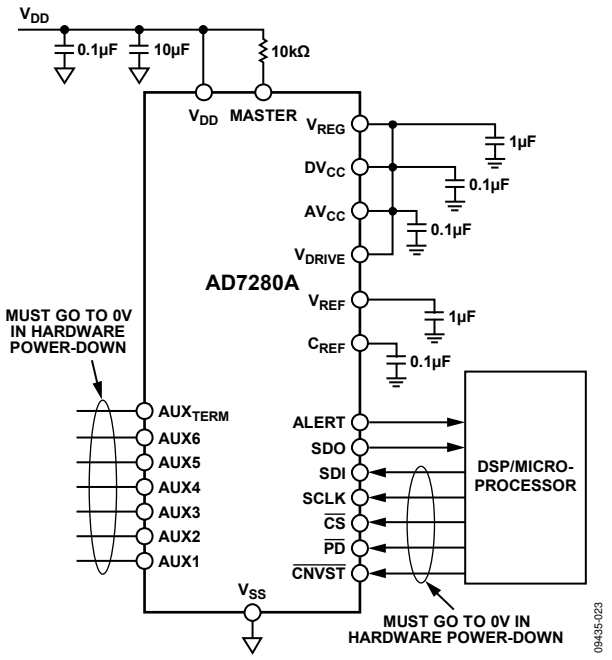

Figure 37. V_{DRIVE} Powered from V_{REG}

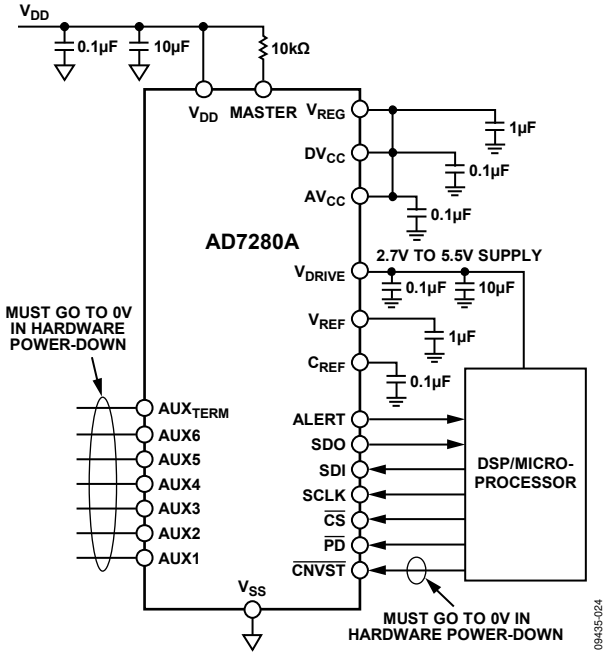

Figure 38. V_{DRIVE} Powered from DSP/Microprocessor