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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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12-Bit Power Amplifier Current Controller with ADC, DACs, Temperature and Current Sensors

Data Sheet **AD7293**

FEATURES

- 4 closed-loop power amplifier (PA) drain current controllers
- Built-in PA protection, sequencing, and alert features
- Compatible with both depletion mode and enhancement mode power amplifiers
- Highly integrated
  - 4 uncommitted 12-bit analog-to-digital converter (ADC) inputs
    - ±0.5 LSB typical integral nonlinearity (INL)
  - Eight 12-bit voltage digital-to-analog converters (DACs)
    - 1.3 µs maximum settling
  - 4 high-side current sense amplifiers, ±0.1% gain error
  - 2 external temperature sensor inputs, ±1.1°C accuracy
  - Internal temperature sensor, ±1.25°C accuracy
  - 2.5 V on-chip reference
- Flexible monitoring and control ranges
  - ADC input ranges: 0 V to 1.25 V, 0 V to 2.5 V, and 0 V to 5 V
  - Bipolar DAC ranges: 0 V to +5 V, −4 V to +1 V, and −5 V to 0 V
  - Bipolar DAC reset and clamping relative to V_{CLAMPx} voltage
  - Unipolar DAC ranges: 0 V to 5 V, 2.5 V to 7.5 V, and 5 V to 10 V
  - Current sense gain: 6.25, 12.5, 25, 50, 100, and more
  - Adjustable closed-loop setpoint ramp time
- High-side voltage current sensing
  - 4 current sense inputs
    - 4 V to AV_{SS} + 60 V, ±200 mV input range
- Small package and flexible interface
  - Serial port interface (SPI) with V_{DRIVE} supporting 1.8 V, 3 V, and 5 V interfaces
  - 56-lead LFCSP
- Temperature range: −40°C to +125°C

APPLICATIONS

- GaN and GaAs power amplifier monitoring and controls
- Base station power amplifiers
- General-purpose system monitoring and controls

GENERAL DESCRIPTION

The AD7293 is a PA drain current controller containing functionality for general-purpose monitoring and control of current, voltage, and temperature, integrated into a single chip solution with an SPI-compatible interface.

The device features a 4-channel, 12-bit successive approximation register (SAR) ADC, eight 12-bit DACs (four bipolar and four unipolar with output ranges that can be configured to shut down under external pin control), a ±1.25°C accurate internal temperature sensor, and eight general-purpose input/output (GPIO) pins.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

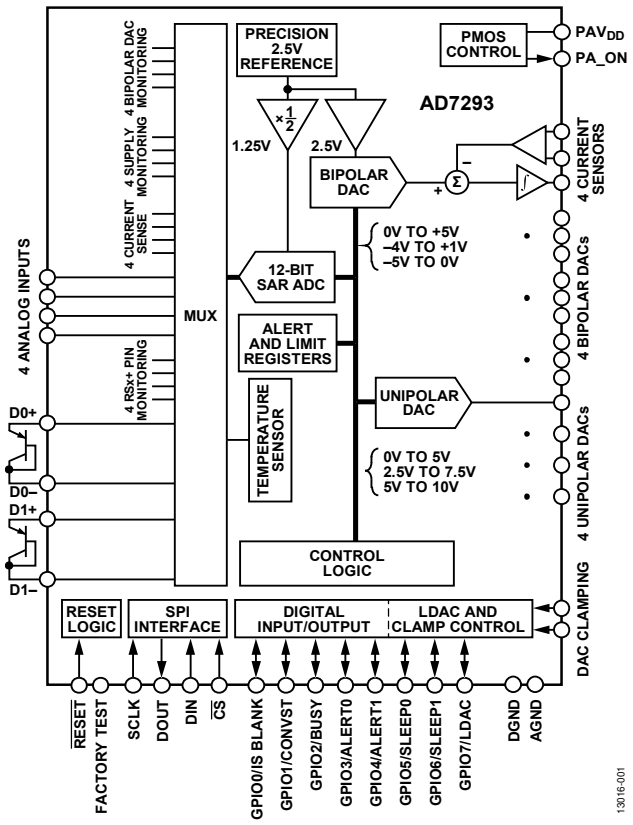

Figure 1.

The device also includes limit registers for alert functions and four high-side current sense amplifiers to measure current across external shunt resistors. These amplifiers can be optionally set to operate as part of four independent closed-loop drain current controllers.

A high accuracy 2.5 V internal reference is provided to drive the DACs and the ADC. The 12-bit ADC monitors and digitizes the internal temperature sensor, and two inputs are included for the external diode temperature sensors.

Note that throughout this data sheet, multifunction pins, such as GPIO4/ALERT1, are referred to either by the entire pin name or by a single function of the pin, for example, ALERT1, when only that function is relevant.

PRODUCT HIGHLIGHTS

1. Four independent closed-loop drain current controllers.
2. Built-in monitoring, sequencing, and alert features.
3. Compatible with both depletion mode and enhancement mode power amplifiers.

Rev. A Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

AD7293* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7293 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1361: AD7293 Closed-Loop for Power Amplifier Drain Current Control

Data Sheet

- AD7293: 12-Bit Power Amplifier Current Controller with ADC, DACs, Temperature and Current Sensors Data Sheet

User Guides

- UG-817: Evaluating the AD7293 12-Bit Power Amplifier Current Controller with ADC, DACs, Temperature and Current Sensors

DESIGN RESOURCES

- AD7293 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7293 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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REVISION HISTORY

6/2016—Revision A: Initial Version

FUNCTIONAL BLOCK DIAGRAMS

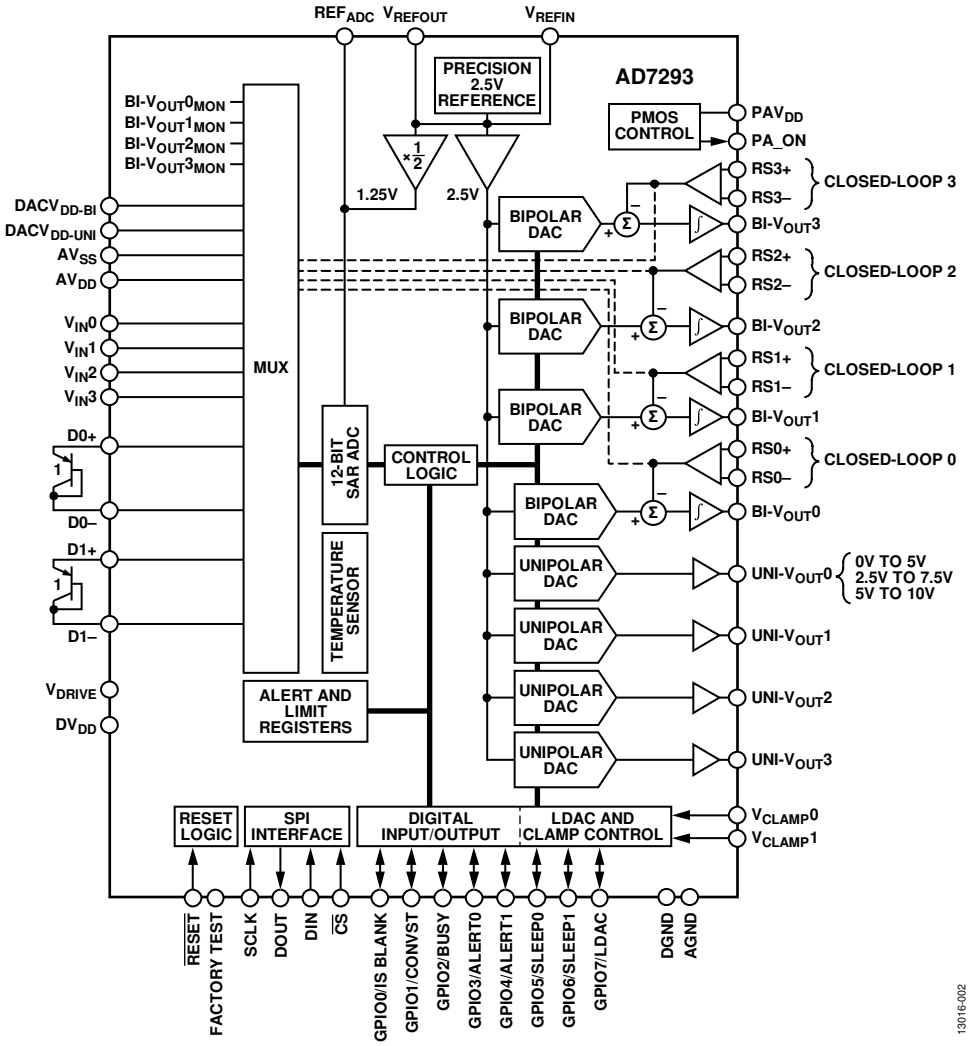

Figure 2. Closed-Loop Functional Block Diagram

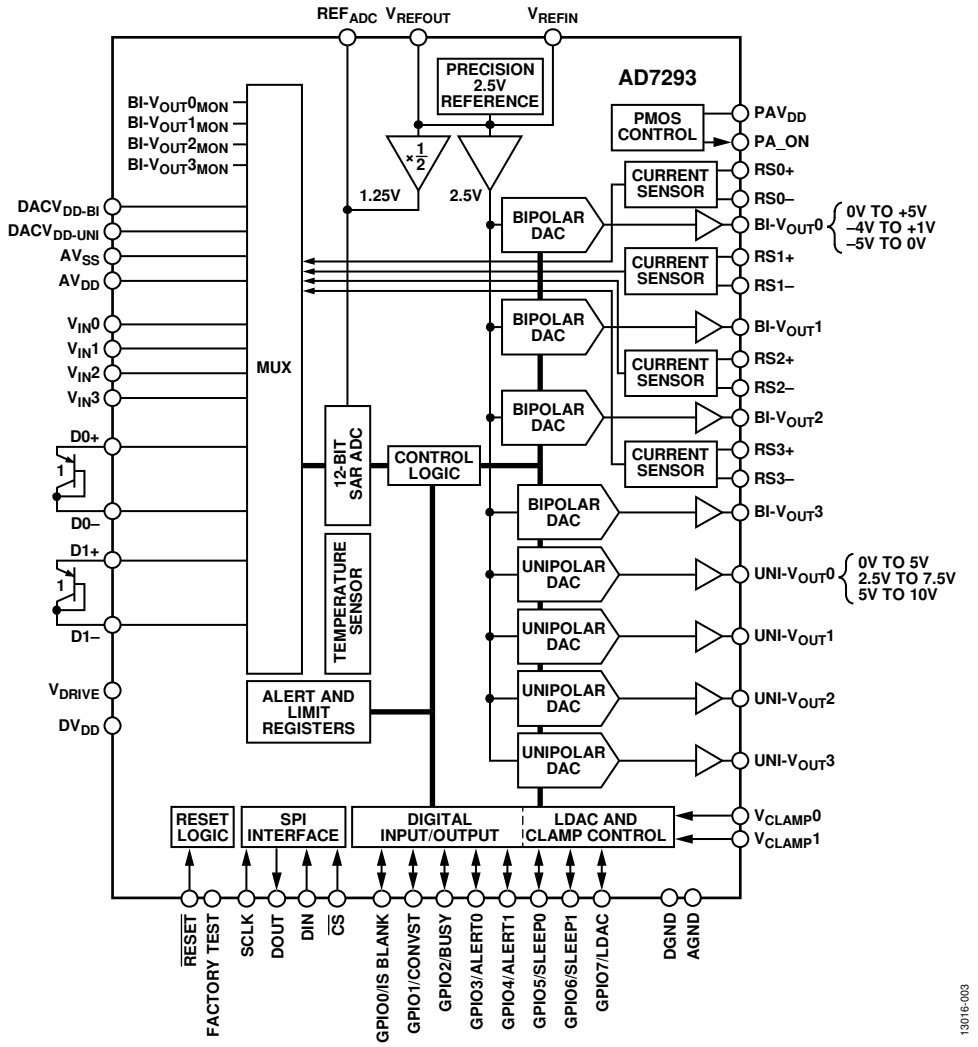

Figure 3. Open-Loop Functional Block Diagram

SPECIFICATIONS

ADC

AV_{DD}, DV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-UNI}$ = 5 V, AV_{SS} = −5 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external; V_{DRIVE} = 1.7 V to 5.5 V; T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC ACCURACY					
Resolution		12		Bits	
Integral Nonlinearity (INL)		±0.5	±1	LSB	
Differential Nonlinearity (DNL)		±0.5	±0.99	LSB	No missing codes
Single-Ended Mode					
Zero Code Error		±0.4	±2.5	LSB	
Zero Code Error Mismatch		±0.6		LSB	
Full-Scale Error			±6.5	LSB	
Full-Scale Error Mismatch		±1.5		LSB	
Differential Mode					
Gain Error		±3	±6.5	LSB	
Gain Error Mismatch		±1.5		LSB	
Zero Code Error		±0.5	±2	LSB	
Zero Code Error Mismatch		±0.6		LSB	
DYNAMIC PERFORMANCE					f_{IN} = 1 kHz sine wave; single-ended mode; 0 V to 4 × REF_{ADC}
Signal-to-Noise Ratio (SNR)[1, 2]		72		dB	
Signal-to-Noise + Distortion (SINAD) Ratio[1, 2]		72		dB	
Total Harmonic Distortion (THD)[1, 2]		−90.5		dB	
Channel to Channel Isolation[2]		95		dB	f_{IN} = 100 Hz to 80 kHz
Full Power Bandwidth[2]		7		MHz	At 0.1 dB; single-ended mode; 0 V to 4 × REF_{ADC}
CONVERSION RATE					
Conversion Time[2]		500		ns	
Track-and-Hold Acquisition Time[2]		100		ns	Voltage inputs in command mode
ANALOG INPUT[1]					REF_{ADC} = 1.25 V
Single-Ended Input Range	0		1.25	V	0 V to REF_{ADC} mode
	0		2.5	V	0 V to 2 × REF_{ADC} mode
	0		5	V	0 V to 4 × REF_{ADC} mode
Pseudo Differential Range ($V_{IN+} - V_{IN-}$[3])	0		1.25	V	0 V to REF_{ADC} mode
	0		2.5	V	0 V to 2 × REF_{ADC} mode
	0		5	V	0 V to 4 × REF_{ADC} mode
Differential Range ($V_{IN+} - V_{IN-}$)[4]	−1.25		+1.25	V	0 V to REF_{ADC} mode
	−2.5		+2.5	V	0 V to 2 × REF_{ADC} mode
	−5		+5	V	0 V to 4 × REF_{ADC} mode
Input Capacitance[2]		30		pF	
DC Input Leakage Current			±1	μA	
INTERNAL BI-V_{OUT}x MONITORING INPUTS					
Full-Scale Input Range	−5		+5	V	
Resolution		12		Bits	LSB step size ≈ 2.5 mV
Gain Error		±0.53		%	
Offset Error		±14		mV	
INTERNAL RSx+ MONITORING INPUTS					
Full-Scale Input Range	0		62.5	V	
Resolution		12		Bits	LSB step size ≈ 15.2 mV
Gain Error		0.06		%	
Offset Error		±11		mV	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INTERNAL SUPPLY MONITORING INPUTS					.
AV_{DD}					
Gain Error		±0.33		%	
Offset Error		±52		mV	
AV_{SS}					
Gain Error		±0.53		%	
Offset Error		±14		mV	
$DACV_{DD-UNI}$					
Gain Error		±0.16		%	
Offset Error		±12		mV	
$DACV_{DD-BI}$					
Gain Error		±0.33		%	
Offset Error		±52		mV	
INTERNAL REFERENCE[2]					
Reference Output Voltage	2.495	2.5	2.505	V	At T_A = 25°C only
Reference Temperature Coefficient		±10	±30	ppm/°C	
EXTERNAL REFERENCE					
Reference Input Voltage Range	2.48	2.5	2.52	V	
DC Input Leakage Current			±2	µA	

[1] See the Analog-to-Digital Converter (ADC) Overview section for more details.
[2] Guaranteed by design and characterization; not production tested.
[3] V_{IN-} = 0 V for specified performance.
[4] V_{IN+} and V_{IN-} must remain within GND and AV_{DD}.

DAC

AV_{DD}, DV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-UNI}$ = 5 V, AV_{SS} = −5 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external; V_{DRIVE} = 1.7 V to 5.5 V; T_A = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY[1]					
Resolution	12			Bits	
Integral Nonlinearity (INL)		±1	±1.7	LSB	Bipolar
			±3		Unipolar
		±1		LSB	Load current ±10 mA within 300 mV of supply
Differential Nonlinearity (DNL)	−0.99	±0.3	+1	LSB	Guaranteed monotonic
Full-Scale (FS) Error		±2.5		mV	All 1s loaded to DAC register, no load applied
		±0.65		% of FS	10 mA load applied
Offset Error		±10		mV	Unipolar, 2.5 V to 7.5 V range, 5 V to 10 V range
			±10	mV	Unipolar, 0 V to 5 V range
		±2.5	±12	mV	Bipolar
Offset Error Temperature Coefficient		±8		µV/°C	Measured in the linear region, T_A = 25°C
Gain Error			±0.15	% FSR	Bipolar
			±0.4	% FSR	Unipolar
Gain Error Temperature Coefficient		±3		ppm/°C	
DAC OUTPUT CHARACTERISTICS					
Bipolar Open-Loop DAC Range	0		5	V	BI-V_{OUT}0, BI-V_{OUT}1, BI-V_{OUT}2, and BI-V_{OUT}3
	−4		+1	V	
	−5		0	V	
Unipolar DAC Range	0		5	V	UNI-V_{OUT}0, UNI-V_{OUT}1, UNI-V_{OUT}2, and UNI-V_{OUT}3
	2.5		7.5	V	
	5		10	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Unipolar DAC Short-Circuit Current		40		mA	Shorted to AGND or $DACV_{DD-UNI}$
Bipolar DAC Short-Circuit Current		42		mA	Shorted to AV_{SS} or $DACV_{DD-BI}$
Load Current[2]	−10		+10	mA	Source and/or sink within 300 mV of supply
Capacitive Load Stability		10		nF	$R_L = \infty$
DC Output Impedance		1		Ω	Midscale
AC CHARACTERISTICS					
Output Voltage Settling Time[2]		1.2	1.3	µs	¼ to ¾ change within ±1 LSB, measured from the last SCLK rising edge, C_L = 200 pF
Slew Rate[2]		7.5		V/µs	
Digital Feedthrough[2]		0.1		nV-sec	
DAC to DAC Crosstalk[2, 3]		0.2		nV-sec	
Output Noise Spectral Density[2, 3]		55		nV/√Hz	f_{IN} = 10 kHz, bipolar
		110		nV/√Hz	f_{IN} = 10 kHz, unipolar
Output Noise[2, 3]		102		µV p-p	Bipolar
		135		µV p-p	Unipolar
CLAMP INPUTS					Controlled by SLEEP0 and SLEEP1 digital pins
Clamp Output Voltage[2]		−3 × $V_{CLAMP}0$, $V_{CLAMP}1$		V	BI-$V_{OUT}x = -3 \times V_{CLAMP}0, V_{CLAMP}1$
Gain Error		0.2		%	Within 200 mV of AV_{SS}
Input Referred Offset Error		5		mV	
$V_{CLAMP}0$ and $V_{CLAMP}1$ Input Current		±1		µA	
Clamp Voltage Range	AV_{SS}		0	V	
Output Current[2]	−10		+10	mA	Source and/or sink within 300 mV of supply
Clamp to Open-Loop Settling Time[2]			5	µs	$R_L = \infty$, C_L = 200 pF, output voltage within 10%, 5 V transition

[1] Specification tested with output unloaded. Linearity calculated using best fit line method and based on a reduced code range equivalent to 100 mV within either side of supply or ground ± 82 codes.
[2] Guaranteed by design and characterization; not production tested.
[3] All unipolar DACs must be enabled with an output code set to a minimum code of 41 LSBs.

TEMPERATURE SENSOR

AV_{DD}, DV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-UNI}$ = 5 V, AV_{SS} = −5 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external; V_{DRIVE} = 1.7 V to 5.5 V; T_A = −40°C to +125°C, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INTERNAL TEMPERATURE SENSOR[1]					
Operating Range[2]	−40		+125	°C	See Figure 30 for −55°C to +125°C operation
Accuracy		±1.25	±3	°C	Internal temperature sensor, T_A = −40°C to +125°C
		±1.25		°C	T_A = 25°C
Resolution		0.125		°C	
EXTERNAL TEMPERATURE SENSOR[1]					External transistor = 2N3906; no capacitor between Dx−/Dx+ pins, and no series resistor between transistor and Dx−/Dx+ pins
Operating Range	−55		+150	°C	Limited by external transistor
Accuracy		±1.1	±3	°C	T_A = −40°C to +105°C
Resolution		0.125		°C	LSB size

[1] Guaranteed by design and characterization; not production tested.
[2] Guaranteed functional to −55°C by design but accuracy is not guaranteed.

CURRENT SENSOR

AV_{DD}, DV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-UNI}$ = 5 V, AV_{SS} = −5 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external; V_{DRIVE} = 1.7 V to 5.5 V; T_A = −40°C to +125°C, gain = 6.25, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT SENSE					RSx+ = AV_{DD} to AV_{SS} + 60 V
Common-Mode Input Voltage Range	4		60	V	AV_{SS} = 0 V
	4		55	V	AV_{SS} = −5 V
Differential Input Voltage Range	−200		+200	mV	Gain = 6.25, for gain settings, see Table 44
Gain Error		±0.1	±0.7	%	
Gain Error Temperature Coefficient		−16		ppm/°C	
Offset Error (Referred to Input, RTI)			±200	µV	
Offset Error Drift		1		µV/°C	
DC Common-Mode Rejection	100	140		dB	
RSx+[1] Pin Input Current		105		µA	
RSx−[1] Pin Input Current		10		nA	
Differential Input Resistance[2]		700		kΩ	

[1] Where x is 0, 1, 2, or 3.
[2] Guaranteed by design and characterization; not production tested.

CLOSED-LOOP SPECIFICATIONS

AV_{DD}, DV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-UNI}$ = 5 V, AV_{SS} = −5 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external; V_{DRIVE} = 1.7 V to 5.5 V; T_A = −40°C to +125°C, unless otherwise noted. Power amplifier transconductance = 1 S to 5 S, and external gate filter time constant (τ_G) = 5 µs to 50 µs.

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
NORMAL OPERATION[1, 2]					
Setpoint Resolution		12		Bits	Equivalent to 200 mV/4096 = 49 µV at the current sense input
Sense Resistor Voltage Range	0		200	mV	
Setpoint Gain Error		±0.5		%	
Setpoint Offset Error (RTI)		±100		µV	Referred to current sense input; see Figure 31
Integrator Time Constant[3]		840		µs	Programmable; see Table 50
Closed-Loop Update Rate[3]		59.6		kHz	
Capacitive Load Stability		1		µF	5 Ω series resistance
Closed-Loop to Clamp Settling Time		1		µs	Within ±10%
Bipolar Closed-Loop Output Range	AV_{SS}		AV_{DD}	V	See the Bipolar DAC (BI-VOUTx) Offset Registers (Register 0x34 to Register 0x37) section
Integrator Programmable Voltage Limit Resolution		2.5		mV	See the Closed-Loop Integrator Programmable Voltage Limit section
START SEQUENCING PA_ON CONTROL[2]					
PA_ON Pin Output Voltage	AGND		PAV_{DD}	V	
PA_ON Off State Enable			500	µs	Measured from AV_{SS} failure event, C_L = 1 nF
			500	µs	Measured from SLEEP0 or SLEEP1 pin, 0 to 1 transition, C_L = 1 nF
PA_ON On State Enable			500	µs	Measured from SLEEP1 to SLEEP0 transition, C_L = 1 nF
PA_ON Short-Circuit Current		±10		mA	
PA_ON Resistance		250		Ω	
AV_{DD}/AV_{SS} ALARM					
AV_{DD} Alarm Threshold	3.2	3.6	3.9	V	
AV_{SS} Alarm Threshold	−3.8	−4.1	−4.4	V	

[1] Power amplifier characteristic dependent.
[2] Guaranteed by design and characterization; not production tested.
[3] Expressed as a function of the internal oscillator frequency.

GENERAL

DV_{DD}, AV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-BI}$ = 5 V, AV_{SS} = −5 V, RSx+ = AV_{DD} to 55 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external, V_{DRIVE} = 1.7 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS						
Input Voltage						
High	V_{IH}	$0.8 \times V_{DRIVE}$			V	
Low	V_{IL}			$0.2 \times V_{DRIVE}$	V	
Input Leakage Current	I_{IN}		±1		µA	
Input Capacitance	C_{IN}		3		pF	
LOGIC OUTPUTS[1]						GPIO0/IS BLANK, GPIO1/CONVST, GPIO2/BUSY, GPIO3/ALERT0, and GPIO4/ALERT1 are open-drain outputs
Output Voltage						
High	V_{OH}			0.4	V	I_{SINK} = 3 mA
Low	V_{OL}			0.6	V	I_{SINK} = 6 mA
Floating-State Leakage Current				±1	µA	
Floating-State Output Capacitance			8		pF	
GENERAL-PURPOSE OUPUTS						
Output Voltage						
High	V_{OH}			V_{DRIVE} − 0.2	V	I_{SINK}/I_{SOURCE} = 1 mA
Low	V_{OL}			0.4	V	I_{SINK}/I_{SOURCE} = 1 mA
POWER REQUIREMENTS						
Supply Voltages						
Positive Analog	AV_{DD}	4.5		5.5	V	
Negative Analog	AV_{SS}	−5.5		−4.5 or 0	V	
Logic Power	V_{DRIVE}	1.7		5.5	V	Supports 1.8 V, 3 V, and 5 V interfaces
Unipolar DAC	$DACV_{DD-UNI}$	4.5		12.5	V	
Bipolar DAC	$DACV_{DD-BI}$	4.5		5.5	V	
PA_ON Power	PAV_{DD}	4.5		AV_{SS} + 60	V	
RSx+ Voltage	V_{RSx+}	4		AV_{SS} + 60	V	
Supply Currents						All power supplies set to maximum voltage; ADC on and converting; DACs enabled with no load applied
AV_{DD}	AI_{DD}		9	12.5	mA	
AV_{SS}	AI_{SS}		−4.4	−5.4	mA	
V_{DRIVE}	I_{DRIVE}		1	2.1	mA	
$DACV_{DD-UNI}$	$DACI_{DD-UNI}$		2.1	3	mA	
$DACV_{DD-BI}$	$DACI_{DD-BI}$		5	8.2	mA	
PAV_{DD}	PAI_{DD}		81	100	µA	
Power Dissipation			110		mW	

[1] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

SPI Serial Interface

AV_{DD}, DV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-UNI}$ = 2.7 V to 16 V, AV_{SS} = 0 V, RSx+ = AV_{DD} to 55 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external, V_{DRIVE} = 1.7 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 7.

Parameter	Description	Limit at T_{MIN}/T_{MAX}		Unit
		V_{DRIVE} = 1.7 V to 2.7 V	V_{DRIVE} = 2.7 V to 5.5 V	
f_{SCLK}	Frequency of serial read clock[1]	8	15	MHz max
t_1	SCLK period	150	66.67	ns min
t_2	SCLK low	40	26	ns min
t_3	SCLK high	40	26	ns min
t_4	$\overline{CS}$ falling edge to SCLK rising edge	5	5	ns min
t_5	DIN setup time to SCLK rising edge	10	10	ns min
t_6[2]	DIN hold time after SCLK rising edge	10	10	ns max
t_7	Last SCLK rising edge to $\overline{CS}$ rising edge	5	5	ns min
t_8	$\overline{CS}$ high	12	10	ns min
t_9[3]	$\overline{CS}$ rising edge to next SCLK rising edge	1	1	ns min
t_{10}	SCLK falling edge to $\overline{CS}$ falling edge	1	1	ns min
t_{11}	SCLK falling edge to output data valid delay time from high impedance[4]	60	30	ns max
t_{12}	SCLK falling edge to output data valid delay time[4]	60	30	ns max
t_{13}	Last SCLK falling edge to DOUT high impedance[4]	20	20	ns typ
t_{14}	$\overline{CS}$ rising edge to DOUT high impedance[4]	25	15	ns max

[1] DOUT loaded with 10 pF for DOUT timing specifications.
[2] Time required for the output to cross 0.2 × V_{DRIVE} and 0.8 × V_{DRIVE} when V_{DRIVE} < 2.7 V; time required for the output to cross 0.3 × V_{DRIVE} and 0.7 × V_{DRIVE} when 2.7 ≤ V_{DRIVE} ≤5.5 V.
[3] Guaranteed by design and characterization; not production tested.
[4] MISO speed set to maximum in the general register.

Asynchronous Inputs

AV_{DD}, DV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-UNI}$ = 2.7 V to 16 V, AV_{SS} = 0 V, RSx+ = AV_{DD} to 55 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external, V_{DRIVE} = 1.7 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 8.

Parameter	Description	Limit at T_{MIN}/T_{MAX}		Unit
		V_{DRIVE} = 1.7 V to 2.7 V	V_{DRIVE} = 2.7 V to 5.5 V	
t_{15}[1]	Minimum LDAC pulse width	90	90	ns min
t_{16}	Minimum CONVST pulse width	90	90	ns min
t_{17}	Minimum IS BLANK pulse width	90	90	ns min
t_{18}	Minimum $\overline{RESET}$ pulse width	90	90	ns min

[1] Guaranteed by design and characterization; not production tested.

Timing Diagrams

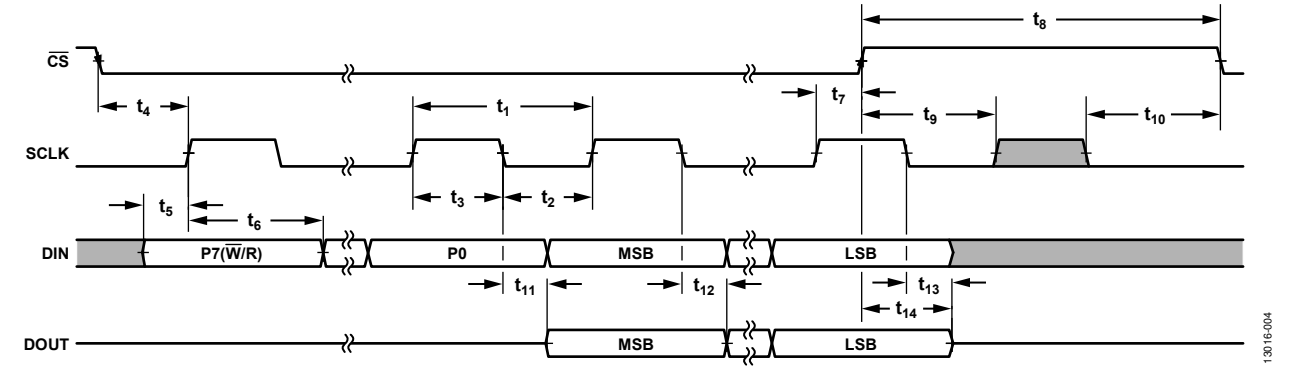

Figure 4. Serial Interface Timing Diagram

Figure 5. Asynchronous Inputs

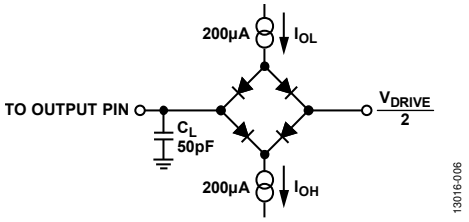

Figure 6. Load Circuit for Digital Output (DOUT) Timing Specifications

ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Rating
±5 V Analog Output Pins (BI-V_{OUT}0, BI-V_{OUT}1, BI-V_{OUT}2, BI-V_{OUT}3) to AV_{SS}	AV_{SS} − 0.3 V to $DACV_{DD-BI}$ + 0.3 V
12.5 V Analog Output Pins (UNI-V_{OUT}0, UNI-V_{OUT}1, UNI-V_{OUT}2, UNI-V_{OUT}3) to AGND	−0.3 V to $DACV_{DD-UNI}$ + 0.3 V
12.5 V Supply ($DACV_{DD-UNI}$) to AGND	−0.3 V to +15 V
2 V Analog Pins (REF_{ADC}, D1−, D1+, D0−, D0+) to AGND	−0.3 V to +2 V
5 V Analog Pins (FACTORY TEST, V_{REFIN}, V_{REFOUT}, V_{CLAMP}0, V_{CLAMP}1, V_{IN}x[1]) to AGND	−0.3 V to AV_{DD} + 0.3 V
5 V Digital Pins (GPIO5/SLEEP0, GPIO6/SLEEP1, $\overline{RESET}$, GPIO7/LDAC, $\overline{CS}$, DOUT) to DGND	−0.3 V to V_{DRIVE} + 0.3 V
5 V Open-Drain Pins (GPIO4/ALERT1, SCLK, DIN, DV_{DD}, GPIO3/ALERT0, GPIO2/BUSY, GPIO1/CONVST, GPIO0/IS BLANK) to DGND	−0.3 V to +7 V
5 V Supply Pins[2] (V_{DRIVE}, $DACV_{DD-BI}$, AV_{DD}) to AGND	−0.3 V to +7 V
−5 V Supply Pin (AV_{SS}) to AGND	−7 V to +0.3 V
60 V Analog Pins (RSx−) to RSx+	(RSx+) − 0.3 V to (RSx+) + 0.3 V
60 V Digital Pin (PA_ON) to AGND	−0.3 V to PAV_{DD} + 0.3 V
60 V Supply Pins (RSx+, PAV_{DD}) to AGND	−0.3 V to AV_{SS} + 65 V
Ground Pins (DGND, AGND) to AGND	−0.3 V to +0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +125°C
Reflow Profile	J-STD 20 (JEDEC)
Maximum Junction Temperature	150°C
ESD Rating, All Pins	
Human Body Model (HBM)	2 kV
Field-Induced Charged Device Model (FICDM)	1 kV

[1] x = 0, 1, 2, or 3.
[2] Connect AV_{DD} and $DACV_{DD-BI}$ to the same potential.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a 4-layer JEDEC 2S2P type printed circuit board (PCB) with a thermal via, that is, a device soldered in a circuit board for surface-mount packages, per JESD51-7.

Table 10. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
56-Lead LFCSP	27	0.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

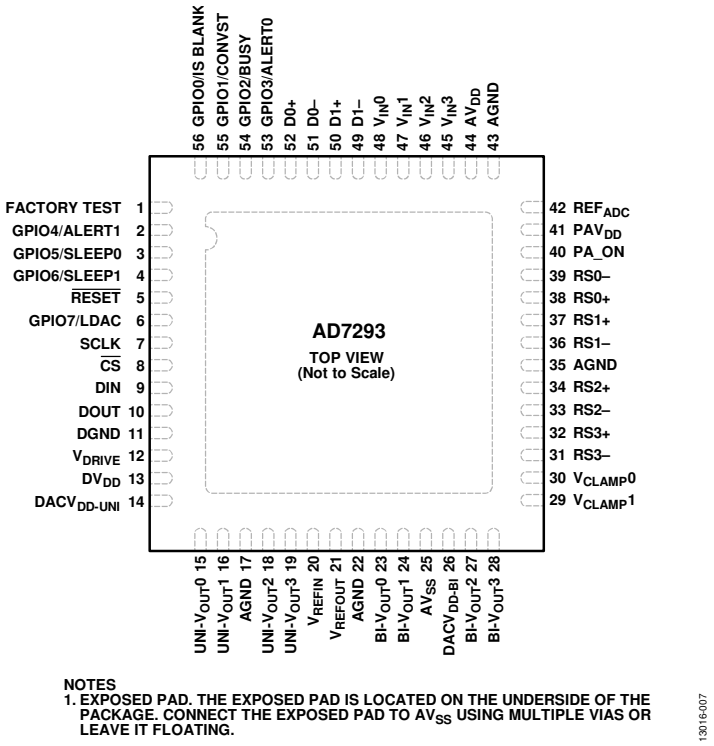

Figure 7. Pin Configuration

Table 11. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	FACTORY TEST	Factory Test Pin. Leave this pin unconnected, or connect it to DGND.
2	GPIO4/ALERT1	General-Purpose Input/Output 4 Pin (GPIO4, Default as Input). Alert 1 Pin (ALERT1, Default). When configured as an alert, this pin acts as an out of range indicator. The polarity of the pin is register selectable. This pin is an open-drain output, and requires a pull-up resistor connected to V_{DRIVE}.
3	GPIO5/SLEEP0	General-Purpose Input/Output 5 Pin (GPIO5, Default as Input). Sleep 0 Pin (SLEEP0). DAC power-down digital input pin (polarity is register selectable). This pin can be configured to trigger DAC clamping on any combination of DAC channels.
4	GPIO6/SLEEP1	General-Purpose Input/Output 6 Pin (GPIO6). Sleep 1 Pin (SLEEP1, Default). DAC power-down digital input pin (polarity is register selectable). This pin can be configured to trigger DAC clamping on any combination of DAC channels.
5	$\overline{\text{RESET}}$	Reset Input. Taking this pin low performs a hardware reset.
6	GPIO7/LDAC	General-Purpose Input/Output 7 Pin (GPIO7). DAC Load Pin (LDAC, Default). When this input is active, the DAC registers are updated. The polarity of this pin is register selectable. See the Load DAC (LDAC Pin) section for more information.
7	SCLK	SPI Serial Clock Input.
8	$\overline{\text{CS}}$	Chip Select Signal. This active low, logic input signal frames the serial data input.
9	DIN	SPI Serial Data Input. The serial data loaded into the registers is provided on this pin. Data is clocked into the device on the rising edge of SCLK.
10	DOUT	SPI Serial Data Output. The serial data read from the registers is provided on this pin. Data is clocked out on the falling edge of SCLK. DOUT is high impedance when it is not outputting data.
11	DGND	Digital Ground. DGND is the ground reference point for all digital circuitry. Refer all digital signals to DGND. Connect both the DGND and AGND pins to the ground plane of the system.
12	V_{DRIVE}	Drive Voltage Reference Level of the SPI Bus from 1.7 V to 5.5 V.
13	DV_{DD}	Digital Supply Voltage from 4.5 V to 5.5 V.

Pin Number	Mnemonic	Description
14	$DACV_{DD-UNI}$	DAC Positive Supply Pin for the Unipolar DAC Output Amplifiers on UNI-V_{OUT}0, UNI-V_{OUT}1, UNI-V_{OUT}2, and UNI-V_{OUT}3.
15, 16, 18, 19	UNI-V_{OUT}0, UNI-V_{OUT}1, UNI-V_{OUT}2, UNI-V_{OUT}3,	Unipolar DAC Outputs. The clamp and power-on reset voltage for these DACs is 0 V.
17, 22, 35, 43	AGND	Analog Ground. Connect both the AGND and DGND pins to the ground plane of the system.
20	V_{REFIN}	Reference Input to the Device. Connect this pin to an external reference voltage, or tie this pin to V_{REFOUT}.
21	V_{REFOUT}	2.5 V Reference Output. Connect to V_{REFIN} to operate in internal reference mode. An optional 10 nF capacitor is recommended between the reference output and AGND for noise filtering.
23, 24, 27, 28	BI-V_{OUT}0, BI-V_{OUT}1, BI-V_{OUT}2, BI-V_{OUT}3	Bipolar DAC Outputs in Open-Loop Mode and Integrator Outputs in Closed-Loop Mode. The clamp and power-on reset voltage for these DACs is dictated by the V_{CLAMP}x pins.
25	AV_{SS}	DAC Negative Supply Pin for the BI-V_{OUT}0, BI-V_{OUT}1, BI-V_{OUT}2, and BI-V_{OUT}3 DAC Output Amplifiers.
26	$DACV_{DD-BI}$	Analog Supply Pin for BI-V_{OUT}0, BI-V_{OUT}1, BI-V_{OUT}2, and BI-V_{OUT}3. Connect AV_{DD} and $DACV_{DD-BI}$ to the same potential.
29	V_{CLAMP}1	Power-On Reset and Clamp Voltage for BI-V_{OUT}2 and BI-V_{OUT}3.
30	V_{CLAMP}0	Power-On Reset and Clamp Voltage for BI-V_{OUT}0 and BI-V_{OUT}1.
31, 33, 36, 39	RS3−, RS2−, RS1−, RS0−	Negative Connection for External Shunt Resistors.
32, 34, 37, 38	RS3+, RS2+, RS1+, RS0+	Positive Connection for External Shunt Resistors.
40	PA_ON	Power Amplifier On. This pin drives an external, positive channel metal oxide semiconductor (PMOS) switch capable of turning on/off the drain current to a PA transistor. The maximum voltage is set by PAV_{DD} and limited to AV_{SS} + 60 V. The power amplifier is turned on when the output is low. The AV_{SS} and AV_{DD} supply alarms can be configured to automatically trigger PA_ON. An alert condition can be configured to trigger PA_ON. Additionally, PA_ON can be turned on/off by issuing a register write.
41	PAV_{DD}	Power Supply for the PA_ON Control Signal. This pin is limited to 4 V to AV_{SS} + 60 V.
42	REF_{ADC}	Internal ADC Reference Voltage. The output at this pin is half the reference value (V_{REFIN}), 1.25 V. Connect decoupling capacitors to this pin to decouple the reference buffer. For best performance, connect a 4.7 µF compensation capacitor between REF_{ADC} and AGND. For stability, the amplifier requires a minimum capacitance of 220 nF (X7R/C0G ceramic) connected between REF_{ADC} and AGND, located as close to the AD7293 as possible (no more than 1 Ω of interconnect resistance).
44	AV_{DD}	Supply Voltage for All of the Analog Circuitry on the AD7293. The operating range is 4.5 V to 5.5 V. Connect AV_{DD} and $DACV_{DD-BI}$ to the same potential.
45 to 48	V_{IN}3, V_{IN}2, V_{IN}1, V_{IN}0	ADC Analog Inputs. Unused inputs must not be left floating. The input range of these pins is register selectable: 0 V to 1.25 V, 0 V to 2.5 V, or 0 V to 5 V.
49, 50, 51, 52	D1−, D1+, D0−, D0+	Temperature Sensor Analog Inputs. Connect these pins to the external temperature sensing transistor. Tie these pins to AGND if unused.
53	GPIO3/ALERT0	General-Purpose Input/Output 3 Pin (GPIO3, Default as Input). Alert 0 Pin (ALERT0). When ALERT0 is configured as an alert, this pin acts as an out of range indicator. Open-drain output whether in GPIO mode or alert mode. The polarity of this pin is register selectable. A pull-up resistor connected to V_{DRIVE} is required.
54	GPIO2/BUSY	General-Purpose Input/Output 2 Pin (GPIO2, Default as Input). Busy Pin (BUSY). When BUSY is configured as a busy output, this pin becomes active when a conversion is in progress. Open-drain output whether in GPIO mode or busy mode. The polarity of this pin is register selectable. A pull-up resistor connected to V_{DRIVE} is required.
55	GPIO1/CONVST	General-Purpose Input/Output 1 Pin (GPIO1, Default as Input). This pin is an open-drain output in GPIO mode. The polarity of this pin is register selectable. ADC External Convert Start Input Pin (CONVST). CONVST triggers conversions via this pin. The CONVST pin is useful for synchronizing the ADC sampling instant with an external source. A pull-up resistor connected to V_{DRIVE} is required in GPIO mode or if unused.
56	GPIO0/IS BLANK	General-Purpose Input/Output 0 Pin (GPIO0, Default as Input). This pin is an open-drain output in GPIO mode. The polarity of this pin is register selectable. A pull-up resistor connected to V_{DRIVE} is required in GPIO mode or if unused. Current Sensor Conversion Blank Pin (IS BLANK). This pin can blank current sensor conversions and the polarity of this pin is register selectable.
	EPAD	Exposed Pad. The exposed pad is located on the underside of the package. Connect the exposed pad to AV_{SS} using multiple vias or leave it floating.

TYPICAL PERFORMANCE CHARACTERISTICS

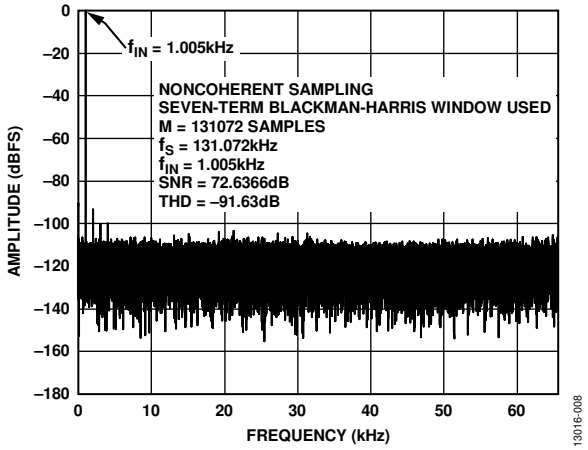

Figure 8. Signal-to-Noise Ratio, Single-Ended Input, 2 × REF_{ADC} Range

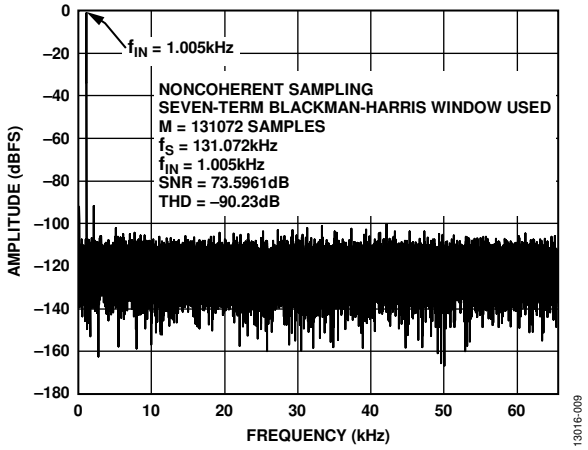

Figure 9. Signal-to-Noise Ratio, Differential Input, REF_{ADC} Range

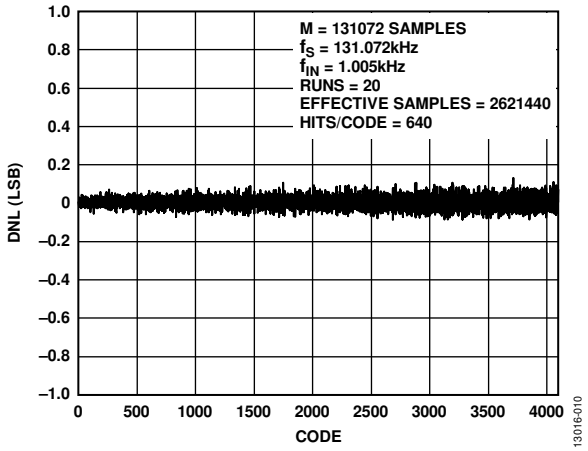

Figure 10. ADC DNL Single-Ended, REF_{ADC} Range

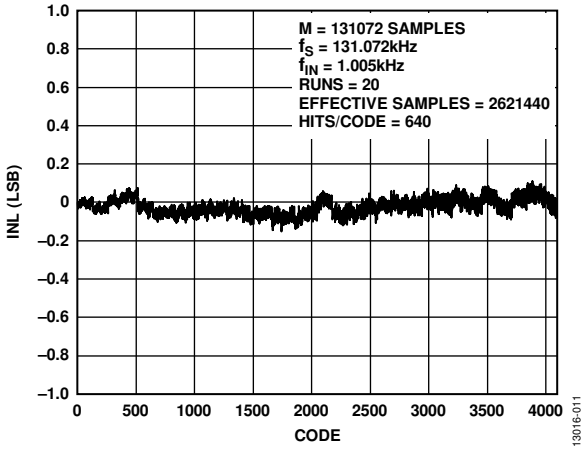

Figure 11. ADC INL Single-Ended, REF_{ADC} Range

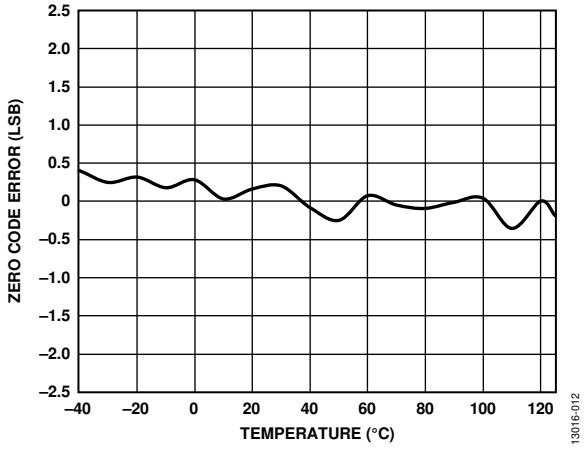

Figure 12. ADC Zero Code Error vs. Temperature

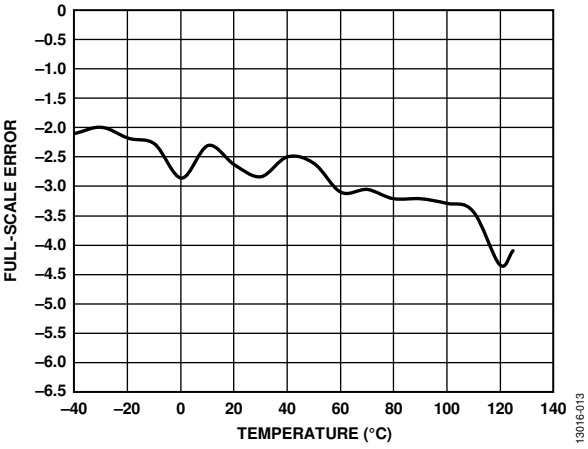

Figure 13. ADC Full-Scale Error vs. Temperature

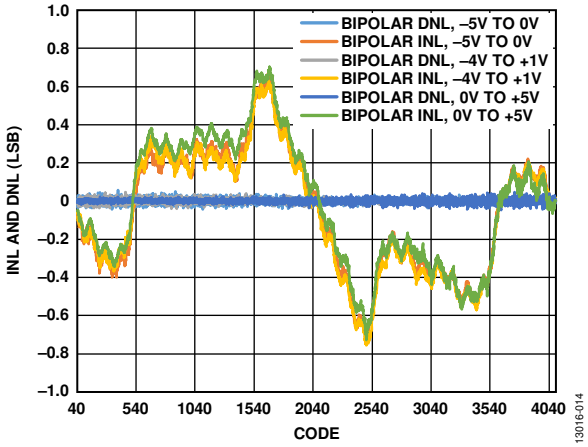

Figure 14. Bipolar DAC INL and DNL

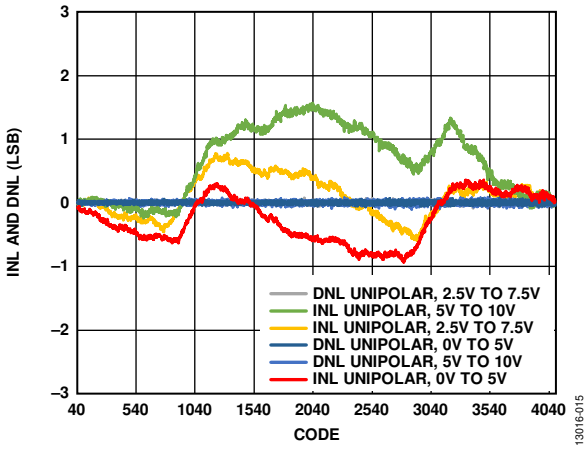

Figure 15. Unipolar DAC INL and DNL

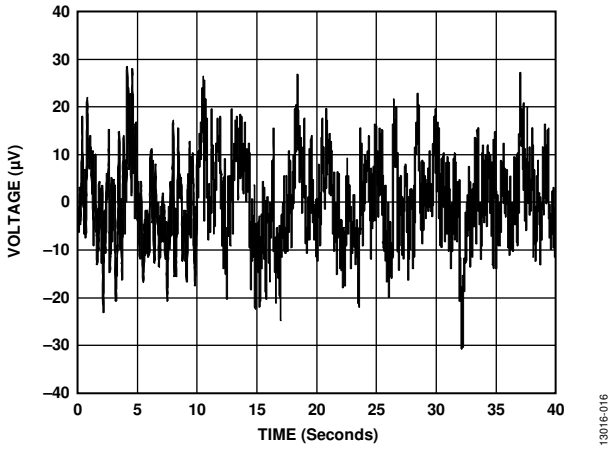

Figure 16. 0.1 Hz to 10 Hz DAC Output Noise, Input Code 0x000

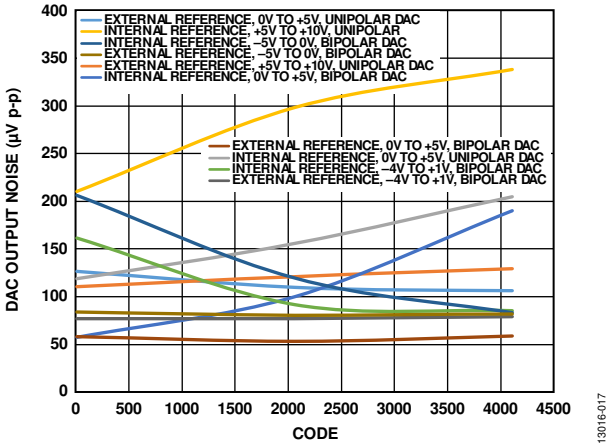

Figure 17. 0.1 Hz to 10 Hz DAC Output Noise vs. Code

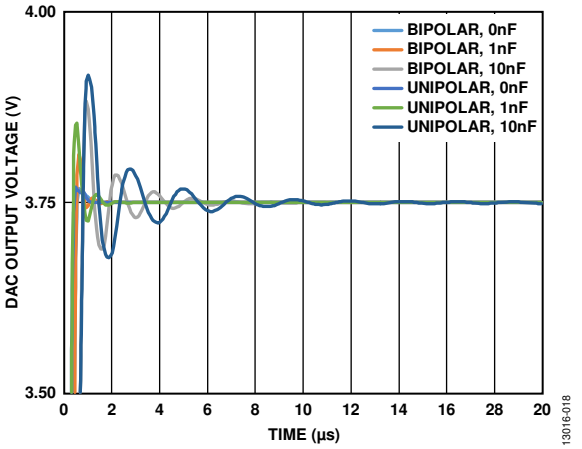

Figure 18. Zoomed In Settling Time for a ¼ to ¾ Output Voltage Step

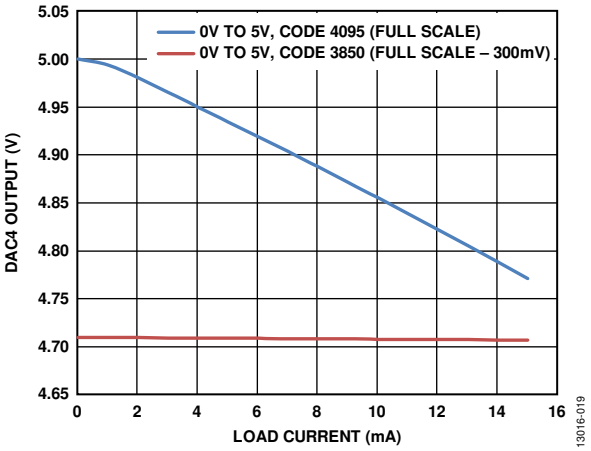

Figure 19. DAC4 Output (Full Scale) vs. Load Current

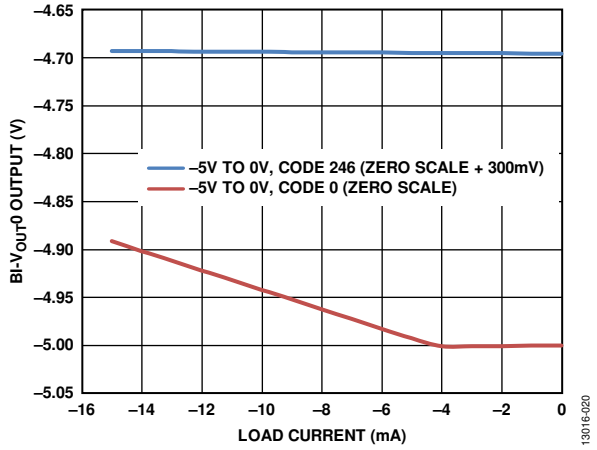

Figure 20. BI-V_{OUT}0 Output Voltage (Zero Scale) vs. Load Current

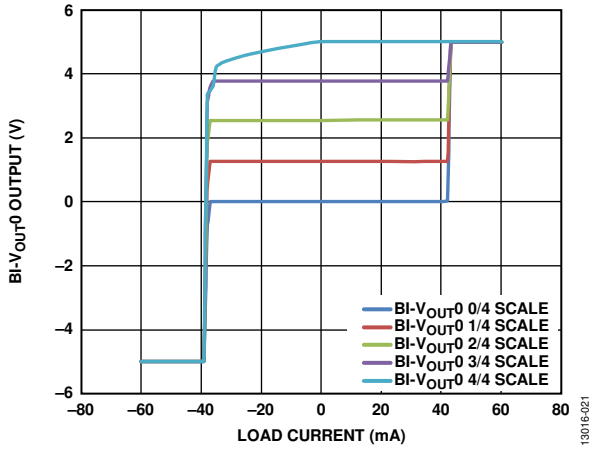

Figure 21. BI-V_{OUT}0 Output Voltage vs. Load Current

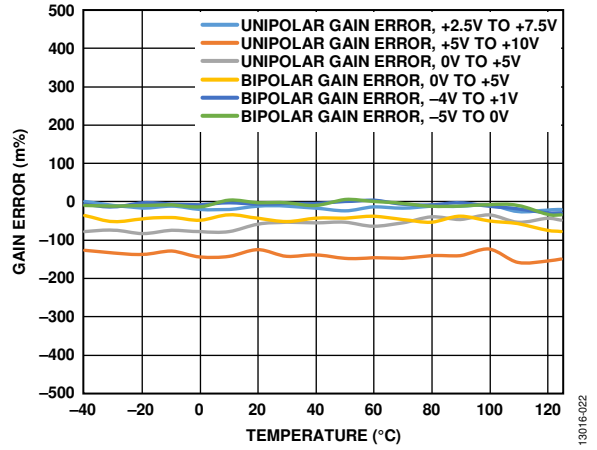

Figure 22. DAC Gain Error vs. Temperature

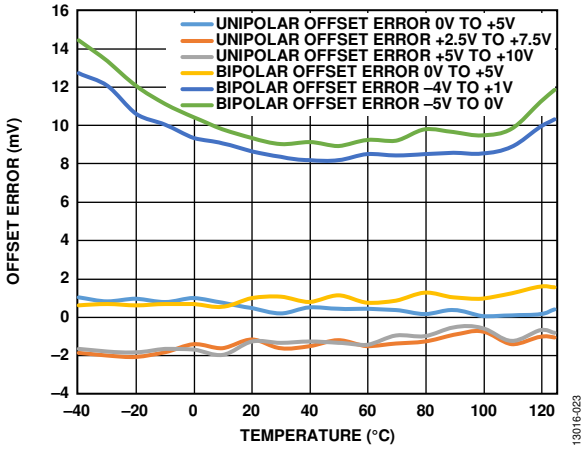

Figure 23. DAC Offset Error vs. Temperature

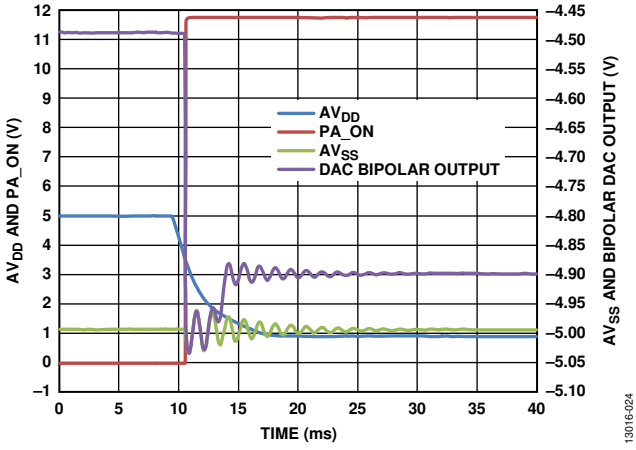

Figure 24. Bipolar DAC Response to AV_{DD} Failure

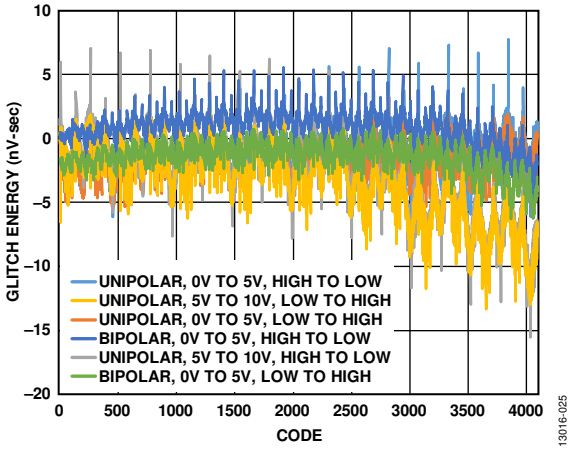

Figure 25. DAC Glitch Energy vs. Code

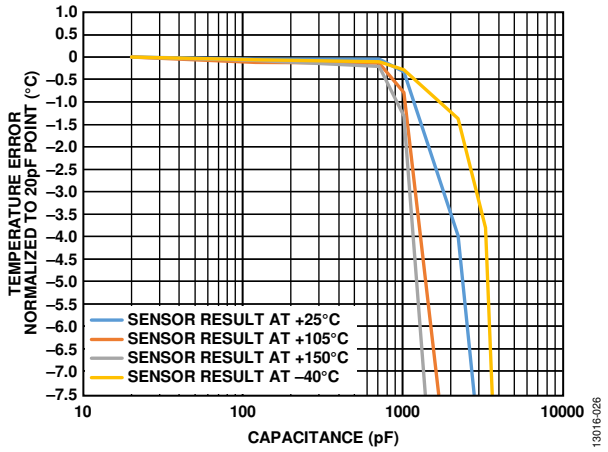

Figure 26. Temperature Error vs. Capacitance from Dx+ to Dx–

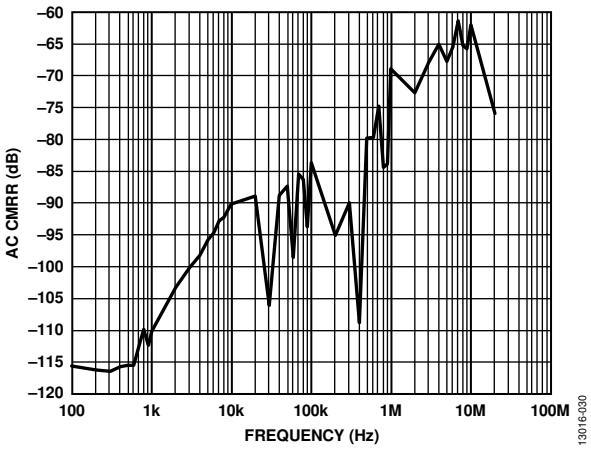

Figure 29. High-Side Current Sensor at Common-Mode Rejection Ratio (CMRR)

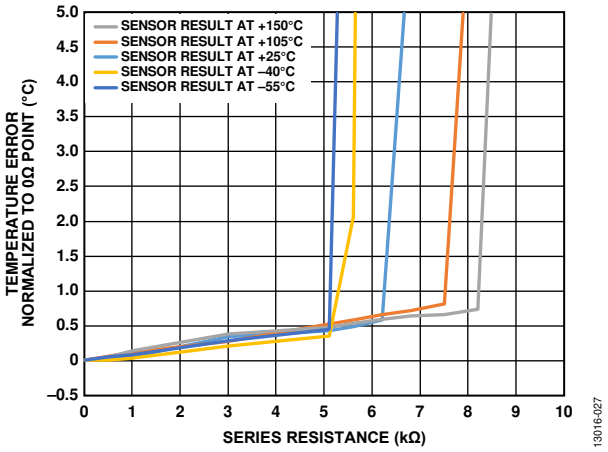

Figure 27. Temperature Error vs. Series Resistance for Typical Devices

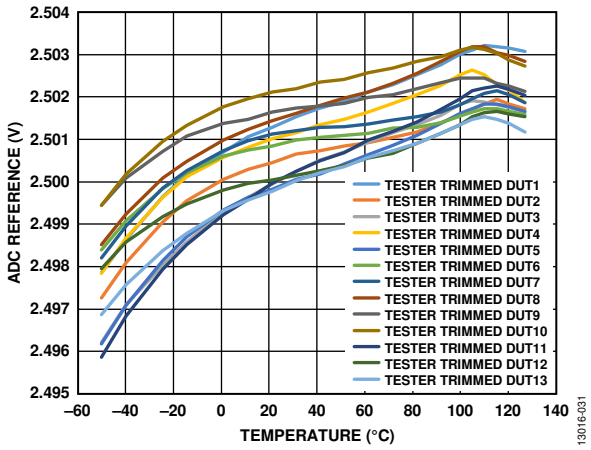

Figure 30. ADC Reference vs. Temperature

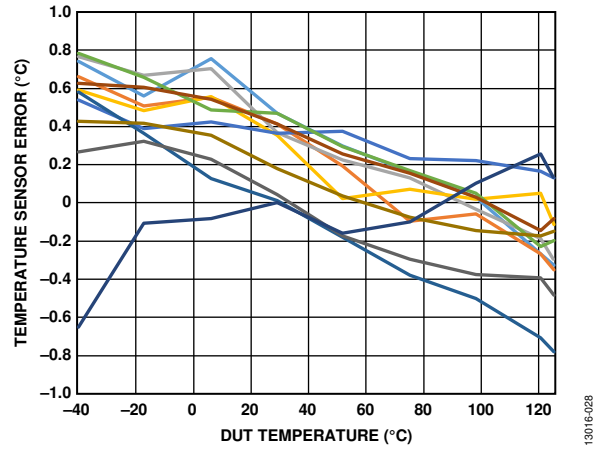

Figure 28. Temperature Sensor Error vs. Device Under Test (DUT) Temperature

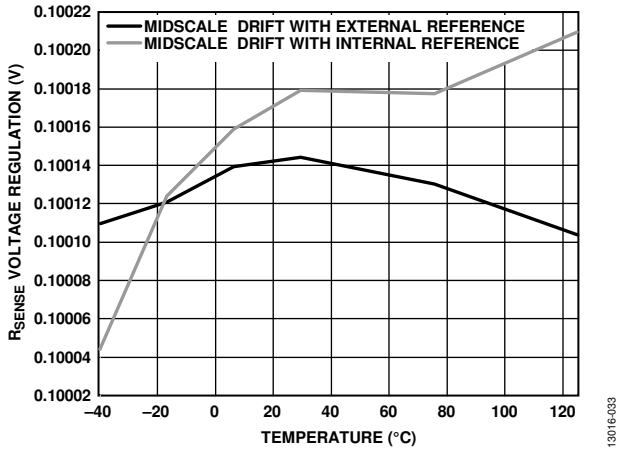

Figure 31. Closed-Loop R_{SENSE} Voltage Regulation vs. Temperature

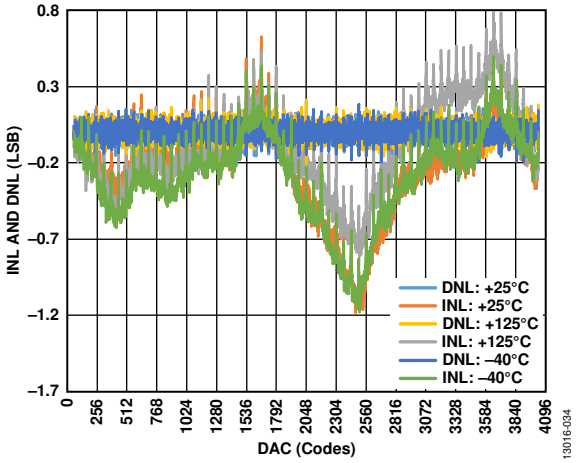

Figure 32. Closed-Loop INL and DNL

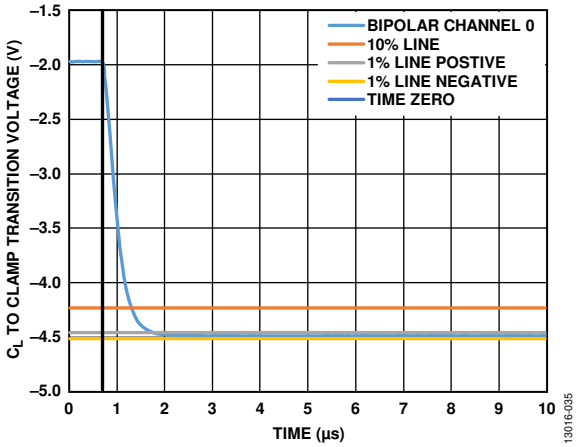

Figure 33. Open Loop to Clamp Settling Time

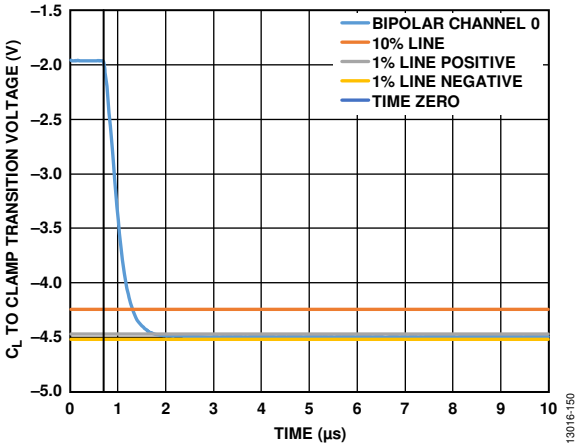

Figure 34. Closed Loop to Clamp Settling Time

THEORY OF OPERATION

ANALOG-TO-DIGITAL CONVERTER (ADC) OVERVIEW

The AD7293 provides the user with a multichannel multiplexer, an on-chip track-and-hold, and a successive approximation ADC based around a capacitive DAC. The analog input range for the ADC is selectable as a 0 V to REF_{ADC}, 0 V to 2 × REF_{ADC}, or 0 V to 4 × REF_{ADC} input single-ended input, where REF_{ADC} = 1.25 V.

The various monitored and uncommitted input signals are multiplexed into the ADC. The AD7293 has four uncommitted analog input channels, $V_{IN}0$ to $V_{IN}3$.

ADC TRANSFER FUNCTIONS

The designed code transitions occur at successive integer least significant bit (LSB) values (1 LSB, 2 × LSB, and so on). The reference voltage for the ADC is referred from the main 2.5 V reference through an amplifier that attenuates the voltage by one half. REF_{ADC} = 1.25 V.

In single-ended mode, the LSB size is $REF_{ADC}/4096$ when the 0 V to REF_{ADC} range is selected, 2 × $REF_{ADC}/4096$ when the 0 V to 2 × REF_{ADC} range is selected, and 4 × $REF_{ADC}/4096$ when the 0 V to 4 × REF_{ADC} range is selected (which is the default value). Figure 35 shows the ideal transfer characteristic for the ADC when outputting straight binary coding.

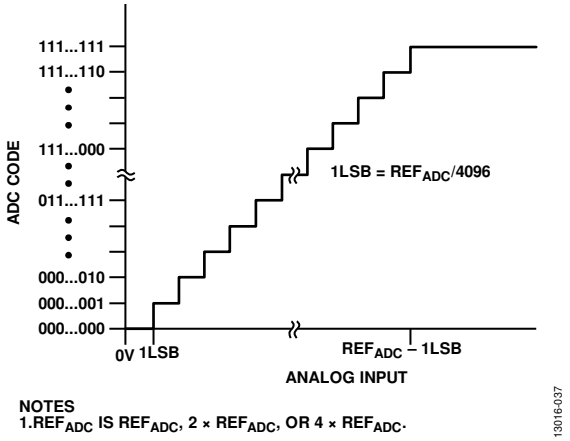

Figure 35. Single-Ended Transfer Characteristics

In differential mode, the LSB size is 2 × $REF_{ADC}/4096$ when the 0 V to REF_{ADC} range is selected, 4 × $REF_{ADC}/4096$ when the 0 V to 2 × REF_{ADC} range is selected, and 8 × $REF_{ADC}/4096$ when the 0 V to 4 × REF_{ADC} range is selected. Figure 36 shows the ideal transfer characteristic for the ADC when outputting differential coding (with the 2 × REF_{ADC} range).

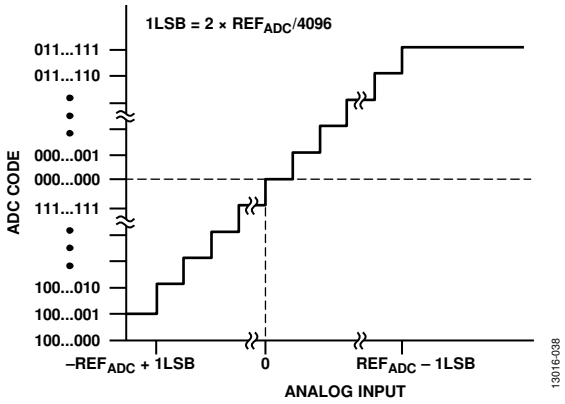

Figure 36. Differential Transfer Characteristics

Table 12. Code Transition and Voltage

Code Transition	Single-Ended Voltage (V_{IN})	Differential Voltage ($V_{IN}+ - V_{IN}-$)
0x000 to 0x001	REF_{ADC} × Range/4096	−REF_{ADC} × Range × 2047/2048
0x7FF to 0x800	REF_{ADC} × Range/2	0 V
0xFFE to 0xFFF	REF_{ADC} × Range × 4095/4096	+REF_{ADC} × Range × 2047/2048

For $V_{IN}0$ to $V_{IN}3$ in single-ended mode, the output code is straight binary, and the ideal input voltage is given by

$$V_{IN} = ((Code + 0.5)/ 4096) \times REF_{ADC} \times Range$$

The differential code is shown in Table 12, and the associated voltage is calculated by

$$V_{IN+} - V_{IN-} = ((Code - 2047.5)/2048) \times REF_{ADC} \times Range$$

where:
Code is the decimal equivalent of the binary code read from the ADC register.
REF_{ADC} = 1.25 V.
Range = 1 when in the 0 V to REF_{ADC} range.
Range = 2 when in the 0 V to 2 × REF_{ADC} range.
Range = 4 when in the 0 V to 4 × REF_{ADC} range.

Table 13. ADC Range Selected vs. LSB Size

Range	Value	Single-Ended ADC LSB	Differential ADC LSB
00	4 × REF_{ADC}[1]	4 × $REF_{ADC}/4096$	8 × $REF_{ADC}/4096$
01	2 × REF_{ADC}[1]	2 × $REF_{ADC}/4096$	4 × $REF_{ADC}/4096$
10	2 × REF_{ADC}[1]	2 × $REF_{ADC}/4096$	4 × $REF_{ADC}/4096$
11	REF_{ADC}[1]	$REF_{ADC}/4096$	2 × $REF_{ADC}/4096$

[1] REF_{ADC} = 1.25 V.

ANALOG INPUTS

The AD7293 has four analog inputs, $V_{IN}3$ to $V_{IN}0$. Depending on the configuration register setup, they can be configured as four single-ended inputs or two fully differential channels.

Single-Ended Mode

The AD7293 can have four single-ended analog input channels. In applications where the signal source is high impedance, it is recommended to buffer the analog input before applying it to the ADC. The analog input range is programmed to the following modes: 0 V to REF_{ADC}, 0 V to 2 × REF_{ADC}, or 4 × REF_{ADC} mode. The voltage, with respect to AGND on the ADC analog input pins, cannot exceed AV_{DD}.

Differential Mode

The AD7293 can have two differential input pairs ($V_{IN}3$ and $V_{IN}2$, $V_{IN}1$ and $V_{IN}0$). The amplitude of the differential signal is the difference between the signals at V_{IN+} and V_{IN-} ($V_{IN}0$ and $V_{IN}1$, or $V_{IN}3$ and $V_{IN}2$). Simultaneously drive V_{IN+} and V_{IN-} by two signals, each of amplitude REF_{ADC}, 2 × REF_{ADC}, or 4 × REF_{ADC}, depending on the range chosen, which are 180° out of phase.

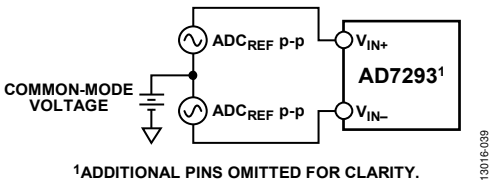

Figure 37. Differential Input (V_{IN+}/V_{IN-} Refer to $V_{IN}0$ to $V_{IN}3$)

Assuming that the 0 V to REF_{ADC} range is selected, the amplitude of the differential signal is, therefore, −REF_{ADC} to +REF_{ADC} peak to peak, regardless of the common-mode voltage (V_{CM}).

The common-mode voltage is the average of the two signals.

$$(V_{IN+} + V_{IN-})/2$$

The common-mode voltage is the voltage on which the two inputs are centered. The result is that the span of each input is V_{CM} ± REF_{ADC}/2. This common-mode voltage must be set up externally.

When a conversion takes place, the common-mode voltage is rejected, resulting in a virtually noise free signal of amplitude −REF_{ADC} to +REF_{ADC}, corresponding to the digital output codes of −2048 to +2047 in twos complement format.

When using the 2 × REF_{ADC} range, the input signal amplitude extends from −2 × REF_{ADC} (V_{IN+} = 0 V and V_{IN-} = REF_{ADC}) to +2 × REF_{ADC} (V_{IN-} = 0 V and V_{IN+} = REF_{ADC}).

Similarly, when using the 4 × REF_{ADC} range, the input signal amplitude extends from −4 × REF_{ADC} (V_{IN+} = 0 V and V_{IN-} = REF_{ADC}) to +4 × REF_{ADC} (V_{IN-} = 0 V and V_{IN+} = REF_{ADC}).

Pseudo Differential Mode

The four uncommitted analog input channels can be configured as two pseudo differential pairs. Two uncommitted inputs, $V_{IN}0$ and $V_{IN}1$, are a pseudo differential pair, as are $V_{IN}2$ and $V_{IN}3$. In this mode, V_{IN+} is connected to the signal source, which can have a maximum amplitude of REF_{ADC}, 2 × REF_{ADC}, or 4 × REF_{ADC}, depending on the range that is chosen, to make use of the full dynamic range of the device. A dc input is applied to V_{IN-}. The voltage applied to this input provides an offset from ground or a pseudo ground for the V_{IN+} input. The ADC channel allocation determines the channel specified as V_{IN+}. The differential mode must be selected to operate in the pseudo differential mode. The resulting converted pseudo differential data is stored in twos complement format in the result register.

For $V_{IN}0$, the governing equation for the pseudo differential mode is

$$V_{OUT} = 2(V_{IN+} - V_{IN-}) - REF_{ADC}$$

where:
V_{IN+} is the single-ended signal.
V_{IN-} is a dc voltage.
REF_{ADC} = 1.25 V.

The benefit of pseudo differential inputs is that they separate the analog input signal ground from the ADC ground, allowing dc common-mode voltages to be cancelled.

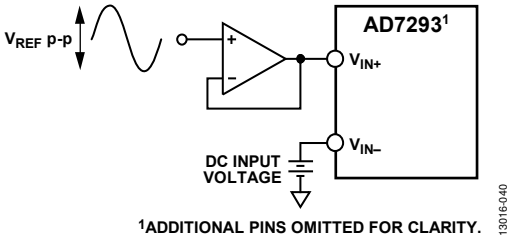

Figure 38. Pseudo Differential Input (V_{IN+}/V_{IN-} Refer to $V_{IN}0$ to $V_{IN}3$)

CURRENT SENSOR

Four bidirectional high-side current sense amplifiers are provided that can accurately amplify differential current shunt voltages in the presence of high common-mode voltages from AV_{DD} up to AV_{SS} + 60 V. The current sensors can be read directly, or optionally, they can be set to operate as part of the four independent closed-loop, drain current controllers. See the Closed-Loop section for more information.

In open-loop operation, the current sense amplifiers measure the current through a shunt resistor. Each amplifier can accept differential inputs up to ±200 mV. A selectable gain amplifies the measured voltage drop across the current sensor.

The AD7293 high-side current sense amplifier is configured as a differential integrator.

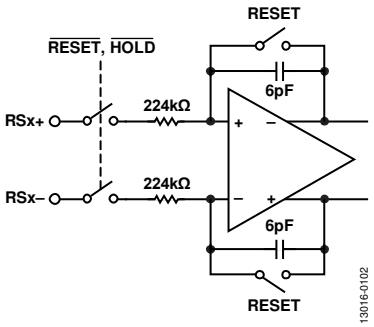

Figure 39. Current Sensor Internal Diagram

Before each measurement, the integrator is held in a reset state for 9.2 µs. The input is then connected and measured for a programmable amount of time, resulting in a gain equal to the following:

$$Gain = Integration\ Time/(224\ k\Omega \times 6\ pF)$$

Table 14. Current Sensor Gain Settings

Code	Typical Gain	Voltage Across R_{SENSE}[1] (mV)	Typical Integration Time (µs)
0000 (Default)	6.25	±200	8.4
0001	12.5	±100	16.8
0010	18.75	±66.67	25.2
0011	25	±50	33.6
0100	37.5	±33.33	50.4
0101	50	±25	67.2
0110	75	±16.67	100.8
0111	100	±12.5	134.4
1000	200	±6.25	268.8
1001	400	±3.125	537.6
1010	781.25	±1.6	1050

[1] R_{SENSE} is the external sense resistor.

When integration is complete, the input switches open, keeping the output constant until the ADC completes its conversion of the output signal. If no other ADC channels are enabled, the conversion takes an additional 4.2 µs. Otherwise, the current sense amplifier waits for its turn in the ADC conversion sequence before resetting and starting a new measurement.

Keep the external source impedance low with respect to the input resistance of the integrator to avoid creating a gain error.

Calculate the current sensor input channel LSB as follows:

$$V_{SENSE}\ LSB = (2 \times REF_{ADC})/(Gain \times 4096)$$

$$V_{RSx+} - V_{RSx-} = -REF_{ADC}/Gain, \text{ with DOUT} = 0x000$$

$$V_{RSx+} - V_{RSx-} = 0\ V, \text{ with DOUT} = 0x7FF$$

$$V_{RSx+} - V_{RSx-} = REF_{ADC}/Gain, \text{ with DOUT} = 0xFFF$$

where:
$V_{SENSE}\ LSB$ is the current sense input channel LSB size in volts.
V_{RSx+} is the voltage for the RSx+ pins.
V_{RSx-} is the voltage for the RSx− pins.
REF_{ADC} = 1.25 V.
Gain can be set between 6.25 and 781.25 as shown in Table 14.

$$I_{SENSE}\ LSB = 2 \times (REF_{ADC}/(Gain \times 4096 \times R_{SENSE}))$$

where:
$I_{SENSE}\ LSB$ is the current sense input channel LSB size in amperes.
R_{SENSE} is the external sense resistor.

Choosing the External Sense Resistor (R_{SENSE})

The resistor values used in conjunction with the current sense amplifiers on the AD7293 are determined by the specific application requirements in terms of voltage, current, and power.

Small resistors minimize power dissipation, have low inductance to prevent induced voltage spikes, and have good tolerance, which reduces current variations. The final values chosen are a compromise between low power dissipation and good accuracy. Low value resistors have less power dissipation and good accuracy; however, higher value resistors may be required to use the full input range of the ADC.

When the sense current is known, the voltage range of the AD7293 current sensor is divided by the maximum sense current to yield a suitable resistor value. If the power dissipation in the shunt resistor is too large, the shunt resistor can be reduced, in which case, the current sensor gain can be increased to maximize the ADC input range used.

R_{SENSE} must be able to dissipate the I^2R losses. If the power dissipation rating of the resistor is exceeded, its value may drift, or the resistor may be damaged, resulting in an open circuit. If the power dissipation of the resistor is exceeded, it can result in a differential voltage across the AD7293 terminals in excess of the absolute maximum ratings.

$$R_{SENSE} \leq \frac{Current\ Sensor\ Input\ Voltage\ Range}{I_{SENSE(MAX)}}$$

where:
R_{SENSE} is the value of the current sense resistor in Ω.
Current Sensor Input Voltage Range is the current sensor amplifier input voltage range as dictated by the gain setting chosen (see Table 14).
$I_{SENSE\ (MAX)}$ is the maximum current required in A.

TEMPERATURE SENSOR

The AD7293 contains one local and two remote temperature sensors. The temperature sensors can continuously monitor the three temperature inputs, and new readings are automatically available every 5 ms.

The on-chip temperature sensor measures the device die temperature. The internal temperature sensor measures between −40°C and 125°C, where the LSB size is 0.125°C.

The AD7293 includes two remote temperate sensors. The device is factory calibrated to work with 2N3906 discrete transistors.

For RF applications, the use of high Q capacitors functioning as a filter protects the integrity of the measurement. Connect these capacitors between the base and the emitter, as close to the external device as possible. However, large capacitances affect the accuracy of the temperature measurement; therefore, the recommended maximum capacitor value is 100 pF. In most cases, a capacitor is not required; the selection of any capacitor is dependent on the noise frequency level.

The AD7293 automatically cancels out the effect of parasitic, base, and collector resistance on the temperature reading. This cancelation gives a more accurate result, without the need for any user characterization of the parasitic resistance. The AD7293 can compensate for up to 4 kΩ series resistance typically.

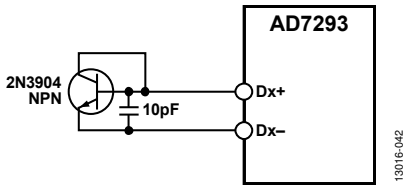

Figure 40. Measuring Temperature Using a NPN Transistor

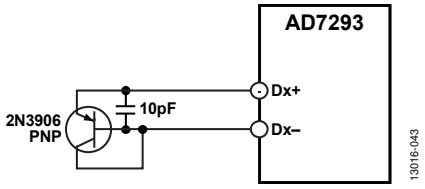

Figure 41. Measuring Temperature Using a PNP Transistor

Table 15. Temperature Sensor Data Format

Temperature (°C)	$T_{SENSE}x$ Result Registers (Page 0x00, Register 0x20 to Register 0x22), Bits[D15:D4]
−40	0110 1100 0000
−25	0111 0011 1000
−10	0111 1011 0000
−0.125	0111 1111 1111
0	1000 0000 0000
+0.125	1000 0000 0001
+10	1000 0101 0000
+25	1000 1100 1000
+50	1001 10 01 0000
+75	1010 0101 1000
+100	1011 0010 0000
+125	1011 1110 1000

INTERNAL CHANNEL MONITORING

The ADC can internally read the outputs of the four bipolar DACs, AV_{DD}, $DACV_{DD-UNI}$, $DACV_{DD-BI}$, AV_{SS}, and the voltage on the RS0+ to RS3+ pins in the background. A sequencer is available that allows multiple channels to be converted in a predetermined sequence.

The ADC is used in its single-ended mode. The LSB size varies with the different supply monitoring registers. AV_{DD} and $DACV_{DD-BI}$ are divided by 5, and $DACV_{DD-UNI}$ is divided by 20 to scale within the 0 V to REF_{ADC} range. AV_{SS} is level shifted to within a −7.5 V to +2.5 V range, where 0x0000 equates to approximately −7.5 V, and 0xFFFF equates to approximately +2.5 V. REF_{ADC} = 1.25 V.

For $RSx+_{MON}$ (internal monitoring of the voltage on the RS0+ to RS3+ pins), divide by 50 to scale them to the 0 V to REF_{ADC} range. Use the ADC in single-ended mode. The $RSx+_{MON}$ monitor result registers store the 12-bit ADC results for the current sense supply channels (see Figure 42).

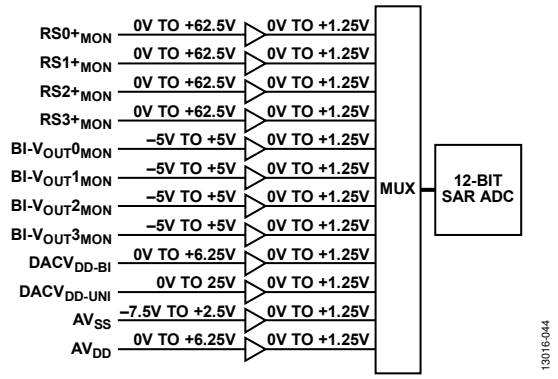

Figure 42. Internal Channel Monitoring

DAC OPERATION

The AD7293 contains eight 12-bit DACs, four bipolar DACs, and four unipolar DACs. These provide digital control with 12 bits of resolution combined with offset range select registers and a 2.5 V internal reference. The DAC core is a 12-bit string DAC. The resistor string structure consists of a string of resistors, each of Value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. When one of the switches connecting the string to an amplifier is closed, the voltage is tapped off. This architecture is inherently monotonic and linear. The eight DACs are split into two groups based on their output range.

Bipolar DACs

The bipolar DACs (BI-V_{OUT}0, BI-V_{OUT}1, BI-V_{OUT}2, and BI-V_{OUT}3) can be configured through the offset range registers to 0 V to +5 V, −5 V to 0 V, or −4 V to +1 V (see Table 85).

Writing to these register addresses sets the 12-bit DAC output voltage. There is also a load bit and a copy bit (see Table 27).

If the load bit is set to 1, the device waits for LDAC to become active before loading the voltage codes onto the DACs rather than immediately after the write operation. If the copy bit is set to 1 when writing to a bipolar DAC register, it sets all bipolar DAC registers to the same value in open-loop mode only.

$$V_{OUT} = \left(2 \times V_{REFIN} \times \left(\frac{D}{2^n}\right)\right) + V_{OFFSET}$$

where:

V_{REFIN} = 2.5 V.

D is the decimal equivalent of the binary code that is loaded to the DAC register (0 to 4095 for the 12-bit AD7293).

n is the resolution of the DAC.

V_{OFFSET} = 0 V (0 V to +5 V range), −4 V (−4 V to +1 V range), or −5 V (−5 V to 0 V range).

Table 16. Bipolar DAC Voltage Offset Ranges

Range (V)	0x000	0xFFF	V_{OFFSET} (V)
0 to +5	0 V	2 V × V_{REFIN}	0
−4 to +1	−1.6 V × V_{REFIN}	0.4 V × V_{REFIN}	−4
−5 to 0	−2 V × V_{REFIN}	0 V	−5

The ADC can also monitor these four outputs.

The bipolar DACs in addition to the four current sensors in the PA controller can operate as four independent closed-loop drain current controllers (see the Closed-Loop Mode section).

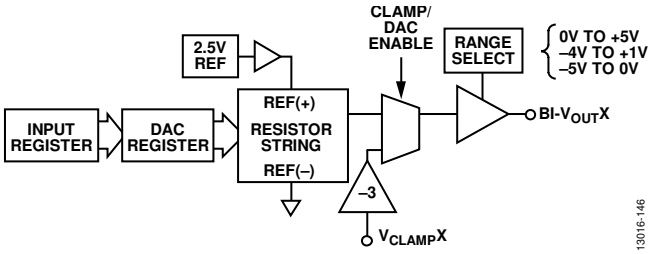

Figure 43. Bipolar DAC Architecture Block Diagram

Unipolar DACs

The unipolar DAC outputs, UNI-V_{OUT}0, UNI-V_{OUT}1, UNI-V_{OUT}2, and UNI-V_{OUT}3, can be configured through the offset range registers to 0 to 5 V, 2.5 V to 7.5 V, or 5 V to 10 V (see Table 84).

The DACs have one control register to control the interaction between two registers: input registers and output registers. The output registers contain the digital code used by the resistor strings as well as a copy and load bit. Writing to these register addresses sets the 12-bit DAC output voltage codes.

If the load bit is set to one, the device waits for LDAC to become active before loading the voltage codes onto the DACs rather than immediately after the write operation. If the copy bit is set to 1, writing to a unipolar DAC registers sets all the other unipolar DAC registers to the same value.

$$V_{OUT} = \left(2 \times V_{REFIN} \times \left(\frac{D}{2^n}\right)\right) + V_{OFFSET}$$

where:
V_{REFIN} = 2.5 V.
D is the decimal equivalent of the binary code that is loaded to the DAC register (0 to 4095 for the 12-bit AD7293).
n is the resolution of the DAC.
V_{OFFSET} = 0 V (0 V to 5 V range), 2.5 V (2.5 V to 7.5 V range), or 5 V (5 V to 10 V range).

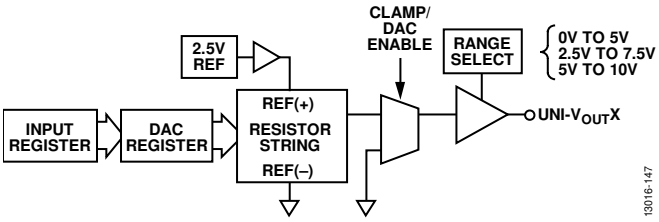

Figure 44. Unipolar DAC Architecture Block Diagram

Table 17. Unipolar DAC Voltage Offset Ranges

Range (V)	0x000	0xFFF	V_{OFFSET} (V)
0 to 5	0 V	2 V × V_{REFIN}	0
2.5 to 7.5	V_{REFIN}	3 V × V_{REFIN}	2.5
5 to 10	2 V × V_{REFIN}	4 V × V_{REFIN}	5

DAC Enabling and Clamping

On power-up, the DAC outputs default to their clamp values (see Table 18). All DACs can be enabled and disabled/clamped via the DAC enable register (common to all pages).

Table 18. Clamp Values

DAC Output	Clamp Value
UNI-V_{OUT}0	0 V
UNI-V_{OUT}1	0 V
UNI-V_{OUT}2	0 V
UNI-V_{OUT}3	0 V
BI-V_{OUT}0	−3 × V_{CLAMP}0
BI-V_{OUT}1	−3 × V_{CLAMP}0
BI-V_{OUT}2	−3 × V_{CLAMP}1
BI-V_{OUT}3	−3 × V_{CLAMP}1

All DACs (bipolar DACs only on power-up) can be set to clamp using the digital SLEEP0 and SLEEP1 pins. The DAC outputs controlled by the digital SLEEP0 and SLEEP1 pins are selectable by writing to the corresponding sleep bit in the DAC snooze/SLEEPx pin register (see Table 45) in the configuration page. When the SLEEPx pin is pulled active, the corresponding unipolar and bipolar DACs associated with the pin are forced into clamp. Clamping does not clear the DAC output register value, making it possible to return to the same voltage as before the clamp event. While in clamp mode, the DAC registers can be updated. When a SLEEPx pin is used, a snooze function is available that clears the DAC registers and requires an additional write to the DAC enable register to wake up the DAC after clearing the clamp condition.

The bipolar DACs power-on reset and clamp value is dependent on the V_{CLAMP}0 and V_{CLAMP}1 voltage level. After a power-on reset or when the digital SLEEP0 or SLEEP1 pin is configured to trigger a clamp, the bipolar DAC outputs reset to the clamp value (see Table 18).

After a power-on reset or when the digital SLEEP0 or SLEEP1 pin is configured to trigger clamping, the unipolar DAC outputs default to 0 V.

Software Clamping: Internal ALERT0 Routing

There is an option to allow the ALERT0 alert to trigger the clamp function. The DACs power back up when the alert is cleared without an additional write to the DAC enable registers. Bit D1 of the general register in the configuration page allows ALERT0 control over the clamping function of the four bipolar DACs.