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12-Bit Monitor and Control System with Multichannel ADC, DACs, Temperature Sensor, and Current Sense

Data Sheet

AD7294-2

FEATURES

- 12-bit SAR ADC with 3 µs conversion time
  - 4 uncommitted analog inputs
    - Differential/single-ended
    - V_{REF}, 2 × V_{REF} input ranges
- 2 high-side current sense inputs
  - 5 V to 59.4 V operating range
  - 0.75% maximum gain error
  - ±200 mV input range
- 2 external diode temperature sensor inputs
  - −55°C to +150°C measurement range
  - ±2°C accuracy
  - Series resistance cancellation
- 1 internal temperature sensor: ±2°C accuracy
- Built-in monitoring features
  - Minimum/maximum recorder for each channel
  - Programmable alert thresholds
  - Programmable hysteresis
- Four 12-bit, monotonic, 15 V DACs
  - 5 V span, 0 V to 10 V offset
  - 8 µs settling time
  - 10 mA sink and source capability
  - Power-on reset (POR) to 0 V
- Internal 2.5 V reference
- 2-wire, fast mode I²C interface
- Temperature range: −40°C to +105°C
- Package type: 64-lead TQFP
- Pin compatible with the AD7294

APPLICATIONS

- Cellular base stations
  - GSM, EDGE, UMTS, CDMA, TD-SCDMA, W-CDMA, WiMAX
- Point-to-multipoint and other RF transmission systems
- 12 V, 24 V, 48 V automotive applications
- Industrial controls

GENERAL DESCRIPTION

The AD7294-2 contains all the functions that are required for general-purpose monitoring and control of current, voltage, and temperature, integrated into a single-chip solution. The part includes low voltage (±200 mV) analog input sense amplifiers for current monitoring across shunt resistors, temperature sense inputs, and four uncommitted analog input channels multiplexed into a SAR analog-to-digital converter (ADC) with a 3 µs conversion time. A high accuracy internal reference is provided to drive both the digital-to-analog converters (DACs) and the ADC. Four 12-bit DACs provide the outputs for voltage control. The AD7294-2 also includes limit registers for alarm functions. The part is designed for high voltage compliance: 59.4 V on the current sense inputs and up to a 15 V DAC output voltage.

The AD7294-2 is a highly integrated solution that offers all the functionality necessary for precise control of the power amplifier in cellular base station applications. In these types of applications, the DACs provide 12-bit resolution to control the bias currents of the power transistors. Thermal diode-based temperature sensors are incorporated to compensate for temperature effects. The ADC monitors the high-side current and temperature. This functionality is provided in a 64-lead TQFP, which operates over a temperature range of −40°C to +105°C.

Rev. 0

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Data Sheet

- AD7294-2: 12-Bit Monitor and Control System with Multichannel ADC, DACs, Temperature Sensor, and Current Sense Data Sheet

User Guides

- UG-605: Evaluating the AD7294-2 12-Bit Monitor and Control System

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REVISION HISTORY

6/13—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

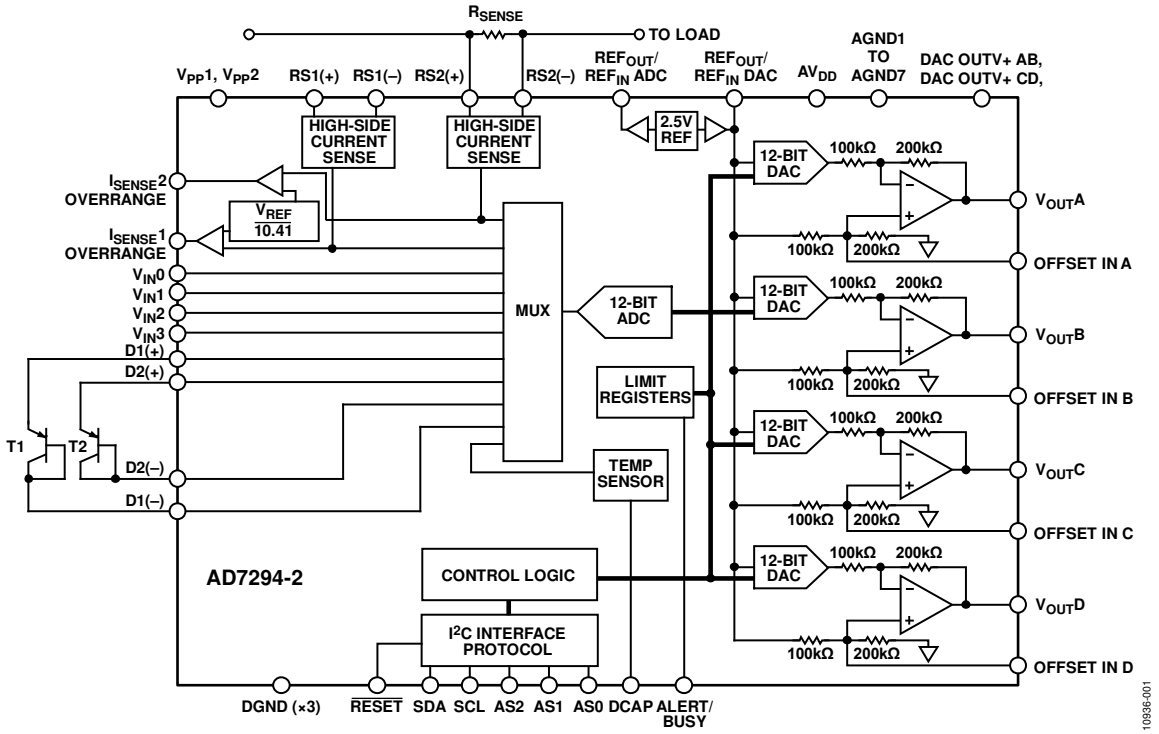


Figure 1.

SPECIFICATIONS

DAC SPECIFICATIONS

AV_{DD} = 4.5 V to 5.5 V, AGND1 to AGND7 = DGND = 0 V, internal 2.5 V reference; V_{DRIVE} = 2.7 V to 5.5 V; T_A = −40°C to +105°C, unless otherwise noted. DAC OUTV+ AB and DAC OUTV+ CD = 4.5 V to 16.5 V; OFFSET IN x is floating; therefore, the DAC output span = 0 V to 5 V.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY[1]					
Resolution	12			Bits	
Relative Accuracy (INL)		±1	±3	LSB	
Differential Nonlinearity (DNL)		±0.3	±1	LSB	Guaranteed monotonic
Zero-Code Error		2.5	6	mV	
Full-Scale Error			10	mV	DAC OUTV+ = 5.5 V
Offset Error			±4	mV	Measured in the linear region, T_A = −40°C to +105°C
			±2	mV	Measured in the linear region, T_A = 25°C
Offset Error Temperature Coefficient		±5		ppm/°C	
Gain Error		±0.025	±0.155	% FSR	
Gain Error Drift		±5		ppm/°C	
DAC OUTPUT CHARACTERISTICS					
Output Voltage Span	0		$2 \times V_{REF}$	V	0 V to 5 V for a 2.5 V reference
Output Voltage Offset	0		10	V	The output voltage span can be positioned in the 0 V to 15 V range; if the OFFSET IN x pin is left floating, the offset = $2/3 \times V_{REF}$, giving an output of 0 V to $2 \times V_{REF}$
Offset Input Pin Range	0		5	V	$V_{OUT} = 3 \times V_{OFFSET} - 2 \times V_{REF} + V_{DAC}$
DC Input Impedance[2]		75		kΩ	100 kΩ to V_{REF}, and 200 kΩ to AGND; see Figure 45
Output Voltage Settling Time[2]		8		µs	1/4 to 3/4 change within 1/2 LSB, measured from last SCL edge
Slew Rate[2]		1.1		V/µs	
Short-Circuit Current[2]		40		mA	Full-scale current shorted to ground
Load Current[2]		±10		mA	Source and/or sink within 200 mV of supply
Capacitive Load Stability[2]	10			nF	$R_L = \infty$
DC Output Impedance[2]		1		Ω	
REFERENCE					
Reference Output Voltage	2.49	2.5	2.51	V	±0.2% maximum at 25°C, AV_{DD} = 5 V
Reference Input Voltage Range	0		$AV_{DD} - 2$	V	
Input Current		400	480	µA	V_{REF} = 2.5 V
Input Capacitance[2]		20		pF	
V_{REF} Output Impedance[2]		5		Ω	A buffer is required if the reference output is used to drive external loads
Reference Temperature Coefficient		10	25	ppm/°C	

[1] Linearity calculated using a reduced code range: Code 10 to Code 4095.
[2] Guaranteed by design and characterization; not production tested.

ADC SPECIFICATIONS

AV_{DD} = 4.5 V to 5.5 V, AGND1 to AGND7 = DGND = 0 V, internal or external 2.5 V reference; V_{DRIVE} = 2.7 V to 5.5 V; V_{PPx} = AV_{DD} to 59.4 V; T_A = −40°C to +105°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC ACCURACY					
Resolution		12		Bits	
Integral Nonlinearity (INL)[1]		±0.5	±1	LSB	Differential mode
		±0.5	±1.5	LSB	Single-ended or pseudo differential mode
Differential Nonlinearity (DNL)[1]		±0.5	±0.99	LSB	Differential, single-ended, and pseudo differential modes
Single-Ended Mode					
Offset Error		±1	±7	LSB	
Offset Error Match		±0.4		LSB	
Gain Error		±0.5	±4.5	LSB	
Gain Error Match		±0.4		LSB	
Differential Mode					
Positive Gain Error		±1		LSB	
Positive Gain Error Match		±0.5		LSB	
Zero Code Error		±3		LSB	
Zero Code Error Match		±0.5		LSB	
Negative Gain Error		±1		LSB	
Negative Gain Error Match		±0.5		LSB	
CONVERSION RATE					
Conversion Time[2]		3		µs	
Autocycle Update Rate[2]		50		µs	
Throughput Rate			22.22	kSPS	f_{SCL} = 400 kHz
ANALOG INPUT[3]					
Single-Ended Input Range	0		V_{REF}	V	0 V to V_{REF} mode
	0		$2 \times V_{REF}$	V	0 V to $2 \times V_{REF}$ mode
Pseudo Differential Input Range: $V_{IN+} - V_{IN-}$[4]	0		V_{REF}	V	0 V to V_{REF} mode
	0		$2 \times V_{REF}$	V	0 V to $2 \times V_{REF}$ mode
Fully Differential Input Range: $V_{IN+} - V_{IN-}$	$-V_{REF}$		$+V_{REF}$	V	0 V to V_{REF} mode
	$-2 \times V_{REF}$		$+2 \times V_{REF}$	V	0 V to $2 \times V_{REF}$ mode
Input Capacitance[2]		30		pF	
DC Input Leakage Current			±1	µA	
DYNAMIC PERFORMANCE					
Signal-to-Noise Ratio (SNR)[1]		73		dB	f_{IN} = 10 kHz sine wave; differential mode
		72		dB	f_{IN} = 10 kHz sine wave; single-ended and pseudo differential modes
Signal-to-Noise and Distortion Ratio (SINAD)[1]		72.5		dB	f_{IN} = 10 kHz sine wave; differential mode
		71.5		dB	f_{IN} = 10 kHz sine wave; single-ended and pseudo differential modes
Total Harmonic Distortion (THD)[1]		−81		dB	f_{IN} = 10 kHz sine wave; differential mode
		−79		dB	f_{IN} = 10 kHz sine wave; single-ended and pseudo differential modes
Spurious-Free Dynamic Range (SFDR)[1]		−81		dB	f_{IN} = 10 kHz sine wave; differential mode
		−79		dB	f_{IN} = 10 kHz sine wave; single-ended and pseudo differential modes
Channel-to-Channel Isolation[2]		−90		dB	f_{IN} = 0.5 Hz to 100 kHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE SENSOR—INTERNAL					
Operating Range	−40		+105	°C	
Accuracy			±2	°C	Internal temperature sensor, T_A = −30°C to +90°C
			±2.5	°C	Internal temperature sensor, T_A = −40°C to +105°C
Resolution		0.25		°C	LSB size
Update Rate		5		ms	
TEMPERATURE SENSOR—EXTERNAL					External transistor is 2N3906
Operating Range	−55		+150	°C	Limited by external diode
Accuracy			±2	°C	$T_A = T_{DIODE}$ = −40°C to +105°C
Resolution		0.25		°C	LSB size
Low Level Output Current Source[2]		8		µA	
Medium Level Output Current Source[2]		32		µA	
High Level Output Current Source[2]		128		µA	
Maximum Series Resistance (R_S) for External Diode[2]			10	kΩ	For <±0.5°C additional error, C_P = 0 (see Figure 29)
Maximum Parallel Capacitance (C_P) for External Diode[2]			1	nF	R_S = 0 (see Figure 28)
CURRENT SENSE					V_{PP} = AV_{DD} to 59.4 V
V_{PP} Supply Range	AV_{DD}		59.4	V	
Gain Error			±0.75	% FSR	2.5 V reference
Differential Input		±200		mV	2.5 V reference
RS(+)/RS(−) Input Bias Current		25	32	µA	
CMRR/PSRR[2]		110		dB	Inputs shorted to V_{PP}
Offset Error		±50	±780	µV	
Offset Drift		3		µV/°C	
Amplifier Peak-to-Peak Noise[2]		400		µV	Referred to input
V_{PP} Supply Current		0.18	0.25	mA	Per channel, $V_{PP}1 = V_{PP}2$ = 59.4 V
REFERENCE					
Reference Output Voltage	2.49	2.5	2.51	V	±0.2% maximum at 25°C
Reference Input Voltage Range[2]	0.1		4.1	V	
DC Leakage Current			±2	µA	
V_{REF} Output Impedance[2]		5		Ω	A buffer is required if the reference output is used to drive external loads
Input Capacitance[2]		20		pF	
Reference Temperature Coefficient		10	25	ppm/°C	

[1] See the Terminology section for more information.
[2] Guaranteed by design and characterization; not production tested.
[3] V_{IN+} and V_{IN-} must remain within AGND/AV_{DD}. (The analog input pins are $V_{IN}3$ to $V_{IN}0$.)
[4] V_{IN-} = 0 V for specified performance. For full input range on V_{IN-}, see Figure 36.

GENERAL SPECIFICATIONS

AV_{DD} = 4.5 V to 5.5 V, AGND1 to AGND7 = DGND = 0 V, internal or external 2.5 V reference; V_{DRIVE} = 2.7 V to 5.5 V; $V_{PP}x$ = AV_{DD} to 59.4 V; DAC OUTV+ AB and DAC OUTV+ CD = 4.5 V to 16.5 V; OFFSET IN x is floating; therefore, DAC output span = 0 V to 5 V; T_A = −40°C to +105°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS						
Input High Voltage	V_{IH}	0.7 V_{DRIVE}			V	SDA, SCL only
Input Low Voltage	V_{IL}			0.3 V_{DRIVE}	V	SDA, SCL only
Input Leakage Current	I_{IN}			±1	µA	
Input Hysteresis[1]	V_{HYST}	0.05 V_{DRIVE}			V	
Input Capacitance[1]	C_{IN}		8		pF	
Glitch Rejection[1]			50		ns	Input filtering suppresses noise spikes of less than 50 ns
Maximum External Capacitance of I^2C Address Pins When Floating[1]				30	pF	Tristate input
LOGIC OUTPUTS						
SDA, ALERT						SDA and ALERT/BUSY are open-drain outputs
Output Low Voltage	V_{OL}			0.4	V	I_{SINK} = 3 mA
				0.6	V	I_{SINK} = 6 mA
Floating-State Leakage Current[1]				±1	µA	
Floating-State Output Capacitance[1]			8		pF	
I_{SENSE} OVERRANGE						$I_{SENSE}x$ OVERRANGE are push-pull outputs
Output High Voltage	V_{OH}			V_{DRIVE} − 0.2	V	I_{SOURCE} = 200 µA for push-pull outputs
Output Low Voltage	V_{OL}			0.2	V	I_{SINK} = 200 µA for push-pull outputs
Overrange Setpoint[1]		V_{FS}	V_{FS} × 1.2		mV	V_{FS} = ±V_{REF} ADC/12.5
POWER REQUIREMENTS						
$V_{PP}1$, $V_{PP}2$		AV_{DD}		59.4	V	
AV_{DD}		4.5		5.5	V	
DAC OUTV+ xx		4.5		16.5	V	
V_{DRIVE}		2.7		5.5	V	
I_{DD}			5.3	7.5	mA	AV_{DD} + V_{DRIVE}; DAC outputs unloaded
DAC OUTV+ xx, I_{DD}			0.6	1.2	mA	At midscale output voltage, DAC outputs unloaded
Power Dissipation			70	110	mW	
Power-Down						
I_{DD}			4.4	5.5	mA	AV_{DD} and V_{DRIVE}; ADC, DACs, and temperature sensor powered down
DAC OUTV+ x, I_{DD}			35	60	µA	
Power Dissipation				70	mW	

[1] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

I²C Serial Interface

AV_{DD} = 4.5 V to 5.5 V, AGND1 to AGND7 = DGND = 0 V, internal or external 2.5 V reference; V_{DRIVE} = 2.7 V to 5.5 V; $V_{PP}x$ = AV_{DD} to 59.4 V; DAC OUTV+ AB and DAC OUTV+ CD = 4.5 V to 16.5 V; OFFSET IN x is floating, therefore, DAC output span = 0 V to 5 V; T_A = −40°C to +105°C, unless otherwise noted.

Table 4.

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Symbol	Description
f_{SCL}	400	kHz max		SCL clock frequency
t_1	2.5	µs min		SCL cycle time
t_2	0.6	µs min	t_{HIGH}	SCL high time
t_3	1.3	µs min	t_{LOW}	SCL low time
t_4	0.6	µs min	$t_{HD,STA}$	Start/repeated start condition hold time
t_5	100	ns min	$t_{SU,DAT}$	Data setup time
t_6	0.9	µs max	$t_{HD,DAT}$	Data hold time
	0	µs min	$t_{HD,DAT}$	Data hold time
t_7	0.6	µs min	$t_{SU,STA}$	Setup time for repeated start
t_8	0.6	µs min	$t_{SU,STO}$	Stop condition setup time
t_9	1.3	µs min	t_{BUF}	Bus free time between a stop and a start condition
t_{10}[2]	300	ns max	t_R	Rise time of SCL and SDA when receiving
	0	ns min	t_R	Rise time of SCL and SDA when receiving (CMOS compatible)
t_{11}[2]	300	ns max	t_F	Fall time of SDA when transmitting
	20 × (V_{DRIVE}/5.5 V)	ns min	t_F	Fall time of SCL and SDA when transmitting
	0	ns min	t_F	Fall time of SDA when receiving (CMOS compatible)
	300	ns max	t_F	Fall time of SCL and SDA when receiving
C_b[3]	400	pF max		Capacitive load for each bus line

[1] See Figure 2.
[2] t_R and t_F are measured between 0.3 V_{DD} and 0.7 V_{DD}.
[3] C_b is the total capacitance in pF of one bus line.

Timing and Circuit Diagrams

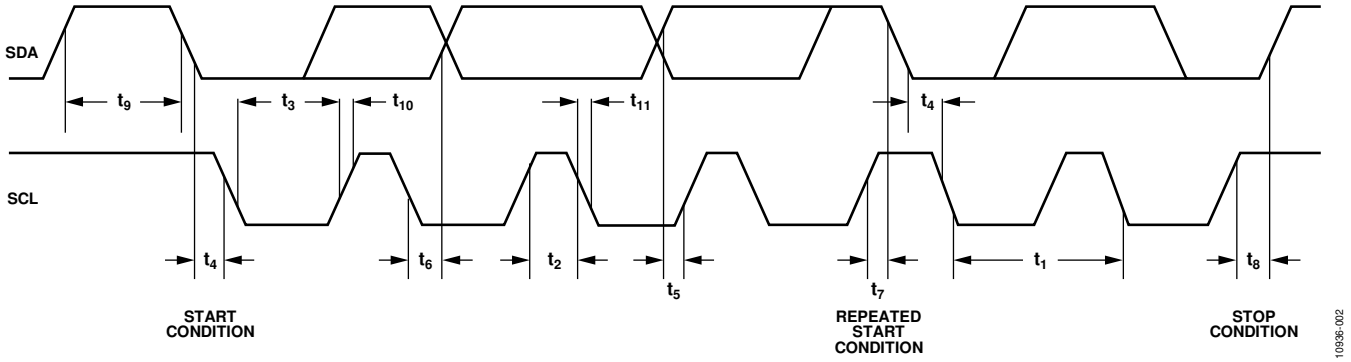


Figure 2. I²C-Compatible Serial Interface Timing Diagram

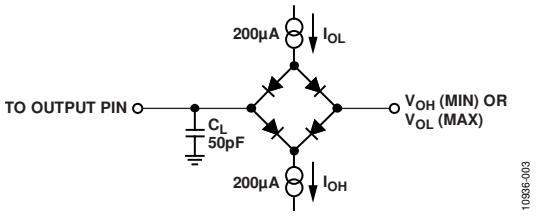


Figure 3. Load Circuit for Digital Output

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.[1]

Table 5.

Parameter	Rating
$V_{PP}x$ to AGND	−0.3 V to +65 V
AV_{DD} to AGND	−0.3 V to +7 V
DAC OUTV+ AB to AGND	−0.3 V to +17 V
DAC OUTV+ CD to AGND	−0.3 V to +17 V
V_{DRIVE} to OPGND	−0.3 V to +7 V
Digital Inputs to OPGND	−0.3 V to V_{DRIVE} + 0.3 V
$\overline{RESET}$ to OPGND	−0.3 V to +7 V
SDA/SCL to OPGND	−0.3 V to +7 V
Digital Outputs to OPGND	−0.3 V to V_{DRIVE} + 0.3 V
RS(+)/RS(−) to $V_{PP}x$	$V_{PP}x$ − 0.3 V to $V_{PP}x$ + 0.3 V
REF_{OUT}/REF_{IN} ADC to AGND	−0.3 V to AV_{DD} + 0.3 V
REF_{OUT}/REF_{IN} DAC to AGND	−0.3 V to AV_{DD} + 0.3 V
OPGND to AGND	−0.3 V to +0.3 V
OPGND to DGND	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
$V_{OUT}x$ to AGND	−0.3 V to DAC OUTV+ xx + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\ MAX}$)	150°C
ESD, Human Body Model	1 kV
Reflow Soldering Peak Temperature	260°C

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

To conform with IPC-2221 industrial standards, it is advisable to use conformal coating on the high voltage pins.

THERMAL RESISTANCE

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
64-Lead TQFP	54	16	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

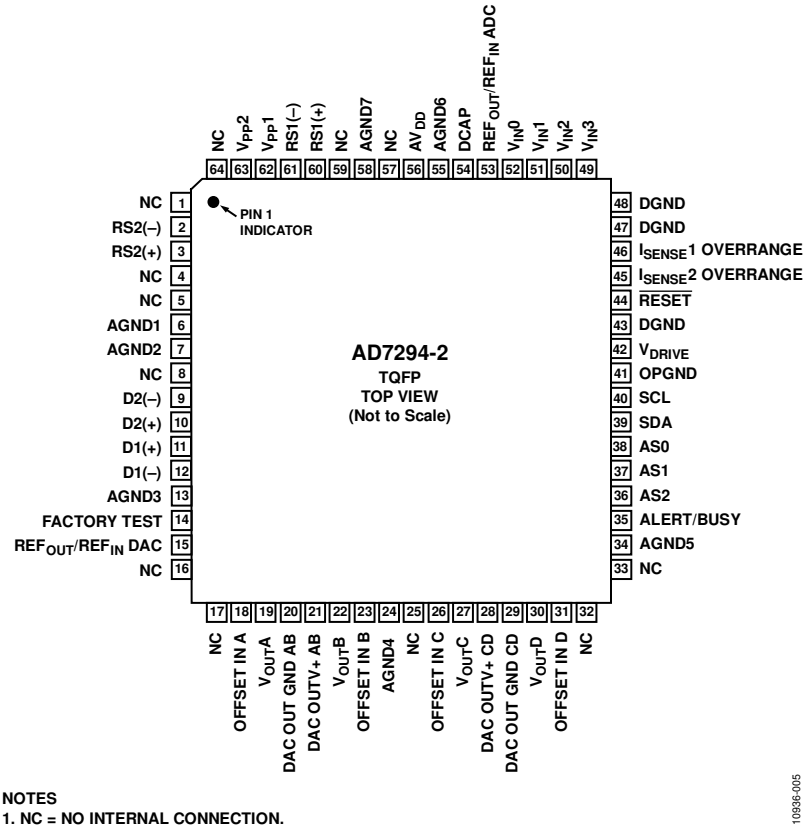


Figure 4. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
2, 61	RS2(–), RS1(–)	Connection for External Shunt Resistor.
3, 60	RS2(+), RS1(+)	Connection for External Shunt Resistor.
1, 4, 5, 8, 16, 17, 25, 32, 33, 57 59, 64	NC	This pin has no internal connection.
14	FACTORY TEST	Factory Test Pin. To maintain pin compatibility with the AD7294, this pin can tolerate being connected to voltages of up to 5.5 V.
56	AV_{DD}	Analog Supply Pin. The operating range is 4.5 V to 5.5 V. This pin provides the supply voltage for all the analog circuitry on the AD7294-2. This supply should be decoupled to AGND with one 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor.
6, 7, 13, 24, 34, 55, 58	AGND1 to AGND7	Analog Ground. Ground reference point for all analog circuitry on the AD7294-2. Refer all analog input signals and any external reference signal to this AGND voltage. Connect all seven of these AGND pins to the AGND plane of the system. Note that AGND5 is a DAC ground reference point and should be used as a star ground for circuitry being driven by the DAC outputs. Ideally, the AGND and DGND voltages should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
9, 12	D2(–), D1(–)	Temperature Sensor Analog Inputs. These pins are connected to the external temperature sensing transistor. See Figure 43 and Figure 44.
10, 11	D2(+), D1(+)	Temperature Sensor Analog Inputs. These pins are connected to the external temperature sensing transistor. See Figure 43 and Figure 44.
15	REF_{OUT}/REF_{IN} DAC	DAC Reference Output/Input Pin. The REF_{OUT}/REF_{IN} DAC pin is common to all four DAC channels. On power-up, the default configuration of this pin is as an external reference (REF_{IN}). Enable the internal reference by writing to the power-down register; see Table 27. Decoupling capacitors (220 nF recommended) are connected to this pin to decouple the reference buffer. If the output is buffered, the on-chip reference can be taken from this pin and applied externally to the rest of a system. A maximum external reference voltage of AV_{DD} – 2 V can be supplied to the REF_{OUT} portion of the REF_{OUT}/REF_{IN} DAC pin.

Pin No.	Mnemonic	Description
18, 23, 26, 31	OFFSET IN A to OFFSET IN D	DAC Analog Offset Input Pins. These pins set the desired output range for each DAC channel. The DACs have an output voltage span of 5 V, which can be shifted from 0 V to 5 V to a maximum output voltage of 10 V to 15 V by supplying an offset voltage to these pins. These pins can be left floating, in which case decouple them to AGND with a 100 nF capacitor.
19, 22, 27, 30	V_{OUT}A to V_{OUT}D	Buffered Analog DAC Outputs for Channel A to Channel D. Each DAC analog output is driven from an output amplifier that can be offset using the OFFSET IN x pin. The DAC has a maximum output voltage span of 5 V that can be level shifted to a maximum output voltage level of 15 V. Each output is capable of sourcing and sinking 10 mA and driving a 10 nF load.
20, 29	DAC OUT GND AB, DAC OUT GND CD	Analog Ground. Analog ground pins for the DAC output amplifiers on V_{OUT}A and V_{OUT}B, and V_{OUT}C and V_{OUT}D, respectively.
21, 28	DAC OUTV+ AB, DAC OUTV+ CD	Analog Supply. Analog supply pins for the DAC output amplifiers on V_{OUT}A and V_{OUT}B, and V_{OUT}C and V_{OUT}D, respectively. The operating range is 4.5 V to 16.5 V.
35	ALERT/BUSY	Digital Output. Selectable as an alert or busy output function in the configuration register. This is an open-drain output. An external pull-up resistor is required. When configured as an alert, this pin acts as an out-of-range indicator and becomes active when the conversion result violates the $DATA_{HIGH}$ or $DATA_{LOW}$ register values. See the Alert Status Registers section. When configured as a busy output, this pin becomes active when a conversion is in progress.
38, 37, 36	AS0, AS1, AS2	Digital Logic Inputs. Together, the logic state of these inputs selects a unique I^2C address for the AD7294-2. See Table 34 for more information.
39	SDA	Digital Input/Output. Serial bus bidirectional data; external pull-up resistor required.
40	SCL	Serial I^2C Bus Clock. The data transfer rate in I^2C mode is compatible with both 100 kHz and 400 kHz operating modes. Open-drain input; external pull-up resistor required.
41	OPGND	Dedicated Ground Pin for I^2C Interface.
42	V_{DRIVE}	Logic Power Supply. The voltage supplied at this pin determines at what voltage the interface operates. Decouple this pin to DGND. The voltage range on this pin is 2.7 V to 5.5 V; it may be different from the voltage level at AV_{DD} but should never exceed it by more than 0.3 V. To set the input and output thresholds, connect this pin to the supply to which the I^2C bus is pulled.
43, 47, 48	DGND	Digital Ground. This pin is the ground for all digital circuitry.
44	$\overline{RESET}$	Reset. Taking $\overline{RESET}$ low performs a reset of the I^2C interface logic. The logic input threshold of the pin is set by V_{DRIVE} (Pin 42). To maintain pin compatibility with the AD7294, this pin can tolerate being connected to voltages of up to 5.5 V.
46, 45	I_{SENSE}1 OVERRANGE, I_{SENSE}2 OVERRANGE	Fault Comparator Outputs. These pins connect to the high-side current sense amplifiers.
49, 50, 51, 52	V_{IN}3 to V_{IN}0	Uncommitted ADC Analog Inputs. These pins are programmable as four single-ended channels or two true differential analog input channel pairs. See Table 2 and Table 10 for more information.
53	REF_{OUT}/REF_{IN} ADC	ADC Reference Output/Input Pin. The REF_{OUT}/REF_{IN} ADC pin provides the reference source for the ADC. On power-up, the default configuration of this pin is as an external reference (REF_{IN}). Enable the internal reference by writing to the power-down register (see Table 27). Connect decoupling capacitors (220 nF recommended) to this pin to decouple the reference buffer. If the output is buffered, the on-chip reference can be taken from this pin and applied externally to the rest of a system. A maximum external reference voltage of 2.5 V can be supplied to the REF_{OUT} portion of this pin.
54	DCAP	External Decoupling Capacitor Input for Internal Temperature Sensor. Decouple this pin to AGND using a 0.1 µF capacitor. In normal operation, the voltage is typically 1.25 V.
62, 63	V_{PP}1, V_{PP}2	Current Sensor Supply Pins. Power supply pins for the high-side current sense amplifiers. The operating range is from AV_{DD} to 59.4 V. Decouple these supplies to AGND. Refer to the Current Sense Filtering section for more information about using these pins.

TYPICAL PERFORMANCE CHARACTERISTICS

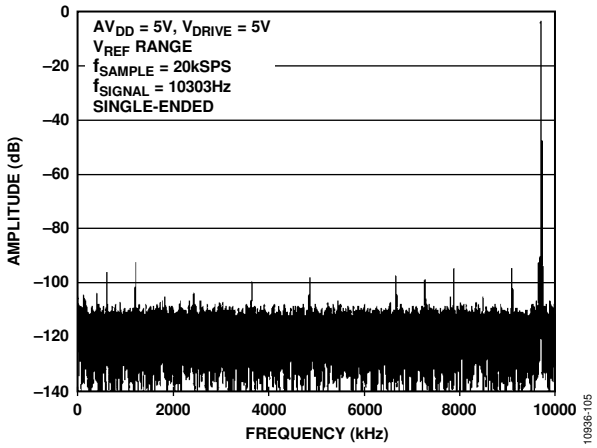


Figure 5. Signal-to-Noise Ratio, Single-Ended Input, V_{REF} Range

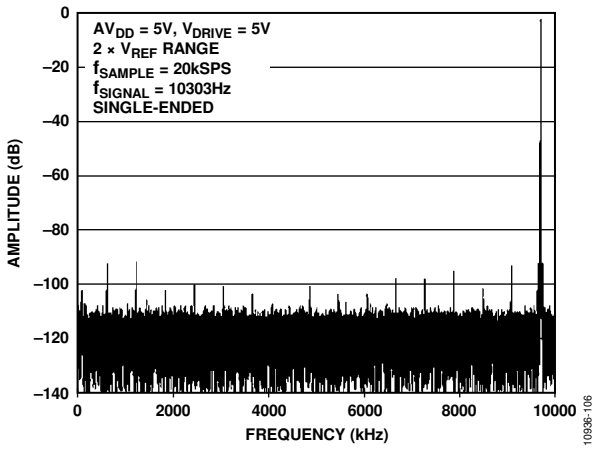


Figure 6. Signal-to-Noise Ratio, Single-Ended Input, 2 × V_{REF} Range

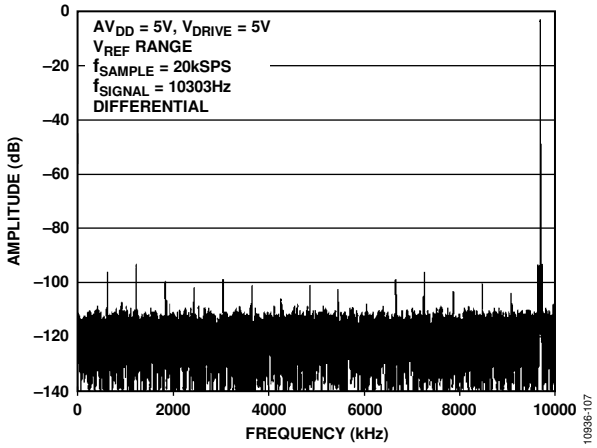


Figure 7. Signal-to-Noise Ratio, Differential Input, V_{REF} Range

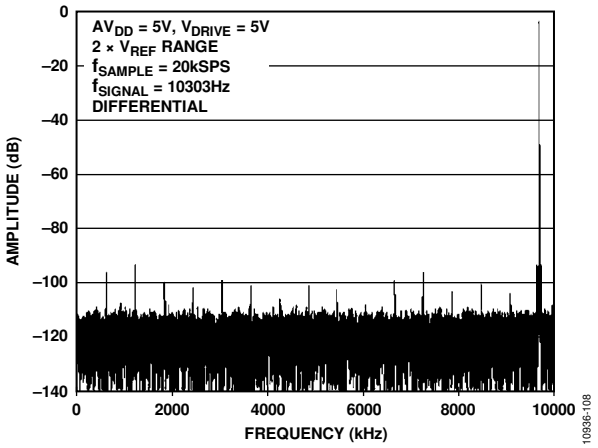


Figure 8. Signal-to-Noise Ratio, Differential Input, 2 × V_{REF} Range

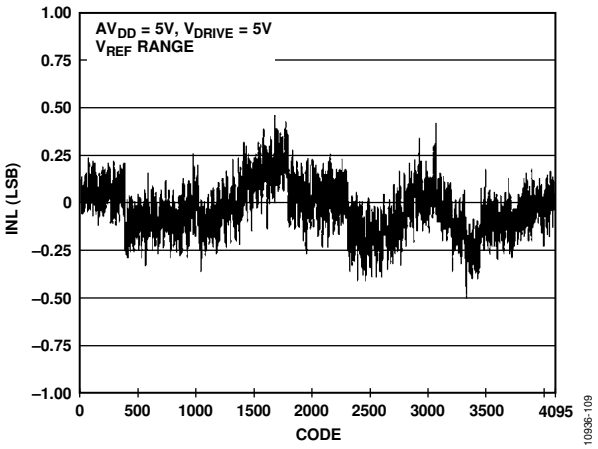


Figure 9. ADC INL, Single-Ended Input, V_{REF} Range

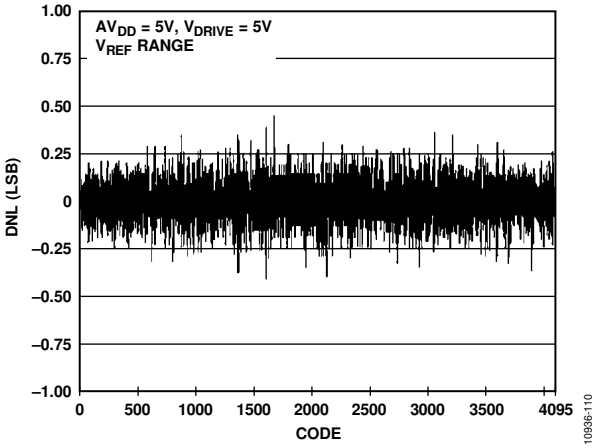


Figure 10. ADC DNL, Single-Ended Input, V_{REF} Range

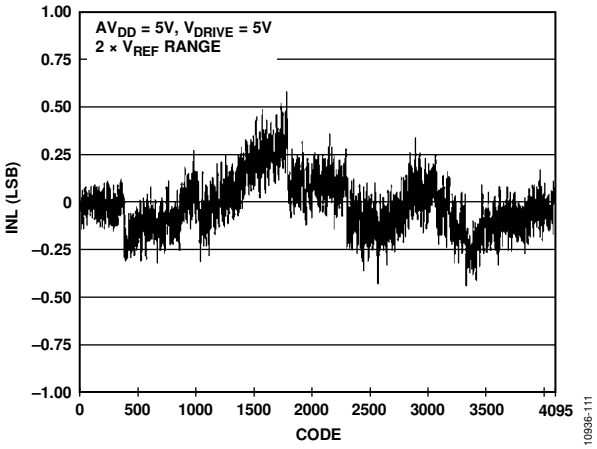


Figure 11. ADC INL, Single-Ended Input, 2 × V_{REF} Range

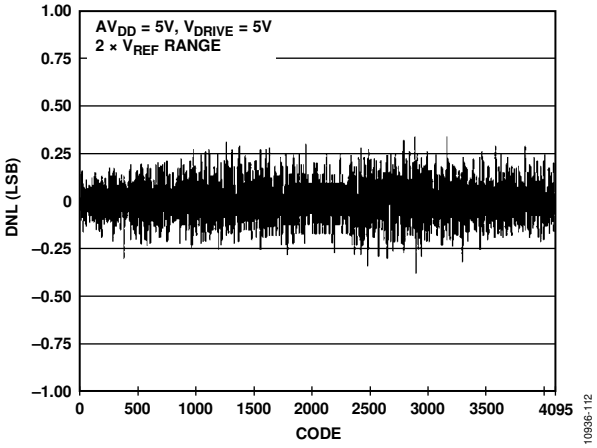


Figure 12. ADC DNL, Single-Ended Input, 2 × V_{REF} Range

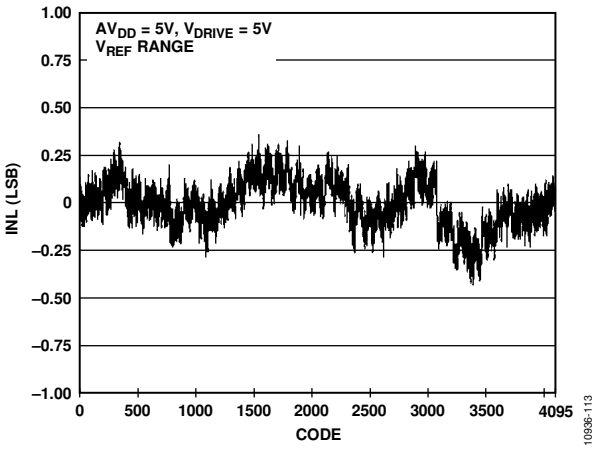


Figure 13. ADC INL, Differential Input, V_{REF} Range

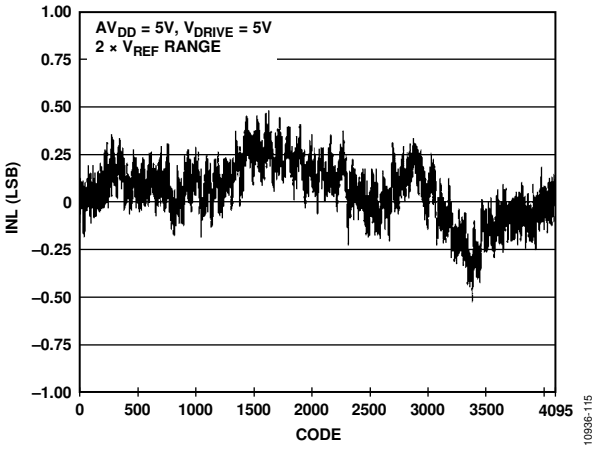


Figure 14. ADC INL, Differential Input, V_{REF} Range

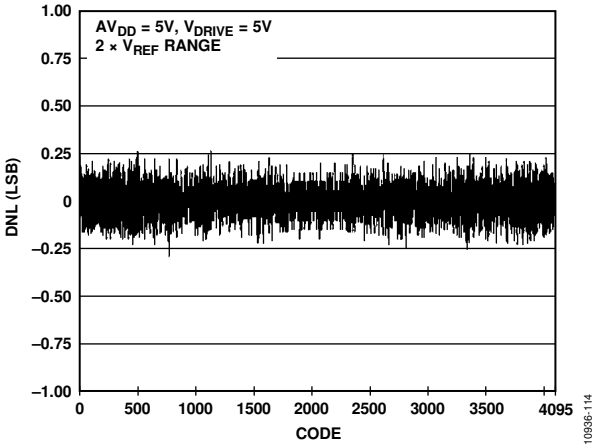


Figure 15. ADC DNL, Differential Input, 2 × V_{REF} Range

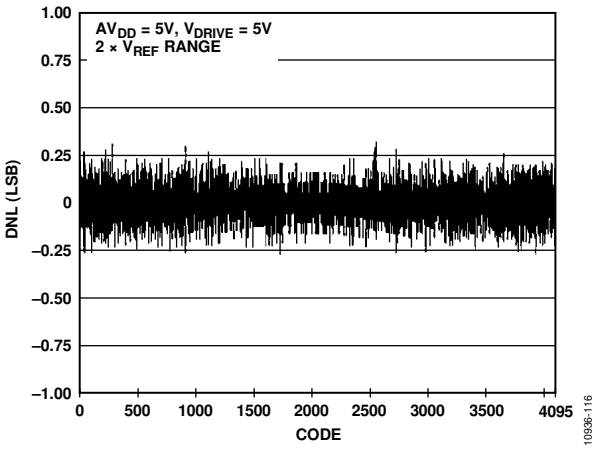


Figure 16. ADC DNL, Differential Input, 2 × V_{REF} Range

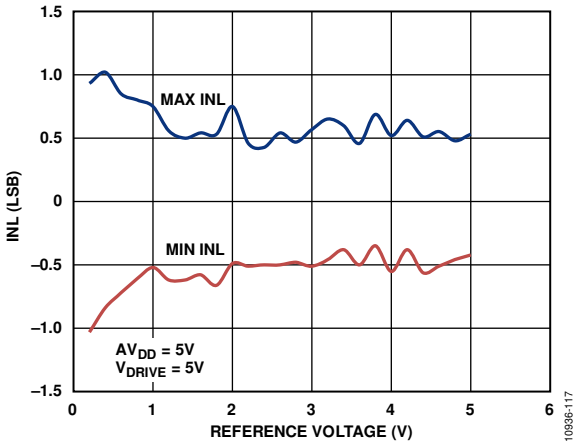


Figure 17. ADC INL vs. Reference Voltage

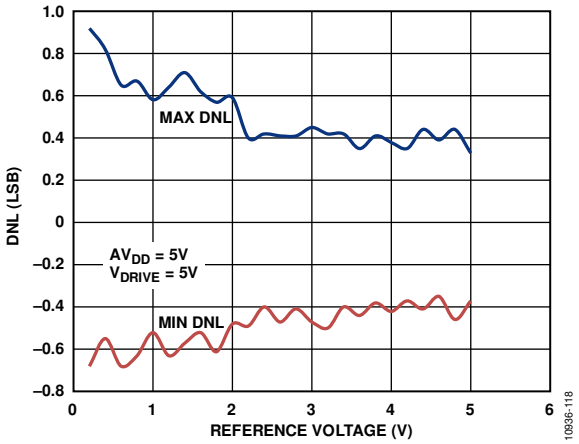


Figure 18. ADC DNL vs. Reference Voltage

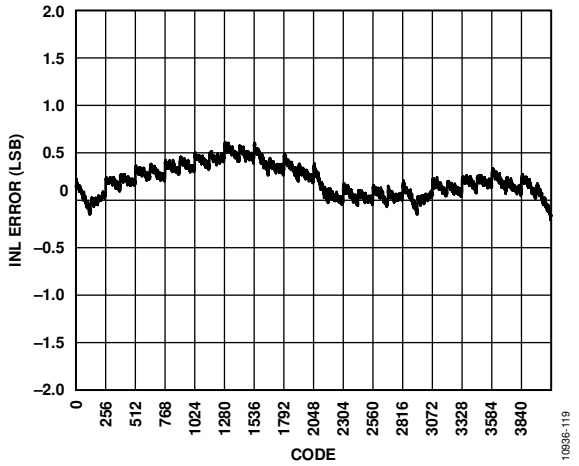


Figure 19. DAC INL

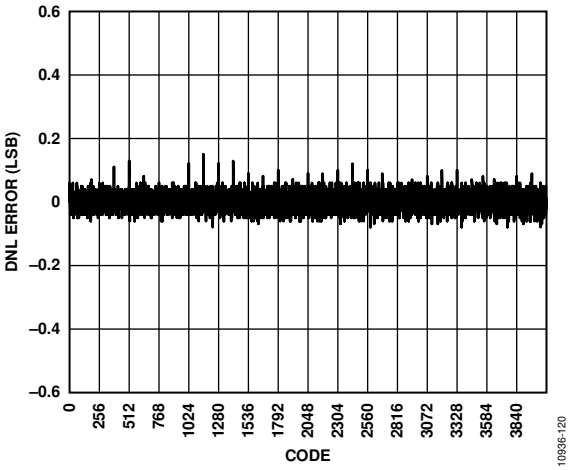


Figure 20. DAC DNL

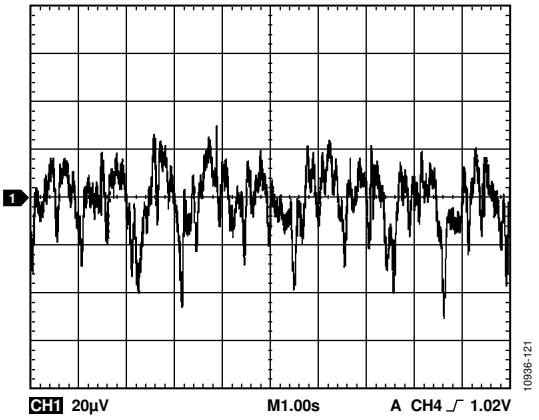


Figure 21. 0.1 Hz to 10 Hz DAC Output Noise, Input Code = 0x800

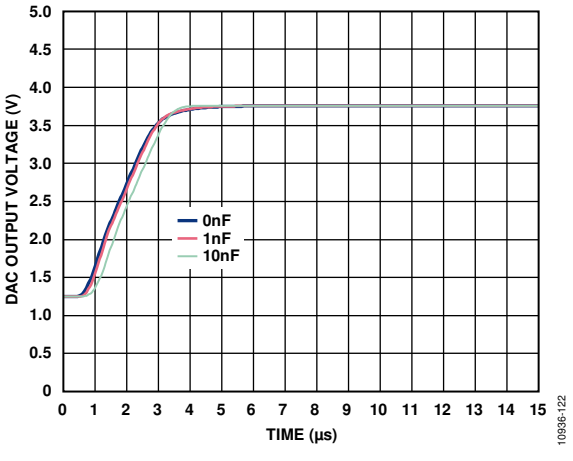


Figure 22. Settling Time for a ¼ to ¾ Output Voltage Step

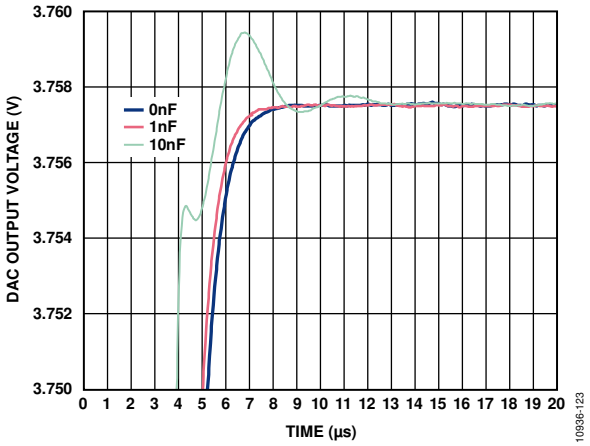


Figure 23. Zoomed-In Settling Time for a ¼ to ¾ Output Voltage Step

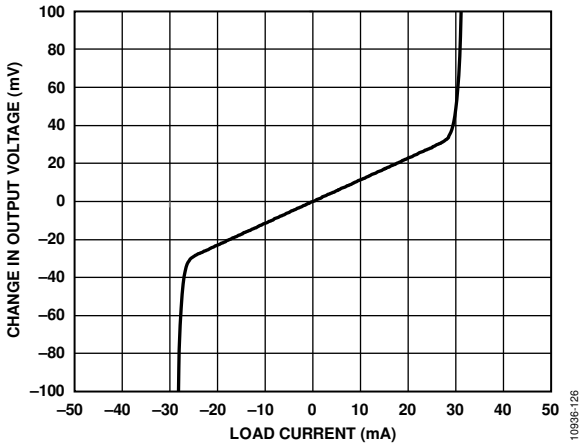


Figure 26. DAC Output Voltage vs. Load Current, Input Code = 0x800

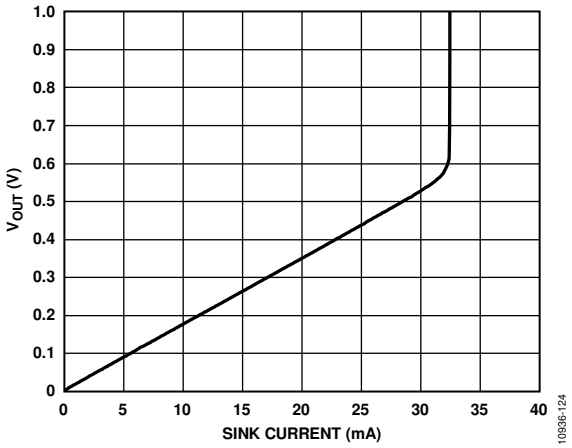


Figure 24. DAC Sinking Current at Input Code = 0x000, (V_{OUT} = 0 V)

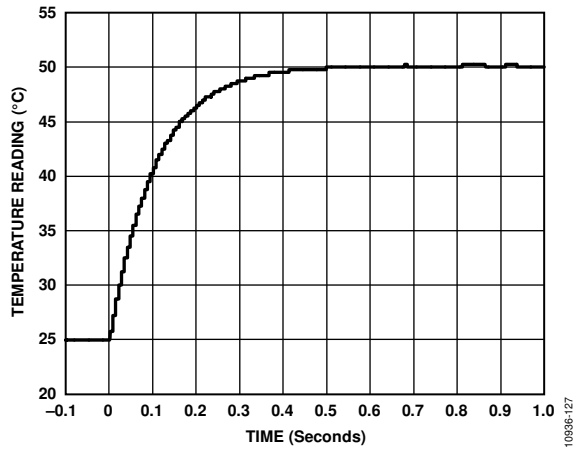


Figure 27. Response of Temperature Sensor to a Step Function

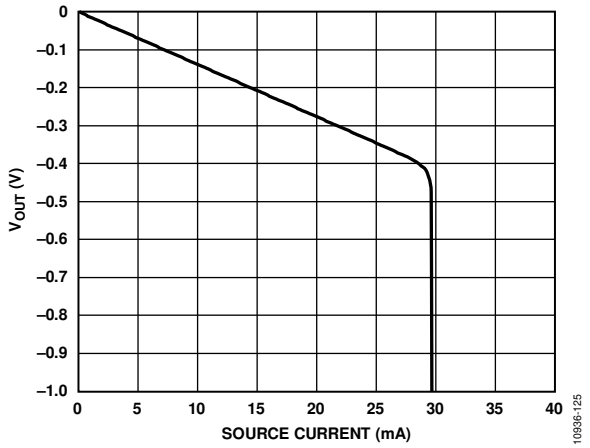


Figure 25. DAC Sourcing Current at Input Code = 0xFFF, (V_{OUT} = AV_{DD})

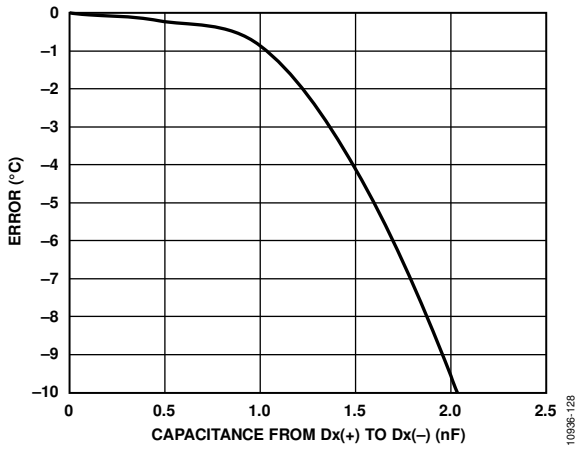


Figure 28. Temperature Error vs. Capacitance from Dx(+) to Dx(–)

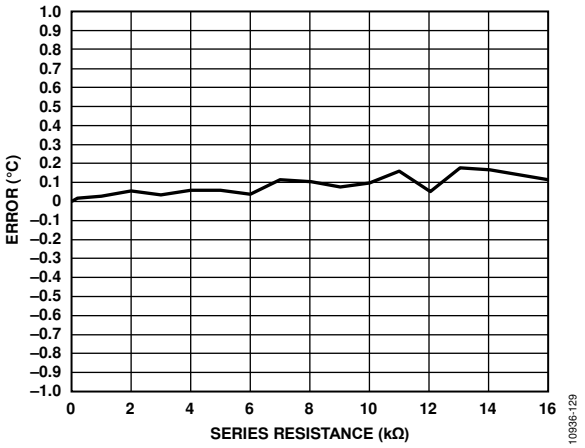


Figure 29. Temperature Error vs. Series Resistance

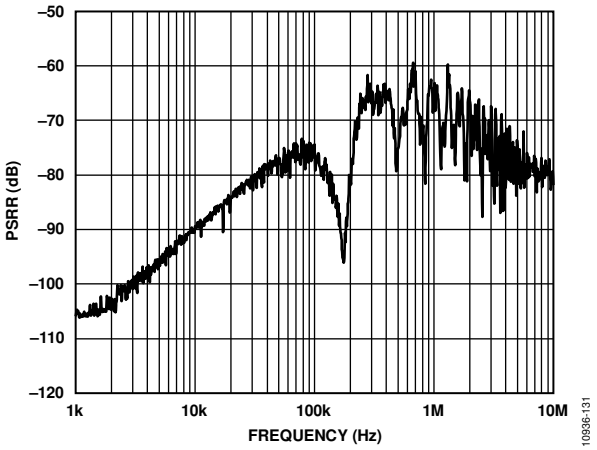


Figure 31. I_{SENSE} Power Supply Rejection Ratio (PSRR) vs. Supply Ripple Frequency Without V_{PP} Supply Decoupling Capacitors for a 500 mV Ripple

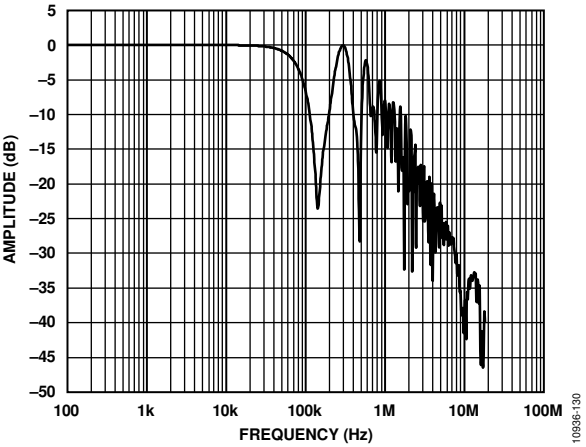


Figure 30. Frequency Response of the High-Side Current Sensor

TERMINOLOGY

DAC TERMINOLOGY

Relative Accuracy
A measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity (DNL)
The difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design.

Zero Code Error
A measure of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero code error is always positive in the AD7294-2 because the output of the DAC cannot go below 0 V. Zero code error is expressed in mV.

Full-Scale Error
A measure of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed in mV.

Gain Error
A measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal, expressed as a percent of the full-scale range (% FSR).

Gain Error Drift
A measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

ADC TERMINOLOGY

Signal-to-Noise-and-Distortion Ratio (SINAD)
The measured ratio of signal-to-noise and distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise-and-distortion ratio for an ideal N-bit converter with a sine wave input is given by

Signal-to-Noise-and-*Distortion* = (6.02 *N* + 1.76) dB

Thus, the SINAD is 74 dB for an ideal 12-bit converter.

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. For the AD7294-2, THD is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^{\,2}+V_3^{\,2}+V_4^{\,2}+V_5^{\,2}+V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics.

Integral Nonlinearity (INL)
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity (DNL)
The difference between the measured change and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (00…000) to (00…001) from the ideal—that is, AGND + 1 LSB.

Offset Error Match
The difference in offset error between any two channels.

Gain Error
The deviation of the last code transition (111 … 110 to 111 … 111) from the ideal (that is, REF_{IN} − 1 LSB) after the offset error has been adjusted out.

Gain Error Match
The difference in gain error between any two channels.

THEORY OF OPERATION

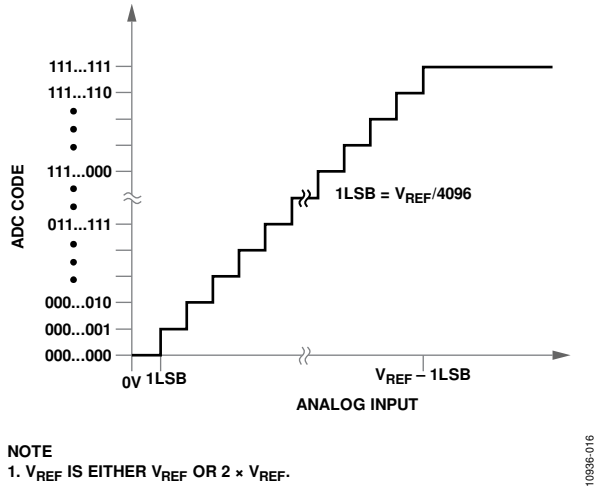
ADC OVERVIEW

The AD7294-2 provides the user with a 9-channel multiplexer, an on-chip track-and-hold, and a successive approximation ADC based on four capacitive DACs. The analog input range for the part can be selected as a 0 V to V_{REF} input or a 2 × V_{REF} input, configured with either single-ended or differential analog inputs. An on-chip 2.5 V reference can be disabled when an external reference is preferred. If the internal ADC reference is to be used elsewhere in a system, the output must first be buffered.

The various monitored and uncommitted input signals are multiplexed into the ADC. The AD7294-2 has four uncommitted analog input channels, $V_{IN}0$ to $V_{IN}3$. These four channels allow single-ended, differential, and pseudo differential mode measurements of various system signals.

ADC TRANSFER FUNCTIONS

The designed code transitions occur at successive integer LSB values (1 LSB, 2 LSB, and so on). In single-ended mode, the LSB size is $V_{REF}/4096$ when the 0 V to V_{REF} range is used, and 2 × $V_{REF}/4096$ when the 0 V to 2 × V_{REF} range is used. The ideal transfer characteristic for the ADC, when outputting straight binary coding, is shown in Figure 32.



NOTE
1. V_{REF} IS EITHER V_{REF} OR 2 × V_{REF}.

Figure 32. Single-Ended Transfer Characteristics

In differential mode, the LSB size is 2 × $V_{REF}/4096$ when the 0 V to V_{REF} range is used, and 4 × $V_{REF}/4096$ when the 0 V to 2 × V_{REF} range is used. The ideal transfer characteristic for the ADC, when outputting twos complement coding, is shown in Figure 33 (with the 2 × V_{REF} range).

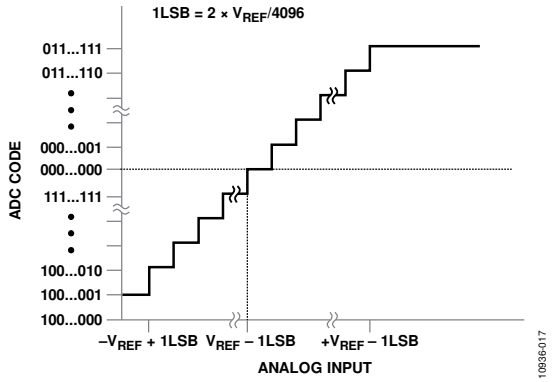


Figure 33. Differential Transfer Characteristics with V_{REF} ± V_{REF} Input Range

For $V_{IN}0$ to $V_{IN}3$ in single-ended mode, the output code is straight binary, where

V_{IN} = 0 V, D_{OUT} = x000, V_{IN} = V_{REF} − 1 LSB, and D_{OUT} = 0xFFF

In differential mode, the code is twos complement, where
$V_{IN+} - V_{IN-}$ = 0 V, and D_{OUT} = 0x00
$V_{IN+} - V_{IN-}$ = V_{REF} − 1 LSB, and D_{OUT} = 00x7FF
$V_{IN+} - V_{IN-}$ = −V_{REF}, and D_{OUT} = 0x800

Channel 5 and Channel 6 (current sensor inputs) are twos complement, where

$V_{IN+} - V_{IN-}$ = 0 mV, and D_{OUT} = 0x000

$V_{IN+} - V_{IN-}$ = $V_{REF}/12.5$ − 1 LSB, and D_{OUT} = 0x7FF

$V_{IN+} - V_{IN-}$ = −$V_{REF}/12.5$, and D_{OUT} = 0x800

Channel 7 to Channel 9 (temperature sensor inputs) are twos complement with the LSB equal to 0.25°C, where

T_{IN} = 0°C, and D_{OUT} = 0x000
T_{IN} = +255.75°C, and D_{OUT} = 0x7FF
T_{IN} = −256°C, and D_{OUT} = 0x800

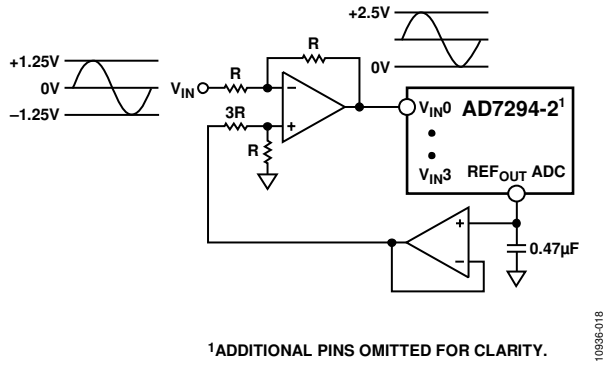
ANALOG INPUTS

The AD7294-2 has four analog inputs, $V_{IN}3$ to $V_{IN}0$. Depending on the configuration register setup, they can be configured as two single-ended inputs, two pseudo differential channels, or two fully differential channels (see the Register Settings section).

Single-Ended Mode

The AD7294-2 can have four single-ended analog input channels. In applications where the signal source has high impedance, it is recommended that the analog input be buffered before it is applied to the ADC. The analog input range can be programmed to either of the following modes: 0 V to V_{REF} or 0 V to 2 × V_{REF}. In 2 × V_{REF} mode, the input is effectively divided by 2 before the conversion takes place. Note that the voltage, with respect to GND on the ADC analog input pins, cannot exceed AV_{DD}.

If the analog input signal to be sampled is bipolar, the internal reference of the ADC can be used to externally bias up this signal so that it is correctly formatted for the ADC. Figure 34 shows a typical connection diagram when operating the ADC in single-ended mode.

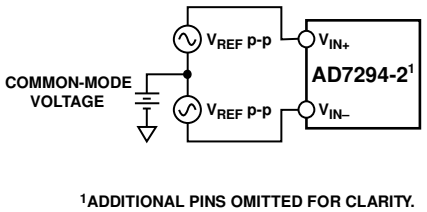


[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 34. Single-Ended Mode Connection Diagram

Differential Mode

The AD7294-2 can have two differential analog input pairs. Differential signals have some benefits over single-ended signals, including noise immunity based on the common-mode rejection of the device and improvements in distortion performance. Figure 35 defines the fully differential analog input of the AD7294-2.



[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 35. Differential Input Definition

The amplitude of the differential signal is the difference between the signals applied to V_{IN+} and V_{IN-} in each differential pair ($V_{IN+} - V_{IN-}$). The resulting converted data is stored in twos complement format in the result register.

Simultaneously drive $V_{IN}0$ and $V_{IN}1$ by two signals, each of amplitude V_{REF} (or 2 × V_{REF}, depending on the range chosen), that are 180° out of phase.

Assuming that the 0 V to V_{REF} range is selected, the amplitude of the differential signal is, therefore, $-V_{REF}$ to $+V_{REF}$ peak-to-peak (2 × V_{REF}), regardless of the common-mode voltage (V_{CM}).

The common-mode voltage is the average of the two signals.

$$(V_{IN+} + V_{IN-})/2$$

The common-mode voltage is, therefore, the voltage on which the two inputs are centered.

The result is that the span of each input is $V_{CM} \pm V_{REF}/2$. This common-mode voltage must be set up externally, and its range varies with the reference value, V_{REF}. As the value of V_{REF} increases, the common-mode range decreases. When driving the inputs with an amplifier, the actual common-mode range is determined by the output voltage swing of the amplifier.

The common-mode voltage must be within this common-mode range to guarantee the functionality of the AD7294-2.

When a conversion takes place, the common-mode voltage is rejected, resulting in a virtually noise-free signal of amplitude $-V_{REF}$ to $+V_{REF}$, corresponding to the digital output codes of −2048 to +2047 in twos complement format.

If the 2 × V_{REF} range is used, the input signal amplitude extends from −2 × V_{REF} (V_{IN+} = 0 V, V_{IN-} = V_{REF}) to +2 × V_{REF} (V_{IN-} = 0 V, V_{IN+} = V_{REF}).

Driving Differential Inputs

The differential modes that are available on $V_{IN}0$ to $V_{IN}3$ (see Table 10) require that V_{IN+} and V_{IN-} be driven simultaneously with two equal signals that are 180° out of phase. The common-mode voltage on which the analog input is centered must be set up externally. The common-mode range is determined by V_{REF}, the power supply, and the particular amplifier used to drive the analog inputs. Differential modes of operation with either an ac or dc input provide the best THD performance over a wide frequency range. Because not all applications have a signal that is preconditioned for differential operation, there is often a need to perform a single-ended-to-differential conversion.

Using an Op Amp Pair

An op amp pair can be used to directly couple a differential signal to one of the analog input pairs of the AD7294-2. The circuit configuration that is illustrated in Figure 38 shows how a dual op amp can be used to convert a single-ended bipolar signal into a differential unipolar input signal.

The voltage applied to Point A sets up the common-mode voltage. As shown in Figure 38, Point A connects to the reference, but any value in the common-mode range can be the input at Point A to set up the common-mode voltage. The AD8022 is a suitable dual op amp that can be used in this configuration to provide differential drive to the AD7294-2.

Care is required when choosing the op amp because the selection depends on the required power supply and system performance objectives. The driver circuit in Figure 38 is optimized for dc coupling applications that require best distortion performance.

The differential op amp driver circuit shown in Figure 38 is configured to convert and level shift a single-ended, ground referenced (bipolar) signal to a differential signal that is centered at the V_{REF} level of the ADC.

Pseudo Differential Mode

The four uncommitted analog input channels can be configured as two pseudo differential pairs. Two uncommitted inputs, $V_{IN}0$ and $V_{IN}1$, are a pseudo differential pair, as are $V_{IN}2$ and $V_{IN}3$. In this mode, V_{IN+} is connected to the signal source, which can have a maximum amplitude of V_{REF} (or $2 \times V_{REF}$, depending on the range that is chosen) to make use of the full dynamic range of the part. A dc input is applied to V_{IN-}. The voltage applied to this input provides an offset from ground or a pseudo ground for the V_{IN+} input. The channel specified as V_{IN+} is determined by the ADC channel allocation. The differential mode must be selected to operate in the pseudo differential mode. The resulting converted pseudo differential data is stored in twos complement format in the result register.

For $V_{IN}0$, the governing equation for the pseudo differential mode is

$$V_{OUT} = 2(V_{IN+} - V_{IN-}) - V_{REF\_ADC}$$

where V_{IN+} is the single-ended signal and V_{IN-} is a dc voltage.

The benefit of pseudo differential inputs is that they separate the analog input signal ground from the ADC ground, allowing dc common-mode voltages to be cancelled.

Figure 36 shows the typical voltage range for V_{IN-} while in pseudo differential mode, and Figure 37 shows a connection diagram for pseudo differential mode.

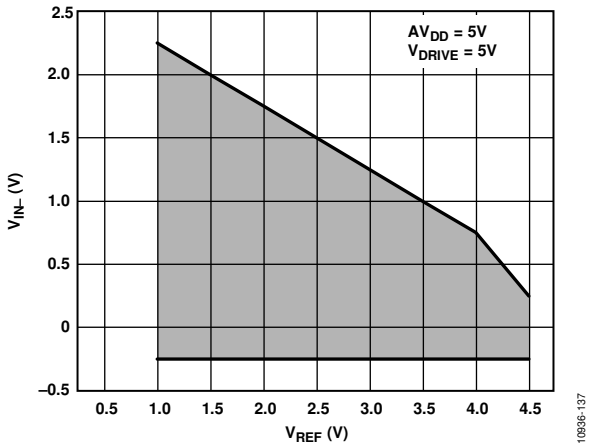


Figure 36. V_{IN-} Input Range vs. V_{REF} in Pseudo Differential Mode

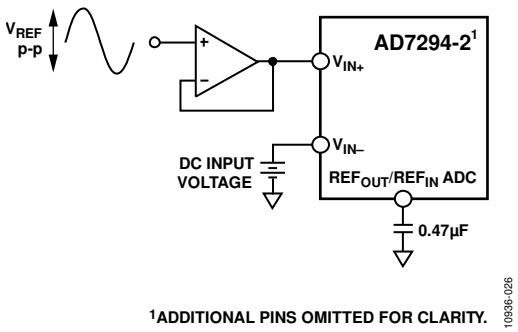


Figure 37. Pseudo Differential Mode Connection Diagram

CURRENT SENSOR

Two bidirectional high-side current sense amplifiers are provided that can accurately amplify differential current shunt voltages in the presence of high common-mode voltages from AV_{DD} up to 59.4 V. Each amplifier can accept a ±200 mV differential input. Both current sense amplifiers have a fixed gain of 12.5 and use an internal 2.5 V reference.

An analog comparator is also provided with each amplifier for fault detection. The threshold is defined as

$$1.2 \times \textit{Full-Scale Voltage Range}$$

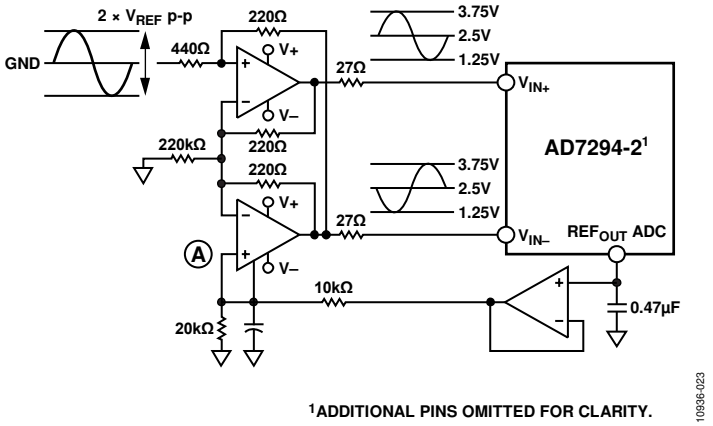


Figure 38. Dual Op Amp Circuit to Convert a Single-Ended Bipolar Signal into a Differential Unipolar Signal

When this limit is reached, the output is latched onto a dedicated pin. This output remains high until the latch is cleared by writing to the appropriate register.

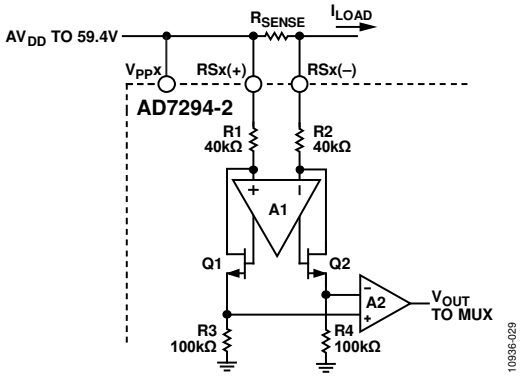


Figure 39. High-Side Current Sense

The AD7294-2 current sense comprises two main blocks: a differential and an instrumentation amplifier. A load current flowing through the external shunt resistor produces a voltage at the input terminals of the AD7294-2. Resistors R1 and R2 connect the input terminals to the differential amplifier (A1). A1 nulls the voltage that appears across its own input terminals by adjusting the current through R1 and R2 with Transistors Q1 and Q2. Common-mode feedback maintains the sum of these currents at approximately 50 µA. When the input signal to the AD7294-2 is zero, the currents in R1 and R2 are equal. When the differential signal is nonzero, the current increases through one of the resistors and decreases in the other. The current difference is proportional to the size and polarity of the input signal.

The differential currents through Q1 and Q2 are converted into a differential voltage by R3 and R4. A2 is configured as an instrumentation amplifier, buffering this voltage and providing additional gain. Therefore, for an input voltage of ±200 mV at the pins, an output span of ±2.5 V is generated.

The current sensors on the AD7294-2 are designed to remove any flicker noise and offset that are present in the sensed signal. This is achieved by using a chopping technique that is transparent to the user. The V_{SENSE} signal is first converted by the AD7294-2, the analog inputs to the amplifiers are then swapped, and the differential voltage is once again converted by the AD7294-2.

The two conversion results enable the digital removal of any offset or noise. Switches on the amplifier inputs enable this chopping technique to be implemented. The process typically requires 6 µs, in total, to return a final result.

Choosing R_{SENSE}

The resistor values used in conjunction with the current sense amplifiers are determined by the specific application requirements in terms of voltage, current, and power. Small resistors minimize power dissipation, have low inductance to prevent any induced voltage spikes, and provide good tolerance, which reduces current variations. The final values chosen are a compromise between low power dissipation and good accuracy. Low value resistors have less power dissipated in them, but higher value resistors may be required to use the full input range of the ADC, thus achieving maximum SNR performance.

When the sense current is known, the voltage range of the AD7294-2 current sensor (200 mV) is divided by the maximum sense current to yield a suitable shunt value. If the power dissipation in the shunt resistor is too large, the size of the shunt resistor can be reduced; in this case, less of the ADC input range is used. Using less of the ADC input range produces conversion results that are more susceptible to noise and offset errors because offset errors are fixed and are, thus, more significant when smaller input ranges are used.

R_{SENSE} must be able to dissipate the I^2R losses. If the power dissipation rating of the resistor is exceeded, its value may drift or the resistor may be damaged, resulting in an open circuit. This open circuit can cause a differential voltage across the terminals of the AD7294-2 in excess of the absolute maximum ratings. Additional protection is afforded to the current sensors on the AD7294-2 by the recommended current limiting resistors, RF1 and RF2, as shown in Figure 40. The AD7294-2 can handle a maximum continuous current of 30 mA; thus, an RF2 of 1 kΩ provides adequate protection for the AD7294-2.

If I_{SENSE} has a large high frequency component, take care to choose a resistor with low inductance. Low inductance metal film resistors are best suited for these applications.

Current Sense Filtering

In some applications, it may be desirable to use external filtering to reduce the input bandwidth of the amplifier (see Figure 40). The −3 dB differential bandwidth of this filter is equal to

$$BW_{DM} = 1/(4 \times \pi \times RC)$$

Note that the maximum series resistance on the RS(+) and RS(−) inputs (see Figure 39) is limited to a maximum of 1 kΩ due to back-to-back ESD protection diodes from RS(+) and RS(−) to $V_{PP}x$. Also, note that if RF1 and RF2 are in series with R1 and R2 (see Figure 39), the gain of the amplifier is affected. Any mismatch between RF1 and RF2 can introduce an offset error.

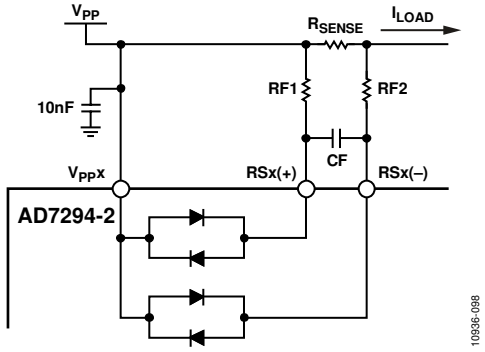


Figure 40. Current Sense Filtering (RSx Can Be Either RS1 or RS2)

For certain RF applications, the optimum value for RF1 and RF2 is 1 kΩ, whereas CF can range from 1 µF to 10 µF. There is an additional decoupling capacitor for the $V_{PP}x$ supply. Its value is application dependent, but for initial evaluation, values in the range of 1 nF to 100 nF are recommended.

Kelvin Sense Resistor Connection

When using a low value sense resistor for high current measurement, the problem of parasitic series resistance can arise. The lead resistance can be a substantial fraction of the rated resistance, making the total resistance a function of lead length. Avoid this problem by using a Kelvin sense connection. This type of connection separates the current path through the resistor and the voltage drop across the resistor. Figure 41 shows the correct way to connect the sense resistor between the RS(+) and RS(−) pins of the AD7294-2.

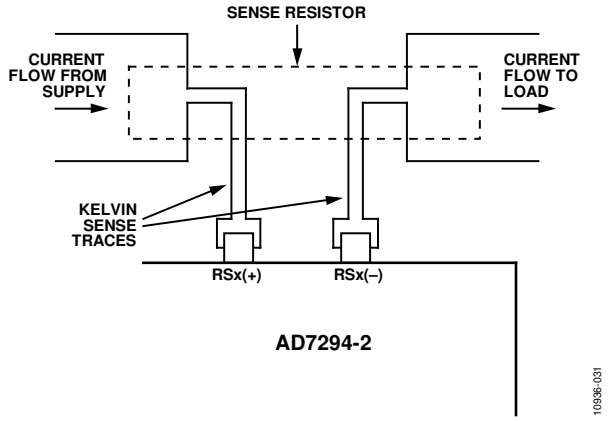


Figure 41. Kelvin Sense Connections (RSx Can Be Either RS1 or RS2)

ANALOG COMPARATOR LOOP

The AD7294-2 contains two setpoint comparators that are used for independent analog control. This circuitry enables users to quickly detect if the sensed voltage across the shunt resistor has increased above the preset ($V_{REF} \times 1.2$)/12.5. If this increase occurs, the $I_{SENSE}x$ OVERRANGE pin is set to a high logic level, enabling appropriate action to be taken to prevent any damage to the external circuitry.

The setpoint threshold level is fixed internally in the AD7294-2, and the current sense amplifier saturates above this level. The comparator is also triggered if a voltage of less than AV_{DD} is applied to the R_{SENSE} resistor or the $V_{PP}x$ pin.

TEMPERATURE SENSOR

The AD7294-2 contains one local and two remote temperature sensors. The temperature sensors continuously monitor the three temperature inputs, and new readings are automatically available every 5 ms.

The on-chip, band gap temperature sensor measures the temperature of the system. Diodes are used in conjunction with the two remote temperature sensors to monitor the temperature of other critical board components.

The temperature sensor module on the AD7294-2 is based on the three-current principle (see Figure 42), where three currents are passed through a diode and the forward voltage drop is measured at each diode, allowing the temperature to be calculated free of errors caused by series resistance.

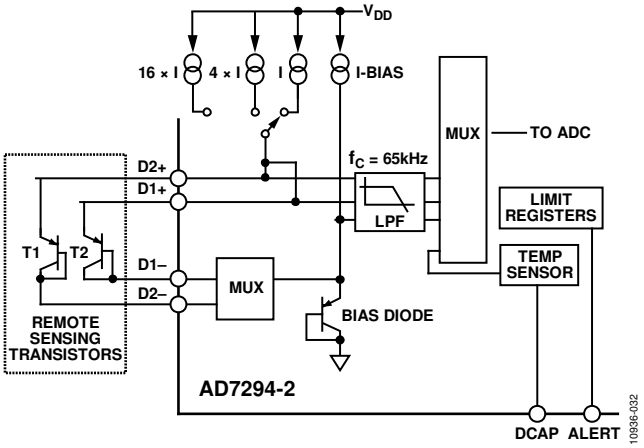


Figure 42. Internal and Remote Temperature Sensors

Each input integrates, in turn, over a period of several hundred microseconds (µs). This integration takes place continuously in the background, leaving the user free to perform conversions on the other channels. When the integration is complete, a signal passes to the control logic to initiate a conversion automatically. If the ADC is in command mode, the temperature conversion is performed as soon as the next conversion is completed. In auto-cycle mode, the conversion is inserted into an appropriate place in the current sequence (see the Register Settings section for further details. If the ADC is idle, the conversion takes place immediately.

Three registers store the result of the last conversion on each temperature channel; these can be read at any time. In addition, in command mode, one or both of the two external channel registers can be read out as part of the output sequence.

Remote Sensing Diode

The AD7294-2 is designed to work with discrete transistors, 2N3904 and 2N3906. If an alternative transistor is used, the AD7294-2 operates as specified, provided that the conditions explained in the following sections are adhered to.

Ideality Factor

The ideality factor of the transistor, n_f, is a measure of the deviation of the thermal diode from ideal behavior. The AD7294-2 is trimmed for an n_f value of 1.008. Use the following equation to calculate the error introduced at a Temperature T (°C) when using a transistor whose n_f does not equal 1.008:

$$\Delta T = (n_f - 1.008) \times (273.15\ \text{K} + T)$$

To factor in this error, the user can write the ΔT value to the offset register. The AD7294-2 automatically adds it to, or subtracts it from, the temperature measurement.

Base Emitter Voltage

The AD7294-2 operates as specified if the base emitter voltage is greater than 0.25 V at 8 µA at the highest operating temperature, and less than 0.95 V at 128 µA for the lowest operating temperature.

h_{FE} Variation

Use a transistor with little variation in h_{FE} (~50 to 150). Little variation in h_{FE} indicates tight control of the V_{BE} characteristics.

For RF applications, the use of high Q capacitors, functioning as a filter, protects the integrity of the measurement. Connect these capacitors, such as Johanson Technology 10 pF, high Q capacitors, Reference Code 500R07S100JV4T, between the base and the emitter, as close to the external device as possible. However, large capacitances affect the accuracy of the temperature measurement; thus, the recommended maximum capacitor value is 100 pF. In most cases, a capacitor is not required; the selection of any capacitor is dependent on the noise frequency level.

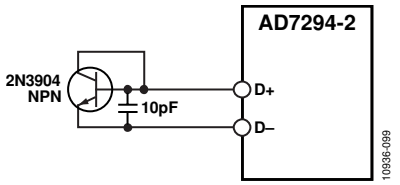


Figure 43. Measuring Temperature Using an NPN Transistor

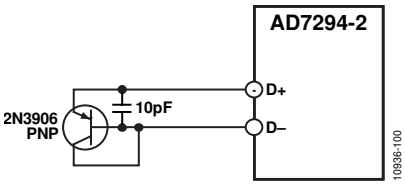


Figure 44. Measuring Temperature Using a PNP Transistor

Series Resistance Cancellation

The AD7294-2 is designed to automatically cancel out the effect of parasitic, base, and collector resistance on the temperature reading. This feature provides a more accurate result, without the need for any user characterization of the parasitic resistance. The AD7294-2 can compensate for up to 10 kΩ in a process that is transparent to the user.

DAC OPERATION

The AD7294-2 contains four 12-bit DACs that provide digital control with 12 bits of resolution and a 2.5 V internal reference. The DAC core is a thin film 12-bit string DAC with a 5 V output span and an output buffer that can drive the high voltage output stage. The DAC has a span of 0 V to 5 V with a 2.5 V reference input. The output range of the DAC, which is controlled by the offset input, can be positioned from 0 V to 15 V.

Resistor String

The resistor string structure is shown in Figure 45. It consists of a string of 2^n resistors, each of Value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. This architecture is inherently monotonic, voltage out, and low glitch. It is also linear because all of the resistors are of equal value.

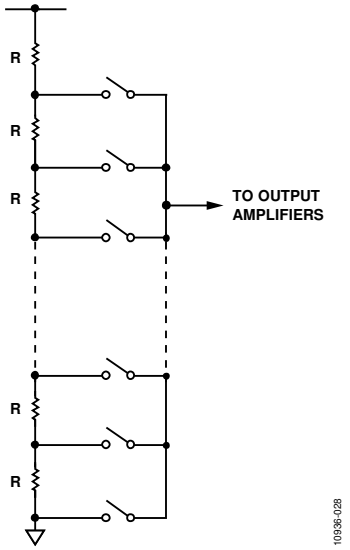


Figure 45. Resistor String Structure

Output Amplifiers

The purpose of Op Amp A1 is to buffer the DAC output range from 0 V to V_{REF}. A second amplifier, Op Amp A2, is configured such that when an offset is applied to OFFSET IN x, its output voltage is 3× the offset voltage minus 2× the DAC voltage.

$$V_{OUT} = 3 \times V_{OFFSET} - 2 \times V_{DAC}$$

The DAC word is digitally inverted on chip such that

$$V_{OUT} = 3 \times V_{OFFSET} + 2 \times (V_{DAC} - V_{REF})$$

$$\text{and } V_{DAC} = \left[V_{REF} \times \left(\frac{D}{2^n} \right) \right]$$

where:
V_{DAC} is the output of the DAC before digital inversion.
D is the decimal equivalent of the binary code that is loaded to the DAC register.
n is the bit resolution of the DAC.

An example of the offset function is given in Table 8.

Table 8. Offset Voltage Function Example

Offset Voltage (V)	V_{OUT} with 0x000 (V)	V_{OUT} with 0xFFF (LSB)
1.67	0	5 V – 1
3.33	5	10 V – 1
5.00	10	15 V – 1

The user has the option of leaving the offset pin open, in which case the voltage on the noninverting input of Op Amp A2 is set by the resistor divider, giving

$$V_{OUT} = 2 \times V_{DAC}$$

This configuration generates the 5 V output span from a 2.5 V reference. Digitally inverting the DAC allows the circuit to operate as a generic DAC when no offset is applied. If the offset pin is not driven, it is best practice to place a 100 nF capacitor between the pin and ground to improve both the settling time and the noise performance of the DAC.

Note that a significant amount of power can be dissipated in the DAC outputs.

ADC AND DAC REFERENCE

The AD7294-2 has two independent, internal, high performance 2.5 V references, one for the ADC and the other for the four on-chip DACs. If the application requires an external reference, it can be applied to the REF_{OUT}/REF_{IN} DAC pin and/or to the REF_{OUT}/REF_{IN} ADC pin. Buffer the internal reference before it is used by external circuitry. Decouple both the REF_{OUT}/REF_{IN} DAC pin and the REF_{OUT}/REF_{IN} ADC pin to AGND, using a 220 nF capacitor. On power-up, the AD7294-2 is configured for use with an external reference. To enable the internal references, write a zero to both the D4 and D5 bits in the power-down register (see the Register Settings section). Both the ADC and DAC references require a minimum of 60 µs to power up and settle to 12-bit performance when a 220 nF decoupling capacitor is used.

The AD7294-2 can also operate with an external reference. Suitable reference sources for the AD7294-2 include the AD780, AD1582, ADR431, REF193, and ADR391. In addition, choosing a reference with an output trim adjustment, such as the ADR441, allows a system designer to trim system errors by setting a reference voltage to a voltage other than the nominal.

Long-term drift is a measure of how much the reference drifts over time. A reference with a low long-term drift specification ensures that the overall solution remains stable during its entire lifetime. If an external reference is used, select a low temperature coefficient specification to reduce the temperature dependence of the system output voltage on ambient conditions.

V_{DRIVE} FEATURE

The AD7294-2 also has a V_{DRIVE} feature to control the voltage at which the I^2C interface operates. The V_{DRIVE} pin is connected to the supply to which the I^2C bus is pulled. This pin sets the input and output threshold levels for the digital logic pins and the $I_{SENSE}x$ OVERRANGE pins. The V_{DRIVE} feature allows the AD7294-2 to easily interface to both 3 V and 5 V processors.

For example, if the AD7294-2 is operated with a V_{DD} of 5 V, the V_{DRIVE} pin can be powered from a 3 V supply, allowing a large dynamic range with low voltage digital processors. Thus, the AD7294-2 can be used with the $2 \times V_{REF}$ input range with a V_{DD} of 5 V, yet it remains capable of interfacing to 3 V digital parts. Decouple the V_{DRIVE} pin to DGND with a 100 nF capacitor and a 1 µF capacitor.