Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

LC²MOS
µP Compatible 14-Bit DAC
AD7535

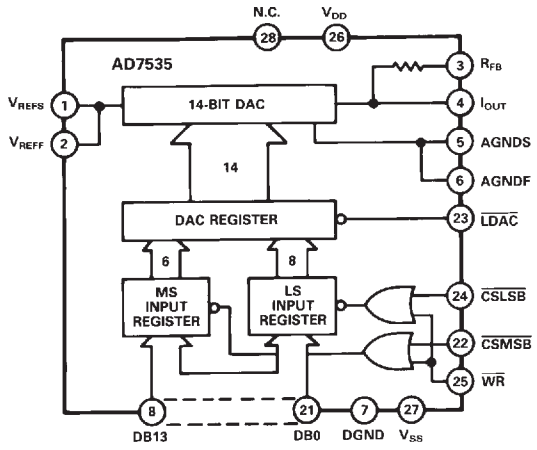
FEATURES

All Grades 14-Bit Monotonic over the Full Temperature Range
Full 4 Quadrant Multiplication
Microprocessor Compatible with Double Buffered Inputs
Exceptionally Low Gain Temperature Coefficient, 0.5ppm/°C typ
Low Output Leakage (<20nA) over the Full Temperature Range

APPLICATIONS

Microprocessor Based Control Systems
Digital Audio
Precision Servo Control
Control and Measurement in High Temperature Environments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7535 is a 14-bit monolithic CMOS D/A converter which uses laser trimmed thin-film resistors to achieve excellent linearity.

Standard Chip Select and Memory Write logic is used to access the DAC.

A novel low leakage configuration (patent pending) enables the AD7535 to exhibit excellent output leakage current characteristics over the specified temperature range.

The device is fully protected against CMOS "latch up" phenomena and does not require the use of external Schottky diodes or the use of a FET Input op-amp. The AD7535 is manufactured using the Linear Compatible CMOS (LC^2MOS) process. It is speed compatible with most microprocessors and accepts TTL or CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. Guaranteed Monotonicity
   The AD7535 is guaranteed monotonic to 14-bits over the full temperature range for all grades.
2. Low Output Leakage
   By tying V_{SS} (Pin 27) to a negative voltage, it is possible to achieve a low output leakage current at high temperatures.
3. Microprocessor Compatibility
   High speed input control (TTL/5V CMOS compatible) allows direct interfacing to most of the popular 8-bit and 16-bit microprocessors. When interfacing to 8-bit processors $\overline{CSMSB}$ and $\overline{CSLSB}$ are separate and the 8-bit data bus is connected to both the MS Input Register and the LS Input Register. For straight 14-bit parallel loading $\overline{CSMSB}$ and $\overline{CSLSB}$ are tied together giving one chip select to load the 14-bit word.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
West Coast 714/641-9391 Central 214/231-5094 Atlantic 215/643-7790

AD7535* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-137: A Digitally Programmable Gain and Attenuation Amplifier Design
- AN-314: 14-Bit DACs Maintain High Performance Over Extended Temperature Range
- AN-320A: CMOS Multiplying DACs and Op Amps Combine to Build Programmable Gain Amplifier, Part 1
- AN-912: Driving a Center-Tapped Transformer with a Balanced Current-Output DAC

Data Sheet

- AD7535: LC^{2}MOS µP Compatible 14-Bit DAC Data Sheet

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

DESIGN RESOURCES

- AD7535 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7535 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

AD7535—SPECIFICATIONS[1] (V_{DD} = +11.4V to +15.75V[2], V_{REF} = +10V; V_{PIN4} = V_{PIN5} = 0V, V_{SS} = −300mV All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic
Differential Nonlinearity	±1	±1	±1	±1	LSB max	over temperature.
Full Scale Error	±8	±4	±8	±4	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain T.C.
Gain Temperature Coefficient[3]; ΔGain/ΔTemperature	±5	±2.5	±5	±2.5	ppm/°C max	Typical value is 0.5ppm/°C
Output Leakage Current I_{OUT} (Pin 4)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs 0V
T_{min} to T_{max}	±10	±10	±20	±20	nA max	V_{SS} = −300mV
T_{min} to T_{max}	±25	±25	±150	±150	nA max	V_{SS} = 0V
REFERENCE INPUT						
Input resistance, pin 1	3.5	3.5	3.5	3.5	kΩ min	Typical Input Resistance = 6kΩ
	10	10	10	10	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V_{min}/V_{max}	Specification guaranteed over
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/mV max	this range
I_{DD}	4	4	4	4	mA max	All digital inputs V_{IL} or V_{IH}
	500	500	500	500	μA max	All digital inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test. (V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN4} = V_{PIN5} = 0V, V_{SS} = 0V OR −300mV, Output Amplifier is AD544 except where stated.)

Parameter	T_A = 25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.003% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's. Typical value of Settling Time is 0.8μs.
Digital to Analog Glitch Impulse	50	–	nV-sec typ	Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's.
Multiplying Feedthrough Error[4]	3	5	mV p-p typ	V_{REF} = ±10V, 10kHz sine wave DAC register loaded with all 0's.
Power Supply Rejection ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUT} (Pin 4)	260	260	pF max	DAC register loaded with all 1's
C_{OUT} (Pin 4)	130	130	pF max	DAC register loaded with all 0's
Output Noise Voltage Density (10Hz–100kHz)	15	–	nV$\sqrt{Hz}$ typ	Measured between R_{FB} and I_{OUT}

NOTES
[1]Temperature range as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C
[2]Specifications are guaranteed for a V_{DD} of +11.4V to +15.75V. At V_{DD} = 5V, the device is fully functional with degraded specifications.
[3]Guaranteed by Product Assurance testing.
[4]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1]

(V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN4} = V_{PIN5} = 0V, V_{SS} = 0V or −300mV
All specifications T_{min} to T_{max} unless otherwise stated. See Figure 1 for Timing Diagram.)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time
t_2	0	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time
t_3	170	200	240	ns min	LDAC Pulse Width
t_4	170	200	240	ns min	Write Pulse Width
t_5	140	160	180	ns min	Data Setup Time
t_6	20	20	30	ns min	Data Hold Time

NOTES
[1]Temperature range as follows: JN, KN Versions: 0 to +70°C
AQ, BQ Versions: −25°C to +85°C
SQ, TQ Versions: −55°C to +125°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise stated)

V_{DD} (pin 26) to DGND . . . . . −0.3V, +17V
V_{SS} (pin 27) to AGND . . . . . −15V, +0.3V
V_{REFS} (pin 1) to AGND . . . . . ±25V
V_{REFF} (pin 2) to AGND . . . . . ±25V
V_{RFB} (pin 3) to AGND . . . . . ±25V
Digital Input Voltage (pins 8–25) to DGND . . −0.3V, V_{DD}
V_{PIN4} to DGND . . . . . −0.3V, V_{DD}
AGND to DGND . . . . . −0.3V, V_{DD}
Power Dissipation (Any Package)
To +75°C 1000mW
Derates above +75°C . . . . . 10mW/°C

Operating Temperature Range
Commercial Plastic (J, K Versions) . . . . . 0 to +70°C
Industrial Ceramic (A, B Versions) . . . . −25°C to +85°C
Extended Ceramic (S, T Versions) . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Full-Scale Error	Package Option*
AD7535JN	0°C to +70°C	±2LSB	±8LSB	N-28
AD7535KN	0°C to +70°C	±1LSB	±4LSB	N-28
AD7535JP	0°C to +70°C	±2LSB	±8LSB	P-28A
AD7535KP	0°C to +70°C	±1LSB	±4LSB	P-28A
AD7535AQ	−25°C to +85°C	±2LSB	±8LSB	Q-28
AD7535BQ	−25°C to +85°C	±1LSB	±4LSB	Q-28
AD7535SQ	−55°C to +125°C	±2LSB	±8LSB	Q-28
AD7535TQ	−55°C to +125°C	±1LSB	±4LSB	Q-28
AD7535SE	−55°C to +125°C	±2LSB	±8LSB	E-28A
AD7535TE	−55°C to +125°C	±1LSB	±4LSB	E-28A

*E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for zero error and full scale error and is normally expressed in Least Significant Bits or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

FULL-SCALE ERROR

Full scale error or gain error is a measure of the output error between an ideal DAC and the actual device output. Full scale error is adjustable to zero with an external potentiometer.

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected from the digital inputs to the analog output when the inputs change state is called Digital-to-Analog Glitch Impulse. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. It is measured with V_{REF} = AGND.

OUTPUT CAPACITANCE

This is the capacitance from I_{OUT} to AGND.

OUTPUT LEAKAGE CURRENT

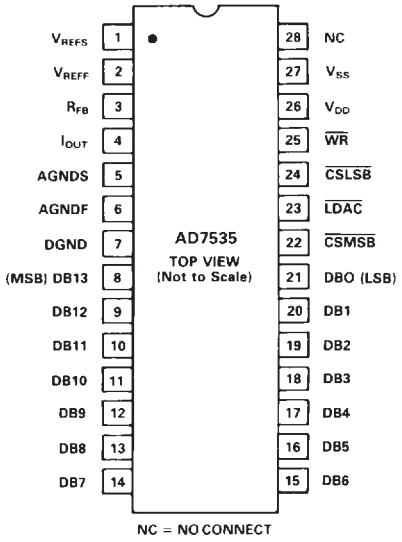
Output Leakage Current is current which appears at I_{OUT} with the DAC register loaded to all 0's.

MULTIPLYING FEEDTHROUGH ERROR

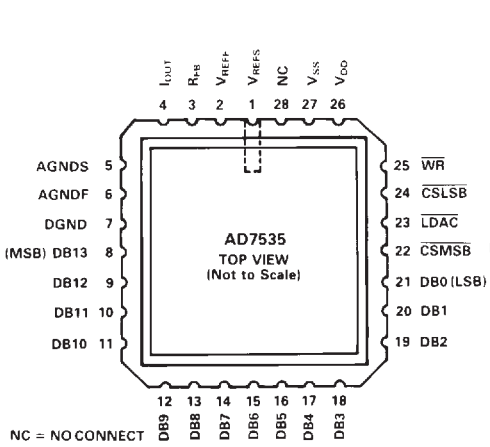
This is the ac error due to capacitive feedthrough from V_{REF} terminal to I_{OUT} with DAC register loaded to all zeros.

PIN CONFIGURATIONS

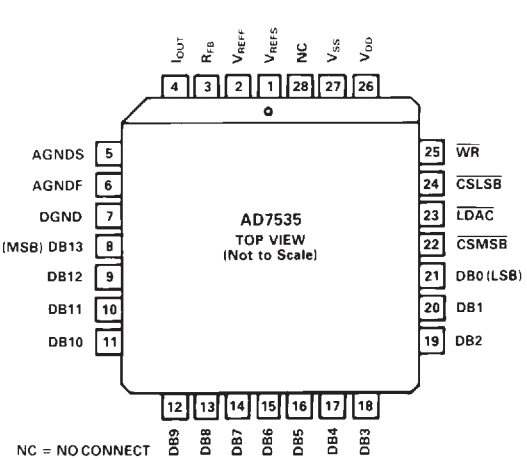
DIP



LCCC



PLCC

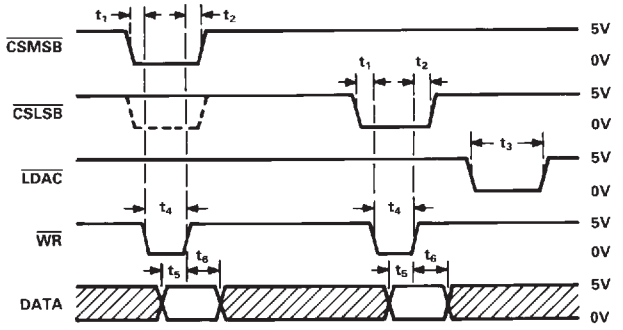


Pin	Function	Description
1	V_{REFS}	Voltage Reference sense pin
2	V_{REFF}	Voltage Reference force pin. If a remote voltage reference is being used V_{REFF} and V_{REFS} can be used in a Kelvin configuration to compensate for IR drop along the V_{REF} line. See Figure 7.
3	R_{FB}	Feedback resistor. Used to close the loop around an external op-amp.
4	I_{OUT}	Current Output Terminal.
5	A_{GNDS}	Analog ground sense line. Reference point for external circuitry. This pin should carry minimal current.
6	A_{GNDF}	Analog ground force line; carries current from internal analog ground connections. A_{GNDF} and A_{GNDS} are tied together internally.
7	DGND	Digital Ground
8	DB13	Data Bit 13. DAC MSB
9	DB12	Data Bit 12
10	DB11	Data Bit 11
11	DB10	Data Bit 10
12	DB9	Data Bit 9
13	DB8	Data Bit 8
14	DB7	Data Bit 7
15	DB6	Data Bit 6
16	DB5	Data Bit 5
17	DB4	Data Bit 4
18	DB3	Data Bit 3
19	DB2	Data Bit 2
20	DB1	Data Bit 1
21	DB0	Data Bit 0. DAC LSB
22	$\overline{CSMSB}$	Chip Select Most Significant (MS) Byte. Active LOW input.
23	$\overline{LDAC}$	Asynchronous Load DAC input. Active LOW.
24	$\overline{CSLSB}$	Chip Select Least Significant (LS) Byte. Active LOW input.
25	$\overline{WR}$	Write input. Active LOW.

$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{LDAC}$	$\overline{WR}$	Operation
0	1	1	0	Load MS Input Register
1	0	1	0	Load LS Input Register
0	0	1	0	Load MS and LS Input Registers
1	1	0	X	Load DAC Register from Input Registers
0	0	0	0	All Registers are transparent
1	1	1	X	No operation
X	X	1	1	No operation

NOTE X = Don't Care

26	V_{DD}	+12V to +15V supply input
27	V_{SS}	Bias pin for High Temperature Low Leakage configuration. To implement low leakage system, the pin should be at a negative voltage. See Figure 4, 5, 6 or 7 for recommended circuitry.
28	N.C.	No connection



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$
3. IF $\overline{LDAC}$ IS ACTIVATED PRIOR TO THE RISING EDGE OF $\overline{WR}$, THEN IT MUST STAY LOW FOR t_3 OR LONGER AFTER $\overline{WR}$ GOES HIGH.

Figure 1. AD7535 Timing Diagram

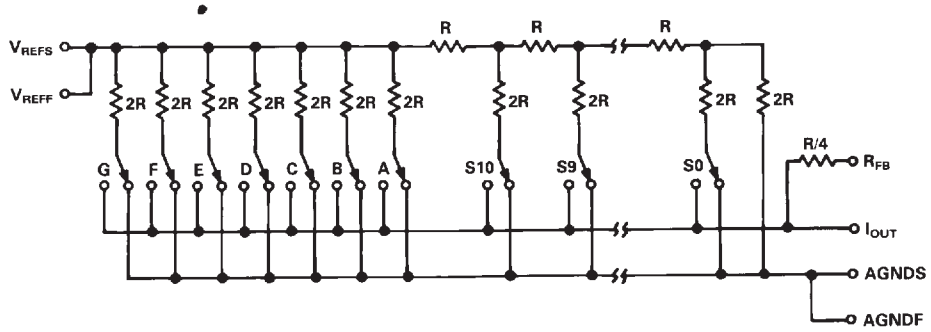


Figure 2. Simplified Circuit Diagram for the AD7535 D/A Section

CIRCUIT INFORMATION – D/A SECTION

Figure 2 shows a simplified circuit diagram for the AD7535 D/A section. The three MSB's of the 14-bit Data Word are decoded to drive the seven switches A-G. The 11 LSB's of the Data Word consist of an R-2R ladder operated in a current steering configuration.

The R-2R ladder current is 1/8 of the total reference input current. 7/8 I flows in the parallel ladder structure. Switches A-G steer equally weighted currents between I_{OUT} and A_{GNDF}.

Since the input resistance at V_{REF} is constant, it may be driven by a voltage source or a current source of positive or negative polarity.

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows an equivalent circuit for the analog section of the AD7535 D/A converter. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The resistor R_O denotes the equivalent output resistance of the DAC which varies with input code. C_{OUT} is the capacitance due to the current steering switches and varies from about 90pF to 180pF (typical values) depending upon the digital input. $g(V_{REF}, N)$ is the Thevenin equivalent voltage generator due to the reference

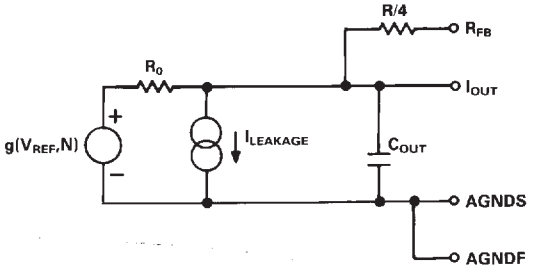


Figure 3. AD7535 Equivalent Analog Output Circuit

input voltage, V_{REF}, and the transfer function of the DAC ladder, N.

CIRCUIT INFORMATION – DIGITAL SECTION

The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode from DGND to each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close as possible to 0 and 5V logic levels.

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2 quadrant multiplication. The code table for Figure 4 is given in Table I.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when high speed op-amps are used.

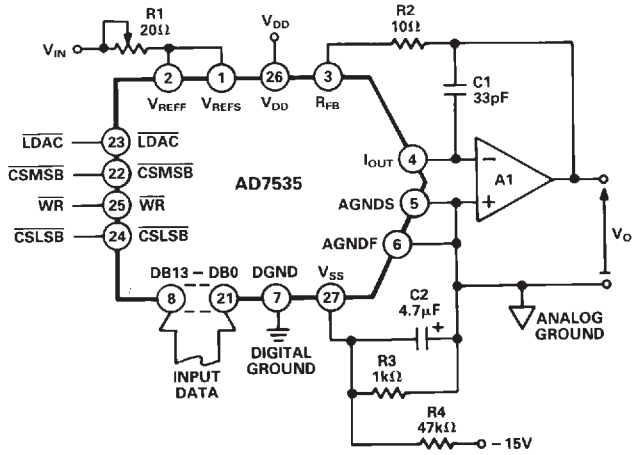


Figure 4. Unipolar Binary Operation

Binary Number In DAC Register	Analog Output, V_{OUT}
MSB LSB 11 1111 1111 1111	$-V_{IN}\left(\frac{16383}{16384}\right)$
10 0000 0000 0000	$-V_{IN}\left(\frac{8192}{16384}\right) = -1/2\,V_{IN}$
00 0000 0000 0001	$-V_{IN}\left(\frac{1}{16384}\right)$
00 0000 0000 0000	0V

Table I. Unipolar Binary Code Table for AD7535

ZERO OFFSET AND GAIN ADJUSTMENT FOR FIGURE 4.

Zero Offset Adjustment

1. Load DAC register with all 0's.
2. Adjust offset of amplifier A1 so that V_O is at a minimum (i.e. $\leq 30\mu V$).

Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R1 so that $V_O = -V_{IN}\frac{(16383)}{(16384)}$

In fixed reference applications, full scale can also be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

For high temperature applications resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7535, Gain Error trimming is not necessary.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 5. Offset binary coding is used.

With the DAC loaded to 10 0000 0000 0000, adjust R1 for $V_O = 0V$. Alternatively, one can omit R1 and R2 and adjust the ratio of R5 and R6 for $V_O = 0V$. Full scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R7.

Resistors R5, R6 and R7 should be ratio matched to 0.006%. Mismatch of R5 and R6 causes both offset and full scale error. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

A range of precision voltage dividers, manufactured by Vishay, offers a suitable solution to implementing the bipolar circuit described above. The resistor networks are TCR and Ratio Matched, giving excellent performance over temperature.

The code table for Figure 5 is given in Table II.

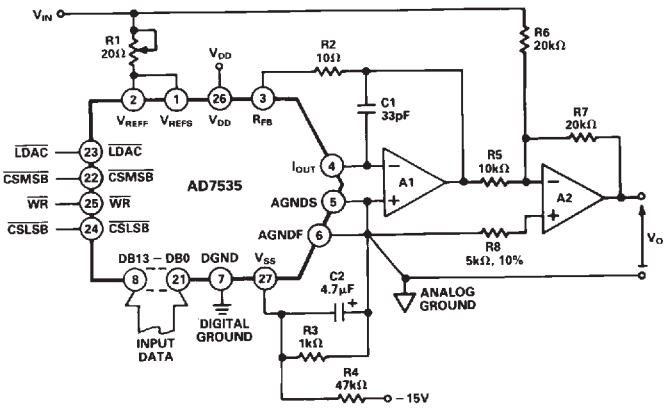


Figure 5. Bipolar Operation

Binary Number in DAC Register MSB LSB	Analog Output V_{OUT}
11 1111 1111 1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10 0000 0000 0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10 0000 0000 0000	0V
01 1111 1111 1111	$-V_{IN}\left(\frac{1}{8192}\right)$
00 0000 0000 0000	$-V_{IN}\left(\frac{8192}{8192}\right)$

Table II. Bipolar Code Table for Offset Binary Circuit of Figure 5.

GROUNDING TECHNIQUES

Since the AD7535 is specified for high accuracy it is important to use a proper grounding technique. The two AGND pins (AGNDF and AGNDS) provide flexibility in this respect. In Figure 4, the AD7535 is connected with the signal ground for the load located close to the DAC. There is no possibility of a voltage drop along the signal ground due to track resistance.

If the signal ground for the load is located at a distance from the DAC then the configuration of Figure 6 should be used. A_2 compensates for the error due to IR voltage drop between the DAC's internal Analog ground and the load signal ground.

Figure 7 shows a remote voltage reference driving the AD7535. Op-amps A2 and A3 compensate for voltage drops along the reference input line and the analog ground line.

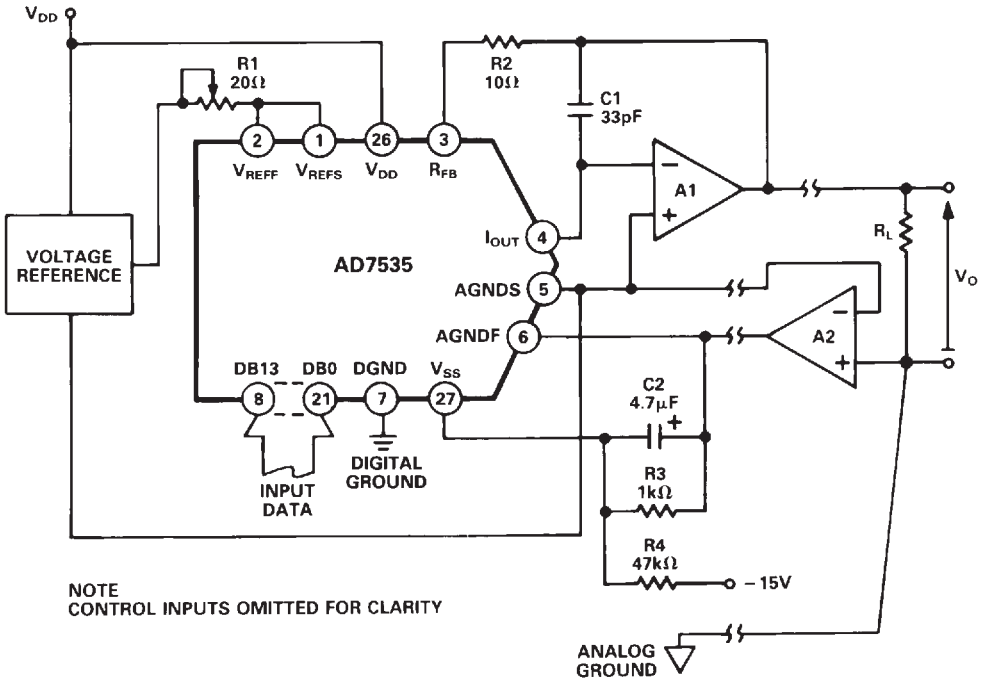


Figure 6. Unipolar Binary Operation with Forced Ground for Remote Load

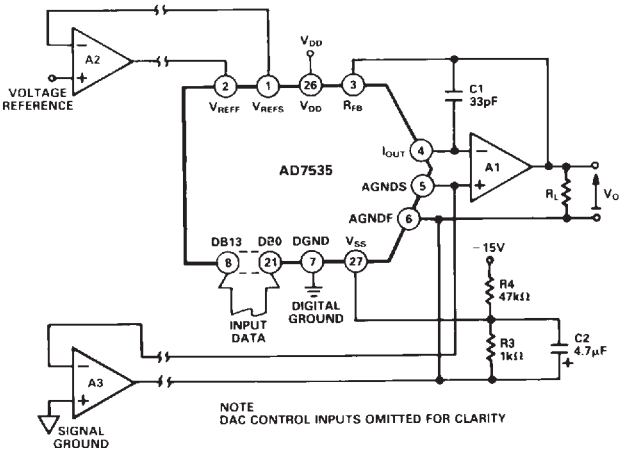


Figure 7. Driving the AD7535 with a Remote Voltage Reference

ZERO OFFSET AND GAIN ADJUSTMENT FOR FIGURE 6

Zero Offset Adjustment

1. Load DAC register with all 0's.
2. Adjust offset of amplifier A2 for a minimum potential at AGNDS. This potential should be ≤30μV with respect to Signal Ground. Adjust offset of amplifier A1 so that V_O is at a minimum (i.e. ≤30μV).

Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R1 so that $V_O = -V_{IN}\frac{(16383)}{(16384)}$

LOW LEAKAGE CONFIGURATION

For CMOS Multiplying D/A converters, as the device is operated at higher temperatures the output leakage current increases. For a 14-bit resolution system, this can be a significant source of error. The AD7535 features a leakage reduction configuration (patent pending) to keep the leakage current low over an extended temperature range. One may operate the device with or without this configuration. If V_{SS} (pin 27) is tied to A_{GND} then the DAC will exhibit normal output leakage current at high temperatures. To use the low leakage facility, V_{SS} should be tied to a voltage of approximately $-0.3V$ as in Figures 4, 5, 6 and 7. A simple resistor divider (R3, R4) produces approximately $-300mV$ from $-15V$. The capacitor C2 in parallel with R3 is an integral part of the low leakage configuration and must be $4.7\mu F$ or greater. Figure 8 is a plot of leakage current versus temperature for both conditions. It clearly shows the improvement gained by using the low leakage configuration.

OP-AMP SELECTION

In choosing an amplifier to be used with the AD7535, three parameters are of prime importance. These are (1) Input Offset Voltage (V_{OS}), (2) Input Bias Current (I_B), (3) Offset Voltage Drift (TC V_{OS}). To maintain specified accuracy with V_{REF} at 10V, V_{OS} must be less than $30\mu V$ while I_B should be less than 2nA. It is important that the amplifier Open Loop Gain, A_{VOL}, be sufficiently large to keep $V_{OS} \leq 30\mu V$ for the full output voltage range. For a maximum output of 10V, A_{VOL} must be greater than 340,000.

The AD OP-07 series of op-amps have a very low V_{OS} ($25\mu V$) and can be used as the output amplifier for the AD7535 without any external adjustment of Offset Voltage. In the Forced Ground configuration of Figure 6, one can use an AD OP-07 for amplifier A2. Settling time to 0.003% for the AD OP-07 is typically greater than $50\mu s$.

For faster settling time, one can use the AD544 series of op amps. Typically this settles to 0.003% (14-bits) in $5\mu s$. Even faster settling time can be achieved using the HA-2620 series of op-amps.

For operation over a wide temperature range Offset Voltage Drift and Bias Current Drift are critical parameters. The OP-27 and OP-37 series of op-amps exhibit extremely low Offset Voltage Drift and the AD544 has very low Bias Current Drift.

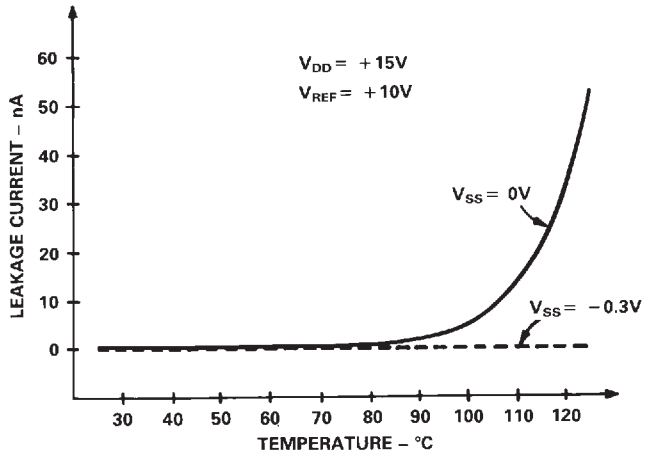


Figure 8. Graph of Typical Leakage Current vs Temperature for AD7535

MICROPROCESSOR INTERFACING

AD7535 – 8086A INTERFACE

The versatility of the AD7535 loading structure allows interfacing to both 8- and 16-bit microprocessor systems. Figure 9 shows the 8086 16-bit processor interfacing to a single device. In this setup the double buffering feature of the DAC is not used. AD0–AD13 of the 16-bit data bus are connected to the DAC data bus (DB0–DB13). The 14-bit word is written to the DAC in one MOV instruction and the analog output responds immediately. In this example the DAC address is D000. A software routine for Figure 9 is given in Table III.

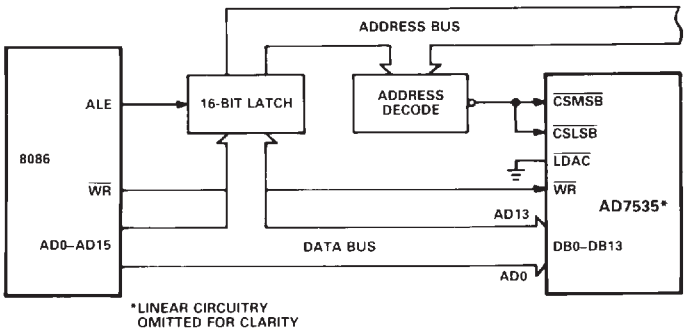


Figure 9. AD7535 – 8086 Interface Circuit

In a multiple DAC system the double buffering of the AD7535 allows the user to simultaneously update all DAC's. In Figure 10, a 14-bit word is loaded to the Input Registers of each of the DACs in sequence. Then, with one instruction to the appropriate address, CS4 (i.e. $\overline{\text{LDAC}}$) is brought low, updating all the DACs simultaneously.

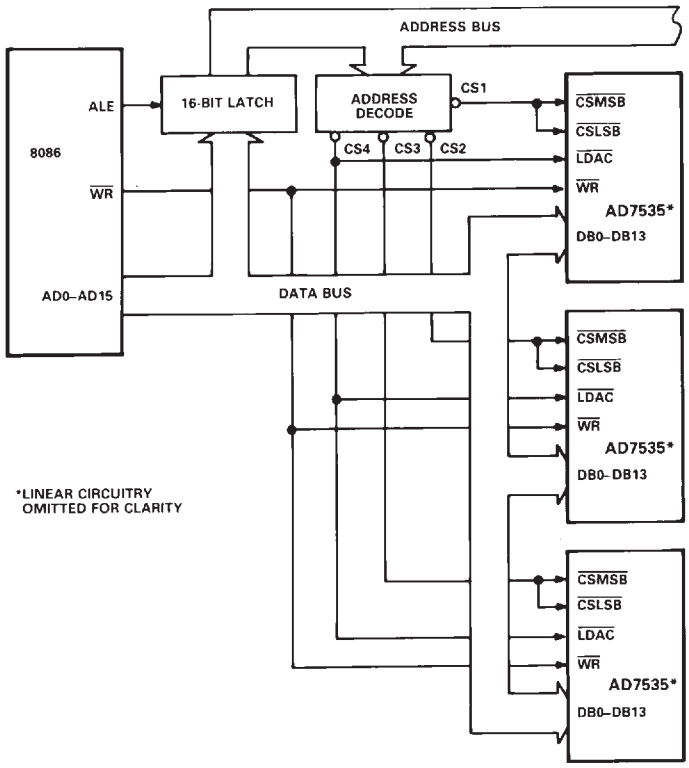


Figure 10. AD7535 – 8086 Interface: Multiple DAC System

```
ASSUME DS: DACLOAD, CS : DACLOAD
DACLOAD SEGMENT AT 000

00   8CC9          MOV CX, CS          :  DEFINE DATA SEGMENT REGISTER EQUAL
02   8ED9          MOV DS, CX          :  TO CODE SEGMENT REGISTER
04   BF00D0        MOV DI, # D000      :  LOAD DI WITH D000
07   C705"YZWX"    MOV MEM,# YZWX"     :  DAC LOADED WITH WXYZ
0B   EA0000                            :  CONTROL IS RETURNED TO THE
0E   00FF                                 MONITOR PROGRAM
```

Table III. Sample Program for Loading AD7535 from 8086

AD7535 – MC68000 INTERFACE

Interfacing between the MC68000 and the AD7535 is accomplished using the circuit of Figure 11. The following routine writes data to the DAC input registers and then outputs the data via the DAC register.

01000	MOVE.W	# W, D0	The desired DAC data, W, is loaded into Data Register 0. W may be any value between 0 and 16383 (decimal) or 0 and 3FFF (hexademical).
	MOVE.W	D0,$E000	The data W is transferred between D0 and the DAC Register.
	MOVE.B	# 228,D7	Control is returned to the System Monitor Program using these two instructions.
	TRAP	# 14	

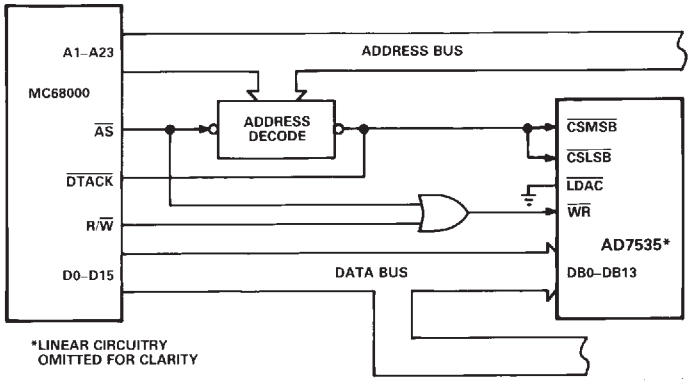


Figure 11. AD7535 – MC68000 Interface

AD7535 – Z80 INTERFACE

Though the AD7535 is primarily intended for use either with 16-bit microprocessors or in stand alone applications, it can also be interfaced to 8-bit processor systems. Figure 12 is an interface circuit for the Z80 microprocessor.

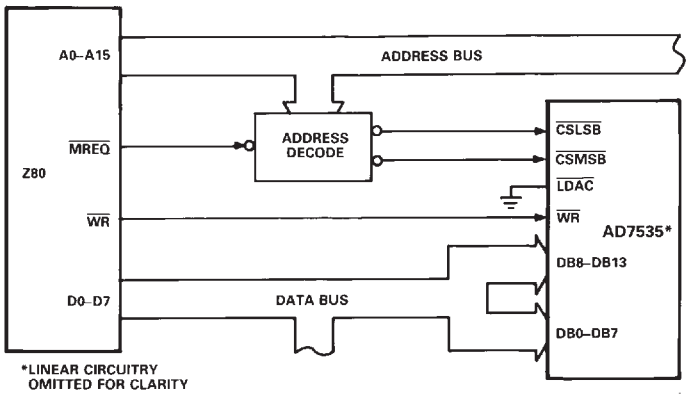


Figure 12. AD7535 – Z80 Interface

DIGITAL FEEDTHROUGH

In the preceding interface configurations, most digital inputs to the AD7535 are directly connected to the microprocessor bus. Even when the device is not selected, these inputs will be constantly changing. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this Digital Feedthrough isolate the DAC from the noise source. Figure 13 shows an interface circuit which physically isolates the DAC from the bus. One may also use other means, such as peripheral interface devices, to reduce the Digital Feedthrough.

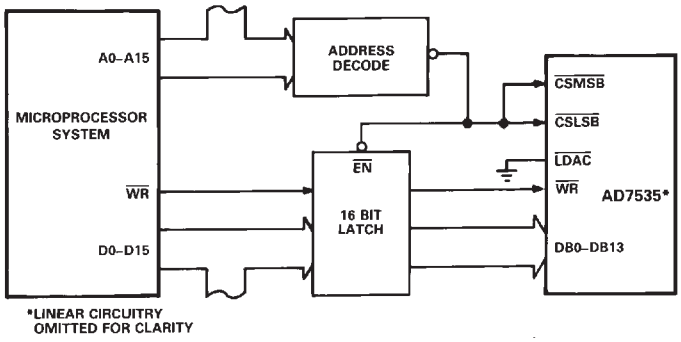
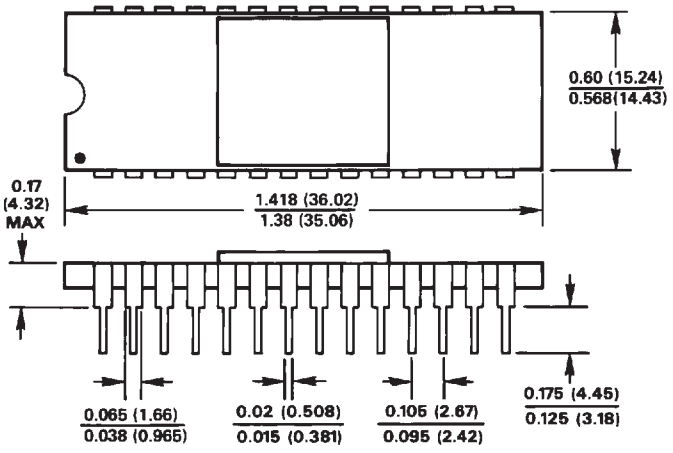


Figure 13. AD7535 Interface Circuit Using Latches to Minimize Digital Feedthrough

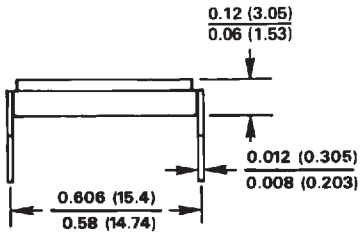
MECHANICAL INFORMATION
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

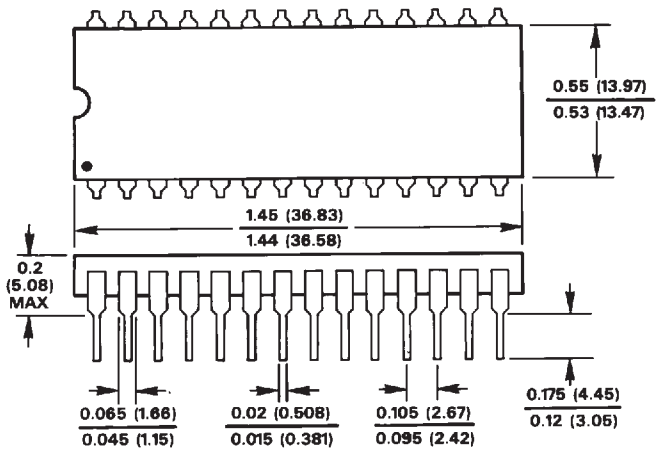
28-Pin Ceramic DIP Package (D-28A)



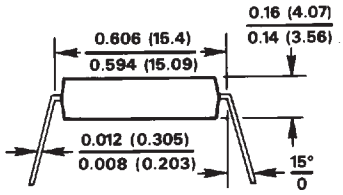
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42



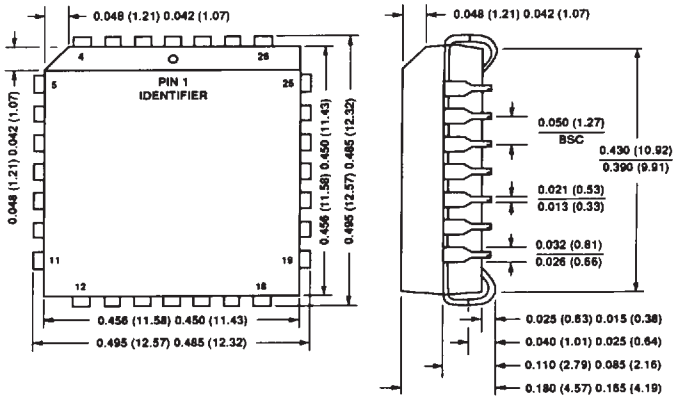
28-Pin Plastic DIP (N-28)



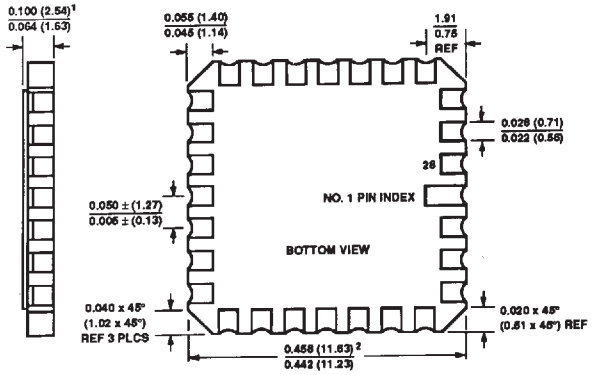
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42



P-28A PLCC



E-28A)
LCCC E Package



NOTES
1. THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
2. APPLIES TO ALL FOUR SIDES.
3. ALL TERMINALS ARE GOLD PLATED.