



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



FEATURES

- 8 simultaneously sampled inputs
- True bipolar analog input ranges: $\pm 10\text{ V}$, $\pm 5\text{ V}$
- Single 5 V analog supply and 2.3 V to 5.25 V V_{DRIVE}
- Fully integrated data acquisition solution
 - Analog input clamp protection
 - Input buffer with 1 M Ω analog input impedance
 - Second-order antialiasing analog filter
 - On-chip accurate reference and reference buffer
 - 18-bit ADC with 200 kSPS on all channels
 - Oversampling capability with digital filter
- Flexible parallel/serial interface
- SPI/QSPI™/MICROWIRE™/DSP compatible
- Pin compatible solutions from 14-bits to 18-bits
- Performance
 - 7 kV ESD rating on analog input channels
 - 98 dB SNR, -107 dB THD
 - Low power: 100 mW
 - Standby mode: 25 mW
- 64-lead LQFP package

APPLICATIONS

- Power line monitoring and protection systems
- Multiphase motor controls
- Instrumentation and control systems
- Multiaxis positioning systems
- Data acquisition systems (DAS)

COMPANION PRODUCTS

- External References: [ADR421](#), [ADR431](#)
- Digital Isolators: [ADuM1402](#), [ADuM5002](#), [ADuM5402](#)
- Voltage Regulator Design Tool: [ADIsimPower](#), [Supervisor](#)
- [Parametric Search](#)
- [Complete list of complements on AD7608 product page](#)

Table 1. High Resolution, Bipolar Input, Simultaneous Sampling DAS Solutions

Resolution	Single-Ended Inputs	True Differential Inputs	Number of Simultaneous Sampling Channels
18 Bits	AD7608 ¹	AD7609	8
16 Bits	AD7606		8
	AD7606-6		6
	AD7606-4		4
14 Bits	AD7607		8

FUNCTIONAL BLOCK DIAGRAM

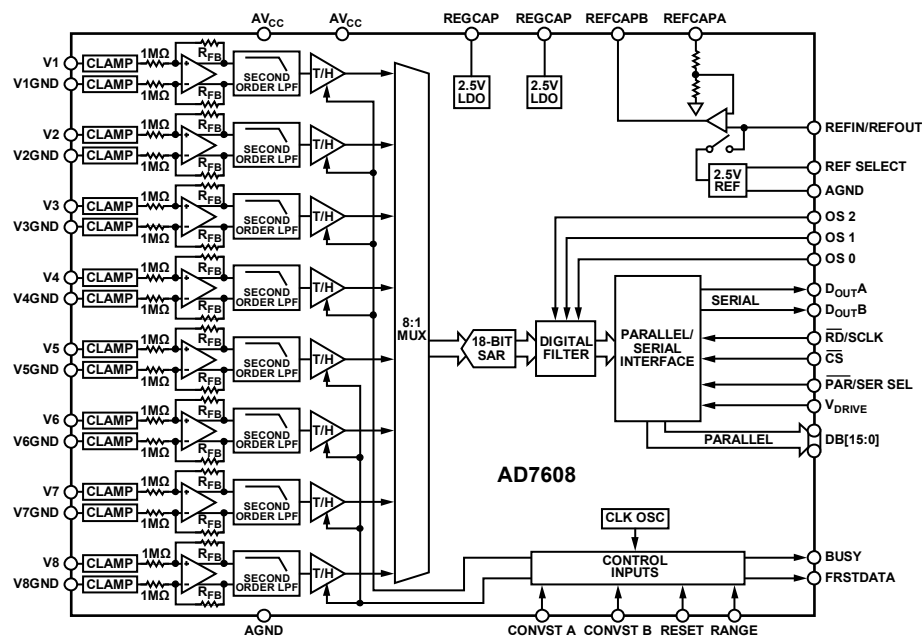


Figure 1.

¹ Patent pending.

Rev. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

AD7608* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7608 Evaluation Board

DOCUMENTATION

Data Sheet

- AD7608: 8-Channel DAS with 18-Bit, Bipolar, Simultaneous Sampling ADC Data Sheet

User Guides

- UG-851: Evaluating the AD7606/AD7606-6/AD7606-4/AD7607/AD7608 and AD7605-4 16-Bit Simultaneous Sampling, 8-/6-/4-Channel, SAR ADC

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD7608 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7608 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

Features	1	Converter Details	19
Applications.....	1	Analog Input	19
Companion Products.....	1	ADC Transfer Function.....	20
Functional Block Diagram	1	Internal/External Reference.....	21
Revision History	2	Typical Connection Diagram	22
General Description	3	Power-Down Modes	22
Specifications.....	4	Conversion Control	23
Timing Specifications	6	Digital Interface	24
Absolute Maximum Ratings.....	10	Parallel Interface ($\overline{\text{PAR}}/\text{SER SEL} = 0$).....	24
Thermal Resistance	10	Serial Interface ($\overline{\text{PAR}}/\text{SER SEL} = 1$).....	25
ESD Caution.....	10	Reading During Conversion.....	25
Pin Configuration and Function Descriptions.....	11	Digital Filter	26
Typical Performance Characteristics	14	Layout Guidelines.....	30
Terminology	18	Outline Dimensions	32
Theory of Operation	19	Ordering Guide	32

REVISION HISTORY

1/12—Rev. 0 to Rev. A

Changes to Analog Input Ranges Section19

4/11—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD7608 is an 18-bit, 8-channel simultaneous sampling, analog-to-digital data acquisition system (DAS). The part contains analog input clamp protection, a second-order antialiasing filter, a track-and-hold amplifier, an 18-bit charge redistribution successive approximation analog-to-digital converter (ADC), a flexible digital filter, a 2.5 V reference and reference buffer, and high speed serial and parallel interfaces.

The AD7608 operates from a single 5 V supply and can accommodate ± 10 V and ± 5 V true bipolar input signals while sampling at throughput rates up to 200 kSPS for all channels. The input clamp protection circuitry can tolerate voltages up to ± 16.5 V. The AD7608 has 1 M Ω analog input impedance regardless of sampling frequency. The single supply operation, on-chip filtering, and high input impedance eliminate the need for driver op amps and external bipolar supplies. The AD7608 antialiasing filter has a 3 dB cutoff frequency of 22 kHz and provides 40 dB antialias rejection when sampling at 200 kSPS. The flexible digital filter is pin driven, yields improvements in SNR, and reduces the 3 dB bandwidth.

SPECIFICATIONS

$V_{REF} = 2.5\text{ V}$ external/internal, $AV_{CC} = 4.75\text{ V}$ to 5.25 V , $V_{DRIVE} = 2.3\text{ V}$ to 5.25 V ; $f_{SAMPLE} = 200\text{ kSPS}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.¹

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit	
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio (SNR) ^{2, 3}	$f_{IN} = 1\text{ kHz}$ sine wave unless otherwise noted					
	Oversampling by 16; $\pm 10\text{ V}$ range; $f_{IN} = 130\text{ Hz}$	98	99.5		dB	
	Oversampling by 16; $\pm 5\text{ V}$ range; $f_{IN} = 130\text{ Hz}$	95.5	97.5		dB	
Signal-to-(Noise + Distortion) (SINAD) ²	No oversampling; $\pm 10\text{ V}$ range	89.5	90.9		dB	
	No oversampling; $\pm 5\text{ V}$ range	88.5	90		dB	
	No oversampling; $\pm 10\text{ V}$ range	88.5	90.5		dB	
Dynamic Range	No oversampling; $\pm 5\text{ V}$ range	88	89.5		dB	
	No oversampling; $\pm 10\text{ V}$ range		91.5		dB	
	No oversampling; $\pm 5\text{ V}$ range		90.5		dB	
Total Harmonic Distortion (THD) ²		-107	-95		dB	
Peak Harmonic or Spurious Noise (SFDR) ²			-108		dB	
Intermodulation Distortion (IMD) ²	$f_a = 1\text{ kHz}$, $f_b = 1.1\text{ kHz}$					
		Second-Order Terms		-110		dB
		Third-Order Terms		-106		dB
Channel-to-Channel Isolation ²	f_{IN} on unselected channels up to 160 kHz		-95		dB	
ANALOG INPUT FILTER						
Full Power Bandwidth	-3 dB, $\pm 10\text{ V}$ range		23		kHz	
	-3 dB, $\pm 5\text{ V}$ range		15		kHz	
	-0.1 dB, $\pm 10\text{ V}$ range		10		kHz	
	-0.1 dB, $\pm 5\text{ V}$ range		5		kHz	
$t_{GROUP\ DELAY}$	$\pm 10\text{ V}$ range		11		μs	
	$\pm 5\text{ V}$ range		15		μs	
DC ACCURACY						
Resolution	No missing codes	18			Bits	
Differential Nonlinearity ²			± 0.75	$-0.99/+2.6$	LSB ⁴	
Integral Nonlinearity ²			± 2.5	± 7.5	LSB	
Total Unadjusted Error (TUE)	$\pm 10\text{ V}$ range		± 15		LSB	
	$\pm 5\text{ V}$ range		± 40		LSB	
Positive Full-Scale Error ^{2, 5}	External reference		± 15	± 128	LSB	
	Internal reference		± 40		LSB	
Positive Full-Scale Error Drift	External reference		± 2		ppm/ $^{\circ}\text{C}$	
	Internal reference		± 7		ppm/ $^{\circ}\text{C}$	
Positive Full-Scale Error Matching ²	$\pm 10\text{ V}$ range		12	95	LSB	
	$\pm 5\text{ V}$ range		30	128	LSB	
Bipolar Zero Code Error ^{2, 6}	$\pm 10\text{ V}$ range		± 3.5	± 24	LSB	
	$\pm 5\text{ V}$ range		± 3.5	± 48	LSB	
Bipolar Zero Code Error Drift	$\pm 10\text{ V}$ range		10		$\mu\text{V}/^{\circ}\text{C}$	
	$\pm 5\text{ V}$ range		5		$\mu\text{V}/^{\circ}\text{C}$	
Bipolar Zero Code Error Matching ²	$\pm 10\text{ V}$ range		3	30	LSB	
	$\pm 5\text{ V}$ range		21	65	LSB	
Negative Full-Scale Error ^{2, 5}	External reference		± 15	± 128	LSB	
	Internal reference		± 40		LSB	
Negative Full-Scale Error Drift	External reference		± 4		ppm/ $^{\circ}\text{C}$	
	Internal reference		± 8		ppm/ $^{\circ}\text{C}$	
Negative Full-Scale Error Matching ²	$\pm 10\text{ V}$ range		12	95	LSB	
	$\pm 5\text{ V}$ range		30	128	LSB	

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT					
Input Voltage Ranges	RANGE = 1			±10	V
	RANGE = 0			±5	V
Analog Input Current	10 V; see Figure 28		5.4		μA
	5 V; see Figure 28		2.5		μA
Input Capacitance ⁷			5		pF
Input Impedance			1		MΩ
REFERENCE INPUT/OUTPUT					
Reference Input Voltage Range		2.475	2.5	2.525	V
DC Leakage Current				±1	μA
Input Capacitance ⁷	REF SELECT = 1		7.5		pF
Reference Output Voltage	REFIN/REFOUT		2.49/ 2.505		V
Reference Temperature Coefficient			±10		ppm/°C
LOGIC INPUTS					
Input High Voltage (V _{INH})		0.9 × V _{DRIVE}			V
Input Low Voltage (V _{INL})				0.1 × V _{DRIVE}	V
Input Current (I _{IN})				±2	μA
Input Capacitance (C _{IN}) ⁷			5		pF
LOGIC OUTPUTS					
Output High Voltage (V _{OH})	I _{SOURCE} = 100 μA	V _{DRIVE} – 0.2			V
Output Low Voltage (V _{OL})	I _{SINK} = 100 μA			0.2	V
Floating-State Leakage Current			±1	±20	μA
Floating-State Output Capacitance ⁷			5		pF
Output Coding	Twos complement				
CONVERSION RATE					
Conversion Time	All eight channels included; see Table 3		4		μs
Track-and-Hold Acquisition Time			1		μs
Throughput Rate	Per channel, all eight channels included			200	kSPS
POWER REQUIREMENTS					
A _{VCC}		4.75		5.25	V
V _{DRIVE}		2.3		5.25	V
I _{TOTAL}	Digital inputs = 0 V or V _{DRIVE}				
Normal Mode (Static)			16	22	mA
Normal Mode (Operational) ⁸	f _{SAMPLE} = 200 kSPS		20	27	mA
Standby Mode			5	8	mA
Shutdown Mode			2	11	μA
Power Dissipation					
Normal Mode (Static)			80	115.5	mW
Normal Mode (Operational) ⁸	f _{SAMPLE} = 200 kSPS		100	142	mW
Standby Mode			25	42	mW
Shutdown Mode			10	58	μW

¹ Temperature range for B version is –40°C to +85°C.

² See the Terminology section.

³ This specification applies when reading during a conversion or after a conversion. If reading during a conversion in parallel mode with V_{DRIVE} = 5 V, SNR typically reduces by 1.5 dB and THD by 3 dB.

⁴ LSB means least significant bit. With ±5 V input range, 1 LSB = 38.14 μV. With ±10 V input range, 1 LSB = 76.29 μV.

⁵ These specifications include the full temperature range variation and contribution from the internal reference buffer but do not include the error contribution from the external reference.

⁶ Bipolar zero code error is calculated with respect to the analog input voltage.

⁷ Sample tested during initial release to ensure compliance.

⁸ Operational power/current figure includes contribution when running in oversampling mode.

TIMING SPECIFICATIONS

$V_{CC} = 4.75\text{ V to }5.25\text{ V}$, $V_{DRIVE} = 2.3\text{ V to }5.25\text{ V}$, $V_{REF} = 2.5\text{ V}$ external reference/internal reference, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.¹

Table 3.

Parameter	Limit at T_{MIN} , T_{MAX}			Unit	Description
	Min	Typ	Max		
PARALLEL/SERIAL/BYTE MODE					
t_{CYCLE}			5	μs	1/throughput rate Parallel mode, reading during or after conversion; or serial mode: $V_{DRIVE} = 3.3\text{ V to }5.25\text{ V}$, reading during a conversion using D_{OUTA} and D_{OUTB} lines
		5		μs	Serial mode reading during conversion; $V_{DRIVE} = 2.7\text{ V}$
			10.5	μs	Serial mode reading after a conversion; $V_{DRIVE} = 2.3\text{ V}$, D_{OUTA} and D_{OUTB} lines
t_{CONV}					Conversion time
	3.45	4	4.15	μs	Oversampling off
	7.87		9.1	μs	Oversampling by 2
	16.05		18.8	μs	Oversampling by 4
	33		39	μs	Oversampling by 8
	66		78	μs	Oversampling by 16
	133		158	μs	Oversampling by 32
	257		315	μs	Oversampling by 64
$t_{WAKE-UP\ STANDBY}$			100	μs	\overline{STBY} rising edge to $CONVST$ x rising edge; power-up time from standby mode
$t_{WAKE-UP\ SHUTDOWN}$					
Internal Reference			30	ms	\overline{STBY} rising edge to $CONVST$ x rising edge; power-up time from shutdown mode
External Reference			13	ms	\overline{STBY} rising edge to $CONVST$ x rising edge; power-up time from shutdown mode
t_{RESET}	50			ns	RESET high pulse width
t_{OS_SETUP}	20			ns	BUSY to OS x pin setup time
t_{OS_HOLD}	20			ns	BUSY to OS x pin hold time
t_1			40	ns	$CONVST$ x high to BUSY high
t_2	25			ns	Minimum $CONVST$ x low pulse
t_3	25			ns	Minimum $CONVST$ x high pulse
t_4	0			ns	BUSY falling edge to \overline{CS} falling edge setup time
t_5^2			0.5	ms	Maximum delay allowed between $CONVST$ A, $CONVST$ B rising edges
t_6			25	ns	Maximum time between last \overline{CS} rising edge and BUSY falling edge
t_7	25			ns	Minimum delay between RESET low to $CONVST$ x high
PARALLEL/BYTE READ OPERATION					
t_8	0			ns	\overline{CS} to \overline{RD} setup time
t_9	0			ns	\overline{CS} to \overline{RD} hold time
t_{10}					\overline{RD} low pulse width
	16			ns	V_{DRIVE} above 4.75 V
	21			ns	V_{DRIVE} above 3.3 V
	25			ns	V_{DRIVE} above 2.7 V
	32			ns	V_{DRIVE} above 2.3 V
t_{11}	15			ns	\overline{RD} high pulse width
t_{12}	22			ns	\overline{CS} high pulse width (see Figure 5); \overline{CS} and \overline{RD} linked

Parameter	Limit at T _{MIN} , T _{MAX}			Unit	Description
	Min	Typ	Max		
t ₁₃			16 20 25 30	ns ns ns ns	Delay from \overline{CS} until DB[15:0] three-state disabled V _{DRIVE} above 4.75 V V _{DRIVE} above 3.3 V V _{DRIVE} above 2.7 V V _{DRIVE} above 2.3 V
t ₁₄ ³			16 21 25 32	ns ns ns ns	Data access time after \overline{RD} falling edge V _{DRIVE} above 4.75 V V _{DRIVE} above 3.3 V V _{DRIVE} above 2.7 V V _{DRIVE} above 2.3 V
t ₁₅	6			ns	Data hold time after \overline{RD} falling edge
t ₁₆	6			ns	\overline{CS} to DB[15:0] hold time
t ₁₇			22	ns	Delay from \overline{CS} rising edge to DB[15:0] three-state enabled
SERIAL READ OPERATION					
f _{SCLK}			23.5 17 14.5 11.5	MHz MHz MHz MHz	Frequency of serial read clock V _{DRIVE} above 4.75 V V _{DRIVE} above 3.3 V V _{DRIVE} above 2.7 V V _{DRIVE} above 2.3 V
t ₁₈			15 20 30	ns ns ns	Delay from \overline{CS} until D _{OUT} A/D _{OUT} B three-state disabled/delay from \overline{CS} until MSB valid V _{DRIVE} above 4.75 V V _{DRIVE} above 3.3 V V _{DRIVE} = 2.3 V to 2.7 V
t ₁₉ ³			17 23 27 34	ns ns ns ns	Data access time after SCLK rising edge V _{DRIVE} above 4.75 V V _{DRIVE} above 3.3 V V _{DRIVE} above 2.7 V V _{DRIVE} above 2.3 V
t ₂₀	0.4 t _{SCLK}			ns	SCLK low pulse width
t ₂₁	0.4 t _{SCLK}			ns	SCLK high pulse width
t ₂₂	7			ns	SCLK rising edge to D _{OUT} A/D _{OUT} B valid hold time
t ₂₃			22	ns	\overline{CS} rising edge to D _{OUT} A/D _{OUT} B three-state enabled
FRSTDATA OPERATION					
t ₂₄			15 20 25 30	ns ns ns ns	Delay from \overline{CS} falling edge until FRSTDATA three-state disabled V _{DRIVE} above 4.75 V V _{DRIVE} above 3.3 V V _{DRIVE} above 2.7 V V _{DRIVE} above 2.3 V
t ₂₅			15 20 25 30	ns ns ns ns	Delay from \overline{CS} falling edge until FRSTDATA high, serial mode V _{DRIVE} above 4.75 V V _{DRIVE} above 3.3 V V _{DRIVE} above 2.7 V V _{DRIVE} above 2.3 V
t ₂₆			16 20 25 30	ns ns ns ns	Delay from \overline{RD} falling edge to FRSTDATA high V _{DRIVE} above 4.75 V V _{DRIVE} above 3.3 V V _{DRIVE} above 2.7 V V _{DRIVE} above 2.3 V

Parameter	Limit at T _{MIN} , T _{MAX}			Unit	Description
	Min	Typ	Max		
t ₂₇			19	ns	Delay from RD falling edge to FRSTDATA low V _{DRIVE} = 3.3 V to 5.25 V
			24	ns	V _{DRIVE} = 2.3 V to 2.7 V
t ₂₈			17	ns	Delay from 16 th SCLK falling edge to FRSTDATA low V _{DRIVE} = 3.3 V to 5.25 V
			22	ns	V _{DRIVE} = 2.3 V to 2.7 V
t ₂₉			24	ns	Delay from CS rising edge until FRSTDATA three-state enabled

¹ Sample tested during initial release to ensure compliance. All input signals are specified with t_r = t_f = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
² The delay between the CONVST x signals was measured as the maximum time allowed while ensuring a <40 LSB performance matching between channel sets.
³ A buffer is used on the data output pins for these measurements, which is equivalent to a load of 20 pF on the output pins.

Timing Diagrams

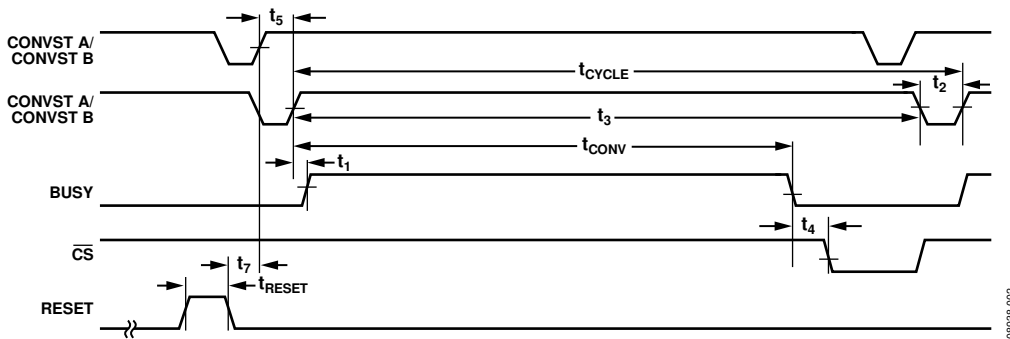


Figure 2. CONVST x Timing—Reading After a Conversion

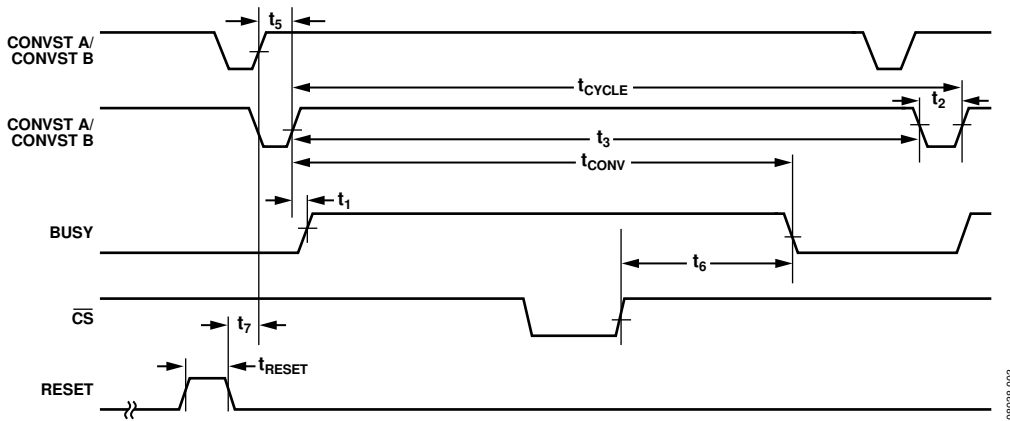


Figure 3. CONVST x Timing—Reading During a Conversion

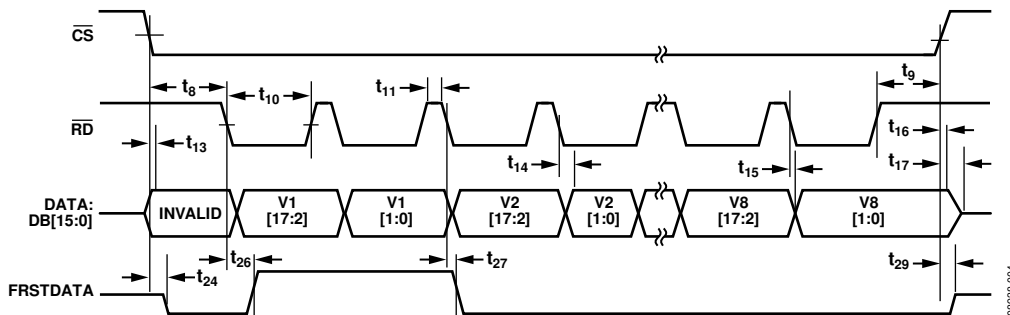


Figure 4. Parallel Mode Separate CS and RD Pulses

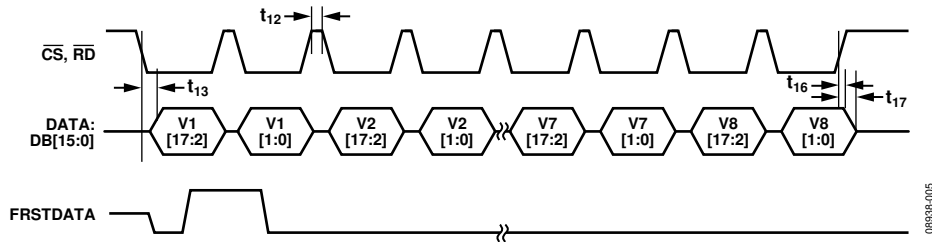


Figure 5. \overline{CS} and \overline{RD} Linked Parallel Mode

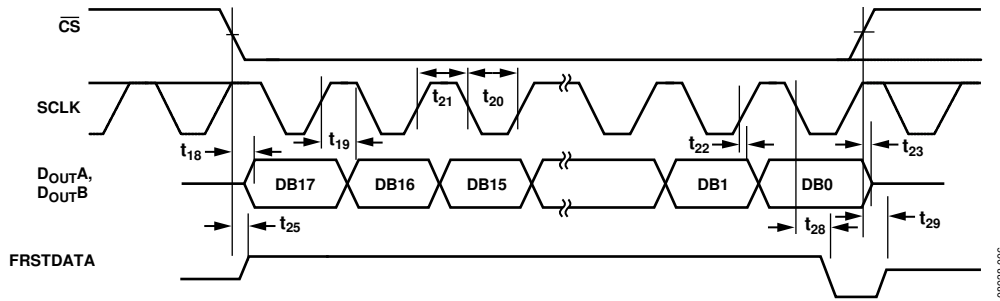


Figure 6. Serial Read Operation (Channel 1)

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Rating
AV_{CC} to AGND	−0.3 V to +7 V
V_{DRIVE} to AGND	−0.3 V to $AV_{CC} + 0.3$ V
Analog Input Voltage to AGND ¹	±16.5 V
Digital Input Voltage to AGND	−0.3 V to $V_{DRIVE} + 0.3$ V
Digital Output Voltage to AGND	−0.3 V to $V_{DRIVE} + 0.3$ V
REFIN to AGND	−0.3 V to $AV_{CC} + 0.3$ V
Input Current to Any Pin Except Supplies ¹	±10 mA
Operating Temperature Range	
B Version	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Pb/SN Temperature, Soldering	
Reflow (10 sec to 30 sec)	240 (+0)°C
Pb-Free Temperature, Soldering Reflow	260 (+0)°C
ESD (All Pins Except Analog Inputs)	2 kV
ESD (Analog Input Pins Only)	7 kV

¹ Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. These specifications apply to a 4-layer board.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
64-Lead LQFP	45	11	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

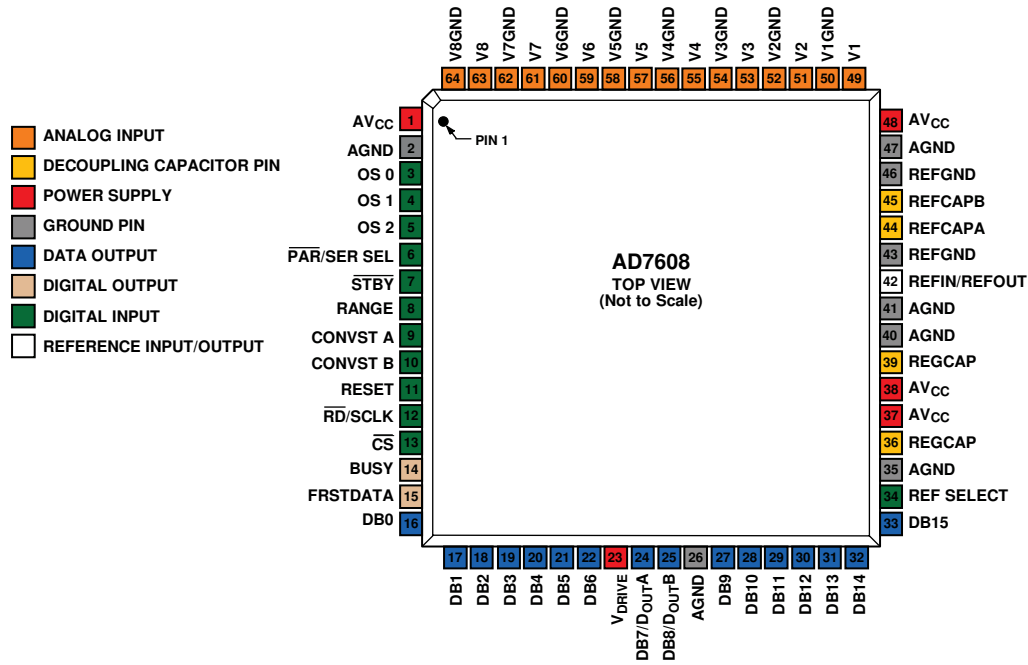


Figure 7. Pin Configuration

08938-007

Table 6. Pin Function Descriptions

Pin No.	Type ¹	Mnemonic	Description
1, 37, 38, 48	P	AV _{CC}	Analog Supply Voltage 4.75 V to 5.25 V. This supply voltage is applied to the internal front-end amplifiers and to the ADC core. These supply pins should be decoupled to AGND.
2, 26, 35, 40, 41, 47	P	AGND	Analog Ground. This pin is the ground reference point for all analog circuitry on the AD7608. All analog input signals and external reference signals should be referred to these pins. All six of these AGND pins should connect to the AGND plane of a system.
5, 4, 3	DI	OS [2:0]	Oversampling Mode Pins. Logic inputs. These inputs are used to select the oversampling ratio. OS 2 is the MSB control bit, while OS 0 is the LSB control bit. See the Digital Filter section for further details on the oversampling mode of operation and Table 8 for oversampling bit decoding.
6	DI	$\overline{\text{PAR/SER SEL}}$	Parallel/Serial Interface Selection Input. Logic input. If this pin is tied to a logic low, the parallel interface is selected. If this pin is tied to a logic high, the serial interface is selected. In serial mode, the $\overline{\text{RD/SCLK}}$ pin functions as the serial clock input. The DB7/D _{OUT} A and DB8/D _{OUT} B pins function as serial data outputs. When the serial interface is selected, DB[15:9] and DB[6:0] pins should be tied to GND.
7	DI	$\overline{\text{STBY}}$	Standby Mode Input. This pin is used to place the AD7608 into one of two power-down modes: standby mode or shutdown mode. The power-down mode entered depends on the state of the RANGE pin as shown in Table 7. When in standby mode, all circuitry, except the on-chip reference regulators, and regulator buffers, is powered down. When in shutdown mode, all circuitry is powered down.
8	DI	RANGE	Analog Input Range Selection. Logic input. The polarity on this pin determines the input range of the analog input channels. If this pin is tied to a logic high, the analog input range is ± 10 V for all channels. If this pin is tied to a logic low, the analog input range is ± 5 V for all channels. A logic change on this pin has an immediate effect on the analog input range. Changing this pin during a conversion is not recommended. See the Analog Input section for more details.
9, 10	DI	CONVST A, CONVST B	Conversion Start Input A, Conversion Start Input B. Logic inputs. These logic inputs are used to initiate conversions on the analog input channels. For simultaneous sampling of all input channels, CONVST A and CONVST B can be shorted together and a single convert start signal applied. Alternatively, CONVST A can be used to initiate simultaneous sampling for V1, V2, V3, and V4, and CONVST B can be used to initiate simultaneous sampling on the other analog inputs (V5, V6, V7, and V8). This is only possible when oversampling is not switched on. When the CONVST A or CONVST B pin transitions from low to high, the front-end track-and-hold circuitry for their respective analog inputs is set to hold. This function allows a phase delay to be created inherently between the sets of analog inputs.

Pin No.	Type ¹	Mnemonic	Description
11	DI	RESET	Reset Input. When set to logic high, the rising edge of RESET resets the AD7608. Once $t_{\text{WAKE-UP}}$ has elapsed, the part should receive a RESET pulse after power up. The RESET high pulse should be typically 100 ns wide. If a RESET pulse is applied during a conversion, the conversion is aborted. If a RESET pulse is applied during a read, the contents of the output registers resets to all zeros.
12	DI	$\overline{\text{RD}}/\text{SCLK}$	Parallel Data Read Control Input when Parallel Interface is Selected ($\overline{\text{RD}}$)/Serial Clock Input when the Serial Interface is Selected (SCLK). When both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic low in parallel mode, the output bus is enabled. In parallel mode, two $\overline{\text{RD}}$ pulses are required to read the full 18 bits of conversion results from each channel. The first $\overline{\text{RD}}$ pulse outputs DB[17:2], the second $\overline{\text{RD}}$ pulse outputs DB[1:0]. In serial mode, this pin acts as the serial clock input for data transfers. The $\overline{\text{CS}}$ falling edge takes the data output lines, D_{OUTA} and D_{OUTB} , out of three-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the D_{OUTA} and D_{OUTB} serial data outputs. For further information, see the Conversion Control section.
13	DI	$\overline{\text{CS}}$	Chip Select. This active low logic input frames the data transfer. When both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic low in parallel mode, the output bus, DB[15:0], is enabled and the conversion result is output on the parallel data bus lines. In serial mode, the $\overline{\text{CS}}$ is used to frame the serial read transfer and clock out the MSB of the serial output data.
14	DO	BUSY	Busy Output. This pin transitions to a logic high after both CONVST A and CONVST B rising edges and indicates that the conversion process has started. The BUSY output remains high until the conversion process for all channels is complete. The falling edge of BUSY signals that the conversion data is being latched into the output data registers and is available to be read after a Time t_4 . Any data read while BUSY is high must be complete before the falling edge of BUSY occurs. Rising edges on CONVST A or CONVST B have no effect while the BUSY signal is high.
15	DO	FRSTDATA	Digital Output. The FRSTDATA output signal indicates when the first channel, V1, is being read back on either the parallel or serial interface. When the $\overline{\text{CS}}$ input is high, the FRSTDATA output pin is in three-state. The falling edge of $\overline{\text{CS}}$ takes FRSTDATA out of three-state. In parallel mode, the falling edge of $\overline{\text{RD}}$ corresponding to the result of V1 then sets the FRSTDATA pin high indicating that the result from V1 is available on the output data bus. The FRSTDATA output returns to a logic low following the third falling edge of $\overline{\text{RD}}$. In serial mode, FRSTDATA goes high on the falling edge of $\overline{\text{CS}}$ as this clocks out the MSB of V1 on D_{OUTA} . It returns low on the 18 th SCLK falling edge after the $\overline{\text{CS}}$ falling edge. See the Conversion Control section for more details.
22 to 16	DO	DB[6:0]	Parallel Output Data Bits, DB6 to DB0. When $\overline{\text{PAR}}/\text{SER SEL} = 0$, these pins act as three-state parallel digital output pins. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, these pins are used to output DB8 to DB2 of the conversion result during the first $\overline{\text{RD}}$ pulse and output 0 during the second $\overline{\text{RD}}$ pulse. When $\overline{\text{PAR}}/\text{SER SEL} = 1$, these pins should be tied to GND.
23	P	V_{DRIVE}	Logic Power Supply Input. The voltage (2.3 V to 5.25 V) supplied at this pin determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface (that is, DSP and FPGA).
24	DO	DB7/ D_{OUTA}	Parallel Output Data Bit 7 (DB7)/Serial Interface Data Output Pin (D_{OUTA}). When $\overline{\text{PAR}}/\text{SER SEL} = 0$, this pin acts as a three-state parallel digital output pin. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, this pin is used to output DB9 of the conversion result. When $\overline{\text{PAR}}/\text{SER SEL} = 1$, this pin functions as D_{OUTA} and outputs serial conversion data. See the Conversion Control section for further details.
25	DO	DB8/ D_{OUTB}	Parallel Output Data Bit 8 (DB8)/Serial Interface Data Output Pin (D_{OUTB}). When $\overline{\text{PAR}}/\text{SER SEL} = 0$, this pin acts as a three-state parallel digital output pin. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, this pin is used to output DB10 of the conversion result. When $\overline{\text{PAR}}/\text{SER SEL} = 1$, this pin functions as D_{OUTB} and outputs serial conversion data. See the Conversion Control section for further details.
31 to 27	DO	DB[13:9]	Parallel Output Data Bits, DB13 to DB9. When $\overline{\text{PAR}}/\text{SER SEL} = 0$, these pins act as three-state parallel digital output pins. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, these pins are used to output DB15 to DB11 of the conversion result during the first $\overline{\text{RD}}$ pulse and output zero during the second $\overline{\text{RD}}$ pulse. When $\overline{\text{PAR}}/\text{SER SEL} = 1$, these pins should be tied to GND.
32	DO/DI	DB14	Parallel Output Data Bit 14 (DB14). When $\overline{\text{PAR}}/\text{SER SEL} = 0$, this pin act as three-state parallel digital output pin. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, this pin is used to output DB16 of the conversion result during the first $\overline{\text{RD}}$ pulse and DB0 of the same conversion result during the second $\overline{\text{RD}}$ pulse. When $\overline{\text{PAR}}/\text{SER SEL} = 1$, this pins should be tied to GND.
33	DO/DI	DB15	Parallel Output Data Bit 15 (DB15). When $\overline{\text{PAR}}/\text{SER SEL} = 0$, this pin acts as three-state parallel digital output pin. This pin is used to output DB17 of the conversion result during the first $\overline{\text{RD}}$ pulse and DB1 of the same conversion result during the second $\overline{\text{RD}}$ pulse. When $\overline{\text{PAR}}/\text{SER SEL} = 1$, this pins should be tied to GND.

Pin No.	Type ¹	Mnemonic	Description
34	DI	REF SELECT	Internal/External Reference Selection Input. Logic input. If this pin is set to logic high then the internal reference is selected and is enabled, if this pin is set to logic low then the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin.
36, 39	P	REGCAP	Decoupling Capacitor Pins for Voltage Output from Internal Regulator. These output pins should be decoupled separately to AGND using a 1 μ F capacitor. The voltage on these output pins is in the range of 2.5 V to 2.7 V.
42	REF	REFIN/ REFOUT	Reference Input/Reference Output. The on-chip reference of 2.5 V is available on this pin for external use if the REF SELECT pin is set to a logic high. Alternatively, the internal reference can be disabled by setting the REF SELECT pin to a logic low and an external reference of 2.5 V can be applied to this input. See the Internal/External Reference section. Decoupling is required on this pin for both the internal or external reference options. A 10 μ F capacitor should be applied from this pin to ground close to the REFGND pins.
43, 46	REF	REFGND	Reference Ground Pins. These pins should be connected to AGND.
44, 45	REF	REFCAPA, REFCAPB	Reference Buffer Output Force/Sense Pins. These pins must be connected together and decoupled to AGND using a low ESR 10 μ F ceramic capacitor.
49, 51, 53, 55, 57, 59, 61, 63	AI	V1 to V8	Analog Inputs. These pins are single-ended analog inputs. The analog input range of these channels is determined by the RANGE pin.
50, 52, 54, 56, 58, 60, 62, 64	AI/ GND	V1GND to V8GND	Analog Input Ground Pins. These pins correspond to the V1 to V8 analog input pins. Connect all analog input AGND pins to the AGND plane of a system.

¹ Refers to classification of pin type; P denotes power, AI denotes analog input, REF denotes reference, DI denotes digital input, DO denotes digital output.

TYPICAL PERFORMANCE CHARACTERISTICS

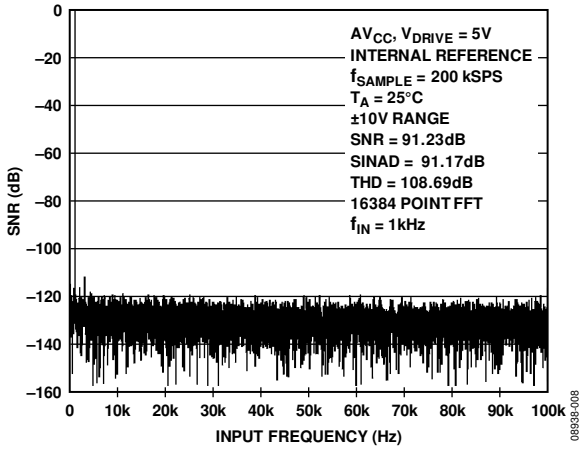


Figure 8. FFT Plot, ±10V Range

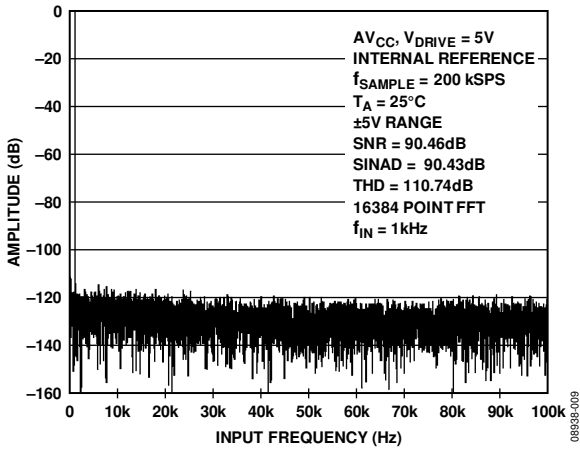


Figure 9. FFT Plot, ±5V Range

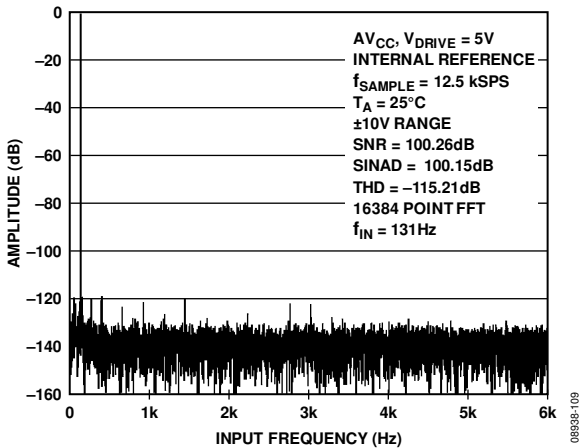


Figure 10. FFT Over Sampling by 16, ±10V Range

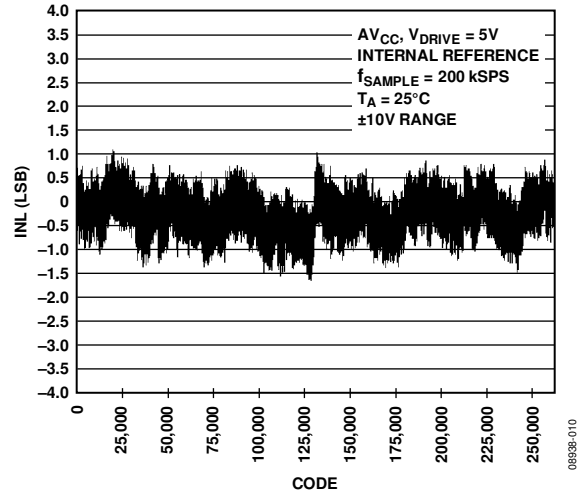


Figure 11. Typical INL, ±10V Range

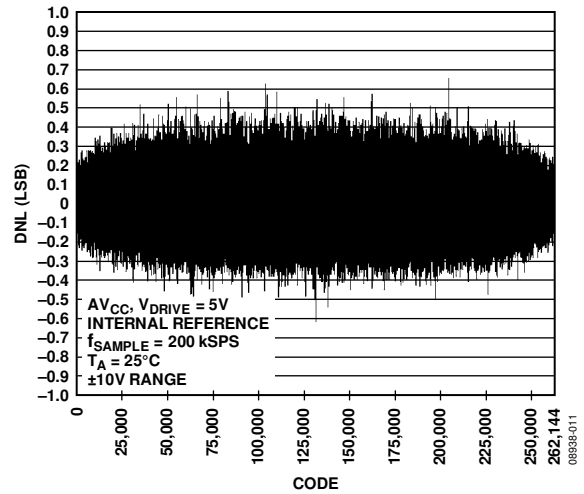


Figure 12. Typical DNL, ±10V Range

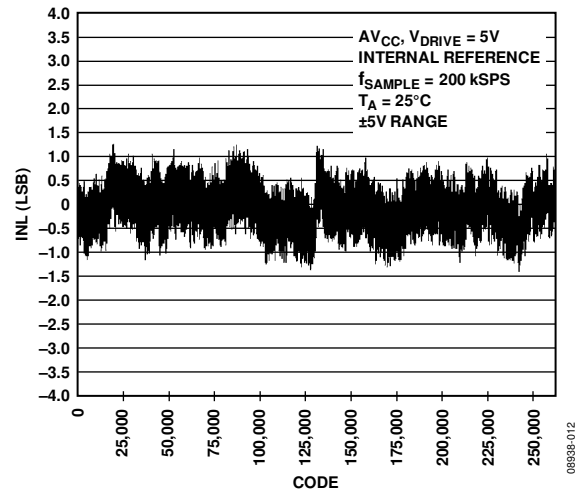


Figure 13. Typical INL, ±5V Range

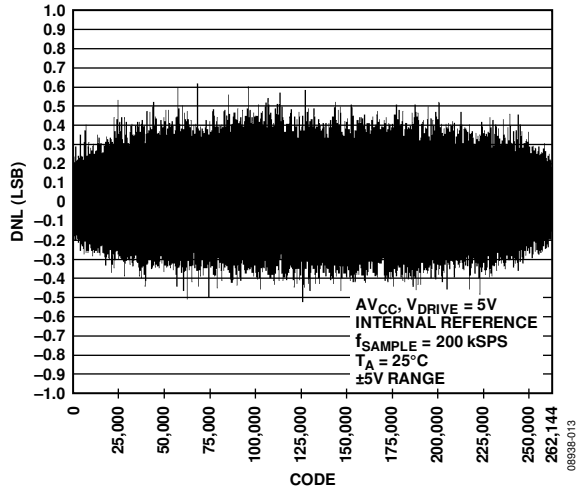


Figure 14. Typical DNL, $\pm 5V$ Range

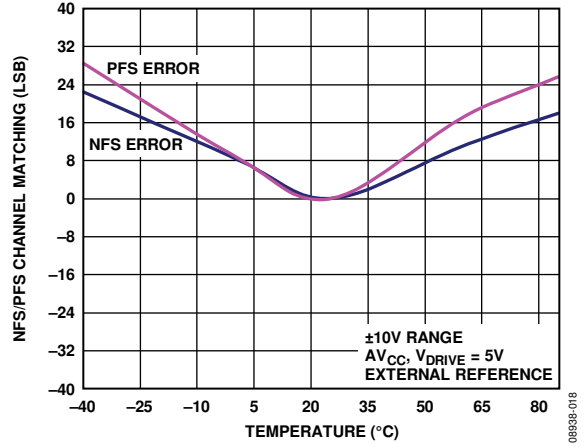


Figure 17. NFS/PFS Error Matching

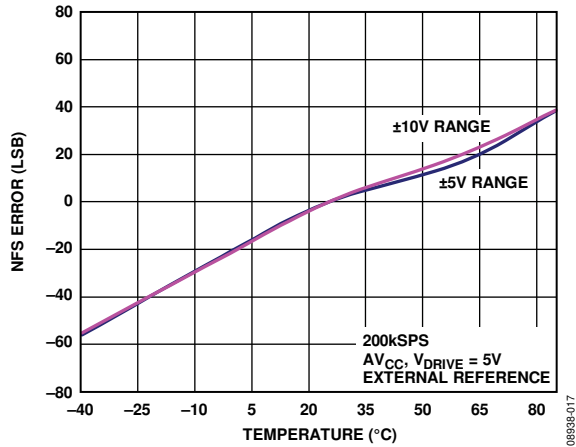


Figure 15. NFS Error vs. Temperature

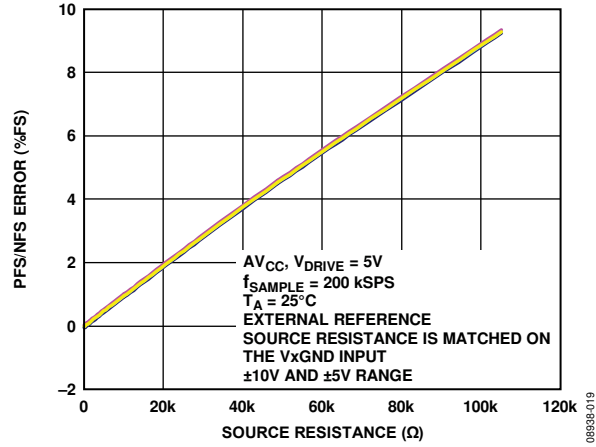


Figure 18. PFS/NFS Error vs. Source Resistance

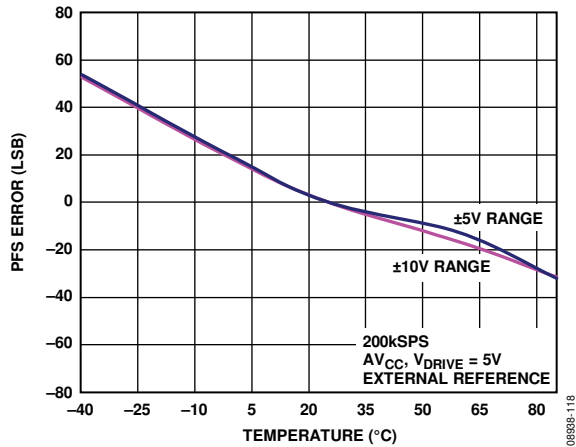


Figure 16. PFS Error vs. Temperature

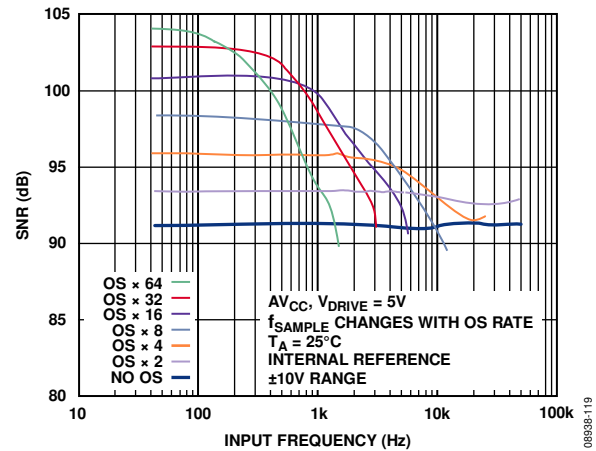


Figure 19. SNR vs. Input Frequency for Different Oversampling Rates, $\pm 10V$ Range

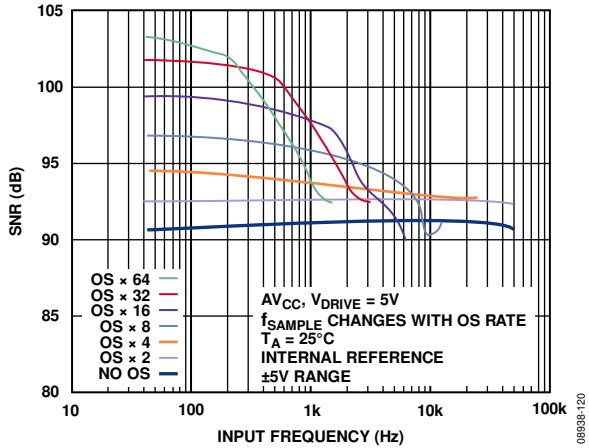


Figure 20. SNR vs. Input Frequency for Different Oversampling Rates, ±5 V Range

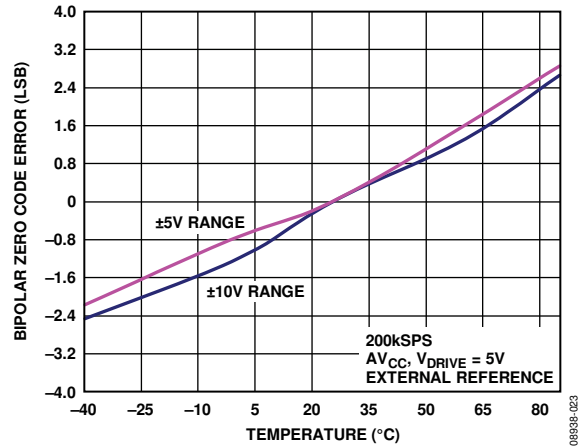


Figure 23. Bipolar Zero Code Error vs. Temperature

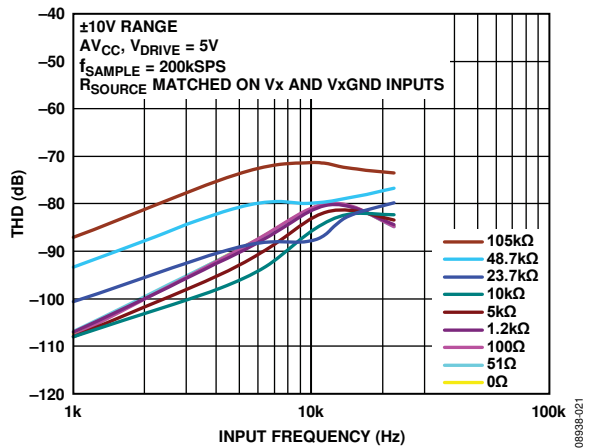


Figure 21. THD vs. Input Frequency for Various Source Impedances, ±10 V Range

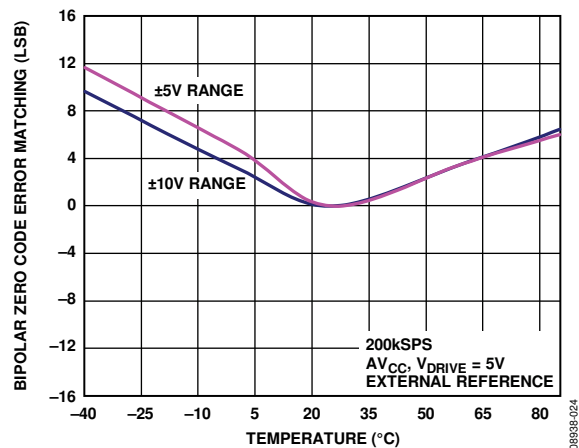


Figure 24. Bipolar Zero Code Error Matching Between Channels

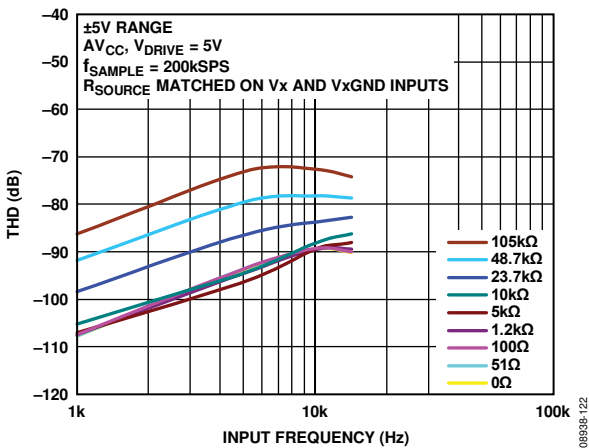


Figure 22. THD vs. Input Frequency for Various Source Impedances, ±5 V Range

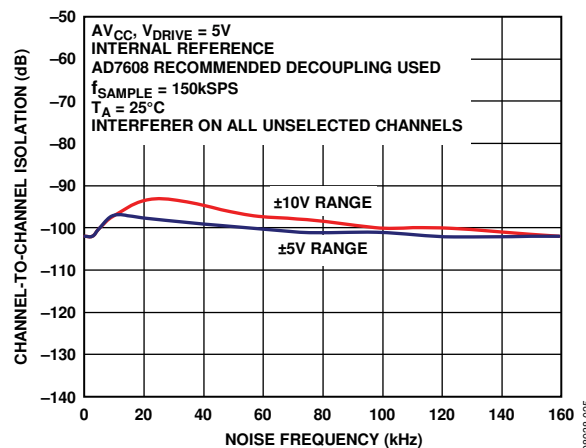


Figure 25. Channel-to-Channel Isolation

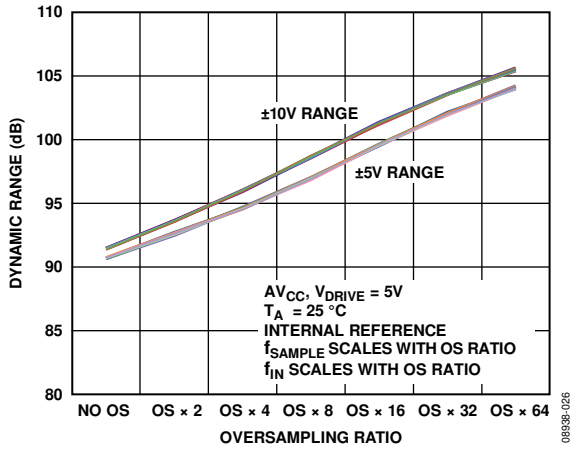


Figure 26. Dynamic Range vs. Oversampling Ratio

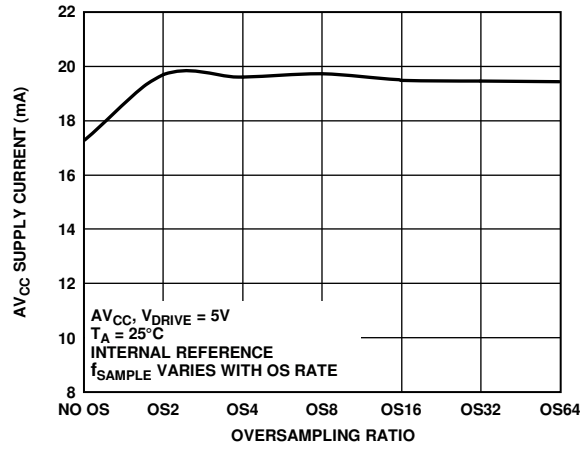


Figure 29. Supply Current vs. Oversampling Rate

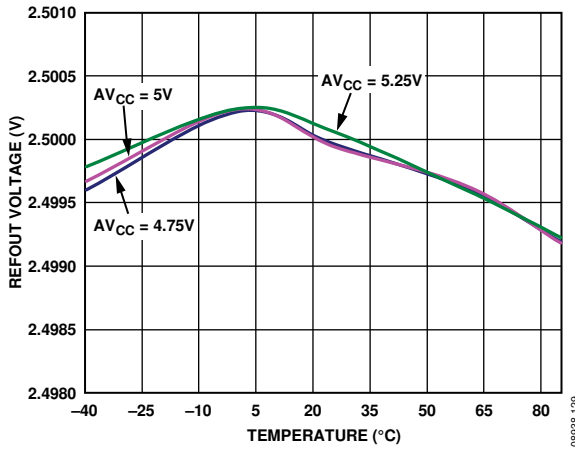


Figure 27. Reference Output Voltage vs. Temperature for Different Supply Voltages

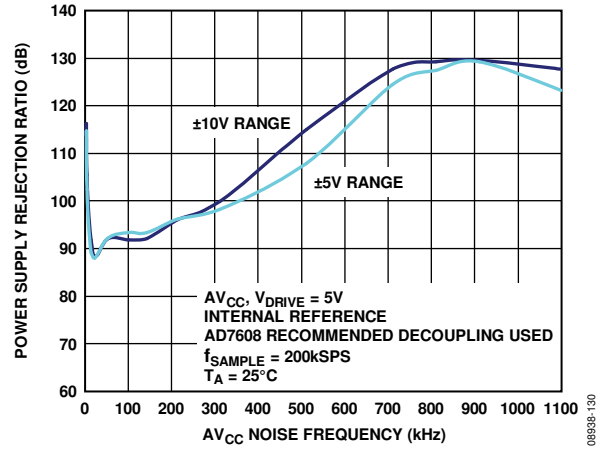


Figure 30. PSRR

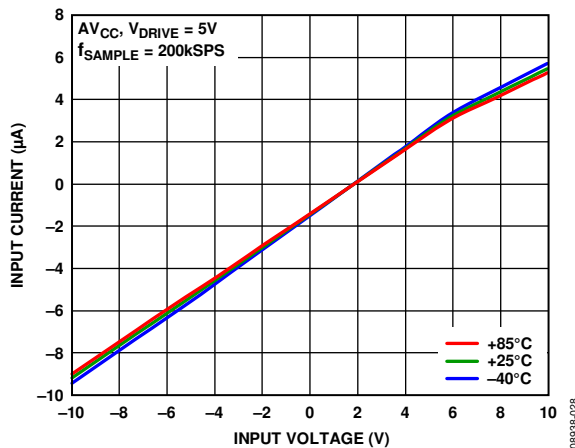


Figure 28. Analog Input Current vs. Input Voltage Across Temperature

TERMINOLOGY

Integral Nonlinearity

The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, at ½ LSB below the first code transition; and full scale, at ½ LSB above the last code transition.

Differential Nonlinearity

The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Code Error

The deviation of the midscale transition (all 1s to all 0s) from the ideal, which is $0\text{ V} - \frac{1}{2}\text{ LSB}$.

Bipolar Zero Code Error Match

The absolute difference in bipolar zero code error between any two input channels.

Positive Full-Scale Error

The deviation of the actual last code transition from the ideal last code transition ($10\text{ V} - \frac{1}{2}\text{ LSB}$ (9.99988) and $5\text{ V} - \frac{1}{2}\text{ LSB}$ (4.99994)) after bipolar zero code error is adjusted out. The positive full-scale error includes the contribution from the internal reference buffer.

Positive Full-Scale Error Match

The absolute difference in positive full-scale error between any two input channels.

Negative Full-Scale Error

The deviation of the first code transition from the ideal first code transition ($-10\text{ V} + \frac{1}{2}\text{ LSB}$ (-9.99996) and $-5\text{ V} + \frac{1}{2}\text{ LSB}$ (-4.99998)) after the bipolar zero code error is adjusted out. The negative full-scale error includes the contribution from the internal reference buffer.

Negative Full-Scale Error Match

The absolute difference in negative full-scale error between any two input channels.

Signal-to-(Noise + Distortion) Ratio

The measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_s/2$, excluding dc).

The ratio depends on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise.

The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$\text{Signal-to-(Noise + Distortion)} = (6.02N + 1.76)\text{ dB}$$

Thus, for an 18-bit converter, the signal-to-(noise + distortion) is 110.12 dB.

Total Harmonic Distortion (THD)

The ratio of the rms sum of the harmonics to the fundamental.

For the AD7608, it is defined as

$$\text{THD (dB)} = 20\log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2 + V_8^2 + V_9^2}}{V_1}$$

where:

V_1 is the rms amplitude of the fundamental.

V_2 to V_9 are the rms amplitudes of the second through ninth harmonics.

Peak Harmonic or Spurious Noise

The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_s/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is determined by a noise peak.

Intermodulation Distortion (IMD)

With inputs consisting of sine waves at two frequencies, f_a and f_b , any active device with nonlinearities creates distortion products at sum and difference frequencies of $m f_a \pm n f_b$, where $m, n = 0, 1, 2, 3$. Intermodulation distortion terms are those for which neither m nor n is equal to 0. For example, the second-order terms include $(f_a + f_b)$ and $(f_a - f_b)$, and the third-order terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$, and $(f_a - 2f_b)$.

The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels (dB).

Power Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the converter's linearity. PSR is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value. The PSR ratio (PSRR) is defined as the ratio of the power in the ADC output at full-scale frequency, f , to the power of a 100 mV p-p sine wave applied to the ADC's V_{DD} and V_{SS} supplies of Frequency f_s .

$$\text{PSRR (dB)} = 10 \log (P_f/P_{f_s})$$

where:

P_f is equal to the power at Frequency f in the ADC output.

P_{f_s} is equal to the power at Frequency f_s coupled onto the AV_{CC} supply.

Channel-to-Channel Isolation

Channel-to-channel isolation is a measure of the level of crosstalk between all input channels. It is measured by applying a full-scale sine wave signal, up to 160 kHz, to all unselected input channels and then determining the degree to which the signal attenuates in the selected channel with a 1 kHz sine wave signal applied (see Figure 25).

THEORY OF OPERATION

CONVERTER DETAILS

The AD7608 is a data acquisition system that employs a high speed, low power, charge redistribution, successive approximation analog-to-digital converter (ADC) and allows the simultaneous sampling of eight analog input channels. The analog inputs on the AD7608 can accept true bipolar input signals. The RANGE pin is used to select either ± 10 V or ± 5 V as the input range. The AD7608 operates from a single 5 V supply.

The AD7608 contains input clamp protection, input signal scaling amplifiers, a second-order antialiasing filter, track-and-hold amplifiers, an on-chip reference, reference buffers, a high speed ADC, a digital filter, and high speed parallel and serial interfaces. Sampling on the AD7608 is controlled using the CONVST_x signals.

ANALOG INPUT

Analog Input Ranges

The AD7608 can handle true bipolar, single-ended input voltages. The logic level on the RANGE pin determines the analog input range of all analog input channels. If this pin is tied to a logic high, the analog input range is ± 10 V for all channels. If this pin is tied to a logic low, the analog input range is ± 5 V for all channels. A logic change on the RANGE pin has an immediate effect on the analog input range; however, there is typically a settling time of approximately 80 μ s, in addition to the normal acquisition time requirement. The recommended practice is to hardwire the RANGE pin according to the desired input range for the system signals.

During normal operation, the applied analog input voltage should remain within the analog input range selected via the range pin. A RESET pulse must be applied after power-up to ensure the analog input channels are configured for the range selected.

When in a power-down mode, it is recommended to tie the analog inputs to GND. As per the input clamp protection section, the overvoltage clamp protection is recommended for use in transient overvoltage conditions and should not remain active for extended periods. Stressing the analog inputs outside of the conditions mentioned here may degrade the Bipolar Zero Code error and THD performance of the AD7608.

Analog Input Impedance

The analog input impedance of the AD7608 is 1 M Ω . This is a fixed input impedance that does not vary with the AD7608 sampling frequency. This high analog input impedance eliminates the need for a driver amplifier in front of the AD7608, allowing for direct connection to the source or sensor. With the need for a driver amplifier eliminated, bipolar supplies (which are often a source of noise in a system) can be removed from the signal chain.

Analog Input Clamp Protection

Figure 31 shows the analog input structure of the AD7608. Each AD7608 analog input contains clamp protection circuitry. Despite single 5 V supply operation, this analog input clamp protection allows for an input overvoltage up to ± 16.5 V.

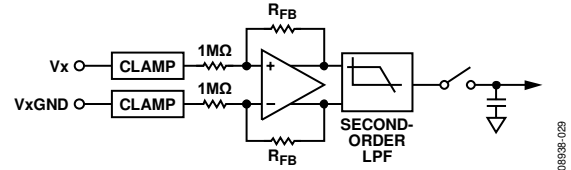


Figure 31. Analog Input Circuitry

Figure 32 shows the voltage vs. current characteristic of the clamp circuit. For input voltages of up to ± 16.5 V, no current flows in the clamp circuit. For input voltages that are above ± 16.5 V, the AD7608 clamp circuitry turns on.

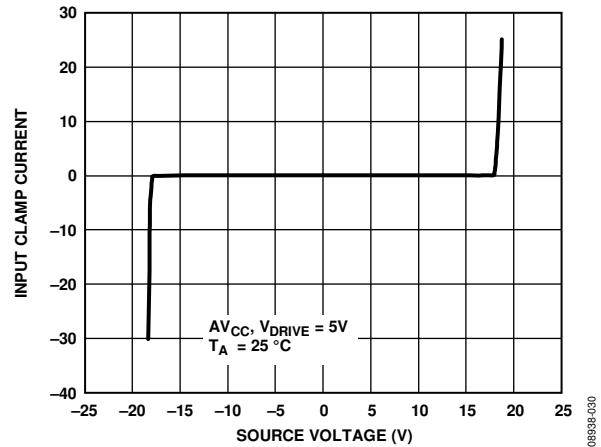


Figure 32. Input Protection Clamp Profile

A series resistor should be placed on the analog input channels to limit the current to ± 10 mA for input voltages above ± 16.5 V. In an application where there is a series resistance on an analog input channel, V_x, a corresponding resistance is required on the analog input GND channel, V_xGND (see Figure 33). If there is no corresponding resistor on the V_xGND channel, an offset error occurs on that channel.

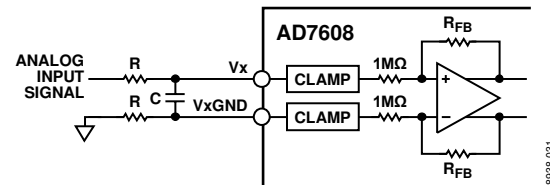


Figure 33. Input Resistance Matching on the Analog Input

Analog Input Antialiasing Filter

An analog antialiasing filter (a second-order Butterworth) is also provided on the AD7608. Figure 34 and Figure 35 show the frequency and phase response, respectively, of the analog antialiasing filter. In the ±5 V range, the -3 dB frequency is typically 15 kHz. In the ±10 V range, the -3 dB frequency is typically 23 kHz.

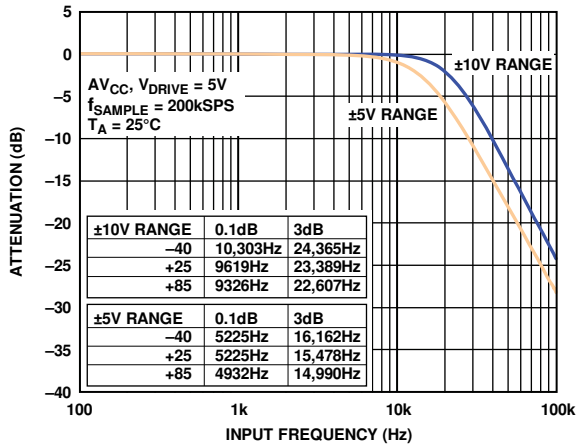


Figure 34. Analog Antialiasing Filter Frequency Response

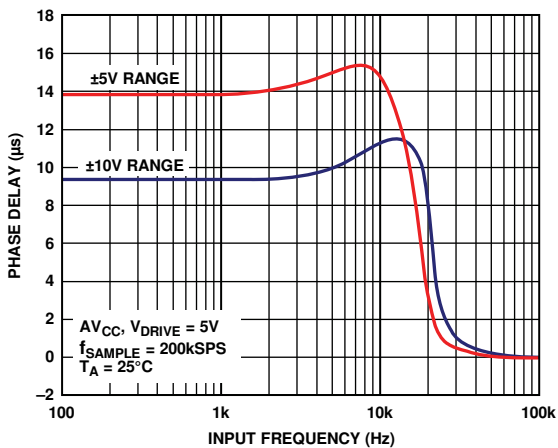


Figure 35. Analog Antialiasing Filter Phase Response

Track-and-Hold Amplifiers

The track-and-hold amplifiers on the AD7608 allow the ADC to accurately acquire an input sine wave of full-scale amplitude to 18-bit resolution. The track-and-hold amplifiers sample their respective inputs simultaneously on the rising edge of CONVST x. The aperture time for track-and-hold (that is, the delay time between the external CONVST x signal and the

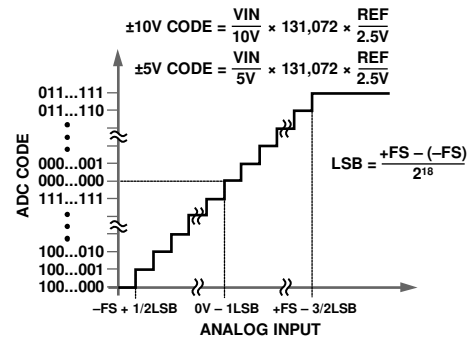
track-and-hold actually going into hold) is well matched, by design, across all eight track-and-holds on one device and from device to device. This matching allows more than one AD7608 device to be sampled simultaneously in a system.

The end of the conversion process across all eight channels is indicated by the falling edge of BUSY; and it is at this point that the track-and-holds return to track mode, and the acquisition time for the next set of conversions begins.

The conversion clock for the part is internally generated, and the conversion time for all channels is 4 µs on the AD7608. The BUSY signal returns low after all eight conversions to indicate the end of the conversion process. On the falling edge of BUSY, the track-and-hold amplifiers return to track mode. New data can be read from the output register via the parallel, parallel byte, or serial interface after BUSY goes low; or, alternatively, data from the previous conversion can be read while BUSY is high. Reading data from the AD7608 while a conversion is in progress has little effect on performance and allows a faster throughput to be achieved. In parallel mode at VDRIVE > 3.3 V, the SNR is reduced by ~1.5 dB when reading during a conversion.

ADC TRANSFER FUNCTION

The output coding of the AD7608 is twos complement. The designed code transitions occur midway between successive integer LSB values, that is, 1/2 LSB, 3/2 LSB. The LSB size is FSR/262,144 for the AD7608. The ideal transfer characteristic for the AD7608 is shown in Figure 36.



	+FS	MIDSCALE	-FS	LSB
±10V RANGE	+10V	0V	-10V	76.29µV
±5V RANGE	+5V	0V	-5V	38.15µV

Figure 36. AD7608 Transfer Characteristic

The LSB size is dependent on the analog input range selected.

INTERNAL/EXTERNAL REFERENCE

The AD7608 contains an on-chip 2.5 V band gap reference. The REFIN/REFOUT pin allows access to the 2.5 V reference that generates the on-chip 4.5 V reference internally, or it allows an external reference of 2.5 V to be applied to the AD7608. An externally applied reference of 2.5 V is also gained up to 4.5 V, using the internal buffer. This 4.5 V buffered reference is the reference used by the SAR ADC.

The REF SELECT pin is a logic input pin that allows the user to select between the internal reference or an external reference. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin. The internal reference buffer is always enabled. After a reset, the AD7608 operates in the reference mode selected by the REF SELECT pin. Decoupling is required on the REFIN/REFOUT pin for both the internal and external reference options. A 10 μF ceramic capacitor is required on the REFIN/REFOUT pin.

The AD7608 contains a reference buffer configured to gain the REF voltage up to ~ 4.5 V, as shown in Figure 37. The REFCAPA and REFCAPB pins must be shorted together externally, and a ceramic capacitor of 10 μF applied to REFGND, to ensure that the reference buffer is in closed-loop operation. The reference voltage available at the REFIN/REFOUT pin is 2.5 V.

When the AD7608 is configured in external reference mode, the REFIN/REFOUT pin is a high input impedance pin. For applications using multiple AD7608 devices, the following configurations are recommended, depending on the application requirements.

External Reference Mode

One [ADR421](#) external reference can be used to drive the REFIN/REFOUT pins of all AD7608 devices (see Figure 38). In this configuration, each REFIN/REFOUT pin of the AD7608 should be decoupled with at least a 100 nF decoupling capacitor.

Internal Reference Mode

One AD7608 device, configured to operate in the internal reference mode, can be used to drive the remaining AD7608 devices, which are configured to operate in external reference mode (see Figure 39). The REFIN/REFOUT pin of the AD7608, configured in internal reference mode, should be decoupled using a 10 μF ceramic decoupling capacitor. The other AD7608 devices, configured in external reference mode, should use at least a 100 nF decoupling capacitor on their REFIN/REFOUT pins.

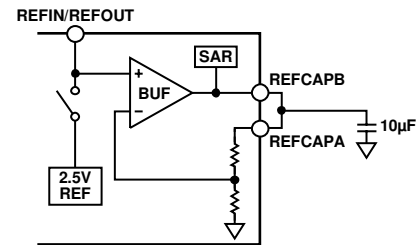


Figure 37. Reference Circuitry

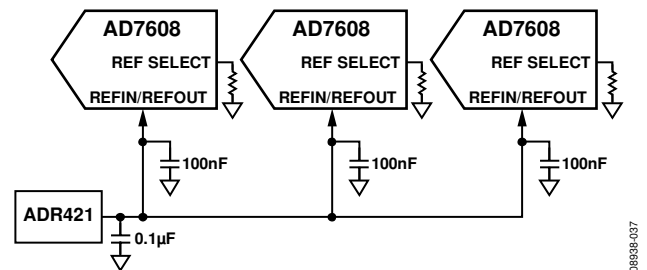


Figure 38. Single External Reference Driving Multiple AD7608 REFIN Pins

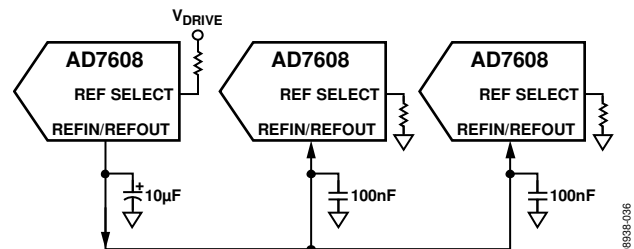


Figure 39. Internal Reference Driving Multiple AD7608 REFIN Pins

TYPICAL CONNECTION DIAGRAM

Figure 40 shows the typical connection diagram for the AD7608. There are four AV_{CC} supply pins on the part, and each of the four pins should be decoupled using a 100 nF capacitor at each supply pin and a 10 μ F capacitor at the supply source. The AD7608 can operate with the internal reference or an externally applied reference. In this configuration, the AD7608 is configured to operate with the internal reference. When using a single AD7608 device on the board, the REFIN/REFOUT pin should be decoupled with a 10 μ F capacitor. Refer to the Internal/External Reference section when using an application with multiple AD7608 devices. The REFCAPA and REFCAPB pins are shorted together and decoupled with a 10 μ F ceramic capacitor.

The V_{DRIVE} supply is connected to the same supply as the processor. The V_{DRIVE} voltage controls the voltage value of the output logic signals. For layout, decoupling, and grounding hints, see the Layout Guidelines section.

After supplies have been applied to the AD7608, apply a RESET signal to the device to ensure it is configured for the correct mode of operation.

POWER-DOWN MODES

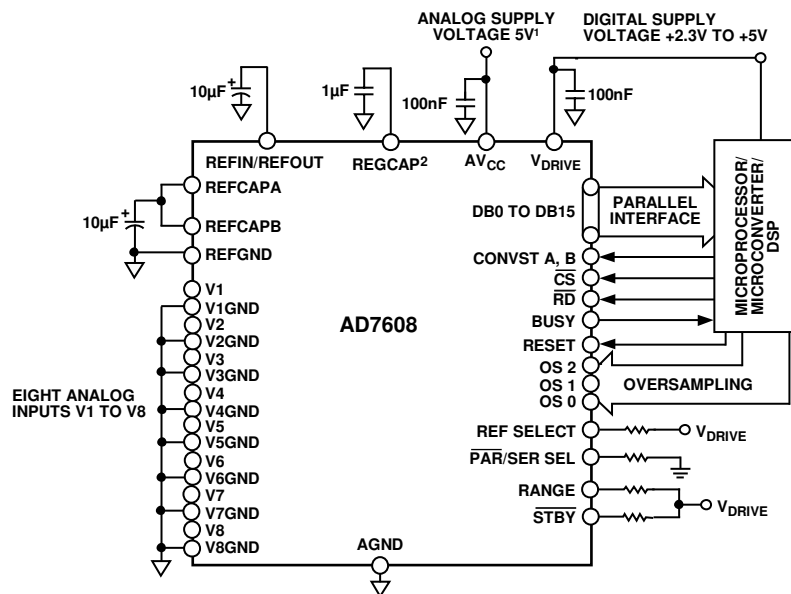
There are two power-down modes available on the AD7608: standby mode and shutdown mode. The STBY pin controls whether the AD7608 is in normal mode or in one of the two power-down modes.

The power-down mode is selected through the state of the RANGE pin when the STBY pin is low. Table 7 shows the configurations required to choose the desired power-down mode. When the AD7608 is placed in standby mode, the current consumption is 8 mA maximum and power-up time is approximately 100 μ s because the capacitor on the REFCAPA and REFCAPB pins must charge up. In standby mode, the on-chip reference and regulators remain powered up, and the amplifiers and ADC core are powered down.

When the AD7608 is placed in shutdown mode, the current consumption is 11 μ A maximum and power-up time is approximately 13 ms (external reference mode). In shutdown mode, all circuitry is powered down. When the AD7608 is powered up from shutdown mode, a RESET signal must be applied to the AD7608 after the required power-up time has elapsed.

Table 7. Power-Down Mode Selection

Power-Down Mode	STBY	RANGE
Standby	0	1
Shutdown	0	0



¹DECOUPLING SHOWN ON THE AV_{CC} PIN APPLIES TO EACH AV_{CC} PIN (PIN 1, PIN 37, PIN 38, PIN 48). DECOUPLING CAPACITOR CAN BE SHARED BETWEEN AV_{CC} PIN 37 AND PIN 38.

²DECOUPLING SHOWN ON THE REGCAP PIN APPLIES TO EACH REGCAP PIN (PIN 36, PIN 39).

06838-038

Figure 40. Typical Connection Diagram

CONVERSION CONTROL

Simultaneous Sampling on All Analog Input Channels

The AD7608 allows simultaneous sampling of all analog input channels. All channels are sampled simultaneously when both CONVST x pins (CONVST A, CONVST B) are tied together. A single CONVST x signal is used to control both CONVST x inputs. The rising edge of this common CONVST x signal initiates simultaneous sampling on all analog input channels.

The AD7608 contains an on-chip oscillator that is used to perform the conversions. The conversion time for all ADC channels is t_{CONV} . The BUSY signal indicates to the user when conversions are in progress, so when the rising edge of CONVST x is applied, BUSY goes logic high and transitions low at the end of the entire conversion process. The falling edge of the BUSY signal is used to place all eight track-and-hold amplifiers back into track mode. The falling edge of BUSY also indicates that the new data can now be read from the parallel bus (DB[15:0]), or the D_{OUT}A and D_{OUT}B serial data lines.

Simultaneously Sampling Two Sets of Channels

The AD7608 also allows the analog input channels to be sampled simultaneously in two sets. This can be used in power-line protection and measurement systems to compensate for phase differences introduced by PT and CT transformers. In a 50 Hz system, this allows for up to 9° of phase compensation; and in a 60 Hz system, it allows for up to 10° of phase compensation.

This is accomplished by pulsing the two CONVST x pins independently and is possible only if oversampling is not in use. CONVST A is used to initiate simultaneous sampling of the first set of channels (V1 to V4) and CONVST B is used to initiate simultaneous sampling on the second set of analog input channels (V5 to V8), as illustrated in Figure 41. On the rising edge of CONVST A, the track-and-hold amplifiers for the first set of channels are placed into hold mode. On the rising edge of CONVST B, the track-and-hold amplifiers for the second set of channels are placed into hold mode. The conversion process begins once both rising edges of CONVST x have occurred; therefore BUSY goes high on the rising edge of the later CONVST x signal. In Table 3, Time t_5 indicates the maximum allowable time between CONVST x sampling points.

There is no change to the data read process when using two separate CONVST x signals.

Connect all unused analog input channels to AGND. The results for any unused channels are still included in the data read because all channels are always converted.

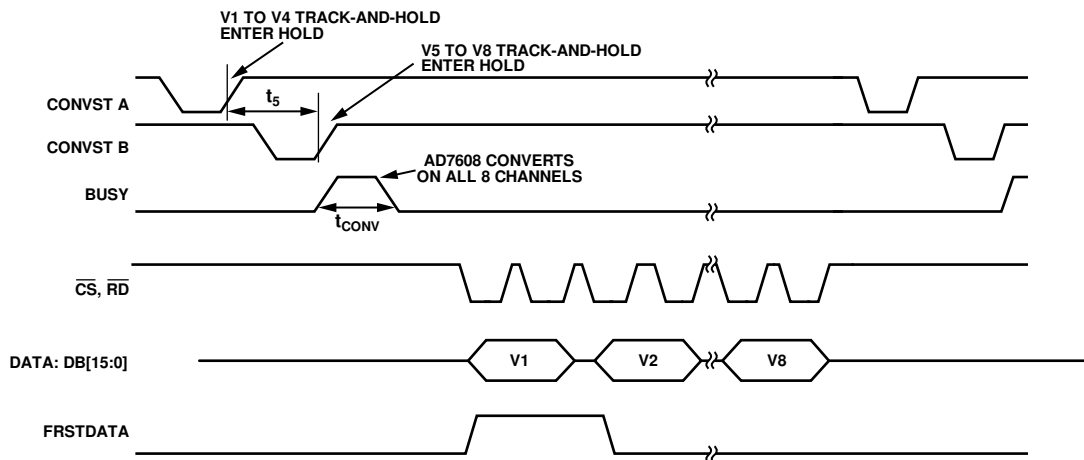


Figure 41. Simultaneous Sampling on Channel Sets Using Independent CONVST A/CONVST B Signals—Parallel Mode

08938-1039

DIGITAL INTERFACE

The AD7608 provides two interface options: a parallel interface and high speed serial interface. The required interface mode is selected via the $\overline{\text{PAR/SER SEL}}$ pin.

The operation of the interface modes is discussed in the following sections.

PARALLEL INTERFACE ($\overline{\text{PAR/SER SEL}} = 0$)

Data can be read from the AD7608 via the parallel data bus with standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals. To read the data over the parallel bus, the $\overline{\text{PAR/SER SEL}}$ pin should be tied low. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ input signals are internally gated to enable the conversion result onto the data bus. The data lines, DB15 to DB0, leave their high impedance state when both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic low.

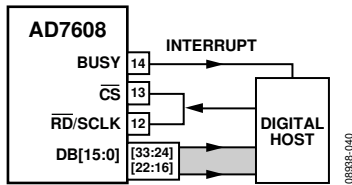


Figure 42. AD7608 interface diagram—One AD7608 Using the Parallel Bus; $\overline{\text{CS}}$ and $\overline{\text{RD}}$ Shorted Together

The rising edge of the $\overline{\text{CS}}$ input signal three-states the bus and the falling edge of the $\overline{\text{CS}}$ input signal takes the bus out of the high impedance state. $\overline{\text{CS}}$ is the control signal that enables the data lines, it is the function that allows multiple AD7608 devices to share the same parallel data bus.

The $\overline{\text{CS}}$ signal can be permanently tied low, and the $\overline{\text{RD}}$ signal can be used to access the conversion results as shown in Figure 4. A read operation of new data can take place after the $\overline{\text{BUSY}}$ signal goes low (Figure 2), or alternatively a read operation of data from the previous conversion process can take place while $\overline{\text{BUSY}}$ is high (Figure 3).

The $\overline{\text{RD}}$ pin is used to read data from the output conversion results register. Two $\overline{\text{RD}}$ pulses are required to read the full 18-bit conversion result from each channel. Applying a sequence of 16 $\overline{\text{RD}}$ pulses to the AD7608 $\overline{\text{RD}}$ pin clocks the conversion results out from each channel onto the 16-bit parallel output bus in ascending order. The first $\overline{\text{RD}}$ falling edge after $\overline{\text{BUSY}}$ goes low clocks out DB[17:2] of the V1 result, the next $\overline{\text{RD}}$ falling edge updates the bus with DB[1:0] of V1 result. It takes 16 $\overline{\text{RD}}$ pulses to read the eight 18-bit conversion results from the AD7608. On the AD7608, the 16th falling edge of $\overline{\text{RD}}$ clocks out the DB[1:0] conversion result for Channel V8. When the $\overline{\text{RD}}$ signal is logic low, it enables the data conversion result from each channel to be transferred to the digital host (DSP, FPGA).

When there is only one AD7608 in a system/board and it does not share the parallel bus, data can be read using just one control signal from the digital host. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals can be tied together as shown in Figure 5. In this case, the data bus comes out of three-state on the falling edge of $\overline{\text{CS}}/\overline{\text{RD}}$. The combined $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signal allows the data to be clocked out of the AD7608 and to be read by the digital host. In this case, $\overline{\text{CS}}$ is used to frame the data transfer of each data channel. In this case, 16 $\overline{\text{CS}}$ pulses are required to read the eight channels of data.