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16-Channel DAS with 16-Bit, Bipolar Input, Dual Simultaneous Sampling ADC

Data Sheet **AD7616**

FEATURES

- 16-channel, dual, simultaneously sampled inputs
- Independently selectable channel input ranges
  - True bipolar: ±10 V, ±5 V, ±2.5 V
- Single 5 V analog supply and 2.3 V to 3.6 V V_{DRIVE} supply
- Fully integrated data acquisition solution
  - Analog input clamp protection
  - Input buffer with 1 MΩ analog input impedance
  - First-order antialiasing analog filter
  - On-chip accurate reference and reference buffer
  - Dual 16-bit successive approximation register (SAR) ADC
  - Throughput rate: 2 × 1 MSPS
  - Oversampling capability with digital filter
  - Flexible sequencer with burst mode
- Flexible parallel/serial interface
  - SPI/QSPI/MICROWIRE/DSP compatible
  - Optional cyclic redundancy check (CRC) error checking
- Hardware/software configuration
- Performance
  - 92 dB SNR at 500 kSPS (2× oversampling)
  - 90.5 dB SNR at 1 MSPS
  - −103 dB THD
  - ±1 LSB INL (typical), ±0.99 LSB DNL (maximum)
  - 8 kV ESD rating on analog input channels
- On-chip self detect function
- 80-lead LQFP package

APPLICATIONS

- Power line monitoring
- Protective relays
- Multiphase motor control
- Instrumentation and control systems
- Data acquisition systems (DASs)

GENERAL DESCRIPTION

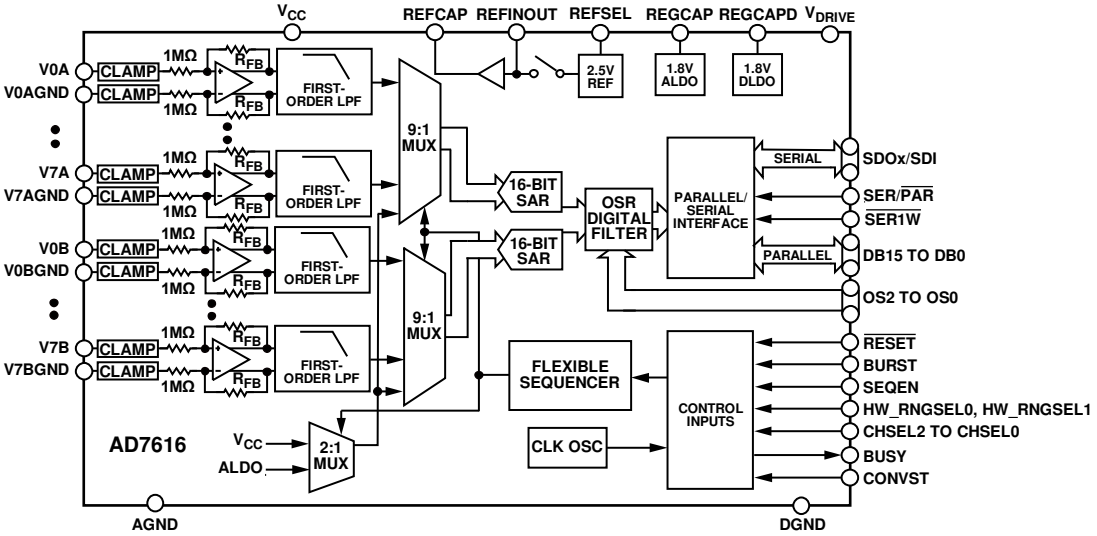
The AD7616 is a 16-bit, DAS that supports dual simultaneous sampling of 16 channels. The AD7616 operates from a single 5 V supply and can accommodate ±10 V, ±5 V, and ±2.5 V true bipolar input signals while sampling at throughput rates up to 1 MSPS per channel pair with 90.5 dB SNR. Higher SNR performance can be achieved with the on-chip oversampling mode (92 dB for an oversampling ratio (OSR) of 2).

The input clamp protection circuitry can tolerate voltages up to ±21 V. The AD7616 has 1 MΩ analog input impedance, regardless of sampling frequency. The single-supply operation, on-chip filtering, and high input impedance eliminate the need for driver op amps and external bipolar supplies.

The device contains analog input clamp protection, a dual, 16-bit charge redistribution SAR analog-to-digital converter (ADC), a flexible digital filter, a 2.5 V reference and reference buffer, and high speed serial and parallel interfaces.

The AD7616 is serial peripheral interface (SPI)/QSPI™/DSP/MICROWIRE compatible

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. MULTIFUNCTION PINS, SUCH AS DB15/OS2, ARE REFERRED TO BY A SINGLE FUNCTION OF THE PIN, FOR EXAMPLE, DB15, WHEN ONLY THAT FUNCTION IS RELEVANT. REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION FOR MORE INFORMATION.

13591-001

Figure 1.

Rev. 0 Document Feedback

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Technical Support www.analog.com

AD7616* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7616 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1409: Achieving Pseudosimultaneous Sampling by Using the AD7616 Flexible Sequencer and Burst Mode

Data Sheet

- AD7616: 16-Channel DAS with 16-Bit, Bipolar Input, Dual Simultaneous Sampling ADC Data Sheet

Product Highlight

- AD7616 Data Acquisition System

User Guides

- UG-1012: Evaluating the AD7616 16-Channel DAS with 16-Bit, Bipolar Input, Dual Simultaneous Sampling ADC

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD7616 No-OS/HDL Drivers

TOOLS AND SIMULATIONS

- AD7616 IBIS Model

REFERENCE MATERIALS

Press

- Data Acquisition System Protects Smart Grid Equipment from Harmful Faults While Improving Power Delivery

DESIGN RESOURCES

- AD7616 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7616 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

10/2016—Revision 0: Initial Version

SPECIFICATIONS

V_{REF} = 2.5 V external/internal, V_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 3.6 V, f_{SAMPLE} = 1 MSPS, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	f_{IN} = 1 kHz sine wave unless otherwise noted				
Signal-to-Noise Ratio (SNR)[1, 2]	No oversampling, ±10 V range	89	90.5		dB
	OSR = 2, ±10 V range,[3] f_{SAMPLE} = 500 kSPS		92		dB
	OSR = 4, ±10 V range[3]		93		dB
	No oversampling, ±5 V range	88	89.5		dB
	No oversampling, ±2.5 V range	85.5	87		dB
Signal-to-Noise-and-Distortion (SINAD)[1]	No oversampling, ±10 V range	88.5	90		dB
	No oversampling, ±5 V range	87.5	89		dB
	No oversampling, ±2.5 V range	85	87		dB
Dynamic Range	No oversampling, ±10 V range		92		dB
	No oversampling, ±5 V range		90.5		dB
	No oversampling, ±2.5 V range		88		dB
Total Harmonic Distortion (THD)[1]	No oversampling, ±10 V range		−103	−93.5	dB
	No oversampling, ±5 V range		−100		dB
	No oversampling, ±2.5 V range		−97		dB
Peak Harmonic or Spurious Noise[1]			−103		dB
Intermodulation Distortion (IMD)[1]	fa = 1 kHz, fb = 1.1 kHz				
Second-Order Terms			−105		dB
Third-Order Terms			−113		dB
Channel to Channel Isolation[1]	f_{IN} on unselected channels up to 5 kHz		−106		dB
ANALOG INPUT FILTER					
Full Power Bandwidth	−3 dB, ±10 V range		39		kHz
	−3 dB, ±5 V/2.5 V range		33		kHz
	−0.1 dB		5.5		kHz
Phase Delay[3]	±10 V range		4.4	6	µs
	±5 V range		5		µs
	±2.5 V range		4.9		µs
Phase Delay Drift[3]	±10 V range		±0.55	5	ns/°C
Phase Delay Matching (Dual Simultaneous Pair)[3]	±10 V range		4.4	100	ns
	±5 V range		4.7		ns
	±2.5 V range		4.1		ns
DC ACCURACY					
Resolution	No missing codes	16			Bits
Differential Nonlinearity (DNL)[1]			±0.5	±0.99	LSB[4]
Integral Nonlinearity (INL)[1]			±1	±2	LSB
Total Unadjusted Error (TUE)	±10 V range		±6		LSB
	±5 V range		±8		LSB
	±2.5 V range		±10		LSB
Positive Full-Scale Error[5]					
External reference	±10 V range		±5	±32	LSB
	±5 V range		± 4		LSB
	±2.5 V range		± 2		LSB
Internal reference					
	±10 V range		±5		LSB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Positive Full-Scale (PFS) Error Drift[3]	External reference		±2	±5	ppm/°C
	Internal reference		±3	±10	ppm/°C
Positive Full-Scale Error Matching[1]	±10 V range		3	11	LSB
	±5 V range		4		LSB
	±2.5 V range		8		LSB
Bipolar Zero Code Error[1]	±10 V range		±0.8	±8	LSB
	±5 V range		±1	±10	LSB
	±2.5 V range		±3	±15	LSB
Bipolar Zero Code Error Drift[3]	±10 V range		±1.3	±20.4	µV/°C
	±5 V range		±0.9		µV/°C
	±2.5 V range		±0.5		µV/°C
Bipolar Zero Code Error Matching	±10 V range		±2	±10	LSB
	±5 V range		±3		LSB
	±2.5 V range		±3		LSB
Negative Full-Scale (NFS) Error[1, 5]	External reference				
	±10 V range		±4	±32	LSB
	±5 V range		±3		LSB
	±2.5 V range		±6		LSB
	Internal reference				
	±10 V range		±3		LSB
Negative Full-Scale Error Drift[3]	External reference		±2	±5	ppm/°C
	Internal reference		±4		ppm/°C
Negative Full-Scale Error Matching[1]	±10 V range		4	12	LSB
	±5 V range		4		LSB
	±2.5 V range		8		LSB
ANALOG INPUT					
Input Voltage Ranges	Software/hardware selectable			±10	V
	Software/hardware selectable			±5	V
	Software/hardware selectable			±2.5	V
Analog Input Current	±10 V range, see Figure 34		±10.5		µA
	±5 V range, see Figure 34		±6.5		µA
	±2.5 V range, see Figure 34		±4		µA
Input Capacitance[6]			10		pF
Input Impedance	See the Analog Input section	0.85	1		MΩ
Input Impedance Drift[3]				25	ppm/°C
REFERENCE INPUT/OUTPUT					
Reference Input Voltage Range	See the ADC Transfer Function section	2.495	2.5	2.505	V
DC Leakage Current				±1	µA
Input Capacitance[6]	REFSEL = 1		7.5		pF
Reference Output Voltage	REFINOUT	2.495		2.505	V
Reference Temperature Coefficient[3]			±2	±15	ppm/°C
LOGIC INPUTS					
Input Voltage					
High (V_{INH})	V_{DRIVE} = 2.7 V to 3.6 V	2			V
	V_{DRIVE} = 2.3 V to 2.7 V	1.7			V
Low (V_{INL})	V_{DRIVE} = 2.7 V to 3.6 V			0.8	V
	V_{DRIVE} = 2.3 V to 2.7 V			0.7	V
Input Current (I_{IN})				±1	µA
Input Capacitance (C_{IN})[6]			5		pF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC OUTPUTS					
Output Voltage					
High (V_{OH})	I_{SOURCE} = 100 µA	V_{DRIVE} − 0.2			V
Low (V_{OL})	I_{SINK} = 100 µA			0.4	V
Floating State Leakage Current			±0.005	±1	µA
Floating State Output Capacitance[6]			5		pF
Output Coding	Twos complement				
CONVERSION RATE					
Conversion Time	Per channel pair		0.5		µs
Acquisition Time	Per channel pair		0.5		µs
Throughput Rate	Per channel pair			1	MSPS
POWER REQUIREMENTS					
V_{CC}		4.75		5.25	V
V_{DRIVE}		2.3		3.6	V
I_{VCC}					
Normal Mode					
Static			37	57	mA
Operational	f_{SAMPLE} = 1 MSPS		42	65	mA
Shutdown Mode			28		µA
I_{DRIVE}	Digital inputs = 0 V or V_{DRIVE}				
Normal Mode					
Static			0.3	0.75	mA
Operational	f_{SAMPLE} = 1 MSPS		7	8	mA
Shutdown Mode			50		µA
Power Dissipation					
Normal Mode					
Static			185	300	mW
Operational	f_{SAMPLE} = 1 MSPS		230	350	mW
Shutdown Mode			0.75		mW

[1] See the Terminology section.
[2] The user can achieve 93 dB SNR by enabling oversampling. The values are valid for manual mode. In burst mode, values degrade by ~1 dB.
[3] Not production tested. Sample tested during initial release to ensure compliance.
[4] LSB means least significant bit. With a ±2.5 V input range, 1 LSB = 76.293 µV. With a ±5 V input range, 1 LSB = 152.58 µV. With a ±10 V input range, 1 LSB = 305.175 µV.
[5] Positive and negative full-scale error for the internal reference excludes reference errors.
[6] Supported by simulation data.

TIMING SPECIFICATIONS

Universal Timing Specifications

V_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 3.6 V, V_{REF} = 2.5 V external reference/internal reference, T_A = −40°C to +125°C, unless otherwise noted. Interface timing tested using a load capacitance of 30 pF, dependent on V_{DRIVE} and load capacitance for serial interface (see Table 14).

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Description
t_{CYCLE}	1			µs	Minimum time between consecutive CONVST rising edges (excluding burst and oversampling modes)
t_{CONV_LOW}	50			ns	CONVST low pulse width
t_{CONV_HIGH}	50			ns	CONVST high pulse width
t_{BUSY_DELAY}			32	ns	CONVST high to BUSY high (manual mode)
t_{CS_SETUP}	20			ns	BUSY falling edge to $\overline{CS}$ falling edge setup time
t_{CH_SETUP}	50			ns	Channel select setup time in hardware mode for CHSELx
t_{CH_HOLD}	20			ns	Channel select hold time in hardware mode for CHSELx
t_{CONV}		475	520	ns	Conversion time for the selected channel pair
t_{ACQ}	480			ns	Acquisition time for the selected channel pair
t_{QUIET}	50			ns	$\overline{CS}$ rising edge to next CONVST rising edge
$t_{\overline{RESET}\_LOW}$					
Partial Reset	40		500	ns	Partial $\overline{RESET}$ low pulse width
Full Reset	1.2			µs	Full $\overline{RESET}$ low pulse width
t_{DEVICE_SETUP}					
Partial Reset	50			ns	Time between partial $\overline{RESET}$ high and CONVST rising edge
Full Reset	15			ms	Time between full $\overline{RESET}$ high and CONVST rising edge
t_{WRITE}					
Partial Reset	50			ns	Time between partial $\overline{RESET}$ high and $\overline{CS}$ for write operation
Full Reset	240			µs	Time between full $\overline{RESET}$ high and $\overline{CS}$ for write operation
$t_{\overline{RESET}\_WAIT}$	1			ms	Time between stable V_{CC}/V_{DRIVE} and release of $\overline{RESET}$ (see Figure 50)
$t_{\overline{RESET}\_SETUP}$					Time prior to release of $\overline{RESET}$ that queried hardware inputs must be stable for (see Figure 50)
Partial Reset	10			ns	
Full Reset	0.05			ms	
$t_{\overline{RESET}\_HOLD}$					Time after release of $\overline{RESET}$ that queried hardware inputs must be stable for (see Figure 50)
Partial Reset	10			ns	
Full Reset	0.24			ms	

[1] Not production tested. Sample tested during initial release to ensure compliance.

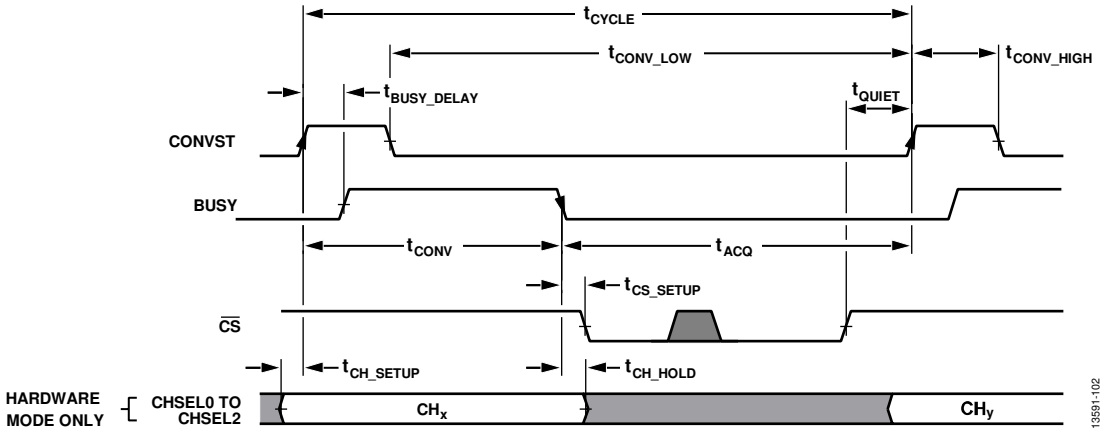


Figure 2. Universal Timing Diagram Across All Interfaces

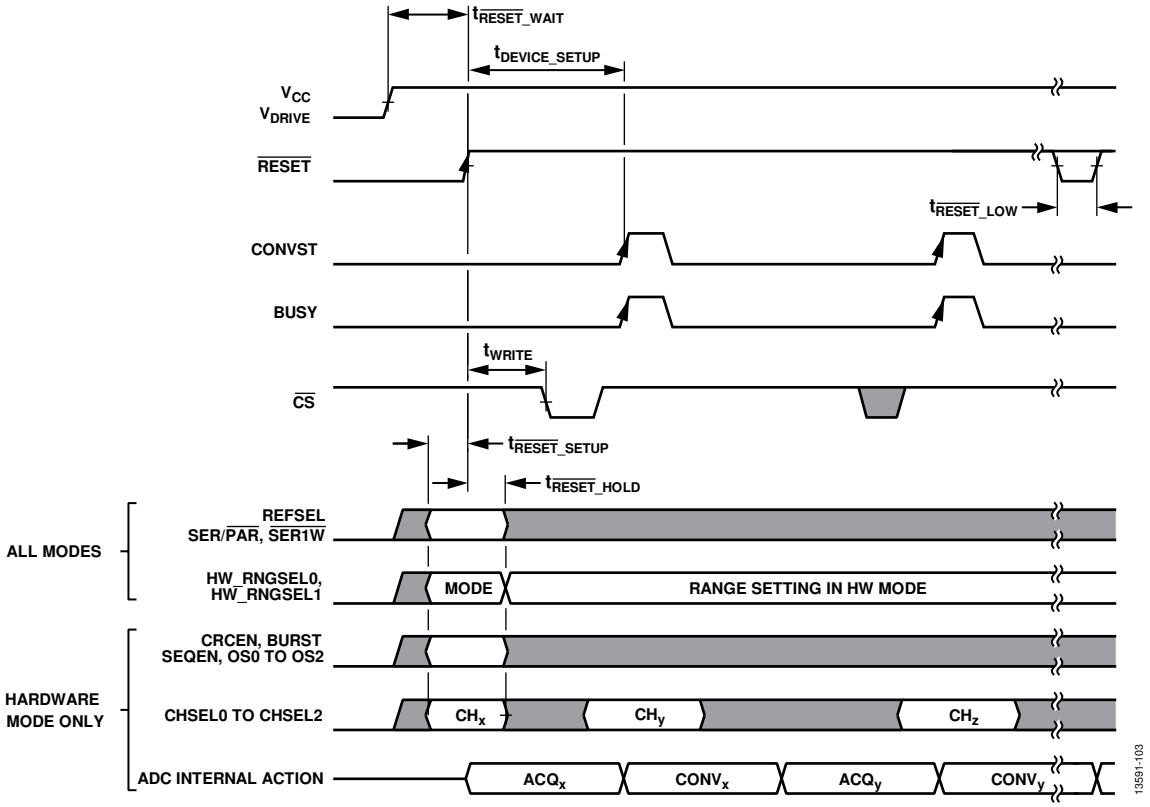


Figure 3. Reset Timing

Parallel Mode Timing Specifications

Table 3.

Parameter	Min	Typ	Max	Unit	Description
$t_{\overline{RD}\_SETUP}$	10			ns	$\overline{CS}$ falling edge to $\overline{RD}$ falling edge setup time
$t_{\overline{RD}\_HOLD}$	10			ns	$\overline{RD}$ rising edge to $\overline{CS}$ rising edge hold time
$t_{\overline{RD}\_HIGH}$	10			ns	$\overline{RD}$ high pulse width
$t_{\overline{RD}\_LOW}$	30			ns	$\overline{RD}$ low pulse width
t_{DOUT_SETUP}			30	ns	Data access time after falling edge of $\overline{RD}$
t_{DOUT_3STATE}			11	ns	$\overline{CS}$ rising edge to DBx high impedance
$t_{\overline{WR}\_SETUP}$	10			ns	$\overline{CS}$ to $\overline{WR}$ setup time
$t_{\overline{WR}\_HIGH}$	20			ns	$\overline{WR}$ high pulse width
$t_{\overline{WR}\_LOW}$	30			ns	$\overline{WR}$ low pulse width
$t_{\overline{WR}\_HOLD}$	10			ns	$\overline{WR}$ hold time
t_{DIN_SETUP}	30			ns	Configuration data to $\overline{WR}$ setup time
t_{DIN_HOLD}	10			ns	Configuration data to $\overline{WR}$ hold time
t_{CONF_SETTLE}	20			ns	Configuration data settle time, $\overline{WR}$ rising edge to CONVST rising edge

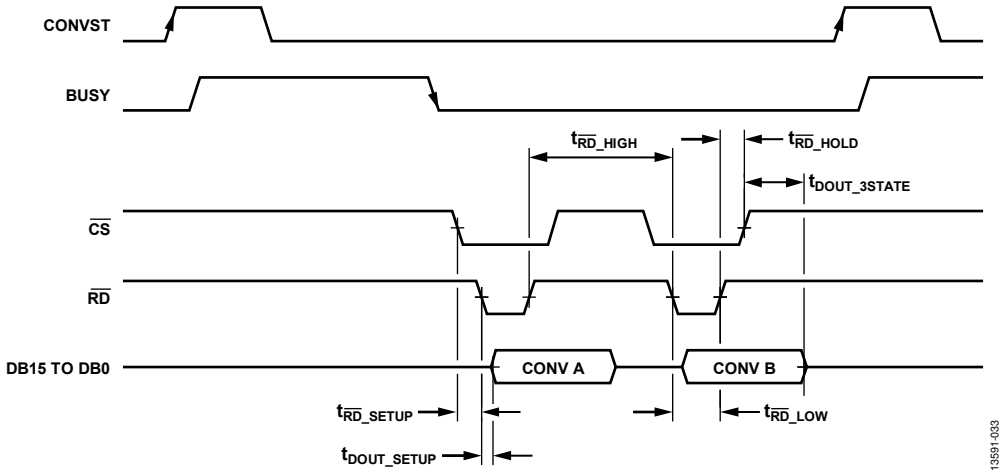


Figure 4. Parallel Read Timing Diagram

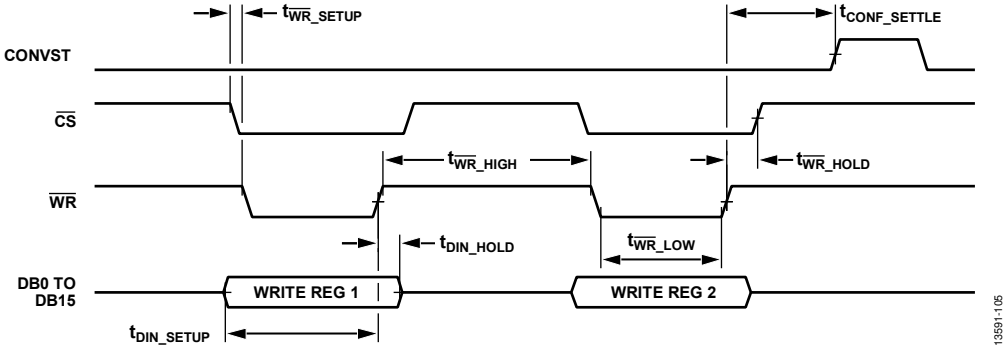


Figure 5. Parallel Write Timing Diagram

Serial Mode Timing Specifications

Table 4.

Parameter	Min	Typ	Max	Unit	Description
f_{SCLK}[1]			40/50	MHz	SCLK frequency
t_{SCLK}	$1/f_{SCLK}$				Minimum SCLK period
t_{SCLK_SETUP}[1]	10.5			ns	$\overline{CS}$ to SCLK falling edge setup time, V_{DRIVE} above 3 V
	13.5			ns	$\overline{CS}$ to SCLK falling edge setup time, V_{DRIVE} above 2.3 V
t_{SCLK_HOLD}	10			ns	SCLK to $\overline{CS}$ rising edge hold time
t_{SCLK_LOW}	8			ns	SCLK low pulse width
t_{SCLK_HIGH}	9			ns	SCLK high pulse width
t_{DOUT_SETUP}[1]			9	ns	Data out access time after SCLK rising edge, V_{DRIVE} above 3 V
			11	ns	Data out access time after SCLK rising edge, V_{DRIVE} above 2.3 V
t_{DOUT_HOLD}	4			ns	Data out hold time after SCLK rising edge
t_{DIN_SETUP}	10			ns	Data in setup time before SCLK falling edge
t_{DIN_HOLD}	8			ns	Data in hold time after SCLK falling edge
t_{DOUT_3STATE}			10	ns	$\overline{CS}$ rising edge to SDOx high impedance

[1] Dependent on V_{DRIVE} and load capacitance (see Table 14).

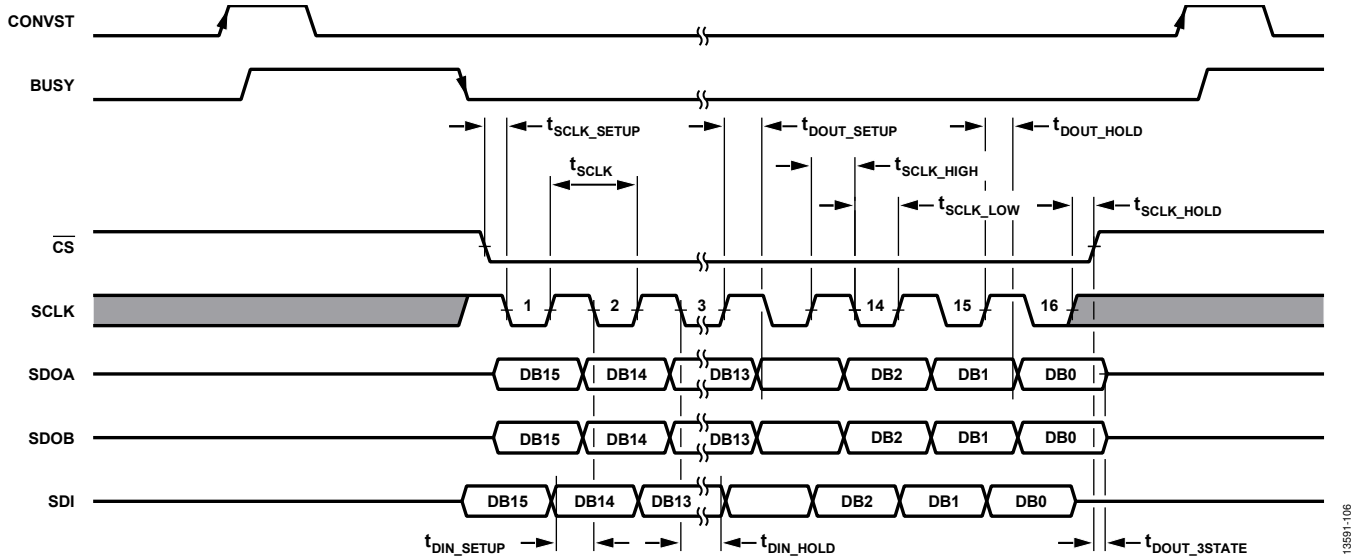


Figure 6. Serial Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{CC} to AGND	−0.3 V to +7 V
V_{DRIVE} to AGND	−0.3 V to V_{CC} + 0.3 V
Analog Input Voltage to AGND[1]	±21 V
Digital Input Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
REFINOUT to AGND	−0.3 V to V_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Soldering Reflow	
Pb/Sn Temperature (10 sec to 30 sec)	240 (+0)°C
Pb-Free Temperature	260 (+0)°C
ESD	
All Pins Except Analog Inputs	2 kV
Analog Input Pins Only	8 kV

[1] Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
ST-80-2[1]	41	7.5	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

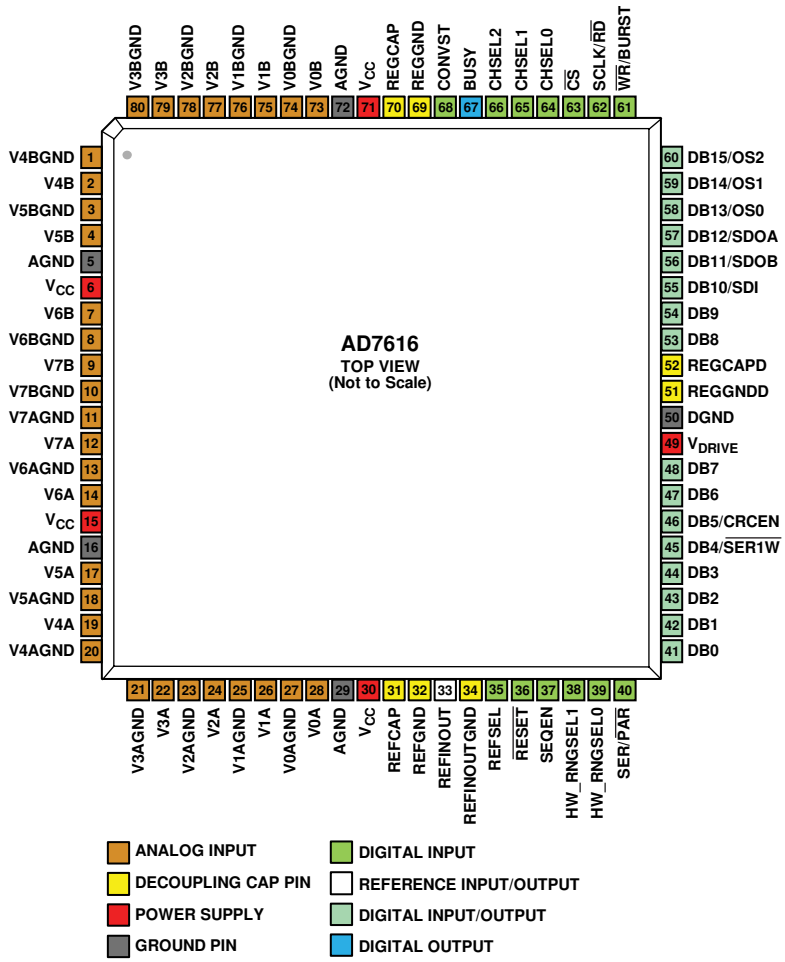


Figure 7. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Type[1]	Mnemonic[2]	Description
1	AI GND	V4BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V4B.
2	AI	V4B	Analog Input for Channel 4, ADC B.
3	AI GND	V5BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V5B.
4	AI	V5B	Analog Input for Channel 5, ADC B.
5, 16, 29, 72	P	AGND	Analog Supply Ground Pins.
6, 15, 30, 71	P	V_{CC}	Analog Supply Voltage, 4.7 V to 5.25 V. This supply voltage is applied to the internal front-end amplifiers and to the ADC core. Decouple these pins to AGND using 0.1 µF and 10 µF capacitors in parallel.
7	AI	V6B	Analog Input for Channel 6, ADC B.
8	AI GND	V6BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V6B.
9	AI	V7B	Analog Input for Channel 7, ADC B.
10	AI GND	V7BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V7B.
11	AI GND	V7AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V7A.
12	AI	V7A	Analog Input for Channel 7, ADC A.
13	AI GND	V6AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V6A.
14	AI	V6A	Analog Input for Channel 6, ADC A.
17	AI	V5A	Analog Input V5A.
18	AI GND	V5AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V5A.
19	AI	V4A	Analog Input V4A.
20	AI GND	V4AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V4A.

Pin No.	Type[1]	Mnemonic[2]	Description
21	AI GND	V3AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V3A.
22	AI	V3A	Analog Input for Channel 3, ADC A.
23	AI GND	V2AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V2A.
24	AI	V2A	Analog Input for Channel 2, ADC A.
25	AI GND	V1AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V1A.
26	AI	V1A	Analog Input for Channel 1, ADC A.
27	AI GND	V0AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V0A.
28	AI	V0A	Analog Input for Channel 0, ADC A.
31	CAP	REFCAP	Reference Buffer Output Force/Sense Pin. Decouple this pin to AGND using a low effective series resistance (ESR), 10 µF, X5R ceramic capacitor, as close to the REFCAP pin as possible. The voltage on this pin is typically 4.096 V.
32	CAP	REFGND	Reference Ground pin. Connect this pin to AGND.
33	REF	REFINOUT	Reference Input/Reference Output. The on-chip reference of 2.5 V is available on this pin for external use when the REFSEL pin is set to logic high. Alternatively, the internal reference can be disabled by setting the REFSEL pin to logic low, and an external reference of 2.5 V can be applied to this input. Decoupling is required on this pin for both the internal and external reference options. Connect a 100 nF, X8R capacitor between the REFINOUT and REFINOUTGND pins, as close to the REFINOUT pin as possible. If using an external reference, connect a 10 kΩ series resistor to this pin to band limit the reference signal.
34	CAP	REFINOUTGND	Reference Input, Reference Output Ground Pin.
35	DI	REFSEL	Internal/External Reference Selection Input. REFSEL is a logic input. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFINOUT pin. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure.
36	DI	$\overline{\text{RESET}}$	Reset Input. Full and partial reset options are available. The type of reset is determined by the length of the $\overline{\text{RESET}}$ pulse. Keeping $\overline{\text{RESET}}$ low places the device into shutdown mode. See the Reset Functionality section for further details.
37	DI	SEQEN	Channel Sequencer Enable Input (Hardware Mode Only). When SEQEN is tied low, the sequencer is disabled. When SEQEN is high, the sequencer is enabled (with restricted functionality in hardware mode). See the Sequencer section for further details. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. In software mode, this pin must be connected to DGND.
38, 39	DI	HW_RNGSEL1, HW_RNGSEL0	Hardware/Software Mode Selection, Hardware Mode Range Select Inputs. Hardware/software mode selection is latched at full reset. Range selection in hardware mode is not latched. HW_RNGSELx = 00: software mode; the AD7616 is configured via the software registers. HW_RNGSELx = 01: hardware mode; analog input range is ±2.5 V. HW_RNGSELx = 10: hardware mode; analog input range is ±5 V. HW_RNGSELx = 11: hardware mode; analog input range is ±10 V.
40	DI	SER/$\overline{\text{PAR}}$	Serial/Parallel Interface Selection Input. Logic input. If this pin is tied to a logic low, the parallel interface is selected. If this pin is tied to logic high, the serial interface is selected. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure.
41, 42, 43, 44	DO/DI	DB0, DB1, DB2, DB3	Parallel Output/Input Data Bit 0 to Data Bit 3. In parallel mode, these pins are output/input parallel data bits, DB7 to DB0. Refer to the Parallel Interface section for further details. In serial mode, these pins must be tied to DGND.
45	DO/DI	DB4/$\overline{\text{SER1W}}$	Parallel Output/Input Data Bit 4/Serial Output Selection. In parallel mode, this pin acts as a three-state parallel digital output/input pin. Refer to the Parallel Interface section for further details. In serial mode, this pin determines whether the serial output operates over SDOA and SDOB or just SDOA. When $\overline{\text{SER1W}}$ is low, the serial output operates over SDOA only. When $\overline{\text{SER1W}}$ is high, the serial output operates over both SDOA and SDOB. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure.

Pin No.	Type[1]	Mnemonic[2]	Description
46	DO/DI	DB5/CRCEN	Parallel Output/Input Data Bit 5/CRC Enable Input. In parallel mode, this pin acts as a three-state parallel digital input/output. While in serial mode, this pin acts as a CRC enable input. The CRCEN signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. Refer to the Digital Interface section for further details. In serial mode, when CRCEN is low, there is no CRC word following the conversion results; when CRCEN is high, an extra CRC word follows the last conversion word configured by CHSELx. See the CRC section for further details. In software mode, this pin must be connected to DGND.
47, 48	DO/DI	DB6, DB7	Parallel Output/Input Data Bit 6 and Data Bit 7. When SER/$\overline{PAR}$ = 0, these pins act as three-state parallel digital input/outputs. Refer to the Parallel Interface section for further details. In serial mode, when SER/$\overline{PAR}$ = 1 these pins must be tied to DGND.
49	P	V_{DRIVE}	Logic Power Supply Input. The voltage (2.3 V to 3.6 V) supplied at this pin determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface. Decouple this pin with 0.1 µF and 10 µF capacitors in parallel.
50	P	DGND	Digital Ground. This pin is the ground reference point for all digital circuitry on the AD7616. The DGND pin must connect to the DGND plane of a system.
51	CAP	REGGNDD	Ground for the Digital Low Dropout (LDO) Regulator Connected to REGCAPD (Pin 52).
52	CAP	REGCAPD	Decoupling Capacitor Pin for Voltage Output from Internal Digital Regulator. Decouple this output pin separately to REGGNDD using a 10 µF capacitor. The voltage at this pin is 1.89 V typical.
53, 54	DO/DI	DB8, DB9	Parallel Output/Input Data Bit 9 and Data Bit 8. When SER/$\overline{PAR}$ = 0, these pins act as three-state parallel digital input/outputs. Refer to the Parallel Interface section for further details. In serial mode, when SER/$\overline{PAR}$ = 1, these pins must be tied to DGND.
55	DO/DI	DB10/SDI	Parallel Output/Input Data Bit DB10/Serial Data Input. When SER/$\overline{PAR}$ = 0, this pin acts as a three-state parallel digital input/output. Refer to the Parallel Interface section for further details. In hardware serial mode, tie this pin to DGND. In serial mode, when SER/$\overline{PAR}$ = 1, this pin acts as the data input of the SPI interface.
56	DO/DI	DB11/SDOB	Parallel Output/Input Data Bit 11/Serial Data Output B. When SER/$\overline{PAR}$ = 0, this pin acts as a three-state parallel digital input/output. Refer to the Parallel Interface section for further details. In serial mode, when SER/$\overline{PAR}$ = 1, this pin functions as SDOB and outputs serial conversion data.
57	DO/DI	DB12/SDOA	Parallel Output/Input Data Bit 12/Serial Data Output A. When SER/$\overline{PAR}$ = 0, this pin acts as a three-state parallel digital input/output. Refer to the Parallel Interface section for further details. In serial mode, when SER/$\overline{PAR}$ = 1, this pin functions as SDOA and outputs serial conversion data.
58, 59, 60	DO/DI	DB13/OS0, DB14/OS1, DB15/OS2	Parallel Output/Input Data Bit 13, Data Bit 14, and Data Bit 15/Oversampling Ratio Selection. When SER/$\overline{PAR}$ = 0, these pins act as three-state parallel digital input/outputs. Refer to the Parallel Interface section for further details. In serial hardware mode, these pins control the oversampling settings. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. See the Digital Filter section for further details. In software serial mode, these pins must be connected to DGND.
61	DI	$\overline{WR}$/BURST	Write/Burst Mode Enable. In software parallel mode, this pin acts as $\overline{WR}$ for a parallel interface. In hardware parallel or serial mode, this pin enables BURST mode. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. Refer to the Burst Sequencer section for further information. In software serial mode, connect this pin to DGND.
62	DI	SCLK/$\overline{RD}$	Serial Clock Input/Parallel Data Read Control Input. In serial mode, this pin acts as the serial clock input for data transfers. The $\overline{CS}$ falling edge takes the SDOA and SDOB data output lines out of three-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the SDOA and SDOB serial data outputs. When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode, the output bus is enabled.
63	DI	$\overline{CS}$	Chip Select. This active low logic input frames the data transfer. In parallel mode, when both $\overline{CS}$ and $\overline{RD}$ are logic low, the DBx output bus is enabled and the conversion result is output on the parallel data bus lines. In serial mode, $\overline{CS}$ frames the serial read transfer and clocks out the MSB of the serial output data.

Pin No.	Type[1]	Mnemonic[2]	Description
64, 65, 66	DI	CHSEL0, CHSEL1, CHSEL2	Channel Selection Input 0 to Input 2. In hardware mode, these inputs select the input channels for the next conversion in Channel Group A and Channel Group B. For example, CHSELx = 0x000 selects V0A and V0B for the next conversion; CHSELx = 0x001 selects V1A and V1B for the next conversion. In software mode, these pins must be connected to DGND.
67	DO	BUSY	Busy Output. This pin transitions to a logic high after a CONVST rising edge and indicates that the conversion process has started. The BUSY output remains high until the conversion process for the current selected channels is complete. The falling edge of BUSY signals that the conversion data is being latched into the output data registers and is available to read. Data must be read after BUSY returns to low. Rising edges on CONVST have no effect while the BUSY signal is high.
68	DI	CONVST	Conversion Start Input for Channel Group A and Channel Group B. This logic input initiates conversions on the analog input channels. A conversion is initiated when CONVST transitions from low to high for the selected analog input pair. When burst mode and oversampling mode are disabled, every CONVST transition from low to high converts one channel pair. In sequencer mode, when burst mode or oversampling is enabled, a single CONVST transition from low to high is necessary to perform the required number of conversions.
69	CAP	REGGND	Internal Analog Regulator Ground. This pin must connect to the AGND plane of a system.
70	CAP	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Analog Regulator. Decouple this output pin separately to REGGND using a 10 µF capacitor. The voltage at this pin is 1.87 V typical.
73	AI	V0B	Analog Input for Channel 0, ADC B.
74	AI GND	V0BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V0B.
75	AI	V1B	Analog Input for Channel 1, ADC B.
76	AI GND	V1BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V1B.
77	AI	V2B	Analog Input for Channel 2, ADC B.
78	AI GND	V2BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V2B.
79	AI	V3B	Analog Input for Channel 3, ADC B.
80	AI GND	V3BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V3B.

[1] AI is analog input, GND is ground, P is power supply, REF is reference input/output, DI is digital input, DO is digital output, and CAP is decoupling capacitor pin.
[2] Note that throughout this data sheet, multifunction pins, such as SER/PAR, are referred to either by the entire pin name or by a single function of the pin, for example, SER, when only that function is relevant.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{REF} = 2.5 V internal, V_{CC} = 5 V, V_{DRIVE} = 3.3 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz T_A = 25°C, unless otherwise noted.

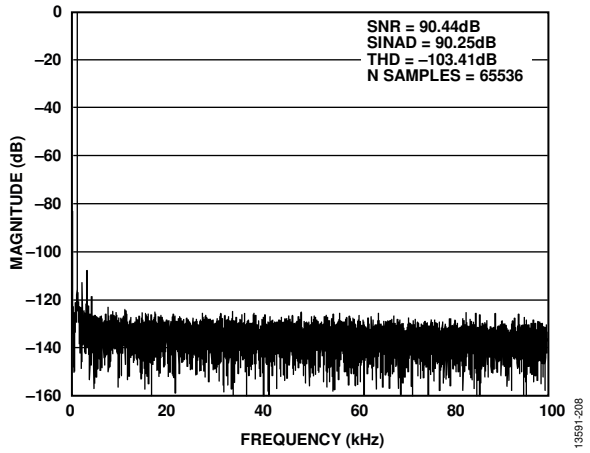


Figure 8. Fast Fourier Transform (FFT), ±10 V Range

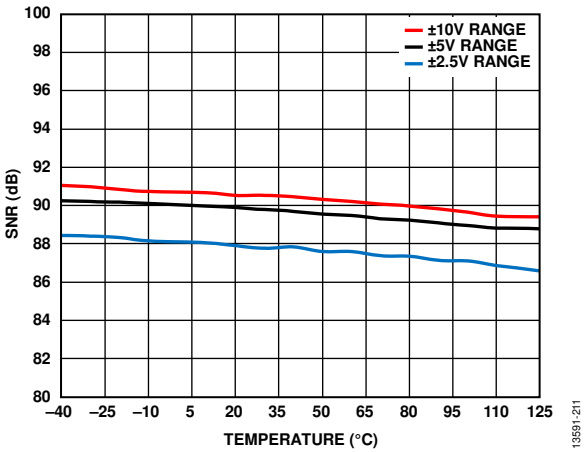


Figure 11. SNR vs. Temperature

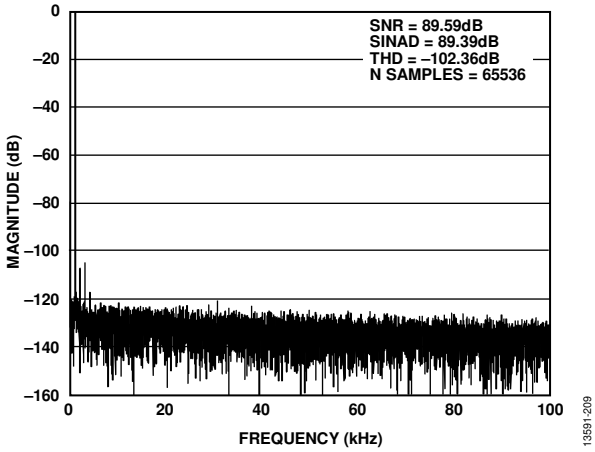


Figure 9. FFT, ±5 V Range

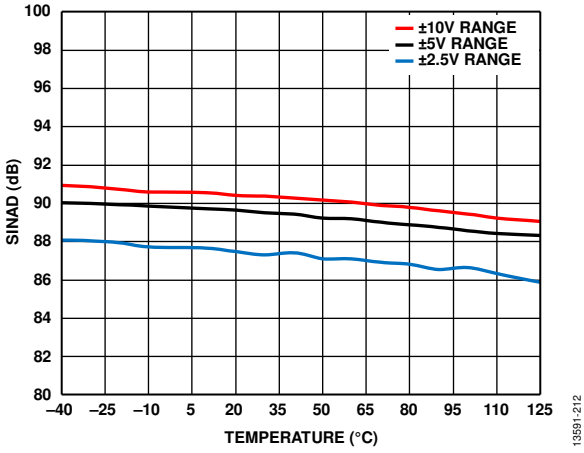


Figure 12. SINAD vs. Temperature

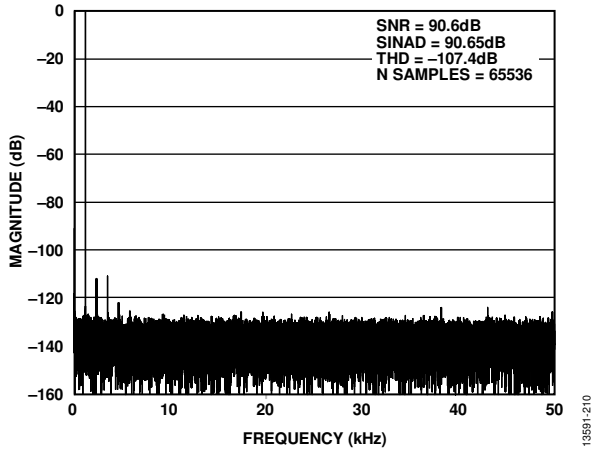


Figure 10. FFT Burst Mode, ±10 V Range

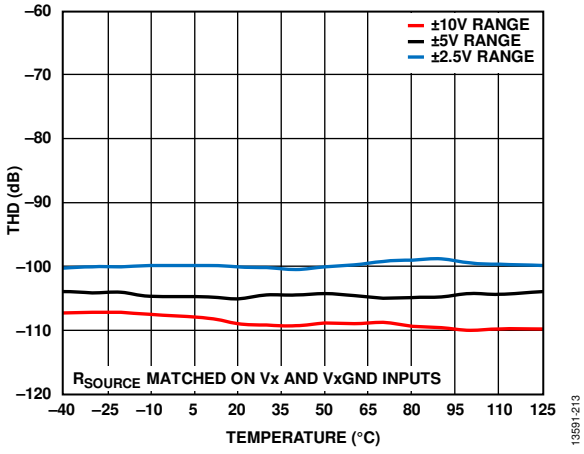


Figure 13. THD vs. Temperature

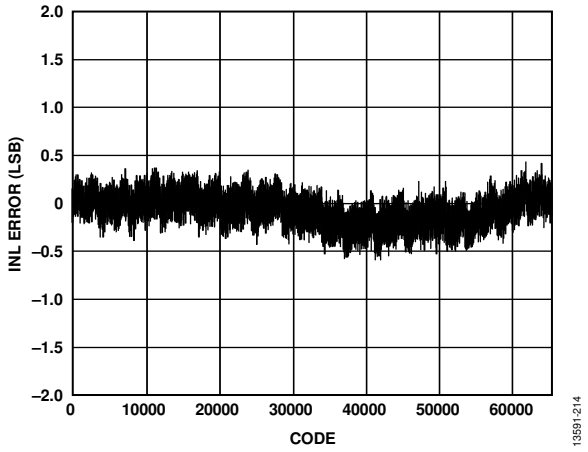


Figure 14. Typical INL Error, ±10 V Range

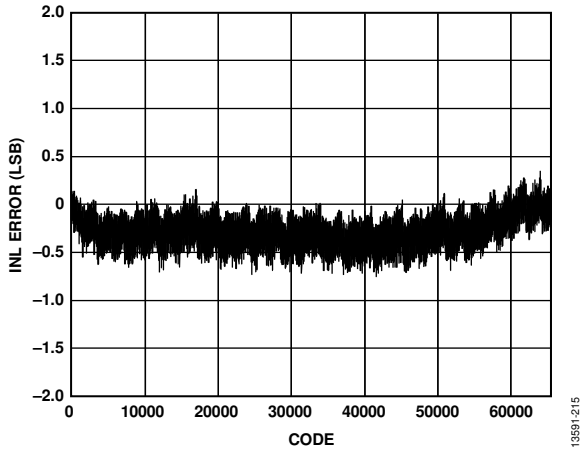


Figure 15. Typical INL Error, ±5 V Range

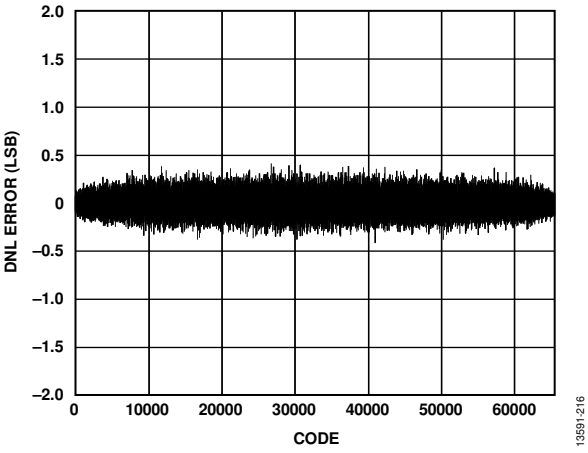


Figure 16. Typical DNL Error, ±10 V Range

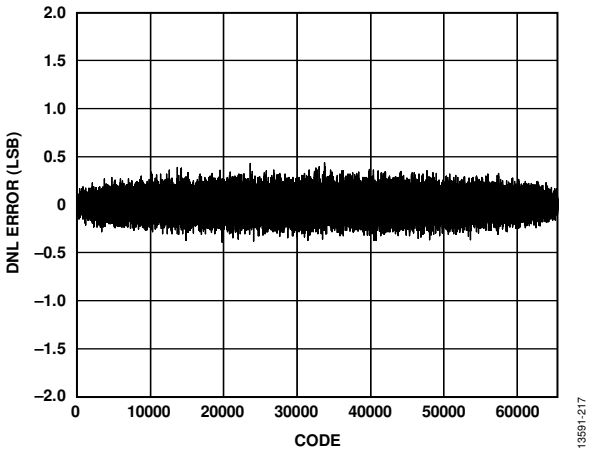


Figure 17. Typical DNL Error, ±5 V Range

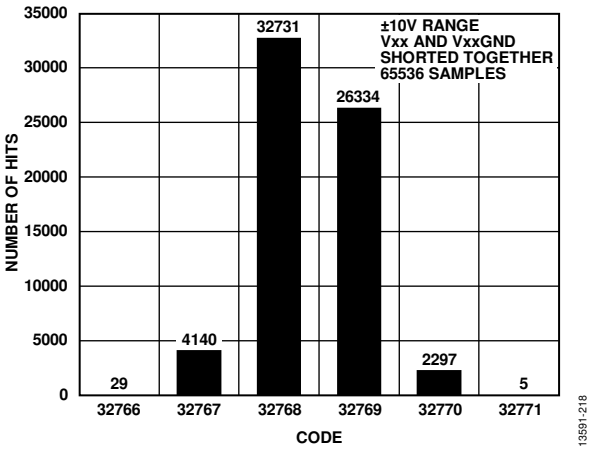


Figure 18. DC Histogram of Codes at Code Center, ±10 V Range

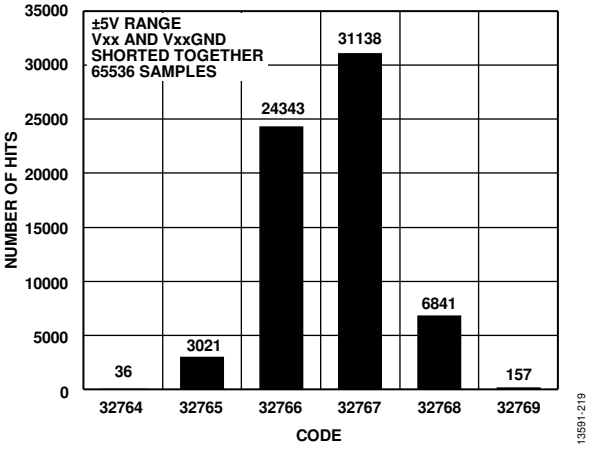


Figure 19. DC Histogram of Codes at Code Center, ±5 V Range

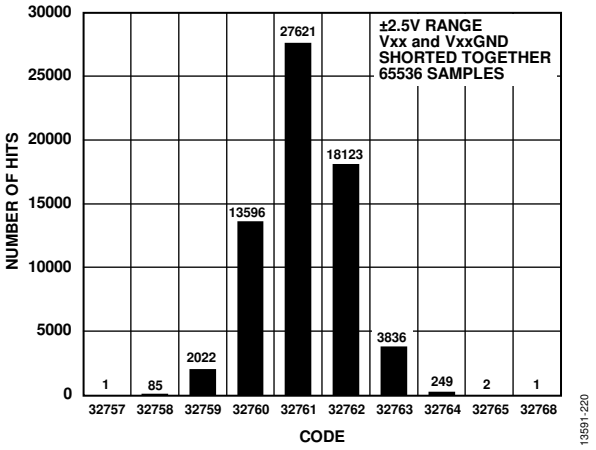


Figure 20. DC Histogram of Codes at Code Center, ±2.5 V Range

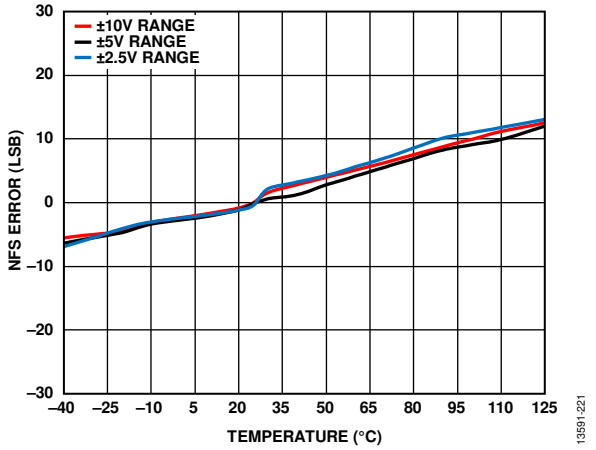


Figure 21. NFS Error vs. Temperature

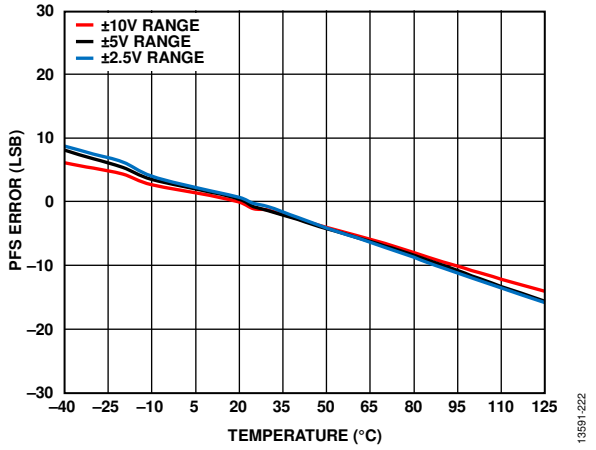


Figure 22. PFS Error vs. Temperature

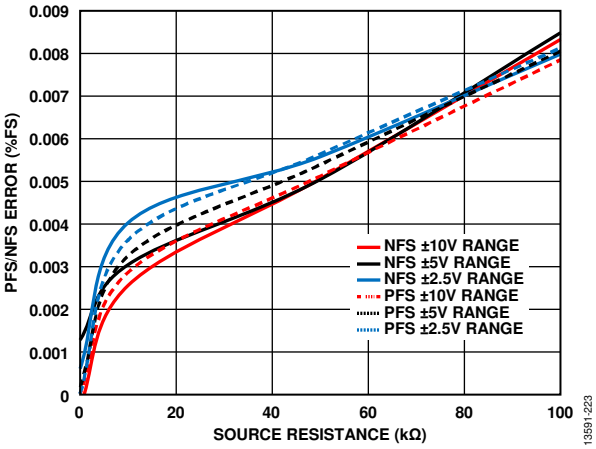


Figure 23. PFS/NFS Error vs. Source Resistance

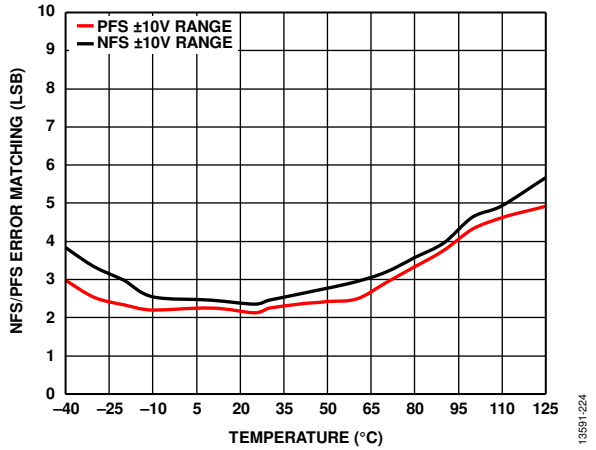


Figure 24. NFS/PFS Error Matching vs. Temperature

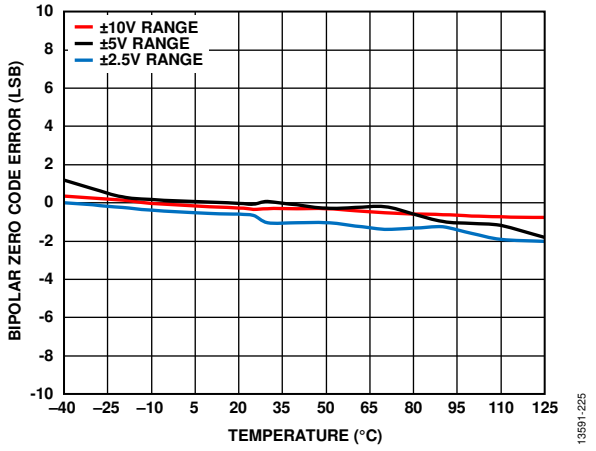


Figure 25. Bipolar Zero Code Error vs. Temperature

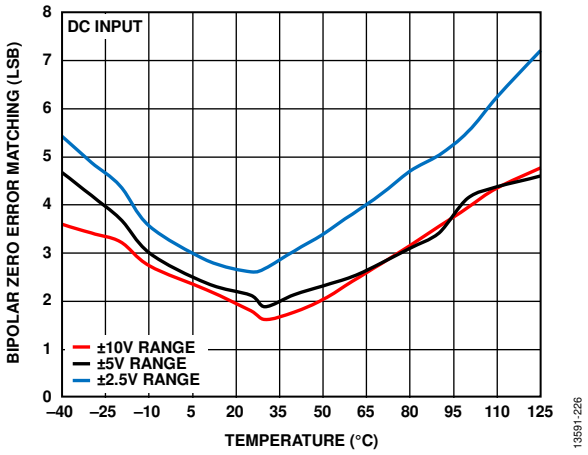


Figure 26. Bipolar Zero Error Matching vs. Temperature

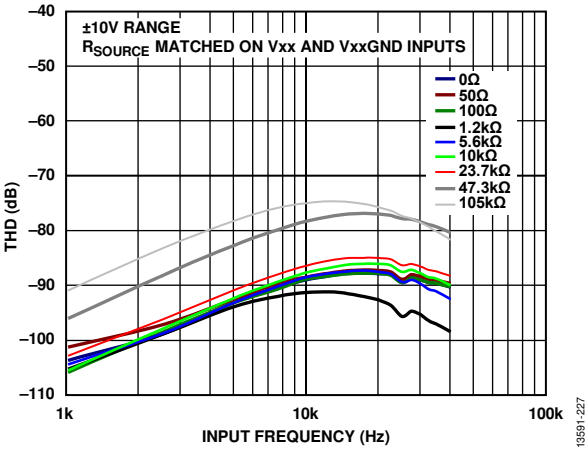


Figure 27. THD vs. Input Frequency for Various Source Impedances, ±10 V Range

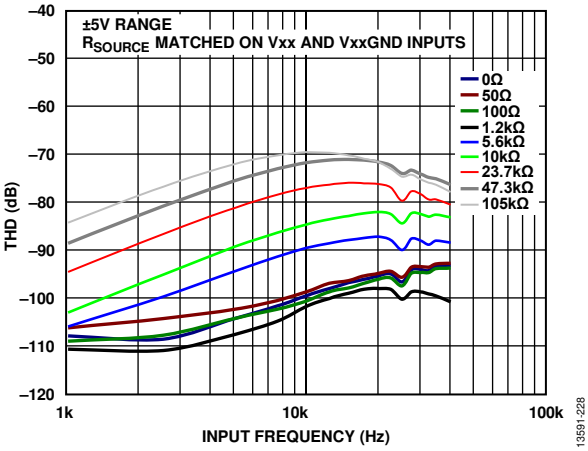


Figure 28. THD vs. Input Frequency for Various Source Impedances, ±5 V Range

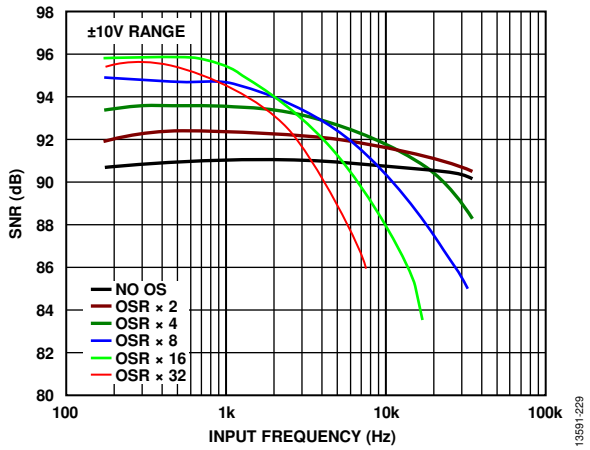


Figure 29. SNR vs. Input Frequency for Different Oversampling Rates, ±10 V Range

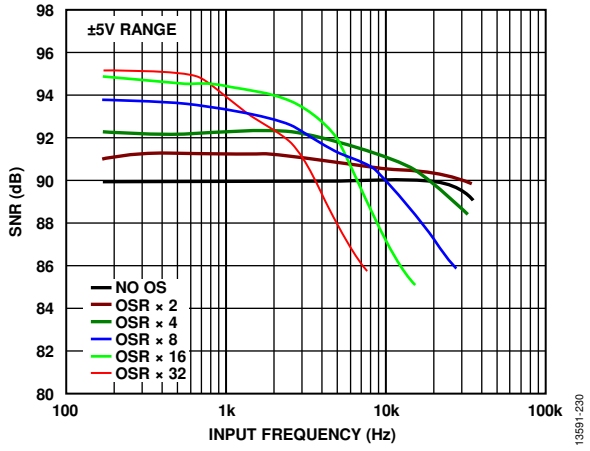


Figure 30. SNR vs. Input Frequency for Different Oversampling Rates, ±5 V Range

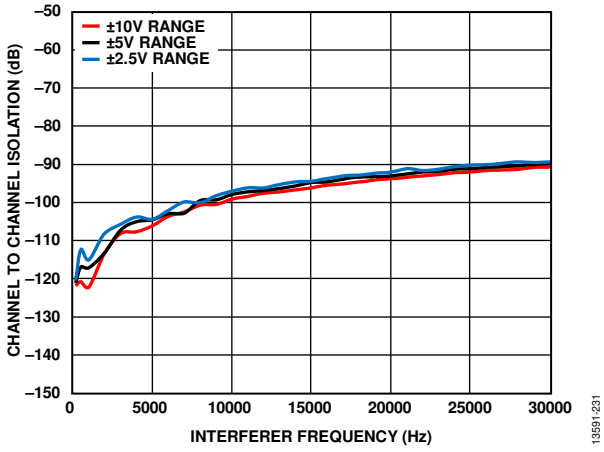


Figure 31. Channel to Channel Isolation

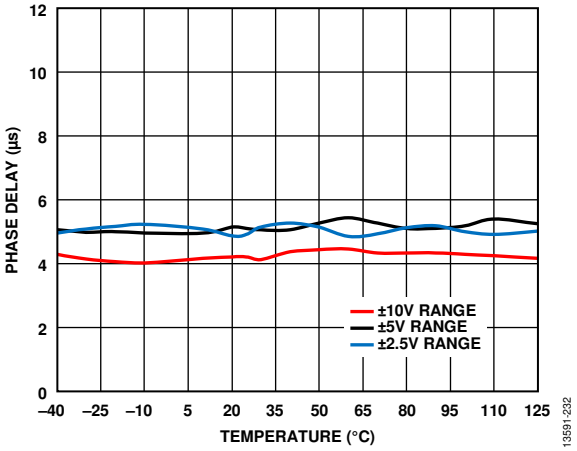


Figure 32. Phase Delay vs. Temperature

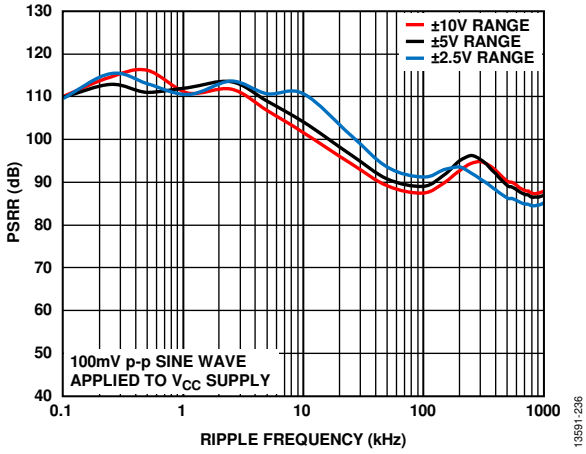


Figure 35. PSRR vs. Ripple Frequency

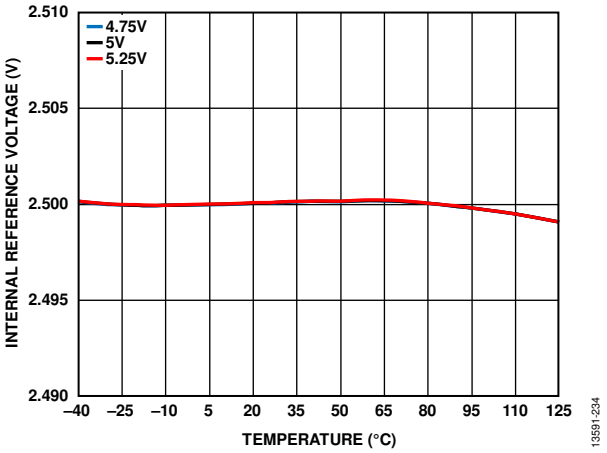


Figure 33. Internal Reference Voltage vs. Temperature for Various Supply Voltages

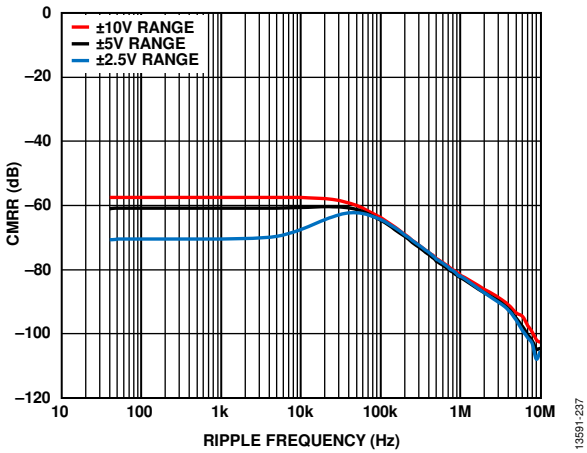


Figure 36. CMRR vs. Ripple Frequency

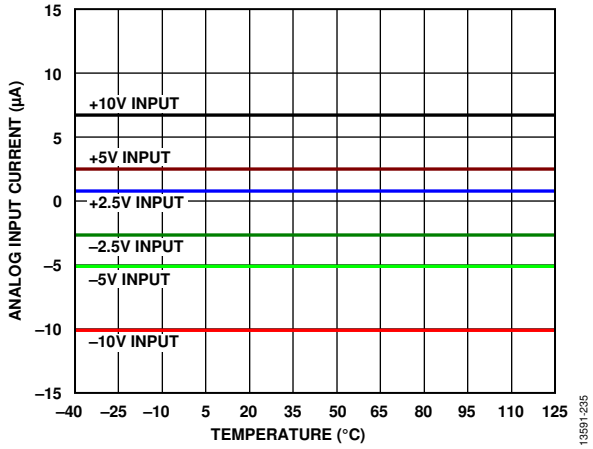


Figure 34. Analog Input Current vs. Temperature for Various Supply Voltages

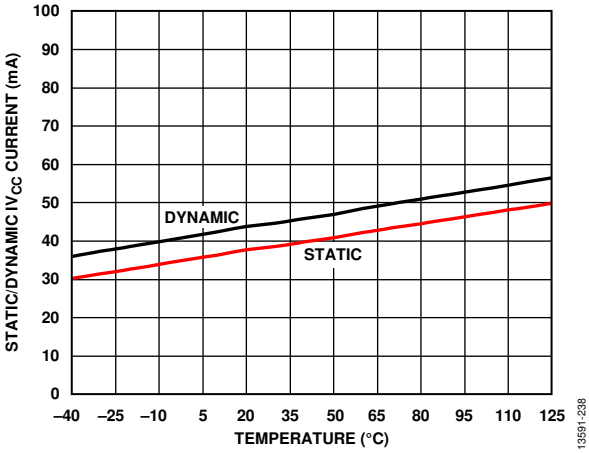


Figure 37. Static/Dynamic IV_{CC} Current vs. Temperature

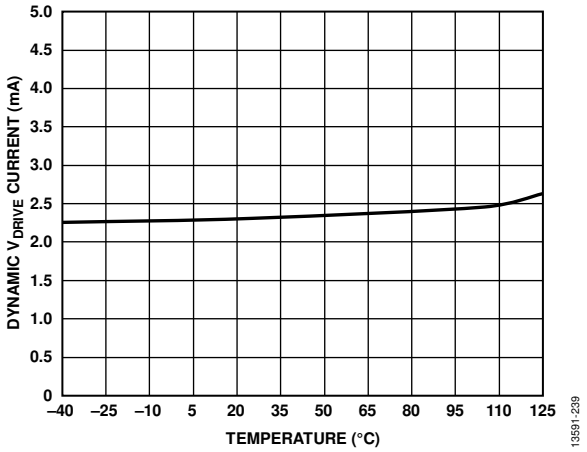


Figure 38. Dynamic V_{DRIVE} Current vs. Temperature

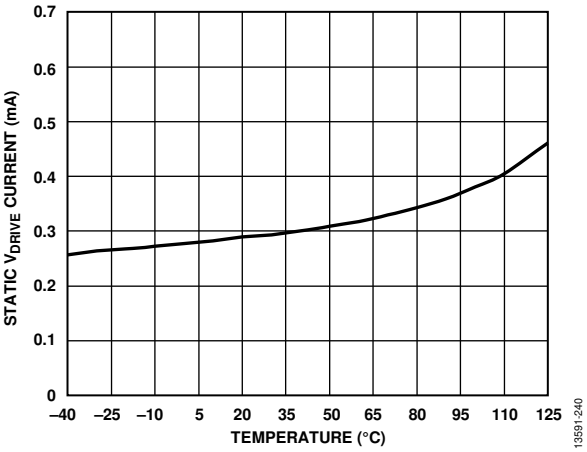


Figure 39. Static V_{DRIVE} Current vs. Temperature

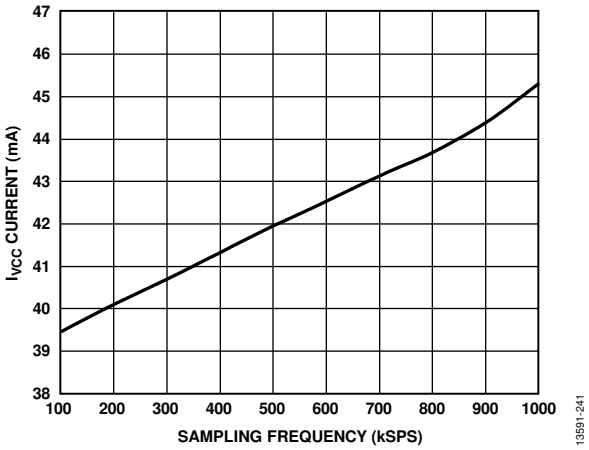


Figure 40. I_{VCC} Current vs. Sampling Frequency

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, at ½ LSB below the first code transition; and full scale, at ½ LSB above the last code transition.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Code Error
Bipolar zero code error is the deviation of the midscale transition (all 1s to all 0s) from the ideal, which is 0 V − ½ LSB.

Bipolar Zero Code Error Matching
Bipolar zero code error matching is the absolute difference in bipolar zero code error between any two input channels.

Positive Full-Scale (PFS) Error
Positive full-scale error is the deviation of the actual last code transition from the ideal last code transition (10 V − 1½ LSB (9.99954), 5 V − 1½ LSB (4.99977) and 2.5 V − 1½ LSB (2.49989)) after bipolar zero code error is adjusted out. The positive full-scale error includes the contribution from the internal reference buffer.

Positive Full-Scale Error Matching
Positive full-scale error matching is the absolute difference in positive full-scale error between any two input channels.

Negative Full-Scale (NFS) Error
Negative full-scale error is the deviation of the first code transition from the ideal first code transition (−10 V + ½ LSB (−9.99985), −5 V + ½ LSB (−4.99992) and −2.5 V + ½ LSB (−2.49996)) after the bipolar zero code error is adjusted out. The negative full-scale error includes the contribution from the internal reference buffer.

Negative Full-Scale Error Matching
Negative full-scale error matching is the absolute difference in negative full-scale error between any two input channels.

Signal-to-Noise-and-Distortion Ratio (SINAD)
SINAD is the measured ratio of signal to noise and distortion at the output of the ADC. The signal is the rms value of the sine wave, and noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), including harmonics, but excluding dc.

Signal-to-Noise Ratio (SNR)
SNR is the measured ratio of signal to noise at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc.

The ratio is dependent on the number of quantization levels in the digitization process: the greater the number of levels, the smaller the quantization noise. The theoretical SNR for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}Noise\ Ratio = (6.02N + 1.76)\ dB$$

Therefore, for a 16-bit converter, the SNR is 98 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels (dB).

Peak Harmonic or Spurious Noise
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is determined by a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at the sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3. Intermodulation distortion terms are those for which neither m nor n is equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels (dB).

Power Supply Rejection Ratio (PSRR)
Variations in power supply affect the full-scale transition but not the linearity of the converter. Power supply rejection is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value. The PSRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the V_{CC} supply of the ADC of frequency, f_S.

$$PSRR\ (dB) = 10\log(Pf/Pf_S)$$

where:
Pf is equal to the power at frequency, f, in the ADC output.
Pf_S is equal to the power at frequency, f_S, coupled onto the V_{CC} supply.

AC Common-Mode Rejection Ratio (AC CMRR)
AC CMRR is defined as the ratio of the power in the ADC output at frequency, f, to the power of a sine wave applied to the common-mode voltage of Vxx and VxxGND at frequency, f_S.

$$AC\ CMRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:
Pf is the power at frequency, f, in the ADC output.
Pf_S is the power at frequency, f_S, in the ADC output.

Channel to Channel Isolation
Channel to channel isolation is a measure of the level of crosstalk between all input channels. It is measured by applying a full-scale sine wave signal, up to 160 kHz, to all unselected input channels and then determining the degree to which the signal attenuates in the selected channel with a 1 kHz sine wave signal applied.

Phase Delay
Phase delay is a measure of the absolute time delay between when an input is sampled by the converter and when the result associated with that sample is available to be read back from the ADC, including delay induced by the analog front end of the device.

Phase Delay Drift
Phase delay drift is the change in group delay per unit temperature across the entire operating temperature of the device.

Phase Delay Matching
Phase delay matching is the maximum phase delay seen between any simultaneously sampled pair.

THEORY OF OPERATION

CONVERTER DETAILS

The AD7616 is a data acquisition system that employs a high speed, low power, charge redistribution, SAR analog-to-digital converter (ADC), and allows dual simultaneous sampling of 16 analog input channels. The analog inputs on the AD7616 can accept true bipolar input signals. Analog input range options include ±10 V, ±5 V, and ±2.5 V. The AD7616 operates from a single 5 V supply.

The AD7616 contains input clamp protection, input signal scaling amplifiers, a first-order antialiasing filter, an on-chip reference, a reference buffer, a dual high speed ADC, a digital filter, a flexible sequencer, and high speed parallel and serial interfaces.

The AD7616 can be operated in hardware or software mode by controlling the HW_RNGSELx pins. In hardware mode, the AD7616 is configured by pin control. In software mode, the AD7616 is configured by the control registers accessed via the serial or parallel interface.

ANALOG INPUT

Analog Input Channel Selection

The AD7616 contains dual, simultaneous sampling, 16-bit ADCs. Each ADC has eight analog input channels for a total of 16 analog inputs. Additionally, the AD7616 has on-chip diagnostic channels to monitor the V_{CC} supply and an on-chip adjustable low dropout regulator. Channels can be selected for conversion by control of the CHSELx pins in hardware mode or via the channel register control in software mode. Software mode is required to sample the diagnostic channels. Channels can be selected dynamically or the AD7616 has an on-chip sequencer to allow the channels for conversion to be preprogrammed. In hardware mode, simultaneous sampling is limited to the corresponding A and B channel, that is, Channel V0A is always sampled with Channel V0B. In software mode, it is possible to select any A channel with any B channel for simultaneous sampling.

Analog Input Ranges

The AD7616 can handle true bipolar, single-ended input voltages. The logic levels on the range select pins, HW_RNGSEL0 and HW_RNGSEL1, determine the analog input range of all analog input channels. If both range select pins are tied to a logic low, the analog input range is determined in software mode via the input range registers (see the Register Summary section for more details). In software mode, it is possible to configure an individual analog input range per channel.

Table 8. Analog Input Range Selection

Analog Input Range	HW_RNGSEL1	HW_RNGSEL0
Configured via the Input Range Registers	0	0
±2.5 V	0	1
±5 V	1	0
±10 V	1	1

In hardware mode, a logic change on these pins has an immediate effect on the analog input range; however, there is typically a settling time of approximately 120 µs in addition to the normal acquisition time requirement. The recommended practice is to hardwire the range select pins according to the desired input range for the system signals.

Analog Input Impedance

The analog input impedance of the AD7616 is 1 MΩ, a fixed input impedance that does not vary with the AD7616 sampling frequency. This high analog input impedance eliminates the need for a driver amplifier in front of the AD7616, allowing direct connection to the source or sensor.

Analog Input Clamp Protection

Figure 41 shows the analog input circuitry of the AD7616. Each analog input of the AD7616 contains clamp protection circuitry. Despite single 5 V supply operation, this analog input clamp protection allows an input overvoltage of between −20 V and +20 V.

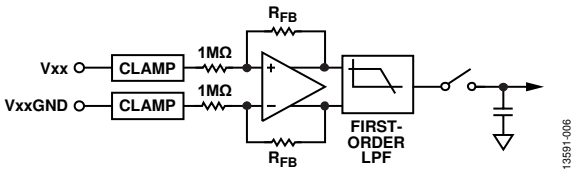


Figure 41. Analog Input Circuitry

Figure 42 shows the input clamp current vs. source voltage characteristic of the clamp circuit. For source voltages between −20 V and +20 V, no current flows in the clamp circuit. For input voltages that are greater than +20 V and less than −20 V, the AD7616 clamp circuitry turns on.

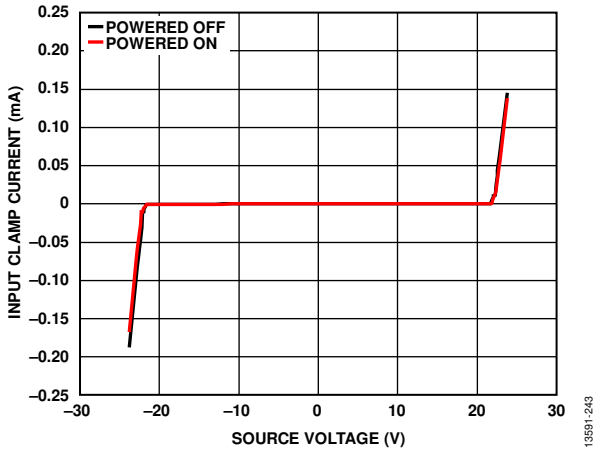


Figure 42. Input Protection Clamp Profile, Input Clamp Current vs. Source Voltage

Place a series resistor on the analog input channels to limit the current to ±10 mA for input voltages greater than +20 V and less than −20 V. In an application where there is a series resistance on an analog input channel, VxA or VxB, a corresponding resistance is required on the analog input ground channel, VxAGND or VxBGND (see Figure 43). If there is no correspond-

ing resistor on the VxAGND or VxBGND channel, an offset error occurs on that channel. Use the input overvoltage clamp protection circuitry to protect the AD7616 against transient overvoltage events. It is not recommended to leave the AD7616 in a condition where the clamp protection circuitry is active in normal or power-down conditions for extended periods.

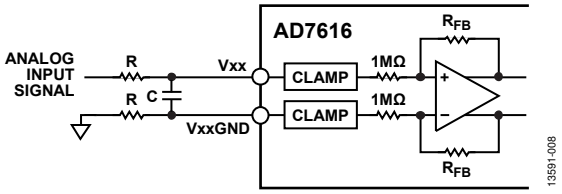


Figure 43. Input Resistance Matching on the Analog Input

Analog Input Antialiasing Filter

An analog antialiasing filter (a first-order Butterworth) is also provided on the AD7616. Figure 44 and Figure 45 show the frequency and phase response, respectively, of the analog antialiasing filter. The typical corner frequency in the ±10 V range is 39 kHz, and 33 kHz in the ±5 V range.

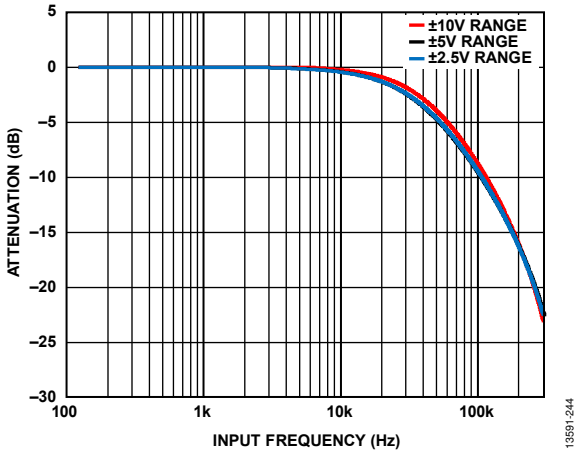


Figure 44. Analog Antialiasing Filter Frequency Response

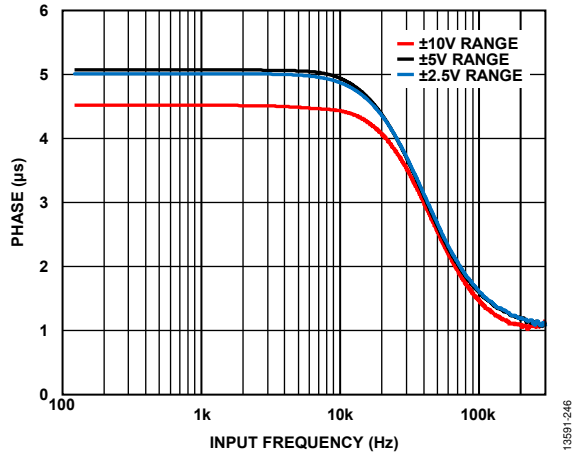
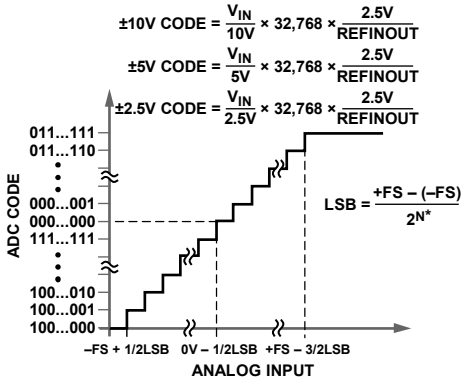


Figure 45. Analog Antialiasing Filter Phase Response

ADC TRANSFER FUNCTION

The output coding of the AD7616 is twos complement. The designed code transitions occur midway between successive integer LSB values, that is, 1/2 LSB and 3/2 LSB. The LSB size is full-scale range ÷ 65,536 for the AD7616. The ideal transfer characteristics for the AD7616 are shown in Figure 46. The LSB size is dependent on the analog input range selected.



	+FS	MIDSCALE	–FS	LSB
±10V RANGE	+10V	0V	–10V	305µV
±5V RANGE	+5V	0V	–5V	152µV
±2.5V RANGE	+2.5V	0V	–2.5V	76µV

*WHERE N IS THE NUMBER OF BITS OF THE CONVERTER

13591-009

Figure 46. Transfer Characteristics

INTERNAL/EXTERNAL REFERENCE

The AD7616 can operate with either an internal or external reference. The device contains an on-chip 2.5 V band gap reference. The REFINOUT pin allows access to the 2.5 V reference that generates the on-chip 4.096 V reference internally, or it allows an external reference of 2.5 V to be applied to the AD7616. An externally applied reference of 2.5 V is also amplified to 4.096 V using the internal buffer. This 4.096 V buffered reference is the reference used by the SAR ADC.

The REFSEL pin is a logic input pin that allows the user to select between the internal reference and an external reference. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFINOUT pin.

The internal reference buffer is always enabled. After a full reset, the AD7616 operates in the reference mode selected by the REFSEL pin. Decoupling is required on the REFINOUT pin for both the internal and external reference options. A 100 nF, X8R ceramic capacitor is required on the REFINOUT pin to REFINOUTGND.

The AD7616 contains a reference buffer configured to amplify the reference voltage to ~4.096 V. A 10 µF, X5R ceramic capacitor is required between REFCAP and REFGND. The reference voltage available at the REFINOUT pin is 2.5 V. When the AD7616 is configured in external reference mode, the REFINOUT pin is a high input impedance pin.