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16-Bit, 2 LSB INL, 3 MSPS PulSAR® ADC

AD7621

FEATURES

Throughput
- **3 MSPS (wideband warp and warp mode)**
- **2 MSPS (normal mode)**
- **1.25 MSPS (impulse mode)**

2.048 V internal reference
Differential input range: ±V_{REF} (V_{REF} up to 2.5 V)
INL: ±2 LSB maximum, ±1 LSB typical
16-bit resolution with no missing codes
SINAD: 89 dB typical @ 100 kHz
THD: −101 dB typical @ 100 kHz
No pipeline delay (SAR architecture)
Parallel (16- or 8-bit bus) and serial 5 V/3.3 V/2.5 V interface
SPI®-/QSPI™-/MICROWIRE™-/DSP-compatible
2.5 V single-supply operation
Power dissipation: 65 mW typical @ 3 MSPS
48-lead LQFP and 48-lead LFCSP_VQ packages
Speed upgrade of the AD7677

APPLICATIONS

Medical instruments
High speed data acquisition
Digital signal processing
Communications
Instrumentation
Spectrum analysis
ATE

FUNCTIONAL BLOCK DIAGRAM

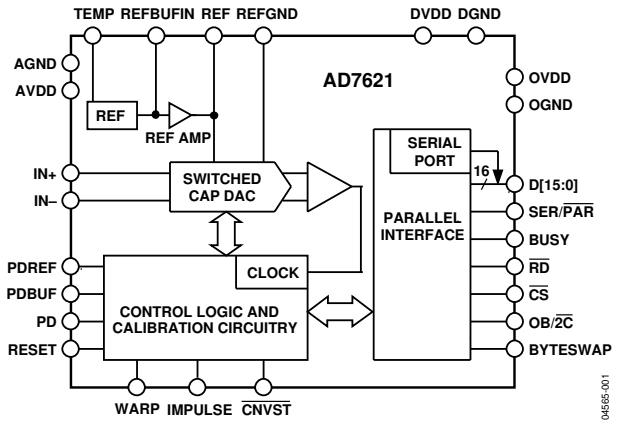

Figure 1.

Table 1. PulSAR Selection

Type/kSPS	100 to 250	500 to 570	800 to 1000	>1000
Pseudo Differential	AD7651 AD7660/61	AD7650/52 AD7664/66	AD7653 AD7667	
True Bipolar	AD7663	AD7665	AD7671	
True Differential	AD7675	AD7676	AD7677	AD7621
18-Bit	AD7678	AD7679	AD7674	AD7641
Multichannel/ Simultaneous		AD7654	AD7655	

GENERAL DESCRIPTION

The AD7621 is a 16-bit, 3 MSPS, charge redistribution SAR, fully differential analog-to-digital converter (ADC) that operates from a single 2.5 V power supply. It contains a high speed 16-bit sampling ADC, an internal conversion clock, an internal reference (and buffer), error correction circuits, and both serial and parallel system interface ports. It features two very high sampling rate modes (wideband warp and warp), a fast mode (normal) for asynchronous rate applications, and a reduced power mode (impulse) for low power applications where the power is scaled with the throughput. Operation is specified from −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Fast Throughput.
   The AD7621 is a 3 MSPS, charge redistribution, 16-bit SAR ADC.
2. Superior Linearity.
   The AD7621 has no missing 16-bit code.
3. Internal Reference.
   The AD7621 has a 2.048 V internal reference with a typical drift of ±7 ppm/°C.
4. Single-Supply Operation.
   The AD7621 operates from a 2.5 V single supply and typically dissipates 65 mW. In impulse mode, its power dissipation decreases with the throughput.
5. Serial or Parallel Interface.
   Versatile parallel (16- or 8-bit bus) or 2-wire serial interface arrangement compatible with 2.5 V, 3.3 V, or 5 V logic.

Rev. 0

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Fax: 781.461.3113

AD7621* PRODUCT PAGE QUICK LINKS

Last Content Update: 04/14/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7621 Evaluation Kit

DOCUMENTATION

Application Notes

- AN-931: Understanding PulSAR ADC Support Circuitry
- AN-932: Power Supply Sequencing

Data Sheet

- AD7621: 16-Bit, 2 LSB INL, 3 MSPS PulSAR™ ADC Data Sheet

Product Highlight

- 8- to 18-Bit SAR ADCs ... From the Leader in High Performance Analog

TOOLS AND SIMULATIONS

- AD7621 IBIS Models

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD7621 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7621 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

5/05 — Revision 0: Initial Version

SPECIFICATIONS

AVDD = DVDD = 2.5 V; OVDD = 2.3 V to 3.6 V; V_{REF} = 2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{IN}+ - V_{IN}-$	$-V_{REF}$		V_{REF}	V
Operating Input Voltage	$V_{IN}+, V_{IN}-$ to AGND	−0.1		AVDD[1]	V
Analog Input CMRR	f_{IN} = 100 kHz		55		dB
Input Current	3 MSPS throughput		25		μA
Input Impedance[2]					
THROUGHPUT SPEED					
Complete Cycle	Wideband warp, warp modes			333	ns
Throughput Rate	Wideband warp, warp modes	0.001		3	MSPS
Time Between Conversions	Wideband warp, warp modes			1	ms
Complete Cycle	Normal mode			500	ns
Throughput Rate	Normal mode	0		2	MSPS
Complete Cycle	Impulse mode			800	ns
Throughput Rate	Impulse mode	0		1.25	MSPS
DC ACCURACY	All modes				
Integral Linearity Error[3]	V_{REF} = 2.048 V, PDREF = high	−2	±1	+2	LSB[4]
No Missing Codes	V_{REF} = 2.048 V, PDREF = high	16			Bits
Differential Linearity Error	V_{REF} = 2.048 V, PDREF = high	−1		+2	LSB
Transition Noise	V_{REF} = 2.5 V		0.69		LSB
Transition Noise	V_{REF} = 2.048 V		0.82		LSB
Zero Error, T_{MIN} to T_{MAX}[5]		−30		+30	LSB
Zero Error Temperature Drift			±1		ppm/°C
Gain Error, T_{MIN} to T_{MAX}[5]		−0.38		+0.38	% of FSR
Gain Error Temperature Drift			±2		ppm/°C
Power Supply Sensitivity	AVDD = 2.5 V ± 5%		±3		LSB
AC ACCURACY					
Dynamic Range	f_{IN} = 20 kHz, V_{REF} = 2.5 V		90.5		dB[6]
Signal-to-Noise	f_{IN} = 20 kHz, V_{REF} = 2.5 V	88	90		dB
	f_{IN} = 20 kHz, V_{REF} = 2.048 V	86	88		dB
	f_{IN} = 100 kHz, V_{REF} = 2.5 V		89.2		dB
Spurious-Free Dynamic Range	f_{IN} = 20 kHz		103		dB
	f_{IN} = 100 kHz		101		dB
Total Harmonic Distortion	f_{IN} = 20 kHz		−102		dB
	f_{IN} = 100 kHz		−100		dB
Signal-to-(Noise + Distortion)	f_{IN} = 20 kHz, V_{REF} = 2.5 V	87.5	89.8		dB
	f_{IN} = 20 kHz, V_{REF} = 2.048 V		87.5		dB
	f_{IN} = 100 kHz, V_{REF} = 2.5 V		89		dB
−3 dB Input Bandwidth			50		MHz
SAMPLING DYNAMICS					
Aperture Delay			1		ns
Aperture Jitter			5		ps rms
Transient Response	Full-scale step			50	ns
INTERNAL REFERENCE	PDREF = PDBUF = low				
Output Voltage	REF @ 25°C	2.038	2.048	2.058	V
Temperature Drift	−40°C to +85°C		±7		ppm/°C
Line Regulation	AVDD = 2.5 V ± 5%		±15		ppm/V

Parameter	Conditions	Min	Typ	Max	Unit
Turn-On Settling Time	C_{REF} = 10 µF		5		ms
REFBUFIN Output Voltage	REFBUFIN @ 25°C		1.2		V
REFBUFIN Output Resistance			6.33		kΩ
EXTERNAL REFERENCE	PDREF = PDBUF = high				
Voltage Range	REF	1.8	2.048	AVDD	V
Current Drain	3 MSPS throughput		250		µA
REFERENCE BUFFER	PDREF = high, PDBUF = low				
REFBUFIN Input Voltage Range		1.05	1.2	1.30	V
TEMPERATURE PIN					
Voltage Output	@ 25°C		273		mV
Temperature Sensitivity			0.85		mV/°C
Output Resistance			4.7		kΩ
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.6	V
V_{IH}		1.7		5.25	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format[7]					
Pipeline Delay[8]					
V_{OL}	I_{SINK} = 500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	OVDD − 0.3			V
POWER SUPPLIES					
Specified Performance					
AVDD		2.37	2.5	2.63	V
DVDD		2.37	2.5	2.63	V
OVDD		2.30[9]		3.6	V
Operating Current[10]	3 MSPS throughput				
AVDD[11]	With internal reference		25.2		mA
DVDD			3.6		mA
OVDD			1		mA
Power Dissipation[11]					
With Internal Reference[10]	3 MSPS throughput		70	86	mW
Without Internal Reference[10]	3 MSPS throughput		65	80	mW
With Internal Reference [12]	1.25 MSPS throughput		42	55	mW
Without Internal Reference[12]	1.25 MSPS throughput		37	50	mW
In Power-Down Mode[13]	PD = high		600		µW
TEMPERATURE RANGE[14]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] When using an external reference. With the internal reference, the input range is −0.1 V to V_{REF}.
[2] See the Analog Inputs section.
[3] Linearity is tested using endpoints, not best fit. Tested with an external reference at 2.048 V.
[4] LSB means least significant bit. With the ±2.048 V input range, 1 LSB is 62.5 µV.
[5] See the Voltage Reference Input section. These specifications do not include the error contribution from the external reference.
[6] All specifications in dB are referred to a full-scale input FSR. Tested with an input signal at 0.5 dB below full-scale, unless otherwise specified.
[7] Parallel or serial 16-bit.
[8] Conversion results are available immediately after completed conversion.
[9] See the Absolute Maximum Ratings section.
[10] In warp mode. Tested in parallel reading mode.
[11] With internal reference, PDREF and PDBUF are low; without internal reference, PDREF and PDBUF are high.
[12] In impulse mode. Tested in parallel reading mode.
[13] With all digital inputs forced to OVDD.
[14] Consult factory for extended temperature range.

TIMING SPECIFICATIONS

AVDD = DVDD = 2.5 V; OVDD = 2.3 V to 3.6 V; V_{REF} = 2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
CONVERSION AND RESET (Refer to Figure 31 and Figure 32)					
Convert Pulse Width	t_1	15		70[1]	ns
Time Between Conversions (Warp[2] Mode/Normal Mode/Impulse Mode)[3]	t_2	333/500/800			ns
$\overline{CNVST}$ Low to BUSY High Delay	t_3			23	ns
BUSY High All Modes (Except Master Serial Read After Convert)	t_4			283/430/560	ns
Aperture Delay	t_5		1		ns
End of Conversion to BUSY Low Delay	t_6	10			ns
Conversion Time (Warp Mode/Normal Mode/Impulse Mode)	t_7			283/430/560	ns
Acquisition Time (Warp Mode/Normal Mode/Impulse Mode)	t_8	50/70/50			ns
RESET Pulse Width	t_9	15			ns
RESET Low to BUSY High Delay[4]	t_{38}		10		ns
BUSY High Time from RESET Low[4]	t_{39}		600		ns
PARALLEL INTERFACE MODES (Refer to Figure 33 and Figure 35)					
$\overline{CNVST}$ Low to DATA Valid Delay (Warp Mode/Normal Mode/Impulse Mode)	t_{10}			283/430/560	ns
DATA Valid to BUSY Low Delay	t_{11}	2			ns
Bus Access Request to DATA Valid	t_{12}			20	ns
Bus Relinquish Time	t_{13}	2		15	ns
MASTER SERIAL INTERFACE MODES[5] (Refer to Figure 37 and Figure 38)					
$\overline{CS}$ Low to SYNC Valid Delay	t_{14}			10	ns
$\overline{CS}$ Low to Internal SCLK Valid Delay[5]	t_{15}			10	ns
$\overline{CS}$ Low to SDOUT Delay	t_{16}			10	ns
$\overline{CNVST}$ Low to SYNC Delay (Warp Mode/Normal Mode/Impulse Mode)	t_{17}		12/137/263		ns
SYNC Asserted to SCLK First Edge Delay	t_{18}	0.5			ns
Internal SCLK Period[6]	t_{19}	8		12	ns
Internal SCLK High[6]	t_{20}	2			ns
Internal SCLK Low[6]	t_{21}	3			ns
SDOUT Valid Setup Time[6]	t_{22}	1			ns
SDOUT Valid Hold Time[6]	t_{23}	0			ns
SCLK Last Edge to SYNC Delay[6]	t_{24}	0			ns
$\overline{CS}$ High to SYNC HI-Z	t_{25}			10	ns
$\overline{CS}$ High to Internal SCLK HI-Z	t_{26}			10	ns
$\overline{CS}$ High to SDOUT HI-Z	t_{27}			10	ns
BUSY High in Master Serial Read after Convert[6]	t_{28}		See Table 4		
$\overline{CNVST}$ Low to SYNC Asserted Delay (All Modes)	t_{29}		275/400/500		ns
SYNC Deasserted to BUSY Low Delay	t_{30}		13		ns

Parameter	Symbol	Min	Typ	Max	Unit
SLAVE SERIAL INTERFACE MODES[5] (Refer to Figure 40 and Figure 41)					
External SCLK Setup Time	t_{31}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{32}	1		8	ns
SDIN Setup Time	t_{33}	5			ns
SDIN Hold Time	t_{34}	5			ns
External SCLK Period	t_{35}	12.5			ns
External SCLK High	t_{36}	5			ns
External SCLK Low	t_{37}	5			ns

[1] See the Conversion Control section.
[2] All timings for wideband warp mode are the same as warp mode.
[3] In warp mode only, the time between conversions is 1 ms; otherwise, there is no required maximum time.
[4] See the Digital Interface, and RESET sections.
[5] In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.
[6] In serial master read during convert mode. See Table 4 for serial master read after convert mode timing specifications.

SERIAL CLOCK TIMING SPECIFICATIONS

Table 4. Serial Clock Timings in Master Read After Convert Mode

DIVSCLK[1] DIVSCLK[0]	Symbol	0 0	0 1	1 0	1 1	Unit
SYNC to SCLK First Edge Delay Minimum	t_{18}	0.5	3	3	3	ns
Internal SCLK Period Minimum	t_{19}	8	16	32	64	ns
Internal SCLK Period Maximum	t_{19}	12	25	50	100	ns
Internal SCLK High Minimum	t_{20}	2	6	15	31	ns
Internal SCLK Low Minimum	t_{21}	3	7	16	32	ns
SDOUT Valid Setup Time Minimum	t_{22}	1	5	5	5	ns
SDOUT Valid Hold Time Minimum	t_{23}	0	0.5	10	28	ns
SCLK Last Edge to SYNC Delay Minimum	t_{24}	0	0.5	9	26	ns
BUSY High Width Maximum (Wideband and Warp Modes)	t_{28}	0.500	0.720	1.160	2.040	µs
BUSY High Width Maximum (Normal Mode)	t_{28}	0.650	0.870	1.310	2.190	µs
BUSY High Width Maximum (Impulse Mode)	t_{28}	0.780	1.000	1.440	2.320	µs

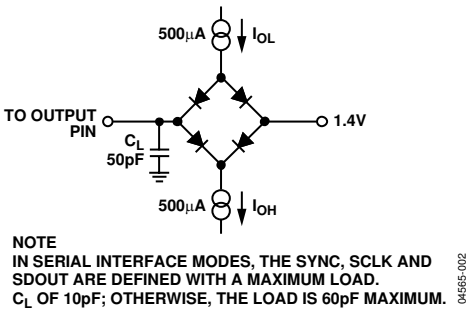


Figure 2. Load Circuit for Digital Interface Timing, SDOUT, SYNC, and SCLK Outputs, C_L = 10 pF

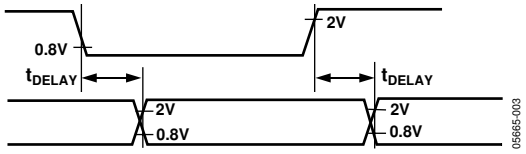


Figure 3. Voltage Reference Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs/Outputs	
IN+[1], IN−, REF, REFBUFIN, TEMP, INGND, REFGND to AGND	AVDD + 0.3 V to AGND − 0.3 V
Ground Voltage Differences	
AGND, DGND, OGND	±0.3 V
Supply Voltages	
AVDD, DVDD	−0.3 V to +2.7 V
OVDD	−0.3 V to +3.8 V
AVDD to DVDD	±2.8 V
AVDD to OVDD	+2.8 V to −3.8 V
OVDD to DVDD[2]	≤ +0.3 V if DVDD < 2.3 V
Digital Inputs	−0.3 V to +5.5 V
PDREF, PDBUF[3]	±20 mA
Internal Power Dissipation[4]	700 mW
Internal Power Dissipation[5]	2.5 W
Junction Temperature	125°C
Storage Temperature Range	−65°C to +125°C

[1] See the Analog Inputs section.
[2] See the Power Supply section.
[3] See the Voltage Reference Input section.
[4] Specification is for the device in free air: 48-Lead LQFP; θ_{JA} = 91°C/W, θ_{JC} = 30°C/W.
[5] Specification is for the device in free air: 48-Lead LFCSP; θ_{JA} = 26°C/W.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

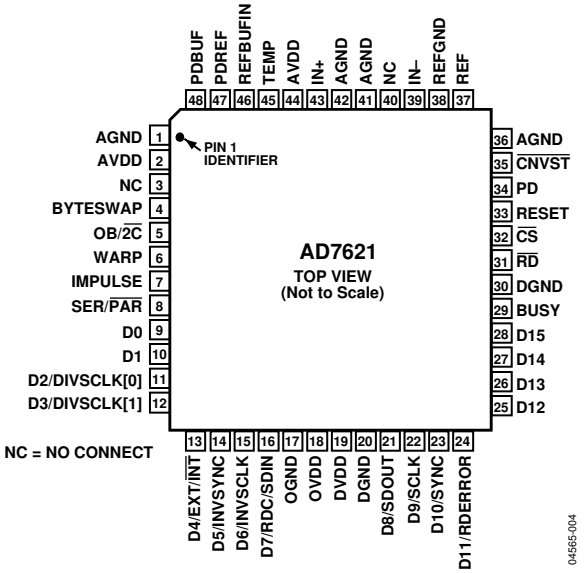


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 41, 42	AGND	P	Analog Power Ground Pin.
2, 44	AVDD	P	Input Analog Power Pins. Nominally 2.5 V.
3, 40	NC		No Connect.
4	BYTESWAP	DI	Parallel Mode Selection (8-Bit/16-Bit). When high, the LSB is output on D[15:8] and the MSB is output on D[7:0]; when low, the LSB is output on D[7:0] and the MSB is output on D[15:8].
5	OB/$\overline{2C}$	DI	Straight Binary/Binary Twos Complement Output. When high, the digital output is straight binary; when low, the MSB is inverted resulting in a twos complement output from its internal shift register.
6	WARP	DI	Conversion Mode Selection. When WARP = high and IMPULSE = high, this selects wideband mode with slightly improved linearity and THD. When WARP = high and IMPULSE = low, this selects warp mode. In either mode, these are the fastest modes; maximum throughput is achievable, and a minimum conversion rate must be applied in order to guarantee full specified accuracy. When WARP = low and IMPULSE = low, this input selects normal mode where full accuracy is maintained independent of the minimum conversion rate.
7	IMPULSE	DI	Conversion Mode Selection. When IMPULSE = high and WARP = low, this input selects impulse mode, a reduced power mode. In this mode, the power dissipation is approximately proportional to the sampling rate.
8	SER/$\overline{PAR}$	DI	Serial/Parallel Selection Input. When high, the serial interface is selected and some bits of the data bus are used as a serial port; the remaining data bits are high impedance outputs. When SER/$\overline{PAR}$ = low, the parallel port is selected.
9, 10	D[0:1]	DO	Bit 0 and Bit 1 of the Parallel Port Data Output Bus.
11, 12	D[2:3] or DIVSCLK[0:1]	DI/O	When SER/$\overline{PAR}$ = low, these outputs are used as Bit 2 and Bit 3 of the parallel port data output bus. When SER/$\overline{PAR}$ = high, serial clock division selection. When using serial master read after convert mode (EXT/$\overline{INT}$ = low, RDC/SDIN = low) these inputs can be used to slow down the internally generated serial clock that clocks the data output. In other serial modes, these pins are high impedance outputs.
13	D4 or EXT/$\overline{INT}$	DI/O	When SER/$\overline{PAR}$ = low, this output is used as Bit 4 of the parallel port data output bus. When SER/$\overline{PAR}$ = high, serial clock source select. This input is used to select the internally generated (master) or external (slave) serial data clock. When EXT/$\overline{INT}$ = low: master mode. The internal serial clock is selected on SCLK output. When EXT/$\overline{INT}$ = high: slave mode. The output data is synchronized to an external clock signal, gated by $\overline{CS}$, connected to the SCLK input.

Pin No.	Mnemonic	Type[1]	Description
14	D5	DI/O	When SER/$\overline{PAR}$ = low this output is used as Bit 5 of the parallel port data output bus.
	or INVSYNC		When SER/$\overline{PAR}$ = high, invert sync select. In serial master mode (EXT/$\overline{INT}$ = low), this input is used to select the active state of the SYNC signal. When INVSYNC = low, SYNC is active high. When INVSYNC = high, SYNC is active low.
15	D6	DI/O	When SER/$\overline{PAR}$ = low this output is used as Bit 6 of the parallel port data output bus.
	or INVSCLK		Invert SCLK Select. In all serial modes, this input is used to invert the SCLK signal.
16	D7	DI/O	Bit 7 of the Parallel Port Data Output Bus.
	or RDC		When SER/$\overline{PAR}$ = high, read during convert. When using Serial Master mode (EXT/$\overline{INT}$ = low), RDC is used to select the read mode. When RDC = high, the previous conversion result is read during current conversion and the period of SCLK changes (see the Master Serial Interface section). When RDC = low (read after convert), the current result is read after conversion.
	or SDIN		Serial Data In. When using serial slave mode, (EXT/$\overline{INT}$ = high), SDIN could be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 16 SCLK periods after the initiation of the read sequence.
17	OGND	P	Input/Output Interface Digital Power Ground.
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply as the supply of the host interface (2.5 V or 3 V).
19	DVDD	P	Digital Power. Nominally at 2.5 V.
20	DGND	P	Digital Power Ground.
21	D8	DO	When SER/$\overline{PAR}$ = low this output is used as Bit 8 of the parallel port data output bus.
	or SDOUT		When SER/$\overline{PAR}$ = high, serial data output. In serial mode, this pin is used as the serial data output synchronized to SCLK. Conversion results are stored in an on-chip register. The AD7621 provides the conversion result, MSB first, from its internal shift register. The data format is determined by the logic level of OB/$\overline{2C}$. In master mode (EXT/$\overline{INT}$ = low). SDOUT is valid on both edges of SCLK. In slave mode (EXT/$\overline{INT}$ = high): When INVSCLK = low, SDOUT is updated on SCLK rising edge and valid on the next falling edge. When INVSCLK = high, SDOUT is updated on SCLK falling edge and valid on the next rising edge.
22	D9	DI/O	Parallel Port Data Output Bus Bit 9. When SER/$\overline{PAR}$ = low, this output is used as Bit 9 of the parallel port data output bus.
	or SCLK		Serial Clock. When SER/$\overline{PAR}$ = high, serial clock. In all serial modes, this pin is used as the serial data clock input or output, dependent upon the logic state of the EXT/$\overline{INT}$ pin. The active edge where the data SDOUT is updated depends upon the logic state of the INVSCLK pin.
23	D10	DO	When SER/$\overline{PAR}$ = low, this output is used as Bit 10 of the parallel port data output bus.
	or SYNC		When SER/$\overline{PAR}$ = high, frame synchronization. In serial master mode (EXT/$\overline{INT}$= low), this output is used as a digital output frame synchronization for use with the internal data clock. When a read sequence is initiated and INVSYNC = low, SYNC is driven high and remains high while SDOUT output is valid. When a read sequence is initiated and INVSYNC = high, SYNC is driven low and remains low while SDOUT output is valid.
24	D11	DO	Parallel Port Data Output Bus Bit 11. When SER/$\overline{PAR}$ = low, this output is used as Bit 11 of the parallel port data output bus.
	or RDERROR		Read Error. When SER/$\overline{PAR}$ = high, read error. In serial slave mode (EXT/$\overline{INT}$ = high), this output is used as an incomplete read error flag. If a data read is started and not completed when the current conversion is complete, the current data is lost and RDERROR is pulsed high.
25 to 28	D[12:15]	DO	Bit 12 to Bit 15 of the Parallel Port Data Output Bus.
29	BUSY	DO	Busy Output. Transitions high when a conversion is started, and remains high until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY can be used as a data ready clock signal.
30	DGND	P	Digital Power Ground.
31	$\overline{RD}$	DI	Read Data. When $\overline{CS}$ and $\overline{RD}$ are both low, the interface parallel or serial output bus is enabled.

Pin No.	Mnemonic	Type[1]	Description
32	$\overline{CS}$	DI	Chip Select. When $\overline{CS}$ and $\overline{RD}$ are both low, the interface parallel or serial output bus is enabled. $\overline{CS}$ is also used to gate the external clock in slave serial mode.
33	RESET	DI	Reset Input. When high, reset the AD7621. Current conversion if any is aborted. Falling edge of RESET enables the calibration mode indicated by pulsing BUSY high. Refer to the Digital Interface section. If not used, this pin can be tied to DGND.
34	PD	DI	Power-Down Input. When high, power down the ADC. Power consumption is reduced and conversions are inhibited after the current one is completed.
35	$\overline{CNVST}$	DI	Conversion Start. A falling edge on $\overline{CNVST}$ puts the internal sample-and-hold into the hold state and initiates a conversion.
36	AGND	P	Analog Power Ground Pin.
37	REF	AI/O	Reference Output/Input. When PDREF/PDBUF = low, the internal reference and buffer are enabled producing 2.048 V on this pin. When PDREF/PDBUF = high, the internal reference and buffer are disabled allowing an externally supplied voltage reference up to AVDD volts. Decoupling is required with or without the internal reference and buffer. Refer to the Voltage Reference Input section.
38	REFGND	AI	Reference Input Analog Ground.
39	IN–	AI	Differential Negative Analog Input.
43	IN+	AI	Differential Positive Analog Input.
45	TEMP	AO	Temperature Sensor Analog Output.
46	REFBUFIN	AI/O	Internal Reference Output/Reference Buffer Input. When PDREF/PDBUF = low, the internal reference and buffer are enabled producing the 1.2 V (typical) bandgap output on this pin, which needs external decoupling. The internal fixed gain reference buffer uses this to produce 2.048V on the REF pin. When using an external reference with the internal reference buffer (PDBUF = low, PDREF = high), applying 1.2 V on this pin produces 2.048 V on the REF pin. Refer to the Voltage Reference Input section.
47	PDREF	DI	Internal Reference Power-Down Input. When low, the internal reference is enabled. When high, the internal reference is powered down and an external reference must been used.
48	PDBUF	DI	Internal Reference Buffer Power-Down Input. When low, the buffer is enabled (must be low when using internal reference). When high, the buffer is powered-down.

[1] AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital input; DI/O = bidirectional digital; DO = digital output; P = power.

TERMINOLOGY

Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from negative full-scale through positive full-scale. The point used as negative full-scale occurs ½ LSB before the first code transition. Positive full-scale is defined as a level 1½ LSBs beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Gain Error
The first transition (from 000…00 to 000…01) should occur for an analog voltage ½ LSB above the nominal negative full-scale (−2.0479688 V for the ±2.048 V range). The last transition (from 111…10 to 111…11) should occur for an analog voltage 1½ LSBs below the nominal full-scale (2.0479531 V for the ±2.048 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Zero Error
The zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Dynamic Range
Dynamic range is the ratio of the rms value of the full-scale to the rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD and is expressed in bits by

$$ENOB = [(SINAD_{dB} - 1.76)/6.02]$$

Aperture Delay
Aperture delay is a measure of the acquisition performance measured from the falling edge of the $\overline{CNVST}$ input to when the input signal is held for a conversion.

Transient Response
The time required for the AD7621 to achieve its rated accuracy after a full-scale step function is applied to its input.

Reference Voltage Temperature Coefficient
Reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN}, T(25°C), and T_{MAX}. It is expressed in ppm/°C as

$$TCV_{REF}(\text{ppm/°C}) = \frac{V_{REF}(Max) - V_{REF}(Min)}{V_{REF}(25°C) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:
$V_{REF}(Max)$ = maximum V_{REF} at T_{MIN}, T (25°C), or T_{MAX}
$V_{REF}(Min)$ = minimum V_{REF} at T_{MIN}, T (25°C), or T_{MAX}
$V_{REF}(25°C)$ = V_{REF} at 25°C
T_{MAX} = +85°C
T_{MIN} = −40°C

TYPICAL PERFORMANCE CHARACTERISTICS

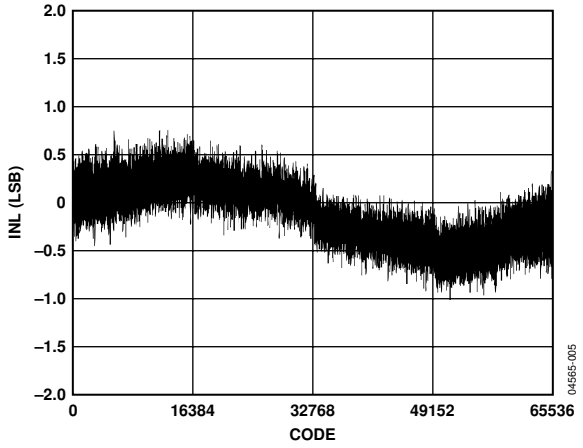


Figure 5. Integral Nonlinearity vs. Code

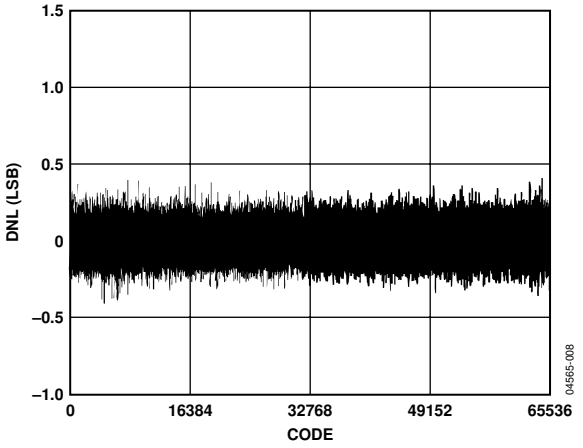


Figure 8. Differential Nonlinearity vs. Code

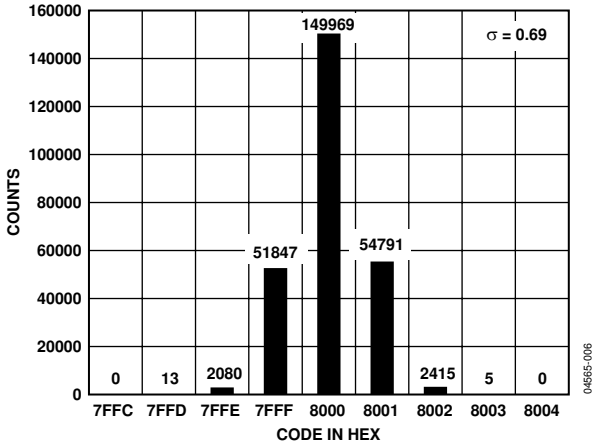


Figure 6. Histogram of 261,120 Conversions of a DC Input at the Code Center (External Reference)

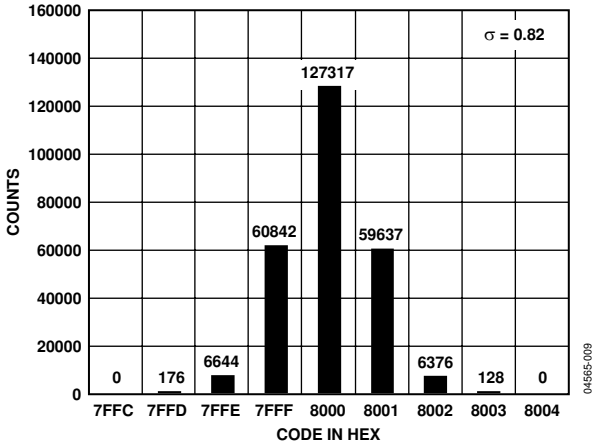


Figure 9. Histogram of 261,120 Conversions of a DC Input at the Code Center (Internal Reference)

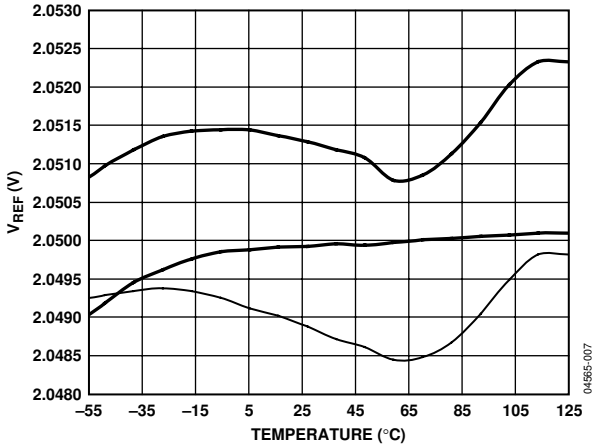


Figure 7. Typical Reference Voltage Output vs. Temperature (3 Units)

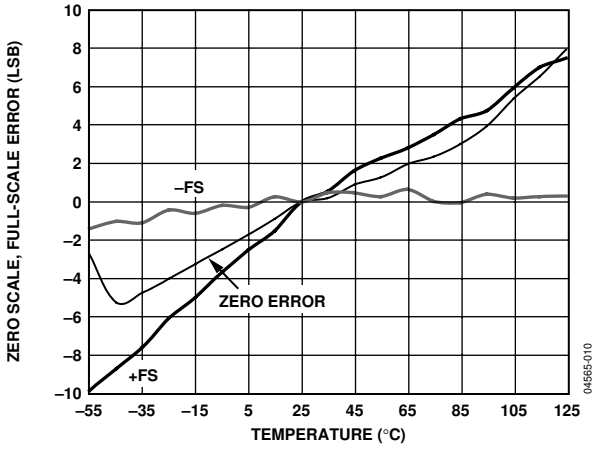


Figure 10. Zero Error, Positive and Negative Full Scale vs. Temperature

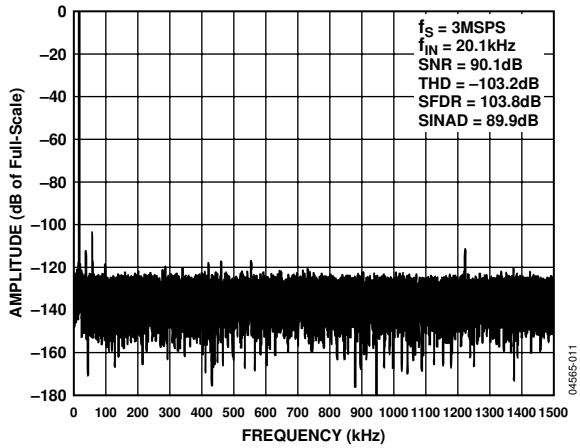


Figure 11. FFT 20 kHz

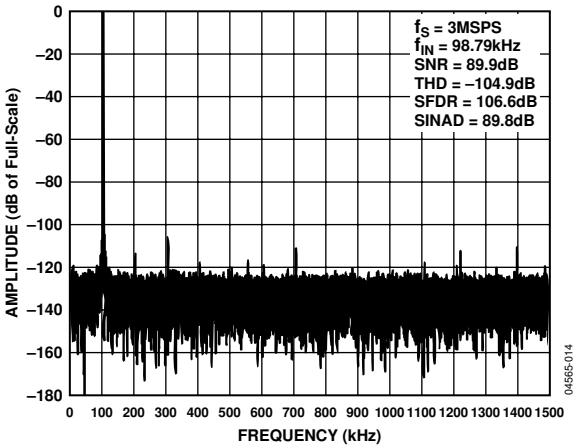


Figure 14. FFT 100 kHz

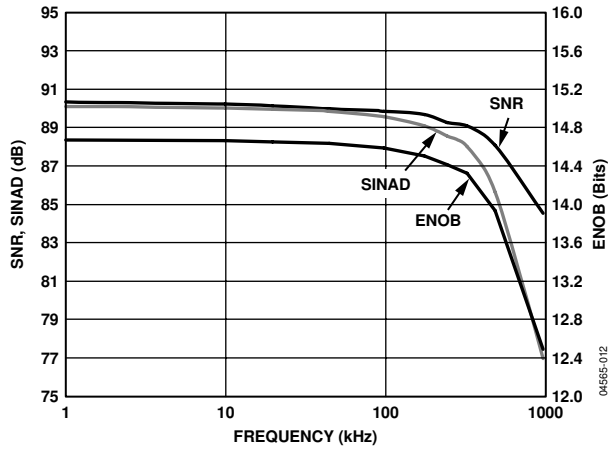


Figure 12. SNR, SINAD and ENOB vs. Frequency

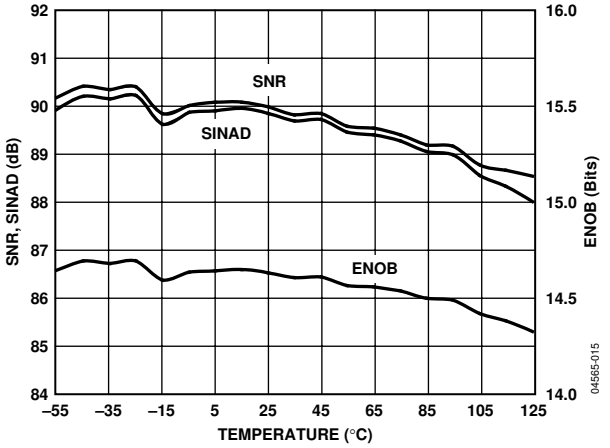


Figure 15. SNR, SINAD, and ENOB vs. Temperature

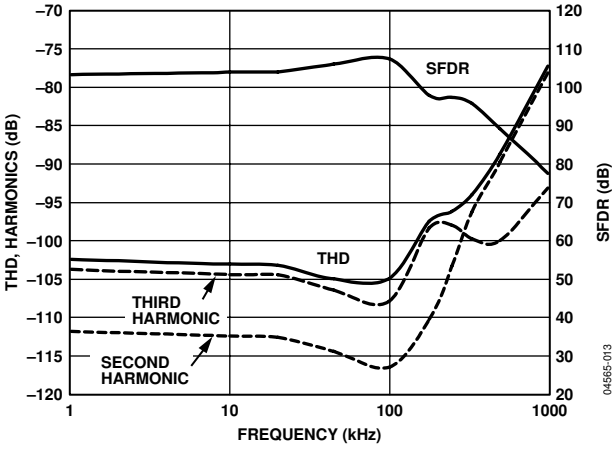


Figure 13. THD, Harmonics, and SFDR vs. Frequency

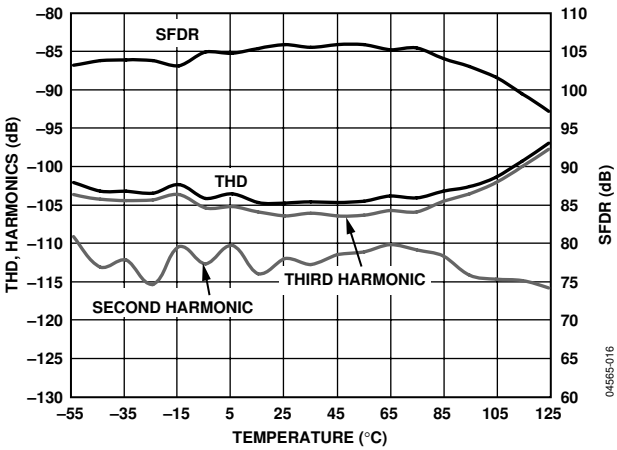


Figure 16. THD, Harmonics, and SFDR vs. Temperature

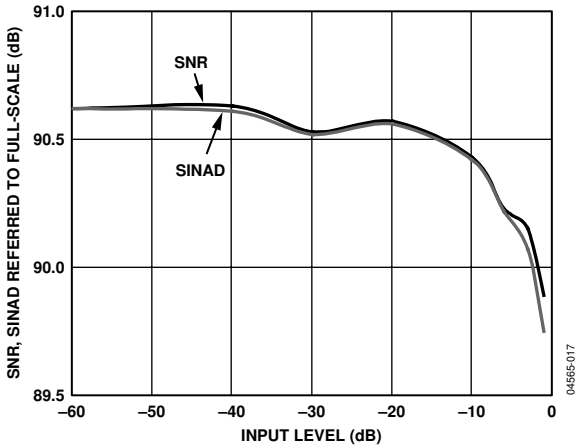


Figure 17. SNR and SINAD vs. Input Level (Referred to Full Scale)

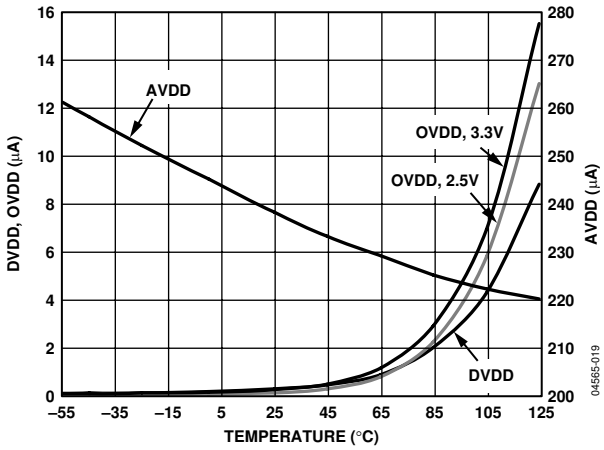


Figure 18. Power-Down Operating Currents vs. Temperature

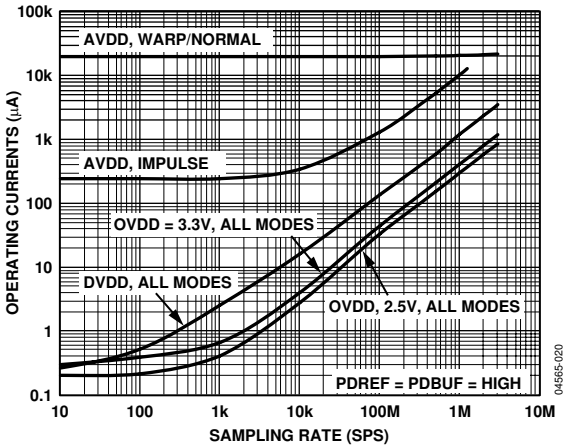


Figure 19. Operating Current vs. Sample Rate

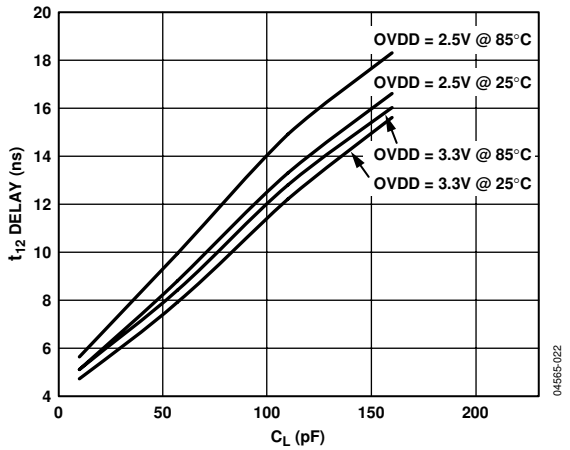


Figure 20. Typical Delay vs. Load Capacitance C_L

THEORY OF OPERATION

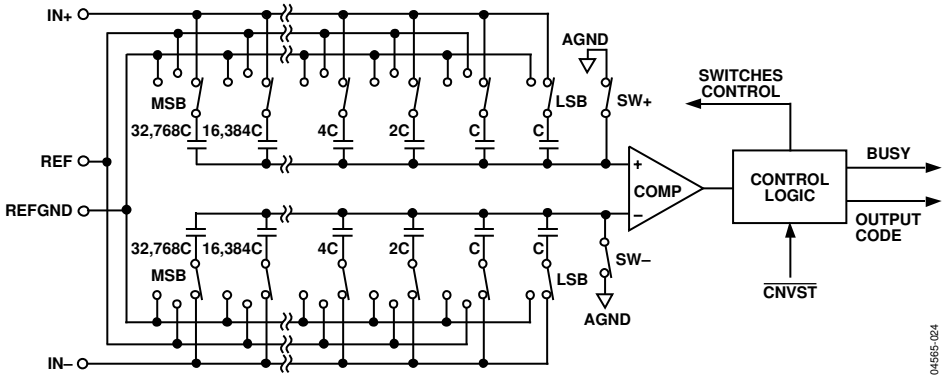


Figure 21. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7621 is a very fast, low power, single-supply, precise, 16-bit analog-to-digital converter (ADC) using successive approximation architecture. The AD7621 features different modes to optimize performances according to the applications. In warp mode, the AD7621 is capable of converting 3,000,000 samples per second (3 MSPS).

The AD7621 provides the user with an on-chip track-and-hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The AD7621 can be operated from a single 2.5 V supply and be interfaced to either 5 V, 3.3 V, or 2.5 V digital logic. It is housed in 48-lead LQFP or tiny LFCSP packages that combine space savings with flexibility, allowing the AD7621 to be configured as either a serial or parallel interface. The AD7621 is pin-to-pin-compatible with, and a speed upgrade of, the AD7677.

CONVERTER OPERATION

The AD7621 is a successive approximation analog-to-digital converter (ADC) based on a charge redistribution DAC. Figure 21 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to AGND via SW+ and SW−. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on IN+ and IN− inputs. A conversion phase is initiated once the acquisition phase is complete and the $\overline{\text{CNVST}}$ input goes low. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the REFGND input. Therefore, the differential voltage between the inputs (IN+ and IN−) captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFGND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ through $V_{REF}/65536$). The control logic toggles these switches, starting with the MSB first, in order to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and brings BUSY output low.

MODES OF OPERATION

The AD7621 features four modes of operation: wideband warp, warp, normal, and impulse. Each of these modes is more suitable to specific applications.

Wideband warp (WARP = high, IMPULSE = high) and warp (WARP = high, IMPULSE = low) modes allow the fastest conversion rate up to 3 MSPS. However, in these modes, the full specified accuracy is guaranteed only when the time between conversions does not exceed 1 ms. If the time between two consecutive conversions is longer than 1 ms (after power up), the first conversion result should be ignored. These modes make the AD7621 ideal for applications where both high accuracy and fast sample rate are required. Wideband warp mode offers slightly improved linearity and THD over warp mode.

Normal mode (WARP = low, IMPULSE = low) is the fastest mode (2 MSPS) without any limitation on time between conversions. This mode makes the AD7621 ideal for asynchronous applications such as data acquisition systems, where both high accuracy and fast sample rate are required.

Impulse mode (WARP = low, IMPULSE = high), the lowest power dissipation mode, allows power saving between conversions. The maximum throughput in this mode is 1.25 MSPS. In this mode, the ADC powers down circuits after conversion making the AD7621 ideal for battery-powered applications.

TRANSFER FUNCTIONS

Using the OB/$\overline{2C}$ digital input, the AD7621 offers two output codings: straight binary and twos complement. The LSB size with V_{REF} = 2.048 V is 2 × V_{REF}/65536, which is 62.5 µV. Refer to Figure 22 and Table 7 for the ideal transfer characteristic.

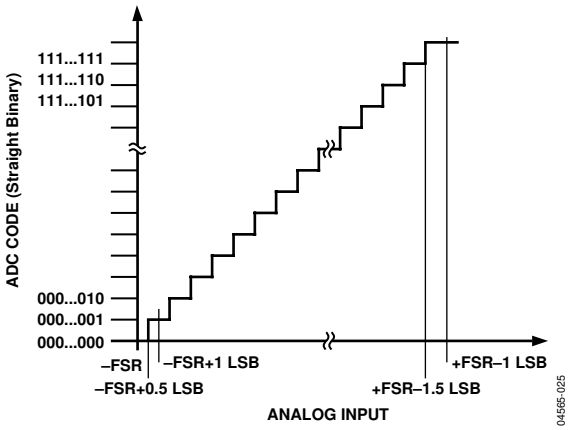
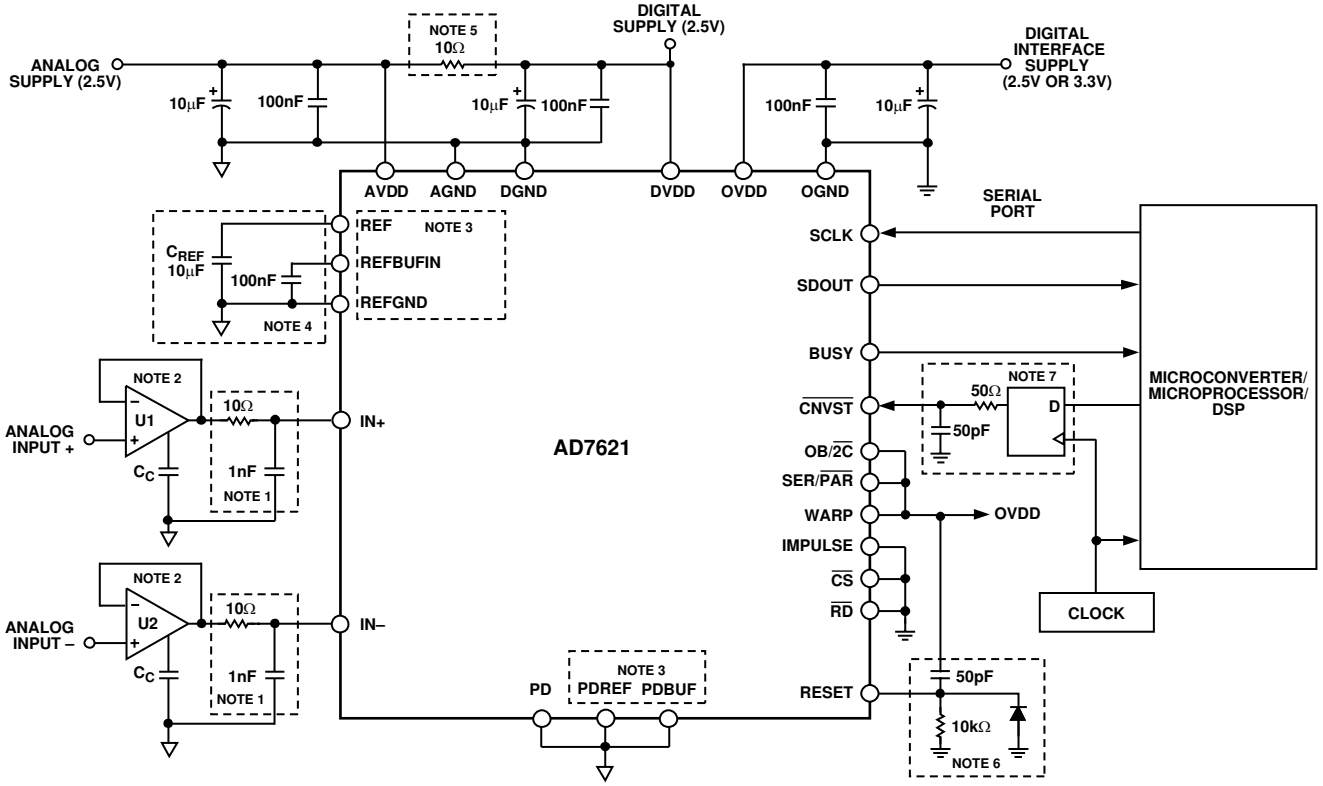


Figure 22. ADC Ideal Transfer Function

Table 7. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 2.048 V	Digital Output Code: Straight Binary	Digital Output Code: Twos Complement
FSR –1 LSB	+2.047938 V	0xFFFF[1]	0x7FFF[1]
FSR – 2 LSB	+2.047875 V	0xFFFE	0x7FFE
Midscale + 1 LSB	+62.5 µV	0x8001	0x0001
Midscale	0 V	0x8000	0x0000
Midscale – 1 LSB	–62.5 µV	0x7FFF	0xFFFF
–FSR + 1 LSB	–2.047938 V	0x0001	0x8001
–FSR	–2.048 V	0x0000[2]	0x8000[2]

[1] This is also the code for overrange analog input (V_{IN+} – $V_{IN–}$ above V_{REF} – V_{REFGND}).
[2] This is also the code for underrange analog input (V_{IN+} – $V_{IN–}$ below –V_{REF} + V_{REFGND}).



1. SEE ANALOG INPUT SECTION.
2. THE AD8021 IS RECOMMENDED. SEE DRIVER AMPLIFIER CHOICE SECTION.
3. THE CONFIGURATION SHOWN IS USING THE INTERNAL REFERENCE. SEE VOLTAGE REFERENCE INPUT SECTION.
4. A 10µF CERAMIC CAPACITOR (X5R, 1206 SIZE) IS RECOMMENDED (e.g., PANASONIC ECJ3YB0J106M). SEE VOLTAGE REFERENCE INPUT SECTION.
5. OPTION, SEE POWER SUPPLY SECTION.
6. OPTION, SEE POWER UP SECTION.
7. OPTIONAL LOW JITTER CNVST, SEE CONVERSION CONTROL SECTION.

Figure 23. Typical Connection Diagram

TYPICAL CONNECTION DIAGRAM

Figure 23 shows a typical connection diagram for the AD7621. Different circuitry from that shown in this diagram are optional and are discussed below.

ANALOG INPUTS

Figure 24 shows an equivalent circuit of the input structure of the AD7621.

The two diodes, D_1 and D_2, provide ESD protection for the analog inputs, IN+ and IN−. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V as this causes the diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of 100 mA maximum. For instance, these conditions could eventually occur when the input buffer's U1 or U2 supplies are different from AVDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

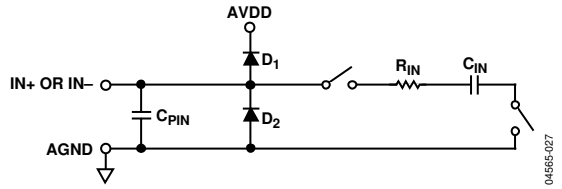


Figure 24. AD7621 Simplified Analog Input.

The analog input of AD7621 is a true differential structure. By using this differential input, small signals common to both inputs are rejected, as shown in Figure 25, representing the typical CMRR over frequency with internal and external references.

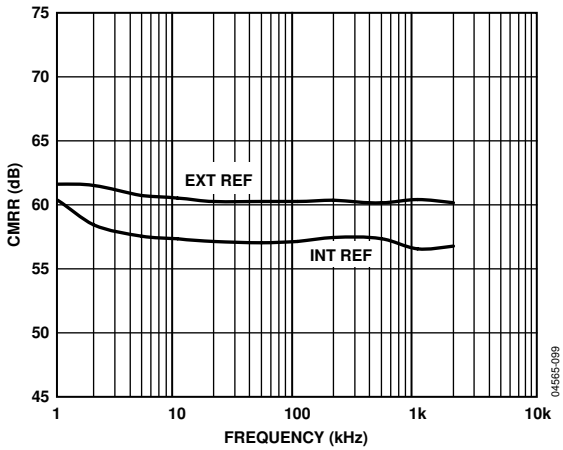


Figure 25. Analog Input CMRR vs. Frequency

During the acquisition phase for ac signals, the impedance of the analog inputs, IN+ and IN−, can be modeled as a parallel combination of Capacitor C_{PIN} and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 350 Ω and is a lumped component comprised of some serial resistors and the on resistance of the switches. C_{IN} is typically 12 pF and is mainly the ADC sampling capacitor. During the conversion phase, when the switches are opened, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a one-pole, low-pass filter that has a typical −3 dB cutoff frequency of 50 MHz, thereby reducing an undesirable aliasing effect while limiting noise from the inputs.

Since the input impedance of the AD7621 is very high, the AD7621 can be directly driven by a low impedance source without gain error. To further improve the noise filtering achieved by the AD7621 analog input circuit, an external, one-pole RC filter between the amplifier's outputs and the ADC analog inputs can be used, as shown in Figure 23. However, large source impedances significantly affect the ac performance, especially total harmonic distortion (THD). The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency, as shown in Figure 26.

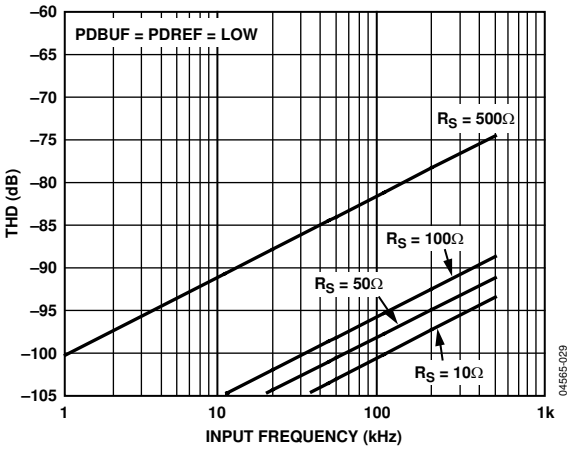


Figure 26. THD vs. Analog Input Frequency and Source Resistance

DRIVER AMPLIFIER CHOICE

Although the AD7621 is easy to drive, the driver amplifier needs to meet the following requirements:

- Together, the driver amplifier and the AD7621 analog input circuit must be able to settle for a full-scale step of the capacitor array at a 16-bit level (0.0015%). In the amplifier data sheet, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection. The AD8021 op amp, which combines ultralow noise and high gain bandwidth, meets this settling time requirement even when used with gains up to 13.
- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7621. The noise

coming from the driver is filtered by the AD7621 analog input circuit one-pole, low-pass filter made by R_{IN} and C_{IN} or by the external filter, if one is used. The SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20\log\left(\frac{53}{\sqrt{2809 + \pi f_{-3dB}\,(Ne_N)^2}}\right)$$

where:

f_{-3dB} is the input bandwidth of the AD7621 (50 MHz) or the cutoff frequency of the input filter (16 MHz), if one is used.

N is the noise factor of the amplifier (+1 in buffer configuration).

e_N is the equivalent input voltage noise density of the op amp, in nV/√Hz.

For instance, a driver with an equivalent input noise density of 2.1 nV/√Hz, like the AD8021 with a noise gain of +1 when configured as a buffer, degrades the SNR by only 0.33 dB when using the RC filter in Figure 23, and by 1 dB without.

- The driver needs to have a THD performance suitable to that of the AD7621. Figure 13 gives the THD vs. frequency that the driver should exceed.

The AD8021 meets these requirements and is appropriate for almost all applications. The AD8021 needs a 10 pF external compensation capacitor that should have good linearity as an NPO ceramic or mica type. Moreover, the use of a noninverting +1 gain arrangement is recommended and helps to obtain the best signal-to-noise ratio.

The AD8022 can also be used when a dual version is needed and a gain of 1 is present. The AD829 is an alternative in applications where high frequency (above 100 kHz) performance is not required. In applications with a gain of 1, an 82 pF compensation capacitor is required. The AD8610 is an option when low bias current is needed in low frequency applications.

Single-to-Differential Driver

For applications using unipolar analog signals, a single-ended-to-differential driver, as shown in Figure 27, allows for a differential input into the part. This configuration, when provided an input signal of 0 to V_{REF}, will produce a differential $\pm V_{REF}$ with midscale at $V_{REF}/2$. The one-pole filter using R = 10 Ω and C = 1 nF provides a corner frequency of 16 MHz.

If the application can tolerate more noise, the AD8139 differential driver can be used.

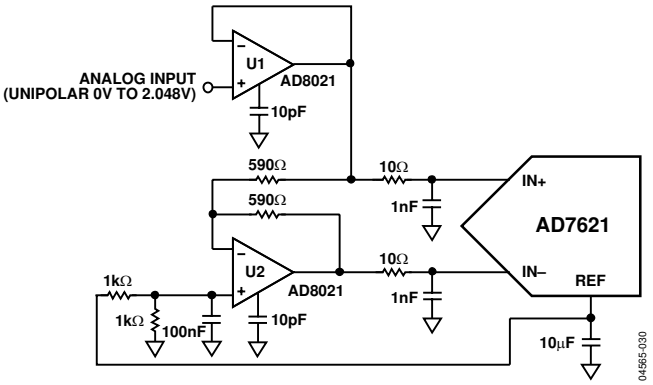


Figure 27. Single-Ended-to-Differential Driver Circuit (Internal Reference Buffer Used)

VOLTAGE REFERENCE INPUT

The AD7621 allows the choice of either a very low temperature drift internal voltage reference or an external reference.

Unlike many ADCs with internal references, the internal reference of the AD7621 provides excellent performance and can be used in almost all applications.

Internal Reference (PDBUF = Low, PDREF = Low)

To use the internal reference, the PDREF and PDBUF inputs must be low. This produces a 1.2 V band gap output on REFBUFIN which, amplified by the internal buffer, results in a 2.048 V reference on the REF pin.

The internal reference is temperature-compensated to 2.048 V ± 10 mV. The reference is trimmed to provide a typical drift of 7 ppm/°C. This typical drift characteristic is shown in Figure 7.

The output resistance of the REFBUFIN is 6.33 kΩ (minimum) when the internal reference is enabled. It is necessary to decouple this with a ceramic capacitor greater than 100 nF. Thus, the capacitor provides an RC filter for noise reduction.

Since the output impedance of REFBUFIN is typically 6.33 kΩ, relative humidity (among other industrial contaminates) can directly affect the drift characteristics of the reference. Typically, a guard ring is used to reduce the effects of drift under such circumstances. However, since the AD7621 has a fine lead pitch, guarding this node is not practical. Therefore, in these industrial and other types of applications, it is recommended to use a conformal coating such as Dow Corning 1-2577 or Humiseal 1B73.

External 1.2 V Reference and Internal Buffer (PDREF = High, PBBUF = Low)

To use an external reference with the internal buffer, PDREF should be high and PDBUF should be low. This powers down the internal reference and allows the 1.2 V reference to be applied to REFBUFIN.

External Reference (PDBUF = High, PRBUF = High)

To use an external reference directly on the REF pin, PDREF and PDBUF should both be high.

For improved drift performance, an external reference, such as the AD780 or ADR431, can be used. The advantages of directly using the external voltage reference are:

- SNR and dynamic range improvement (about 1.7 dB) resulting from the use of a reference voltage very close to the supply (2.5 V) instead of a typical 2.048 V reference when the internal reference is used. This is calculated by

$$SNR = 20\log\left(\frac{2.048}{2.50}\right)$$

- Power savings when the internal reference is powered down (PBREF = PDBUF = high).

PDREF and PDBUF power down the internal reference and the internal reference buffer, respectively.

Reference Decoupling

Whether using an internal or external reference, the AD7621 voltage reference input (REF) has a dynamic input impedance; therefore, it should be driven by a low impedance source with efficient decoupling between the REF and REFGND inputs. This decoupling depends on the choice of the voltage reference, but usually consists of a low ESR capacitor connected to REF and REFGND with minimum parasitic inductance. A 10 µF (X5R, 1206 size) ceramic chip capacitor (or 47 µF tantalum capacitor) is appropriate when using either the internal reference or one of these recommended reference voltages:

- The low noise, low temperature drift ADR431 and AD780
- The low power ADR291
- The low cost AD1582

The placement of the reference decoupling is also important to the performance of the AD7621. The decoupling capacitor should be mounted on the same side as the ADC right at the REF pin with a thick PCB trace. The REFGND should also connect to the reference decoupling capacitor with the shortest distance.

For applications that use multiple AD7621 devices, it is more effective to use the internal reference buffer in order to buffer the reference voltage.

The voltage reference temperature coefficient (TC) directly impacts full scale; therefore, in applications where full-scale accuracy matters, care must be taken with the TC. For instance, a ±15 ppm/°C TC of the reference changes full-scale by ±1 LSB/°C.

Temperature Sensor

The TEMP pin measures the temperature of the AD7621. To improve the calibration accuracy over the temperature range, the output of the TEMP pin is applied to one of the inputs of the analog switch (such as, ADG779), and the ADC itself is used to measure its own temperature. This configuration is shown in Figure 28.

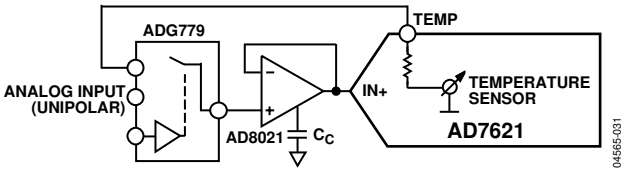


Figure 28. Use of the Temperature Sensor

POWER SUPPLY

The AD7621 uses three sets of power supply pins: an analog 2.5 V supply AVDD, a digital 2.5 V core supply DVDD, and a digital input/output interface supply OVDD. The OVDD supply allows direct interface with any logic working between 2.3 V and 5.25 V. To reduce the number of supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply as shown in Figure 23.

Power Sequencing

The AD7621 is independent of power supply sequencing once OVDD does not exceed DVDD by more than 0.3 V until DVDD = 2.3 V during any time; for instance, at power-up or power-down (see the Absolute Maximum Ratings section). Additionally, it is very insensitive to power supply variations over a wide frequency range as shown in Figure 29.

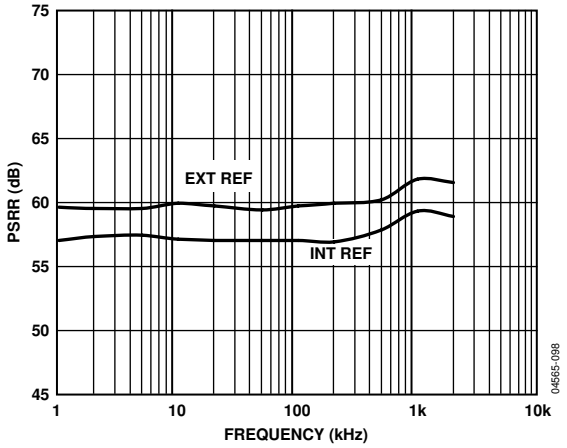


Figure 29. PSRR vs. Frequency

Power-Up

At power-up, or returning to operational mode from the power-down mode (PD = high), the AD7621 engages an initialization process. During this time, the first 128 conversions should be ignored or the RESET input could be pulsed to engage a faster initialization process. Refer to the Digital Interface section for RESET and timing details.

A simple power-on reset circuit, as shown in Figure 23, can be used to minimize the digital interface. As OVDD powers up, the capacitor is shorted and brings RESET high; it is then charged returning RESET to low. However, this circuit only works when powering up the AD7621 because the power down mode (PD = high) does not power down any of the supplies. As a result, RESET is low.

POWER DISSIPATION VS. THROUGHPUT

In impulse mode, the AD7621 automatically reduces its power consumption at the end of each conversion phase. During the acquisition phase, the operating currents are very low which allows a significant power saving when the conversion rate is reduced (see Figure 30). This feature makes the AD7621 ideal for very low power, battery-operated applications.

It should be noted that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, drive the digital inputs close to the power rails (that is, OVDD and OGND).

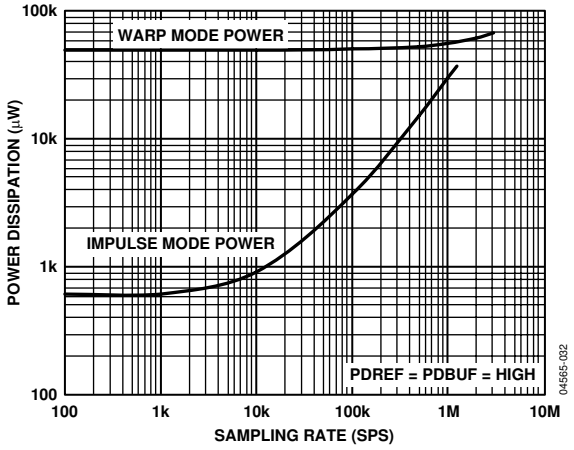


Figure 30. Power Dissipation vs. Sample Rate

CONVERSION CONTROL

The AD7621 is controlled by the $\overline{\text{CNVST}}$ input. A falling edge on $\overline{\text{CNVST}}$ is all that is necessary to initiate a conversion. Detailed timing diagrams of the conversion process are shown in Figure 31. Once initiated, it cannot be restarted or aborted, even by the power-down input, PD, until the conversion is complete. The $\overline{\text{CNVST}}$ signal operates independently of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals.

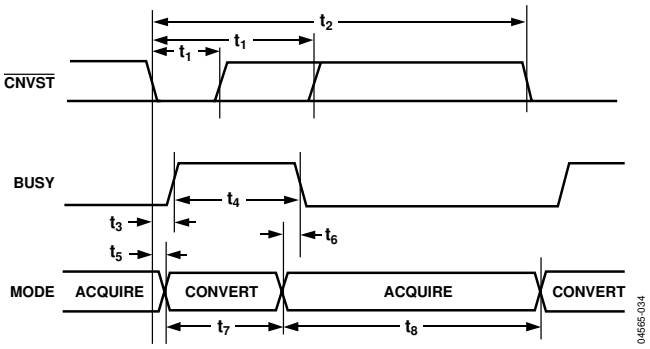


Figure 31. Basic Conversion Timing

For optimal performance, the rising edge of $\overline{\text{CNVST}}$ should not occur after the maximum $\overline{\text{CNVST}}$ low time, t_1, or until the end of conversion.

Although $\overline{\text{CNVST}}$ is a digital signal, it should be designed with special care with fast, clean edges, and levels with minimum overshoot, undershoot, or ringing.

The $\overline{\text{CNVST}}$ trace should be shielded with ground and a low value (such as 50 Ω) serial resistor termination should be added close to the output of the component that drives this line. Also, a 60 pF capacitor is recommended to further reduce the effects of overshoot and undershoot as shown in Figure 23.

For applications where SNR is critical, the $\overline{\text{CNVST}}$ signal should have very low jitter. This can be achieved by using a dedicated oscillator for $\overline{\text{CNVST}}$ generation, or by clocking $\overline{\text{CNVST}}$ with a high frequency, low jitter clock, as shown in Figure 23.

INTERFACES

DIGITAL INTERFACE

The AD7621 has a versatile digital interface that can be set up as either a serial or parallel interface with the host system. The serial interface is multiplexed on the parallel data bus. The AD7621 digital interface also accommodates 2.5 V, 3.3 V, or 5 V logic with either OVDD at 2.5 V or 3.3 V. OVDD defines the logic high output voltage. In most applications, the OVDD supply pin of the AD7621 is connected to the host system interface 2.5 V or 3.3 V digital supply. Finally, by using the OB/$\overline{2C}$ input pin, both twos complement or straight binary coding can be used.

The two signals, $\overline{CS}$ and $\overline{RD}$, control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually, $\overline{CS}$ allows the selection of each AD7621 in multicircuit applications and is held low in a single AD7621 design. $\overline{RD}$ is generally used to enable the conversion result on the data bus.

RESET

The RESET input is used to reset the AD7621 and generate a fast initialization. A rising edge on RESET aborts the current conversion (if any) and tristates the data bus. The falling edge of RESET clears the data bus and engages the initialization process indicated by pulsing BUSY high. Conversions can take place after the falling edge of BUSY. Refer to Figure 32 for the RESET timing details.

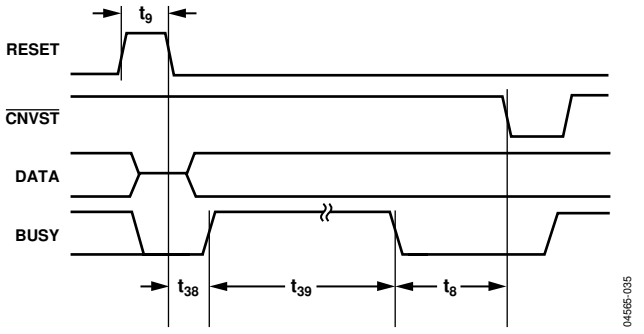


Figure 32. RESET Timing

PARALLEL INTERFACE

The AD7621 is configured to use the parallel interface when SER/$\overline{PAR}$ is held low.

Master Parallel Interface

Data can be continuously read by tying $\overline{CS}$ and $\overline{RD}$ low thus requiring minimal microprocessor connections. However, in this mode the data bus is always driven and cannot be used in shared bus applications (unless the device is held in RESET). Figure 33 details the timing for this mode.

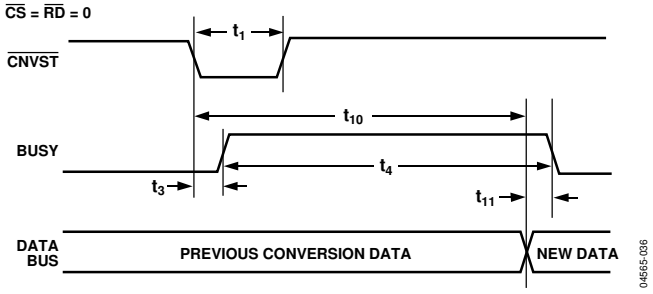


Figure 33. Master Parallel Data Timing for Reading (Continuous Read)

Slave Parallel Interface

In slave parallel reading mode, the data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion, as shown in Figure 34 and Figure 35, respectively. When the data is read during the conversion, it is recommended that it is read-only during the first half of the conversion phase. This avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

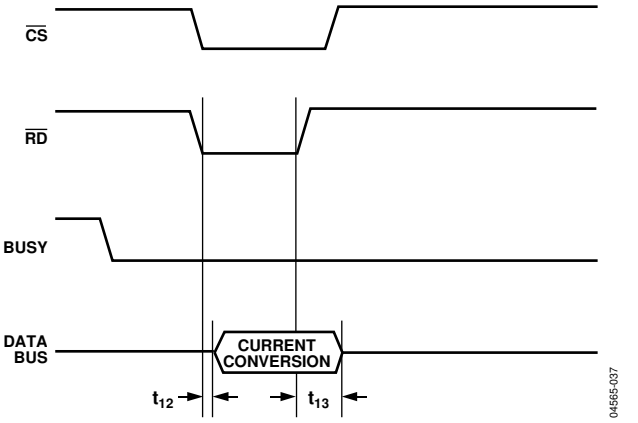


Figure 34. Slave Parallel Data Timing for Reading (Read After Convert)

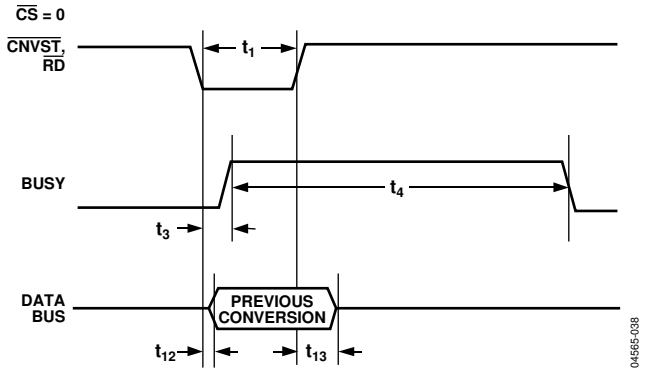


Figure 35. Slave Parallel Data Timing for Reading (Read During Convert)

8-Bit Interface (Master or Slave)

The BYTESWAP pin allows a glueless interface to an 8-bit bus. As shown in Figure 36, when BYTESWAP is low, the LSB byte is output on D[7:0] and the MSB is output on D[15:8]. When BYTESWAP is high, the LSB and MSB bytes are swapped, and the LSB is output on D[15:8] and the MSB is output on D[7:0]. By connecting BYTESWAP to an address line, the 16-bit data can be read in two bytes on either D[15:8] or D[7:0]. This interface can be used in both master and slave parallel reading modes.

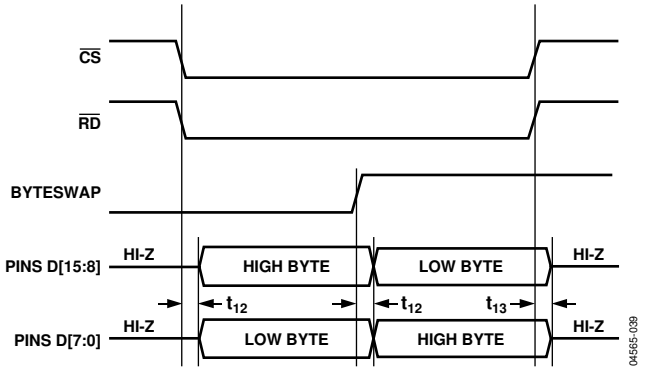


Figure 36. 8-Bit and 16-Bit Parallel Interface

SERIAL INTERFACE

The AD7621 is configured to use the serial interface when SER/$\overline{\text{PAR}}$ is held high. The AD7621 outputs 16 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 16 clock pulses provided on the SCLK pin. The output data is valid on both the rising and falling edge of the data clock.

MASTER SERIAL INTERFACE

Internal Clock

The AD7621 is configured to generate and provide the serial data clock SCLK when the EXT/$\overline{\text{INT}}$ pin is held low. The AD7621 also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted, if desired. Depending on the read during convert input, RDC/SDIN, the data can be read after each conversion or during the following conversion. Figure 37 and Figure 38 show detailed timing diagrams of these two modes.

Usually, because the AD7621 is used with a fast throughput, the master read during conversion mode is the most recommended serial mode. In this mode, the serial clock and data toggle at appropriate instants, minimizing potential feedthrough between digital activity and critical conversion decisions. In this mode, the SCLK period changes since the LSBs require more time to settle and the SCLK is derived from the SAR conversion cycle.

In read after conversion mode, unlike other modes, the BUSY signal returns low after the 16 data bits are pulsed out and not at the end of the conversion phase resulting in a longer BUSY width. As a result, the maximum throughput cannot be achieved in this mode.

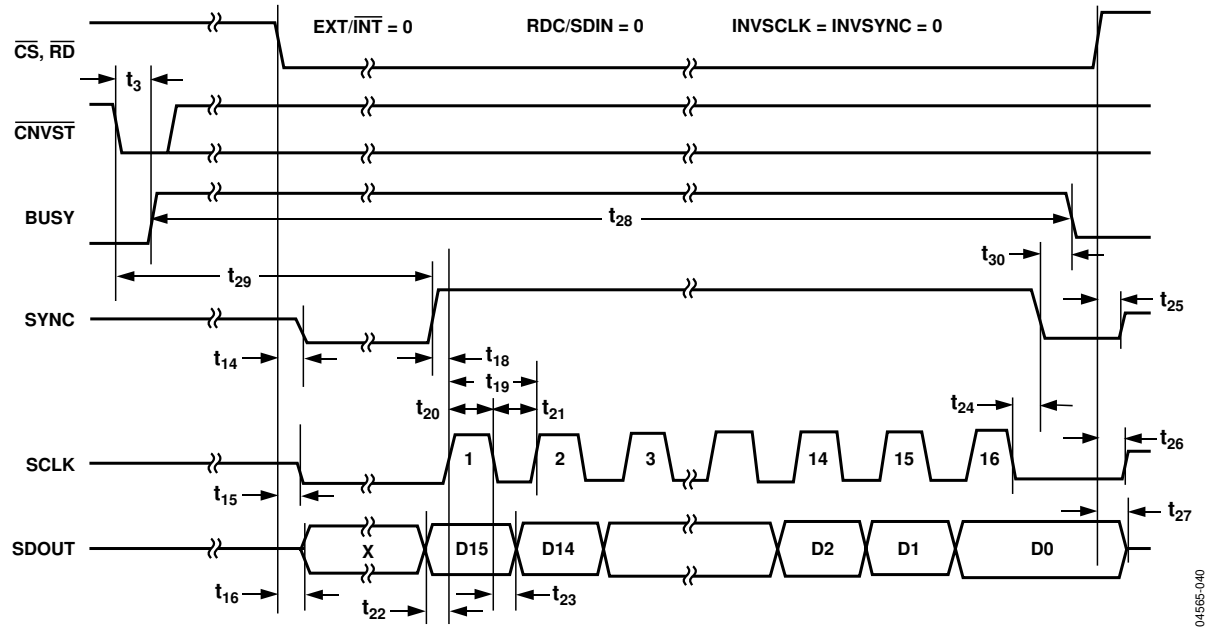


Figure 37. Master Serial Data Timing for Reading (Read After Convert)

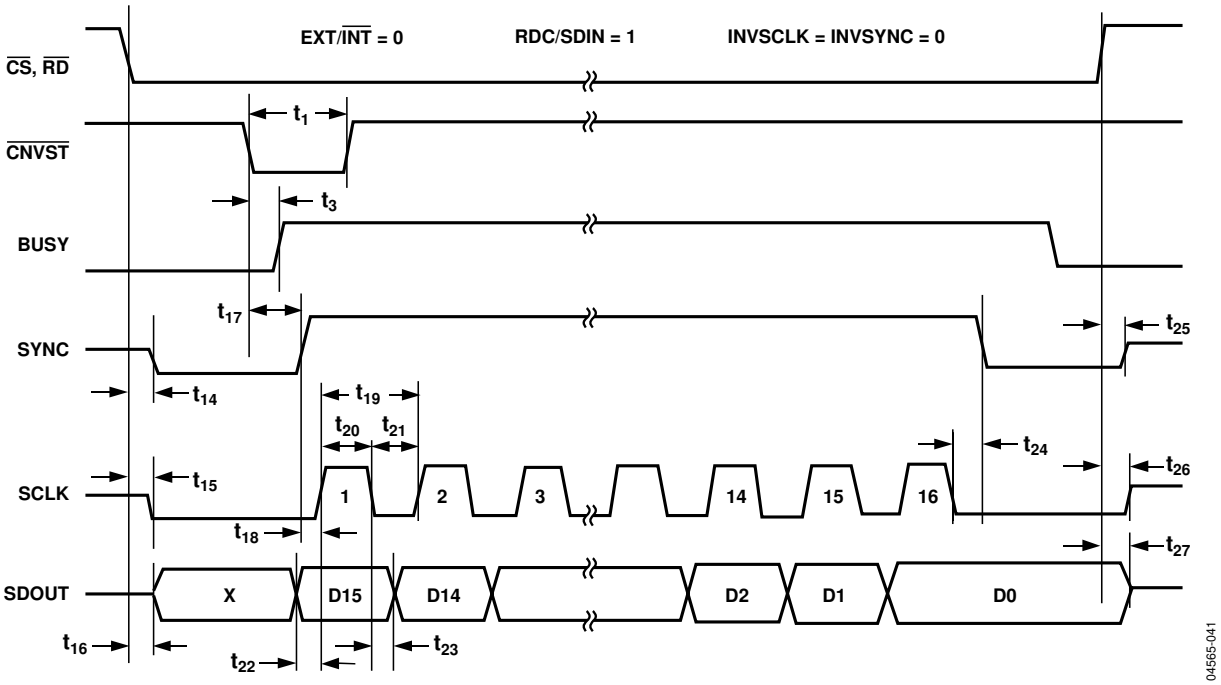


Figure 38. Master Serial Data Timing for Reading (Read Previous Conversion During Convert)

SLAVE SERIAL INTERFACE

External Clock

The AD7621 is configured to accept an externally supplied serial data clock on the SCLK pin when the EXT/$\overline{\text{INT}}$ pin is held high. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{\text{CS}}$. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or a discontinuous clock. A discontinuous clock can be either normally high or normally low when inactive. Figure 40 and Figure 41 show the detailed timing diagrams of these methods.

While the AD7621 is performing a bit decision, it is important that voltage transients be avoided on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase because the AD7621 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it is a discontinuous clock that is toggling only when BUSY is low or, more importantly, that it does not transition during the latter half of BUSY high.

External Discontinuous Clock Data Read After Conversion

Though the maximum throughput cannot be achieved using this mode, it is the most recommended of the serial slave modes. Figure 40 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by BUSY returning low, the conversion result can be read while both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low. Data is shifted out MSB first with 16 clock pulses and is valid on the rising and falling edges of the clock.

Among the advantages of this method is the fact that conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process. Another advantage is the ability to read the data at any speed up to 80 MHz, which accommodates both the slow digital host interface and the fastest serial reading.

Finally, in this mode only, the AD7621 provides a daisy-chain feature using the RDC/SDIN pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when desired, as, for instance, in isolated multiconverter applications.

An example of the concatenation of two devices is shown in Figure 39. Simultaneous sampling is possible by using a common $\overline{\text{CNVST}}$ signal. It should be noted that the RDC/SDIN input is latched on the edge of SCLK opposite to the one used to shift out the data on SDOUT. Hence, the MSB of the upstream converter just follows the LSB of the downstream converter on the next SCLK cycle.

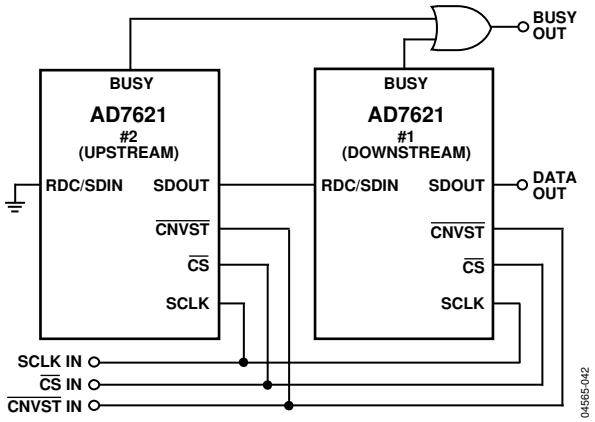


Figure 39. Two AD7621 Devices in a Daisy-Chain Configuration

External Clock Data Read During Previous Conversion

Figure 41 shows the detailed timing diagrams of this method. During a conversion, while both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, the result of the previous conversion can be read. The data is shifted out, MSB first, with 16 clock pulses and is valid on both the rising and falling edge of the clock. The 16 bits have to be read before the current conversion is complete, otherwise; RDERROR is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading. There is no daisy-chain feature in this mode and RDC/SDIN input should always be tied either high or low.

To reduce performance degradation due to digital activity, a fast discontinuous clock (at least 30 MHz when impulse mode is used, 60 MHz when normal mode is used, or 80 MHz when warp mode is used) is recommended to ensure that all the bits are read during the first half of the SAR conversion phase.

It is also possible to begin to read data after conversion and continue to read the last bits after a new conversion has been initiated. However, this is not recommended when using the fastest throughput of any mode since the acquisition times are only 70 ns, 100 ns, and 50 ns for warp, normal, and impulse modes.

If the maximum throughput is not used, thus allowing more acquisition time, then the use of a slower clock speed can be used to read the data.