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### FEATURES

Multiple pins/software-programmable input ranges

5 V (10 V p-p), +10 V (20 V p-p), ±5 V (20 V p-p),  
±10 V (40 V p-p)

Pins or serial SPI<sup>®</sup>-compatible input ranges/mode selection

Throughput

670 kSPS (warp mode)

570 kSPS (normal mode)

450 kSPS (impulse mode)

INL: ±1.5 LSB typical, ±2.5 LSB maximum (±9.5 ppm of FSR)

18-bit resolution with no missing codes

Dynamic range: 102.5 dB

SNR: 101 dB @ 2 kHz

THD: -112 dB @ 2kHz

iCMOS<sup>®</sup> process technology

5 V internal reference: typical drift 3 ppm/°C; TEMP output

No pipeline delay (SAR architecture)

Parallel (18-/16-/8-bit bus) and serial 5 V/3.3 V interface

SPI-/QSPI<sup>™</sup>-/MICROWIRE<sup>™</sup>-/DSP-compatible

Power dissipation

180 mW @ 670 kSPS, warp mode

28 mW @ 100 kSPS, impulse mode

10 mW @ 1 kSPS, impulse mode

Pb-free, 48-lead LQFP and 48-Lead LFCSP (7 mm × 7 mm)

### APPLICATIONS

CT scanners

High dynamic data acquisition

Σ-Δ replacement

Spectrum analysis

Medical instruments

Instrumentation

Process controls

### GENERAL DESCRIPTION

The AD7634 is an 18-bit charge redistribution successive approximation register (SAR), architecture analog-to-digital converter (ADC) fabricated on Analog Devices, Inc.'s iCMOS high voltage process. The device is configured through hardware or via a dedicated write-only serial configuration port for input range and operating mode. The AD7634 contains a high speed 18-bit sampling ADC, an internal conversion clock, an internal reference (and buffer), error correction circuits, and both serial and parallel system interface ports. A falling edge on CNVST samples the fully differential analog inputs on IN+ and IN-. The AD7634 features four different analog input ranges and three different sampling modes. Operation is specified from -40°C to +85°C.

Rev. B

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### FUNCTIONAL BLOCK DIAGRAM

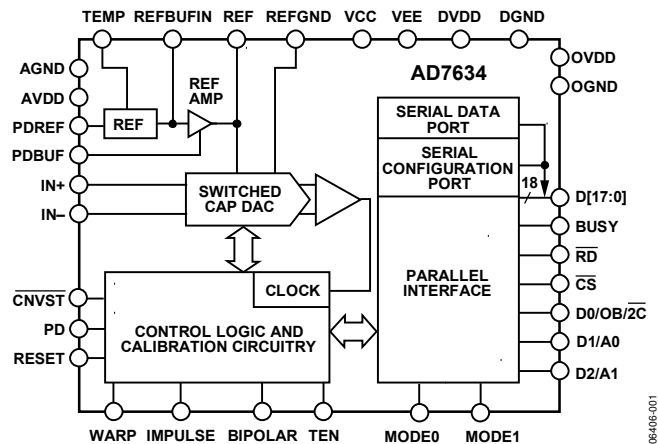


Figure 1.

Table 1. 48-Lead PulSAR Selection

Input Type	Res (Bits)	100 to 250 (kSPS)	500 to 570 (kSPS)	570 to 1000 (kSPS)	>1000 (kSPS)
Bipolar	14			AD7951	
Differential Bipolar	14			AD7952	
Unipolar	16	AD7651 AD7660 AD7661	AD7650 AD7652 AD7664 AD7666	AD7653 AD7667	
Bipolar	16	AD7610 AD7663	AD7665	AD7612 AD7671	
Differential Unipolar	16	AD7675	AD7676	AD7677	AD7621 AD7622 AD7623
Simultaneous/Multichannel Unipolar	16		AD7654 AD7655		
Differential Unipolar	18	AD7678	AD7679	AD7674	AD7641 AD7643
Differential Bipolar	18	AD7631		AD7634	

# AD7634\* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- AD7634 Evaluation Kit

## DOCUMENTATION

### Application Notes

- AN-931: Understanding PulSAR ADC Support Circuitry
- AN-932: Power Supply Sequencing

### Data Sheet

- AD7634: 18-Bit, 670 kSPS, Differential Programmable Input PulSAR® ADC Data Sheet

## REFERENCE MATERIALS

### Informational

- iCMOS Technology Enabling the +/-10V World

### Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

## DESIGN RESOURCES

- AD7634 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all AD7634 EngineerZone Discussions.

## SAMPLE AND BUY

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## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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## REVISION HISTORY

### 12/12—Rev. A to Rev. B

Changes to Power Sequencing Section .....	23
Updated Outline Dimensions .....	32
Changes to Ordering Guide .....	32

### 3/11—Rev. 0 to Rev. A

Changes to Resolution Parameter, Table 2 .....	3
Changes to Figure 4 and Table 6.....	8
Added Exposed Pad Notation to Outline Dimensions .....	32

### 1/07—Revision 0: Initial Version

## SPECIFICATIONS

AVDD = DVDD = 5 V; OVDD = 2.7 V to 5.5 V; VCC = 15 V; VEE = -15 V; VREF = 5 V; all specifications T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.

Table 2.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		18			Bits
ANALOG INPUTS					
Differential Voltage Range, V <sub>IN</sub>	(V <sub>IN+</sub> ) - (V <sub>IN-</sub> )				
0 V to 5 V	V <sub>IN</sub> = 10 V p-p	-V <sub>REF</sub>		+V <sub>REF</sub>	V
0 V to 10 V	V <sub>IN</sub> = 20 V p-p	-2 V <sub>REF</sub>		+2 V <sub>REF</sub>	V
±5 V	V <sub>IN</sub> = 20 V p-p	-2 V <sub>REF</sub>		+2 V <sub>REF</sub>	V
±10 V	V <sub>IN</sub> = 40 V p-p	-4 V <sub>REF</sub>		+4 V <sub>REF</sub>	V
Operating Voltage Range	V <sub>IN+</sub> , V <sub>IN-</sub> to AGND				
0 V to 5 V		-0.1		+5.1	V
0 V to 10 V		-0.1		+10.1	V
±5 V		-5.1		+5.1	V
±10 V		-10.1		+10.1	V
Common-Mode Voltage Range	V <sub>IN+</sub> , V <sub>IN-</sub>				
5 V		V <sub>REF</sub> /2 - 0.1	V <sub>REF</sub> /2	V <sub>REF</sub> /2 + 0.1	V
10 V		V <sub>REF</sub> - 0.2	V <sub>REF</sub>	V <sub>REF</sub> + 0.2	V
Bipolar Ranges		-0.1	0	+0.1	V
Analog Input CMRR	f <sub>IN</sub> = 100 kHz		75		dB
Input Current	V <sub>IN</sub> = ±5 V, ±10 V @ 670 kSPS		220 <sup>1</sup>		μA
Input Impedance	See Analog Inputs section				
THROUGHPUT SPEED					
Complete Cycle	In warp mode			1.49	μs
Throughput Rate	In warp mode	1		670	kSPS
Time Between Conversions	In warp mode			1	ms
Complete Cycle	In normal mode			1.75	μs
Throughput Rate	In normal mode	0		570	kSPS
Complete Cycle	In impulse mode			2.22	μs
Throughput Rate	In impulse mode	0		450	kSPS
DC ACCURACY					
Integral Linearity Error <sup>2</sup>	600 kSPS throughput	-2.5	±1.5	+2.5	LSB <sup>3</sup>
Integral Linearity Error	670 kSPS throughput		±1.5		LSB
No Missing Codes		18			Bits
Differential Linearity Error <sup>2</sup>		-1		+2.5	LSB
Transition Noise			0.75		LSB
Unipolar Zero Error		-0.06		+0.06	%FS
Bipolar Zero Error		-0.03		+0.03	%FS
Zero Error Temperature Drift			±0.5		ppm/°C
Bipolar Full-Scale Error		-0.09		+0.09	%FS
Unipolar Full-Scale Error		-0.07		+0.07	%FS
Full-Scale Error Temperature Drift			±0.5		ppm/°C
Power Supply Sensitivity	AVDD = 5 V ± 5%		3		LSB
AC ACCURACY					
Dynamic Range	V <sub>IN</sub> = 0 to 5 V, f <sub>IN</sub> = 2 kHz, -60 dB	100	101.8		dB <sup>4</sup>
	V <sub>IN</sub> = all other input ranges, f <sub>IN</sub> = 2 kHz, -60 dB	100	102.5		dB
Signal-to-Noise Ratio (SNR)	V <sub>IN</sub> = 0 to 5 V, f <sub>IN</sub> = 2 kHz	98.5	100.5		dB
	V <sub>IN</sub> = all other input ranges, f <sub>IN</sub> = 2 kHz	98.5	101		dB
Signal-to-(Noise + Distortion), SINAD	f <sub>IN</sub> = 2 kHz		100		dB
Total Harmonic Distortion	f <sub>IN</sub> = 2 kHz		112		dB
Spurious-Free Dynamic Range	f <sub>IN</sub> = 2 kHz		113		dB
-3 dB Input Bandwidth	V <sub>IN</sub> = 0 V to 5 V		45		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Jitter			5		ps rms
Transient Response	Full-scale step			500	ns

Parameter	Conditions/Comments	Min	Typ	Max	Unit
INTERNAL REFERENCE	PDREF = PDBUF = low				
Output Voltage	REF @ 25°C	4.965	5.000	5.035	V
Temperature Drift	−40°C to +85°C		±3		ppm/°C
Line Regulation	AVDD = 5 V ± 5%		±15		ppm/V
Long-Term Drift	1000 hours		50		ppm
Turn-On Settling Time	C <sub>REF</sub> = 22 μF		10		ms
REFERENCE BUFFER	PDREF = high				
REFBUF <sub>IN</sub> Input Voltage Range		2.4	2.5	2.6	V
EXTERNAL REFERENCE	PDREF = PDBUF = high				
Voltage Range	REF	4.75	5	AVDD + 0.1	V
Current Drain	670 kSPS throughput		250		μA
TEMPERATURE PIN					
Voltage Output	@ 25°C		311		mV
Temperature Sensitivity			1		mV/°C
Output Resistance			4.33		kΩ
DIGITAL INPUTS					
Logic Levels					
V <sub>IL</sub>		−0.3		+0.6	V
V <sub>IH</sub>		2.1		OVDD + 0.3	V
I <sub>IL</sub>		−1		+1	μA
I <sub>IH</sub>		−1		+1	μA
DIGITAL OUTPUTS					
Data Format	Parallel or serial 18-bit				
Pipeline Delay <sup>5</sup>					
V <sub>OL</sub>	I <sub>SINK</sub> = 500 μA			0.4	V
V <sub>OH</sub>	I <sub>SOURCE</sub> = −500 μA	OVDD − 0.6			V
POWER SUPPLIES					
Specified Performance					
AVDD		4.75 <sup>6</sup>	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.7		5.25	V
VCC		7	15	15.75	V
VEE		−15.75	−15	0	V
Operating Current <sup>7,8</sup>	@ 670 kSPS throughput				
AVDD					
With Internal Reference			18.2		mA
With Internal Reference Disabled			16.5		mA
DVDD			7.1		mA
OVDD			0.3		mA
VCC	VCC = 15 V, with internal reference buffer		2.9		mA
	VCC = 15 V		2		mA
VEE	VEE = −15 V		2		mA
Power Dissipation	@ 670 kSPS throughput				
With Internal Reference	PDREF = PDBUF = low		195	225	mW
With Internal Reference Disabled	PDREF = PDBUF = high		175	205	mW
In Power-Down Mode <sup>9</sup>	PD = high		10		μW
TEMPERATURE RANGE <sup>10</sup>					
Specified Performance	T <sub>MIN</sub> to T <sub>MAX</sub>	−40		+85	°C

<sup>1</sup> With V<sub>IN</sub> = unipolar 5 V or unipolar 10 V ranges, the input current is typically 70 μA. In all input ranges, the input current scales with throughput. See the Analog Inputs section.

<sup>2</sup> Linearity is tested using endpoints, not best fit. All linearity is tested with an external 5 V reference.

<sup>3</sup> LSB means least significant bit. All specifications in LSB do not include the error contributed by the reference.

<sup>4</sup> All specifications in decibels are referred to a full-scale range input, FSR. Tested with an input signal at 0.5 dB below full-scale, unless otherwise specified.

<sup>5</sup> Conversion results are available immediately after completed conversion.

<sup>6</sup> 4.75 V or V<sub>REF</sub> − 0.1 V, whichever is larger.

<sup>7</sup> Tested in parallel reading mode.

<sup>8</sup> With internal reference, PDREF = PDBUF = low; with internal reference disabled, PDREF = PDBUF = high. With internal reference buffer, PDBUF = low.

<sup>9</sup> With all digital inputs forced to OVDD.

<sup>10</sup> Consult sales for extended temperature range.

**TIMING SPECIFICATIONS**

AVDD = DVDD = 5 V; OVDD = 2.7 V to 5.5 V; VCC = 15 V; VEE = -15 V; V<sub>REF</sub> = 5 V; all specifications T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.

**Table 3.**

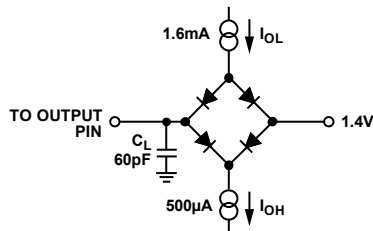
Parameter	Symbol	Min	Typ	Max	Unit
<b>CONVERSION AND RESET (See Figure 35 and Figure 36)</b>					
Convert Pulse Width	t <sub>1</sub>	10			ns
Time Between Conversions	t <sub>2</sub>				
Warp Mode/Normal Mode/Impulse Mode <sup>1</sup>		1.49/1.75/2.22			μs
CNVST Low to BUSY High Delay	t <sub>3</sub>			35	ns
BUSY High All Modes (Except Master Serial Read After Convert)	t <sub>4</sub>				
Warp Mode/Normal Mode/Impulse Mode				1.18/1.43/1.68	μs
Aperture Delay	t <sub>5</sub>		2		ns
End of Conversion to BUSY Low Delay	t <sub>6</sub>	10			ns
Conversion Time	t <sub>7</sub>				
Warp Mode/Normal Mode/Impulse Mode				1.18/1.43/1.68	μs
Acquisition Time, All modes	t <sub>8</sub>	310			ns
RESET Pulse Width	t <sub>9</sub>	10			ns
<b>PARALLEL INTERFACE MODES (See Figure 37 and Figure 39)</b>					
CNVST Low to Data Valid Delay	t <sub>10</sub>				
Warp Mode/Normal Mode/Impulse Mode				1.15/1.40/1.65	μs
Data Valid to BUSY Low Delay	t <sub>11</sub>	20			ns
Bus Access Request to Data Valid	t <sub>12</sub>			40	ns
Bus Relinquish Time	t <sub>13</sub>	2		15	ns
<b>MASTER SERIAL INTERFACE MODES<sup>2</sup> (See Figure 41 and Figure 42)</b>					
C <sub>S</sub> Low to SYNC Valid Delay	t <sub>14</sub>			10	ns
C <sub>S</sub> Low to Internal SDCLK Valid Delay <sup>2</sup>	t <sub>15</sub>			10	ns
C <sub>S</sub> Low to SDOUT Delay	t <sub>16</sub>			10	ns
CNVST Low to SYNC Delay, Read During Convert	t <sub>17</sub>				
Warp Mode/Normal Mode/Impulse Mode			50/290/530		ns
SYNC Asserted to SDCLK First Edge Delay	t <sub>18</sub>	3			ns
Internal SDCLK Period <sup>3</sup>	t <sub>19</sub>	30		45	ns
Internal SDCLK High <sup>3</sup>	t <sub>20</sub>	15			ns
Internal SDCLK Low <sup>3</sup>	t <sub>21</sub>	10			ns
SDOUT Valid Setup Time <sup>3</sup>	t <sub>22</sub>	4			ns
SDOUT Valid Hold Time <sup>3</sup>	t <sub>23</sub>	5			ns
SDCLK Last Edge to SYNC Delay <sup>3</sup>	t <sub>24</sub>	5			ns
C <sub>S</sub> High to SYNC High-Z	t <sub>25</sub>			10	ns
C <sub>S</sub> High to Internal SDCLK High-Z	t <sub>26</sub>			10	ns
C <sub>S</sub> High to SDOUT High-Z	t <sub>27</sub>			10	ns
BUSY High in Master Serial Read After Convert <sup>3</sup>	t <sub>28</sub>		See Table 4		
CNVST Low to SYNC Delay Read After Convert					
Warp Mode/Normal Mode/Impulse Mode	t <sub>29</sub>		1.1/1.3/1.5		μs
SYNC Deasserted to BUSY Low Delay	t <sub>30</sub>		25		ns

Parameter	Symbol	Min	Typ	Max	Unit
SLAVE SERIAL/SERIAL CONFIGURATION INTERFACE MODES <sup>2</sup> (See Figure 44, Figure 45, and Figure 47)					
External SDCLK, SCCLK Setup Time	t <sub>31</sub>	5			ns
External SDCLK Active Edge to SDOUT Delay	t <sub>32</sub>	2		18	ns
SDIN/SCIN Setup Time	t <sub>33</sub>	5			ns
SDIN/SCIN Hold Time	t <sub>34</sub>	5			ns
External SDCLK/SCCLK Period	t <sub>35</sub>	25			ns
External SDCLK/SCCLK High	t <sub>36</sub>	10			ns
External SDCLK/SCCLK Low	t <sub>37</sub>	10			ns

<sup>1</sup> In warp mode only, the time between conversions is 1 ms; otherwise, there is no required maximum time.  
<sup>2</sup> In serial interface modes, the SDSYNC, SDSCLK, and SDOUT timings are defined with a maximum load C<sub>L</sub> of 10 pF; otherwise, the load is 60 pF maximum.  
<sup>3</sup> In serial master read during convert mode. See Table 4 for serial master read after convert mode.

Table 4. Serial Clock Timings in Master Read After Convert Mode

DIVSCLK[1] DIVSCLK[0]	Symbol	0 0	0 1	1 0	1 1	Unit
SYNC to SDCLK First Edge Delay Minimum	t <sub>18</sub>	3	20	20	20	ns
Internal SDCLK Period Minimum	t <sub>19</sub>	30	60	120	240	ns
Internal SDCLK Period Maximum	t <sub>19</sub>	45	90	180	360	ns
Internal SDCLK High Minimum	t <sub>20</sub>	15	30	60	120	ns
Internal SDCLK Low Minimum	t <sub>21</sub>	10	25	55	115	ns
SDOUT Valid Setup Time Minimum	t <sub>22</sub>	4	20	20	20	ns
SDOUT Valid Hold Time Minimum	t <sub>23</sub>	5	8	35	90	ns
SDCLK Last Edge to SYNC Delay Minimum	t <sub>24</sub>	5	7	35	90	ns
BUSY High Width Maximum	t <sub>28</sub>					
Warp Mode		1.98	2.78	4.34	7.46	μs
Normal Mode		2.23	3.03	4.59	7.71	μs
Impulse Mode		2.48	3.28	4.84	7.96	μs



NOTES  
 1. IN SERIAL INTERFACE MODES, THE SYNC, SDCLK, AND SDOUT ARE DEFINED WITH A MAXIMUM LOAD C<sub>L</sub> OF 10pF; OTHERWISE, THE LOAD IS 60pF MAXIMUM.

Figure 2. Load Circuit for Digital Interface Timing, SDOUT, SYNC, and SDCLK Outputs, C<sub>L</sub> = 10 pF

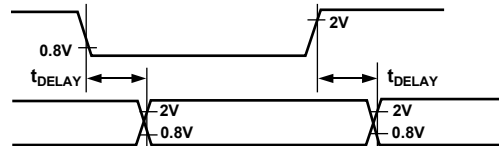


Figure 3. Voltage Reference Levels for Timing



## ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs/Outputs IN <sup>+</sup> <sup>1</sup> , IN <sup>-</sup> <sup>1</sup> to AGND	VEE – 0.3 V to VCC + 0.3 V
REF, REFBUF <sub>IN</sub> , TEMP, REFGND to AGND	AVDD + 0.3 V to AGND – 0.3 V
Ground Voltage Differences AGND, DGND, OGND	±0.3 V
Supply Voltages AVDD, DVDD, OVDD	–0.3 V to +7 V
AVDD to DVDD, AVDD to OVDD	±7 V
DVDD to OVDD	±7 V
VCC to AGND, DGND	–0.3 V to +16.5 V
VEE to GND	+0.3 V to –16.5 V
Digital Inputs PDREF, PDBUF	–0.3 V to OVDD + 0.3 V ±20 mA
Internal Power Dissipation <sup>2</sup>	700 mW
Internal Power Dissipation <sup>3</sup>	2.5 W
Junction Temperature	125°C
Storage Temperature Range	–65°C to +125°C

<sup>1</sup> See the Analog Inputs section.

<sup>2</sup> Specification is for the device in free air: 48-lead LFPQ;  $\theta_{JA} = 91^\circ\text{C}/\text{W}$ ,  
 $\theta_{JC} = 30^\circ\text{C}/\text{W}$ .

<sup>3</sup> Specification is for the device in free air: 48-lead LFCSP;  $\theta_{JA} = 26^\circ\text{C}/\text{W}$ .

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

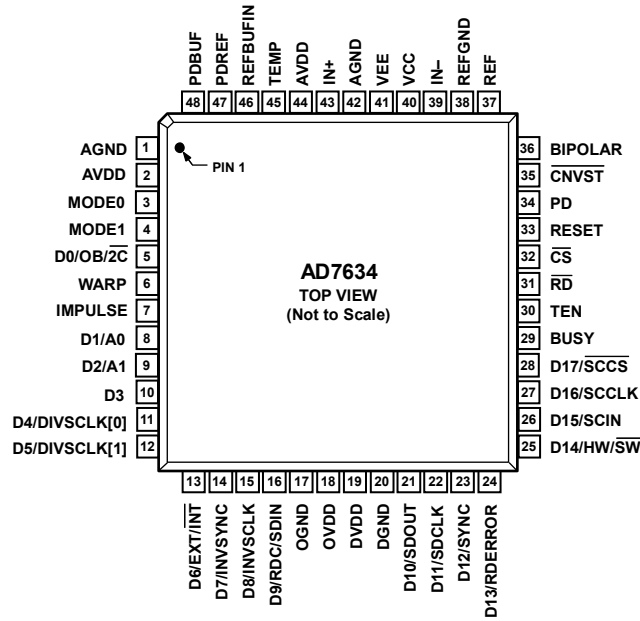
### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
1. FOR THE LEAD FRAME CHIP SCALE PACKAGE (LFCSP), THE EXPOSED PAD SHOULD BE CONNECTED TO VEE. THIS CONNECTION IS NOT REQUIRED TO MEET THE ELECTRICAL PERFORMANCES.

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type <sup>1</sup>	Description																				
1, 42	AGND	P	Analog Power Ground Pins. Ground reference point for all analog I/O. All analog I/O should be referenced to AGND and should be connected to the analog ground plane of the system. In addition, the AGND, DGND, and OGNND voltages should be at the same potential.																				
2, 44	AVDD	P	Analog Power Pins. Nominally 4.75 V to 5.25 V and decoupled with 10 μF and 100 nF capacitors.																				
3, 4	MODE[0:1]	DI	Data Input/Output Interface Mode Selection. <table border="1"> <thead> <tr> <th>Interface Mode</th> <th>MODE1</th> <th>MODE0</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Low</td> <td>Low</td> <td>18-bit interface</td> </tr> <tr> <td>1</td> <td>Low</td> <td>High</td> <td>16-bit interface</td> </tr> <tr> <td>2</td> <td>High</td> <td>Low</td> <td>8-bit (byte) interface</td> </tr> <tr> <td>3</td> <td>High</td> <td>High</td> <td>Serial interface</td> </tr> </tbody> </table>	Interface Mode	MODE1	MODE0	Description	0	Low	Low	18-bit interface	1	Low	High	16-bit interface	2	High	Low	8-bit (byte) interface	3	High	High	Serial interface
Interface Mode	MODE1	MODE0	Description																				
0	Low	Low	18-bit interface																				
1	Low	High	16-bit interface																				
2	High	Low	8-bit (byte) interface																				
3	High	High	Serial interface																				
5	D0/OB/ $\overline{2C}$	DI/O <sup>2</sup>	In 18-bit parallel mode, this output is used as Bit 0 of the parallel port data output bus and the data coding is straight binary. In all other modes, this pin allows the choice of straight binary or twos complement. When $\overline{OB/2C}$ = high, the digital output is straight binary When $\overline{OB/2C}$ = low, the MSB is inverted resulting in a twos complement output from its internal shift register.																				
6	WARP	DI <sup>2</sup>	Conversion Mode Selection. See the Modes of Operation section for a more detailed description. Used in conjunction with the IMPULSE input per the following: <table border="1"> <thead> <tr> <th>Conversion Mode</th> <th>WARP</th> <th>IMPULSE</th> </tr> </thead> <tbody> <tr> <td>Normal</td> <td>Low</td> <td>Low</td> </tr> <tr> <td>Impulse</td> <td>Low</td> <td>High</td> </tr> <tr> <td>Warp</td> <td>High</td> <td>Low</td> </tr> <tr> <td>Normal</td> <td>High</td> <td>High</td> </tr> </tbody> </table>	Conversion Mode	WARP	IMPULSE	Normal	Low	Low	Impulse	Low	High	Warp	High	Low	Normal	High	High					
Conversion Mode	WARP	IMPULSE																					
Normal	Low	Low																					
Impulse	Low	High																					
Warp	High	Low																					
Normal	High	High																					
7	IMPULSE	DI <sup>2</sup>	Conversion Mode Selection. See the WARP pin description in this table. See the Modes of Operation section for a more detailed description.																				

Pin No.	Mnemonic	Type <sup>1</sup>	Description
8	D1/A0	DI/O	When MODE[1:0] = 0, this pin is Bit 1 of the parallel port data output bus. In all other modes, this input pin controls the form in which data is output as shown in Table 7.
9	D2/A1	DI/O	When MODE[1:0] = 0, this pin is Bit 2 of the parallel port data output bus.
10	D3	DO	When MODE[1:0] = 1 or 2, this input pin controls the form in which data is output as shown in Table 7. When MODE[1:0] = 0, 1, or 2, this output is used as Bit 3 of the parallel port data output bus. This pin is always an output, regardless of the interface mode.
11, 12	D[4:5] or DIVSCLK[0:1]	DI/O	When MODE[1:0] = 0, 1, or 2, these pins are Bit 4 and Bit 5 of the parallel port data output bus. When MODE[1:0] = 3, serial data clock division selection. When using serial master read after convert mode (EXT/INT = low, RDC/SDIN = low), these inputs can be used to slow down the internally generated serial clock that clocks the data output. In other serial modes, these pins are high impedance outputs.
13	D6 or EXT/INT	DO/I	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 6 of the parallel port data output bus. When MODE[1:0] = 3, Serial Data Clock Source Select. In serial mode, this input is used to select the internally generated (master) or external (slave) serial data clock for the AD7634 output data. When EXT/INT = low (master mode), the internal serial data clock is selected on SDCLK output. When EXT/INT = high (slave mode), the output data is synchronized to an external clock signal (gated by CS) connected to the SDCLK input.
14	D7 or INVSYNC	DI/O	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 7 of the parallel port data output bus. When MODE[1:0] = 3, Serial Data Invert Sync Select. In serial master mode (MODE[1:0] = 3, EXT/INT = low), this input is used to select the active state of the SYNC signal. When INVSYNC = low, SYNC is active high. When INVSYNC = high, SYNC is active low.
15	D8 or INVSCCLK	DI/O	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 8 of the parallel port data output bus. When MODE[1:0] = 3, Invert SDCLK/SCCLK Select. This input is used to invert both SDCLK and SCCLK. When INVSCCLK = low, the rising edge of SDCLK/SCCLK are used. When INVSCCLK = high, the falling edge of SDCLK/SCCLK are used.
16	D9 or RDC or SDIN	DI/O	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 9 of the parallel port data output bus. When MODE[1:0] = 3, Serial Data Read During Convert. In serial master mode (MODE[1:0] = 3, EXT/INT = low), RDC is used to select the read mode. See the Master Serial Interface section. When RDC = low, the current result is read after conversion. Note the maximum throughput is not attainable in this mode. When RDC = high, the previous conversion result is read during the current conversion. When MODE[1:0] = 3, Serial Data In. In serial slave mode (MODE[1:0] = 3, EXT/INT = high), SDIN can be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 16 SDCLK periods after the initiation of the read sequence.
17	OGND	P	Input/Output Interface Digital Power Ground. Ground reference point for digital outputs. Should be connected to the system digital ground ideally at the same potential as AGND and DGND.
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply as the supply of the host interface 2.5 V, 3 V, or 5 V and decoupled with 10 μF and 100 nF capacitors.
19	DVDD	P	Digital Power. Nominally at 4.75 V to 5.25 V and decoupled with 10 μF and 100 nF capacitors. Can be supplied from AVDD.
20	DGND	P	Digital Power Ground. Ground reference point for digital outputs. Should be connected to system digital ground ideally at the same potential as AGND and OGND.
21	D10 or SDOUT	DI/O	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 10 of the parallel port data output bus. When MODE[1:0] = 3, Serial Data Output. In all serial modes, this pin is used as the serial data output synchronized to SDCLK. Conversion results are stored in an on-chip register. The AD7634 provides the conversion result, MSB first, from its internal shift register. The data format is determined by the logic level of OB/2C. When EXT/INT = low (master mode), SDOUT is valid on both edges of SDCLK. When EXT/INT = high (slave mode): When INVSCCLK = low, SDOUT is updated on SDCLK rising edge. When INVSCCLK = high, SDOUT is updated on SDCLK falling edge.

Pin No.	Mnemonic	Type <sup>1</sup>	Description															
22	D11 or SDCLK	DI/O	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 11 of the parallel port data output bus. When MODE[1:0] = 3, Serial Data Clock. In all serial modes, this pin is used as the serial data clock input or output, dependent on the logic state of the EXT/INT pin. The active edge where the data SDOUT is updated depends on the logic state of the INVCLK pin.															
23	D12 or SYNC	DO	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 12 of the parallel port data output bus. When MODE[1:0] = 3, Serial Data Frame Synchronization. In serial master mode (MODE[1:0] = 3, EXT/INT = low), this output is used as a digital output frame synchronization for use with the internal data clock. When a read sequence is initiated and INVSYNC = low, SYNC is driven high and remains high while the SDOUT output is valid. When a read sequence is initiated and INVSYNC = high, SYNC is driven low and remains low while the SDOUT output is valid.															
24	D13 or RDERROR	DO	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 13 of the parallel port data output bus. When MODE[1:0] = 3, Serial Data Read Error. In serial slave mode (MODE[1:0] = 3, EXT/INT = high), this output is used as an incomplete data read error flag. If a data read is started and not completed when the current conversion is completed, the current data is lost and RDERROR is pulsed high.															
25	D14 or HW/SW	DI/O	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 14 of the parallel port data output bus. When MODE[1:0] = 3, Serial Configuration Hardware/Software Select. In serial mode, this input is used to configure the AD7634 by hardware or software. See the Hardware Configuration section and Software Configuration section. When HW/SW = low, the AD7634 is configured through software using the serial configuration register. When HW/SW = high, the AD7634 is configured through dedicated hardware input pins.															
26	D15 or SCIN	DI/O	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 15 of the parallel port data output bus. When MODE[1:0] = 3, Serial Configuration Data Input. In serial software configuration mode (HW/SW = low), this input is used to serially write in, MSB first, the configuration data into the serial configuration register. The data on this input is latched with SCCLK. See the Software Configuration section.															
27	D16 or SCCLK	DI/O	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 16 of the parallel port data output bus. When MODE[1:0] = 3, Serial Configuration Clock. In serial software configuration mode (HW/SW = low), this input is used to clock in the data on SCIN. The active edge where the data SCIN is updated depends on the logic state of the INVCLK pin. See the Software Configuration section.															
28	D17 or SCCS	DI/O	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 17 of the parallel port data output bus. When MODE[1:0] = 3, Serial Configuration Chip Select. In serial software configuration mode (HW/SW = low), this input enables the serial configuration port. See the Software Configuration section.															
29	BUSY	DO	Busy Output. Transitions high when a conversion is started and remains high until the conversion is completed and the data is latched into the on-chip shift register. The falling edge of BUSY can be used as a data-ready clock signal. Note that in master read after convert mode (MODE[1:0] = 3, EXT/INT = low, RDC = low), the busy time changes according to Table 4.															
30	TEN	DI <sup>2</sup>	Input Range Select. Used in conjunction with BIPOLAR per the following: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Input Range</th> <th>BIPOLAR</th> <th>TEN</th> </tr> </thead> <tbody> <tr> <td>0V to 5V</td> <td>Low</td> <td>Low</td> </tr> <tr> <td>0V to 10V</td> <td>Low</td> <td>High</td> </tr> <tr> <td>±5V</td> <td>High</td> <td>Low</td> </tr> <tr> <td>±10V</td> <td>High</td> <td>High</td> </tr> </tbody> </table>	Input Range	BIPOLAR	TEN	0V to 5V	Low	Low	0V to 10V	Low	High	±5V	High	Low	±10V	High	High
Input Range	BIPOLAR	TEN																
0V to 5V	Low	Low																
0V to 10V	Low	High																
±5V	High	Low																
±10V	High	High																
31	RD	DI	Read Data. When CS and RD are both low, the interface parallel or serial output bus is enabled.															
32	CS	DI	Chip Select. When CS and RD are both low, the interface parallel or serial output bus is enabled. CS is also used to gate the external clock in slave serial mode (not used for serial configurable port).															
33	RESET	DI	Reset Input. When high, reset the AD7634. Current conversion, if any, is aborted. The falling edge of RESET resets the data outputs to all zeros (with OB/2C = high) and clears the configuration register. See the Digital Interface section. If not used, this pin can be tied to OGND.															
34	PD	DI <sup>2</sup>	Power-Down Input. When PD = high, power down the ADC. Power consumption is reduced and conversions are inhibited after the current one is completed. The digital interface remains active during power down.															
35	CNVST	DI	Conversion Start. A falling edge on CNVST puts the internal sample-and-hold into the hold state and initiates a conversion.															

Pin No.	Mnemonic	Type <sup>1</sup>	Description
36	BIPOLAR	DI <sup>2</sup>	Input Range Select. See description for Pin 30.
37	REF	AO/I	Reference Input/Output. When PDREF/PDBUF = low, the internal reference and buffer are enabled, producing 5 V on this pin. When PDREF/PDBUF = high, the internal reference and buffer are disabled, allowing an externally supplied voltage reference up to AVDD volts. Decoupling with at least a 22 $\mu$ F capacitor is required with or without the internal reference and buffer. See the Voltage Reference Input/Output section.
38	REFGND	AI	Reference Input Analog Ground. Connected to analog ground plane.
39	IN–	AI	Analog Input. Referenced to IN+. In the 0 V to 5 V input range, IN– is between 0 V and $V_{REF}$ V centered about $V_{REF}/2$ . In the 0 V to 10 V range, IN– is between 0 V and $2 V_{REF}$ V centered about $V_{REF}$ . In the $\pm 5$ V and $\pm 10$ V ranges, IN– is true bipolar up to $\pm 2 V_{REF}$ V ( $\pm 5$ V range) or $\pm 4 V_{REF}$ V ( $\pm 10$ V range) and centered about 0 V. In all ranges, IN– must be driven 180° out of phase with IN+.
40	VCC	P	High Voltage Positive Supply. Normally 7 V to 15 V.
41	VEE	P	High Voltage Negative Supply. Normally 0 V to –15 V (0 V in unipolar ranges).
43	IN+	AI	Analog Input. Referenced to IN–. In the 0 V to 5 V input range, IN+ is between 0 V and $V_{REF}$ V centered about $V_{REF}/2$ . In the 0 V to 10 V range, IN+ is between 0 V and $2 V_{REF}$ V centered about $V_{REF}$ . In the $\pm 5$ V and $\pm 10$ V ranges, IN+ is true bipolar up to $\pm 2 V_{REF}$ V ( $\pm 5$ V range) or $\pm 4 V_{REF}$ V ( $\pm 10$ V range) and centered about 0 V. In all ranges, IN+ must be driven 180° out of phase with IN–
45	TEMP	AO	Temperature Sensor Analog Output. When the internal reference is enabled (PDREF = PDBUF = low), this pin outputs a voltage proportional to the temperature of the AD7634. See the Voltage Reference Input/Output section.
46	REFBUFIN	AI	Reference Buffer Input. When using an external reference with the internal reference buffer (PDBUF = low, PDREF = high), applying 2.5 V on this pin produces 5 V on the REF pin. See the Voltage Reference Input/Output section.
47	PDREF	DI	Internal Reference Power-Down Input. When low, the internal reference is enabled. When high, the internal reference is powered down, and an external reference must be used.
48	PDBUF	DI	Internal Reference Buffer Power-Down Input. When low, the buffer is enabled (must be low when using internal reference). When high, the buffer is powered-down.
49	EPAD <sup>3</sup>	NC	Exposed Pad. The exposed pad is not connected internally. It is recommended that the pad be soldered to VEE.

<sup>1</sup> AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital input; DI/O = bidirectional digital; DO = digital output; P = power, NC = no internal connection.

<sup>2</sup> In serial configuration mode (MODE[1:0] = 3, HW/ $\overline{SW}$  = low), this input is programmed with the serial configuration register and this pin is a don't care. See the Hardware Configuration section and the Software Configuration section.

<sup>3</sup> LFCSP\_VQ package only.

**Table 7. Data Bus Interface Definition**

MODE	MODE1	MODE0	D0/OB/ $\overline{2C}$	D1/A0	D2/A1	D[3]	D[4:9]	D[10:11]	D[12:15]	D[16:17]	Description
0	0	0	R[0]	R[1]	R[2]	R[3]	R[4:9]	R[10:11]	R[12:15]	R[16:17]	18-bit parallel
1	0	1	OB/ $\overline{2C}$	A0 = 0	R[2]	R[3]	R[4:9]	R[10:11]	R[12:15]	R[16:17]	16-bit high word
1	0	1	OB/ $\overline{2C}$	A0 = 1	R[0]	R[1]	All zeros				16-bit low word
2	1	0	OB/ $\overline{2C}$	A0 = 0	A1 = 0	All High-Z		R[10:11]	R[12:15]	R[16:17]	8-bit high byte
2	1	0	OB/ $\overline{2C}$	A0 = 0	A1 = 1	All High-Z		R[2:3]	R[4:7]	R[8:9]	8-bit midbyte
2	1	0	OB/ $\overline{2C}$	A0 = 1	A1 = 0	All High-Z		R[0:1]	All zeros		8-bit low byte
2	1	0	OB/ $\overline{2C}$	A0 = 1	A1 = 1	All High-Z		All zeros		R[0:1]	8-bit low byte
3	1	1	OB/ $\overline{2C}$	All High-Z			Serial interface				Serial interface

# TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = DVDD = 5 V; OVDD = 5 V; VCC = 15 V; VEE = -15 V; V<sub>REF</sub> = 5 V; T<sub>A</sub> = 25°C.

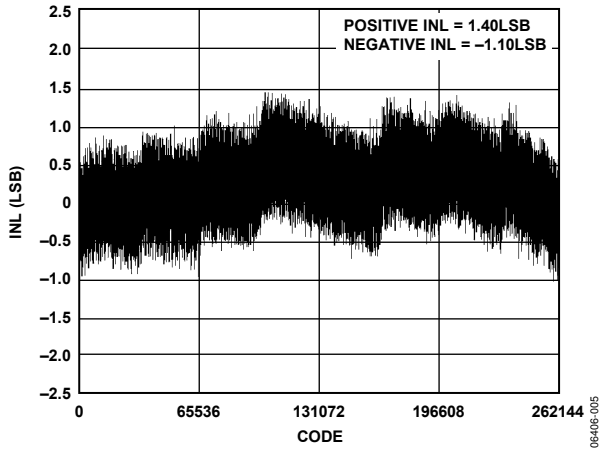


Figure 5. Integral Nonlinearity vs. Code, Bipolar 10 V Range

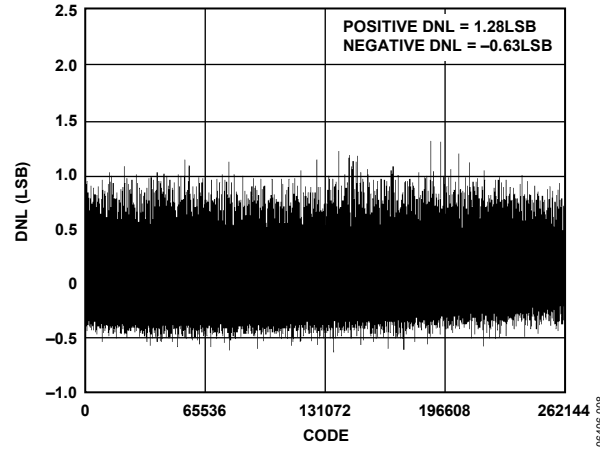


Figure 8. Differential Nonlinearity vs. Code, Bipolar 10 V Range

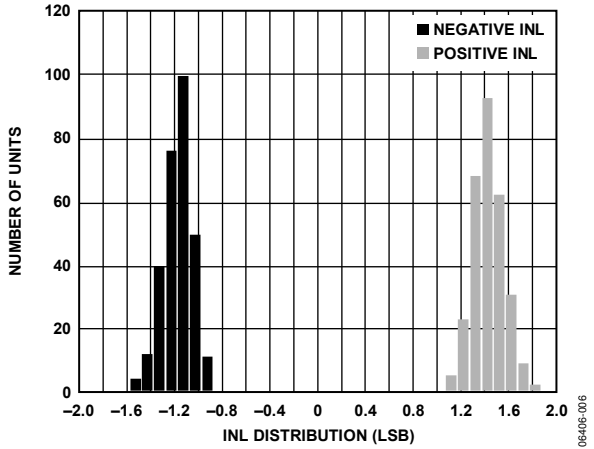


Figure 6. Integral Nonlinearity Distribution, Unipolar 10 V Range (288 Devices)

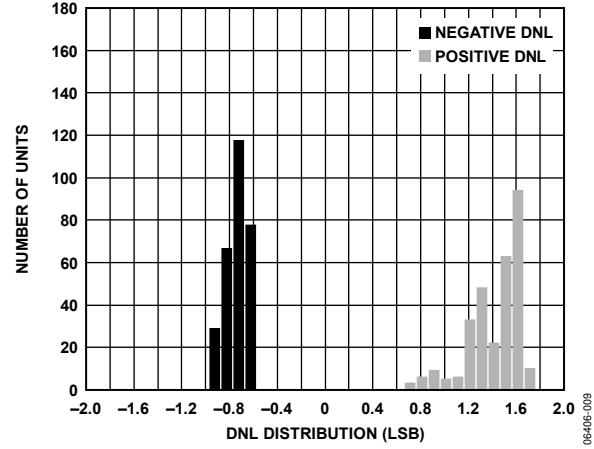


Figure 9. Differential Nonlinearity Distribution, Bipolar 5 V Range (288 Devices)

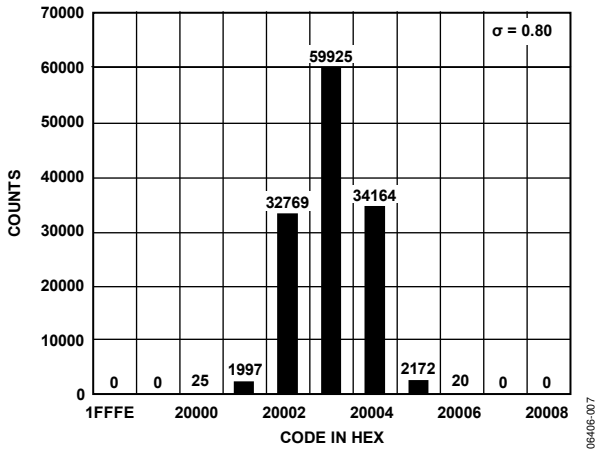


Figure 7. Histogram of 261,120 Conversions of a DC Input at the Code Center, Bipolar 5 V Range

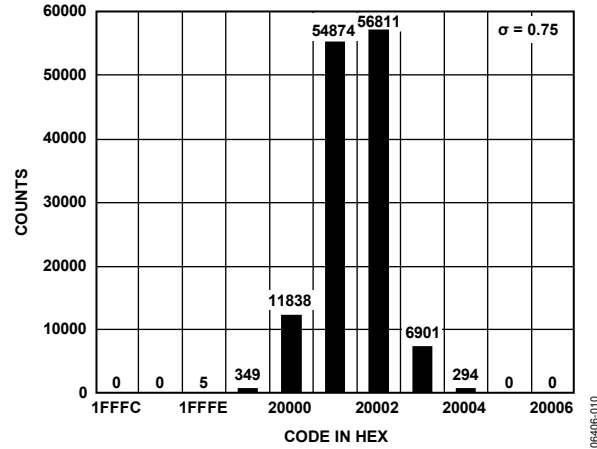


Figure 10. Histogram of 261,120 Conversions of a DC Input at the Code Transition, Bipolar 5 V Range

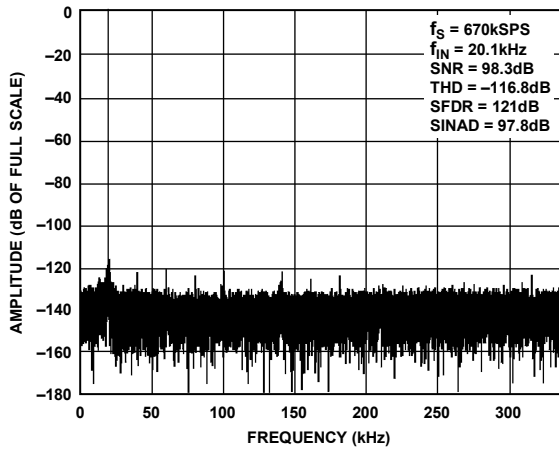


Figure 11. FFT 20 kHz, Bipolar 5 V Range, Internal Reference

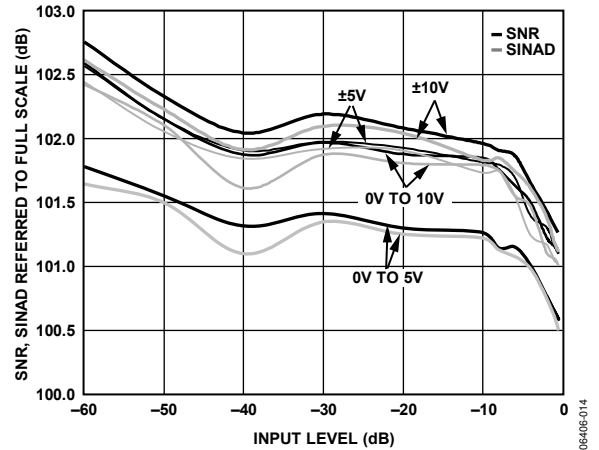


Figure 14. SNR and SINAD vs. Input Level (Referred to Full Scale)

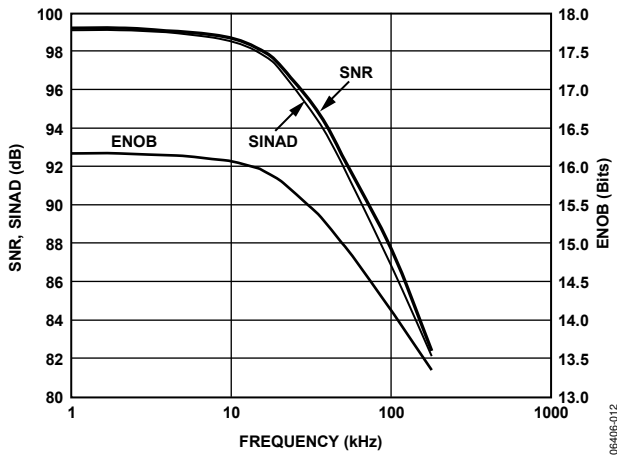


Figure 12. SNR, SINAD, and ENOB vs. Frequency, Unipolar 5 V Range

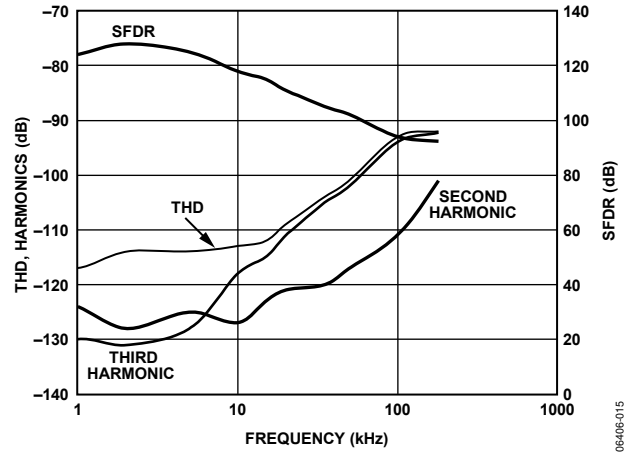


Figure 15. THD, Harmonics, and SFDR vs. Frequency, Unipolar 5 V Range

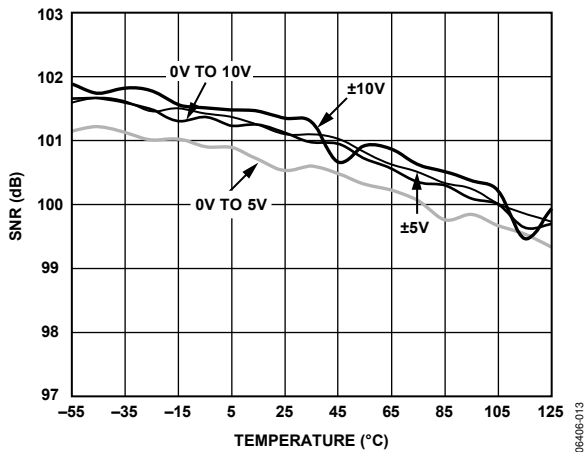


Figure 13. SNR vs. Temperature

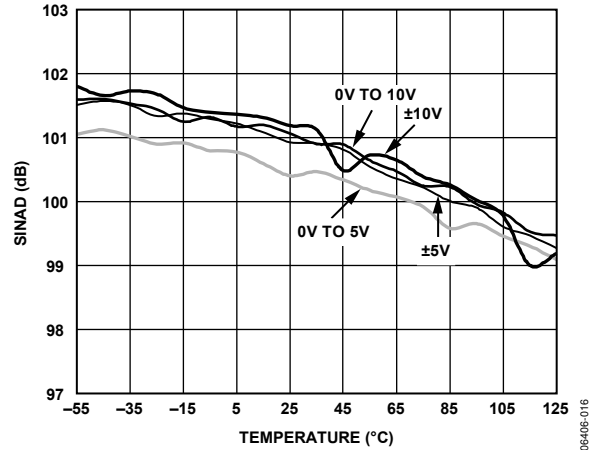


Figure 16. SINAD vs. Temperature

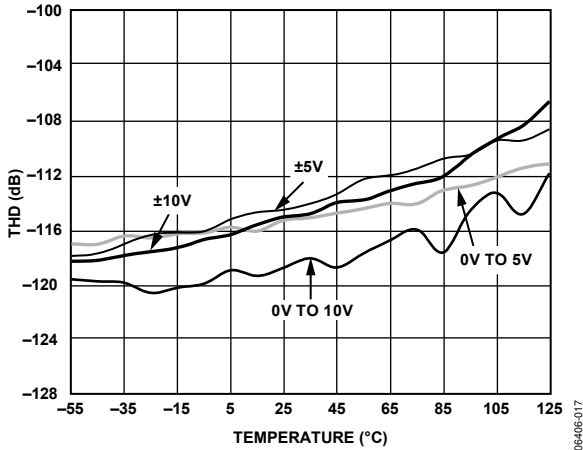


Figure 17. THD vs. Temperature

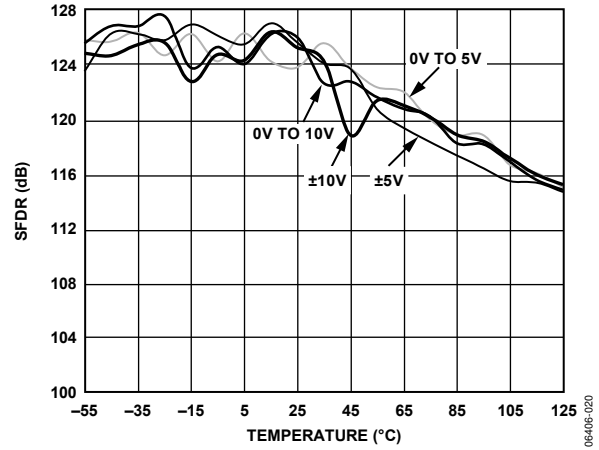


Figure 20. SFDR vs. Temperature (Excludes Harmonics)

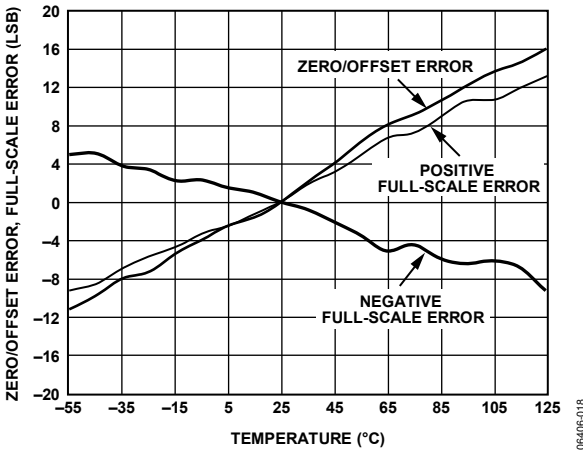


Figure 18. Zero/Offset Error, Positive and Negative Full-Scale Error vs. Temperature, All Normalized to 25°C

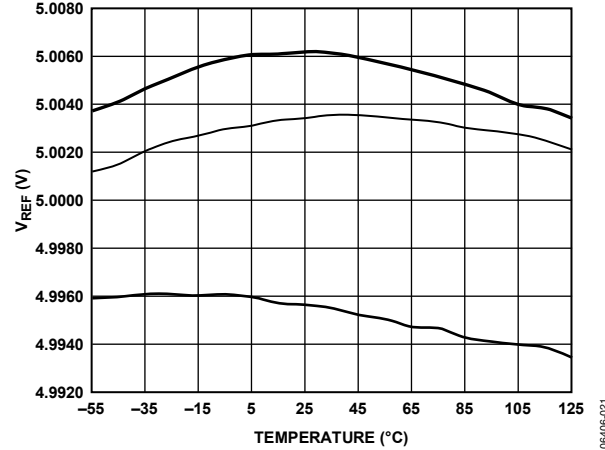


Figure 21. Typical Reference Voltage Output vs. Temperature (3 Devices)

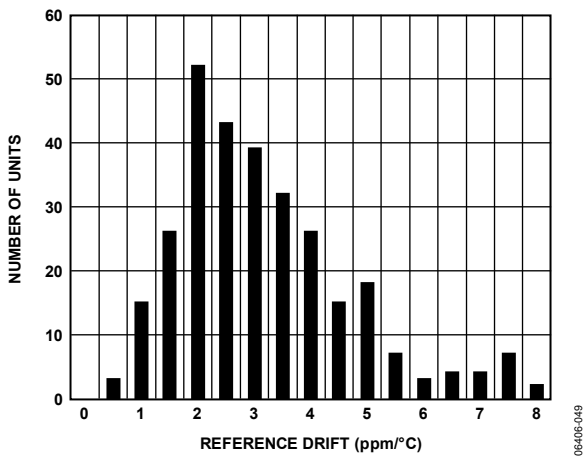


Figure 19. Reference Voltage Temperature Coefficient Distribution (247 Devices)

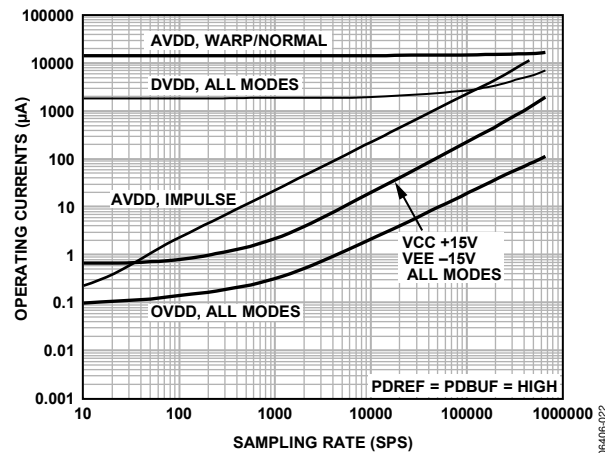


Figure 22. Operating Currents vs. Sample Rate



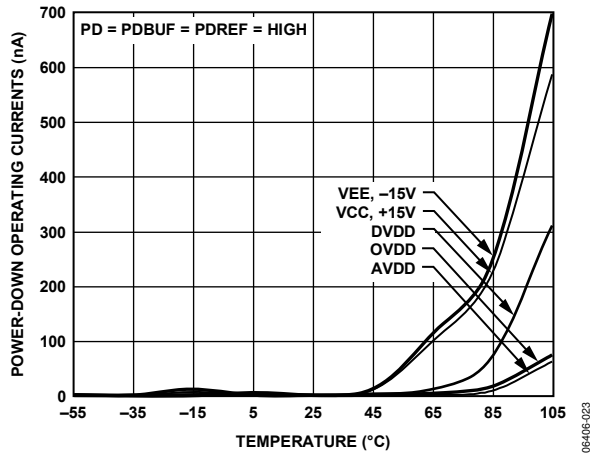


Figure 23. Power-Down Operating Currents vs. Temperature

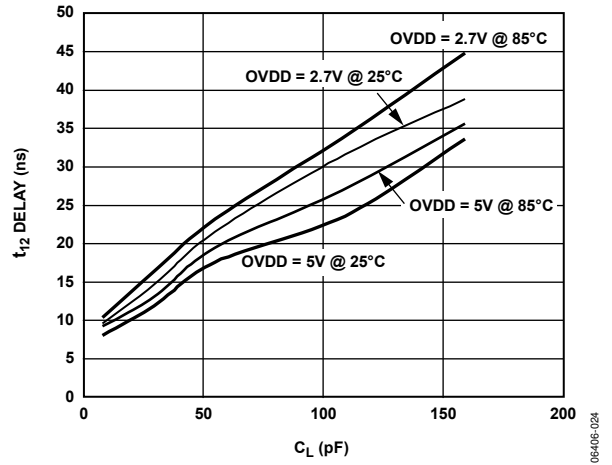


Figure 24. Typical Delay vs. Load Capacitance C<sub>L</sub>

## TERMINOLOGY

### Least Significant Bit (LSB)

The least significant bit, or LSB, is the smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is

$$LSB (V) = \frac{V_{INP-P}}{2^N}$$

### Integral Nonlinearity Error (INL)

Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full-scale. The point used as negative full scale occurs a ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSBs beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

### Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

### Bipolar Zero Error

The difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

### Unipolar Offset Error

The first transition should occur at a level ½ LSB above analog ground. The unipolar offset error is the deviation of the actual transition from that point.

### Full-Scale Error

The last transition (from 111...10 to 111...11 in straight binary format) should occur for an analog voltage 1½ LSB below the nominal full-scale. The full-scale error is the deviation in LSB (or % of full-scale range) of the actual level of the last transition from the ideal level and includes the effect of the offset error. Closely related is the gain error (also in LSB or % of full-scale range), which does not include the effects of the offset error.

### Dynamic Range

Dynamic range is the ratio of the rms value of the full scale to the rms noise measured for an input typically at –60 dB. The value for dynamic range is expressed in decibels.

### Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

### Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

### Signal-to-(Noise + Distortion) Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

### Spurious-Free Dynamic Range (SFDR)

The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

### Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD and is expressed in bits by

$$ENOB = [(SINAD_{dB} - 1.76)/6.02]$$

### Aperture Delay

Aperture delay is a measure of the acquisition performance measured from the falling edge of the CNVST input to when the input signal is held for a conversion.

### Transient Response

The time required for the AD7634 to achieve its rated accuracy after a full-scale step function is applied to its input.

### Reference Voltage Temperature Coefficient

Reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage ( $V_{REF}$ ) measured at  $T_{MIN}$ ,  $T(25^\circ\text{C})$ , and  $T_{MAX}$ . It is expressed in ppm/°C as

$$TCV_{REF} (\text{ppm}/^\circ\text{C}) = \frac{V_{REF} (Max) - V_{REF} (Min)}{V_{REF} (25^\circ\text{C}) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:

$V_{REF} (Max)$  = maximum  $V_{REF}$  at  $T_{MIN}$ ,  $T(25^\circ\text{C})$ , or  $T_{MAX}$ .

$V_{REF} (Min)$  = minimum  $V_{REF}$  at  $T_{MIN}$ ,  $T(25^\circ\text{C})$ , or  $T_{MAX}$ .

$V_{REF} (25^\circ\text{C})$  =  $V_{REF}$  at 25°C.

$T_{MAX}$  = +85°C.

$T_{MIN}$  = –40°C.

## THEORY OF OPERATION

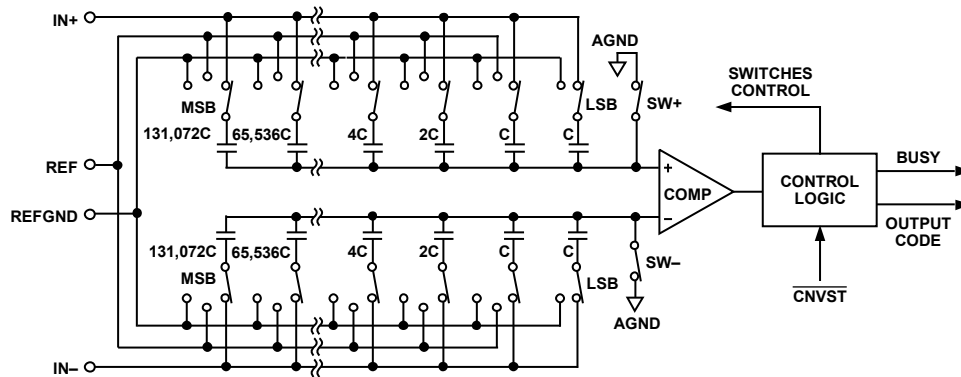


Figure 25. ADC Simplified Schematic

### OVERVIEW

The AD7634 is a very fast, low power, precise, 18-bit ADC using successive approximation capacitive digital-to-analog (CDAC) architecture.

The AD7634 can be configured at any time for one of four input ranges and conversion mode with inputs in parallel and serial hardware modes or by a dedicated write-only, SPI-compatible interface via a configuration register in serial software mode. The AD7634 uses Analog Devices' patented iCMOS high voltage process to accommodate 0 V to +5 V (10 V p-p), 0 V to +10 V (20 V p-p),  $\pm 5$  V (20 V p-p), and  $\pm 10$  V (40 V p-p) input ranges on the fully differential IN+ and IN- inputs without the use of conventional thin films. Only one acquisition cycle,  $t_s$ , is required for the inputs to latch to the correct configuration. Resetting or power cycling is not required for reconfiguring the ADC.

The AD7634 features different modes to optimize performance according to the applications. It is capable of converting 670,000 samples per second (670 kSPS) in warp mode, 570 kSPS in normal mode, and 450 kSPS in impulse mode.

The AD7634 provides the user with an on-chip, track-and-hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple, multiplexed channel applications.

For unipolar input ranges, the AD7634 typically requires three supplies: VCC, AVDD (which can supply DVDD), and OVDD (which can be interfaced to either 5 V, 3.3 V, or 2.5 V digital logic). For bipolar input ranges, the AD7634 requires the use of the additional VEE supply.

The device is housed in a Pb-free, 48-lead LQFP or a 48-lead tiny LFCSP (7 mm  $\times$  7 mm) that combine space savings with flexibility. In addition, the AD7634 can be configured as either a parallel or serial SPI-compatible interface.

### CONVERTER OPERATION

The AD7634 is a successive approximation ADC based on a charge redistribution DAC. Figure 25 shows the simplified schematic of the ADC. The CDAC consists of two identical arrays of 18 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to AGND via SW+ and SW-. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on IN+ and IN- inputs. A conversion phase is initiated once the acquisition phase is completed and the  $\overline{\text{CNVST}}$  input goes low. When the conversion phase begins, SW+ and SW- are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the REFGND input. Therefore, the differential voltage between the inputs (IN+ and IN-) captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFGND and REF, the comparator input varies by binary weighted voltage steps ( $V_{\text{REF}}/2$ ,  $V_{\text{REF}}/4$  through  $V_{\text{REF}}/262,144$ ). The control logic toggles these switches, starting with the MSB first, to bring the comparator back into a balanced condition.

After the completion of this process, the control logic generates the ADC output code and brings the BUSY output low.

### MODES OF OPERATION

The AD7634 features three modes of operation: warp, normal, and impulse. Each of these modes is more suitable to specific applications. The mode is configured with the input pins, WARP and IMPULSE, or via the configuration register. See Table 6 for the pin details; see the Hardware Configuration section and the Software Configuration section for programming the mode selection with either pins or configuration register. Note that when using the configuration register, the WARP and IMPULSE inputs are don't cares and should be tied to either high or low.

**Warp Mode**

Setting WARP = high and IMPULSE = low allows the fastest conversion rate of up to 670 kSPS. However, in this mode, the full-specified accuracy is guaranteed only when the time between conversions does not exceed 1 ms. If the time between two consecutive conversions is longer than 1 ms (after power-up), the first conversion result should be ignored because in warp mode, the ADC performs a background calibration during the SAR conversion process. This calibration can drift if the time between conversions exceeds 1 ms thus causing the first conversion to appear offset. This mode makes the AD7634 ideal for applications where both high accuracy and fast sample rate are required.

**Normal Mode**

Setting WARP = IMPULSE = low or WARP = IMPULSE = high allows the fastest mode (570 kSPS) without any limitation on time between conversions. This mode makes the AD7634 ideal for asynchronous applications such as data acquisition systems, where both high accuracy and fast sample rate are required.

**Impulse Mode**

Setting WARP = low and IMPULSE = high uses the lowest power dissipation mode and allows power savings between conversions. The maximum throughput in this mode is 450 kSPS, and in this mode, the ADC powers down circuits after conversion, making the AD7634 ideal for battery-powered applications.

**TRANSFER FUNCTIONS**

Except in 18-bit parallel interface mode, using the  $\overline{D0/OB/2C}$  digital input or via the configuration register, the AD7634 offers two output codings: straight binary and twos complement. See Figure 26 and Table 8 for the ideal transfer characteristic and digital output codes for the different analog input ranges,  $V_{IN}$ . Note that when using the configuration register, the  $\overline{D0/OB/2C}$  input is a don't care and should be tied to either high or low.

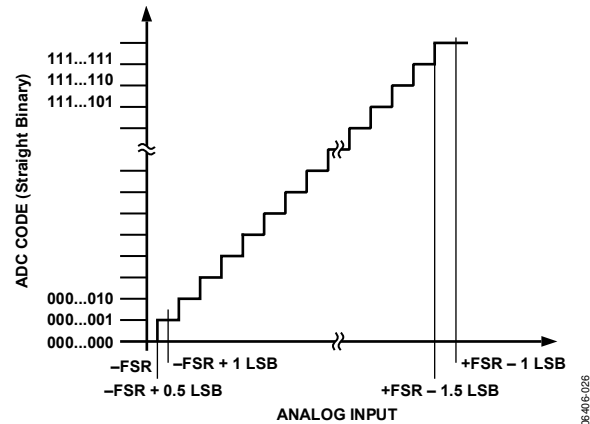


Figure 26. ADC Ideal Transfer Function

**Table 8. Output Codes and Ideal Input Voltages**

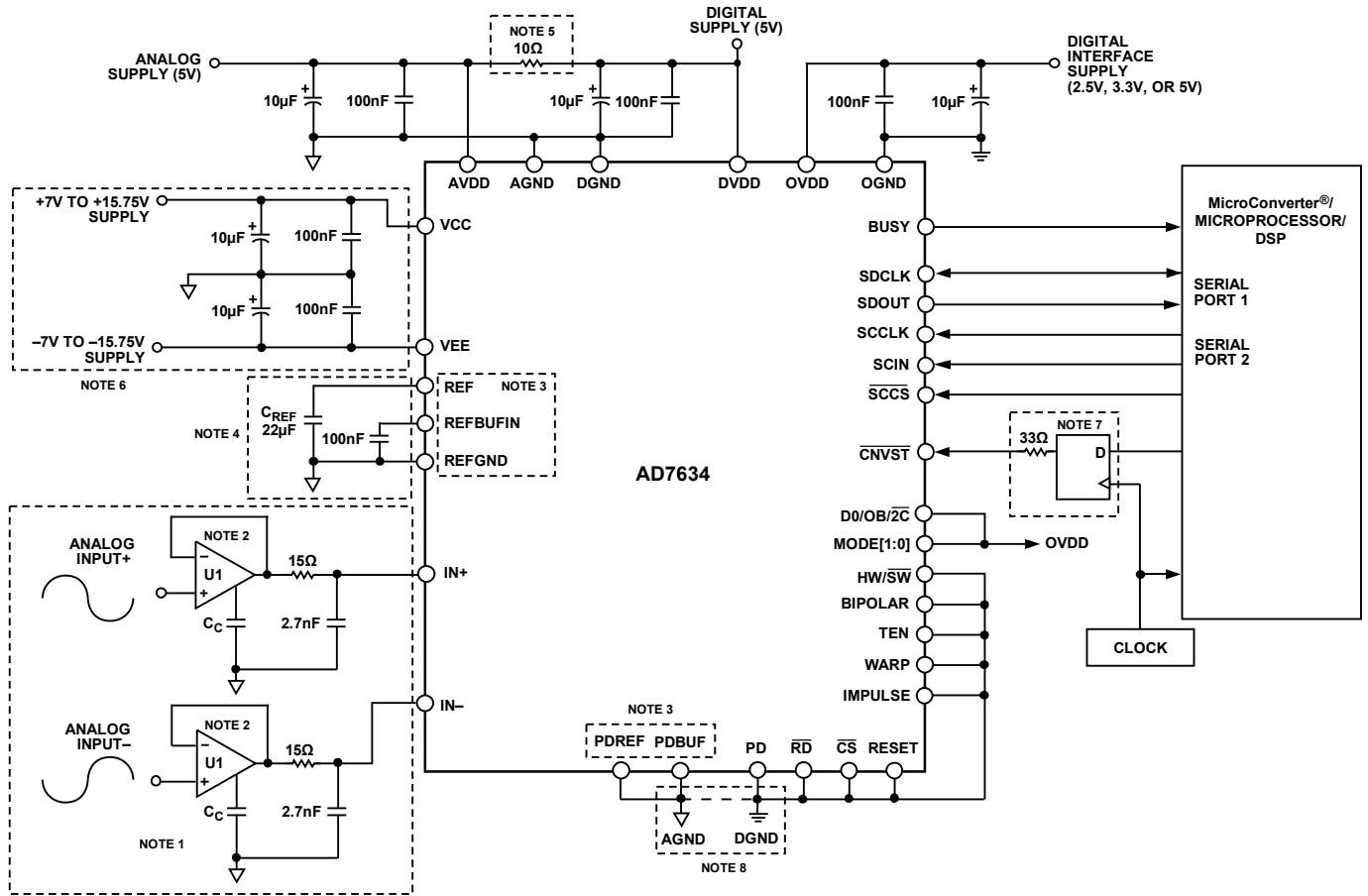
Description	$V_{REF} = 5\text{ V}$				Digital Output Code	
	$V_{IN} = 0\text{ V to }+5\text{ V}$ (10 V p-p)	$V_{IN} = 0\text{ V to }+10\text{ V}$ (20 V p-p)	$V_{IN} = \pm 5\text{ V}$ (20 V p-p)	$V_{IN} = \pm 10\text{ V}$ (40 V p-p)	Straight Binary	Twos Complement
FSR – 1 LSB	+4.999962 V	+9.999924 V	+9.999924 V	+19.999847 V	0x3FFFF <sup>1</sup>	0x1FFFF <sup>1</sup>
FSR – 2 LSB	+4.999924 V	+9.999847 V	+9.999847 V	+19.999695 V	0x3FFFE	0x1FFFE
Midscale + 1 LSB	+38.15 $\mu\text{V}$	–76.29 $\mu\text{V}$	–76.29 $\mu\text{V}$	+152.59 $\mu\text{V}$	0x20001	0x00001
Midscale	0 V	0 V	0 V	0 V	0x20000	0x00000
Midscale – 1 LSB	–38.15 $\mu\text{V}$	–76.29 $\mu\text{V}$	–76.29 $\mu\text{V}$	–152.59 $\mu\text{V}$	0x1FFFF	0x3FFFF
–FSR + 1 LSB	–4.999962 V	–9.999924 V	–9.999924 V	–19.999847 V	0x00001	0x20001
–FSR	–5 V	–10 V	–10 V	–20 V	0x00000 <sup>2</sup>	0x20000 <sup>2</sup>

<sup>1</sup> This is also the code for overrange analog input.

<sup>2</sup> This is also the code for underrange analog input.

TYPICAL CONNECTION DIAGRAM

Figure 27 shows a typical connection diagram for the AD7634 using the internal reference, serial data interface, and serial configuration port. Different circuitry from that shown in Figure 27 is optional and is discussed in the following sections.



- NOTES**
1. ANALOG INPUTS ARE DIFFERENTIAL (ANTIPHASE). SEE ANALOG INPUTS SECTION.
  2. THE AD8021 IS RECOMMENDED. SEE DRIVER AMPLIFIER CHOICE SECTION.
  3. THE CONFIGURATION SHOWN IS USING THE INTERNAL REFERENCE. SEE VOLTAGE REFERENCE INPUT/OUTPUT SECTION.
  4. A 22µF CERAMIC CAPACITOR (X5R, 1206 SIZE) IS RECOMMENDED (FOR EXAMPLE, PANASONIC ECJ4YB1A226M). SEE VOLTAGE REFERENCE INPUT/OUTPUT SECTION.
  5. OPTIONAL, SEE POWER SUPPLIES SECTION.
  6. THE VCC AND VEE SUPPLIES SHOULD BE VCC = [VIN(MAX) + 2V] AND VEE = [VIN(MIN) - 2V] FOR BIPOLAR INPUT RANGES. FOR UNIPOLAR INPUT RANGES, VEE CAN BE 0V. SEE POWER SUPPLIES SECTION.
  7. OPTIONAL LOW JITTER CNVST, SEE CONVERSION CONTROL SECTION.
  8. A SEPARATE ANALOG AND DIGITAL GROUND PLANE IS RECOMMENDED, CONNECTED TOGETHER DIRECTLY UNDER THE ADC. SEE LAYOUT GUIDELINES SECTION.

Figure 27. Typical Connection Diagram Shown with Serial Interface and Serial Programmable Port

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## ANALOG INPUTS

### Input Range Selection

In parallel mode and serial hardware mode, the input range is selected by using the BIPOLAR (bipolar) and TEN (10 V range) inputs. See Table 6 for pin details; see the Hardware Configuration section and the Software Configuration section for programming the mode selection with either pins or configuration register. Note that when using the configuration register, the BIPOLAR and TEN inputs are don't cares and should be tied to either high or low.

### Input Structure

Figure 28 shows an equivalent circuit for the input structure of the AD7634.

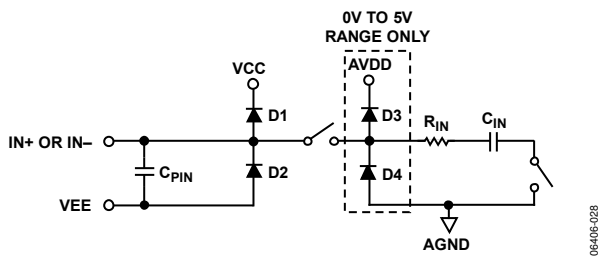


Figure 28. AD7634 Simplified Analog Input

The four diodes, D1 to D4, provide ESD protection for the analog inputs, IN+ and IN-. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V, because this causes the diodes to become forward-biased and to start conducting current. These diodes can handle a forward-biased current of 120 mA maximum. For instance, these conditions could eventually occur when the input buffer's U1 supplies are different from AVDD, VCC, and VEE. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part although most op amps' short-circuit current is <100 mA. Note that D3 and D4 are only used in the 0 V to 5 V range to allow for additional protection in applications that are switching from the higher voltage ranges.

This analog input structure of the AD7634 is a true differential structure allowing the sampling of the differential signal between IN+ and IN-. By using this differential input, small signals common to both inputs are rejected as shown in Figure 29, which represents the typical CMRR over frequency.

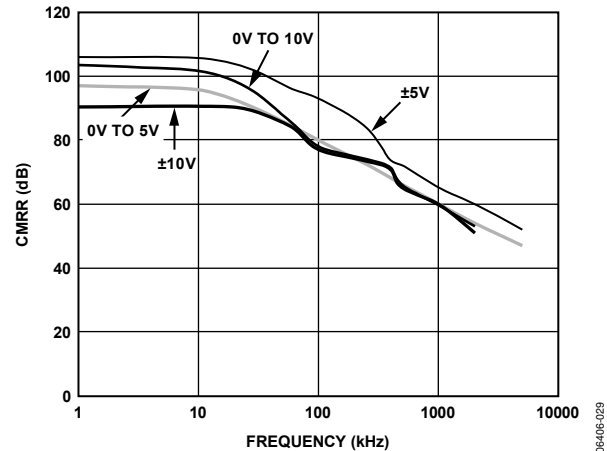


Figure 29. Analog Input CMRR vs. Frequency

During the acquisition phase for ac signals, the impedance of the analog inputs, IN+ and IN-, can be modeled as a parallel combination of Capacitor  $C_{PIN}$  and the network formed by the series connection of  $R_{IN}$  and  $C_{IN}$ .  $C_{PIN}$  is primarily the pin capacitance.  $R_{IN}$  is typically  $70 \Omega$  and is a lumped component comprised of serial resistors and the on resistance of the switches.  $C_{IN}$  is primarily the ADC sampling capacitor and depending on the input range selected is typically 48 pF in the 0 V to 5 V range, typically 24 pF in the 0 V to 10 V and  $\pm 5$  V ranges, and typically 12 pF in the  $\pm 10$  V range. During the conversion phase, when the switches are opened, the input impedance is limited to  $C_{PIN}$ .

Because the input impedance of the AD7634 is very high, it can be directly driven by a low impedance source without gain error. To further improve the noise filtering achieved by the AD7634 analog input circuit, an external, one-pole RC filter between the amplifier's outputs and the ADC analog inputs can be used, as shown in Figure 27. However, large source impedances significantly affect the ac performance, especially the THD. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency, as shown in Figure 30.

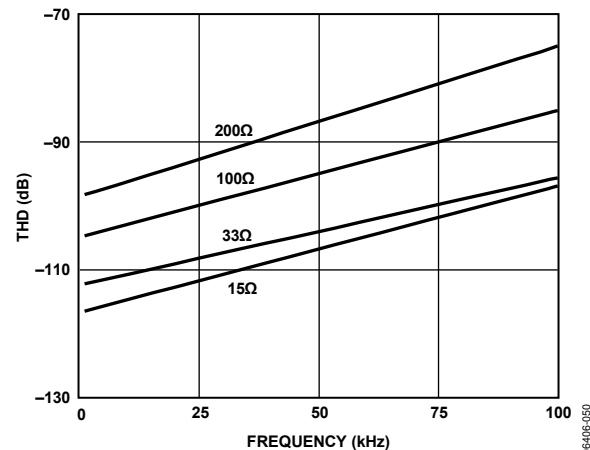


Figure 30. THD vs. Analog Input Frequency and Source Resistance

**DRIVER AMPLIFIER CHOICE**

Although the AD7634 is easy to drive, the driver amplifier must meet the following requirements:

- For multichannel, multiplexed applications, the driver amplifier and the AD7634 analog input circuit must be able to settle for a full-scale step of the capacitor array at a 18-bit level (0.0004%). For the amplifier, settling at 0.1% to 0.01% is more commonly specified. This differs significantly from the settling time at a 18-bit level and should be verified prior to driver selection. The AD8021 op amp combines ultra-low noise and high gain bandwidth and meets this settling time requirement even when used with gains of up to 13.
- The noise generated by the driver amplifier needs to be kept as low as possible to preserve the SNR and transition noise performance of the AD7634. The noise coming from the driver is filtered by the external 1-pole low-pass filter, as shown in Figure 27. The SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20 \log \left( \frac{V_{NADC}}{\sqrt{V_{NADC}^2 + \frac{\pi}{2} f_{-3dB} (Ne_{N+})^2 + \frac{\pi}{2} f_{-3dB} (Ne_{N-})^2}} \right)$$

where:

$V_{NADC}$  is the noise of the ADC, which is:

$$V_{NADC} = \frac{2V_{INP-P}}{10^{\frac{SNR}{20}}}$$

$f_{-3dB}$  is the cutoff frequency of the input filter (3.9 MHz).

$N$  is the noise factor of the amplifier (+1 in buffer configuration).

$e_{N+}$  and  $e_{N-}$  are the equivalent input voltage noise densities of the op amps connected to IN+ and IN-, in nV/ $\sqrt{Hz}$ .

This approximation can be utilized when the resistances used around the amplifiers are small. If larger resistances are used, their noise contributions should also be root-sum squared.

- The driver needs to have a THD performance suitable to that of the AD7634. Figure 15 shows the THD vs. frequency that the driver should exceed.

The AD8021 meets these requirements and is appropriate for almost all applications. The AD8021 needs a 10 pF external compensation capacitor that should have good linearity as an NPO ceramic or mica type. Moreover, the use of a noninverting +1 gain arrangement is recommended and helps to obtain the best signal-to-noise ratio.

The AD8022 can also be used when a dual version is needed and a gain of 1 is present. The AD829 is an alternative in applications where high frequency (above 100 kHz) performance is not required. In applications with a gain of 1, an 82 pF compensation

capacitor is required. The AD8610 is an option when low bias current is needed in low frequency applications.

Because the AD7634 uses a large geometry, high voltage input switch, the best linearity performance is obtained when using the amplifier at its maximum full power bandwidth. Gaining the amplifier to make use of the more dynamic range of the ADC results in increased linearity errors. For applications requiring more resolution, the use of an additional amplifier with gain should precede a unity follower driving the AD7634. See Table 9 for a list of recommended op amps.

**Table 9. Recommended Driver Amplifiers**

Amplifier	Typical Application
AD829	$\pm 15$ V supplies, very low noise, low frequency
AD8021	$\pm 12$ V supplies, very low noise, high frequency
AD8022	$\pm 12$ V supplies, very low noise, high frequency, dual
ADA4922-1	$\pm 12$ V supplies, low noise, high frequency, single-ended-to-differential driver
AD8610/ AD8620	$\pm 13$ V supplies, low bias current, low frequency, single/dual

**Single-to-Differential Driver**

For single-ended sources, a single-to-differential driver, such as the ADA4922-1, can be used because the AD7634 needs to be driven differentially. The 1-pole filter using  $R = 15 \Omega$  and  $C = 2.7$  nF provides a corner frequency of 3.9 MHz.

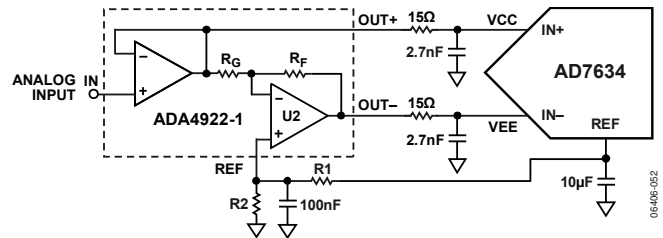


Figure 31. Single-to-Differential Driver Using the ADA4922-1

For unipolar 5 V and 10 V input ranges, the internal (or external) reference source can be used to level shift U2 for the correct input span. If using an external reference, the values for R1/R2 can be lowered to reduce resistive Johnson noise ( $1.29E - 10 \times \sqrt{R}$ ). For the bipolar  $\pm 5$  V and  $\pm 10$  V input ranges, the reference connection is not required because the common-mode voltage is 0 V. See Table 10 for R1/R2 for the different input ranges.

**Table 10. R1/R2 Configuration**

Input Range	R1	R2	Common-Mode Voltage
5 V	2.5 k $\Omega$	2.5 k $\Omega$	2.5 V
10 V	2.5 k $\Omega$	Open	5 V
$\pm 5$ V, $\pm 10$ V		100 $\Omega$	0 V

This circuit can also be made discretely, and thus more flexible, using any of the recommended low noise amplifiers in Table 9. Again, to preserve the SNR of the converter, the resistors,  $R_F$  and  $R_G$ , should be kept low.

## VOLTAGE REFERENCE INPUT/OUTPUT

The AD7634 allows the choice of either a very low temperature drift internal voltage reference, an external reference, or an external buffered reference.

The internal reference of the AD7634 provides excellent performance and can be used in almost all applications. However, the linearity performance is guaranteed only with an external reference.

### Internal Reference (REF = 5 V) (PDREF = Low, PDBUF = Low)

To use the internal reference, the PDREF and PDBUF inputs must be low. This enables the on-chip, band gap reference, buffer, and TEMP sensor, resulting in a 5.00 V reference on the REF pin.

The internal reference is temperature-compensated to 5.000 V  $\pm$  35 mV. The reference is trimmed to provide a typical drift of 3 ppm/ $^{\circ}$ C. This typical drift characteristic is shown in Figure 19.

### External 2.5 V Reference and Internal Buffer (REF = 5 V) (PDREF = High, PDBUF = Low)

To use an external reference with the internal buffer, PDREF should be high and PDBUF should be low. This powers down the internal reference and allows the 2.5 V reference to be applied to REFBUFIN producing 5 V on the REF pin. The internal reference buffer is useful in multiconverter applications because a buffer is typically required in these applications to avoid reference coupling amongst the different converters.

### External 5 V Reference (PDREF = High, PDBUF = High)

To use an external reference directly on the REF pin, PDREF and PDBUF should both be high. PDREF and PDBUF power down the internal reference and the internal reference buffer, respectively. For improved drift performance, an external reference, such as the ADR445 or ADR435, is recommended.

### Reference Decoupling

Whether using an internal or external reference, the AD7634 voltage reference input (REF) has a dynamic input impedance; therefore, it should be driven by a low impedance source with efficient decoupling between the REF and REFGND inputs. This decoupling depends on the choice of the voltage reference but usually consists of a low ESR capacitor connected to REF and REFGND with minimum parasitic inductance. A 22  $\mu$ F (X5R, 1206 size) ceramic chip capacitor (or 47  $\mu$ F low ESR tantalum capacitor) is appropriate when using either the internal reference or the ADR445/ADR435 external reference.

The placement of the reference decoupling is also important to the performance of the AD7634. The decoupling capacitor should be mounted on the same side as the ADC right at the REF pin with a thick PCB trace. The REFGND should also connect to the reference decoupling capacitor with the shortest distance and to the analog ground plane with several vias.

For applications that use multiple AD7634 or other PulSAR devices, it is more effective to use the internal reference buffer to buffer the external 2.5 V reference voltage.

The voltage reference temperature coefficient (TC) directly impacts full scale; therefore, in applications where full-scale accuracy matters, care must be taken with the TC. For instance, a  $\pm 4$  ppm/ $^{\circ}$ C TC of the reference changes full scale by  $\pm 1$  LSB/ $^{\circ}$ C.

### Temperature Sensor

The TEMP pin measures the temperature of the AD7634. To improve the calibration accuracy over the temperature range, the output of the TEMP pin is applied to one of the inputs of the analog switch (such as ADG779), and the ADC itself is used to measure its own temperature. This configuration is shown in Figure 32.

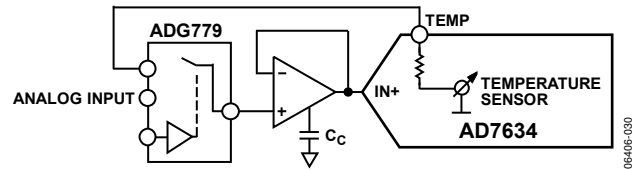


Figure 32. Use of the Temperature Sensor

## POWER SUPPLIES

The AD7634 uses five sets of power supply pins:

- AVDD: analog 5 V core supply
- VCC: analog high voltage positive supply
- VEE: high voltage negative supply
- DVDD: digital 5 V core supply
- OVDD: digital input/output interface supply

### Core Supplies

The AVDD and DVDD supply the AD7634 analog and digital cores, respectively. Sufficient decoupling of these supplies is required consisting of at least a 10  $\mu$ F capacitor and a 100 nF capacitor on each supply. The 100 nF capacitors should be placed as close as possible to the AD7634. To reduce the number of supplies needed, the DVDD can be supplied through a simple RC filter from the analog supply, as shown in Figure 27.

### High Voltage Supplies

The high voltage bipolar supplies, VCC and VEE, are required and must be at least 2 V larger than the maximum input voltage. For example, if using the  $\pm 10$  V range, the supplies should be  $\pm 12$  V minimum. This allows for 40 V p-p fully differential input ( $\pm 10$  V on each input IN+ and IN-). Sufficient decoupling of these supplies is also required consisting of at least a 10  $\mu$ F capacitor and a 100 nF capacitor on each supply. For unipolar operation, the VEE supply can be grounded with some slight THD performance degradation.

### Digital Output Supply

The OVDD supplies the digital outputs and allows direct interface with any logic working between 2.3 V and 5.25 V. OVDD should be set to the same level as the system interface. Sufficient decoupling is required consisting of at least a 10  $\mu$ F capacitor and a 100 nF



capacitor with the 100 nF capacitor placed as close as possible to the AD7634.

**Power Sequencing**

The AD7634 requires sequencing of the AVDD and DVDD supplies. AVDD should come up prior to or simultaneously with DVDD. This can be achieved using the configuration in Figure 27 or sequencing the supplies in that manner. The other supplies can be sequenced as desired as long as absolute maximum ratings are observed. The AD7634 is very insensitive to power supply variations on AVDD over a wide frequency range, as shown in Figure 33.

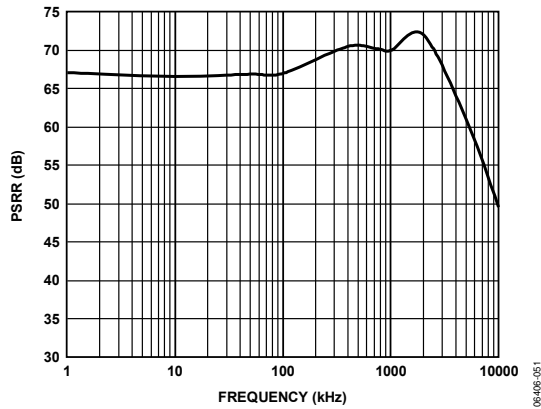


Figure 33. AVDD PSRR vs. Frequency

**Power Dissipation vs. Throughput**

In impulse mode, the AD7634 automatically reduces its power consumption at the end of each conversion phase. During the acquisition phase, the operating currents are very low, which allows a significant power savings when the conversion rate is reduced (see Figure 34). This feature makes the AD7634 ideal for very low power, battery-operated applications.

It should be noted that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, drive the digital inputs close to the power rails, that is, OVDD and OGND.

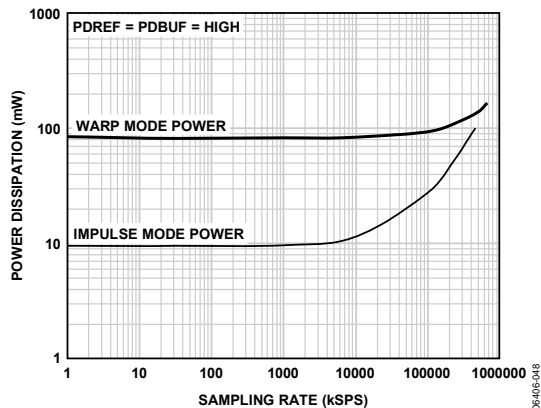


Figure 34. Power Dissipation vs. Sample Rate

**Power Down**

Setting PD = high powers down the AD7634, thus reducing supply currents to their minimums, as shown in Figure 23. When the ADC is in power down, the current conversion (if any) is completed and the digital bus remains active. To further reduce the digital supply currents, drive the inputs to OVDD or OGND.

Power down can also be programmed with the configuration register. See the Software Configuration section for details. Note that when using the configuration register, the PD input is a don't care and should be tied to either high or low.

**CONVERSION CONTROL**

The AD7634 is controlled by the  $\overline{\text{CNVST}}$  input. A falling edge on  $\overline{\text{CNVST}}$  is all that is necessary to initiate a conversion. A detailed timing diagram of the conversion process is shown in Figure 35. Once initiated, it cannot be restarted or aborted, even by the power-down input, PD, until the conversion is complete. The  $\overline{\text{CNVST}}$  signal operates independently of CS and RD signals.

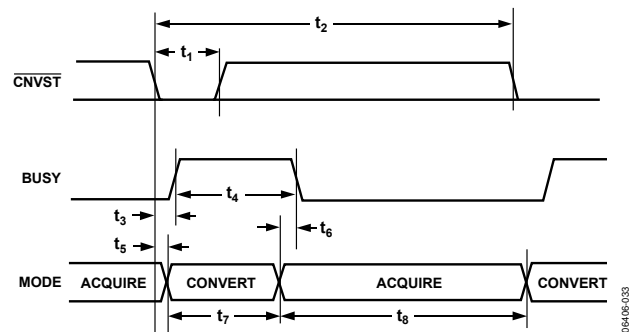


Figure 35. Basic Conversion Timing

Although  $\overline{\text{CNVST}}$  is a digital signal, it should be designed with special care with fast, clean edges and levels with minimum overshoot, undershoot, or ringing.

The  $\overline{\text{CNVST}}$  trace should be shielded with ground and a low value (such as 50  $\Omega$ ) serial resistor termination should be added close to the output of the component that drives this line.

For applications where SNR is critical, the  $\overline{\text{CNVST}}$  signal should have very low jitter. This can be achieved by using a dedicated oscillator for  $\overline{\text{CNVST}}$  generation, or by clocking  $\overline{\text{CNVST}}$  with a high frequency, low jitter clock, as shown in Figure 27.

## INTERFACES

### DIGITAL INTERFACE

The AD7634 has a versatile digital interface that can be set up as either a serial or a parallel interface with the host system. The serial interface is multiplexed on the parallel data bus. The AD7634 digital interface also accommodates 2.5 V, 3.3 V, or 5 V logic. In most applications, the OVDD supply pin is connected to the host system interface 2.5 V to 5.25 V digital supply. Finally, by using the D0/OB/2C input pin, both twos complement or straight binary coding can be used, except for in a 18-bit parallel interface.

Two signals,  $\overline{CS}$  and  $\overline{RD}$ , control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually,  $\overline{CS}$  allows the selection of each AD7634 in multicircuit applications and is held low in a single AD7634 design.  $\overline{RD}$  is generally used to enable the conversion result on the data bus.

### RESET

The RESET input is used to reset the AD7634. A rising edge on RESET aborts the current conversion (if any) and tristates the data bus. The falling edge of RESET resets the AD7634 and clears the data bus and configuration register. See Figure 36 for the RESET timing details.

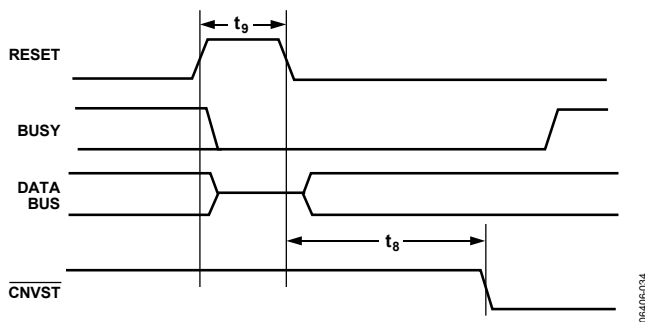


Figure 36. RESET Timing

### PARALLEL INTERFACE

The AD7634 is configured to use the parallel interface when the MODE[1:0] pins = 0, 1 or 2 for 18-/16-/8-bit interfaces, respectively, as detailed in Table 7.

#### Master Parallel Interface

Data can be continuously read by tying  $\overline{CS}$  and  $\overline{RD}$  low, thus requiring minimal microprocessor connections. However, in this mode, the data bus is always driven and cannot be used in shared bus applications (unless the device is held in RESET). Figure 37 details the timing for this mode.

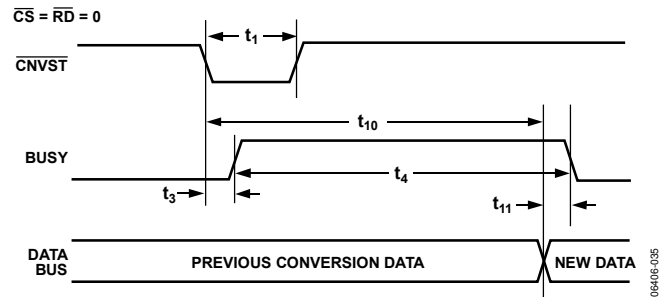


Figure 37. Master Parallel Data Timing for Reading (Continuous Read)

#### Slave Parallel Interface

In slave parallel reading mode, the data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion, as shown in Figure 38 and Figure 39, respectively. When the data is read during the conversion, it is recommended that it is read-only during the first half of the conversion phase. This avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

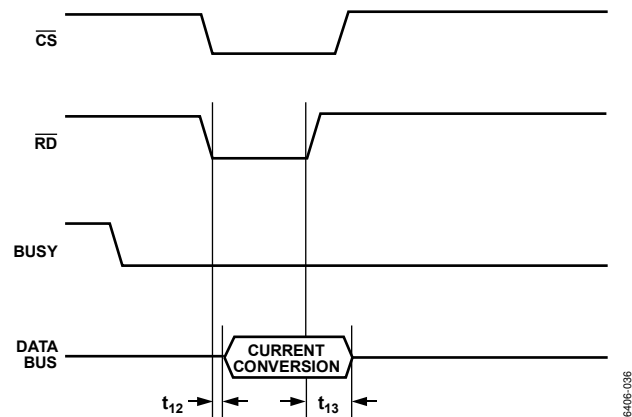


Figure 38. Slave Parallel Data Timing for Reading (Read After Convert)

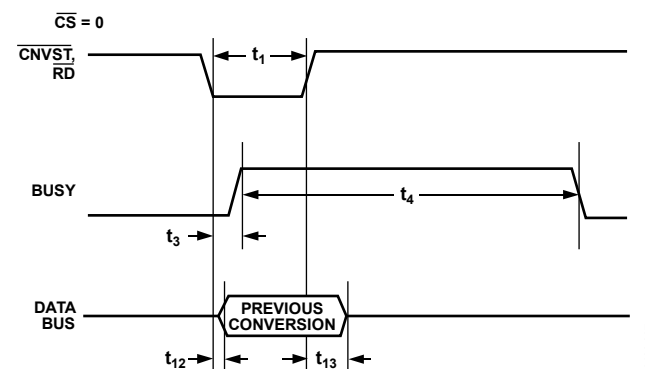


Figure 39. Slave Parallel Data Timing for Reading (Read During Convert)