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16-Bit, 1.5 LSB INL, 250 kSPS PulSAR Differential ADC in MSOP

Data Sheet **AD7687**

FEATURES

- 16-bit resolution with no missing codes
- Throughput: 250 kSPS
- INL: ±0.4 LSB typ, ±1.5 LSB max (±23 ppm of FSR)
- Dynamic range: 96.5 dB
- SNR: 95.5 dB at 20 kHz
- THD: −118 dB at 20 kHz
- True differential analog input range
  - $\pm V_{REF}$
  - 0 V to V_{REF} with V_{REF} up to VDD on both inputs
- No pipeline delay
- Single-supply 2.3 V to 5.5 V operation with
  - 1.8 V/2.5 V/3 V/5 V logic interface
- Proprietary serial interface: SPI/QSPI™/MICROWIRE/DSP compatible
- Daisy-chain multiple ADCs and BUSY indicator
- Power dissipation
  - 1.35 mW at 2.5 V/100 kSPS, 4 mW at 5 V/100 kSPS, and
  - 1.4 µW at 2.5 V/100 SPS
- Standby current: 1 nA
- 10-lead MSOP and 10-lead, 3 mm × 3 mm LFCSP
- Pin-for-pin compatible with AD7685, AD7686, and AD7688

APPLICATIONS

- Battery-powered equipment
- Data acquisitions
- Instrumentation
- Medical instruments
- Process controls

TYPICAL APPLICATION CIRCUIT

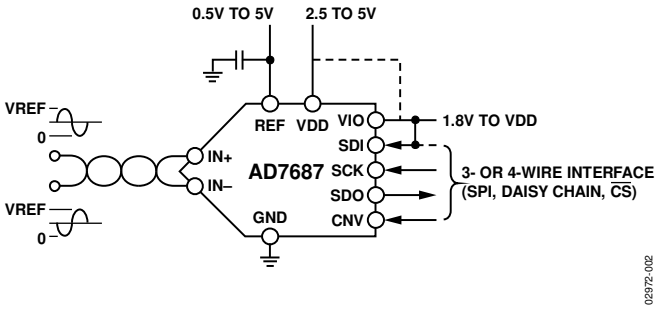

Figure 1.

GENERAL DESCRIPTION

The AD7687[1] is a 16-bit, charge redistribution, successive approximation, analog-to-digital converter (ADC) that operates from a single power supply, VDD, between 2.3 V to 5.5 V. It contains a low power, high speed, 16-bit sampling ADC with no missing codes, an internal conversion clock, and a versatile serial interface port. The device also contains a low noise, wide bandwidth, short aperture delay track-and-hold circuit. On the CNV rising edge, the AD7687 the samples the voltage difference between IN+ and IN− pins, which can range from $-V_{REF}$ to $+V_{REF}$. The reference voltage, V_{REF}, is applied externally and can be set up to the supply voltage.

The power consumption of the device scales linearly with throughput.

The SPI-compatible serial interface also features the ability to daisy-chain several ADCs on a single 3-wire bus and provides an optional BUSY indicator by means of the SDI pin. It is compatible with 1.8 V, 2.5 V, 3 V, or 5 V logic using the separate supply VIO.

The AD7687 comes in a 10-lead MSOP or a 10-lead LFCSP with operation specified from −40°C to +85°C.

Table 1. MSOP, LFCSP/SOT-23 16-Bit PulSAR® ADC

Type	100 kSPS	250 kSPS	500 kSPS
True Differential	AD7684	AD7687	AD7688
Pseudo Differential/Unipolar	AD7683	AD7685 AD7694	AD7686
Unipolar	AD7680		

[1] Protected by U.S. Patent 6,703,961.

Rev. E
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

AD7687* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7687 Evaluation Kit
- Precision ADC PMOD Compatible Boards

DOCUMENTATION

Application Notes

- AN-931: Understanding PulSAR ADC Support Circuitry
- AN-932: Power Supply Sequencing

Data Sheet

- AD7687: 16-Bit, 1.5 LSB INL, 250 kSPS PulSAR Differential ADC in MSOP Data Sheet

Product Highlight

- [NO TITLE FOUND] Product Highlight
- 8- to 18-Bit SAR ADCs ... From the Leader in High Performance Analog
- Lowest-Power 16-Bit ADC Optimizes Portable Designs (eeProductCenter, 10/4/2006)

User Guides

- UG-340: Evaluation Board for the 10-Lead Family 14-/16-/18-Bit PulSAR ADCs
- UG-682: 6-Lead SOT-23 ADC Driver for the 8-/10-Lead Family of 14-/16-/18-Bit PulSAR ADC Evaluation Boards

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD7687 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design
- BeMicro FPGA Project for AD7687 with Nios driver

TOOLS AND SIMULATIONS

- AD7685 IBIS Models

REFERENCE DESIGNS

- CN0225

REFERENCE MATERIALS

Technical Articles

- MS-1779: Nine Often Overlooked ADC Specifications
- MS-2210: Designing Power Supplies for High Speed ADC

Tutorials

- MT-074: Differential Drivers for Precision ADCs

DESIGN RESOURCES

- AD7687 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7687 EngineerZone Discussions.

SAMPLE AND BUY

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TECHNICAL SUPPORT

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REVISION HISTORY

12/15—Rev. D to Rev. E

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Change to Signal-to-(Noise + Distortion) Parameter, Table 2 4
Added Timing Diagrams Section 7
Moved Figure 2 and Figure 3 7
Changes to Table 8 9
Changes to Figure 7 Caption, Figure 8 Caption, Figure 10 Caption, and Figure 11 Caption 11
Added Theory of Operation Section 14
Changes to Analog Input Section 16
Changes to Drive Amplifier Choice Section, Table 10, Figure 30, Voltage Reference Input Section, and Power Supply Section 17
Changes to Supplying the ADC from the Reference Section and Digital Interface Section 18
Changed $\overline{CS}$ Mode, 3-Wire, No BUSY Indicator Section to $\overline{CS}$ Mode, 3-Wire Without BUSY Indicator Section 19
Changes to $\overline{CS}$ Mode, 3-Wire Without BUSY Indicator Section 19
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Changed Chain Mode, No BUSY Indicator Section to Chain Mode Without BUSY Indicator Section 23
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4/15—Rev. C to Rev. D

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7/14—Rev. B to Rev. C

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Changes to Table 6 7
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4/05—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.3 V to 5.5 V, VIO = 2.3 V to VDD, V_{REF} = VDD, T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	IN+ − IN−	$-V_{REF}$		$+V_{REF}$	V
Absolute Input Voltage	IN+ and IN−	−0.1		V_{REF} + 0.1	V
Common-Mode Input Range	IN+ and IN−	0	$V_{REF}/2$	$V_{REF}/2$ + 0.1	V
Analog Input CMRR	f_{IN} = 250 kHz		65		dB
Leakage Current at 25°C	Acquisition phase		1		nA
Input Impedance		See the Analog Input section			
ACCURACY					
No Missing Codes		16			Bits
Differential Linearity Error		−1	±0.4	+1	LSB[1]
Integral Linearity Error		−1.5	±0.4	+1.5	LSB
Transition Noise	REF = VDD = 5 V		0.35		LSB
Gain Error[2], T_{MIN} to T_{MAX}			±2	±6	LSB
Gain Error Temperature Drift			±0.3		ppm/°C
Offset Error[2], T_{MIN} to T_{MAX}	VDD = 4.5 V to 5.5 V		±0.1	±1.6	mV
	VDD = 2.3 V to 4.5 V		±0.7	±3.5	mV
Offset Temperature Drift			±0.3		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±0.05		LSB
THROUGHPUT					
Conversion Rate	VDD = 4.5 V to 5.5 V	0		250	kSPS
	VDD = 2.3 V to 4.5 V	0		200	kSPS
Transient Response	Full-scale step			1.8	µs
AC ACCURACY					
Dynamic Range	V_{REF} = 5 V	95.8	96.5		dB[3]
Signal-to-Noise Ratio	f_{IN} = 20 kHz, V_{REF} = 5 V	94	95.5		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V	92	92.5		dB
Spurious-Free Dynamic Range	f_{IN} = 20 kHz		−118		dB
Total Harmonic Distortion	f_{IN} = 20 kHz		−118		dB
Signal-to-(Noise + Distortion) Ratio	f_{IN} = 20 kHz, V_{REF} = 5 V	94	95		dB
	f_{IN} = 20 kHz, V_{REF} = 5 V, −60 dB input		36.5		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V	92	92.5		dB
Intermodulation Distortion[4]			115		dB

[1] LSB means least significant bit. With the ±5 V input range, one LSB is 152.6 µV.
[2] See the Terminology section. These specifications do include full temperature range variation but do not include the error contribution from the external reference.
[3] All specifications in dB are referred to a full-scale input FSR. Tested with an input signal at 0.5 dB below full-scale, unless otherwise specified.
[4] f_{IN1} = 21.4 kHz, f_{IN2} = 18.9 kHz, each tone at −7 dB below full-scale.

VDD = 2.3 V to 5.5 V, VIO = 2.3 V to VDD, V_{REF} = VDD, T_A = −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		0.5		VDD + 0.3	V
Load Current	250 kSPS, REF = 5 V		50		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			2		MHz
Aperture Delay	VDD = 5 V		2.5		ns
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.3 × VIO	V
V_{IH}		0.7 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format		Serial 16-bits twos complement			
Pipeline Delay		Conversion results available immediately after completed conversion			
V_{OL}	I_{SINK} = 500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD	Specified performance	2.3		5.5	V
VIO	Specified performance	2.3		VDD + 0.3	V
VIO Range		1.8		VDD + 0.3	V
Standby Current[1, 2]	VDD and VIO = 5 V, 25°C		1	50	nA
Power Dissipation	VDD = 2.5 V, 100 SPS throughput		1.4		µW
	VDD = 2.5 V, 100 kSPS throughput		1.35		mW
	VDD = 2.5 V, 200 kSPS throughput		2.7		mW
	VDD = 5 V, 100 kSPS throughput		4	5.5	mW
	VDD = 5 V, 250 kSPS throughput			12.5	mW
TEMPERATURE RANGE[3]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] With all digital inputs forced to VIO or GND as required.
[2] During acquisition phase.
[3] Contact sales for extended temperature range.

TIMING SPECIFICATIONS

−40°C to +85°C, VDD = 4.5 V to 5.5 V, VIO = 2.3 V to 5.5 V or VDD + 0.3 V, whichever is the lowest, unless otherwise stated.

See Figure 2 and Figure 3 for load conditions.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
CONVERSION TIME: CNV RISING EDGE TO DATA AVAILABLE	t_{CONV}	0.5		2.2	µs
ACQUISITION TIME	t_{ACQ}	1.8			µs
TIME BETWEEN CONVERSIONS	t_{CYC}	4			µs
CNV PULSE WIDTH ($\overline{CS}$ MODE)	t_{CNVH}	10			ns
SCK PERIOD	t_{SCK}				
$\overline{CS}$ Mode		15			ns
Chain Mode					
VIO Above 4.5 V		17			ns
VIO Above 3 V		18			ns
VIO Above 2.7 V		19			ns
VIO Above 2.3 V		20			ns
SCK TIME					
Low	t_{SCKL}	7			ns
High	t_{SCKH}	7			ns
SCK FALLING EDGE					
To Data Remains Valid	t_{HSDO}	5			
To Data Valid Delay	t_{DSDO}				
VIO Above 4.5 V				14	ns
VIO Above 3 V				15	ns
VIO Above 2.7 V				16	ns
VIO Above 2.3 V				17	ns
CNV OR SDI					
Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO Above 4.5 V				15	ns
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				22	ns
High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			25	ns
SDI					
Valid Setup Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{SSDICNV}$	15			ns
Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	0			ns
Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	3			ns
Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	4			ns
High to SDO High (Chain Mode with BUSY indicator)	$t_{DSDOSDI}$				
VIO Above 4.5 V				15	ns
VIO Above 2.3 V				26	ns
SCK					
Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	5			ns

−40°C to +85°C, VDD = 2.3 V to 4.5 V, VIO = 2.3 V to 4.5 V or VDD + 0.3 V, whichever is the lowest, unless otherwise stated.

See Figure 2 and Figure 3 for load conditions.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit
CONVERSION TIME: CNV RISING EDGE TO DATA AVAILABLE	t_{CONV}	0.7		3.2	µs
ACQUISITION TIME	t_{ACQ}	1.8			µs
TIME BETWEEN CONVERSIONS	t_{CYC}	5			µs
CNV PULSE WIDTH ($\overline{CS}$ MODE)	t_{CNVH}	10			ns
SCK PERIOD	t_{SCK}				
$\overline{CS}$ Mode		25			ns
Chain Mode					
VIO Above 3 V		29			ns
VIO Above 2.7 V		35			ns
VIO Above 2.3 V		40			ns
SCK TIME					
Low	t_{SCKL}	12			ns
High	t_{SCKH}	12			ns
SCK FALLING EDGE					
To Data Remains Valid	t_{HSDO}	5			
To Data Valid Delay	t_{DSDO}				
VIO Above 3 V				24	ns
VIO Above 2.7 V				30	ns
VIO Above 2.3 V				35	ns
CNV OR SDI					
Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				22	ns
High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			25	ns
SDI					
Valid Setup Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{SSDICNV}$	30			ns
Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	0			ns
Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	5			ns
Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	4			ns
High to SDO High (Chain Mode with BUSY indicator)	$t_{DSDOSDI}$			36	ns
SCK					
Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	8			ns

Timing Diagrams

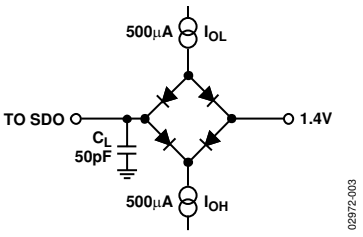

Figure 2. Load Circuit for Digital Interface Timing

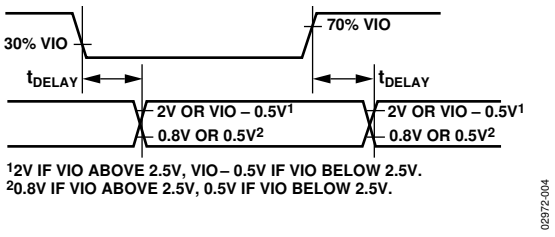

Figure 3. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Inputs	
IN+[1], IN−[1]	GND − 0.3 V to VDD + 0.3 V or ±130 mA
REF	GND − 0.3 V to VDD + 0.3 V
Supply Voltages	
VDD, VIO to GND	−0.3 V to +7 V
VDD to VIO	±7 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature Range	JEDEC J-STD-20

[1] See the Analog Input section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
10-Lead LFCSP	84	2.96	°C/W
10-Lead MSOP	200	44	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

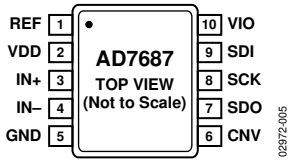

Figure 4. 10-Lead MSOP Pin Configuration

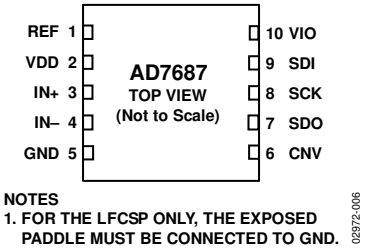

Figure 5. 10-Lead LFCSP Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Function
1	REF	AI	Reference Input Voltage. The REF range is from 0.5 V to VDD, referred to the GND pin. Place a 10 µF decoupling capacitor as close to the pin as possible.
2	VDD	P	Power Supply.
3	IN+	AI	Differential Positive Analog Input.
4	IN–	AI	Differential Negative Analog Input.
5	GND	P	Power Supply Ground.
6	CNV	DI	Convert Input. This input has multiple functions. On its leading edge, it initiates a conversion and selects the interface mode: chain or $\overline{CS}$ (depending on the state of SDI). In $\overline{CS}$ mode, CNV enables the SDO pin when low. In chain mode, the data is read while CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK. SDO also acts as the BUSY indicator if the feature is enabled.
8	SCK	DI	Serial Data Clock Input. This input primarily shifts data out on SDO when data is valid. In chain mode, the state of SCK determines if the BUSY indicator feature is enabled. If SCK is low during the CNV rising edge, the BUSY feature is disabled. If it is high during the CNV rising edge, the BUSY feature is enabled.
9	SDI	DI	Serial Data Input. This input serves multiple functions. It selects the interface mode of the ADC as follows: Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low, and if SDI or CNV is low when the conversion is complete, the BUSY indicator feature is enabled.
10	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
	EPAD	N/A	For the LFCSP only, the exposed paddle must be connected to GND.

[1]AI means analog input, DI means digital input, DO means digital output, P means power, and N/A means not applicable.

TERMINOLOGY

Integral Nonlinearity Error (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. Measure the deviation from the middle of each code to the true straight line (see Figure 25).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. The DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error
Zero error is the difference between the ideal midscale voltage, that is, 0 V, from the actual voltage producing the midscale output code, that is, 0 LSB.

Gain Error
The first transition (from 100…00 to 100…01) should occur at a level ½ LSB above nominal negative full scale (−4.999924 V for the ±5 V range). The last transition (from 011…10 to 011…11) should occur for an analog voltage 1½ LSB below the nominal full scale (+4.999771 V for the ±5 V range.) The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the following formula

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

and is expressed in bits.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in dB.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in dB.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in dB.

Aperture Delay
Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to acquire its input accurately after a full-scale step function is applied.

TYPICAL PERFORMANCE CHARACTERISTICS

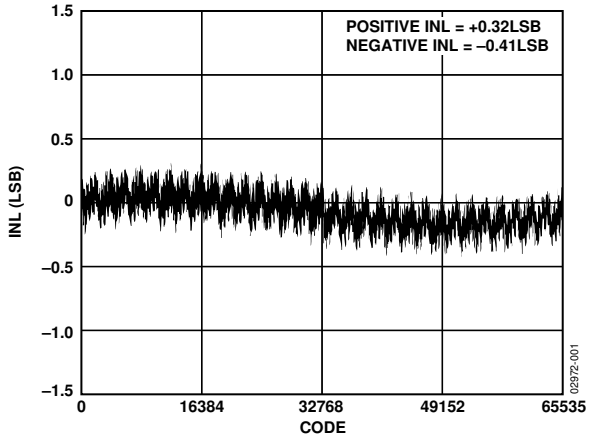

Figure 6. Integral Nonlinearity vs. Code

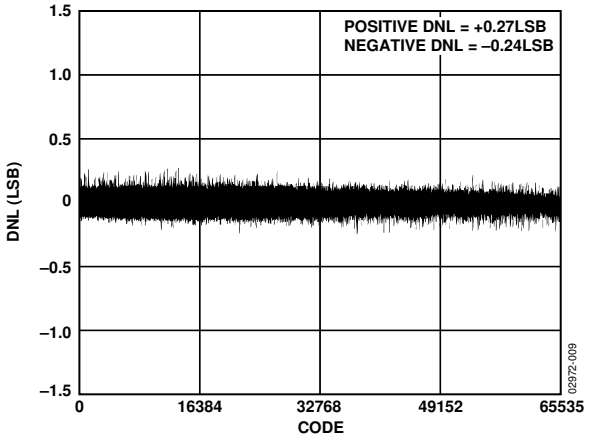

Figure 9. Differential Nonlinearity vs. Code

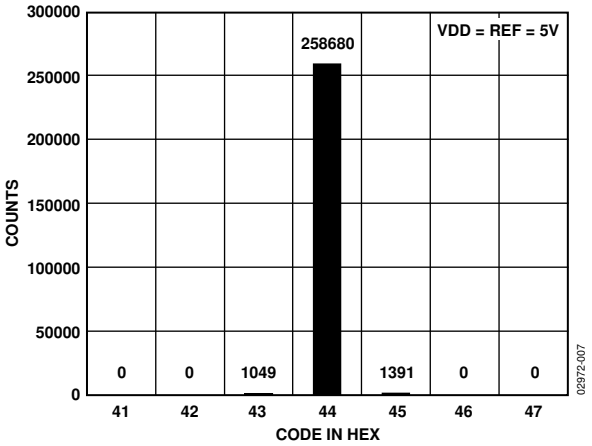

Figure 7. Histogram of a DC Input at the Code Center, VDD = REF = 5 V

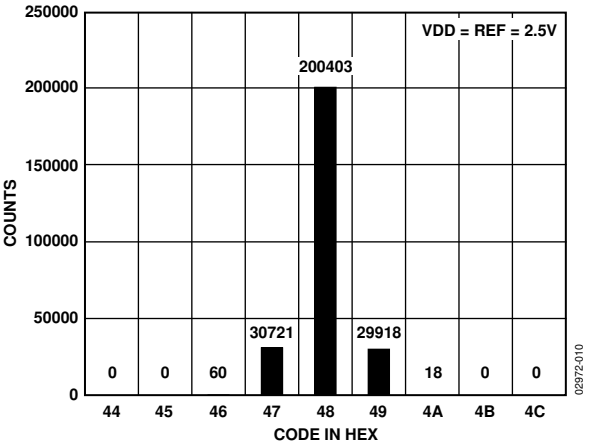

Figure 10. Histogram of a DC Input at the Code Center, VDD = REF = 2.5 V

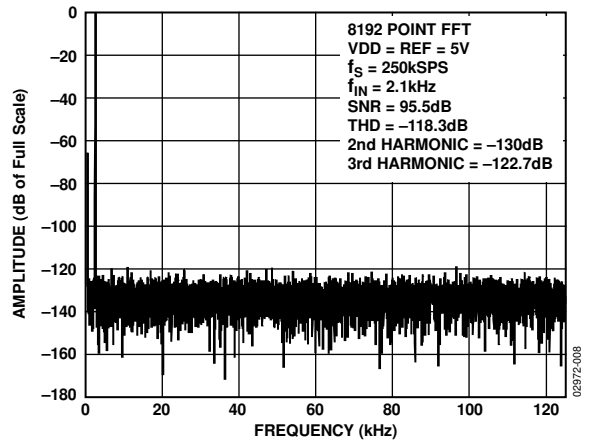

Figure 8. FFT Plot, VDD = REF = 5 V

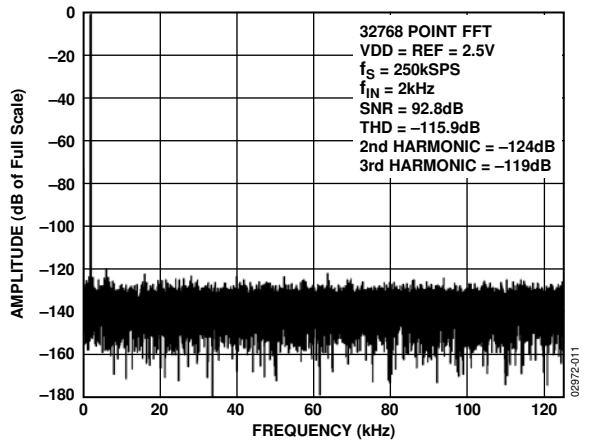

Figure 11. FFT Plot, VDD = REF = 2.5 V

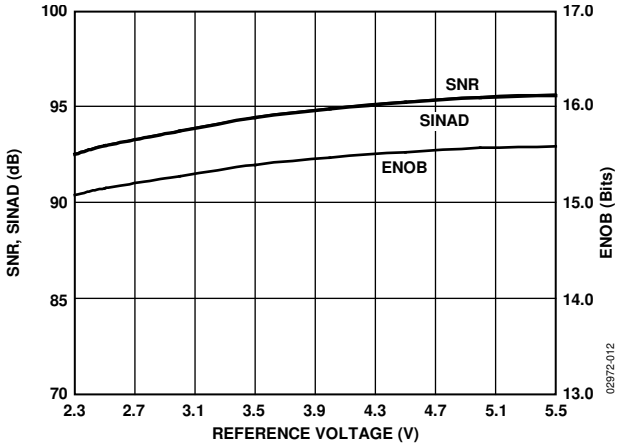

Figure 12. SNR, SINAD, and ENOB vs. Reference Voltage

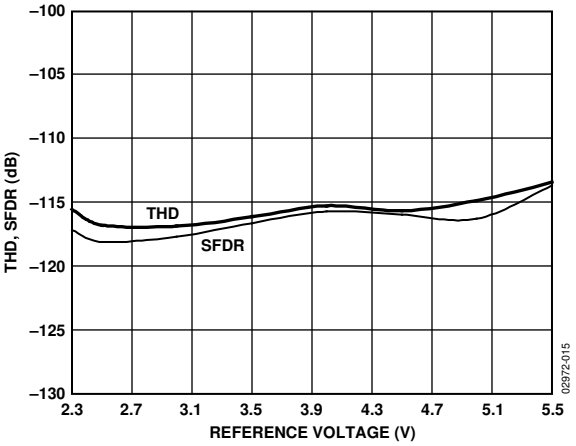

Figure 15. THD, SFDR vs. Reference Voltage

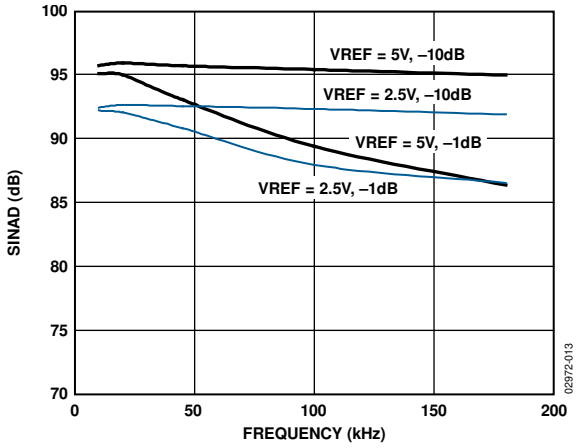

Figure 13. SINAD vs. Frequency

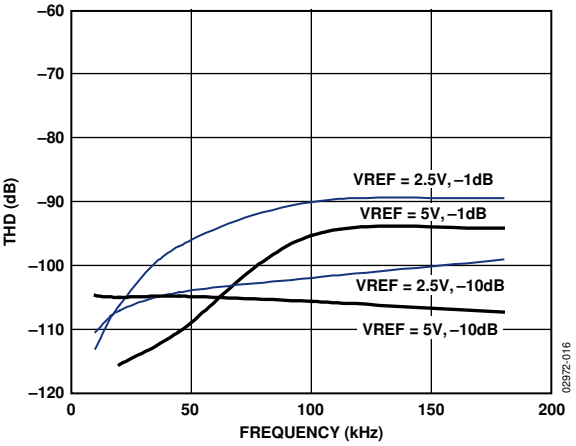

Figure 16. THD vs. Frequency

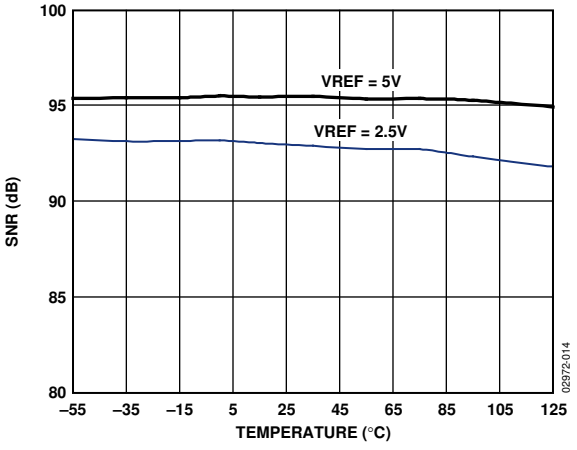

Figure 14. SNR vs. Temperature

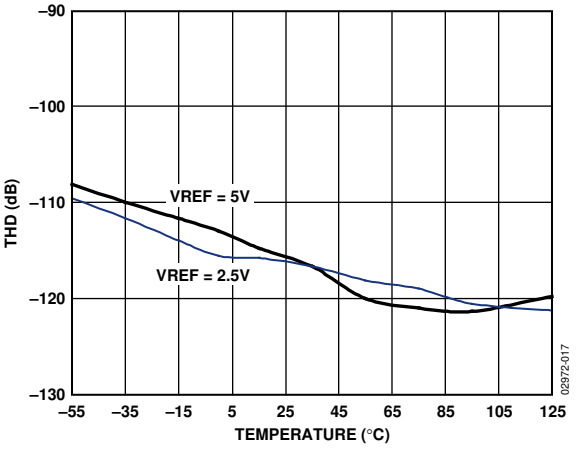

Figure 17. THD vs. Temperature

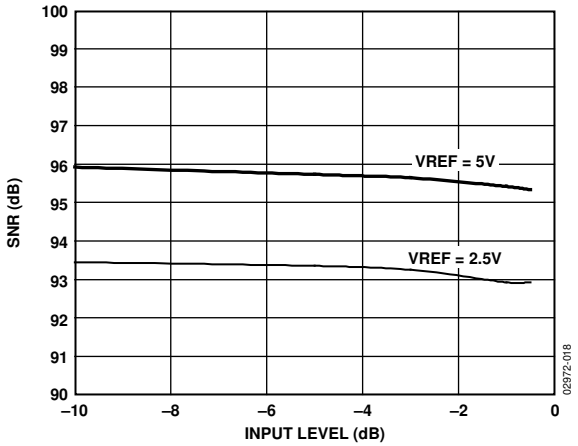

Figure 18. SNR vs. Input Level

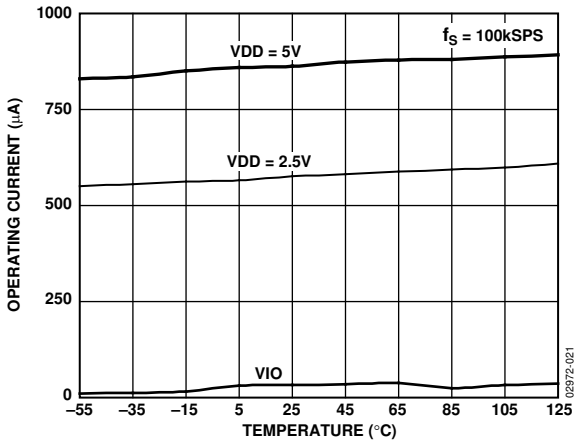

Figure 21. Operating Current vs. Temperature

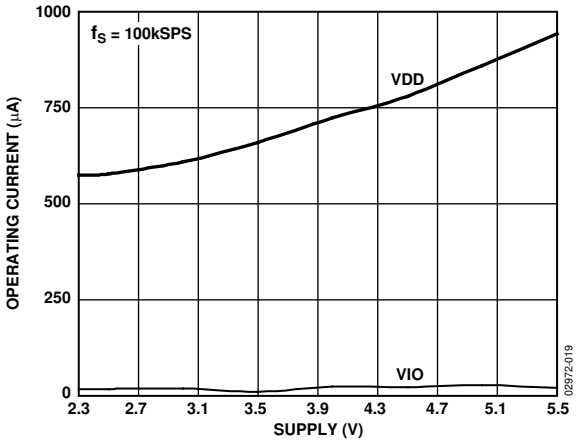

Figure 19. Operating Current vs. Supply

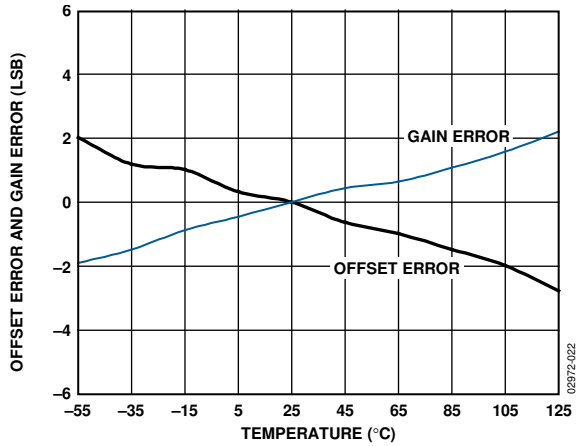

Figure 22. Offset Error and Gain Error vs. Temperature

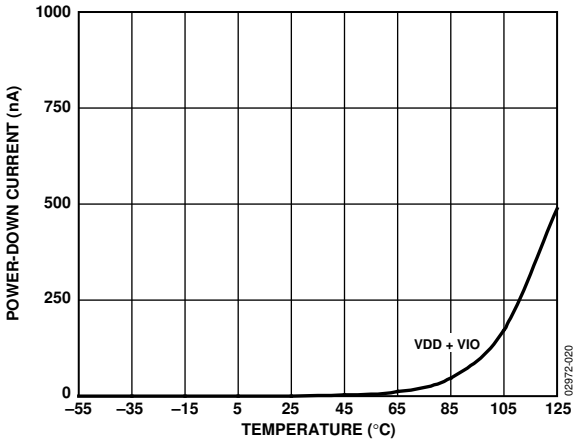

Figure 20. Power-Down Current vs. Temperature

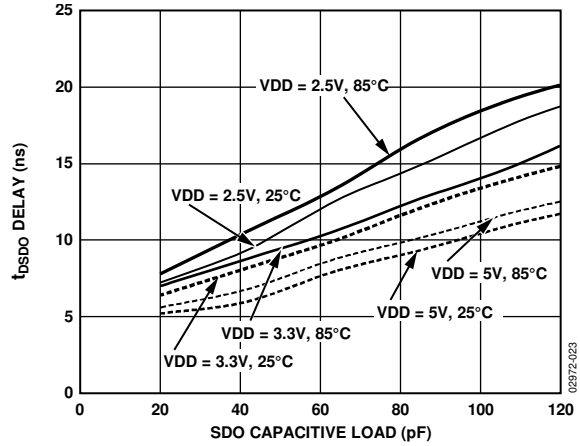

Figure 23. t_{DSDO} Delay vs. Capacitance Load and Supply

THEORY OF OPERATION

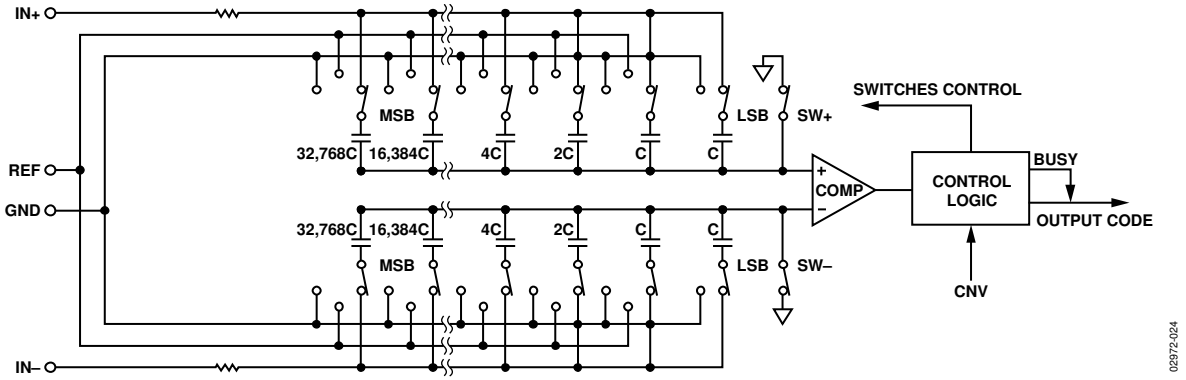

Figure 24. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7687 is a fast, low power, single-supply, precise 16-bit ADC using a successive approximation architecture.

The AD7687 is capable of converting 250,000 samples per second (250 kSPS) and powers down between conversions. When operating at 100 SPS, for example, it typically consumes 1.35 µW, which is ideal for battery-powered applications.

The AD7687 provides the user with an on-chip track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple multiplexed channel applications.

The AD7687 is specified for use from 2.3 V to 5.5 V and can be interfaced to any of the 1.8 V to 5 V digital logic family. It is housed in a 10-lead MSOP or in a tiny 10-lead LFCSP that saves space and allows flexible configurations.

It is pin-for-pin-compatible with the AD7685, AD7686, and AD7688.

CONVERTER OPERATION

The AD7687 is a successive approximation ADC based on a charge redistribution DAC. Figure 24 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the input of the comparator are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. Thus, the capacitor arrays function as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW− open first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs IN+ and IN− captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4 \ldots V_{REF}/65536$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the device returns to the acquisition phase and the control logic generates the ADC output code and a BUSY signal indicator.

Because the AD7687 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

Transfer Functions

Figure 25 and Table 9 show the ideal transfer characteristic for the AD7687.

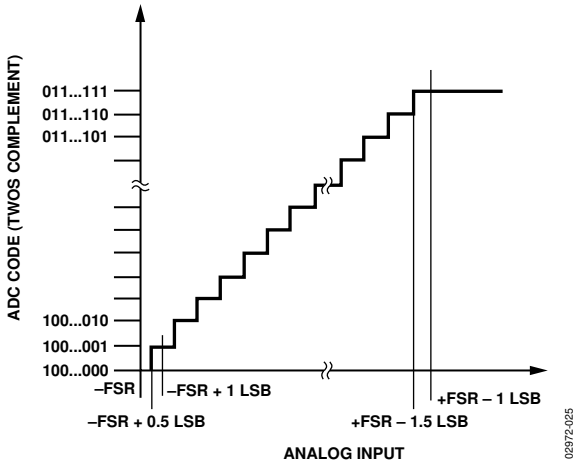

Figure 25. ADC Ideal Transfer Function

Table 9. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 5 V	Digital Output Code Hexadecimal
FSR – 1 LSB	+4.999847 V	7FFF[1]
Midscale + 1 LSB	+152.6 µV	0001
Midscale	0 V	0000
Midscale – 1 LSB	–152.6 µV	FFFF
–FSR + 1 LSB	–4.999847 V	8001
–FSR	–5 V	8000[2]

[1] This is also the code for an overranged analog input (V_{IN+} – V_{IN-} above V_{REF} – V_{GND}).
[2] This is also the code for an underranged analog input (V_{IN+} – V_{IN-} below –V_{REF} + V_{GND}).

TYPICAL CONNECTION DIAGRAM

Figure 26 shows an example of the recommended connection diagram for the AD7687 when multiple supplies are available.

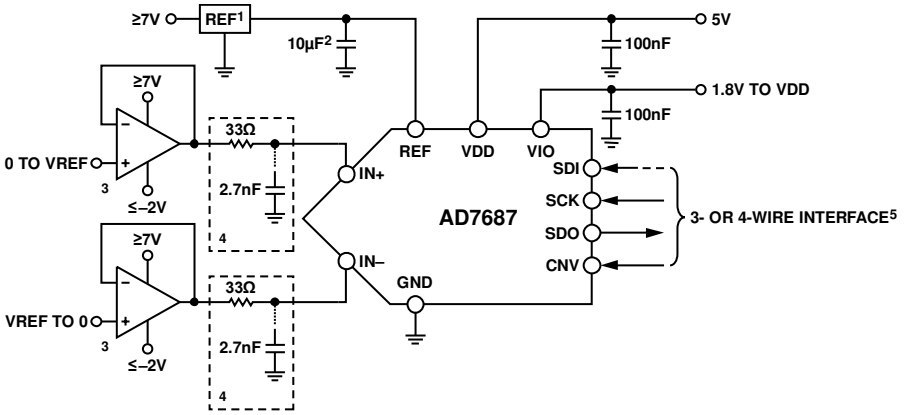

Figure 26. Typical Connection Diagram with Multiple Supplies

ANALOG INPUT

Figure 27 shows an equivalent circuit of the input structure of the AD7687.

The two diodes, D1 and D2, provide ESD protection for the analog inputs IN+ and IN−. Take care to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V because this causes these diodes to begin to forward-bias and start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. These overvoltage conditions can occur if the supplies of the input buffer (U1) differ from VDD. In such a case, use an input buffer with a short-circuit current limitation to protect the device.

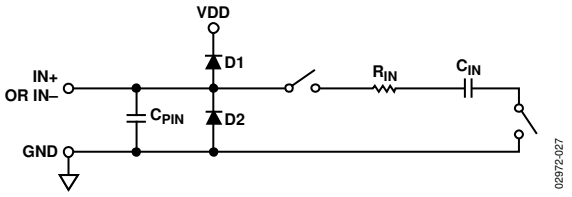

Figure 27. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. This differential input scheme allows for rejection of common-mode signals. Figure 28 shows the typical CMRR over frequency.

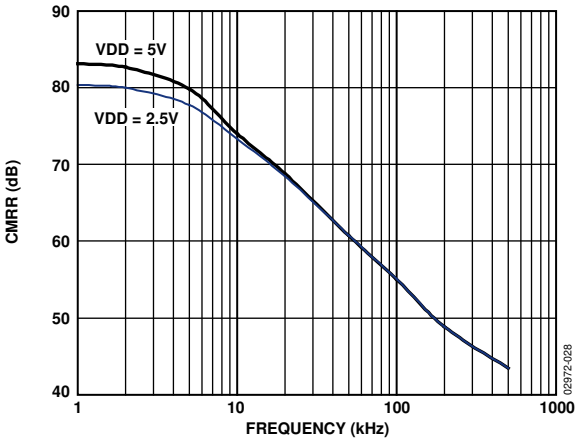

Figure 28. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog inputs (IN+ or IN−) can be modeled as a parallel combination of capacitor, C_{PIN}, and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 3 kΩ and is a lumped component made up of some serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor. During the conversion phase, where the switches are opened, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a 1-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise.

If the source impedance of the driving circuit is sufficiently low, the AD7687 can be driven directly. Large source impedances significantly affect the ac performance, especially the total harmonic distortion (THD). The maximum source impedance depends on the amount of THD that can be tolerated by the AD7687. The THD degrades as a function of the source impedance and the maximum input frequency, as shown in Figure 29.

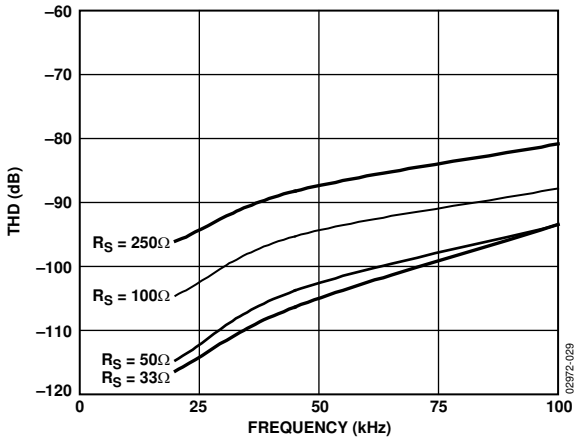

Figure 29. THD vs. Analog Input Frequency and Source Resistance

DRIVER AMPLIFIER CHOICE

Although the AD7687 is easy to drive, consider the following when selecting a driver amplifier.

The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7687. The AD7687 has a noise much lower than most of the other 16-bit ADCs and, therefore, can be driven by a noisier op amp while preserving the same or better system performance. The noise coming from the driver is filtered by the AD7687 analog input circuit 1-pole, low-pass filter made by R_{IN} and C_{IN} or by an external filter. Because the typical noise of the AD7687 is 53 µV rms, the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20\log\left(\frac{53}{\sqrt{53^2 + \frac{\pi}{2} f_{-3dB}(2Ne_N)^2}}\right)$$

where:

f_{-3dB} is either the input bandwidth in MHz of the AD7687 (2 MHz) or the cutoff frequency of an external filter, if one is used.
N is the noise gain of the amplifier (for example, +1 in buffer configuration).
e_N is the equivalent input noise voltage of the op amp, in nV/√Hz.

For ac applications, ensure that the THD performance of the driver is commensurate with the AD7687 and that the driver exceeds the THD vs. frequency shown in Figure 16.

For multichannel multiplexed applications, the driver amplifier and the AD7687 analog input circuit must settle a full-scale step onto the capacitor array at a 16-bit level (0.0015%, 15 ppm). Settling at 0.1% to 0.01% is more commonly specified in the amplifier data sheet. This can differ significantly from the settling time at a 16-bit level and must be verified prior to driver selection.

Table 10. Recommended Driver Amplifiers.

Amplifier	Typical Application
AD8021	Very low noise and high frequency
AD8022	Low noise and high frequency
AD8031	High frequency and low power
AD8519	Small, low power and low frequency
AD8605, AD8615	5 V single-supply, low power
AD8655	5 V single-supply, low noise
ADA4841-2	Very low noise, small, and low power
ADA4941-1	Very low noise, low power single-ended-to-differential
OP184	Low power, low noise, and low frequency

SINGLE-TO-DIFFERENTIAL DRIVER

For applications using a single-ended analog signal, either bipolar or unipolar, a single-ended-to-differential driver (like the one shown in Figure 30) allows for a differential input into the part. When provided a single-ended input signal, this configuration produces a differential $\pm V_{REF}$ with midscale at $V_{REF}/2$.

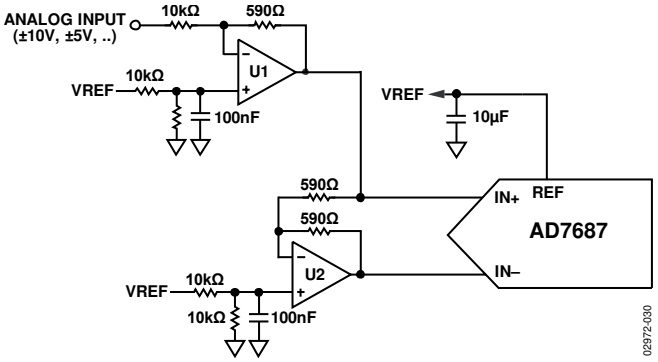

Figure 30. Single-Ended-to-Differential Driver Circuit

VOLTAGE REFERENCE INPUT

The AD7687 voltage reference input, REF, has a dynamic input impedance and must therefore be driven by a low impedance source with sufficient decoupling between the REF and GND pins (as explained in the Layout section).

For optimum performance, drive the REF pin with a low output impedance amplifier (such as the AD8031 or the AD8605) as a reference buffer with a 10 µF (X5R, 0805 size) ceramic chip decoupling capacitor.

If an unbuffered reference voltage is used, the decoupling value depends on the reference used. For instance, a 22 µF (X5R, 1206 size) ceramic chip capacitor is appropriate for optimum performance using a low temperature drift ADR431, ADR433, ADR434, or ADR435 reference.

If desired, smaller reference decoupling capacitor values down to 2.2 µF can be used with a minimal impact on performance, especially DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and GND pins.

POWER SUPPLY

The AD7687 is specified for use over a wide operating range of 2.3 V to 5.5 V. Unlike other low voltage converters, it has a low enough noise to design a 16-bit resolution system with low voltage supplies while maintaining respectable performance. It uses two power supply pins: a core supply, VDD, and a digital input/output interface supply, VIO. VIO allows direct interface with any logic between 1.8 V and VDD. VIO and VDD can be powered by the same source, reducing the number of supplies required in the overall design. The AD7687 is independent of power supply sequencing between VIO and VDD.

Additionally, it is resistant to power supply variations over a wide frequency range. Figure 31 shows the power supply rejection ration (PSRR) of the device over frequency.

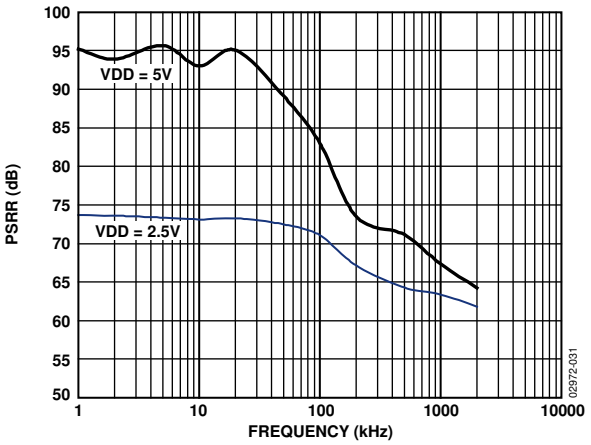

Figure 31. PSRR vs. Frequency

The AD7687 powers down automatically at the end of each conversion phase, and consequentially its power consumption scales linearly with the sampling rate, as shown in Figure 32. This makes the device ideal for low sampling rate (even a few SPS) and low battery-powered applications.

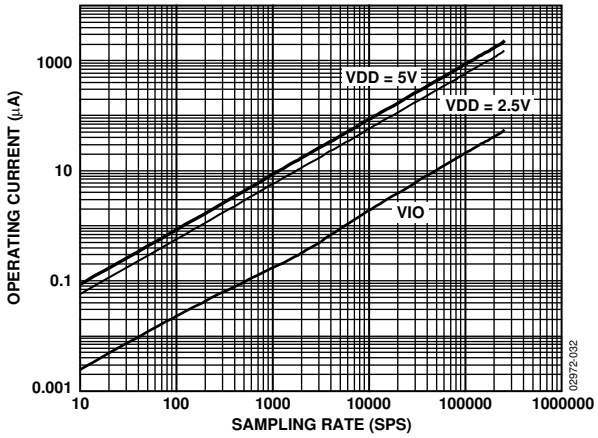

Figure 32. Operating Currents vs. Sampling Rate

SUPPLYING THE ADC FROM THE REFERENCE

With its low operating current, the AD7687 can be supplied directly by the reference circuitry (see Figure 33). The reference line is driven by one of the following:

- The system power supply directly.
- A reference voltage with enough current output capability, such as the ADR435.
- A reference buffer, such as the AD8031, which can also filter the system power supply (see Figure 33).

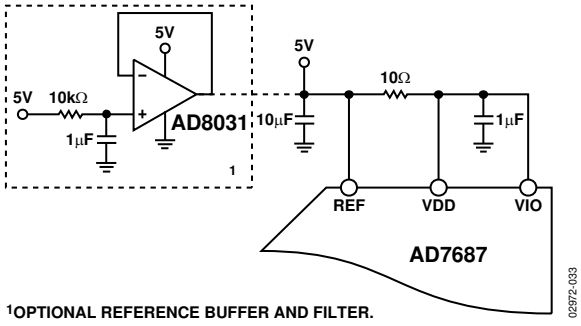

Figure 33. Example of Application Circuit

DIGITAL INTERFACE

Though the AD7687 has a reduced number of pins, it offers flexibility in its serial interface modes.

When in $\overline{CS}$ mode, the AD7687 is compatible with SPI, QSPI, digital hosts, and DSPs, such as the Blackfin® processors or the high performance, mixed-signal DSP family. In this mode, the AD7687 uses either a 3-wire or a 4-wire interface. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections and is useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). This is useful in low jitter sampling or simultaneous sampling applications.

When in chain mode, the AD7687 provides a daisy chain feature using the SDI input for cascading multiple ADCs on a single data line similar to a shift register.

The mode in which the device operates depends on the SDI level when the CNV rising edge occurs. The $\overline{CS}$ mode is selected if SDI is high, and the chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected together, the chain mode is always selected.

The initial state of SDO on power up is indeterminate. Therefore, to put SDO in a known state, initiate a conversion and clock out all data bits.

In either mode, the AD7687 offers the option of forcing a start bit in front of the data bits. Use this start bit as a BUSY signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a BUSY indicator, the user must time out the maximum conversion time prior to readback.

The BUSY indicator feature is enabled

- In the $\overline{CS}$ mode if CNV or SDI is low when the ADC conversion ends (see Figure 37 and Figure 41).
- In the chain mode if SCK is high during the CNV rising edge (see Figure 45).

$\overline{CS}$ MODE, 3-WIRE WITHOUT BUSY INDICATOR

This mode is usually used when a single AD7687 is connected to an SPI-compatible digital host. Figure 34 shows the connection diagram and Figure 35 gives the corresponding timing.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. Once a conversion is initiated, it continues to completion irrespective of the state of CNV. For instance, it can be useful to bring CNV low to select other SPI devices, such as analog multiplexers, but CNV must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid the generation of the BUSY signal indicator (see t_{CONV} in Table 5). When the conversion is complete, the AD7687 enters the acquisition phase and powers down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate (provided it has an acceptable hold time). After the 16th SCK falling edge, or when CNV goes high, whichever is earlier, SDO returns to high impedance.

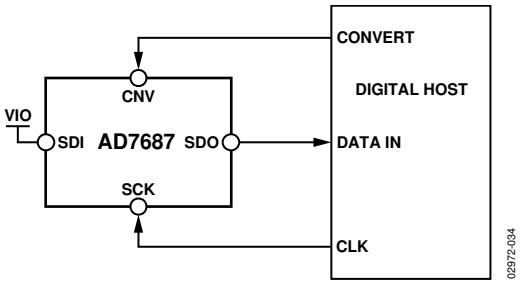

Figure 34. $\overline{CS}$ Mode, 3-Wire Without BUSY Indicator Connection Diagram (SDI High)

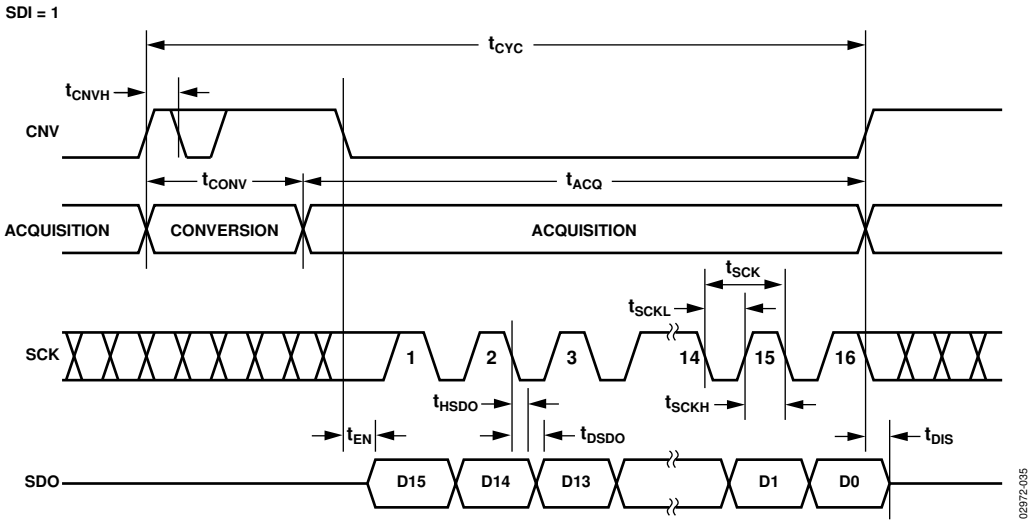

Figure 35. $\overline{CS}$ Mode, 3-Wire Without BUSY Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE, 3-WIRE WITH BUSY INDICATOR

This mode is usually used when a single AD7687 is connected to an SPI-compatible digital host having an interrupt input.

Figure 36 shows the connection diagram and Figure 37 gives the corresponding timing.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion irrespective of the state of CNV. Prior to the minimum conversion time, CNV can be used to select other SPI devices, such as analog multiplexers, but CNV must be returned low before the minimum conversion time and held low until the maximum conversion time to guarantee the generation of the BUSY signal indicator (see t_{CONV} in Table 5). When the conversion is complete, SDO goes from high to low impedance. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. When using this option, select the value of the pull-up resistor such that it maintains an appropriate rise time on the SDO line for the application. This is a function of the resistance of the pull-up and the capacitance of the SDO line. The AD7687 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate (provided it has an acceptable hold time). After the optional 17th SCK falling edge, or when CNV goes high, whichever is earlier, SDO returns to high impedance.

If multiple AD7687 devices are selected at the same time, the SDO output pin handles this contention without damage or induced latch-up. Keep this contention as short as possible to limit extra power dissipation.

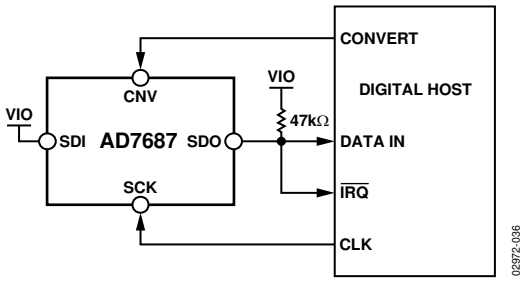

Figure 36. $\overline{CS}$ Mode, 3-Wire with BUSY Indicator Connection Diagram (SDI High)

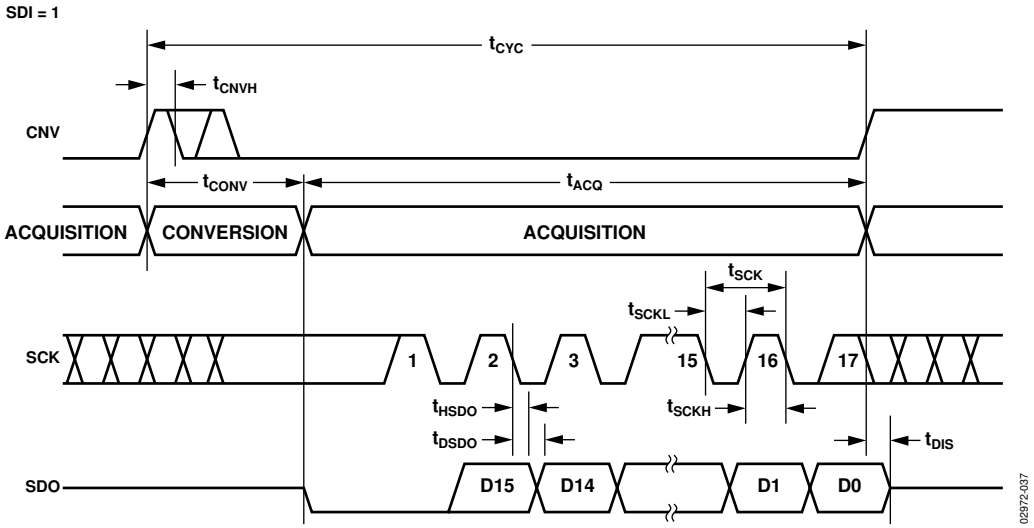

Figure 37. $\overline{CS}$ Mode, 3-Wire with BUSY Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE, 4-WIRE WITHOUT BUSY INDICATOR

This mode is usually used when multiple AD7687 devices are connected to an SPI-compatible digital host.

Figure 38 shows a connection diagram example using two AD7687 devices and Figure 39 gives the corresponding timing.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI can be used to select other SPI devices, such as analog multiplexers, but SDI must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid the generation of the BUSY signal indicator. When the conversion is complete, the AD7687 enters the acquisition phase and powers down. Each ADC result can be read by bringing low its SDI input, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate (provided it has an acceptable hold time). After the 16th SCK falling edge, or when SDI goes high, whichever is earlier, SDO returns to high impedance and another AD7687 can be read.

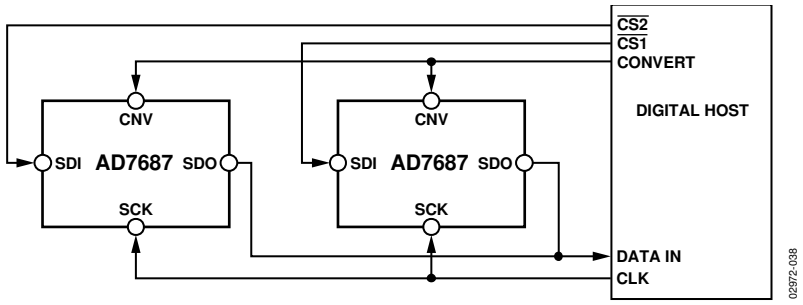

Figure 38. $\overline{CS}$ Mode, 4-Wire Without BUSY Indicator Connection Diagram

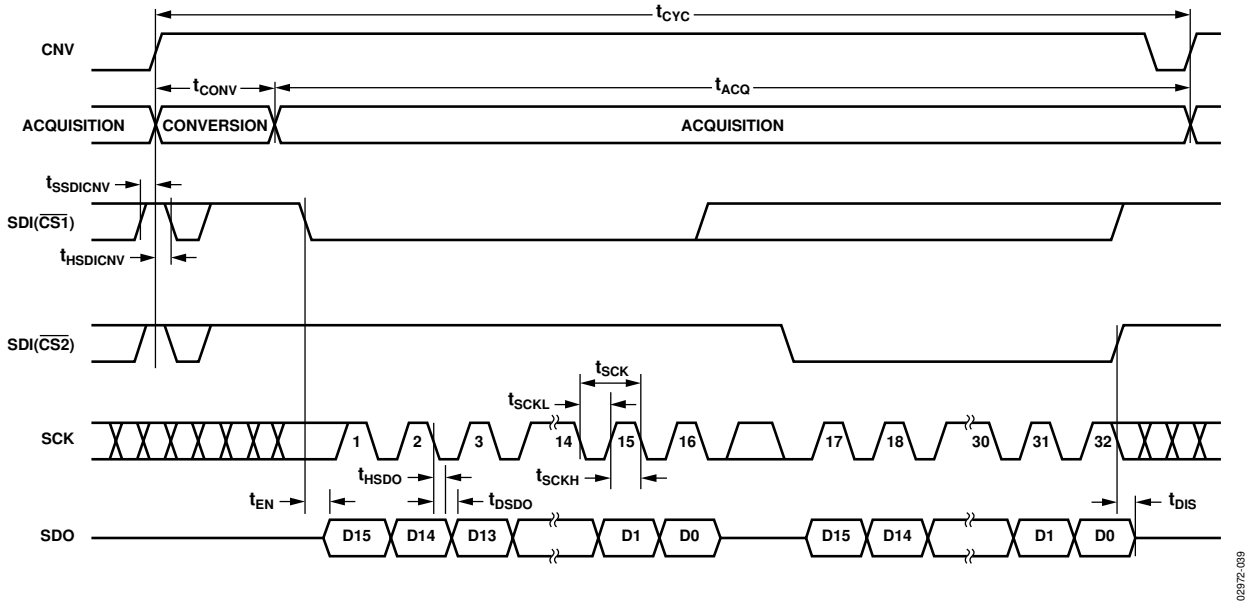

Figure 39. $\overline{CS}$ Mode, 4-Wire Without BUSY Indicator Serial Interface Timing

$\overline{CS}$ MODE, 4-WIRE WITH BUSY INDICATOR

This mode is usually used when a single AD7687 is connected to an SPI-compatible digital host, which has an interrupt input, and it is desired to keep CNV, which is used to sample the analog input, independent of the signal used to select the data reading. This requirement is particularly important in applications where low jitter on CNV is desired.

Figure 40 shows the connection diagram and Figure 41 gives the corresponding timing.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI can select other SPI devices, such as analog multiplexers, but SDI must be returned low before the minimum conversion time and held low until the maximum conversion time to guarantee the generation of the BUSY signal indicator. When the conversion is complete, SDO goes from high to low impedance. With a pull-up on the SDO line, this transition can act as an interrupt signal to initiate the data readback controlled by the digital host.

When using this option, select the value of the pull-up resistor such that it maintains an appropriate rise time on the SDO line for the application. This is a function of the resistance of the pull-up and the capacitance of the SDO line. The AD7687 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate (provided it has an acceptable hold time). After the optional 17th SCK falling edge, or SDI going high, whichever is earlier, the SDO returns to high impedance.

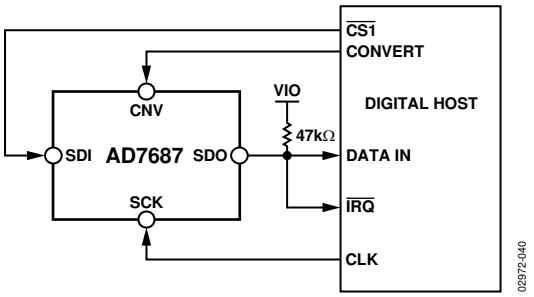

Figure 40. $\overline{CS}$ Mode, 4-Wire with BUSY Indicator Connection Diagram

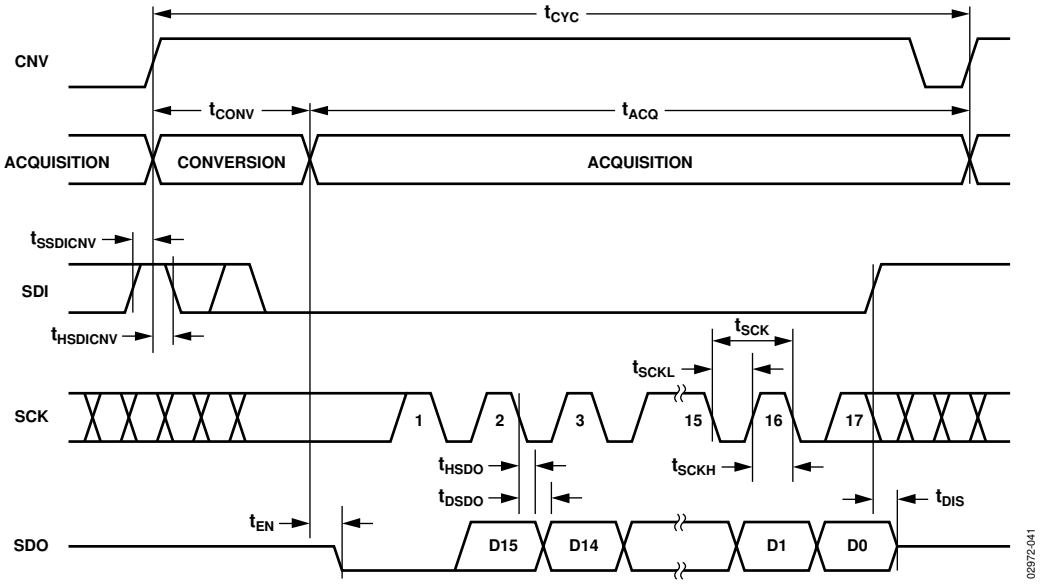

Figure 41. $\overline{CS}$ Mode, 4-Wire with BUSY Indicator Serial Interface Timing

CHAIN MODE WITHOUT BUSY INDICATOR

Use this mode to daisy-chain multiple AD7687 devices on a 3-wire serial interface. This feature is useful for reducing component count and wiring connections, for isolated multiconverter applications, or for systems with a limited interfacing capacity (for example). Data readback is analogous to clocking a shift register.

Figure 42 shows a connection diagram example using two AD7687 devices and Figure 43 gives the corresponding timing.

When SDI and CNV are low, SDO is driven low. With SDI and SCK low, a rising edge on CNV initiates a conversion, selects the chain mode, and disables the BUSY indicator. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO and the AD7687 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are then shifted out by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register; these data bits are also shifted in by the SCK falling edge. Each of the N ADCs in the chain outputs its data MSB first. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate and, consequently, more AD7687 devices in the chain (provided the digital host has an acceptable hold time). After the 16 × Nth SCK falling edge or CNV rising edge, whichever is earlier, SDO is driven low again. The maximum conversion rate can be reduced due to the total readback time. For example, using a digital host with a 3 ns set-up time and 3 V interface, up to eight AD7687 devices daisy-chained on a 3-wire port can be run at a maximum effective conversion rate of 220 kSPS.

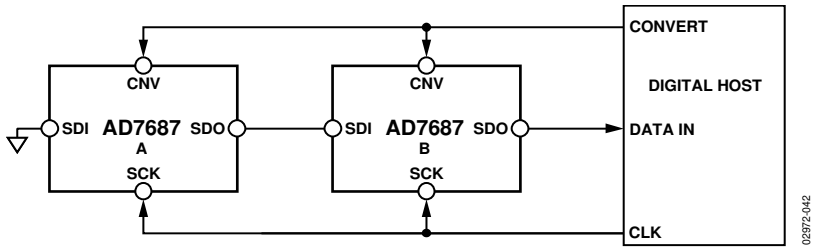

Figure 42. Chain Mode Without BUSY Indicator Connection Diagram

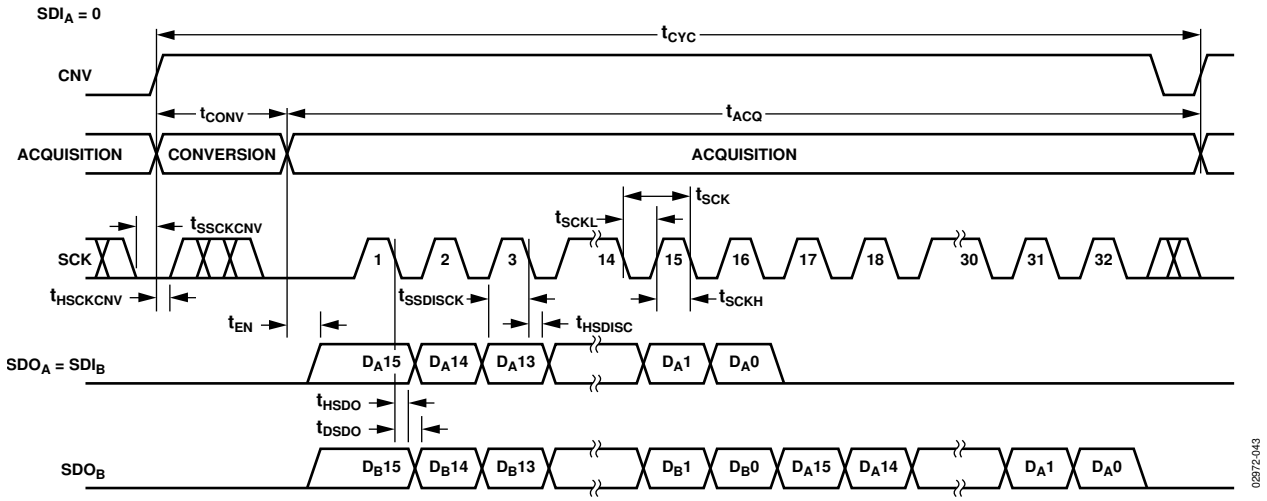

Figure 43. Chain Mode Without BUSY Indicator Serial Interface Timing

CHAIN MODE WITH BUSY INDICATOR

This mode can also be used to daisy-chain multiple AD7687 devices on a 3-wire serial interface while providing a BUSY indicator. This feature is useful for reducing component count and wiring connections, for isolated multiconverter applications or for systems with a limited interfacing capacity (for example). Data readback is analogous to clocking a shift register.

Figure 44 shows a connection diagram example using three AD7687 devices, and Figure 45 gives the corresponding timing.

When SDI and CNV are low, SDO is driven low. With SDI low and SCK high, a rising edge on CNV initiates a conversion, selects the chain mode, and enables the BUSY indicator feature. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When all ADCs in the chain have completed their conversions, the SDO pin of the ADC closest to the digital host (see the AD7687 C in Figure 44) is driven high. This transition on SDO can act as a BUSY indicator to trigger the data readback controlled by the digital host. The AD7687 then enters the acquisition phase and powers down. The data bits stored in the internal shift register are then clocked out, MSB first, by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register; these data bits are also shifted in by the SCK falling edge. Each of the N ADCs in the chain outputs its data MSB first. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate and, consequently, more AD7687 devices in the chain (provided the digital host has an acceptable hold time). After the optional (16 × N) + 1th SCK falling edge or CNV rising edge, whichever is earlier, SDO is driven low again. The maximum conversion rate may be reduced due to the total readback time. For example, using a digital host with a 3 ns set-up time and 3 V interface, up to eight AD7687 devices daisy-chained on a 3-wire port can be run at a maximum effective conversion rate of 220 kSPS.

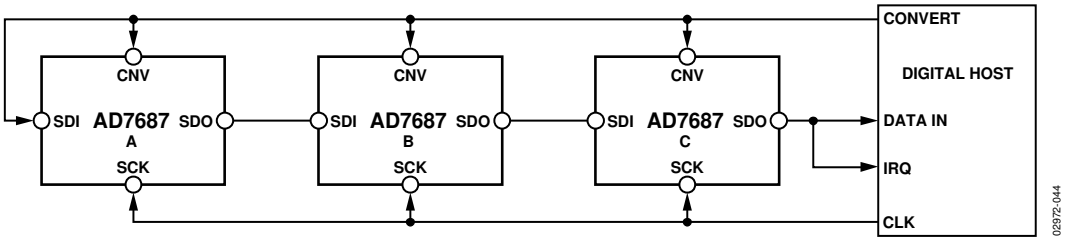

Figure 44. Chain Mode with BUSY Indicator Connection Diagram

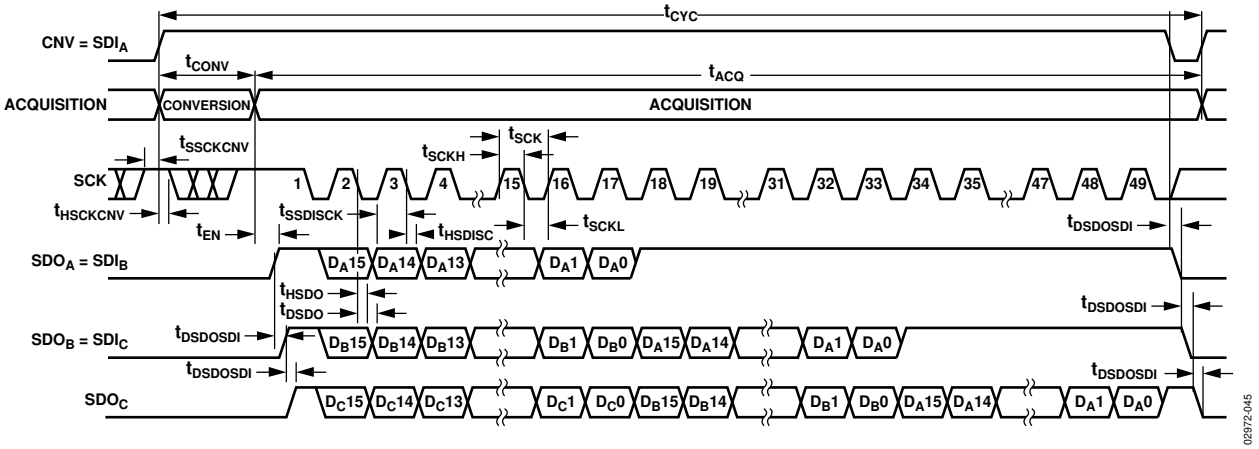

Figure 45. Chain Mode with BUSY Indicator Serial Interface Timing