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16-Bit, 4-Channel/8-Channel, 250 kSPS PulSAR ADC

Data Sheet **AD7682/AD7689**

FEATURES

- 16-bit resolution with no missing codes
- 4-channel (AD7682)/8-channel (AD7689) multiplexer with choice of inputs
- Unipolar single-ended
- Differential (GND sense)
- Pseudobipolar
- Throughput: 250 kSPS
- INL: ±0.4 LSB typical, ±1.5 LSB maximum (±23 ppm or FSR)
- Dynamic range: 93.8 dB
- SINAD: 92.5 dB at 20 kHz
- THD: −100 dB at 20 kHz
- Analog input range: 0 V to V_{REF} with V_{REF} up to VDD
- Multiple reference types
  - Internal selectable 2.5 V or 4.096 V
  - External buffered (up to 4.096 V)
  - External (up to VDD)
- Internal temperature sensor (TEMP)
- Channel sequencer, selectable 1-pole filter, busy indicator
- No pipeline delay, SAR architecture
- Single-supply 2.3 V to 5.5 V operation with 1.8 V to 5.5 V logic interface
- Serial interface compatible with SPI, MICROWIRE, QSPI, and DSP
- Power dissipation
  - 3.5 mW at 2.5 V/200 kSPS
  - 12.5 mW at 5 V/250 kSPS
- Standby current: 50 nA
- Low cost grade available
- 20-lead 4 mm × 4 mm LFCSP package
- 20-lead 2.4 mm × 2.4 mm WLCSP package

APPLICATIONS

- Multichannel system monitoring
- Battery-powered equipment
- Medical instruments: ECG/EKG
- Mobile communications: GPS
- Power line monitoring
- Data acquisition
- Seismic data acquisition systems
- Instrumentation
- Process control

FUNCTIONAL BLOCK DIAGRAM

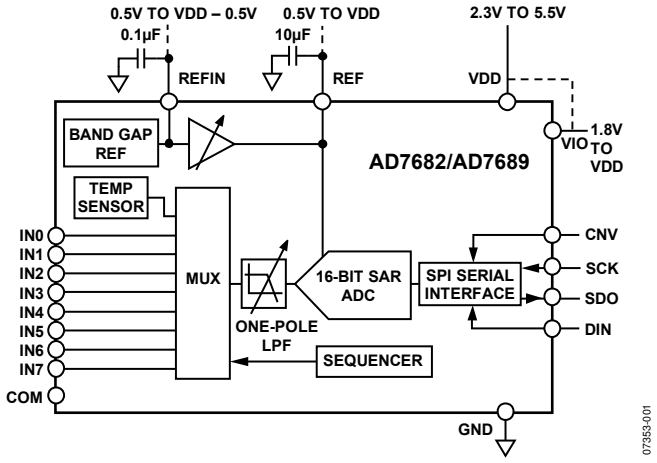

Figure 1.

GENERAL DESCRIPTION

The AD7682/AD7689 are 4-channel/8-channel, 16-bit, charge redistribution successive approximation register (SAR) analog-to-digital converters (ADCs) that operate from a single power supply, VDD.

The AD7682/AD7689 contain all components for use in a multichannel, low power data acquisition system, including a true 16-bit SAR ADC with no missing codes; a 4-channel (AD7682) or 8-channel (AD7689) low crosstalk multiplexer that is useful for configuring the inputs as single-ended (with or without ground sense), differential, or bipolar; an internal low drift reference (selectable 2.5 V or 4.096 V) and buffer; a temperature sensor; a selectable one-pole filter; and a sequencer that is useful when channels are continuously scanned in order.

The AD7682/AD7689 use a simple SPI interface for writing to the configuration register and receiving conversion results. The SPI interface uses a separate supply, VIO, which is set to the host logic level. Power dissipation scales with throughput.

The AD7682/AD7689 are housed in a tiny 20-lead LFCSP and 20-lead WLCSP with operation specified from −40°C to +85°C.

Table 1. Multichannel 14-/16-Bit PulSAR® ADCs

Type	Channels	250 kSPS	500 kSPS	ADC Driver
14-Bit	8	AD7949		ADA4805-1/ ADA4807-1
16-Bit	4	AD7682		ADA4805-1/ ADA4807-1
16-Bit	8	AD7689	AD7699	ADA4805-1/ ADA4807-1

Rev. F Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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Added WLCSP Signal-to-Noise and SINAD Parameters; Table 2 ... 3
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5/08—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, V_{REF} = VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Test Conditions/ Comments	AD7689A			AD7682B/AD7689B			Unit
		Min	Typ	Max	Min	Typ	Max	
RESOLUTION		16			16			Bits
ANALOG INPUT								
Voltage Range	Unipolar mode	0		$+V_{REF}$	0		$+V_{REF}$	V
	Bipolar mode	$-V_{REF}/2$		$+V_{REF}/2$	$-V_{REF}/2$		$+V_{REF}/2$	
Absolute Input Voltage	Positive input, unipolar and bipolar modes	−0.1		V_{REF} + 0.1	−0.1		V_{REF} + 0.1	V
	Negative or COM input, unipolar mode	−0.1		+0.1	−0.1		+0.1	V
	Negative or COM input, bipolar mode	$V_{REF}/2 - 0.1$	$V_{REF}/2$	$V_{REF}/2 + 0.1$	$V_{REF}/2 - 0.1$	$V_{REF}/2$	$V_{REF}/2 + 0.1$	V
Analog Input CMRR	f_{IN} = 250 kHz		68			68		dB
Leakage Current at 25°C	Acquisition phase		1			1		nA
Input Impedance[1]								
THROUGHPUT								
Conversion Rate								
Full Bandwidth[2]	VDD = 4.5 V to 5.5 V	0		250	0		250	kSPS
	VDD = 2.3 V to 4.5 V	0		200	0		200	kSPS
¼ Bandwidth[2]	VDD = 4.5 V to 5.5 V	0		62.5	0		62.5	kSPS
	VDD = 2.3 V to 4.5 V	0		50	0		50	kSPS
Transient Response	Full-scale step, full bandwidth			1.8			1.8	µs
	Full-scale step, ¼ bandwidth			14.5			14.5	µs
ACCURACY								
No Missing Codes		15			16			Bits
Integral Linearity Error		−4		+4	−1.5	±0.4	+1.5	LSB[3]
Differential Linearity Error					−1	±0.25	+1.5	LSB
Transition Noise	REF = VDD = 5 V		0.6			0.5		LSB
Gain Error[4]		−32		+32	−8	±1	+8	LSB
Gain Error Match			±2		−4	±0.5	+4	LSB
Gain Error Temperature Drift			±1			±1		ppm/°C
Offset Error[4]	VDD = 4.5 V to 5.5 V	−32		+32	−8	±1	+8	LSB
	VDD = 2.3 V to 4.5 V		±32			±5		LSB
Offset Error Match			±2		−4	±0.5	+4	LSB
Offset Error Temperature Drift			±1			±1		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±1.5			±1.5		LSB
AC ACCURACY[5]								
Dynamic Range			90.5			93.8		dB[6]
Signal-to-Noise								
LFCSP	f_{IN} = 20 kHz, V_{REF} = 5 V		90		92.5	93.5		dB
	f_{IN} = 20 kHz, V_{REF} = 4.096 V, internal REF		89		91	92.3		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V, internal REF		86		87.5	88.8		dB

Parameter	Test Conditions/ Comments	AD7689A Min	AD7689A Typ	AD7689A Max	AD7682B/AD7689B Min	AD7682B/AD7689B Typ	AD7682B/AD7689B Max	Unit
WLFCSP	f_{IN} = 20 kHz, V_{REF} = 5 V				91	92		dB
	f_{IN} = 20 kHz, V_{REF} = 4.096 V, internal REF				89.5	91		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V, internal REF				86	87.5		dB
SINAD								
LFCSP	f_{IN} = 20 kHz, V_{REF} = 5 V		89		91	92.5		dB
	f_{IN} = 20 kHz, V_{REF} = 5 V, −60 dB input		30.5			33.5		dB
	f_{IN} = 20 kHz, V_{REF} = 4.096 V internal REF		88		90	91		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V internal REF		86		87	88.4		dB
WLFCSP	f_{IN} = 20 kHz, V_{REF} = 5 V				89.5	91		dB
	f_{IN} = 20 kHz, V_{REF} = 5 V, −60 dB input					32		dB
	f_{IN} = 20 kHz, V_{REF} = 4.096 V internal REF				88.5	89.5		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V internal REF				85.5	87		dB
Total Harmonic Distortion (THD)	f_{IN} = 20 kHz		−97			−100		dB
Spurious-Free Dynamic Range	f_{IN} = 20 kHz		105			110		dB
Channel-to-Channel Crosstalk	f_{IN} = 100 kHz on adjacent channel(s)		−120			−125		dB
SAMPLING DYNAMICS								
−3 dB Input Bandwidth	Full bandwidth		1.7			1.7		MHz
	¼ bandwidth		0.425			0.425		MHz
Aperture Delay	VDD = 5 V		2.5			2.5		ns

[1] See the Analog Inputs section.
[2] The bandwidth is set in the configuration register.
[3] LSB means least significant bit. With the 5 V input range, one LSB is 76.3 µV.
[4] See the Terminology section. These specifications include full temperature range variation but not the error contribution from the external reference.
[5] With VDD = 5 V, unless otherwise noted.
[6] All specifications expressed in decibels are referred to a full-scale input FSR and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, V_{REF} = VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INTERNAL REFERENCE					
REF Output Voltage	2.5 V at 25°C	2.490	2.500	2.510	V
	4.096 V at 25°C	4.086	4.096	4.106	V
REFIN Output Voltage[1]	2.5 V at 25°C		1.2		V
	4.096 V at 25°C		2.3		V
REF Output Current			±300		µA
Temperature Drift			±10		ppm/°C
Line Regulation	VDD = 5 V ± 5%		±15		ppm/V
Long-Term Drift	1000 hours		50		ppm
Turn-On Settling Time	C_{REF} = 10 µF		5		ms
EXTERNAL REFERENCE					
Voltage Range	REF input	0.5		VDD + 0.3	V
	REFIN input (buffered)	0.5		VDD − 0.5	V
Current Drain[2]	250 kSPS, REF = 5 V		50		µA
TEMPERATURE SENSOR					
Output Voltage[3]	25°C		283		mV
Temperature Sensitivity			1		mV/°C
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.3 × VIO	V
V_{IH}		0.7 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format[4]					
Pipeline Delay[5]					
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD[6]	Specified performance	2.3		5.5	V
VIO	Specified performance	1.8		VDD + 0.3	V
Standby Current[7, 8]	VDD and VIO = 5 V at 25°C		50		nA
Power Dissipation	VDD = 2.5 V, 100 SPS throughput		1.7		µW
	VDD = 2.5 V, 200 kSPS throughput		3.5		mW
	VDD = 5 V, 250 kSPS throughput		12.5	18	mW
	VDD = 5 V, 250 kSPS throughput with internal reference		15.5	21	mW
Energy per Conversion	VDD = 5 V		60		nJ
TEMPERATURE RANGE[9]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] This is the output from the internal band gap.
[2] This is an average current and scales with throughput.
[3] The output voltage is internal and present on a dedicated multiplexer input.
[4] Unipolar mode is serial 16-bit straight binary. Bipolar mode is serial 16-bit twos complement.
[5] Conversion results available immediately after completed conversion.
[6] The minimum VDD supply must be 3 V when the 2.5 V internal reference is enabled, and 4.5 V when the 4.096 V internal reference is enabled. See Figure 23 for more information.
[7] With all digital inputs forced to VIO or GND as required.
[8] During acquisition phase.
[9] Contact an Analog Devices, Inc., sales representative for the extended temperature range.

TIMING SPECIFICATIONS

VDD = 4.5 V to 5.5 V, VIO = 1.8 V to VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1]	Symbol	Min	Typ	Max	Unit
CONVERSION TIME					
CNV Rising Edge to Data Available	t_{CONV}			2.2	µs
ACQUISITION TIME	t_{ACQ}	1.8			µs
TIME BETWEEN CONVERSIONS	t_{CYC}	4.0			µs
DATA WRITE/READ DURING CONVERSION	t_{DATA}			1.2	µs
SCK					
Period	t_{SCK}	t_{DSDO} + 2			ns
Low Time	t_{SCKL}	11			ns
High Time	t_{SCKH}	11			ns
Falling Edge to Data Remains Valid	t_{HSDO}	4			ns
Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				23	ns
VIO Above 1.8 V				28	ns
CNV					
Pulse Width	t_{CNVH}	10			ns
Low to SDO D15 MSB Valid	t_{EN}				
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				22	ns
VIO Above 1.8 V				25	ns
High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}			32	ns
Low to SCK Rising Edge	t_{CLSCK}	10			ns
DIN					
Valid Setup Time from SCK Rising Edge	t_{SDIN}	5			ns
Valid Hold Time from SCK Rising Edge	t_{HDIN}	5			ns

[1] See Figure 2 and Figure 3 for load conditions.

VDD = 2.3 V to 4.5 V, VIO = 1.8 V to VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter[1]	Symbol	Min	Typ	Max	Unit
CONVERSION TIME	t_{CONV}			3.2	µs
CNV Rising Edge to Data Available					
ACQUISITION TIME	t_{ACQ}	1.8			µs
TIME BETWEEN CONVERSIONS	t_{CYC}	5			µs
DATA WRITE/READ DURING CONVERSION	t_{DATA}			1.2	µs
SCK					
Period	t_{SCK}	t_{DSDO} + 2			ns
Low Time	t_{SCKL}	12			ns
High Time	t_{SCKH}	12			ns
Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 3 V				24	ns
VIO Above 2.7 V				30	ns
VIO Above 2.3 V				38	ns
VIO Above 1.8 V				48	ns
CNV	t_{EN}				
Pulse Width	t_{CNVH}	10			ns
Low to SDO D15 MSB Valid					
VIO Above 3 V				21	ns
VIO Above 2.7 V				27	ns
VIO Above 2.3 V				35	ns
VIO Above 1.8 V				45	ns
High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}			50	ns
Low to SCK Rising Edge	t_{CLSCK}	10			ns
DIN					
Valid Setup Time from SCK Rising Edge	t_{SDIN}	5			ns
Valid Hold Time from SCK Rising Edge	t_{HDIN}	5			ns

[1] See Figure 2 and Figure 3 for load conditions.

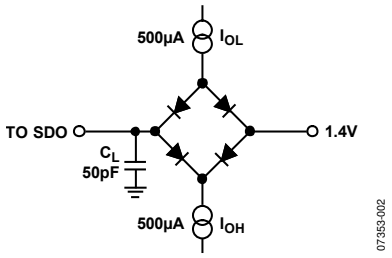


Figure 2. Load Circuit for Digital Interface Timing

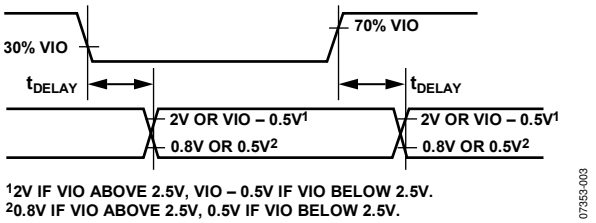


Figure 3. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Inputs	
INx,[1] COM	GND − 0.3 V to VDD + 0.3 V or VDD ± 130 mA
REF, REFIN	GND − 0.3 V to VDD + 0.3 V
Supply Voltages	
VDD, VIO to GND	−0.3 V to +7 V
VIO to VDD	−0.3 V to VDD + 0.3 V
DIN, CNV, SCK to GND	−0.3 V to VIO + 0.3 V
SDO to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (LFCSP)	48°C/W
θ_{JC} Thermal Impedance (LFCSP)	4.4°C/W

[1] See the Analog Inputs section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

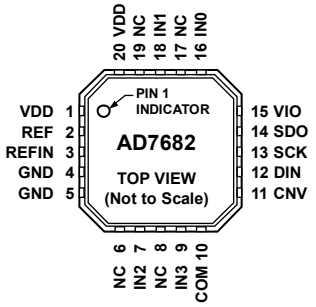


Figure 4. AD7682 LFCSP Pin Configuration

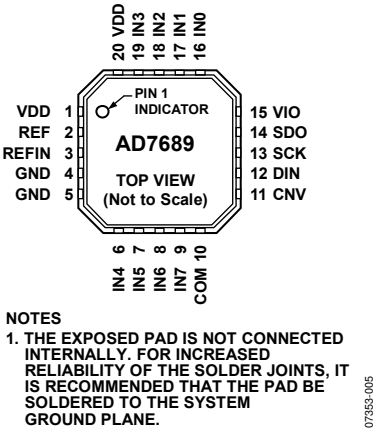


Figure 5. AD7689 LFCSP Pin Configuration

Table 7. AD7682 LFCSP and AD7689 LFCSP Pin Function Descriptions

Pin No.	AD7682 LFCSP Mnemonic	AD7689 LFCSP Mnemonic	Type[1]	Description
1, 20	VDD	VDD	P	Power Supply. Nominally 2.5 V to 5.5 V when using an external reference and decoupled with 10 µF and 100 nF capacitors. When using the internal reference for a 2.5 V output, the minimum must be 3.0 V. When using the internal reference for 4.096 V output, the minimum must be 4.6 V.
2	REF	REF	AI/O	Reference Input/Output. See the Voltage Reference Output/Input section. When the internal reference is enabled, this pin produces a selectable system reference of 2.5 V or 4.096 V. When the internal reference is disabled and the buffer is enabled, REF produces a buffered version of the voltage present on the REFIN pin (VDD − 0.5 V, maximum), which is useful when using low cost, low power references. For improved drift performance, connect a precision reference to REF (0.5 V to VDD). For any reference method, this pin needs decoupling with an external 10 µF capacitor connected as close to REF as possible. See the Reference Decoupling section.
3	REFIN	REFIN	AI/O	Internal Reference Output/Reference Buffer Input. See the Voltage Reference Output/Input section. When using the internal reference, the internal unbuffered reference voltage is present and requires decoupling with a 0.1 µF capacitor. When using the internal reference buffer, apply a source between 0.5 V and (VDD − 0.5 V) that is buffered to the REF pin, as described in the REF pin description.
4, 5	GND	GND	P	Power Supply Ground.
6	NC	IN4	AI	No Connection (AD7682). Analog Input Channel 4 (AD7689).
7	IN2	IN5	AI	Analog Input Channel 2 (AD7682). Analog Input Channel 5 (AD7689).
8	NC	IN6	AI	No Connection (AD7682). Analog Input Channel 6 (AD7689).
9	IN3	IN7	AI	Analog Input Channel 3 (AD7682). Analog Input Channel 7 (AD7689).
10	COM	COM	AI	Common Channel Input. All input channels, IN[7:0], can be referenced to a common-mode point of 0 V or V_{REF}/2 V.
11	CNV	CNV	DI	Conversion Input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is held low, the busy indictor is enabled.
12	DIN	DIN	DI	Data Input. Use this input for writing to the 14-bit configuration register. The configuration register can be written to during and after conversion.
13	SCK	SCK	DI	Serial Data Clock Input. This input is used to clock out the data on SDO and clock in data on DIN in an MSB first fashion.

Pin No.	AD7682 LFCSP Mnemonic	AD7689 LFCSP Mnemonic	Type[1]	Description
14	SDO	SDO	DO	Serial Data Output. The conversion result is output on this pin, synchronized to SCK. In unipolar modes, conversion results are straight binary; in bipolar modes, conversion results are twos complement.
15	VIO	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
16	IN0	IN0	AI	Analog Input Channel 0.
17	NC	IN1	AI	No Connection (AD7682). Analog Input Channel 1 (AD7689).
18	IN1	IN2	AI	Analog Input Channel 1 (AD7682). Analog Input Channel 2 (AD7689).
19	NC	IN3	AI	No Connection (AD7682). Analog Input Channel 3 (AD7689).
21	EPAD	EPAD	NC	Exposed Pad. The exposed pad is not connected internally. For increased reliability of the solder joints, it is recommended that the pad be soldered to the system ground plane.

[1]AI means analog input, AI/O means analog input/output, DI means digital input, DO means digital output, P means power, and NC means no internal connection.

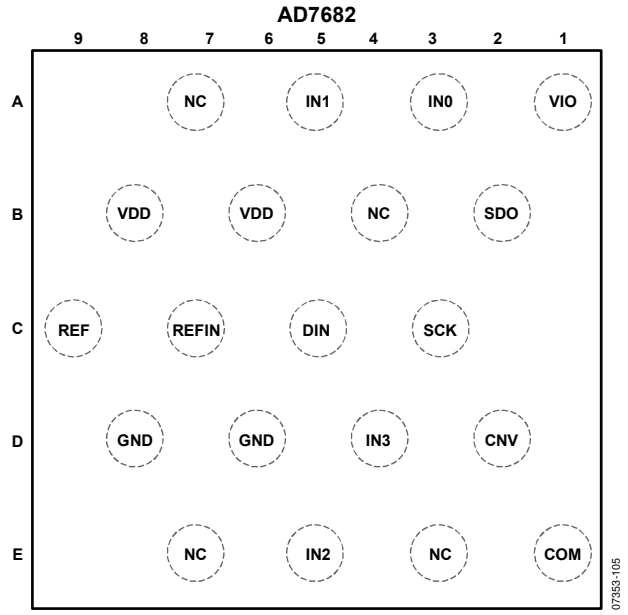


Figure 6. AD7682 WLCSP Pin Configuration

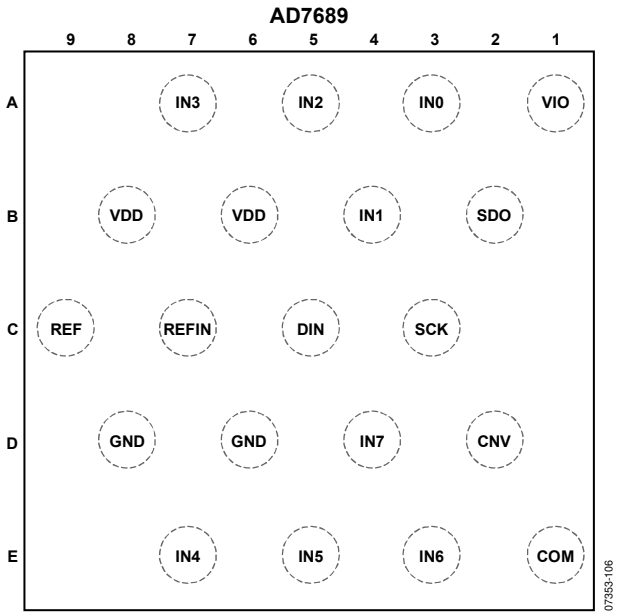


Figure 7. AD7689 WLCSP Pin Configuration

Table 8. AD7682 WLCSP and AD7689 WLCSP Pin Function Descriptions

Pin No.	AD7682 WLCSP Mnemonic	AD7689 WLCSP Mnemonic	Type[1]	Description
B6, B8	VDD	VDD	P	Power Supply. Nominally 2.5 V to 5.5 V when using an external reference and decoupled with 10 µF and 100 nF capacitors. When using the internal reference for a 2.5 V output, the minimum must be 3.0 V. When using the internal reference for 4.096 V output, the minimum must be 4.6 V.
C9	REF	REF	AI/O	Reference Input/Output. See the Voltage Reference Output/Input section. When the internal reference is enabled, this pin produces a selectable system reference of 2.5 V or 4.096 V. When the internal reference is disabled and the buffer is enabled, REF produces a buffered version of the voltage present on the REFIN pin (VDD − 0.5 V, maximum), which is useful when using low cost, low power references. For improved drift performance, connect a precision reference to REF (0.5 V to VDD). For any reference method, this pin needs decoupling with an external 10 µF capacitor connected as close to REF as possible. See the Reference Decoupling section.
C7	REFIN	REFIN	AI/O	Internal Reference Output/Reference Buffer Input. See the Voltage Reference Output/Input section. When using the internal reference, the internal unbuffered reference voltage is present and requires decoupling with a 0.1 µF capacitor. When using the internal reference buffer, apply a source between 0.5 V and (VDD − 0.5 V) that is buffered to the REF pin, as described in the REF pin description.
D6, D8	GND	GND	P	Power Supply Ground.
A7	NC	IN3	AI	No Connection (AD7682). Analog Input Channel 3 (AD7689).
E5	IN2	IN5	AI	Analog Input Channel 2 (AD7682). Analog Input Channel 5 (AD7689).
E3	NC	IN6	AI	No Connection (AD7682). Analog Input Channel 6 (AD7689).
D4	IN3	IN7	AI	Analog Input Channel 3 (AD7682). Analog Input Channel 7 (AD7689).
E1	COM	COM	AI	Common Channel Input. All input channels, IN[7:0], can be referenced to a common-mode point of 0 V or V_{REF}/2 V.
D2	CNV	CNV	DI	Conversion Input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is held low, the busy indictor is enabled.

Pin No.	AD7682 WLCSP Mnemonic	AD7689 WLCSP Mnemonic	Type[1]	Description
C5	DIN	DIN	DI	Data Input. Use this input for writing to the 14-bit configuration register. The configuration register can be written to during and after conversion.
C3	SCK	SCK	DI	Serial Data Clock Input. This input is used to clock out the data on SDO and clock in data on DIN in an MSB first fashion.
B2	SDO	SDO	DO	Serial Data Output. The conversion result is output on this pin, synchronized to SCK. In unipolar modes, conversion results are straight binary; in bipolar modes, conversion results are twos complement.
A1	VIO	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
A3	IN0	IN0	AI	Analog Input Channel 0.
B4	NC	IN1	AI	No connection (AD7682). Analog Input Channel 1 (AD7689).
A5	IN1	IN2	AI	Analog Input Channel 1 (AD7682). Analog Input Channel 2 (AD7689).
E7	NC	IN4	AI	No Connection (AD7682). Analog Input Channel 4 (AD7689).

[1]AI means analog input, AI/O means analog input/output, DI means digital input, DO means digital output, P means power, and NC means no internal connection.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 2.5 V to 5.5 V, V_{REF} = 2.5 V to 5 V, VIO = 2.3 V to VDD, unless otherwise noted.

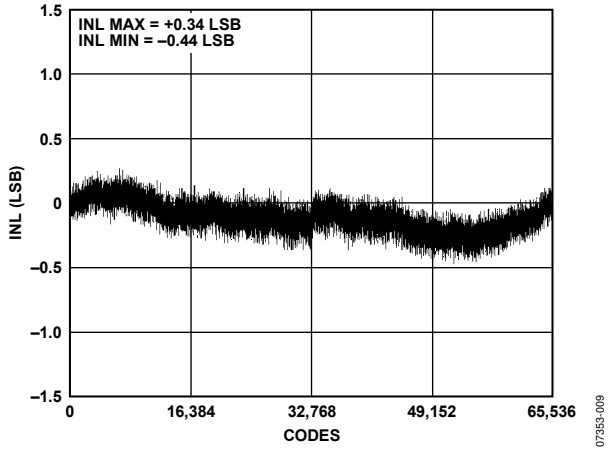


Figure 8. Integral Nonlinearity vs. Code, V_{REF} = VDD = 5 V

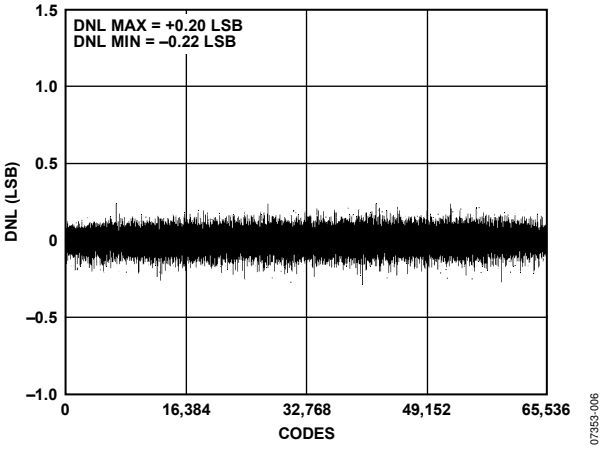


Figure 11. Differential Nonlinearity vs. Code, V_{REF} = VDD = 5 V

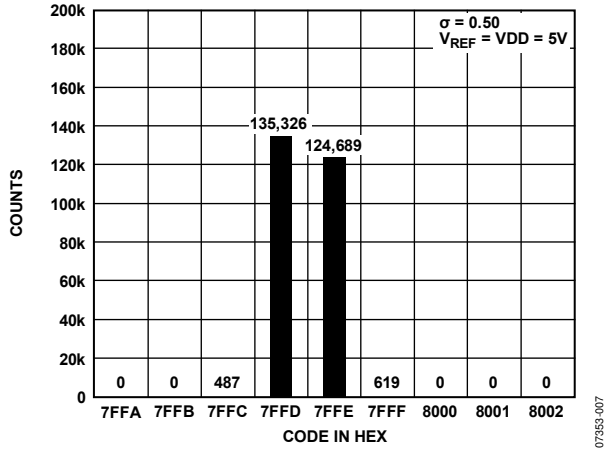


Figure 9. Histogram of a DC Input at Code Center

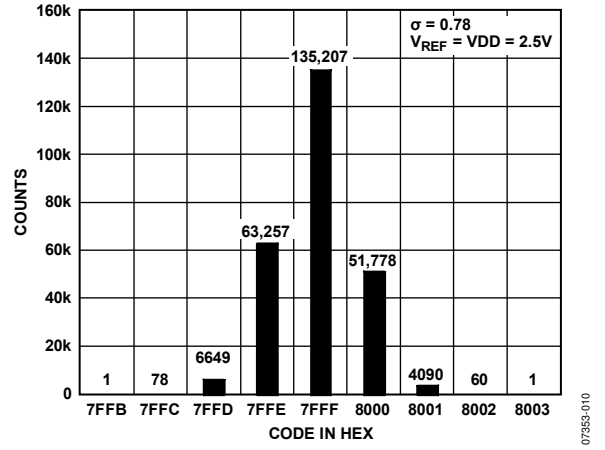


Figure 12. Histogram of a DC Input at Code Center

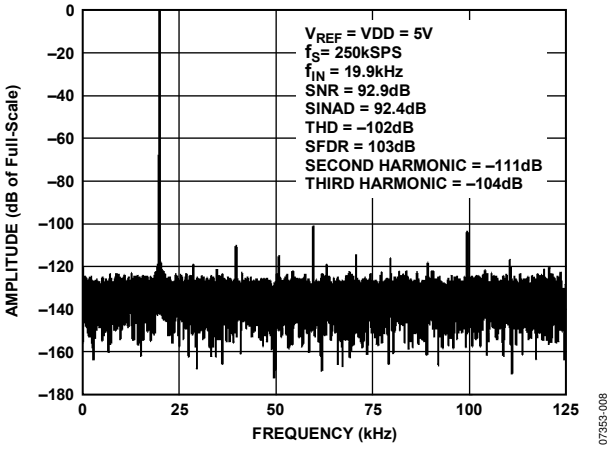


Figure 10. 20 kHz FFT, V_{REF} = VDD = 5 V

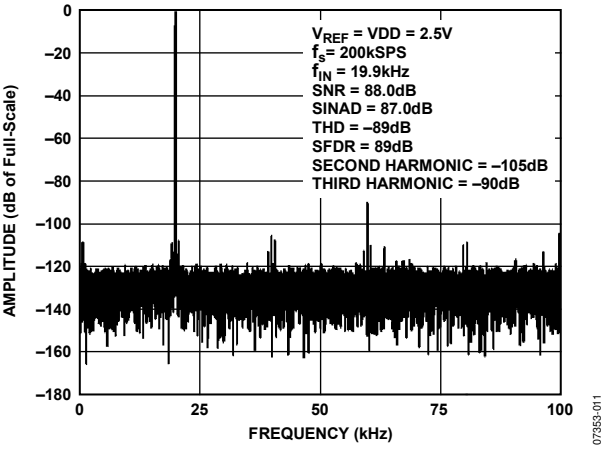


Figure 13. 20 kHz FFT, V_{REF} = VDD = 2.5 V

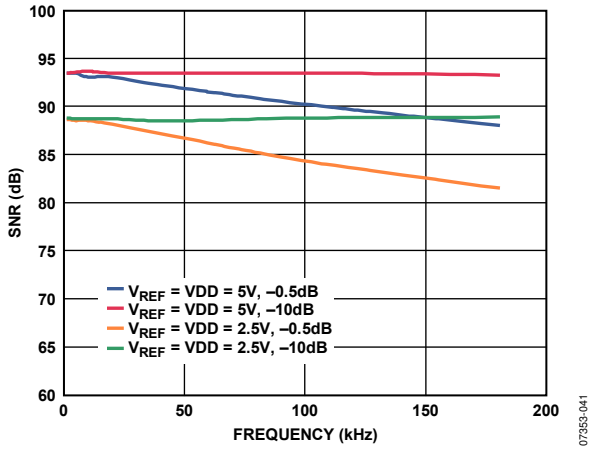


Figure 14. SNR vs. Frequency

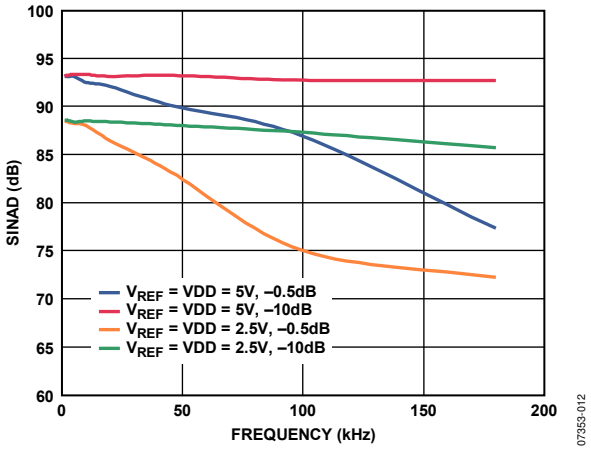


Figure 17. SINAD vs. Frequency

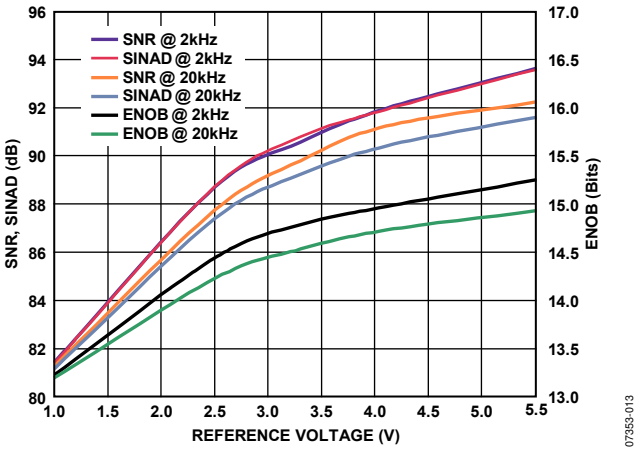


Figure 15. SNR, SINAD, and ENOB vs. Reference Voltage

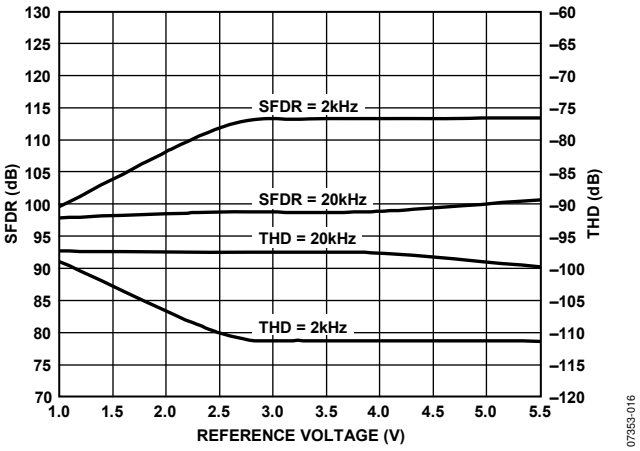


Figure 18. SFDR and THD vs. Reference Voltage

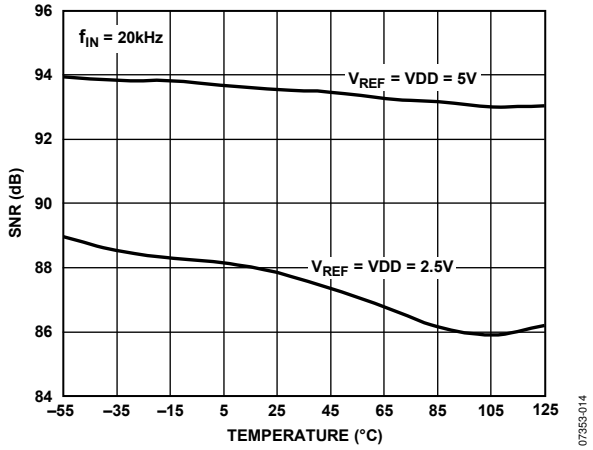


Figure 16. SNR vs. Temperature

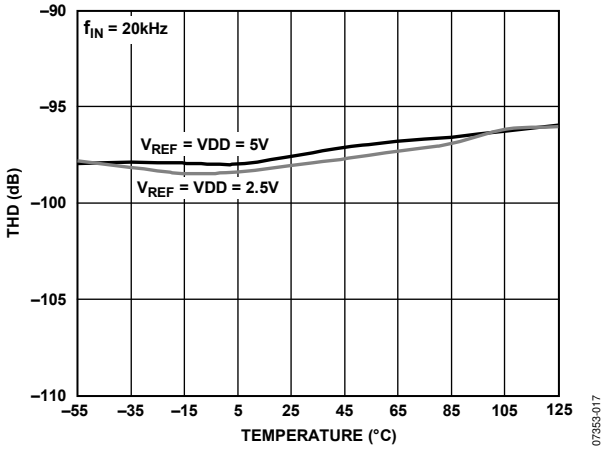


Figure 19. THD vs. Temperature

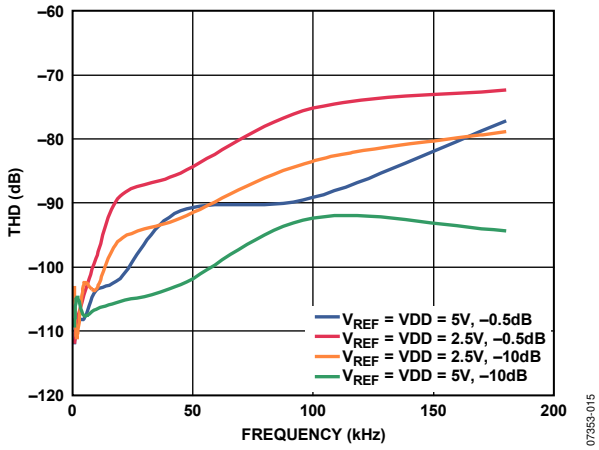


Figure 20. THD vs. Frequency

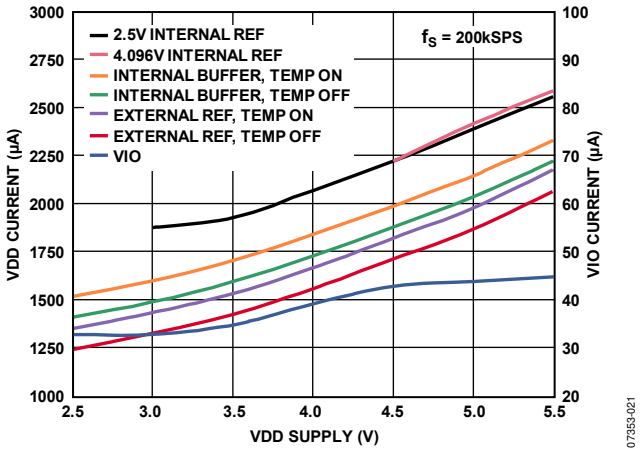


Figure 23. Operating Currents vs. Supply

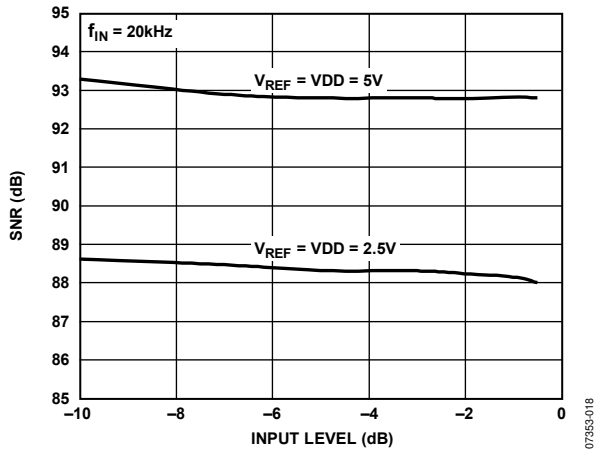


Figure 21. SNR vs. Input Level

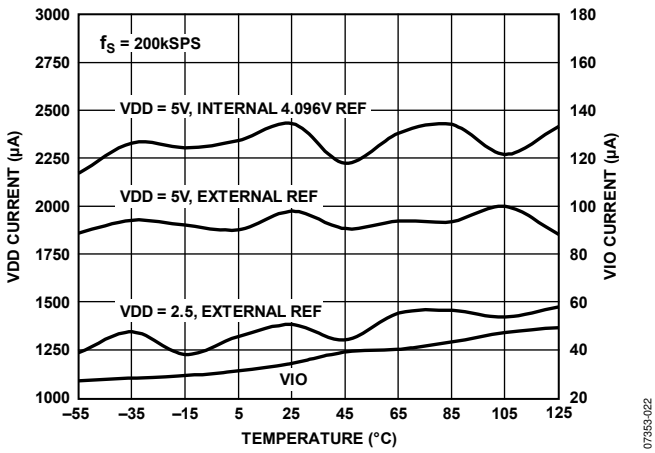


Figure 24. Operating Currents vs. Temperature

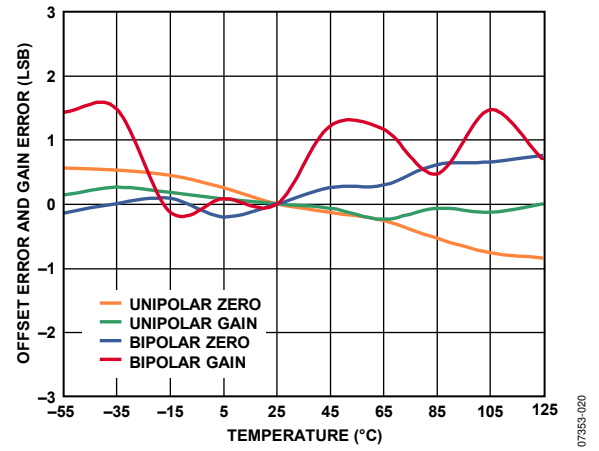


Figure 22. Offset and Gain Errors vs. Temperature

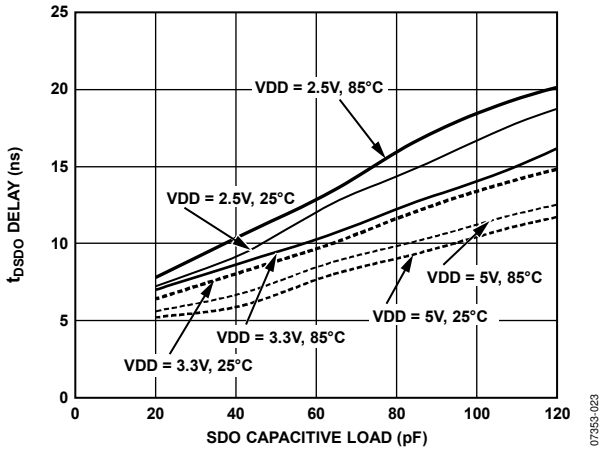


Figure 25. t_{DSDO} Delay vs. SDO Capacitance Load and Supply

TERMINOLOGY

Least Significant Bit (LSB)
The LSB is the smallest increment represented by a converter. For an ADC with N bits of resolution, the LSB expressed in volts is

$$LSB\ (\mathrm{V}) = \frac{V_{REF}}{2^N}$$

Integral Nonlinearity Error (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 27).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error
The first transition must occur at a level ½ LSB above analog ground. The offset error is the deviation of the actual transition from that point.

Gain Error
The last transition (from 111…10 to 111…11) must occur for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation in LSB (or percentage of full-scale range) of the actual level of the last transition from the ideal level after the offset error is adjusted out. Closely related is the full-scale error (also in LSB or percentage of full-scale range), which includes the effects of the offset error.

Aperture Delay
Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the CNV input and the point at which the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the formula

$$ENOB = (SINAD_{\mathrm{dB}} - 1.76)/6.02$$

and is expressed in bits.

Channel-to-Channel Crosstalk
Channel-to-channel crosstalk is a measure of the level of crosstalk between any two adjacent channels. It is measured by applying a dc to the channel under test and applying a full-scale, 100 kHz sine wave signal to the adjacent channel(s). The crosstalk is the amount of signal that leaks into the test channel, and is expressed in decibels.

Reference Voltage Temperature Coefficient
Reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN}, T (25°C), and T_{MAX}. It is expressed in ppm/°C as

$$TCV_{REF}(\mathrm{ppm/^\circ C}) = \frac{V_{REF}(Max) - V_{REF}(Min)}{V_{REF}(25^\circ C) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:
$V_{REF}(Max)$ = maximum V_{REF} at T_{MIN}, T (25°C), or T_{MAX}.
$V_{REF}(Min)$ = minimum V_{REF} at T_{MIN}, T (25°C), or T_{MAX}.
$V_{REF}(25^\circ C)$ = V_{REF} at 25°C.
T_{MAX} = +85°C.
T_{MIN} = −40°C.

THEORY OF OPERATION

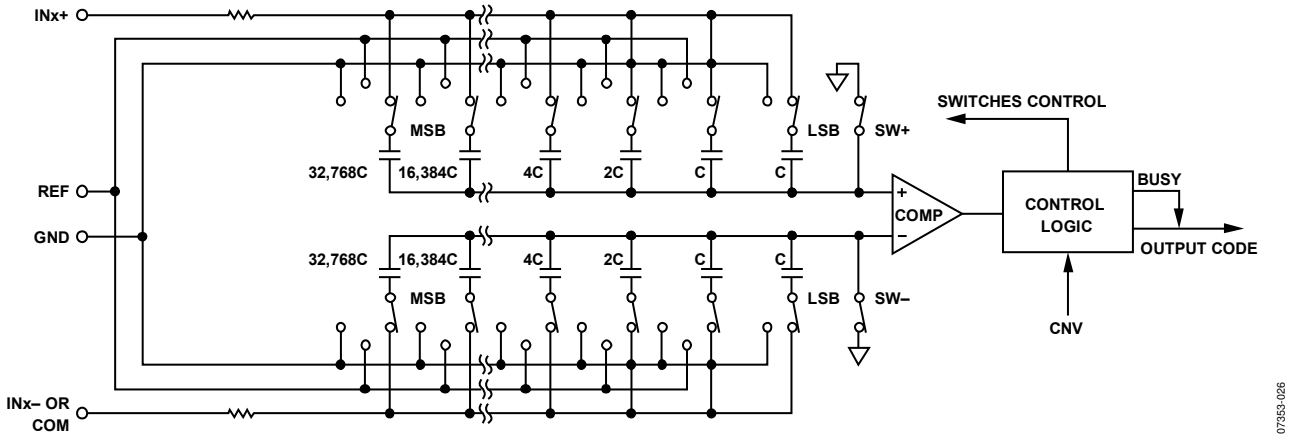


Figure 26. ADC Simplified Schematic

OVERVIEW

The AD7682/AD7689 are 4-channel/8-channel, 16-bit, charge redistribution SAR ADCs. These devices are capable of converting 250,000 samples per second (250 kSPS) and power down between conversions. For example, when operating with an external reference at 1 kSPS, they consume 17 µW typically, ideal for battery-powered applications.

The AD7682/AD7689 contain all of the components for use in a multichannel, low power data acquisition system, including

- 16-bit SAR ADC with no missing codes
- 4-channel/8-channel, low crosstalk multiplexer
- Internal low drift reference and buffer
- Temperature sensor
- Selectable one-pole filter
- Channel sequencer

These components are configured through an SPI-compatible, 14-bit register. Conversion results, also SPI compatible, can be read after or during conversions with the option for reading back the configuration associated with the conversion.

The AD7682/AD7689 provide the user with an on-chip track-and-hold and do not exhibit pipeline delay or latency.

The AD7682/AD7689 are specified from 2.3 V to 5.5 V and can be interfaced to any 1.8 V to 5 V digital logic family. They are housed in a 20-lead, 4 mm × 4 mm LFCSP and a 20-lead, 2.4 mm × 2.4 mm WLCSP that combine space savings and allow flexible configurations. They are pin-for-pin compatible with the 16-bit AD7699 and 14-bit AD7949.

CONVERTER OPERATION

The AD7682/AD7689 are successive approximation ADCs based on a charge redistribution DAC. Figure 26 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator input are connected to GND via SW+ and SW–. All independent switches are connected to the analog inputs.

The capacitor arrays are used as sampling capacitors and acquire the analog signal on the INx+ and INx– (or COM) inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW– open first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the INx+ and INx– (or COM) inputs captured at the end of the acquisition phase applies to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$...$V_{REF}/32{,}768$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the device returns to the acquisition phase, and the control logic generates the ADC output code and a busy signal indicator.

Because the AD7682/AD7689 have an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

TRANSFER FUNCTIONS

With the inputs configured for unipolar range (single-ended, COM with ground sense, or paired differentially with INx− as ground sense), the data output is straight binary.

With the inputs configured for bipolar range (COM = $V_{REF}/2$ or paired differentially with INx− = $V_{REF}/2$), the data outputs are twos complement.

The ideal transfer characteristic for the AD7682/AD7689 is shown in Figure 27 and for both unipolar and bipolar ranges with the internal 4.096 V reference.

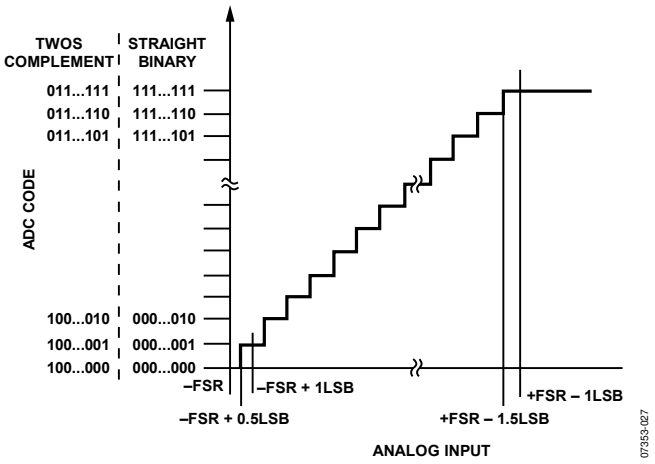


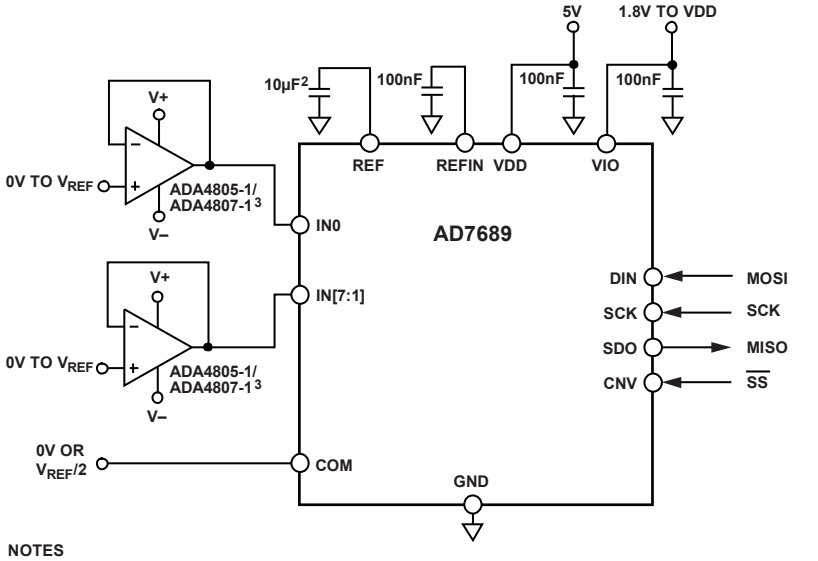
Figure 27. ADC Ideal Transfer Function

Table 9. Output Codes and Ideal Input Voltages

Description	Unipolar Analog Input[1] V_{REF} = 4.096 V	Digital Output Code (Straight Binary Hex)	Bipolar Analog Input[2] V_{REF} = 4.096 V	Digital Output Code (Twos Complement Hex)
FSR − 1 LSB	4.095938 V	0xFFFF[3]	2.047938 V	0x7FFF[3]
Midscale + 1 LSB	2.048063 V	0x8001	62.5 µV	0x0001
Midscale	2.048 V	0x8000	0 V	0x0000
Midscale − 1 LSB	2.047938 V	0x7FFF	−62.5 µV	0xFFFF
−FSR + 1 LSB	62.5 µV	0x0001	−2.047938 V	0x8001
−FSR	0 V	0x0000[4]	−2.048 V	0x8000[4]

[1] With COM or INx− = 0 V or all INx referenced to GND.
[2] With COM or INx− = V_{REF} /2.
[3] This is also the code for an overranged analog input ((INx+) − (INx−), or COM, above V_{REF} − GND).
[4] This is also the code for an underranged analog input ((INx+) − (INx−), or COM, below GND).

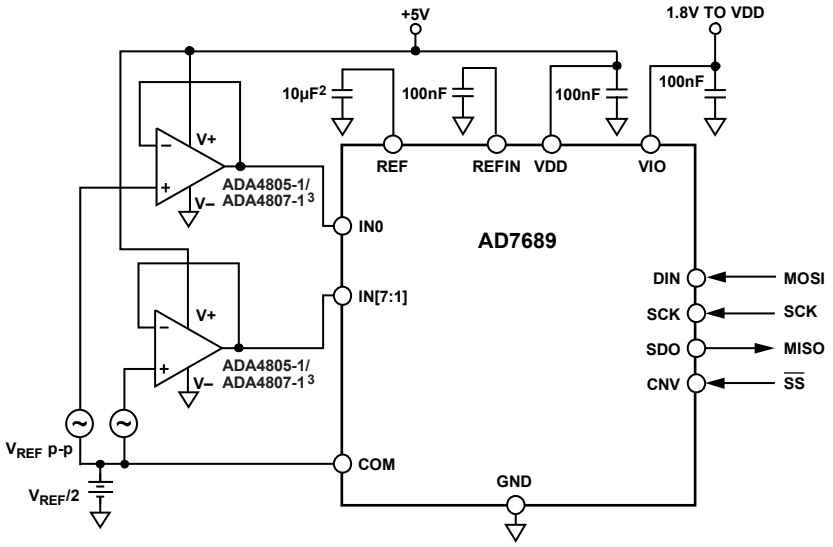
TYPICAL CONNECTION DIAGRAMS



NOTES
1. INTERNAL REFERENCE SHOWN. SEE VOLTAGE REFERENCE OUTPUT/INPUT SECTION FOR REFERENCE SELECTION.
2. C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR (X5R).
3. SEE THE DRIVER AMPLIFIER CHOICE SECTION FOR ADDITIONAL RECOMMENDED AMPLIFIERS.
4. SEE THE DIGITAL INTERFACE SECTION FOR CONFIGURING AND READING CONVERSION DATA.

07353-028

Figure 28. Typical Application Diagram with Multiple Supplies



NOTES
1. INTERNAL REFERENCE SHOWN. SEE VOLTAGE REFERENCE OUTPUT/INPUT SECTION FOR REFERENCE SELECTION.
2. C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR (X5R).
3. SEE THE DRIVER AMPLIFIER CHOICE SECTION FOR ADDITIONAL RECOMMENDED AMPLIFIERS.
4. SEE THE DIGITAL INTERFACE SECTION FOR CONFIGURING AND READING CONVERSION DATA.

07353-029

Figure 29. Typical Application Diagram Using Bipolar Input

Unipolar or Bipolar

Figure 28 shows an example of the recommended connection diagram for the AD7682/AD7689 when multiple supplies are available.

Bipolar Single Supply

Figure 29 shows an example of a system with a bipolar input using single supplies with the internal reference (optional different VIO supply). This circuit is also useful when the amplifier/signal conditioning circuit is remotely located with some common mode present. Note that for any input configuration, the INx inputs are unipolar and are always referenced to GND (no negative voltages even in bipolar range).

For this circuit, a rail-to-rail input/output amplifier can be used; however, take the offset voltage vs. input common-mode range into consideration (1 LSB = 62.5 µV with V_{REF} = 4.096 V). Note that the conversion results are in twos complement format when using the bipolar input configuration. Refer to the AN-581 Application Note, *Biasing and Decoupling Op Amps in Single Supply Applications,* for additional details about using single-supply amplifiers.

ANALOG INPUTS

Input Structure

Figure 30 shows an equivalent circuit of the input structure of the AD7682/AD7689. The two diodes, D1 and D2, provide ESD protection for the analog inputs, IN[7:0] and COM. Care must be taken to ensure that the analog input signal does not exceed the supply rails by more than 0.3 V because this causes the diodes to become forward biased and to start conducting current.

These diodes can handle a maximum forward-biased current of 130 mA. For instance, these conditions may eventually occur when the input buffer supplies are different from VDD. In such a case, for example, an input buffer with a short circuit, the current limitation can be used to protect the device.

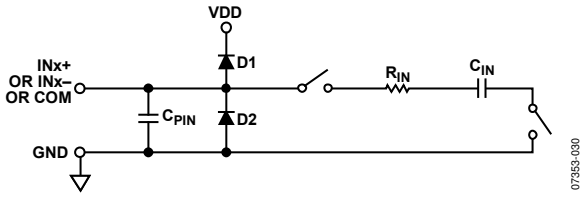


Figure 30. Equivalent Analog Input Circuit

This analog input structure allows the sampling of the true differential signal between INx+ and COM or INx+ and INx−. (COM or INx− = GND ± 0.1 V or V_{REF} ± 0.1 V). By using these differential inputs, signals common to both inputs are rejected, as shown in Figure 31.

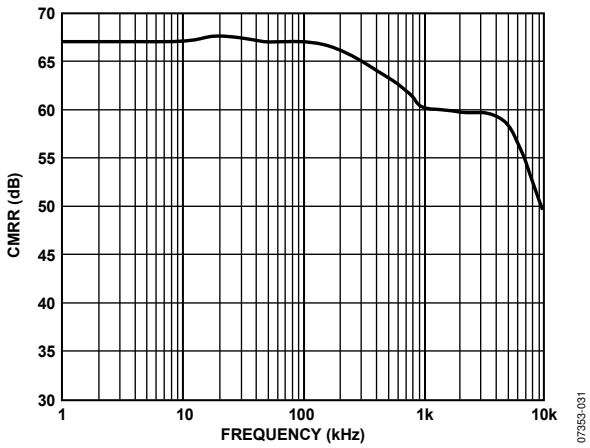


Figure 31. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog inputs can be modeled as a parallel combination of the capacitor, CPIN, and the network formed by the series connection of RIN and CIN. CPIN is primarily the pin capacitance. RIN is typically 2.2 kΩ and is a lumped component composed of serial resistors and the on resistance ofthe switches. CIN is typically 27 pF and is mainly the ADC sampling capacitor.

Selectable Low-Pass Filter

During the conversion phase, when the switches are opened, the input impedance is limited to C_{PIN}. While the AD7682/AD7689 are acquiring, R_{IN} and C_{IN} make a one-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise from the driving circuitry. The low-pass filter can be programmed for the full bandwidth or ¼ of the bandwidth with CFG[6], as shown in Table 11. This setting changes R_{IN} to 19 kΩ. Note that the converter throughput must also be reduced by ¼ when using the filter. If the maximum throughput is used with the bandwidth (BW) set to ¼, the converter acquisition time, t_{ACQ}, is violated, resulting in increased THD.

Input Configurations

Figure 32 shows the different methods for configuring the analog inputs with the configuration register, CFG[12:10]. Refer to the Configuration Register, CFG, section for more details.

The analog inputs can be configured as shown in

- Figure 32 (A), single-ended referenced to system ground; CFG[12:10] = 111_2. In this configuration, all inputs (IN[7:0]) have a range of GND to V_{REF}.
- Figure 32 (B), bipolar differential with a common reference point; COM = $V_{REF}/2$; CFG[12:10] = 010_2. Unipolar differential with COM connected to a ground sense; CFG[12:10] = 110_2. In this configuration, all inputs IN[7:0] have a range of GND to V_{REF}.
- Figure 32 (C), bipolar differential pairs with the negative input channel referenced to $V_{REF}/2$; CFG[12:10] = $00X_2$. Unipolar differential pairs with the negative input channel referenced to a ground sense; CFG[12:10] = $10X_2$. In these configurations, the positive input channels have the range of GND to V_{REF}. The negative input channels are a sense referred to $V_{REF}/2$ for bipolar pairs, or GND for unipolar pairs. The positive channel is configured with CFG[9:7]. If CFG[9:7] is even, then IN0, IN2, IN4, and IN6 are used. If CFG[9:7] is odd, then IN1, IN3, IN5, and IN7 are used, as indicated by the channels with parentheses in Figure 32 (C). For example, for IN0/IN1 pairs with the positive channel on IN0, CFG[9:7] = 000_2. For IN4/IN5 pairs with the positive channel on IN5, CFG[9:7] = 101_2. Note that for the sequencer, detailed in the Channel Sequencer section, the positive channels are always IN0, IN2, IN4, and IN6.
- Figure 32 (D), inputs configured in any of the preceding combinations (showing that the AD7682/AD7689 can be configured dynamically).

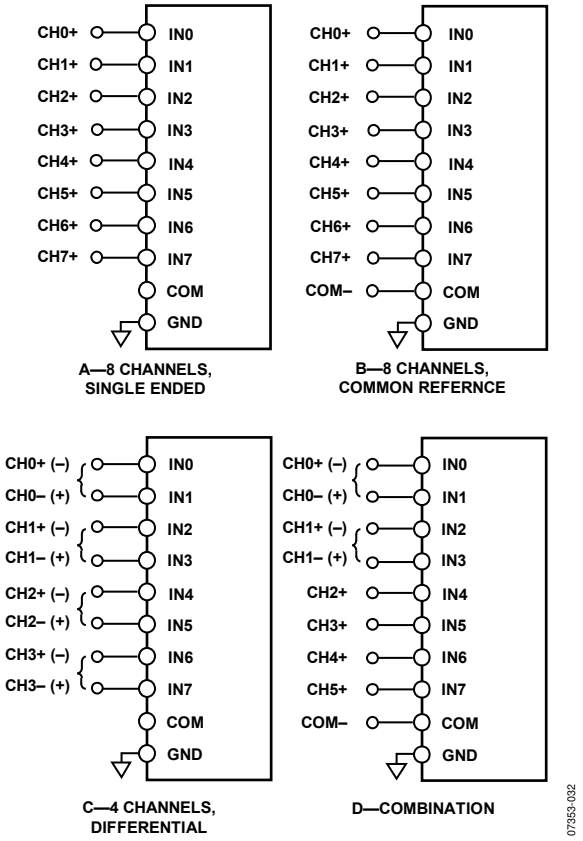


Figure 32. Multiplexed Analog Input Configurations

Sequencer

The AD7682/AD7689 include a channel sequencer useful for scanning channels in a repeated fashion. Refer to the Channel Sequencer section for further details on the sequencer operation.

Source Resistance

When the source impedance of the driving circuit is low, the AD7682/AD7689 can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

DRIVER AMPLIFIER CHOICE

Although the AD7682/AD7689 are easy to drive, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and transition noise performance of the AD7682/AD7689. Note that the AD7682/AD7689 have a noise much lower than most other 16-bit ADCs and, therefore, can be driven by a noisier amplifier to meet a given system noise specification. The noise from the amplifier is filtered by the AD7682/AD7689 analog input circuit low-pass filter made by R_{IN} and C_{IN}, or by an external filter, if one is used. Because the typical noise of the AD7682/AD7689 is 35 µV rms (with V_{REF} = 5 V), the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20\log\left(\frac{35}{\sqrt{35^2 + \frac{\pi}{2} f_{-3dB}(Ne_N)^2}}\right)$$

  where:
  f_{-3dB} is the input bandwidth in megahertz of the AD7682/AD7689 (1.7 MHz in full BW or 425 kHz in ¼ BW), or the cutoff frequency of an input filter, if one is used.
  N is the noise gain of the amplifier (for example, 1 in buffer configuration).
  e_N is the equivalent input noise voltage of the op amp, in nV/√Hz.
- For ac applications, the driver must have a THD performance commensurate with the AD7682/AD7689. Figure 20 shows THD vs. frequency for the AD7682/AD7689.
- For multichannel, multiplexed applications on each input or input pair, the driver amplifier and the AD7682/AD7689 analog input circuit must settle a full-scale step onto the capacitor array at a 16-bit level (0.0015%). In amplifier data sheets, settling at 0.1% to 0.01% is more commonly specified. This may differ significantly from the settling time at a 16-bit level and must be verified prior to driver selection.

Table 10. Recommended Driver Amplifiers

Amplifier	Typical Application
ADA4805-1	Low noise, small size, and low power
ADA4807-1	Very low noise and high frequency
ADA4627-1	Precision, low noise, and low input bias
ADA4522-1	Precision, zero drift, and EMI enhanced
ADA4500-2	Precision, rail-to-rail input/output, and zero input crossover distortion

VOLTAGE REFERENCE OUTPUT/INPUT

The AD7682/AD7689 allow the choice of a very low temperature drift internal voltage reference, an external reference, or an external buffered reference.

The internal reference of the AD7682/AD7689 provide excellent performance and can be used in almost all applications. There are six possible choices of voltage reference schemes, briefly described in Table 11, with more details in each of the following sections.

Internal Reference/Temperature Sensor

The precision internal reference, suitable for most applications, can be set for either a 2.5 V or a 4.096 V output, as detailed in Table 11. With the internal reference enabled, the band gap voltage is also present on the REFIN pin, which requires an external 0.1 µF capacitor. Because the current output of REFIN is limited, it can be used as a source if followed by a suitable buffer, such as the AD8605. Note that the voltage of REFIN changes depending on the 2.5 V or 4.096 V internal reference.

Enabling the reference also enables the internal temperature sensor, which measures the internal temperature of the AD7682/AD7689, and is therefore useful for performing a system calibration. For applications requiring the use of the temperature sensor, the internal reference must be active (internal buffer can be disabled in this case). Note that, when using the temperature sensor, the output is straight binary referenced from the AD7682/AD7689 GND pin.

The internal reference is temperature compensated to within 10 mV. The reference is trimmed to provide a typical drift of ±10 ppm/°C.

Connect the AD7682/AD7689 as shown in Figure 33 for either a 2.5 V or 4.096 V internal reference.

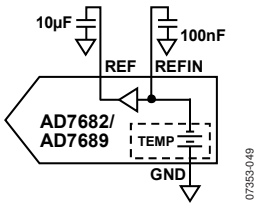


Figure 33. 2.5 V or 4.096 V Internal Reference Connection

External Reference and Internal Buffer

For improved drift performance, an external reference can be used with the internal buffer, as shown in Figure 34. The external source is connected to REFIN, the input to the on-chip unity-gain buffer, and the output is produced on the REF pin. An external reference can be used with the internal buffer with or without the temperature sensor enabled. Refer to Table 11 for register details. With the buffer enabled, the gain is unity and is limited to an input/output of VDD = −0.2 V; however, the maximum voltage allowable must be ≤(VDD − 0.5 V).

The internal reference buffer is useful in multiconverter applications because a buffer is typically required in these applications. In addition, a low power reference can be used because the internal buffer provides the necessary performance to drive the SAR architecture of the AD7682/AD7689.

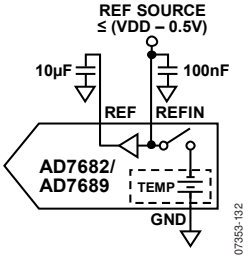


Figure 34. External Reference Using Internal Buffer

External Reference

In any of the six voltage reference schemes, an external reference can be connected directly on the REF pin as shown in Figure 35 because the output impedance of REF is >5 kΩ. To reduce power consumption, power down the reference and buffer. Refer to Table 11 for register details. For improved drift performance, an external reference from the family of devices that includes the ADR430, ADR431, ADR433, ADR434, and ADR435, or the family of devices that includes the ADR440, ADR441, ADR443, ADR444, and ADR445 is recommended.

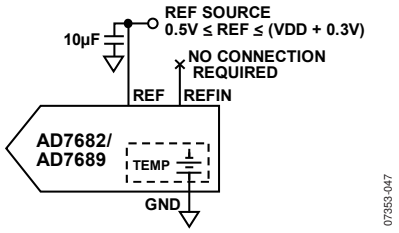


Figure 35.External Reference

Note that the best SNR is achieved with a 5 V external reference as the internal reference is limited to 4.096 V. The SNR degradation is as follows:

$$SNR_{LOSS} = 20 \log \frac{4.096}{5}$$

Reference Decoupling

Whether using an internal or external reference, the AD7682/AD7689 voltage reference output/input, REF, has a dynamic input impedance and must be driven by a low impedance source with efficient decoupling between the REF and GND pins. This decoupling depends on the choice of the voltage reference but usually consists of a low ESR capacitor connected to REF and GND with minimum parasitic inductance. A 10 µF (X5R, 1206 size) ceramic chip capacitor is appropriate when using the internal reference, a member of the ADR430, ADR431, ADR433, ADR434, and ADR435 family of external references, a member of the ADR440, ADR441, ADR443, ADR444, and ADR445 family of external references, or a low impedance buffer such as the AD8031 or the AD8605.

The placement of the reference decoupling capacitor is also important to the performance of the AD7682/AD7689, as explained in the Layout section. Mount the decoupling capacitor with a thick PCB trace on the same side as the ADC at the REF pin. The GND must also connect to the reference decoupling capacitor with the shortest distance and to the analog ground plane with several vias.

If desired, smaller reference decoupling capacitor values down to 2.2 µF can be used with a minimal impact on performance, especially on DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and GND pins.

For applications that use multiple AD7682/AD7689 devices or other PulSAR devices, it is more effective to use the internal reference buffer to buffer the external reference voltage, thus reducing SAR conversion crosstalk.

The voltage reference temperature coefficient (TC) directly impacts full scale; therefore, in applications where full-scale accuracy matters, care must be taken with the TC. For instance, a ±10 ppm/°C TC of the reference changes full scale by ±1 LSB/°C.

POWER SUPPLY

The AD7682/AD7689 use two power supply pins: an analog and digital core supply (VDD), and a digital input/output interface supply (VIO). VIO allows direct interface with any logic between 1.8 V and VDD. To reduce the supplies needed, the VIO and VDD pins can be tied together. The AD7682/AD7689 are independent of power supply sequencing between VIO and VDD. Additionally, they are very insensitive to power supply variations over a wide frequency range, as shown in Figure 36.

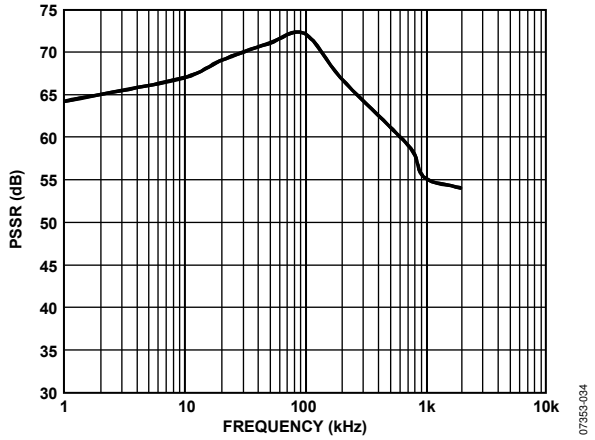


Figure 36. PSRR vs. Frequency

The AD7682/AD7689 power down automatically at the end of each conversion phase; therefore, the operating currents and power scale linearly with the sampling rate. This makes the device ideal for low sampling rates (even of a few hertz), and low battery-powered applications.

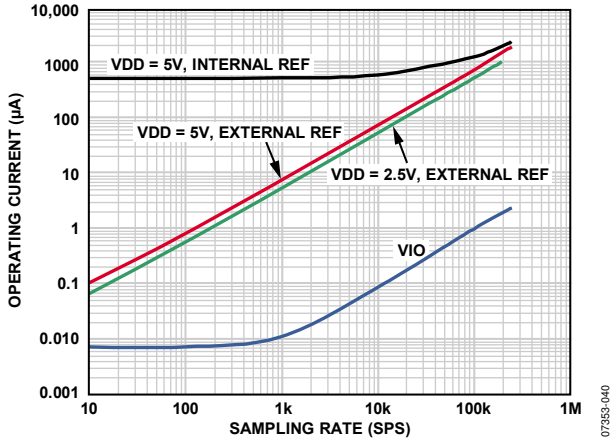
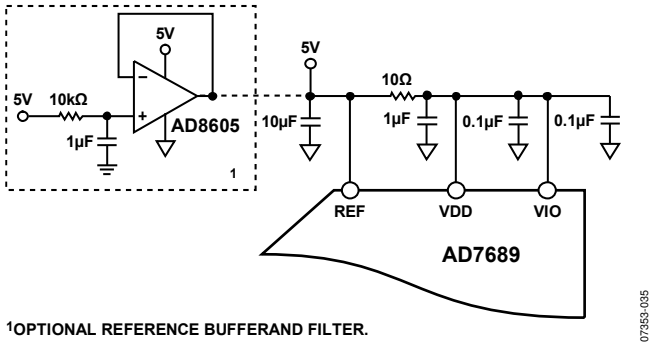


Figure 37. Operating Currents vs. Sampling Rate

SUPPLYING THE ADC FROM THE REFERENCE

For simplified applications, the AD7682/AD7689, with their low operating current, can be supplied directly using an external reference circuit like the one shown in Figure 38. The reference line can be driven by

- The system power supply directly.
- A reference voltage with enough current output capability, such as the ADR430, ADR431, ADR433, ADR434, ADR435, ADR440, ADR441, ADR443, ADR444, or ADR445.
- A reference buffer, such as the AD8605, which can also filter the system power supply, as shown in Figure 38.



[1]OPTIONAL REFERENCE BUFFERAND FILTER.

Figure 38. Example of an Application Circuit