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3 V/5 V, 1 mW, 2-/3-Channel, 16-Bit, Sigma-Delta ADCs

AD7705/AD7706

FEATURES

AD7705: 2 fully differential input channel ADCs
AD7706: 3 pseudo differential input channel ADCs
16 bits no missing codes
0.003% nonlinearity
Programmable gain front end: gains from 1 to 128
3-wire serial interface
SPI®-, QSPI™-, MICROWIRE™-, and DSP-compatible
Schmitt-trigger input on SCLK
Ability to buffer the analog input
2.7 V to 3.3 V or 4.75 V to 5.25 V operation
Power dissipation 1 mW maximum @ 3 V
Standby current 8 µA maximum
16-lead PDIP, 16-lead SOIC, and 16-lead TSSOP packages

GENERAL DESCRIPTION

The AD7705/AD7706 are complete analog front ends for low frequency measurement applications. These 2-/3-channel devices can accept low level input signals directly from a transducer and produce serial digital output. The devices employ a Σ-Δ conversion technique to realize up to 16 bits of no missing codes performance. The selected input signal is applied to a proprietary, programmable-gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via an on-chip control register, allowing adjustment of the filter cutoff and output update rate.

The AD7705/AD7706 devices operate from a single 2.7 V to 3.3 V or 4.75 V to 5.25 V supply. The AD7705 features two fully differential analog input channels; the AD7706 features three pseudo differential input channels.

Both devices feature a differential reference input. Input signal ranges of 0 mV to 20 mV through 0 V to 2.5 V can be incorporated on both devices when operating with a V_{DD} of 5 V and a reference of 2.5 V. They can also handle bipolar input signal ranges of ±20 mV through ±2.5 V, which are referenced to the AIN(–) inputs on the AD7705 and to the COMMON input on the AD7706.

FUNCTIONAL BLOCK DIAGRAM

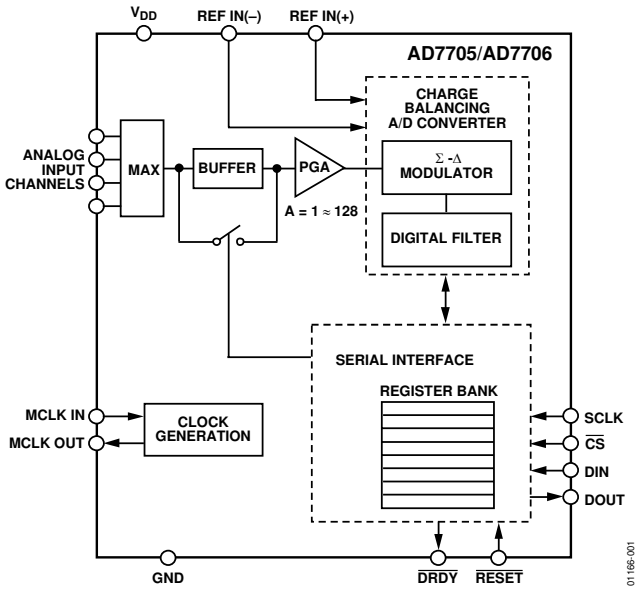

Figure 1.

The AD7705/AD7706 devices, with a 3 V supply and a 1.225 V reference, can handle unipolar input signal ranges of 0 mV to 10 mV through 0 V to 1.225 V. The devices can accept bipolar input ranges of ±10 mV through ±1.225 V. Therefore, the AD7705/AD7706 devices perform all signal conditioning and conversion for a 2-channel or 3-channel system.

The AD7705/AD7706 are ideal for use in smart, microcontroller, or DSP-based systems. The devices feature a serial interface that can be configured for 3-wire operation. Gain settings, signal polarity, and update rate selection can be configured in software using the input serial port. The parts contains self-calibration and system calibration options to eliminate gain and offset errors on the part itself or in the system. CMOS construction ensures very low power dissipation, and the power-down mode reduces the standby power consumption to 20 µW typ.

These parts are available in a 16-lead, wide body (0.3 inch), plastic dual in-line package (DIP); a 16-lead, wide body (0.3 inch), standard small outline (SOIC) package; and a low profile, 16-lead, thin shrink small outline package (TSSOP).

Rev. C

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11/98—Rev. 0 to Rev. A

Revision 0: Initial Version

PRODUCT HIGHLIGHTS

1. The AD7705/AD7706 devices consume less than 1 mW at 3 V supplies and 1 MHz master clock, making them ideal for use in low power systems. Standby current is less than 8 μA.
2. The programmable gain input allows the AD7705/AD7706 to accept input signals directly from a strain gage or transducer, removing a considerable amount of signal conditioning.
3. The AD7705/AD7706 are ideal for microcontroller or DSP processor applications with a 3-wire serial interface, reducing the number of interconnect lines and reducing the number of opto-couplers required in isolated systems.
4. The parts feature excellent static performance specifications with 16 bits, no missing codes, ±0.003% accuracy, and low rms noise (<600 nV). Endpoint errors and the effects of temperature drift are eliminated by on-chip calibration options, which remove zero-scale and full-scale errors.

SPECIFICATIONS

V_{DD} = 3 V or 5 V, REF IN(+) = 1.225 V with V_{DD} = 3 V, and 2.5 V with V_{DD} = 5 V; REF IN(−) = GND; MCLK IN = 2.4576 MHz, unless otherwise noted. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Version[1]	Unit	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	16	Bits min	Guaranteed by design, filter notch < 60 Hz
Output Noise	See Table 5 and Table 7		Depends on filter cutoffs and selected gain
Integral Nonlinearity[2]	±0.003	% of FSR max	Filter notch < 60 Hz, typically ±0.0003%
Unipolar Offset Error[3]			
Unipolar Offset Drift[4]	0.5	µV/°C typ	
Bipolar Zero Error[3]			
Bipolar Zero Drift[4]	0.5	µV/°C typ	For gains 1, 2, and 4
	0.1	µV/°C typ	For gains 8, 16, 32, 64, and 128
Positive Full-Scale Error[3, 5]			
Full-Scale Drift[4, 6]	0.5	µV/°C typ	
Gain Error[3, 7]			
Gain Drift[4, 8]	0.5	ppm of FSR/°C typ	
Bipolar Negative Full-Scale Error[2]	±0.003	% of FSR typ	Typically ±0.001%
Bipolar Negative Full-Scale Drift[4]	1	µV/°C typ	For gains of 1 to 4
	0.6	µV/°C typ	For gains of 8 to 128
ANALOG INPUTS/REFERENCE INPUTS			Specifications for AIN and REF IN, unless otherwise noted
Common-Mode Rejection (CMR)[2]			
V_{DD} = 5 V			
Gain = 1	96	dB typ	
Gain = 2	105	dB typ	
Gain = 4	110	dB typ	
Gain = 8 to 128	130	dB typ	
V_{DD} = 3 V			
Gain = 1	105	dB typ	
Gain = 2	110	dB typ	
Gain = 4	120	dB typ	
Gain = 8 to 128	130	dB typ	
Normal-Mode 50 Hz Rejection[2]	98	dB typ	For filter notches of 25 Hz, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
Normal-Mode 60 Hz Rejection[2]	98	dB typ	For filter notches of 20 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode 50 Hz Rejection[2]	150	dB typ	For filter notches of 25 Hz, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode 60 Hz Rejection[2]	150	dB typ	For filter notches of 20 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
Absolute/Common-Mode REF IN Voltage[2]	GND to V_{DD}	V min to V max	
Absolute/Common-Mode AIN Voltage[2, 9, 10]	GND − 100 mV	V min	BUF bit of setup register = 0
	V_{DD} + 30 mV	V max	
Absolute/Common-Mode AIN Voltage[2, 9]	GND + 50 mV	V min	BUF bit of setup register = 1
	V_{DD} − 1.5 V	V max	
AIN DC Input Current[2]	1	nA max	
AIN Sampling Capacitance[2]	10	pF max	
AIN Differential Voltage Range[11]	0 to $+V_{REF}$/gain[12]	nom	Unipolar input range ($\overline{B}$/U bit of setup register = 1)
	$\pm V_{REF}$/gain	nom	Bipolar input range ($\overline{B}$/U bit of setup register = 0)

Parameter	B Version[1]	Unit	Conditions/Comments
AIN Input Sampling Rate, f_S	Gain × f_{CLKIN}/64		For gains of 1 to 4
	f_{CLKIN}/8		For gains of 8 to 128
Reference Input Range			
REF IN(+) − REF IN(−) Voltage	1/1.75	V min/V max	V_{DD} = 2.7 V to 3.3 V V_{REF} = 1.225 ± 1% for specified performance
REF IN(+) − REF IN(−) Voltage	1/3.5	V min/V max	V_{DD} = 4.75 V to 5.25 V V_{REF} = 2.5 ± 1% for specified performance
REF IN Input Sampling Rate, f_S	f_{CLKIN}/64		
LOGIC INPUTS			
Input Current			
All Inputs, Except MCLK IN	±1	μA max	Typically ±20 nA
MCLK IN	±10	μA max	Typically ±2 μA
All Inputs, Except SCLK and MCLK IN			
Input Low Voltage, V_{INL}	0.8	V max	V_{DD} = 5 V
	0.4	V max	V_{DD} = 3 V
Input High Voltage, V_{INH}	2.0	V min	V_{DD} = 3 V and 5 V
SCLK Only (Schmitt-Triggered Input)			V_{DD} = 5 V nominal
V_{T+}	1.4/3	V min/V max	
V_{T-}	0.8/1.4	V min/V max	
$V_{T+} - V_{T-}$	0.4/0.8	V min/V max	
SCLK Only (Schmitt-Triggered Input)			V_{DD} = 3 V nominal
V_{T+}	1/2	V min/V max	
V_{T-}	0.4/1.1	V min/V max	
$V_{T+} - V_{T-}$	0.375/0.8	V min/V max	
MCLK IN Only			V_{DD} = 5 V nominal
Input Low Voltage, V_{INL}	0.8	V max	
Input High Voltage, V_{INH}	3.5	V min	
MCLK IN Only			V_{DD} = 3 V nominal
Input Low Voltage, V_{INL}	0.4	V max	
Input High Voltage, V_{INH}	2.5	V min	
LOGIC OUTPUTS (Including MCLK OUT)			
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 800 μA, except for MCLK OUT;[13] V_{DD} = 5 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 100 μA, except for MCLK OUT;[13] V_{DD} = 3 V
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 200 μA, except for MCLK OUT;[13] V_{DD} = 5 V
Output High Voltage, V_{OH}	V_{DD} − 0.6	V min	I_{SOURCE} = 100 μA, except for MCLK OUT;[13] V_{DD} = 3 V
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[14]	9	pF typ	
Data Output Coding	Binary		Unipolar mode
	Offset binary		Bipolar mode
SYSTEM CALIBRATION			
Positive Full-Scale Limit[15]	(1.05 × V_{REF})/gain	V max	Gain is the selected PGA gain (1 to 128)
Negative Full-Scale Limit[15]	−(1.05 × V_{REF})/gain	V max	Gain is the selected PGA gain (1 to 128)
Offset Limit[15]	−(1.05 × V_{REF})/gain	V max	Gain is the selected PGA gain (1 to 128)
Input Span[16]	(0.8 × V_{REF})/gain	V min	Gain is the selected PGA gain (1 to 128)
	(2.1 × V_{REF})/gain	V max	Gain is the selected PGA gain (1 to 128)

Parameter	B Version[1]	Unit	Conditions/Comments
POWER REQUIREMENTS			
V_{DD} Voltage	2.7 to 3.3	V min to V max	For specified performance
Power Supply Currents[17]			Digital I/Ps = 0 V or V_{DD}, external MCLK IN and CLKDIS = 1
	0.32	mA max	BUF bit = 0, f_{CLKIN} = 1 MHz, gains of 1 to 128
	0.6	mA max	BUF bit = 1, f_{CLKIN} = 1 MHz, gains of 1 to 128
	0.4	mA max	BUF bit = 0, f_{CLKIN} = 2.4576 MHz, gains of 1 to 4
	0.6	mA max	BUF bit = 0, f_{CLKIN} = 2.4576 MHz, gains of 8 to 128
	0.7	mA max	BUF bit = 1, f_{CLKIN} = 2.4576 MHz, gains of 1 to 4
	1.1	mA max	BUF bit = 1, f_{CLKIN} = 2.4576 MHz, gains of 8 to 128
V_{DD} Voltage	4.75 to 5.25	V min to V max	For specified performance
Power Supply Currents[17]			Digital I/Ps = 0 V or V_{DD}, external MCLK IN and CLKDIS = 1
	0.45	mA max	BUF bit = 0, f_{CLKIN} = 1 MHz, gains of 1 to 128
	0.7	mA max	BUF bit = 1, f_{CLKIN} = 1 MHz, gains of 1 to 128
	0.6	mA max	BUF bit = 0, f_{CLKIN} = 2.4576 MHz, gains of 1 to 4
	0.85	mA max	BUF bit = 0, f_{CLKIN} = 2.4576 MHz, gains of 8 to 128
	0.9	mA max	BUF bit = 1, f_{CLKIN} = 2.4576 MHz, gains of 1 to 4
	1.3	mA max	BUF bit = 1, f_{CLKIN} = 2.4576 MHz, gains of 8 to 128
Standby (Power-Down) Current[18]	16	µA max	External MCLK IN = 0 V or V_{DD}, V_{DD} = 5 V, see Figure 12
	8	µA max	External MCLK IN = 0 V or V_{DD}, V_{DD} = 3 V
Power Supply Rejection[19, 20]		dB typ	

[1] Temperature range is −40°C to +85°C.
[2] These numbers are established from characterization or design data at initial product release.
[3] A calibration is effectively a conversion; therefore, these errors are of the order of the conversion noise shown in Table 5 and Table 7. This applies after calibration at the temperature of interest.
[4] Recalibration at any temperature removes these drift errors.
[5] Positive full-scale error includes zero-scale errors (unipolar offset error or bipolar zero error) and applies to both unipolar and bipolar input ranges.
[6] Full-scale drift includes zero-scale drift (unipolar offset drift or bipolar zero drift) and applies to both unipolar and bipolar input ranges.
[7] Gain error does not include zero-scale errors. It is calculated as (full-scale error – unipolar offset error) for unipolar ranges and (full-scale error - bipolar zero error) for bipolar ranges.
[8] Gain drift does not include unipolar offset drift or bipolar zero drift. It is effectively the drift of the part if only zero-scale calibrations are performed.
[9] This common-mode voltage range is allowed, provided that the input voltage on analog inputs is not more positive than V_{DD} + 30 mV or more negative than GND − 100 mV. Parts are functional with voltages down to GND − 200 mV, but with increased leakage at high temperatures.
[10] The AD7705/AD7706 can tolerate absolute analog input voltages down to GND − 200 mV, but the leakage current increases.
[11] The analog input voltage range on AIN(+) is given with respect to the voltage on AIN(−) on the AD7705, and with respect to the voltage of the COMMON input on the AD7706. The absolute voltage on the analog inputs should not be more positive than V_{DD} + 30 mV, or more negative than GND − 100 mV for specified performance. Input voltages of GND − 200 mV can be accommodated, but with increased leakage at high temperatures.
[12] V_{REF} = REFIN(+) − REFIN(−).
[13] These logic output levels apply to the MCLK OUT only when it is loaded with one CMOS load.
[14] Sample tested at 25°C to ensure compliance.
[15] After calibration, if the analog input exceeds positive full scale, the converter outputs all 1s. If the analog input is less than negative full scale, the device outputs all 0s.
[16] These calibration and span limits apply, provided that the absolute voltage on the analog inputs does not exceed V_{DD} + 30 mV or go more negative than GND − 100 mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.
[17] When using a crystal or ceramic resonator across the MCLK pins as the clock source for the device, the V_{DD} current and power dissipation varies depending on the crystal or resonator type (see Clocking and Oscillator Circuit section).
[18] If the external master clock continues to run in standby mode, the standby current increases to 150 µA typical at 5 V and 75 µA at 3 V. When using a crystal or ceramic resonator across the MCLK pins as the clock source for the device, the internal oscillator continues to run in standby mode, and the power dissipation depends on the crystal or resonator type (see Standby Mode section).
[19] Measured at dc and applies in the selected pass band. PSRR at 50 Hz exceeds 120 dB, with filter notches of 25 Hz or 50 Hz. PSRR at 60 Hz exceeds 120 dB, with filter notches of 20 Hz or 60 Hz.
[20] PSRR depends on both gain and V_{DD}, as follows:

Gain	1	2	4	8 to 128
V_{DD} = 3 V	86	78	85	93
V_{DD} = 5 V	90	78	84	91

TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.25 V; GND = 0 V; f_{CLKIN} = 2.4576 MHz; Input Logic 0 = 0 V, Logic 1 = V_{DD}, unless otherwise noted.

Table 2. Timing Characteristics[1, 2]

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Unit	Conditions/Comments
f_{CLKIN}[3, 4]	400	kHz min	Master clock frequency (crystal oscillator or externally supplied)
	2.5	MHz max	For specified performance
$t_{CLKIN\ LO}$	0.4 × t_{CLKIN}	ns min	Master clock input low time, t_{CLKIN} = 1/f_{CLKIN}
$t_{CLKIN\ HI}$	0.4 × t_{CLKIN}	ns min	Master clock input high time
t_1	500 × t_{CLKIN}	ns nom	$\overline{DRDY}$ high time
t_2	100	ns min	$\overline{RESET}$ pulse width
Read Operation			
t_3	0	ns min	$\overline{DRDY}$ to $\overline{CS}$ setup time
t_4	120	ns min	$\overline{CS}$ falling edge to SCLK rising edge setup time
t_5[5]	0	ns min	SCLK falling edge to data valid delay
	80	ns max	V_{DD} = 5 V
	100	ns max	V_{DD} = 3.0 V
t_6	100	ns min	SCLK high pulse width
t_7	100	ns min	SCLK low pulse width
t_8	0	ns min	$\overline{CS}$ rising edge to SCLK rising edge hold time
t_9[6]	10	ns min	Bus relinquish time after SCLK rising edge
	60	ns max	V_{DD} = 5 V
	100	ns max	V_{DD} = 3.0 V
t_{10}	100	ns max	SCLK falling edge to $\overline{DRDY}$ high[7]
Write Operation			
t_{11}	120	ns min	$\overline{CS}$ falling edge to SCLK rising edge setup time
t_{12}	30	ns min	Data valid to SCLK rising edge setup time
t_{13}	20	ns min	Data valid to SCLK rising edge hold time
t_{14}	100	ns min	SCLK high pulse width
t_{15}	100	ns min	SCLK low pulse width
t_{16}	0	ns min	$\overline{CS}$ rising edge to SCLK rising edge hold time

[1] Sample tested at 25°C to ensure compliance. All input signals are specified with t_R = t_F = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[2] See Figure 19 and Figure 20.
[3] The f_{CLKIN} duty cycle range is 45% to 55%. f_{CLKIN} must be supplied whenever the AD7705/AD7706 are not in standby mode. If no clock is present, the devices can draw higher current than specified, and possibly become uncalibrated.
[4] The AD7705/AD7706 are production tested with f_{CLKIN} at 2.4576 MHz (1 MHz for some I_{DD} tests). They are guaranteed by characterization to operate at 400 kHz.
[5] These numbers are measured with the load circuit of Figure 2 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[6] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.
[7] $\overline{DRDY}$ returns high upon completion of the first read from the device after an output update. The same data can be reread while $\overline{DRDY}$ is high, but care should be taken that subsequent reads do not occur close to the next output update.

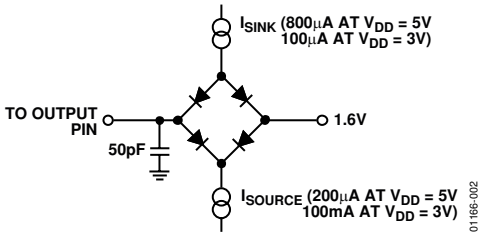

Figure 2. Load Circuit for Access Time and Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameters	Ratings
V_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Commercial (B Version)	−40°C to + 85°C
Storage Temperature Range	−65°C to + 150°C
Junction Temperature	150°C
PDIP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	105°C/W
Lead Temperature (Soldering, 10 sec)	260°C
SOIC Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	75°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
SSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	139°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD Rating	>4000 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

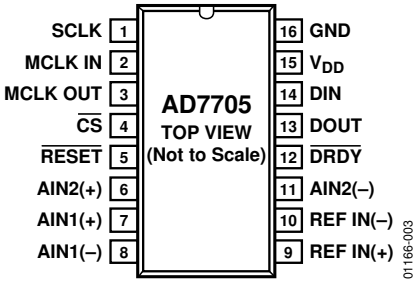

Figure 3. AD7705 Pin Configuration

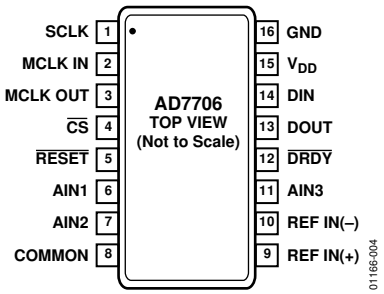

Figure 4. AD7706 Pin Configuration

Table 4. Pin Function Descriptions

	Mnemonic		
Pin No.	**AD7705**	**AD7706**	**Description**
1	SCLK	SCLK	Serial Clock. An external serial clock is applied to the Schmitt-triggered logic input to access serial data from the AD7705/AD7706. This serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information transmitted to the AD7705/AD7706 in smaller batches of data.
2	MCLK IN	MCLK IN	Master Clock Signal. This can be provided in the form of a crystal/resonator or external clock. A crystal/resonator can be tied across the Pin MCLK IN and Pin MCLK OUT. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock with the MCLK OUT pin left unconnected. The parts can be operated with clock frequencies in the range of 500 kHz to 5 MHz.
3	MCLK OUT	MCLK OUT	When the master clock for these devices is a crystal/resonator, the crystal/resonator is connected between Pin MCLK IN and Pin MCLK OUT. If an external clock is applied to Pin MCLK IN, Pin MCLK OUT provides an inverted clock signal. This clock can be used to provide a clock source for external circuitry and is capable of driving 1 CMOS load. If the user does not require this clock externally, Pin MCLK OUT can be turned off via the CLKDIS bit of the clock register. This ensures that the part does not unnecessarily burn power driving capacitive loads on Pin MCLK OUT.
4	$\overline{CS}$	$\overline{CS}$	Chip Select. Active low logic input used to select the AD7705/AD7706. With this input hardwired low, the AD7705/AD7706 can operate in its 3-wire interface mode with Pin SCLK, Pin DIN, and Pin DOUT used to interface to the device. The $\overline{CS}$ pin can be used to select the device communicating with the AD7705/AD7706.
5	$\overline{RESET}$	$\overline{RESET}$	Logic Input. Active low input that resets the control logic, interface logic, calibration coefficients, digital filter, and analog modulator of the parts to power-on status.
6	AIN2(+)	AIN1	Positive Input of the Differential Analog Input Pair AIN2(+)/AIN2(–) for AD7705. Channel 1 for AD7706.
7	AIN1(+)	AIN2	Positive Input of the Differential Analog Input Pair AIN1(+)/AIN1(–) for AD7705. Channel 2 for AD7706.
8	AIN1(–)	COMMON	Negative Input of the Differential Analog Input Pair AIN1(+)/AIN1(–) for AD7705. COMMON input for AD7706 with Channel 1, Channel 2, and Channel 3 referenced to this input.
9	REF IN(+)	REF IN(+)	Reference Input. Positive input of the differential reference input to the AD7705/AD7706. The reference input is differential with the provision that REF IN(+) must be greater than REF IN(–). REF IN(+) can lie anywhere between V_{DD} and GND.
10	REF IN(–)	REF IN(–)	Reference Input. Negative input of the differential reference input to the AD7705/AD7706. The REF IN(–) can lie anywhere between V_{DD} and GND, provided that REF IN(+) is greater than REF IN(–).
11	AIN2(–)	AIN3	Negative Input of the Differential Analog Input Pair AIN2(+)/AIN2(–) for AD7705. Channel 3 for AD7706.
12	$\overline{DRDY}$	$\overline{DRDY}$	Logic Output. A logic low on this output indicates that a new output word is available from the AD7705/AD7706 data register. The $\overline{DRDY}$ pin returns high upon completion of a read operation of a full output word. If no data read has taken place between output updates, the $\overline{DRDY}$ line returns high for 500 × $t_{CLK\ IN}$ cycles prior to the next output update. While $\overline{DRDY}$ is high, a read operation should neither be attempted nor in progress to avoid reading from the data register as it is being updated. The $\overline{DRDY}$ line returns low after the update has taken place. $\overline{DRDY}$ is also used to indicate when the AD7705/AD7706 has completed its on-chip calibration sequence.
13	DOUT	DOUT	Serial Data Output. Serial data is read from the output shift register on the part. The output shift register can contain information from the setup register, communication register, clock register, or data register, depending on the register selection bits of the communication register.

Pin No.	Mnemonic		Description
	AD7705	AD7706	
14	DIN	DIN	Serial Data Input. Serial data is written to the input shift register on the part. Data from the input shift register is transferred to the setup register, clock register, or communication register, depending on the register selection bits of the communication register.
15	V_{DD}	V_{DD}	Supply Voltage. 2.7 V to 5.25 V operation.
16	GND	GND	Ground Reference Point for the AD7705/AD7706 Internal Circuitry.

OUTPUT NOISE (5 V OPERATION)

Table 5 shows the AD7705/AD7706 output rms noise for the selectable notch and −3 dB frequencies for the parts, as selected by FS0 and FS1 of the clock register. The numbers given are for the bipolar input ranges with a V_{REF} of 2.5 V and V_{DD} = 5 V. These numbers are typical and are generated at an analog input voltage of 0 V with the parts used in either buffered or unbuffered mode. Table 6 shows the output peak-to-peak noise for the selectable notch and −3 dB frequencies for the parts.

Note that these numbers represent the resolution for which there is no code flicker. They are not calculated based on rms noise, but on peak-to-peak noise. The numbers given are for bipolar input ranges with a V_{REF} of 2.5 V for either buffered or unbuffered mode. These numbers are typical and are rounded to the nearest LSB. The numbers apply for the CLKDIV bit of the clock register set to 0.

Table 5. Output RMS Noise vs. Gain and Output Update Rate @ 5 V

Filter First Notch and O/P Data Rate	−3 dB Frequency	Typical Output RMS Noise in µV							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
50 Hz	13.1 Hz	4.1	2.1	1.2	0.75	0.7	0.66	0.63	0.6
60 Hz	15.72 Hz	5.1	2.5	1.4	0.8	0.75	0.7	0.67	0.62
250 Hz	65.5 Hz	110	49	31	17	8	3.6	2.3	1.7
500 Hz	131 Hz	550	285	145	70	41	22	9.1	4.7
MCLK IN = 1 MHz									
20 Hz	5.24 Hz	4.1	2.1	1.2	0.75	0.7	0.66	0.63	0.6
25 Hz	6.55 Hz	5.1	2.5	1.4	0.8	0.75	0.7	0.67	0.62
100 Hz	26.2 Hz	110	49	31	17	8	3.6	2.3	1.7
200 Hz	52.4 Hz	550	285	145	70	41	22	9.1	4.7

Table 6. Peak-to-Peak Resolution vs. Gain and Output Update Rate @ 5 V

Filter First Notch and O/P Data Rate	−3 dB Frequency	Typical Peak-to-Peak Resolution Bits							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
50 Hz	13.1 Hz	16	16	16	16	16	16	15	14
60 Hz	15.72 Hz	16	16	16	16	15	14	14	13
250 Hz	65.5 Hz	13	13	13	13	13	13	12	12
500 Hz	131 Hz	10	10	10	10	10	10	10	10
MCLK IN = 1 MHz									
20 Hz	5.24 Hz	16	16	16	16	16	16	15	14
25 Hz	6.55 Hz	16	16	16	16	15	14	14	13
100 Hz	26.2 Hz	13	13	13	13	13	13	12	12
200 Hz	52.4 Hz	10	10	10	10	10	10	10	10

OUTPUT NOISE (3 V OPERATION)

Table 7 shows the AD7705/AD7706 output rms noise for the selectable notch and −3 dB frequencies for the parts, as selected by FS0 and FS1 of the clock register. The numbers given are for the bipolar input ranges with a V_{REF} of 1.225 V and a V_{DD} = 3 V. These numbers are typical and are generated at an analog input voltage of 0 V with the parts used in either buffered or unbuffered mode. Table 8 shows the output peak-to-peak noise for the selectable notch and −3 dB frequencies for the parts.

Note that these numbers represent the resolution for which there is no code flicker. They are not calculated based on rms noise, but on peak-to-peak noise. The numbers given are for bipolar input ranges with a V_{REF} of 1.225 V for either buffered or unbuffered mode. These numbers are typical and are rounded to the nearest LSB. The numbers apply for the CLKDIV bit of the clock register set to 0.

Table 7. Output RMS Noise vs. Gain and Output Update Rate @ 3 V

Filter First Notch and O/P Data Rate	−3 dB Frequency	Typical Output RMS Noise in μV							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
50 Hz	13.1 Hz	3.8	2.4	1.5	1.3	1.1	1.0	0.9	0.9
60 Hz	15.72 Hz	5.1	2.9	1.7	1.5	1.2	1.0	0.9	0.9
250 Hz	65.5 Hz	50	25	14	9.9	5.1	2.6	2.3	2.0
500 Hz	131 Hz	270	135	65	41	22	9.7	5.1	3.3
MCLK IN = 1 MHz									
20 Hz	5.24 Hz	3.8	2.4	1.5	1.3	1.1	1.0	0.9	0.9
25 Hz	6.55 Hz	5.1	2.9	1.7	1.5	1.2	1.0	0.9	0.9
100 Hz	26.2 Hz	50	25	14	9.9	5.1	2.6	2.3	2.0
200 Hz	52.4 Hz	270	135	65	41	22	9.7	5.1	3.3

Table 8. Peak-to-Peak Resolution vs. Gain and Output Update Rate @ 3 V

Filter First Notch and O/P Data Rate	−3 dB Frequency	Typical Peak-to-Peak Resolution in Bits							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
50 Hz	13.1 Hz	16	16	15	15	14	13	13	12
60 Hz	15.72 Hz	16	16	15	14	14	13	13	12
250 Hz	65.5 Hz	13	13	13	13	12	12	11	11
500 Hz	131 Hz	10	10	10	10	10	10	10	10
MCLK IN = 1 MHz									
20 Hz	5.24 Hz	16	16	15	15	14	13	13	12
25 Hz	6.55 Hz	16	16	15	14	14	13	13	12
100 Hz	26.2 Hz	13	13	13	13	12	12	11	11
200 Hz	52.4 Hz	10	10	10	10	10	10	10	10

TYPICAL PERFORMANCE CHARACTERISTICS

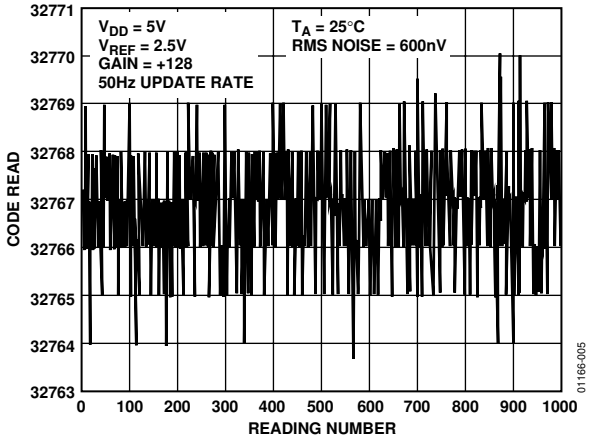

Figure 5. Noise @ Gain = +128 With 50 Hz Update Rate

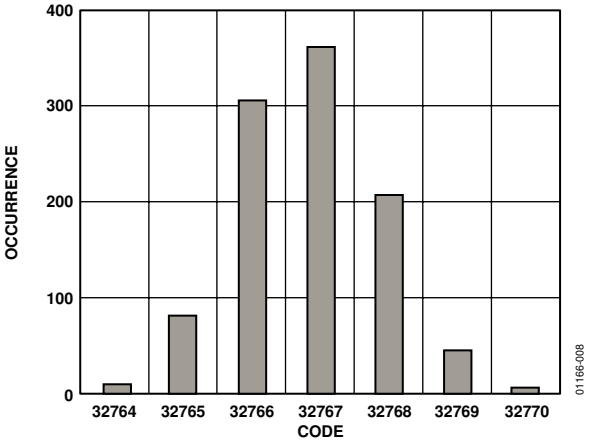

Figure 8. Histogram of Data in Figure 5

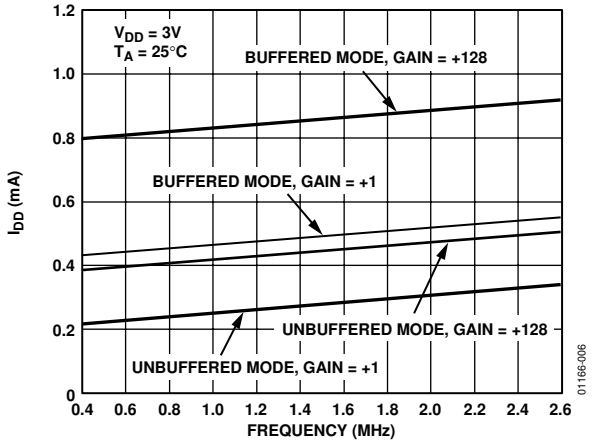

Figure 6. I_{DD} vs. MCLK IN Frequency @ 3 V

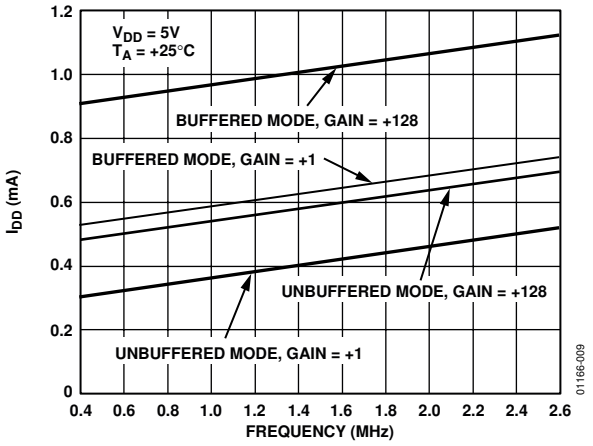

Figure 9. I_{DD} vs. MCLK IN Frequency @ 5 V

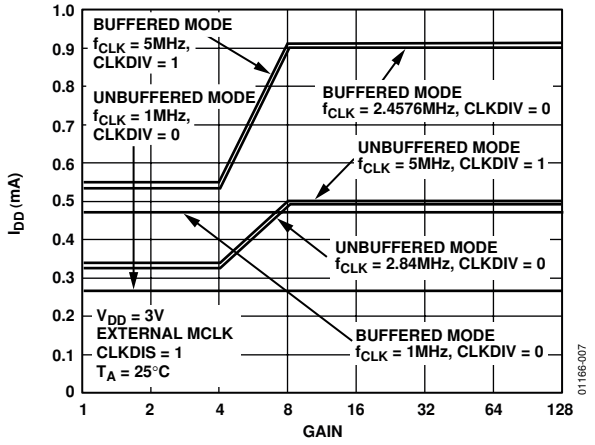

Figure 7. I_{DD} vs. Gain and Clock Frequency @ 3 V

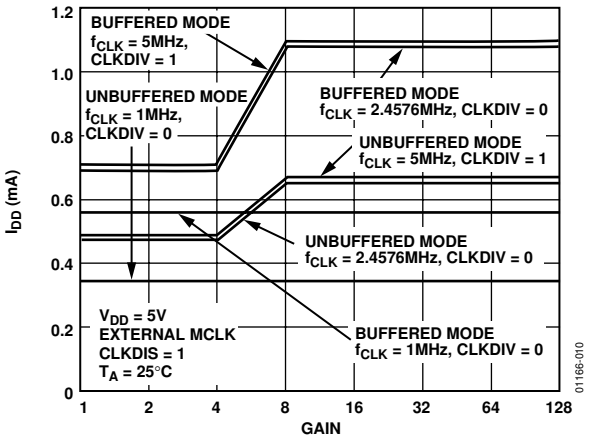

Figure 10. I_{DD} vs. Gain and Clock Frequency @ 5 V

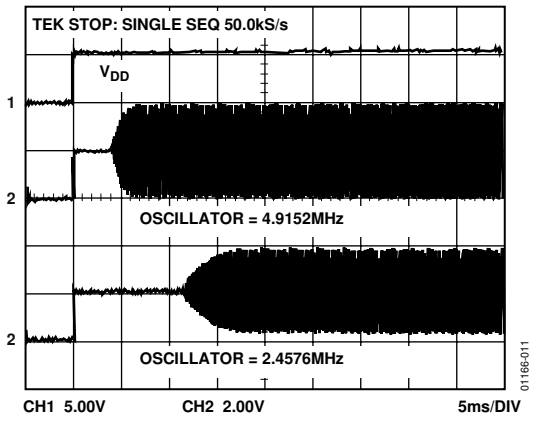

Figure 11. Crystal Oscillator Power-Up Time

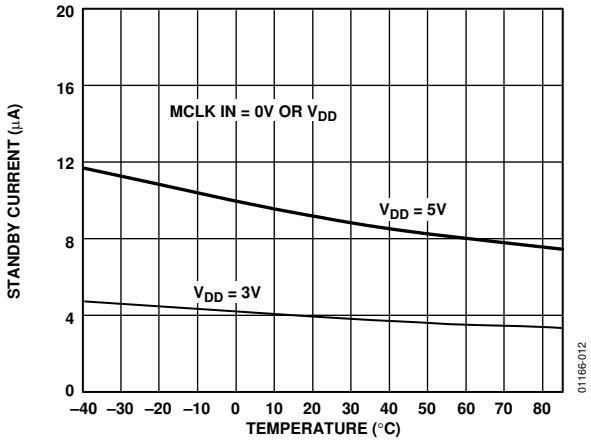

Figure 12. Standby Current vs. Temperature

ON-CHIP REGISTERS

The AD7705/AD7706 each contain eight on-chip registers that can be accessed via the serial port. The first of these is a communication register that controls the channel selection, decides whether the next operation is a read or write operation, and decides which register the next read or write operation accesses.

All communication to the AD7705/AD7706 must start with a write operation to the communication register. After a power-on or reset, the device expects a write to its communication register. The data written to this register determines whether the next operation is a read or write operation and to which register this operation occurs. Therefore, write access to any register on the part starts with a write operation to the communication register, followed by a write to the selected register. Likewise, a read operation from any register on the part, including the communication register itself and the output data register, starts with a write operation to the communication register, followed by a read operation from the selected register. The communication register also controls the standby mode and channel selection. The $\overline{\text{DRDY}}$ status is available by reading from the communication register.

The second register is a setup register that determines calibration mode, gain setting, bipolar/unipolar operation, and buffered mode. The third register is labeled the clock register and contains the filter selection bits and clock control bits. The fourth register is the data register from which the output data is accessed. The final registers are the calibration registers, which store channel calibration data. The registers are discussed in more detail in the following sections.

COMMUNICATION REGISTER (RS2, RS1, RS0 = 0, 0, 0)

The communication register is an 8-bit register from which data can be read or to which data can be written. All communication to the part must start with a write operation to its communication register. The data written to the communication register determines whether the next operation is a read or write operation and to which register this operation takes place. After the read or write operation is complete, the interface returns to its default state, where it expects a write operation to the communication register. In situations where the interface sequence is lost, a write operation of a least 32 serial clock cycles with DIN high returns the ADC to its default state by resetting the part. Table 10 outlines the bit designations for the communication register.

Table 9. Communication Register

0/$\overline{\text{DRDY}}$ (0)	RS2 (0)	RS1 (0)	RS0 (0)	R/$\overline{\text{W}}$ (0)	STBY (0)	CH1 (0)	CH0 (0)

Table 10. Communication Register Bit Description

Register	Description
0/$\overline{\text{DRDY}}$	For a write operation to the communications register, a 0 must be written to this bit. If a 1 is written to this bit, the part does not clock subsequent bits into the register. It stays at this bit location until a 0 is written. Then, the next seven bits are loaded into the communication register. For a read operation, this bit provides the status of the $\overline{\text{DRDY}}$ flag, which is the same as the $\overline{\text{DRDY}}$ output pin.
RS2–RS0	Register Selection Bits. These bits are used to select which of the AD7705/AD7706 registers are being accessed during the serial interface communication.
R/$\overline{\text{W}}$	Read/$\overline{\text{WRITE}}$ Select. This bit selects whether the next operation is a read or write operation. A 0 indicates a write cycle for the next operation to the selected register, and a 1 indicates a read operation from the selected register.
STBY	Standby. Writing 1 to this bit puts the part into standby or power-down mode. In this mode, the part consumes only 10 µA of power supply current. The part retains its calibration coefficients and control word information when in standby. Writing 0 to this bit places the parts in normal operating mode.
CH1, CH0	Channel Select. These two bits select a channel for conversion or for access to the calibration coefficients, as outlined in Table 12. Following a calibration on a channel, three pairs of calibration registers store the calibration coefficients. Table 12 (for the AD7705) and Table 13 (for the AD7706) show which channel combinations have independent calibration coefficients. With CH1 at Logic 1 and CH0 at Logic 0, the AD7705 looks at the AIN1(–) input internally shorted to itself, while the AD7706 looks at the COMMON input internally shorted to itself. This can be used as a test method to evaluate the noise performance of the parts with no external noise sources. In this mode, the AIN1(–)/COMMON input should be connected to an external voltage within the allowable common-mode range for the parts.

Table 11. Register Selection

RS2	RS1	RS0	Register	Register Size
0	0	0	Communication register	8 bits
0	0	1	Setup register	8 bits
0	1	0	Clock register	8 bits
0	1	1	Data register	16 bits
1	0	0	Test register	8 bits
1	0	1	No operation	
1	1	0	Offset register	24 bits
1	1	1	Gain register	24 bits

Table 12. Channel Selection for AD7705

CH1	CH0	AIN(+)	AIN(–)	Calibration Register Pair
0	0	AIN1(+)	AIN1(–)	Register Pair 0
0	1	AIN2(+)	AIN2(–)	Register Pair 1
1	0	AIN1(–)	AIN1(–)	Register Pair 0
1	1	AIN1(–)	AIN2(–)	Register Pair 2

Table 13. Channel Selection for AD7706

CH1	CH0	AIN	Reference	Calibration Register Pair
0	0	AIN1	COMMON	Register Pair 0
0	1	AIN2	COMMON	Register Pair 1
1	0	COMMON	COMMON	Register Pair 0
1	1	AIN3	COMMON	Register Pair 2

SETUP REGISTER (RS2, RS1, RS0 = 0, 0, 1); POWER-ON/RESET STATUS: 01 HEXADECIMAL

The setup register is an 8-bit register from which data can be read or to which data can be written.

Table 14 outlines the bit designations for the setup register.

Table 14. Setup Register

MD1 (0)	MD0 (0)	G2 (0)	G1 (0)	G0 (0)	$\overline{B}$/U (0)	BUF (0)	FSYNC (1)

Table 15. Setup Register Description

Register	Description
MD1, MD0	ADC Mode Bits. These bits select the operational mode of the ADC as outlined in Table 16.
G2 to G0	Gain Selection Bits. These bits select the gain setting for the on-chip PGA, as outlined in Table 17.
$\overline{B}$/U	Bipolar/Unipolar Operation. A 0 in this bit selects bipolar operation; a 1 in this bit selects unipolar operation.
BUF	Buffer Control. With this bit at 0, the on-chip buffer on the analog input is shorted out. With the buffer shorted out, the current flowing in the V_{DD} line is reduced. When this bit is high, the on-chip buffer is in series with the analog input, allowing the input to handle higher source impedances.
FSYNC	Filter Synchronization. When this bit is high, the nodes of the digital filter, the filter control logic, the calibration control logic, and the analog modulator are held in a reset state. When this bit goes low, the modulator and filter start to process data, and a valid word is available in 3 × 1/output rate, that is, the settling time of the filter. This FSYNC bit does not affect the digital interface and does not reset the $\overline{DRDY}$ output if it is low.

Table 16. Operating Mode Options

MD1	MD0	Operating Mode
0	0	Normal Mode. In this mode, the device performs normal conversions.
0	1	Self-Calibration. This activates self-calibration on the channel selected by CH1 and CH0 of the communication register. This is a one-step calibration sequence. When the sequence is complete, the part returns to normal mode, with both MD1 and MD0 returning to 0. The DRDY output or bit goes high when calibration is initiated, and returns low when self-calibration is complete and a new valid word is available in the data register. The zero-scale calibration is performed at the selected gain on internally shorted (zeroed) inputs, and the full-scale calibration is performed at the selected gain on an internally generated V_{REF}/selected gain.
1	0	Zero-Scale System Calibration. This activates zero-scale system calibration on the channel selected by CH1 and CH0 of the communication register. Calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. The DRDY output or bit goes high when calibration is initiated, and returns low when zero-scale calibration is complete and a new valid word is available in the data register. At the end of the calibration, the part returns to normal mode, with both MD1 and MD0 returning to 0.
1	1	Full-Scale System Calibration. This activates full-scale system calibration on the selected input channel. Calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. The DRDY output or bit goes high when calibration is initiated, and returns low when full-scale calibration is complete and a new valid word is available in the data register. At the end of the calibration, the part returns to normal mode, with both MD1 and MD0 returning to 0.

Table 17. Gain Selection

G2	G1	G0	Gain Setting
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

CLOCK REGISTER (RS2, RS1, RS0 = 0, 1, 0); POWER-ON/RESET STATUS: 05 HEXADECIMAL

The clock register is an 8-bit register from which data can be read or to which data can be written.

Table 18 outlines the bit designations for the clock register.

Table 18. Clock Register

ZERO (0)	ZERO (0)	ZERO (0)	CLKDIS (0)	CLKDIV (0)	CLK (1)	FS1 (0)	FS0 (1)

Table 19. Clock Register Description

Register	Description
ZERO	Zero. A zero must be written to these bits to ensure correct operation of the AD7705/AD7706. Failure to do so might result in unspecified operation of the device.
CLKDIS	Master Clock Disable Bit. Logic 1 in this bit disables the master clock, preventing it from appearing at the MCLK OUT pin. When disabled, the MCLK OUT pin is forced low. This feature allows the user the flexibility of either using the MCLK OUT as a clock source for other devices in the system, or turning off the MCLK OUT as a power-saving feature. When using an external master clock on the MCLK IN pin, the AD7705/AD7706 continue to have internal clocks and convert normally with the CLKDIS bit active. When using a crystal oscillator or ceramic resonator across Pin MCLK IN and Pin MCLK OUT, the AD7705/AD7706 clocks are stopped, and no conversions take place when the CLKDIS bit is active.
CLKDIV	Clock Divider Bit. With this bit at Logic 1, the clock frequency appearing at the MCLK IN pin is divided by 2 before being used internally by the AD7705/AD7706. For example, when this bit is set to Logic 1, the user can operate with a 4.9152 MHz crystal between Pin MCLK IN and Pin MCLK OUT, and internally the part operates with the specified 2.4576 MHz. With this bit at Logic 0, the clock frequency appearing at the MCLK IN pin is the frequency used internally by the part.
CLK	Clock Bit. This bit should be set in accordance with the operating frequency of the AD7705/AD7706. If the device has a master clock frequency of 2.4576 MHz (CLKDIV = 0) or 4.9152 MHz (CLKDIV = 1), this bit should be set to Logic 1. If the device has a master clock frequency of 1 MHz (CLKDIV = 0) or 2 MHz (CLKDIV = 1), this bit should be set to Logic 0. This bit sets up the appropriate scaling currents for a given operating frequency and, together with FS1 and FS0, chooses the output update rate for the device. If this bit is not set correctly for the master clock frequency of the device, the AD7705/AD7706 might not operate to specification.
FS1, FS0	Filter Selection Bits. Along with the CLK bit, FS1 and FS0 determine the output update rate, the filter's first notch, and the −3 dB frequency, as outlined in Table 20. The on-chip digital filter provides a sinc^3 (or $(\text{sinx/x})^3$) filter response. In association with the gain selection, it also determines the output noise of the device. Changing the filter notch frequency, as well as the selected gain, impacts resolution. Table 5 through Table 8 show the effects of filter notch frequency and gain on the output noise and effective resolution of the part. The output data rate, or effective conversion time, for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, a new word is available at a 50 Hz output rate, or every 20 ms. If the first notch is at 500 Hz, a new word is available every 2 ms. A calibration should be initiated when any of these bits are changed. The settling time of the filter to a full-scale step input is worst case 4 × 1/(output data rate). For example, with the filter-first notch at 50 Hz, the settling time of the filter to a full-scale step input is 80 ms maximum. If the first notch is at 500 Hz, the settling time is 8 ms maximum. This settling time can be reduced to 3 × 1/(output data rate) by synchronizing the step input change with a reset of the digital filter. In other words, if the step input takes place with the FSYNC bit high, the settling time is 3 × 1/(output data rate) from the time when the FSYNC bit returns low. The −3 dB frequency is determined by the programmed first notch frequency according to the relationship: $filter - 3\text{ dB}\ frequency = 0.262 \times filter\text{ - }first\ notch\ frequency$

Table 20. Output Update Rates

CLK[1]	FS1	FS0	Output Update Rate	−3 dB Filter Cutoff
0	0	0	20 Hz	5.24 Hz
0	0	1	25 Hz	6.55 Hz
0	1	0	100 Hz	26.2 Hz
0	1	1	200 Hz	52.4 Hz
1	0	0	50 Hz	13.1 Hz
1	0	1	60 Hz	15.7 Hz
1	1	0	250 Hz	65.5 Hz
1	1	1	500 Hz	131 Hz

[1] Assumes correct clock frequency on MCLK IN pin with the CLKDIV bit set appropriately.

DATA REGISTER (RS2, RS1, RS0 = 0, 1, 1)

The data register is a 16-bit, read-only register that contains the most up-to-date conversion result from the AD7705/AD7706. If the communication register sets up the part for a write operation to this register, a write operation must take place to return the part to its default state. However, the 16 bits of data written to the part will be ignored by the AD7705/AD7706.

TEST REGISTER (RS2, RS1, RS0 = 1, 0, 0); POWER-ON/RESET STATUS: 00 HEXADECIMAL

The part contains a test register that is used when testing the device. The user is advised not to change the status of any of the bits in this register from the default (power-on or reset) status of all 0s, because the part will be placed in one of its test modes and will not operate correctly.

ZERO-SCALE CALIBRATION REGISTER (RS2, RS1, RS0 = 1, 1, 0); POWER-ON/RESET STATUS: 1F4000 HEXADECIMAL

The AD7705/AD7706 contain independent sets of zero-scale registers, one for each of the input channels. Each register is a 24-bit read/write register; therefore, 24 bits of data must be written, or no data is transferred to the register. This register is used in conjunction with its associated full-scale register to form a register pair. These register pairs are associated with input channel pairs, as outlined in Table 12 and Table 13.

While the part is set up to allow access to these registers over the digital interface, the parts themselves can no longer access the register coefficients to scale the output data correctly. As a result, the first output data read from the part after accessing the calibration registers (for either a read or write operation) might contain incorrect data. In addition, a write to the calibration register should not be attempted while a calibration is in progress. These eventualities can be avoided by taking the FSYNC bit in the mode register high before the calibration register operation, and taking it low after the operation is complete.

FULL-SCALE CALIBRATION REGISTER (RS2, RS1, RS0 = 1, 1, 1); POWER-ON/RESET STATUS: 5761AB HEXADECIMAL

The AD7705/AD7706 contain independent sets of full-scale registers, one for each of the input channels. Each register is a 24-bit read/write register; therefore, 24 bits of data must be written, or no data is transferred to the register. This register is used in conjunction with its associated zero-scale register to form a register pair. These register pairs are associated with input channel pairs, as outlined in Table 12 and Table 13.

While the part is set up to allow access to these registers over the digital interface, the part itself can no longer access the register coefficients to scale the output data correctly. As a result, the first output data read from the part after accessing the calibration registers (for either a read or write operation) might contain incorrect data. In addition, a write to the calibration register should not be attempted while a calibration is in progress. These eventualities can be avoided by taking FSYNC bit in the mode register high before the calibration register operation, and taking it low after the operation is complete.

Calibration Sequences

The AD7705/AD7706 contain a number of calibration options, as previously outlined. Table 21 summarizes the calibration types, the operations involved, and the duration of the operations. There are two methods for determining the end of a calibration. The first is to monitor when $\overline{\text{DRDY}}$ returns low at the end of the sequence. This technique not only indicates when the sequence is complete, but also when the part has a valid new sample in its data register. This valid new sample is the result of a normal conversion that follows the calibration sequence. The second method for determining when calibration is complete is to monitor the MD1 and MD0 bits of the setup register. When these bits return to 0 following a calibration command, the calibration sequence is complete. This technique can indicate the completion of a calibration earlier than the first method can, but it cannot indicate when there is a valid new result in the data register. The time that it takes the mode bits, MD1 and MD0, to return to 0 represents the duration of the calibration. The sequence when $\overline{\text{DRDY}}$ goes low includes a normal conversion and a pipeline delay, t_P, to scale the results of this first conversion correctly. Note that t_P never exceeds 2000 × t_{CLKIN}. The time for both methods is shown in Table 21.

Table 21. Calibration Sequences

Calibration Type	MD1, MD0	Calibration Sequence	Duration of Mode Bits	Duration of $\overline{\text{DRDY}}$
Self-Calibration	0, 1	Internal ZS calibration @ selected gain + internal FS calibration @ selected gain	6 × 1/output rate	9 × 1/output rate + t_P
ZS System Calibration	1, 0	ZS calibration on AIN @ selected gain	3 × 1/output rate	4 × 1/output rate + t_P
FS System Calibration	1, 1	FS calibration on AIN @ selected gain	3 × 1/output rate	4 × 1/output rate + t_P

CIRCUIT DESCRIPTION

The AD7705/AD7706 are Σ-Δ analog-to-digital converters (ADC) with on-chip digital filtering, intended for the measurement of wide, dynamic range, low frequency signals, such as those in industrial-control or process-control applications. Each contains a Σ-Δ (or charge-balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter, and a bidirectional serial communication port. The parts consume only 320 μA of power supply current, making them ideal for battery-powered or loop-powered instruments. These parts operate with a supply voltage of 2.7 V to 3.3 V or 4.75 V to 5.25 V.

The AD7705 contains two programmable-gain, fully differential analog input channels, and the AD7706 contains three pseudo differential analog input channels. The selectable gains on these inputs are 1, 2, 4, 8, 16, 32, 64, and 128, allowing the parts to accept unipolar signals of 0 mV to 20 mV and 0 V to 2.5 V, or bipolar signals in the range of ±20 mV to ±2.5 V when the reference input voltage equals 2.5 V. With a reference voltage of 1.225 V, the input ranges are from 0 mV to 10 mV and 0 V to 1.225 V in unipolar mode, and from ±10 mV to ±1.225 V in bipolar mode. Note that the bipolar ranges are with respect to AIN(–) on the AD7705, and with respect to COMMON on the AD7706, but not with respect to GND.

The input signal to the analog input is continuously sampled at a rate determined by the frequency of the master clock, MCLK IN, and the selected gain. A charge-balancing ADC (Σ-Δ modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this Σ-Δ modulator, with the input sampling frequency being modified to provide higher gains. A sinc^3, digital, low-pass filter processes the output of the Σ-Δ modulator and updates the output register at a rate determined by the first notch frequency of this filter.

The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The frequency of the first notch of the digital filter ranges from 50 Hz to 500 Hz; therefore, the programmable range for the −3 dB frequency is 13.1 Hz to 131 Hz. With a master clock frequency of 1 MHz, the programmable range for this first notch frequency is 20 Hz to 200 Hz, giving a programmable range for the −3 dB frequency of 5.24 Hz to 52.4 Hz.

The AD7705 basic connection diagram is shown in Figure 13. It shows the AD7705 driven from an analog 5 V supply. An AD780 or REF192 precision 2.5 V reference provides the reference source for the part. On the digital side, the part is configured for 3-wire operation with $\overline{CS}$ tied to GND. A quartz crystal or ceramic resonator provides the master clock source for the part. In most cases, it is necessary to connect capacitors on the crystal or resonator to ensure that it does not oscillate at overtones of its fundamental operating frequency. The values of capacitors vary, depending on the manufacturer's specifications. The same setup applies to the AD7706.

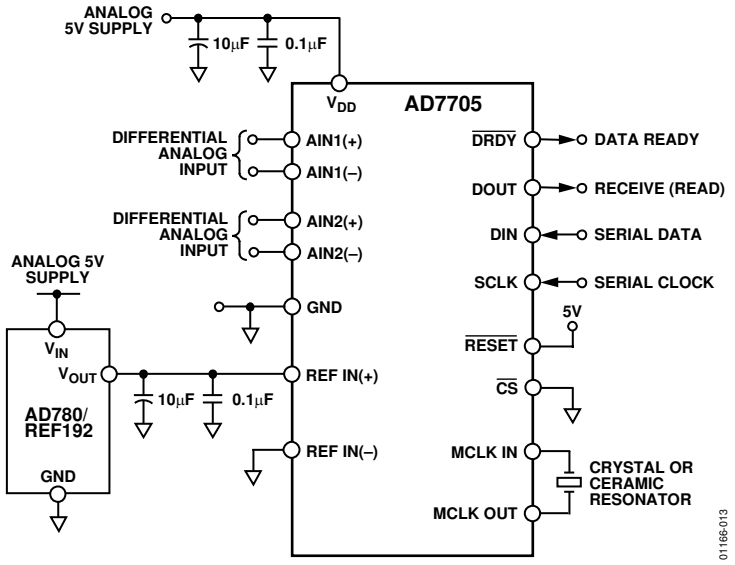

Figure 13. AD7705 Basic Connection Diagram

ANALOG INPUT

Ranges

The AD7705 contains two differential analog input pairs, AIN1(+)/AIN1(−) and AIN2(+)/AIN2(−). These input pairs provide programmable-gain, differential input channels that can handle either unipolar or bipolar input signals. It should be noted that the bipolar input signals are referenced to the respective AIN(−) input of each input pair. The AD7706 contains three pseudo differential analog input pairs, AIN1, AIN2, and AIN3, which are referenced to the COMMON input.

In unbuffered mode, the common-mode range of the input is from GND to V_{DD}, provided that the absolute value of the analog input voltage lies between GND − 100 mV and V_{DD} + 30 mV. Therefore, in unbuffered mode, the part can handle both unipolar and bipolar input ranges for all gains. The AD7705 can tolerate absolute analog input voltages down to GND − 200 mV, but the leakage current increases at high temperatures. In buffered mode, the analog inputs can handle much larger source impedances, but the absolute input voltage range is restricted to between GND + 50 mV and V_{DD} − 1.5 V, which also restricts the common-mode range. Therefore, in buffered mode, there are some restrictions on the allowable gains for bipolar input ranges. Care must be taken in setting up the common-mode voltage and input voltage ranges so that the above limits are not exceeded; otherwise, there is a degradation in linearity performance.

In unbuffered mode, the analog inputs look directly into the 7 pF input sampling capacitor, C_{SAMP}. The dc input leakage current in this unbuffered mode is 1 nA maximum. As a result, the analog inputs see a dynamic load that is switched at the input sample rate (see Figure 14). This sample rate depends on master clock frequency and selected gain. C_{SAMP} is charged to AIN(+) and discharged to AIN(−) every input sample cycle. The effective on resistance of the switch, R_{SW}, is typically 7 kΩ.

C_{SAMP} must be charged through R_{SW} and any external source impedances every input sample cycle. Therefore, in unbuffered mode, source impedances mean a longer charge time for C_{SAMP}, which might result in gain errors on the parts. Table 22 shows the allowable external resistance-capacitance values for unbuffered mode, such that no gain error to the 16-bit level is introduced in the part. Note that these capacitances are total capacitances on the analog input—external capacitance plus 10 pF capacitance from the pins and lead frame of the devices.

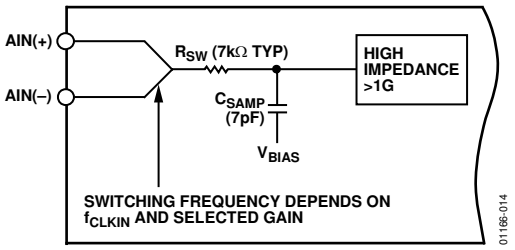

Figure 14. Unbuffered Analog Input Structure

Table 22. External Resistance-Capacitance Combination for Unbuffered Mode (Without 16-Bit Gain Error)

	External Capacitance (pF)					
Gain	**10**	**50**	**100**	**500**	**1000**	**5000**
1	152 kΩ	53.9 kΩ	31.4 kΩ	8.4 kΩ	4.76 kΩ	1.36 kΩ
2	75.1 kΩ	26.6 kΩ	15.4 kΩ	4.14 kΩ	2.36 kΩ	670 Ω
4	34.2 kΩ	12.77 kΩ	7.3 kΩ	1.95 kΩ	1.15 kΩ	320 Ω
8 to 128	16.7 kΩ	5.95 kΩ	3.46 kΩ	924 Ω	526 Ω	150 Ω

In buffered mode, the analog inputs look into the high impedance inputs stage of the on-chip buffer amplifier. C_{SAMP} is charged via this buffer amplifier such that source impedances do not affect the charging of C_{SAMP}. This buffer amplifier has an offset leakage current of 1 nA. In this buffered mode, large source impedances result in a small dc offset voltage developed across the source impedance, but not in a gain error.

Sample Rate

The modulator sample frequency for the AD7705/AD7706 remains at $f_{CLKIN}/128$ (19.2 kHz @ f_{CLKIN} = 2.4576 MHz), regardless of the selected gain. However, gains greater than 1 are achieved by a combination of multiple input samples per modulator cycle and a scaling of the ratio of reference capacitor to input capacitor. As a result of the multiple sampling, the input sample rate of these devices varies with the selected gain (see Table 23). In buffered mode, the input is buffered before the input sampling capacitor. In unbuffered mode, where the analog input looks directly into the sampling capacitor, the effective input impedance is $1/C_{SAMP} \times f_S$, where C_{SAMP} is the input sampling capacitance and f_S is the input sample rate.

Table 23. Input Sampling Frequency vs. Gain

Gain	Input Sampling Frequency (f_S)
1	$f_{CLKIN}/64$ (38.4 kHz @ f_{CLKIN} = 2.4576 MHz)
2	$2 \times f_{CLKIN}/64$ (76.8 kHz @ f_{CLKIN} = 2.4576 MHz)
4	$4 \times f_{CLKIN}/64$ (76.8 kHz @ f_{CLKIN} = 2.4576 MHz)
8 to 128	$8 \times f_{CLKIN}/64$ (307.2 kHz @ f_{CLKIN} = 2.4576 MHz)

BIPOLAR/UNIPOLAR INPUT

The analog inputs on the AD7705/AD7706 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that these parts can handle negative voltages on their analog inputs; the analog inputs cannot go more negative than −100 mV to ensure correct operation of these parts. The input channels are fully differential. As a result, on the AD7705, the voltage to which the unipolar and bipolar signals on the AIN(+) input are referenced is the voltage on the respective AIN(−) input.

On the AD7706, the voltages applied to the analog input channels are referenced to the COMMON input. For example, if AIN1(−) is 2.5 V and AD7705 is configured for unipolar operation with a gain of 2 and a V_{REF} of 2.5 V, the input voltage range on the AIN1(+) input is 2.5 V to 3.75 V.

If AIN1(−) is 2.5 V and AD7705 is configured for bipolar mode with a gain of 2 and a V_{REF} of 2.5 V, the analog input range on the AIN1(+) input is 1.25 V to 3.75 V (i.e., 2.5 V ± 1.25 V). If AIN1(−) is at GND, the part cannot be configured for bipolar ranges in excess of ±100 mV.

Bipolar or unipolar options are chosen by programming the $\overline{B}$/U bit of the setup register. This programs the channel for either unipolar or bipolar operation. Programming the channel for either unipolar or bipolar operation does not change the input signal conditioning, it simply changes the data output coding and the points on the transfer function where calibrations occur.

REFERENCE INPUT

The AD7705/AD7706 reference inputs, REF IN(+) and REF IN(−), provide a differential reference input capability. The common-mode range for these differential inputs is from GND to V_{DD}. The nominal reference voltage, V_{REF} (REF IN(+) − REF IN(−)), for specified operation is 2.5 V for the AD7705/AD7706 operated with a V_{DD} of 5 V, and 1.225 V for the AD7705/AD7706 operated with a V_{DD} of 3 V. The parts are functional with V_{REF} voltages down to 1 V, but performance will be degraded because the output noise, in terms of LSB size, is larger. REF IN(+) must be greater than REF IN(−) for correct operation of the AD7705/AD7706.

Both reference inputs provide a high impedance, dynamic load similar to the analog inputs in unbuffered mode. The maximum dc input leakage current is ±1 nA over temperature, and source resistance might result in gain errors on the part. In this case, the sampling switch resistance is 5 kΩ typ, and the reference capacitor, C_{REF}, varies with gain. The sample rate on the reference inputs is $f_{CLKIN}/64$ and does not vary with gain. For gains of 1 and 2, C_{REF} is 8 pF; for gains of 16, 32, 64, and 128, it is 5.5 pF, 4.25 pF, 3.625 pF, and 3.3125 pF, respectively.

The output noise performance outlined in Table 5, Table 6, Table 7, and Table 8 is for an analog input of 0 V, which effectively removes the effect of noise on the reference. To obtain the noise performance shown in the noise tables over the full input range requires a low noise reference source for the AD7705/AD7706. If the reference noise in the bandwidth of interest is excessive, it degrades the performance of the AD7705/AD7706. In applications where the excitation voltage for the bridge transducer on the analog input also derives the reference voltage for the part, the effect of the noise in the excitation voltage is removed because the application is ratiometric.

Recommended reference voltage sources for the AD7705/AD7706 with a V_{DD} of 5 V include the AD780, REF43, and REF192; the recommended reference sources for the AD7705/AD7706 operated with a V_{DD} of 3 V include the AD589 and AD1580. It is generally recommended to decouple the output of these references to reduce the noise level further.

DIGITAL FILTERING

The AD7705/AD7706 each contain an on-chip, low-pass digital filter that processes the output of the Σ-Δ modulator. Therefore, the parts not only provide the ADC function, but also provide a level of filtering. There are a number of system differences when the filtering function is provided in the digital domain, rather than in the analog domain.

For example, because it occurs after the A/D conversion process, digital filtering can remove noise injected during the conversion process, whereas analog filtering cannot do this. In addition, the digital filter can be made programmable far more readily than the analog filter. Depending on the digital filter design, this provides the user with the update rate.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this, and noise peaks riding on signals near full scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits.

To alleviate this problem, the AD7705/AD7706 have overrange headroom built into the Σ-Δ modulator and digital filter that allows overrange excursions of 5% above the analog input range. If noise signals are larger than this, consider filtering the analog input, or reducing the input channel voltage so that its full scale is half that of the analog input channel full scale. This provides an overrange capability greater than 100% at the expense of reducing the dynamic range by 1 bit (50%).

In addition, the digital filter does not provide any rejection at integer multiples of the digital filter's sample frequency. However, the input sampling on the part provides attenuation at multiples of the digital filter's sampling frequency so that the unattenuated bands occur around multiples of the sampling frequency, f_S, as defined in Table 23. Thus, the unattenuated bands occur at $n \times f_S$ (where n = 1, 2, 3 . . .). At these frequencies, there are frequency bands $\pm f_{3\,dB}$ wide ($f_{3\,dB}$ is the cutoff frequency of the digital filter) at either side where noise passes unattenuated to the output.

Filter Characteristics

The AD7705/AD7706 digital filter is a low-pass filter with a $(\sin x/x)^3$ response (also called sinc^3). The transfer function for the filter is described in the z-domain by

$$H(z)\left|\frac{1}{N}\times\frac{1-Z^{-N}}{1-Z^{-1}}\right|^3$$

and in the frequency domain by

$$H(f)=\left|\frac{1}{N}\times\frac{\sin\left(N\times\pi\times f/f_S\right)}{\sin\left(\pi\times f/f_S\right)}\right|^3$$

where N is the ratio of the modulator rate to the output rate.

The phase response is defined by the following equation:

$$\angle H=-3\pi\left(N-2\right)\times f/f_S\ Rad$$

Figure 15 shows the filter frequency response for a cutoff frequency of 15.72 Hz, which corresponds to a first filter notch frequency of 60 Hz. The plot is shown from dc to 390 Hz. This response is repeated at either side of the digital filter's sample frequency and at either side of multiples of the filter's sample frequency.

The response of the filter is similar to that of an averaging filter, but with a sharper roll-off. The output rate for the digital filter corresponds with the positioning of the first notch of the filter's frequency response. Thus, for Figure 15, where the output rate is 60 Hz, the first notch of the filter is at 60 Hz. The notches of this $(\sin x/x)^3$ filter are repeated at multiples of the first notch. The filter provides attenuation of better than 100 dB at these notches.

The cutoff frequency of the digital filter is determined by the value loaded to Bit FS0 and Bit FS1 in the clock register. Programming a different cutoff frequency via Bit FS0 and Bit FS1 does not alter the profile of the filter response, but changes the frequency of the notches. The output update of the part and the frequency of the first notch correspond.

Because the AD7705/AD7706 contain this on-chip, low-pass filtering, a settling time is associated with step function inputs, and data on the output is invalid after a step change until the settling time has elapsed. The settling time depends on the output rate chosen for the filter. The settling time of the filter to a full-scale step input can be up to four times the output data period. For a synchronized step input using the FSYNC function, the settling time is three times the output data period.

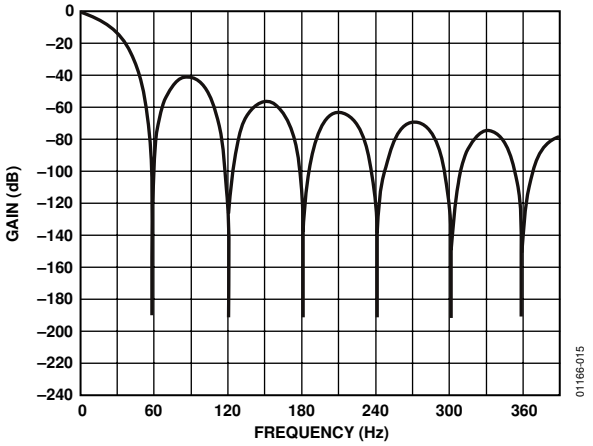

Figure 15. Frequency Response of AD7705 Filter

Postfiltering

The on-chip modulator provides samples at a 19.2 kHz output rate with f_{CLKIN} at 2.4576 MHz. The on-chip digital filter decimates these samples to provide data at an output rate that corresponds to the programmed output rate of the filter. Because the output data rate is higher than the Nyquist criterion, the output rate for a given bandwidth satisfies most application requirements. Some applications, however, might require a higher data rate for a given bandwidth and noise performance. Applications that need this higher data rate will require postfiltering following the digital filtering performed by the AD7705/AD7706.

For example, if the required bandwidth is 7.86 Hz, but the required update rate is 100 Hz, data can be taken from the AD7705/AD7706 at the 100 Hz rate, giving a −3 dB bandwidth of 26.2 Hz. Postfiltering can then be applied to reduce the bandwidth and output noise to the 7.86 Hz bandwidth level while maintaining an output rate of 100 Hz.

Postfiltering can also be used to reduce the output noise from the devices for bandwidths below 13.1 Hz. At a gain of 128 and a bandwidth of 13.1 Hz, the output rms noise is 450 nV. This is essentially device noise, or white noise. Because the input is chopped, the noise has a primarily flat frequency response. By reducing the bandwidth below 13.1 Hz, the noise in the resultant pass band is reduced. A reduction in bandwidth by a factor of 2 results in a reduction of approximately 1.25 in the output rms noise. This additional filtering results in a longer settling time.

ANALOG FILTERING

The digital filter does not provide any rejection at integer multiples of the modulator sample frequency, as outlined earlier. However, due to the part's high oversampling ratio, these bands occupy only a small fraction of the spectrum, and most broadband noise is filtered. Therefore, the analog filtering requirements in front of the AD7705/AD7706 are considerably reduced vs. a conventional converter without on-chip filtering. In addition, because the parts' common-mode rejection performance of 100 dB extends to several kHz, common-mode noise in this frequency range is substantially reduced.

Depending on the application, however, it might be necessary to provide attenuation of the signal before it reaches the AD7705/AD7706 to eliminate unwanted frequencies that can pass through the digital filter. It might also be necessary to provide analog filtering in front of the AD7705/AD7706 to ensure that differential noise signals outside the band of interest do not saturate the analog modulator.

If passive components are placed in front of the AD7705/AD7706 in unbuffered mode, care must be taken to ensure that the source impedance is low enough not to introduce gain errors in the system. This significantly limits the amount of passive antialiasing filtering, which can be provided in front of the AD7705/AD7706 when the parts are used in unbuffered mode. However, when the parts are used in buffered mode, large source impedances result in a small dc offset error (a 10 kΩ source resistance causes an offset error of less than 10 μV). Therefore, if the system requires significant source impedances to provide passive analog filtering in front of the AD7705/AD7706, it is recommended to operate the part in buffered mode.

CALIBRATION

The AD7705/AD7706 provide a number of calibration options that can be programmed via the MD1 and MD0 bits of the setup register. The different calibration options are outlined in the Setup Register (RS2, RS1, RS0 = 0, 0, 1); Power-On/Reset Status: 01 Hex, and Calibration Sequences sections. A calibration cycle can be initiated at any time by writing to these bits of the setup register. Calibration on the AD7705/AD7706 removes offset and gain errors from the devices. A calibration routine should be initiated on these devices whenever there is a change in the ambient operating temperature or supply voltage. It should also be initiated if there is a change in the selected gain, filter notch, or bipolar/unipolar input range.

The AD7705/AD7706 offer self-calibration and system calibration facilities. For full calibration to occur on the selected channel, the on-chip microcontroller must record the modulator output for two input conditions: zero-scale point and full-scale point. These points are derived by performing a conversion on the different input voltages provided to the input of the modulator during calibration. As a result, the accuracy of the calibration is only as good as the noise level that it provides in normal mode.

The result of the zero-scale calibration conversion is stored in the zero-scale calibration register, and the result of the full-scale calibration conversion is stored in the full-scale calibration register. With these readings, the microcontroller can calculate the offset and the gain slope for the input-to-output transfer function of the converter. Internally, the part works with a resolution of 33 bits to determine the conversion result of 16 bits.

Self-Calibration

A self-calibration is initiated on the AD7705/AD7706 by writing the appropriate values (0, 1) to the MD1 and MD0 bits of the setup register. In self-calibration mode with a unipolar input range, the zero-scale point used to determine the calibration coefficients is with the inputs of the differential pair internally shorted on the part (i.e., AIN(+) = AIN(−) = internal bias voltage on the AD7705, and AIN = COMMON = internal bias voltage on the AD7706). The PGA is set for the selected gain for this zero-scale calibration conversion, as per the G1 and G0 bits in the communication register. The full-scale calibration conversion is performed at the selected gain on an internally generated voltage of V_{REF}/selected gain.

The duration time for the calibration is 6 × 1/output rate. This is composed of 3 × 1/output rate for the zero-scale calibration and 3 × 1/output rate for the full-scale calibration. Then, the MD1 and MD0 bits in the setup register return to 0, 0. This provides the earliest indication that the calibration sequence is complete. The $\overline{\text{DRDY}}$ line goes high when calibration is initiated and does not return low until there is a valid new word in the data register. The duration time from the calibration command being issued to $\overline{\text{DRDY}}$ going low is 9 × 1/output rate. This is composed of 3 × 1/output rate for the zero-scale calibration, 3 × 1/output rate for the full-scale calibration, 3 × 1/output rate for a conversion on the analog input, and some overhead to set up the coefficients correctly. If $\overline{\text{DRDY}}$ is low before (or goes low during) writing the calibration command to the setup register, it can take up to one modulator cycle (MCLK IN/128) before $\overline{\text{DRDY}}$ goes high to indicate that a calibration is in progress. Therefore, $\overline{\text{DRDY}}$ should be ignored for one modulator cycle after the last bit is written to the setup register in the calibration command.

For bipolar input ranges in the self-calibrating mode, the sequence is very similar to that outlined in the previous paragraph. In this case, the two points are the same as above, but the shorted inputs point is midscale of the transfer function because the part is configured for bipolar operation.

System Calibration

System calibration allows the AD7705/AD7706 to compensate for system gain and offset errors, as well as their own internal errors. System calibration performs the same slope factor calculations as self-calibration, but uses voltage values presented by the system to the AIN inputs for the zero- and full-scale points. Full system calibration requires a two-step process, a zero-scale system calibration followed by a full-scale system calibration.