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16-Bit Σ-Δ ADC with Switchable Current Sources

AD7709

FEATURES

16-Bit Σ-Δ ADC
Programmable Gain Front End
Simultaneous 50 Hz and 60 Hz Rejection at 20 Hz Update Rate
***VREF Select*™ Allows Absolute and Ratiometric Measurement Capability**
***ISOURCE Select*™**
16-Bit No Missing Codes
13-Bit p-p Resolution @ 20 Hz, 20 mV Range
16-Bit p-p Resolution @ 20 Hz, 2.56 V Range

INTERFACE

3-Wire Serial
SPI®, QSPI™, MICROWIRE™, and DSP Compatible
Schmitt Trigger on SCLK

POWER

Specified for Single 3 V and 5 V Operation
Normal: 1.25 mA Typ @ 3 V
Power-Down: 7 μA (32.768 kHz Crystal Running)

ON-CHIP FUNCTIONS

Rail-to-Rail Input Buffer and PGA
Selectable Reference Inputs
3 Switchable, Ratioed Current Sources for V_{BE} Measurements
4-Bit Digital I/O Port
Low-Side Power Switches

APPLICATIONS

Sensor Measurement
Temperature Measurement
Pressure Measurements
Weigh Scales
Portable Instrumentation
4–20 mA Loops

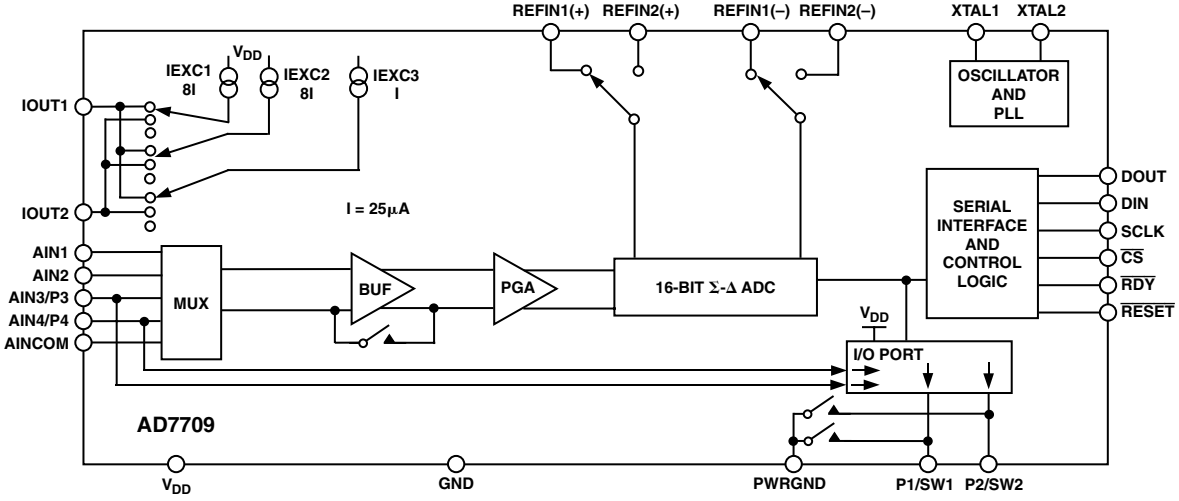
GENERAL DESCRIPTION

The AD7709 is a complete analog front end for low frequency measurement applications. It contains a 16-bit Σ-Δ ADC, selectable reference inputs, three switchable matched excitation current sources, low-side power switches, and a digital I/O port. The 16-bit channel with PGA accepts fully differential, unipolar, and bipolar input signal ranges from 1.024 × REFIN/128 to 1.024 × REFIN. It can be configured as two fully differential input channels or four pseudo-differential input channels. Signals can be converted directly from a transducer without the need for signal conditioning.

The device operates from a 32.768 kHz crystal with an on-chip PLL generating the required internal operating frequency. The output data rate from the part is software programmable. The p-p resolution from the part varies with the programmed gain and output data rate.

The part operates from a single 3 V or 5 V supply. When operating from 3 V supplies, the power dissipation for the part is 3.75 mW. The AD7709 is housed in a 24-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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Fax: 781/326-8703

AD7709* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7709 Evaluation Board

DOCUMENTATION

Application Notes

- AN-202: An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change
- AN-283: Sigma-Delta ADCs and DACs
- AN-311: How to Reliably Protect CMOS Circuits Against Power Supply Overvoltaging
- AN-388: Using Sigma-Delta Converters-Part 1
- AN-389: Using Sigma-Delta Converters-Part 2
- AN-397: Electrically Induced Damage to Standard Linear Integrated Circuits:
- AN-607: Selecting a Low Bandwidth (<15 kSPS) Sigma-Delta ADC
- AN-608: Input Buffers on Sigma-Delta ADCs
- AN-609: Chopping on Sigma-Delta ADCs
- AN-610: The PGA on Sigma-Delta ADCs
- AN-611: 50 Hz/60Hz Rejection on Sigma-Delta ADCs
- AN-615: Peak-to-Peak Resolution Versus Effective Resolution

Data Sheet

- AD7709: 16-Bit Sigma Delta ADC with Switchable Current Sources Data Sheet

TOOLS AND SIMULATIONS

- Sigma-Delta ADC Tutorial

REFERENCE MATERIALS

Technical Articles

- Delta-Sigma Rocks RF, As ADC Designers Jump On Jitter
- MS-2210: Designing Power Supplies for High Speed ADC
- Part 1: Circuit Suggestions Using Features and Functionality of New Sigma-Delta ADCs
- Part 2: Circuit Suggestions Using Features and Functionality of New Sigma-Delta ADCs

DESIGN RESOURCES

- AD7709 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7709 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

SPECIFICATIONS[1] (V_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, REFIN(+) = 2.5 V; REFIN(–) = GND; GND = 0 V; XTAL1/XTAL2 = 32.768 kHz Crystal; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	AD7709A, AD7709B	Unit	Test Conditions
ADC CHANNEL SPECIFICATION			
Output Update Rate	5.4	Hz min	0.732 ms Increments
	105	Hz max	
ADC CHANNEL			
No Missing Codes[2]	16	Bits min	20 Hz Update Rate
Resolution	13	Bits p-p	±20 mV Range, 20 Hz Update Rate
	16	Bits p-p	±2.56 V Range, 20 Hz Update Rate
Output Noise and Update Rates	See Tables II to V		
Integral Nonlinearity[2]	±30	ppm of FSR max	Typically 2 ppm $FSR = \frac{2 \times 1.024\ REFIN}{GAIN}$
Offset Error	±3	µV typ	
Offset Error Drift vs. Temperature	±10	nV/°C typ	
Full-Scale Error[3]	±0.75	LSB typ	B Grade, V_{DD} = 4 V
	±0.2	% of FS typ	A Grade
Gain Drift vs. Temperature	±0.5	ppm/°C typ	
Power Supply Rejection (PSR)	85	dB typ	Input Range = ±2.56 V 100 dB typ on ±20 mV Range
ANALOG INPUTS			
Differential Input Voltage Ranges	$\frac{\pm 1.024 \times REFIN}{GAIN}$	V nom	REFIN = REFIN(+) – REFIN(–) GAIN = 1 to 128
ADC Range Matching	±2	µV typ	Input Voltage = 19 mV on All Ranges
Absolute AIN1–AIN4 Voltage Limits[2]	GND + 100 mV	V min	
	V_{DD} – 100 mV	V max	
AIN1–AIN4 Analog Input Current			
DC Input Current[2]	±1	nA max	
DC Input Current Drift	±5	pA /°C typ	
Absolute AINCOM Voltage Limits[2]	GND – 30 mV	V min	
	V_{DD} + 30 mV	V max	
AINCOM Analog Input Current			Pseudo-Differential Mode of Operation
DC Input Current	±125	nA/V typ	Input Current Varies with Input Range
DC Input Current Drift	±2	pA/V/°C typ	
Normal-Mode Rejection[2, 4]			
@ 50 Hz	100	dB min	50 Hz ± 1 Hz, 16.65 Hz Update Rate, SF = 82
@ 60 Hz	100	dB min	60 Hz ± 1 Hz, 20 Hz Update Rate, SF = 68
Common-Mode Rejection			
@ DC	100	dB typ	Input Range = ±2.56 V, AIN = 1 V 110 dB typ on ±20 mV Range
@ 50 Hz[2]	100	dB min	50 Hz ± 1 Hz, Range = ±2.56 V, AIN = 1 V
@ 60 Hz[2]	100	dB min	60 Hz ± 1 Hz, Range = ±2.56 V, AIN = 1 V
REFERENCE INPUTS (REFIN1 and REFIN2)			
REFIN Voltage	2.5	V nom	REFIN = REFIN(+) – REFIN(–)
REFIN Voltage Range[2]	1	V min	
	V_{DD}	V max	
Absolute REFIN Voltage Limits[2]	GND – 30 mV	V min	
	V_{DD} + 30 mV	V max	
Average Reference Input Current	0.5	µA/V typ	
Average Reference Input Current Drift	±0.01	nA/V/°C typ	
Normal-Mode Rejection[2, 4]			
@ 50 Hz	100	dB min	50 Hz ± 1 Hz, SF = 82
@ 60 Hz	100	dB min	60 Hz ± 1 Hz, SF = 68
Common-Mode Rejection			
@ DC	110	dB typ	Input Range = ±2.56 V, AIN = 1 V
@ 50 Hz	110	dB typ	50 Hz ± 1 Hz, Range = 2.56 V, AIN = 1 V
@ 60 Hz	110	dB typ	60 Hz ± 1 Hz, Range = 2.56 V, AIN = 1 V

See Notes on page 5.

SPECIFICATIONS (continued)

Parameter	AD7709A, AD7709B	Unit	Test Conditions
EXCITATION CURRENT SOURCES (IEXC1, IEXC2, and IEXC3)			
Output Current			
IEXC1, IEXC2	200	µA nom	
IEXC3	25	µA nom	
Initial Tolerance at 25°C	±10	% typ	
Drift	200	ppm/°C typ	
Initial Current Matching at 25°C	±2.5	% max	B Grade, No Load
(between IEXC1 and IEXC2)	±2.5	% typ	A Grade, No Load
Drift Matching (between IEXC1 and IEXC2)	20	ppm/°C typ	
Initial Current Matching at 25°C (between 8 × IEXC3 and IEXC1/IEXC2)	±5	% max	B Grade, No Load
	±5	% typ	A Grade, No Load
Drift Matching (between 8 × IEXC3 and IEXC1/IEXC2)	20	ppm/°C typ	
Line Regulation			V_{DD} = 5 V ± 5%
IEXC1, IEXC2	1.25	µA/V typ	A, B Grades
	2.6	µA/V max	B Grade
IEXC3	1	µA/V max	B Grade
	1	µA/V typ	A Grade
Load Regulation	300	nA/V typ	
Output Compliance	V_{DD} – 0.6	V max	
	GND –30 mV	V min	
LOW-SIDE POWER SWITCHES (SW1 and SW2)			
R_{ON}	3	Ω typ	V_{DD} = 5 V, A and B Grade
	5	Ω max	B Grade
	4.5	Ω typ	V_{DD} = 3 V, A and B Grade
	7	Ω max	B Grade
Allowable Current[2]	20	mA max	Continuous Current per Switch
LOGIC INPUTS			
All Inputs Except SCLK and XTAL1[2]			
V_{INL}, Input Low Voltage	0.8	V max	V_{DD} = 5 V
	0.4	V max	V_{DD} = 3 V
V_{INH}, Input High Voltage	2.0	V min	V_{DD} = 3 V or 5 V
SCLK Only (Schmitt-Triggered Input)[2]			
$V_{T(+)}$	1.4/2	V min/V max	V_{DD} = 5 V
$V_{T(-)}$	0.8/1.4	V min/V max	V_{DD} = 5 V
$V_{T(+)} - V_{T(-)}$	0.3/0.85	V min/V max	V_{DD} = 5 V
$V_{T(+)}$	0.95/2	V min/V max	V_{DD} = 3 V
$V_{T(-)}$	0.4/1.1	V min/V max	V_{DD} = 3 V
$V_{T(+)} - V_{T(-)}$	0.3/0.85	V min/V max	V_{DD} = 3 V
XTAL1 Only[2]			
V_{INL}, Input Low Voltage	0.8	V max	V_{DD} = 5 V
V_{INH}, Input High Voltage	3.5	V min	V_{DD} = 5 V
V_{INL}, Input Low Voltage	0.4	V max	V_{DD} = 3 V
V_{INH}, Input High Voltage	2.5	V min	V_{DD} = 3 V
Input Currents (except XTAL)	±2	µA max	V_{IN} = V_{DD}
	–70	µA max	V_{IN} = GND, Typically –40 µA @ 5 V and –20 µA at 3 V; Weak Pull-Ups on the Logic Inputs
Input Capacitance	10	pF typ	All Digital Inputs

Parameter	AD7709A, AD7709B	Unit	Test Conditions
LOGIC OUTPUTS (Excluding XTAL2)			
V_{OH}, Output High Voltage[2]	V_{DD} – 0.6	V min	V_{DD} = 3 V, I_{SOURCE} = 100 μA
V_{OL}, Output Low Voltage[2]	0.4	V max	V_{DD} = 3 V, I_{SINK} = 100 μA
V_{OH}, Output High Voltage[2]	4	V min	V_{DD} = 5 V, I_{SOURCE} = 200 μA
V_{OL}, Output Low Voltage[2]	0.4	V max	V_{DD} = 5 V, I_{SINK} = 1.6 mA
Floating-State Leakage Current	±10	μA max	
Floating-State Output Capacitance	±10	pF typ	
Data Output Coding	Binary		Unipolar Mode
	Offset Binary		Bipolar Mode
I/O PORT			
V_{INL}, Input Low Voltage[2]	0.8	V max	V_{DD} = 5 V
	0.4	V max	V_{DD} = 3 V
V_{INH}, Input High Voltage[2]	2.0	V min	V_{DD} = 3 V or 5 V
Input Currents	±2	μA max	V_{IN} = V_{DD}
	–70	μA max	V_{IN} = GND, Typically –40 μA @ V_{DD} = 5 V and –20 μA at V_{DD} = 3 V; Weak Pull-Ups on the Logic Inputs
Input Capacitance	10	pF typ	All Digital Inputs
V_{OH}, Output High Voltage[2]	V_{DD} – 0.6	V min	V_{DD} = 3 V, I_{SOURCE} = 100 μA
V_{OL}, Output Low Voltage[2]	0.4	V max	V_{DD} = 3 V, I_{SINK} = 100 μA
V_{OH}, Output High Voltage[2]	4	V min	V_{DD} = 5 V, I_{SOURCE} = 200 μA
V_{OL}, Output Low Voltage[2]	0.4	V max	V_{DD} = 5 V, I_{SINK} = 1.6 mA
Floating-State Output Leakage Current	±10	μA max	
Floating-State Output Capacitance	±10	pF typ	
START-UP TIME			
From Power-On	300	ms typ	
From Standby Mode	1	ms typ	OSCPD = 0
From Power-Down Mode	300	ms typ	OSCPD = 1
POWER REQUIREMENTS			
Power Supply Voltage			
V_{DD} – GND	2.7/3.6	V min/max	V_{DD} = 3 V nom
	4.75/5.25	V min/max	V_{DD} = 5 V nom
Power Supply Currents			
I_{DD} Current	1.5	mA max	V_{DD} = 3 V, 1.25 mA typ
	1.75	mA max	V_{DD} = 5 V, 1.45 mA typ
I_{DD} (Low Power Mode)	7	μA max	B Grade, V_{DD} = 3 V, Standby Mode
	7	μA typ	A Grade, V_{DD} = 3 V, Standby Mode
	1.5	μA max	B Grade, V_{DD} = 3 V, Power-Down Mode
	1.5	μA typ	A Grade, V_{DD} = 3 V, Power-Down Mode
	26	μA max	B Grade, V_{DD} = 5 V, Standby Mode
	26	μA typ	A Grade, V_{DD} = 5 V, Standby Mode
	6.5	μA max	B Grade, V_{DD} = 5 V, Power-Down Mode
	6.5	μA typ	A Grade, V_{DD} = 5 V, Power-Down Mode
I_{DD} for One Conversion Second	107[5]	μA typ	V_{DD} = 3 V, Standby Mode
	134[5]	μA typ	V_{DD} = 5 V, Standby Mode

NOTES

[1]Temperature Range –40°C to +85°C.

[2]Guaranteed by design and/or characterization data on production release.

[3]Full-scale error applies to both positive and negative full scale.

[4]Simultaneous 50 Hz and 60 Hz rejection is achieved using 19.79 Hz update rate. Normal mode rejection in this case is 60 dB min.

[5]When the part is placed in power-down mode for a single conversion/second, at an update rate of 19.79 Hz, the current consumption is higher compared to when the part is placed in standby mode as the crystal oscillator takes approximately 100 ms to begin clocking. The device will, therefore, use full current for the conversion time and the 100 ms period required for the oscillator to begin clocking. However, if the conversion rate is lower, the current consumption will be reduced so that it is worthwhile to use the power-down rather than the standby mode.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = 2.7 V to 3.6 V or V_{DD} = 4.75 V to 5.25 V; GND = 0 V; X_{TAL} = 32.768 kHz; Input Logic 0 = 0 V, Logic 1 = V_{DD} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} (A, B Version)	Unit	Conditions/Comments
t_1	30.5176	μs typ	Crystal Oscillator Period
t_2	50	ns min	$\overline{\text{RESET}}$ Pulsewidth
Read Operation			
t_3	0	ns min	$\overline{\text{RDY}}$ to $\overline{\text{CS}}$ Setup Time
t_4	0	ns min	$\overline{\text{CS}}$ Falling Edge to SCLK Active Edge Setup Time[3]
t_5[4]	0	ns min	SCLK Active Edge to Data Valid Delay[3]
	60	ns max	V_{DD} = 4.75 V to 5.25 V
	80	ns max	V_{DD} = 2.7 V to 3.6 V
t_{5A}[4, 5]	0	ns min	$\overline{\text{CS}}$ Falling Edge to Data Valid Delay
	60	ns max	V_{DD} = 4.75 V to 5.25 V
	80	ns max	V_{DD} = 2.7 V to 3.6 V
t_6	100	ns min	SCLK High Pulsewidth
t_7	100	ns min	SCLK Low Pulsewidth
t_8	0	ns min	$\overline{\text{CS}}$ Rising Edge to SCLK Inactive Edge Hold Time[3]
t_9[6]	10	ns min	Bus Relinquish Time after SCLK Inactive Edge[3]
	80	ns max	
t_{10}	100	ns max	SCLK Active Edge to $\overline{\text{RDY}}$ High[3, 7]
Write Operation			
t_{11}	0	ns min	$\overline{\text{CS}}$ Falling Edge to SCLK Active Edge Setup Time[3]
t_{12}	30	ns min	Data Valid to SCLK Edge Setup Time
t_{13}	25	ns min	Data Valid to SCLK Edge Hold Time
t_{14}	100	ns min	SCLK High Pulsewidth
t_{15}	100	ns min	SCLK Low Pulsewidth
t_{16}	0	ns min	$\overline{\text{CS}}$ Rising Edge to SCLK Edge Hold Time

NOTES

[1]Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

[2]See Figures 2 and 3.

[3]SCLK active edge is falling edge of SCLK.

[4]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

[5]This specification comes into play only if $\overline{\text{CS}}$ goes low while SCLK is low. It is required primarily for interfacing to DSP machines.

[6]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the Timing Characteristics table are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

[7]$\overline{\text{RDY}}$ returns high after a read of the ADC. The same data can be read again, if required, while $\overline{\text{RDY}}$ is high, although care should be taken that subsequent reads do not occur close to the next output update.

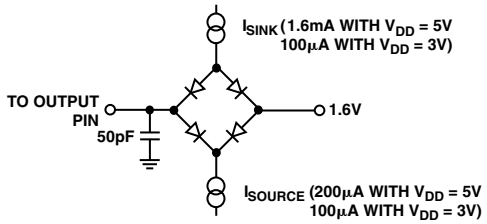


Figure 1. Load Circuit for Timing Characterization

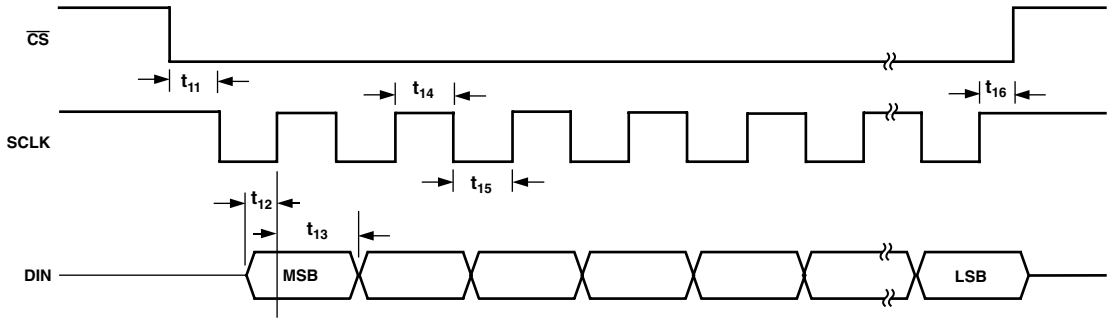


Figure 2. Write Cycle Timing Diagram

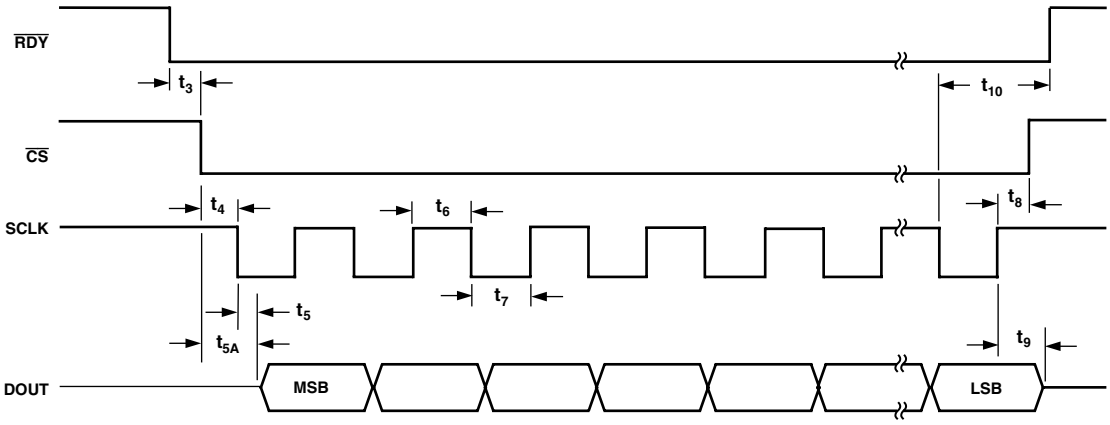


Figure 3. Read Cycle Timing Diagram

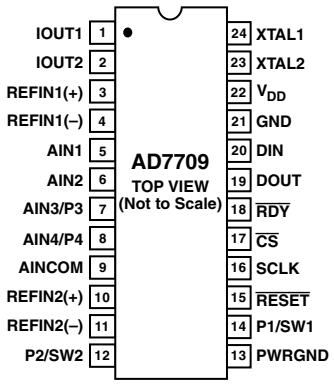
ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND . . . . . –0.3 V to +7 V
PWRGND to AGND . . . . . –20 mV to +20 mV
Analog Input Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND . . . –0.3 V to V_{DD} + 0.3 V
Total AIN/REFIN Current (Indefinite) . . . . . 30 mA
Digital Input Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
θ_{JA} Thermal Impedance . . . . . 97.9°C/W
θ_{JC} Thermal Impedance . . . . . 14°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7709ARU	–40°C to +85°C	TSSOP	RU-24
AD7709BRU	–40°C to +85°C	TSSOP	RU-24
EVAL-AD7709EB		Evaluation Board	

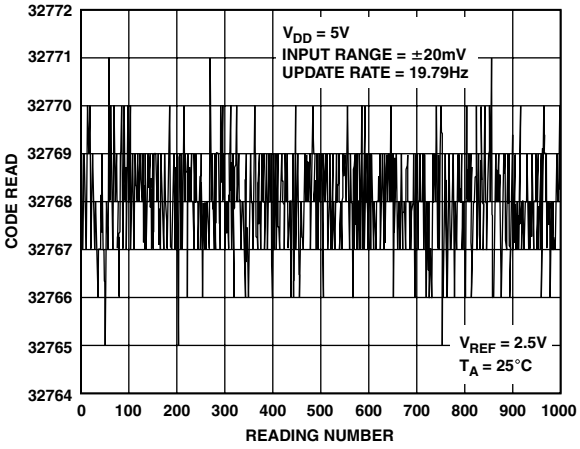
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7709 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

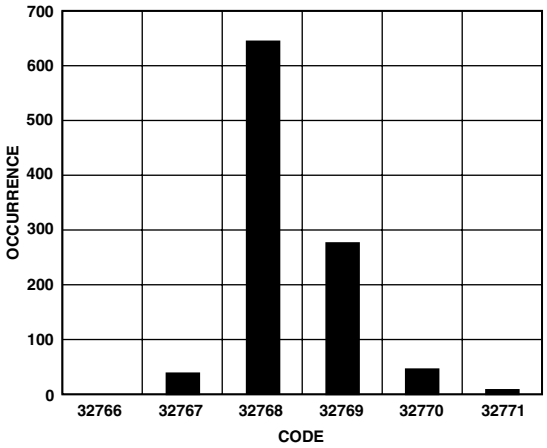
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	IOUT1	Output for Internal Excitation Current Source. Either current source IEXC1, IEXC2, IEXC3, or a combination of the current sources, can be switched to this output.
2	IOUT2	Output for Internal Excitation Current Source. Either current source IEXC1, IEXC2, IEXC3, or a combination of the current sources, can be switched to this output.
3	REFIN1(+)	Positive Reference Input. REFIN1(+) can lie anywhere between V_{DD} and GND + 1 V. The nominal reference voltage (REFIN1(+) – REFIN1(–)) is 2.5 V, but the part is functional with a reference range from 1 V to V_{DD}.
4	REFIN1(–)	Negative Reference Input. This reference input can lie anywhere between GND and V_{DD} – 1 V.
5	AIN1	Analog Input. Programmable gain input that can be used as a pseudo-differential input when used with AINCOM or as the positive input of a fully differential input pair when used with AIN2.
6	AIN2	Analog Input. Programmable gain input that can be used as a pseudo-differential input when used with AINCOM or as the negative input of a fully differential input pair when used with AIN1.
7	AIN3/P3	Analog Input/Digital Port Bit. Programmable gain input that can be used as a pseudo-differential input when used with AINCOM or as the positive input of a fully differential input pair when used with AIN4. This pin can also be programmed as a general-purpose digital input bit.
8	AIN4/P4	Analog Input/Digital Port Bit. Programmable gain input that can be used as a pseudo-differential input when used with AINCOM or as the negative input of a fully-differential input pair when used with AIN3. This pin can also be programmed as a general-purpose digital input bit.
9	AINCOM	All analog inputs are referenced to this input when configured in pseudo-differential input mode.
10	REFIN2(+)	Positive Reference Input. REFIN2(+) can lie anywhere between V_{DD} and GND + 1 V. The nominal reference voltage (REFIN2(+) – REFIN2(–)) is 2.5 V, but the part is functional with a reference range from 1 V to V_{DD}.
11	REFIN2(–)	Negative Reference Input. This reference input can lie anywhere between GND and V_{DD} – 1 V.
12	P2/SW2	Dual-Purpose Pin. It can act as a general-purpose output (P2) bit or as a low-side power switch (SW2) to PWRGND.
13	PWRGND	Ground Point for the Low-Side Power Switches SW2 and SW1. PWRGND must be tied to GND.
14	P1/SW1	Dual-Purpose Pin. It can act as a general-purpose output (P1) bit or as a low-side power switch (SW1) to PWRGND.
15	$\overline{\text{RESET}}$	Digital Input Used to Reset the ADC to Its Power-On-Reset Status. This pin has a weak pull-up internally to V_{DD}.
16	SCLK	Serial Clock Input for Data Transfers to and from the ADC. The SCLK has a Schmitt-triggered input making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the AD7709 in smaller batches of data. A weak pull-up to V_{DD} is provided on the SCLK input.
17	$\overline{\text{CS}}$	Chip Select Input. This is an active low logic input used to select the AD7709. $\overline{\text{CS}}$ can be used to select the AD7709 in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{\text{CS}}$ can be hardwired low allowing the AD7709 to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device. A weak pull-up to V_{DD} is provided on the $\overline{\text{CS}}$ input.
18	$\overline{\text{RDY}}$	$\overline{\text{RDY}}$ is a Logic Low Status Output from the AD7709. $\overline{\text{RDY}}$ is low if the ADC has valid data in its data register. This output returns high on completion of a read operation from the data register. If data is not read, $\overline{\text{RDY}}$ will return high prior to the next update indicating to the user that a read operation should not be initiated.
19	DOUT	Serial Data Output Accessing the Output Shift Register of the AD7709. The output shift register can contain data from any of the on-chip data or control registers.
20	DIN	Serial Data Input Accessing the Input Shift Register on the AD7709. Data in this shift register is transferred to the control registers within the ADC, the selection bits of the communications register selecting which control register. A weak pull-up to V_{DD} is provided on the DIN input.
21	GND	Ground Reference Point for the AD7709
22	V_{DD}	Supply Voltage, 3 V or 5 V Nominal
23	XTAL2	Output from the 32.768 kHz Crystal Oscillator Inverter
24	XTAL1	Input to the 32.768 kHz Crystal Oscillator Inverter

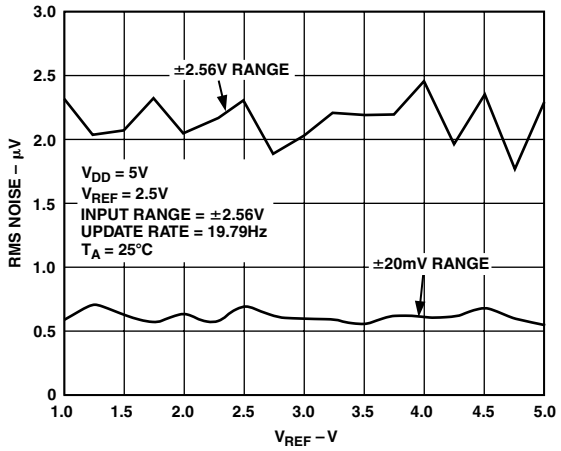
AD7709–Typical Performance Characteristics



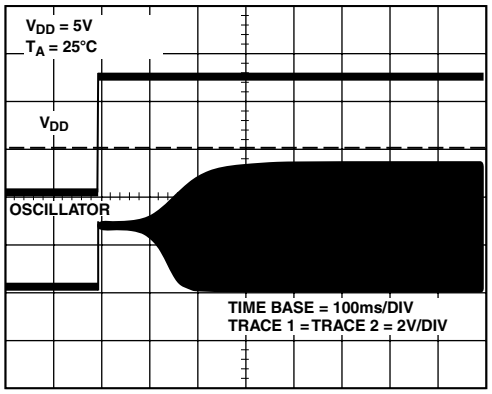
TPC 1. Typical Noise Plot on ±20 mV Input Range



TPC 3. Noise Histogram



TPC 2. RMS Noise vs. Reference Input



TPC 4. Typical Oscillator Power-Up

ADC CIRCUIT INFORMATION

Overview

The AD7709 incorporates a Σ-Δ ADC channel with on-chip digital filtering intended for the measurement of wide dynamic range, low frequency signals such as those in weigh-scale, strain-gauge, pressure transducer, or temperature measurement applications.

Σ-Δ ADC

This channel can be programmed to have one of eight input voltage ranges from ±20 mV to ±2.56 V. This channel can be configured as either two fully differential inputs (AIN1/AIN2 and AIN3/AIN4) or four pseudo-differential input channels (AIN1/AINCOM, AIN2/AINCOM, AIN3/AINCOM, and AIN4/AINCOM). Buffering the input channel means that the part can accommodate significant source impedances on the analog input and that R, C filtering (for noise rejection or RFI reduction) can be placed on the analog inputs if required.

The ADC employs a Σ-Δ conversion technique to realize up to 16 bits of no-missing-codes performance. The Σ-Δ modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A Sinc^3 programmable low-pass filter is then employed to decimate the modulator output data stream to give a valid data conversion result at programmable output rates from 5.35 Hz (186.77 ms) to 105.03 Hz (9.52 ms). A chopping scheme is also employed to minimize ADC channel offset errors. A block diagram of the ADC input channel is shown in Figure 4.

The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (which results from the analog-to-digital conversion) so that the noise is pushed toward one-half of the modulator frequency. The output of the Σ-Δ modulator feeds directly into the digital filter. The digital filter then band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a band-limited, low noise output from the AD7709 ADC. The AD7709 filter is a low-pass, Sinc^3, or (SIN(x)/x)^3 filter whose primary function is to remove the quantization noise introduced at the modulator. The cutoff frequency and decimated output data rate of the filter are programmable via the SF word loaded to the filter register.

A chopping scheme is employed where the complete signal chain is chopped, resulting in excellent dc offset and offset drift specifications, and is extremely beneficial in applications where drift, noise rejection, and optimum EMI rejection are important factors. With chopping, the ADC repeatedly reverses its inputs. The decimated digital output words from the Sinc^3 filters therefore have a positive offset and negative offset term included. As a result, a final summing stage is included so that each output word from the filter is summed and averaged with the previous filter output to produce a new valid output result to be written to the ADC data register.

The input chopping is incorporated into the input multiplexer while the output chopping is accomplished by an XOR gate at the output of the modulator. The chopped modulator bit stream is applied to a Sinc^3 filter. The programming of the Sinc^3 decimation factor is restricted to an 8-bit register SF, the actual decimation factor is the register value × 8. The decimated output rate from the Sinc^3 filter (and the ADC conversion rate) will therefore be:

$$f_{ADC} = \frac{1}{3} \times \left(\frac{1}{8 \times SF} \right) \times f_{MOD}$$

where:

f_{ADC} is the ADC update rate.

SF is the decimal equivalent of the word loaded to the filter register.

f_{MOD} is the modulator sampling rate of 32.768 kHz.

Programming the filter register determines the update rate for the ADC. The chop rate of the channel is half the output data rate.

The frequency response of the filter H(f) is as follows:

$$\left(\frac{1}{SF \times 8} \times \frac{\sin (SF \times 8 \times \pi \times f/f_{MOD})}{\sin (\pi \times f/f_{MOD})} \right)^3 \times \left(\frac{1}{2} \times \frac{\sin (2 \times \pi \times f/f_{OUT})}{\sin (\pi \times f/f_{OUT})} \right)$$

where:

f_{MOD} = 32,768 Hz.

SF = value programmed into Filter Register.

$$f_{OUT} = f_{MOD}/(\text{SF} \times 8 \times 3)$$

The following shows plots of the filter frequency response for the SF words shown in Table I. The overall frequency response is the product of a Sinc^3 and a sinc response. There are Sinc^3 notches at integer multiples of 3 × f_{ADC}, and there are sinc notches at odd integer multiples of f_{ADC}/2. The 3 dB frequency for all values of SF obeys the following equation:

$$f\left(3\ dB\right) = 0.24 \times f_{ADC}$$

The signal chain is chopped as shown in Figure 4. The chop frequency is:

$$f_{CHOP} = \left(\frac{f_{ADC}}{2} \right)$$

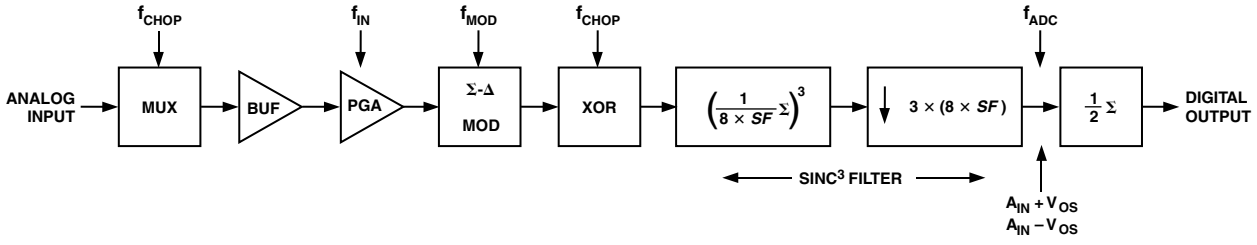


Figure 4. ADC Channel Block Diagram

As shown in the block diagram, the Sinc^3 filter outputs alternately contain $+V_{OS}$ and $-V_{OS}$, where V_{OS} is the respective channel offset. This offset is removed by performing a running average of 2, which means that the settling time to any change in programming of the ADC will be twice the normal conversion time, while an asynchronous step change on the analog input will not be fully reflected until the third subsequent output.

$$t_{SETTLE} = \left(\frac{2}{f_{ADC}} \right) = 2 \times t_{ADC}$$

The allowable range for SF is 13 to 255, with a default of 69 (45H). The corresponding conversion rates, conversion times, and settling times are shown in Table I. Note that the conversion time increases by 0.732 ms for each increment in SF.

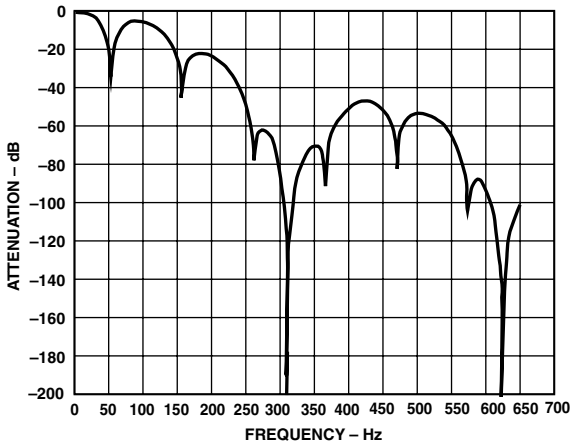


Figure 5. Filter Profile with SF = 13

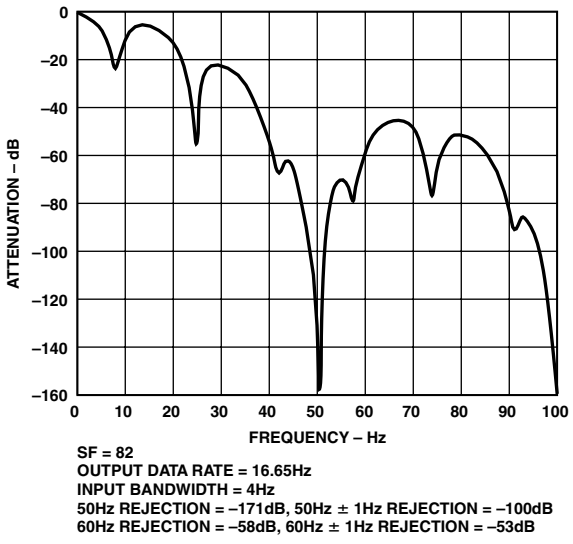


Figure 6. Filter Profile with SF = 82

Table I. ADC Conversion and Settling Times for Various SF Words

SF Word	Data Update Rate f_{ADC} (Hz)	Settling Time t_{SETTLE} (ms)
13	105.3	19.04
69 (Default)	19.79	101.07
255	5.35	373.54

Normal mode rejection is the major function of the digital filter on the AD7709. The normal mode 50 ± 1 Hz rejection with an SF word of 82 is typically –100 dB. The 60 ± 1 Hz rejection with SF = 68 is typically –100 dB. Simultaneous 50 Hz and 60 Hz rejection of better than 60 dB is achieved with an SF of 69. Choosing an SF word of 69 places notches at both 50 Hz and 60 Hz. Figures 5 to 8 show the filter rejection for a selection of SF words.

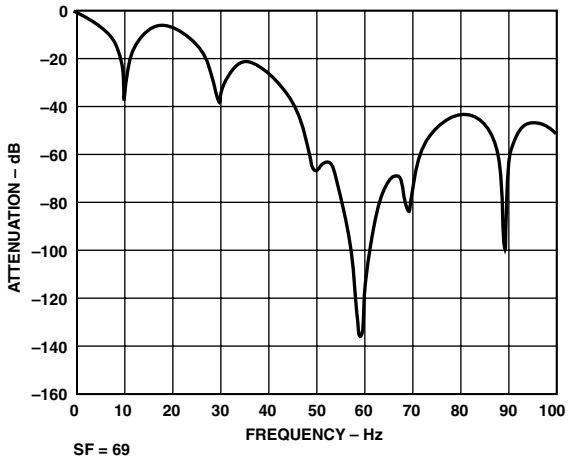


Figure 7. Filter Profile with Default SF = 69 Giving Filter Notches at Both 50 Hz and 60 Hz

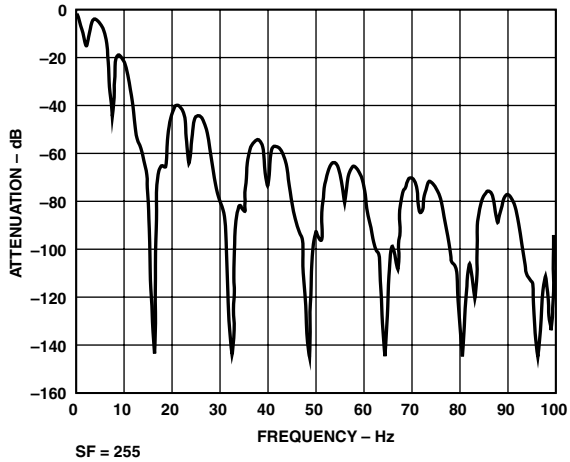


Figure 8. Filter Profile with SF = 255

NOISE PERFORMANCE

Tables II and III show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for a selection of output update rates. The numbers are typical and generated at a differential input voltage of 0 V. The output update rate is selected via the SF7–SF0 bits in the Filter Register. It is important to note that the peak-to-peak resolution figures represent the resolution for which there will be no code flicker within a six-sigma limit. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. Second, when the analog input is converted into the digital domain, quantization noise is added. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. The numbers in the tables are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers will be the same as the bipolar range, but the peak-to-peak resolution is now based on half the signal range, which effectively means losing 1 bit of resolution.

ON-CHIP REGISTERS

The AD7709 is controlled and configured via a number of on-chip registers, as shown in Figure 9 and described in more detail in the following pages. In the following descriptions, *set* implies a Logic 1 state and *cleared* implies a Logic 0 state, unless otherwise stated.

Table II. Typical Output RMS Noise vs. Input Range and Update Rate for the AD7709 (Output RMS Noise in μV)

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	1.50	1.50	1.60	1.75	3.50	4.50	6.70	11.75
69	19.79	0.60	0.65	0.65	0.65	0.65	0.95	1.40	2.30
255	5.35	0.35	0.35	0.37	0.37	0.37	0.51	0.82	1.25

Table III. Peak-to-Peak Resolution vs. Input Range and Update Rate for the AD7709 (Peak-to-Peak Resolution in Bits)

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	12	13	14	15	15	15.5	16	16
69	19.79	13	14	15	16	16	16	16	16
255	5.35	14	15	16	16	16	16	16	16

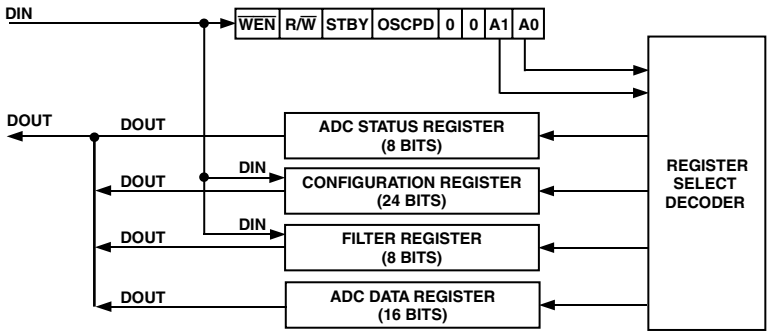


Figure 9. On-Chip Registers

Communications Register (A1, A0 = 0, 0)

The Communications Register is an 8-bit write-only register. All communications to the part must start with a write operation to the Communications Register. The data written to the Communications Register determines whether the next operation is a read or write operation, and to which register this operation takes place. For read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the Communications Register. This is the default state of the interface, and on power-up or after a $\overline{\text{RESET}}$, the AD7709 is in this default state waiting for a write operation to the Communications Register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high, returns the AD7709 to this default state by resetting the part. Table IV outlines the bit designations for the Communications Register. CR0 to CR7 indicate the bit location, CR denoting the bits are in the Communications Register. CR7 denotes the first bit of the data stream.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}$(0)	R/$\overline{\text{W}}$(0)	STBY(0)	OSCPD(0)	0(0)	0(0)	A1(0)	A(0)

Table IV. Communications Register Bit Designations

Bit Location	Bit Name	Description
CR7	$\overline{\text{WEN}}$	Write Enable Bit. A 0 must be written to this bit so the write operation to the Communications Register actually takes place. If a 1 is written to this bit, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a 0 is written to this bit. Once a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits will be loaded to the Communications Register.
CR6	R/$\overline{\text{W}}$	A 0 in this bit location indicates that the next operation will be a write to a specified register. A 1 in this position indicates that the next operation will be a read from the designated register.
CR5	STBY	Standby Bit Location. A 1 in this location places the AD7709 in low power mode. A 0 in this location powers up the AD7709.
CR4	OSCPD	Oscillator Power-Down Bit. If this bit is set, placing the AD7709 in standby mode will stop the crystal oscillator also, reducing the power consumed by the part to a minimum. The oscillator will require 300 ms to begin oscillating when the ADC is taken out of power-down mode. If this bit is cleared, the oscillator is not stopped when the ADC is placed in power-down mode. When the ADC is taken out of power-down mode, the oscillator does not require the 300 ms start-up time.
CR3–CR2	0	These bits must be programmed with a Logic 0 for correct operation.
CR1–CR0	A1–A0	Register Address Bits. These address bits are used to select which of the AD7709 registers are accessed during this serial interface communication.

Table V. Register Selection Table

A1	A0	Register
0	0	Communications Register during a Write Operation
0	0	Status Register during a Read Operation
0	1	Configuration Register
1	0	Filter Register
1	1	ADC Data Register

Status Register (A1, A0 = 0, 0; Power-On-Reset = 00H)
The ADC Status Register is an 8-bit read-only register. To access the ADC Status Register, the user must write to the Communications Register, selecting the next operation to be a read and load bits A1–A0 with 0, 0. Table VI outlines the bit designations for the Status Register. SR0 to SR7 indicate the bit location, SR denoting the bits are in the Status Register. SR7 denotes the first bit of the data stream. The number in brackets indicates the power-on-reset default status of that bit.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
RDY(0)	0(0)	0(0)	0(0)	ERR(0)	0(0)	STBY(0)	LOCK(0)

Table VI. Status Register Bit Designations

Bit Location	Bit Name	Description
SR7	RDY	Ready Bit for ADC. Set when data is written to the ADC data register. The RDY bit is cleared automatically after the ADC data register has been read or a period of time before the data register is updated with a new conversion result.
SR6	0	This bit is automatically cleared.
SR5	0	This bit is automatically cleared.
SR4	0	This bit is automatically cleared.
SR3	ERR	ADC Error Bit. This bit is set at the same time as the RDY bit. Set to indicate that the result written to the ADC data register has been clamped to all zeros or all ones. Error sources include Overrange, Underrange. Cleared by a write to the mode bits to initiate a conversion.
SR2	0	This bit is automatically cleared.
SR1	STBY	Standby Bit Indication. When this bit is set, the AD7709 is in power-down mode. This bit is cleared when the ADC is powered up.
SR0	LOCK	PLL Lock Status Bit. Set if the PLL has locked onto the 32.768 kHz crystal oscillator clock. If the user is worried about exact sampling frequencies, etc., the LOCK bit should be interrogated and the result discarded if the LOCK bit is 0.

Configuration Register (A1, A0 = 0, 1; Power-On-Reset = 000007H)

The Configuration Register is a 24-bit register from which data can either be read or to which data can be written. This register is used to select the input channel and configure the input range, excitation current sources, and I/O port. Table VII outlines the bit designations for this register. CONFIG23 to CONFIG0 indicate the bit location, CONFIG denoting the bits are in the Configuration Register. CONFIG23 denotes the first bit of the data stream. The number in brackets indicates the power-on-reset default status of that bit. A write to the Configuration Register has immediate effect and does not reset the ADC. Therefore, if a current source is switched while the ADC is converting, the user will have to wait for the full settling time of the sinc^3 filter before obtaining a fully settled output. This equates to three outputs.

CONFIG23	CONFIG22	CONFIG21	CONFIG20	CONFIG19	CONFIG18	CONFIG17	CONFIG16
PSW2(0)	PSW1(0)	I3EN1(0)	I3EN0(0)	I2EN1(0)	I2EN0(0)	I1EN1(0)	I1EN0(0)

CONFIG15	CONFIG14	CONFIG13	CONFIG12	CONFIG11	CONFIG10	CONFIG9	CONFIG8
P4DIG(0)	P3DIG(0)	P2EN(0)	P1EN(0)	P4DAT(0)	P3DAT(0)	P2DAT(0)	P1DAT(0)

CONFIG7	CONFIG6	CONFIG5	CONFIG4	CONFIG3	CONFIG2	CONFIG1	CONFIG0
REFSEL(0)	CH2(0)	CH1(0)	CH0(0)	UNI(0)	RN2(1)	RN1(1)	RN0(1)

Table VII. Configuration Register Bit Designations

Bit Location	Bit Name	Description
CONFIG23	PSW2	Power Switch 2 Control Bit. Set by user to enable power switch SW2/P2 to PWRGND. Cleared by user to enable use as a standard I/O pin. When the ADC is in standby mode, the power switches are open.
CONFIG22	PSW1	Power Switch 1 Control Bit. Set by user to enable power switch SW1/P1 to PWRGND. Cleared by user to enable use as a standard I/O pin. When the ADC is in standby mode, the power switches are open.
CONFIG21	I3EN1	IEXC3 Current Source Enable Bit
CONFIG20	I3EN0	IEXC3 Current Source Enable Bit

I3EN1	I3EN0	Function
0	0	IEXC3 Current Source OFF
0	1	IEXC3 Current Source Routed to the IOUT1 Pin
1	0	IEXC3 Current Source Routed to the IOUT2 Pin
1	1	Reserved

CONFIG19	I2EN1	IEXC2 Current Source Enable Bit
CONFIG18	I2EN0	IEXC2 Current Source Enable Bit

I2EN1	I2EN0	Function
0	0	IEXC2 Current Source OFF
0	1	IEXC2 Current Source Routed to the IOUT1 Pin
1	0	IEXC2 Current Source Routed to the IOUT2 Pin
1	1	Reserved

CONFIG17	I1EN1	IEXC1 Current Source Enable Bit

Table VII. Configuration Register Bit Designations (continued)

<table>
<tr><th>Bit Location</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>CONFIG16</td><td>I1EN0</td><td>IEXC1 Current Source Enable Bit
<table>
<tr><th>I1EN1</th><th>I1EN0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>IEXC1 Current Source OFF</td></tr>
<tr><td>0</td><td>1</td><td>IEXC1 Current Source Routed to the IOUT1 Pin</td></tr>
<tr><td>1</td><td>0</td><td>IEXC1 Current Source Routed to the IOUT2 Pin</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>CONFIG15</td><td>P4DIG</td><td>Digital Input Enable.
Set by user to enable pin AIN4/P4 as a digital input. A weak pull-up resistor is activated in this state.
Cleared by user to configure pin AIN4/P4 as an analog input.</td></tr>
<tr><td>CONFIG14</td><td>P3DIG</td><td>Digital Input Enable.
Set by user to enable pin AIN3/P3 as a digital input. A weak pull-up resistor is activated in this state.
Cleared by user to configure pin AIN3/P3 as an analog input.</td></tr>
<tr><td>CONFIG13</td><td>P2EN</td><td>SW2/P2 Digital Output Enable Bit.
Set by user to enable P2 as a regular digital output pin.
Cleared by user to three-state the P2 output. PSW2 takes precedence over P2EN.</td></tr>
<tr><td>CONFIG12</td><td>P1EN</td><td>SW1/P1 Digital Output Enable Bit.
Set by user to enable P1 as a regular digital output pin.
Cleared by user to three-state the P1 output. PSW1 takes precedence over P1EN.</td></tr>
<tr><td>CONFIG11</td><td>P4DAT</td><td>Digital Input Port Data Bit.
P4DAT is read only and will return a zero if P4DIG equals zero.
If P4 is enabled as a digital input, the readback value indicates the status of pin P4.</td></tr>
<tr><td>CONFIG10</td><td>P3DAT</td><td>Digital Input Port Data Bit.
P3DAT is read only and will return a zero if P3DIG equals zero.
If P3 is enabled as a digital input, the readback value indicates the status of pin P3.</td></tr>
<tr><td>CONFIG9</td><td>P2DAT</td><td>Digital Output Port Data Bit. P2 is a digital output only. When the port is active as an output (P2EN = 1), the value written to this data bit appears at the output port. Reading P2DAT will return the last value written to the P2DAT bit.</td></tr>
<tr><td>CONFIG8</td><td>P1DAT</td><td>Digital Output Port Data Bit. P1 is a digital output only. When the port is active as an output (P1EN = 1), the value written to this data bit appears at the output port. Reading P1DAT will return the last value written to the P1DAT bit.</td></tr>
<tr><td>CONFIG7</td><td>REFSEL</td><td>ADC Reference Input Select.
Cleared by the user to select REFIN1(+) and REFIN1(–) as the ADC reference.
Set by the user to select REFIN2(+) and REFIN2(–) as the ADC reference.</td></tr>
<tr><td>CONFIG6</td><td>CH2</td><td rowspan="3">ADC Input Channel Selection Bit. It is used in conjunction with CH1 and CH0 as shown below.
ADC Input Channel Selection Bit. It is used in conjunction with CH2 and CH0 as shown below.
ADC Input Channel Selection Bit. It is used in conjunction with CH2 and CH1 as shown below.
<table>
<tr><th>CH2</th><th>CH1</th><th>CH0</th><th>Positive Input</th><th>Negative Input</th><th>Buffer</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>AIN1</td><td>AINCOM</td><td>Positive Analog Input</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>AIN2</td><td>AINCOM</td><td>Positive Analog Input</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>AIN3</td><td>AINCOM</td><td>Positive Analog Input</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>AIN4</td><td>AINCOM</td><td>Positive Analog Input</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>AIN1</td><td>AIN2</td><td>Positive and Negative Analog Inputs</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>AIN3</td><td>AIN4</td><td>Positive and Negative Analog Inputs</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>AINCOM</td><td>AINCOM</td><td>None</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>AIN2</td><td>AIN2</td><td>Positive and Negative Analog Inputs</td></tr>
</table>
The Buffer column indicates if the analog inputs are buffered or unbuffered. This determines the common-mode input range on each input. If the input is unbuffered (AINCOM), the common-mode input includes ground.</td></tr>
<tr><td>CONFIG5</td><td>CH1</td></tr>
<tr><td>CONFIG4</td><td>CH0</td></tr>
</table>

Table VII. Configuration Register Bit Designations (continued)

Bit Location	Bit Name	Description
CONFIG3	UNI	Unipolar/Bipolar Operation Selection Bit. Set by the user to enable unipolar operation. In this mode, the device uses straight binary output coding i.e., 0 differential input will generate a result of 0000h and a full-scale differential input will generate a code of FFFFh. Cleared by the user to enable pseudo-bipolar operation. The device uses offset binary coding, i.e., a negative full-scale differential input will result in a code of 0000h, a 0 differential input will generate a code of 8000h, while a positive full-scale differential input will result in a code of FFFFh.
CONFIG2	RN2	This bit is used in conjunction with RN1 and RN0 to select the analog input range as shown below.
CONFIG1	RN1	This bit is used in conjunction with RN2 and RN0 to select the analog input range as shown below.
CONFIG0	RN0	This bit is used in conjunction with RN2 and RN1 to select the analog input range as shown below.

RN2	RN1	RN0	Selected ADC Input Range (V_{REF} = 2.5 V)
0	0	0	±20 mV
0	0	1	±40 mV
0	1	0	±80 mV
0	1	1	±160 mV
1	0	0	±320 mV
1	0	1	±640 mV
1	1	0	±1.28 V
1	1	1	±2.56 V

Table VIII. Filter Register Bit Designations

FR7	FR6	FR5	FR4	FR3	FR2	FR1	FR0
SF7(0)	SF6(1)	SF5(0)	SF4(0)	SF3(0)	SF2(1)	SF1(0)	SF0(1)

Table IX. Update Rate vs. SF WORD

SF (Dec)	SF (Hex)	f_{ADC} (Hz)	t_{ADC} (ms)
13	0D	105.3	9.52
69	45	19.79	50.34
255	FF	5.35	186.77

Filter Register (A1, A0 = 1, 0; Power-On-Reset = 45h)
The Filter Register is an 8-bit register from which data can be read or to which data can be written. This register determines the amount of averaging performed by the sinc filter. Table VIII outlines the bit designations for the Filter Register. FR7 through FR0 indicate the bit location, FR denoting the bits are in the Filter Register. FR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit. The number in this register is used to set the decimation factor and thus the output update rate for the ADC. The Filter Register cannot be written to by the user while the ADC is active. The update rate is calculated as follows:

$$f_{ADC} = \frac{1}{3} \times \frac{1}{8 \times SF} \times f_{MOD}$$

where:

f_{ADC} is the ADC output update rate.
f_{MOD} is the Modulator Clock Frequency = 32.768 kHz.
SF is the decimal value written to the SF Register.

The allowable range for SF is 13dec to 255dec. Examples of SF values and corresponding conversion rate (f_{ADC}) and time (t_{ADC}) are shown in Table IX. It should also be noted that the ADC input channel is chopped to minimize offset errors. This means that the time for a single conversion or the time to the first conversion result is $2 \times t_{ADC}$.

ADC Data Result Register (A1, A0 = 1, 1; Power-On-Reset = 0000h)
The conversion result is stored in the ADC Data Register (DATA). This register is 16-bits wide. This is a read-only register. On completion of a read from this register, the RDY bit in the Status Register is cleared.

CONFIGURING THE AD7709

The four user-accessible registers on the AD7709 are accessed via the serial interface. Communication with any of these registers is initiated by first writing to the Communications Register. The AD7709 begins converting on power-up without the need to write to the registers. The default conditions are used, i.e., the AD7709 operates at a 19.79 Hz update rate that offers 50 Hz and 60 Hz rejection.

Figure 10 outlines a flow diagram of the sequence used to configure all registers after a power-up or reset on the AD7709. The flowchart shows two methods of determining when it is valid to read the data register. The first method is hardware polling of the $\overline{RDY}$ pin and the second method involves software interrogation of the RDY bit in the status register. The flowchart details all the necessary programming steps required to initialize the ADC and read data from the ADC channel following a power-on or reset. The steps can be broken down as follows:

1. Configure and initialize the microcontroller or microprocessor serial port.
2. Initialize the AD7709 by configuring the following registers:
   a) Filter Register to configure the update rate for the channel. The AD7709 must be placed in standby mode before the Filter Register can be written to.
   b) Configuration Register to select the input channel to be converted, its input range, and reference. This register is also used to configure internal current sources, power switches, and I/O port.

   Both of these operations consist of a write to the Communications Register to specify the next operation as a write to a specified register. Data is then written to this register. When each sequence is complete, the ADC defaults to waiting for another write to the Communications Register to specify the next operation.
3. When configuration is complete, the user needs to determine when it is valid to read the data from the data register. This is accomplished either by polling the $\overline{RDY}$ pin (hardware polling) or by interrogating the RDY bit in the STATUS register (software polling). Both are shown in Figure 10.

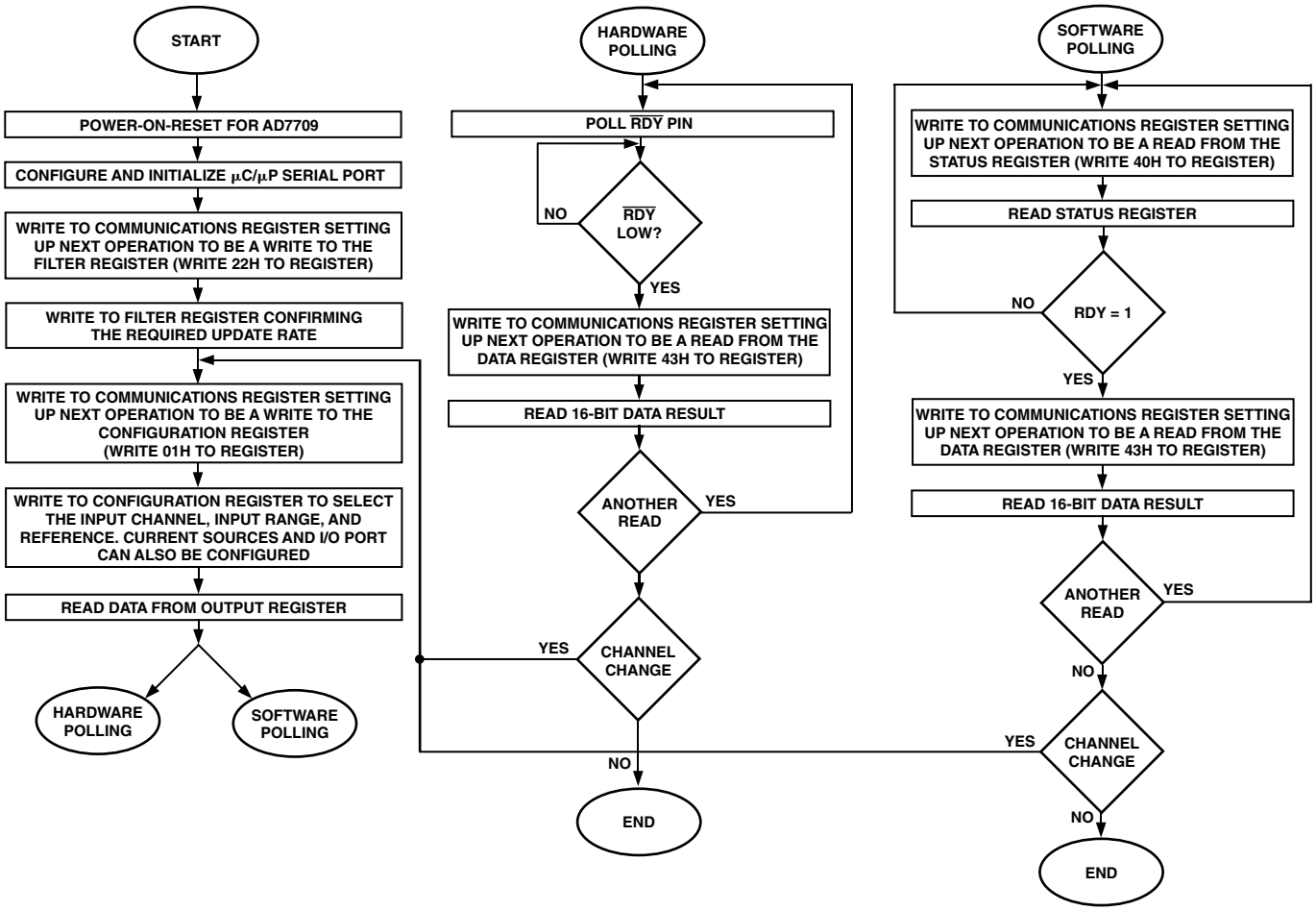


Figure 10. Flowchart for Initializing and Reading Data from the AD7709

DIGITAL INTERFACE

As previously outlined, AD7709 programmable functions are controlled using a set of on-chip registers. Data is written to these registers via the part's serial interface and read access to the on-chip registers is also provided by this interface. All communications to the part must start with a write operation to the Communications Register. After power-on or reset, the device expects a write to its Communications Register. The data written to this register determines whether the next operation to the part is a read or a write operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part starts with a write operation to the Communications Register followed by a write to the selected register. A read operation from any other register on the part (including the output data register) starts with a write operation to the Communications Register followed by a read operation from the selected register.

The AD7709 serial interface consists of five signals: $\overline{CS}$, SCLK, DIN, DOUT, and RDY. The DIN line is used for transferring data into the on-chip registers, while the DOUT line is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device, and all data transfers (either on DIN or DOUT) take place with respect to this SCLK signal. The RDY line is used as a status signal to indicate when data is ready to be read from the AD7709 data register. RDY goes low when a new data-word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the output register to indicate when *not* to read from the device to ensure that a data read is not attempted while the register is being updated. $\overline{CS}$ is used to select the device. It can be used to decode the AD7709 in systems where a number of parts are connected to the serial bus.

Figures 2 and 3 show timing diagrams for interfacing to the AD7709 with $\overline{CS}$ used to decode the part. Figure 3 is for a read operation from the AD7709 output shift register while Figure 2 shows a write operation to the input shift register. It is possible to read the same data twice from the output register even though the RDY line returns high after the first read operation. Care must be taken, however, to ensure that the read operations have been completed before the next output update is about to take place.

The AD7709 serial interface can operate in 3-wire mode by tying the $\overline{CS}$ input low. In this case, the SCLK, DIN, and DOUT lines are used to communicate with the AD7709, and the status of the RDY bit can be obtained by interrogating the Status Register. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port bit. For microcontroller interfaces, it is recommended that the SCLK idles high between data transfers.

The AD7709 can also be operated with $\overline{CS}$ used as a frame synchronization signal. This scheme is suitable for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{CS}$ since $\overline{CS}$ would normally occur after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers provided the timing numbers are obeyed.

The serial interface can be reset by exercising the $\overline{RESET}$ input on the part. It can also be reset by writing a series of 1s on the DIN input. If a Logic 1 is written to the AD7709 DIN line for at least 32 serial clock cycles, the serial interface is reset. This ensures that in 3-wire systems, if the interface gets lost either via a software error or by some glitch in the system, it can be reset back to a known state. This state returns the interface to where the AD7709 is expecting a write operation to its Communications Register. This operation resets the contents of all registers to their power-on reset values.

Some microprocessor or microcontroller serial interfaces have a single serial data line. In this case, it is possible to connect the AD7709 DOUT and DIN lines together and connect them to the single data line of the processor. A 10 kΩ pull-up resistor should be used on this single data line. In this case, if the interface gets lost, because the read and write operations share the same line, the procedure to reset it back to a known state is somewhat different than previously described. It requires a read operation of 24 serial clocks followed by a write operation where a Logic 1 is written for at least 32 serial clock cycles to ensure that the serial interface is back into a known state.

MICROCOMPUTER/MICROPROCESSOR INTERFACING

The AD7709 flexible serial interface allows for easy interface to most microcomputers and microprocessors. The flowchart of Figure 10 outlines the sequence that should be followed when interfacing a microcontroller or microprocessor to the AD7709. Figures 11, 12, and 13 show some typical interface circuits. The serial interface on the AD7709 is capable of operating from just three wires and is compatible with SPI interface protocols. The 3-wire operation makes the part ideal for isolated systems where minimizing the number of interface lines minimizes the number of opto-isolators required in the system. The serial clock input is a Schmitt-triggered input to accommodate slow edges from opto-couplers. The rise and fall times of other digital inputs to the AD7709 should be no longer than 1 μs.

Some of the registers on the AD7709 are 8-bit registers, which facilitates easy interfacing to the 8-bit serial ports of microcontrollers. The Data Register on the AD7709 is 16 bits and the Configuration Register is 24 bits, but data transfers to these registers can consist of multiple 8-bit transfers to the serial port of the microcontroller. DSP processors and microprocessors generally transfer 16 bits of data in a serial data operation. Some of these processors, such as the ADSP-2105, have the facility to program the amount of cycles in a serial transfer. This allows the user to tailor the number of bits in any transfer to match the register length of the required register in the AD7709.

Even though some of the registers on the AD7709 are only 8 bits in length, communicating with two of these registers in successive write operations can be handled as a single 16-bit data transfer if required. For example, if the Filter Register is to be updated, the processor must first write to the Communications Register (saying that the next operation is a write to the Filter Register), and then write 8 bits to the Filter Register. If required, this can all be done in a single 16-bit transfer because once the eight serial clocks of the write operation to the Communications Register have been completed, the part immediately sets itself up for a write operation to the Filter Register.

AD7709-to-68HC11 Interface

Figure 11 shows an interface between the AD7709 and the 68HC11 microcontroller. The diagram shows the minimum (3-wire) interface with $\overline{CS}$ on the AD7709 hardwired low. In this scheme, the RDY bit of the Status Register is monitored to determine when the Data Register is updated. An alternative scheme, which increases the number of interface lines to four, is to monitor the $\overline{RDY}$ output line from the AD7709. The monitoring of the $\overline{RDY}$ line can be done in two ways. First, $\overline{RDY}$ can be connected to one of the 68HC11 port bits (such as PC0), which is configured as an input. This port bit is then polled to determine the status of $\overline{RDY}$. The second scheme is to use an interrupt driven system, in which case the $\overline{RDY}$ output is connected to the IRQ input of the 68HC11. For interfaces that require control of the $\overline{CS}$ input on the AD7709, one of the port bits of the 68HC11 (such as PC1), which is configured as an output, can be used to drive the $\overline{CS}$ input.

The 68HC11 is configured in the master mode with its CPOL bit set to a Logic 1 and its CPHA bit set to a Logic 1. When the 68HC11 is configured like this, its SCLK line idles high between data transfers. The AD7709 is not capable of full-duplex operation. If the AD7709 is configured for a write operation, no data appears on the DOUT lines even when the SCLK input is active. Similarly, if the AD7709 is configured for a read operation, data presented to the part on the DIN line is ignored even when SCLK is active.

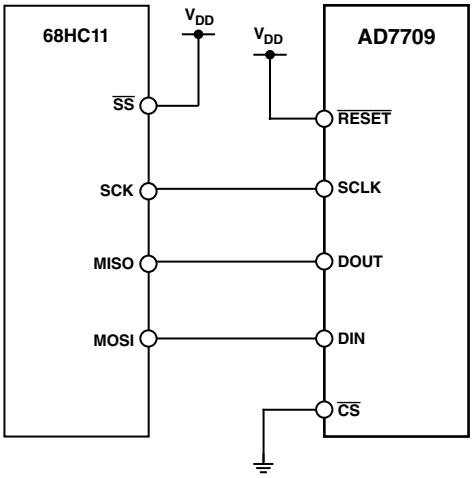


Figure 11. AD7709-to-68HC11 Interface

AD7709-to-8051 Interface

An interface circuit between the AD7709 and the 8XC51 microcontroller is shown in Figure 12. The diagram shows the minimum number of interface connections with $\overline{CS}$ on the AD7709 hardwired low. In the case of the 8XC51 interface, the minimum number of interconnects is just two. In this scheme, the RDY bit of the Status Register is monitored to determine when the Data Register is updated. The alternative scheme, which increases the number of interface lines to three, is to monitor the $\overline{RDY}$ output line from the AD7709. The monitoring of the $\overline{RDY}$ line can be done in two ways. First, $\overline{RDY}$ can be connected to one of the 8XC51 port bits (such as P1.0) which is configured as an input. This port bit is then polled to determine the status of $\overline{RDY}$.

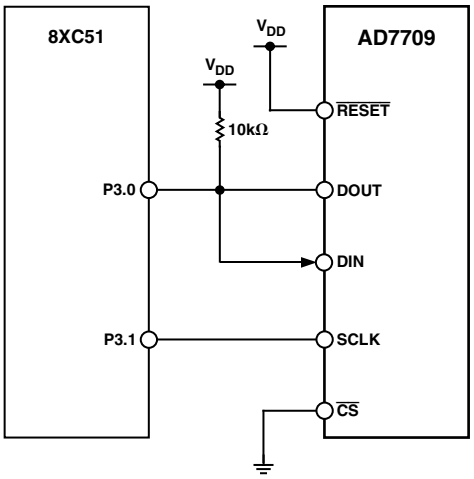


Figure 12. AD7709-to-8XC51 Interface

The second scheme is to use an interrupt-driven system, in which case the $\overline{RDY}$ output is connected to the INT1 input of the 8XC51. For interfaces that require control of the $\overline{CS}$ input on the AD7709, one of the port bits of the 8XC51 (such as P1.1), which is configured as an output, can be used to drive the $\overline{CS}$ input. The 8XC51 is configured in its Mode 0 serial interface mode. Its serial interface contains a single data line. As a result, the DOUT and DIN pins of the AD7709 should be connected together with a 10 kΩ pull-up resistor. The serial clock on the 8XC51 idles high between data transfers. The 8XC51 outputs the LSB first in a write operation, while the AD7709 expects the MSB first so the data to be transmitted has to be rearranged before being written to the output serial register. Similarly, the AD7709 outputs the MSB first during a read operation while the 8XC51 expects the LSB first. Therefore, the data read into the serial buffer needs to be rearranged before the correct data word from the AD7709 is available in the accumulator.

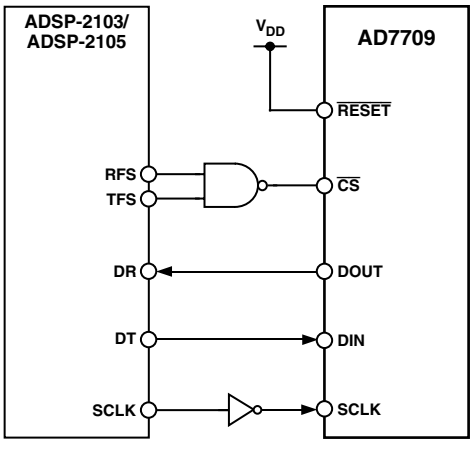


Figure 13. AD7709-to-ADSP-2103/ADSP-2105 Interface

AD7709-to-ADSP-2103/ADSP-2105 Interface

Figure 13 shows an interface between the AD7709 and the ADSP-2103/ADSP-2105 DSP processor. In the interface shown, the RDY bit of the Status Register is again monitored to determine when the Data Register is updated. The alternative scheme is to use an interrupt-driven system, in which case the

$\overline{RDY}$ output is connected to the IRQ2 input of the ADSP-2103/ADSP-2105. The serial interface of the ADSP-2103/ADSP-2105 is set up for alternate framing mode. The RFS and TFS pins of the ADSP-2103/ADSP-2105 are configured as active low outputs and the ADSP-2103/ADSP-2105 serial clock line, SCLK, is also configured as an output. The $\overline{CS}$ for the AD7709 is active when either the RFS or TFS outputs from the ADSP-2103/ADSP-2105 are active. The serial clock rate on the ADSP-2103/ADSP-2105 should be limited to 3 MHz to ensure correct operation with the AD7709.

CIRCUIT DESCRIPTION

The AD7709 is a Σ-Δ A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in weigh scale, pressure, temperature, industrial control, or process control applications. It employs a Σ-Δ conversion technique to realize up to 16 bits of no-missing-codes performance. The Σ-Δ modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A $Sinc^3$ programmable low-pass filter is then employed to decimate the modulator output data stream to give a valid data conversion result at programmable output rates from 5.35 Hz (186.77 ms) to 105.03 Hz (9.52 ms). A chopping scheme is also employed to minimize ADC offset and offset and gain drift errors. The channel is buffered and can be programmed for one of eight input ranges from ±20 mV to ±2.56 V. The input channels can be configured for either fully differential inputs or pseudo-differential input channels via the CH2, CH1, and CH0 bits in the Configuration Register. Buffering the input channel allows the part to handle significant source impedances on the analog input, allowing R/C filtering (for noise rejection or RFI reduction) to be placed on the analog inputs if required. These input channels are intended for converting signals directly from sensors without the need for external signal conditioning. Other functions contained on-chip that augment the operation of the ADC include software configurable current sources, switchable reference inputs, and low-side power switches.

The basic connection diagram for the AD7709 is shown in Figure 14. An AD780/REF195, precision 2.5 V reference, provides the reference source for the part. A quartz crystal or ceramic resonator provides the 32.768 kHz master clock source for the part. In some cases, it will be necessary to connect capacitors on the crystal or resonator to ensure that it does not oscillate at overtones of its fundamental operating frequency. The values of capacitors will vary depending on manufacturer specifications.

Analog Input Channels

The main ADC has five associated analog input pins (labeled AIN1 to AIN4 and AINCOM) that can be configured as two fully differential input channels (AIN1–AIN2 and AIN3–AIN4) or four pseudo-differential input channels (AIN1–AINCOM, AIN2–AINCOM, AIN3–AINCOM, and AIN4–AINCOM). Channel selection bits CH2, CHI, and CH0 in the Configuration Register detail the different configurations. When the analog input channel is switched, the settling time of the part must elapse before a new valid word is available from the ADC.

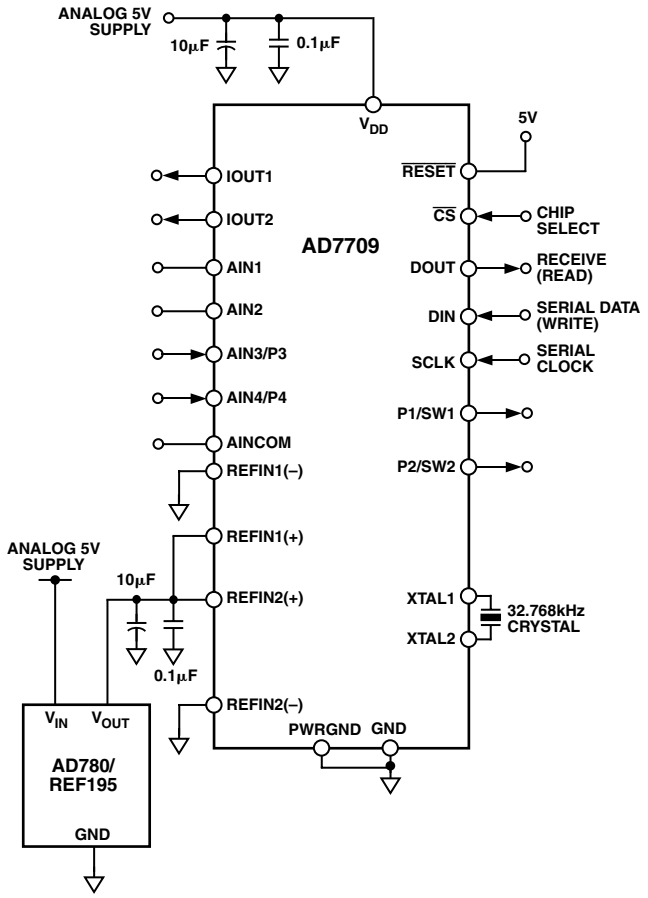


Figure 14. Basic Connection Diagram

The output of the ADC multiplexer feeds into a high impedance input stage of the buffer amplifier. As a result, the ADC inputs can handle significant source impedances and are tailored for direct connection to external resistive-type sensors like strain gauges or Resistance Temperature Detectors (RTDs).

The absolute input voltage range on the ADC inputs when buffered (AIN1 to AIN4) is restricted to a range between GND + 100 mV and V_{DD} – 100 mV. Care must be taken in setting up the common-mode voltage and input voltage range so that these limits are not exceeded; otherwise, there will be a degradation in linearity and noise performance.

The absolute input voltage range on the ADC inputs when unbuffered (AINCOM) includes the range between GND – 30 mV to V_{DD} + 30 mV as a result of being unbuffered. The negative absolute input voltage limit does allow the possibility of monitoring small true bipolar signals with respect to GND.

Programmable Gain Amplifier

The output from the buffer on the ADC is applied to the input of the on-chip programmable gain amplifier (PGA). The PGA can be programmed through eight different unipolar and bipolar ranges. The PGA gain range is programmed via the range bits in the Configuration Register. With an external 2.5 V reference applied, the unipolar ranges are 0 mV to 20 mV, 0 mV to 40 mV, 0 mV to 80 mV, 0 mV to 160 mV, 0 mV to 320 mV, 0 mV to 640 mV, 0 V to 1.28 V, and 0 to 2.56 V, while bipolar ranges are ±20 mV, ±40 mV, ±80 mV, ±160 mV, ±320 mV, ±640 mV, ±1.28 V, and ±2.56 V. These are the ranges that should appear at the input to the on-chip PGA.

Typical matching across ranges is shown in Figure 15. Here, the ADC is configured in fully differential, bipolar mode with an external 2.5 V reference, while an analog input voltage of just greater than 19 mV is forced on its analog inputs. The ADC continuously converts the dc voltage at an update rate of 5.35 Hz, i.e., SF = FFh. A total of 800 conversion results are gathered. The first 100 results gathered with the ADC operating in the ±20 mV. The ADC range is then switched to ±40 mV and 100 more results are gathered, and so on, until the last 100 samples are gathered with the ADC configured in the ±2.5 V range. From Figure 15, the variation in the sample mean through each range, i.e., the range matching, is seen to be on the order of 2 μV.

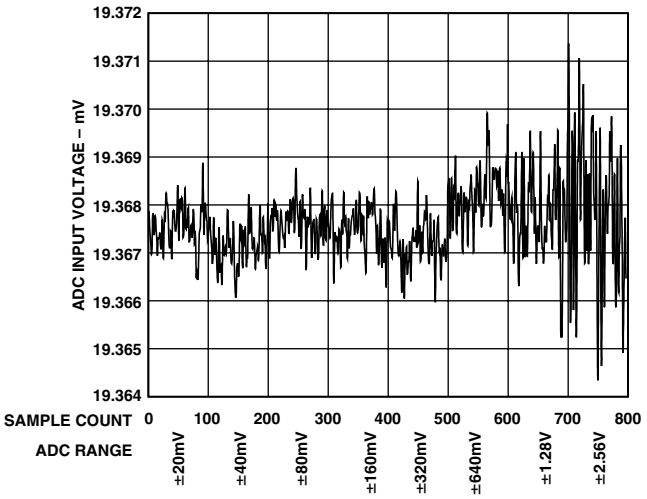


Figure 15. ADC Range Matching

Bipolar/Unipolar Configuration

The analog inputs on the AD7709 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that the part can handle negative voltages with respect to system GND. Unipolar and bipolar signals on the AIN(+) input on the ADC are referenced to the voltage on the respective AIN(–) input. AIN(+) and AIN(–) refer to the signals seen by the modulator that come from the output of the multiplexer, as shown in Figures 16 and 17.

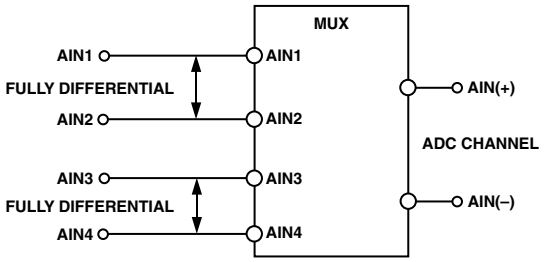


Figure 16. Fully Differential Mode of Operation

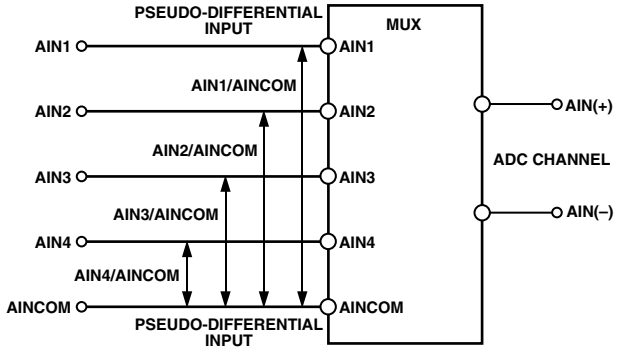


Figure 17. Pseudo-Differential Mode of Operation

For example, if AIN(–) is 2.5 V and the ADC is configured for an analog input range of 0 mV to 20 mV, the input voltage range on the AIN(+) input is 2.5 V to 2.52 V. If AIN(–) is 2.5 V and the AD7709 is configured for an analog input range of ±1.28 V, the analog input range on the AIN(+) input is 1.22 V to 3.78 V (i.e., 2.5 V ±1.28 V). Bipolar or unipolar options are chosen by programming the UNI bit in the Configuration Register. This programs the ADC for either unipolar or bipolar operation. Programming for either unipolar or bipolar operation does not change any of the input signal conditioning; it simply changes the data output coding.

Data Output Coding

When the ADC is configured for unipolar operation, the output coding is natural (straight) binary with a zero differential input voltage resulting in a code of 000 . . . 000, a midscale voltage resulting in a code of 100 . . . 000, and a full-scale input voltage resulting in a code of 111 . . . 111. The output code for any analog input voltage on the ADC can be represented as follows:

$$Code = \frac{\left(AIN \times GAIN \times 2^{N}\right)}{\left(1.024 \times V_{REF}\right)}$$

where:

AIN is the analog input voltage.

GAIN is the PGA gain, i.e., 1 on the 2.56 V range and 128 on the 20 mV range.

N = 16.

When the ADC is configured for bipolar operation, the coding is offset binary with a negative full-scale voltage resulting in a code of 000 . . . 000, a zero differential voltage resulting in a code of 100 . . . 000, and a positive full-scale voltage resulting in a code of 111 . . . 111. The output code from the ADC for any analog input voltage can be represented as follows:

$$Code = 2^{N-1} \times \left[\left(AIN \times GAIN / \left(1.024 \times V_{REF}\right)\right) + 1\right]$$

where:

AIN is the analog input voltage.

GAIN in the PGA gain, i.e., 1 on the ±2.56 V range and 128 on the ±20 mV range.

N = 16.

Excitation Currents

The AD7709 also contains three software configurable constant current sources. IEXC1 and IEXC2 provide 200 μA of current while IEXC3 provides 25 μA of current. All source current from V_{DD} is directed to either the IOUT1 or IOUT2 pins of the device. These current sources are controlled via bits in the Configuration Register. The configuration bits enable the current sources, and they can be configured to source current individually to both pins or a combination of currents, i.e., 400 μA, 225 μA, or 425 μA to either of the selected output pins. These current sources can be used to excite external resistive bridge or RTD sensors.

Crystal Oscillator

The AD7709 is intended for use with a 32.768 kHz watch crystal. A PLL internally locks onto a multiple of this frequency to provide a stable 4.194304 MHz clock for the ADC. The modulator sample rate is the same as the crystal oscillator frequency.

The start-up time associated with 32.768 kHz crystals is typically 300 ms. The OSCPD bit in the Communications Register can be used to prevent the oscillator from powering down when the AD7709 is placed in power-down mode. This avoids having to wait 300 ms after exiting power-down to start a conversion at the expense of raising the power-down current.

Reference Input

The AD7709 has a fully differential reference input capability for the channel. On the channel, the reference inputs can be REFIN1(+) and REFIN1(–) or REFIN2(+) and REFIN2(–). They provide a differential reference input capability. The common-mode range for these differential inputs is from GND to V_{DD}. The reference input is unbuffered and therefore excessive R-C source impedances will introduce gain errors. The nominal reference voltage, V_{REF}, ((REFIN1(+) – REFIN1(–) or (REFIN2(+) – REFIN2(–)), for specified operation is 2.5 V, but the AD7709 is functional with reference voltages from 1 V to V_{DD}. In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the part, the effect of the low frequency noise in the excitation source will be removed because the application is ratiometric. If the AD7709 is used in a nonratiometric application, a low noise reference should be used. Recommended reference voltage sources for the AD7709 include the AD780, REF43, and REF192. It should also be noted that the reference inputs provide a high impedance, dynamic load. Because the input impedance of each reference input is dynamic, resistor/capacitor combinations on these inputs can cause dc gain errors, depending on the output impedance of the source that is driving the reference inputs. Reference voltage sources like those recommended above (e.g., AD780) will typically have low output impedances and are therefore tolerant to having decoupling capacitors on the REFIN(+) without introducing gain errors in the system. Deriving the reference input voltage across an external resistor, as shown in Figure 18, will mean that the reference input sees a significant external source impedance. External decoupling on the REFIN pins would not be recommended in this type of circuit configuration.

Reset Input

The $\overline{\text{RESET}}$ input on the AD7709 resets all the logic, the digital filter, and the analog modulator while all on-chip registers are reset to their default state. $\overline{\text{RDY}}$ is driven high and the AD7709 ignores all communications to any of its registers while the $\overline{\text{RESET}}$ input is low. When the $\overline{\text{RESET}}$ input returns high, the AD7709 operates with its default setup conditions and it is necessary to set up all registers after a $\overline{\text{RESET}}$ command.

Power-Down Mode

Loading 0 to the STBY bit in the ADC Communications Register places the AD7709 in device power-down mode. The AD7709 retains the contents of all its on-chip registers (including the data register) while in power-down mode.

The device power-down mode does not affect the digital interface, but it does affect the status of the $\overline{\text{RDY}}$ pin. Putting the AD7709 into power-down mode will reset the $\overline{\text{RDY}}$ line high. Placing the part in power-down mode reduces the total current to 26 μA typical when the part is operated at 5 V with the oscillator running during power-down mode. With the oscillator shut down, the total I_{DD} is 1.5 μA typical at 3 V and 6.5 μA typical at 5 V.

Grounding and Layout

Since the analog inputs and reference inputs on the ADC are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part will remove common-mode noise on these inputs. The digital filter will provide rejection of broadband noise on the power supply, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs, provided these noise sources do not saturate the analog modulator. As a result, the AD7709 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7709 is so high, and the noise levels from the AD7709 so low, care must be taken with regard to grounding and layout.