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ANALOG DEVICES

3 V/5 V, CMOS, 500 μA Signal Conditioning ADC

AD7714

FEATURES

Charge Balancing ADC
- **24 Bits No Missing Codes**
- **0.0015% Nonlinearity**

Five-Channel Programmable Gain Front End
- **Gains from 1 to 128**
- **Can Be Configured as Three Fully Differential Inputs or Five Pseudo-Differential Inputs**

Three-Wire Serial Interface
- **SPI™, QSPI™, MICROWIRE™ and DSP Compatible**

3 V (AD7714-3) or 5 V (AD7714-5) Operation

Low Noise (<150 nV rms)

Low Current (350 μA typ) with Power-Down (5 μA typ)

AD7714Y Grade:
- **+2.7 V to 3.3 V or +4.75 V to +5.25 V Operation**
- **0.0010% Linearity Error**
- **–40°C to +105°C Temperature Range**
- **Schmitt Trigger on SCLK and DIN**
- **Low Current (226 μA typ) with Power-Down (4 μA typ)**
- **Lower Power Dissipation than Standard AD7714**
- **Available in 24-Lead TSSOP Package**

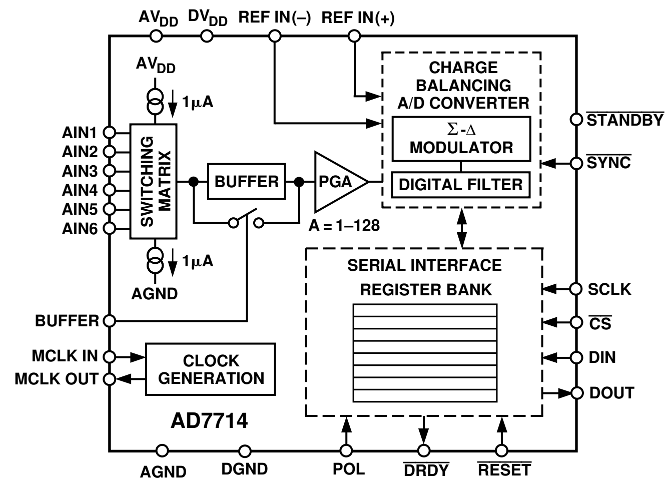
Low-Pass Filter with Programmable Filter Cutoffs

Ability to Read/Write Calibration Coefficients

APPLICATIONS

Portable Industrial Instruments
Portable Weigh Scales
Loop-Powered Systems
Pressure Transducers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION†

The AD7714 is a complete analog front end for low-frequency measurement applications. The device accepts low level signals directly from a transducer and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

The part features three differential analog inputs (which can also be configured as five pseudo-differential analog inputs) as well as a differential reference input. It operates from a single supply (+3 V or +5 V). The AD7714 thus performs all signal conditioning and conversion for a system consisting of up to five channels.

The AD7714 is ideal for use in smart, microcontroller- or DSP-based systems. It features a serial interface that can be configured for three-wire operation. Gain settings, signal polarity and channel selection can be configured in software using the serial port. The AD7714 provides self-calibration, system calibration and background calibration options and also allows the user to read and write the on-chip calibration registers.

CMOS construction ensures very low power dissipation, and the power-down mode reduces the standby power consumption to 15 μW typ. The part is available in a 24-pin, 0.3 inch-wide, plastic dual-in-line package (DIP); a 24-lead small outline (SOIC) package, a 28-lead shrink small outline package (SSOP) and a 24-lead thin shrink small outline package (TSSOP).

PRODUCT HIGHLIGHTS

1. The AD7714Y offers the following features in addition to the standard AD7714: wider temperature range, Schmitt trigger on SCLK and DIN, operation down to 2.7 V, lower power consumption, better linearity, and availability in 24-lead TSSOP package.
2. The AD7714 consumes less than 500 μA ($f_{CLK\ IN}$ = 1 MHz) or 1 mA ($f_{CLK\ IN}$ = 2.5 MHz) in total supply current, making it ideal for use in loop-powered systems.
3. The programmable gain channels allow the AD7714 to accept input signals directly from a strain gage or transducer removing a considerable amount of signal conditioning.
4. The AD7714 is ideal for microcontroller or DSP processor applications with a three-wire serial interface reducing the number of interconnect lines and reducing the number of opto-couplers required in isolated systems. The part contains on-chip registers that allow control over filter cutoff, input gain, channel selection, signal polarity and calibration modes.
5. The part features excellent static performance specifications with 24-bit no missing codes, ±0.0015% accuracy and low rms noise (140 nV). Endpoint errors and the effects of temperature drift are eliminated by on-chip self-calibration, which removes zero-scale and full-scale errors.

†See page 39 for data sheet index.
SPI and QSPI are trademarks of Motorola, Inc.
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REV. C

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AD7714* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7714 Evaluation Kit

DOCUMENTATION

Application Notes

- AN-202: An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change
- AN-283: Sigma-Delta ADCs and DACs
- AN-311: How to Reliably Protect CMOS Circuits Against Power Supply Overvoltaging
- AN-388: Using Sigma-Delta Converters-Part 1
- AN-389: Using Sigma-Delta Converters-Part 2
- AN-397: Electrically Induced Damage to Standard Linear Integrated Circuits:
- AN-553: Adjusting the Calibration Coefficients on the AD771X Family of ADCs
- AN-607: Selecting a Low Bandwidth (<15 kSPS) Sigma-Delta ADC
- AN-615: Peak-to-Peak Resolution Versus Effective Resolution

Data Sheet

- AD7714: CMOS, 3V/5V, 500 μA, 24-Bit Sigma-Delta, Signal Conditioning ADC Data Sheet

User Guides

- UG-761: Evaluation Board for the AD7714-3, 24-Bit Low Power Sigma-Delta ADC

TOOLS AND SIMULATIONS

- AD7714 Digital Filter Model
- dt_Register_Assistant
- Sigma-Delta ADC Tutorial

REFERENCE MATERIALS

Technical Articles

- Delta-Sigma Rocks RF, As ADC Designers Jump On Jitter
- MS-2210: Designing Power Supplies for High Speed ADC
- Part 1: Circuit Suggestions Using Features and Functionality of New Sigma-Delta ADCs
- Part 2: Circuit Suggestions Using Features and Functionality of New Sigma-Delta ADCs

DESIGN RESOURCES

- AD7714 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7714 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

AD7714-5–SPECIFICATIONS (AV_{DD} = +5 V, DV_{DD} = +3.3 V or +5 V, REF IN(+) = +2.5 V; REF IN(–) = AGND; $f_{CLK\ IN}$ = 2.4576 MHz unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	24	Bits min	Guaranteed by Design. Bipolar Mode. For Filter Notches ≤ 60 Hz
	22	Bits min	For Filter Notch = 100 Hz
	18	Bits min	For Filter Notch = 250 Hz
	15	Bits min	For Filter Notch = 500 Hz
	12	Bits min	For Filter Notch = 1 kHz
Output Noise	See Tables I to IV		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity	±0.0015	% of FSR max	Filter Notches ≤ 60 Hz
Unipolar Offset Error	See Note 2		
Unipolar Offset Drift[3]	0.5	μV/°C typ	For Gains of 1, 2, 4
	0.3	μV/°C typ	For Gains of 8, 16, 32, 64, 128
Bipolar Zero Error	See Note 2		
Bipolar Zero Drift[3]	0.5	μV/°C typ	For Gains of 1, 2, 4
	0.3	μV/°C typ	For Gains of 8, 16, 32, 64, 128
Positive Full-Scale Error[4]	See Note 2		
Full-Scale Drift[3, 5]	0.5	μV/°C typ	For Gains of 1, 2, 4
	0.3	μV/°C typ	For Gains of 8, 16, 32, 64, 128
Gain Error[6]	See Note 2		
Gain Drift[3, 7]	0.5	ppm of FSR/°C typ	
Bipolar Negative Full-Scale Error	±0.0015	% of FSR max	Typically ±0.0004%
Bipolar Negative Full-Scale Drift[3]	1	μV/°C typ	For Gains of 1, 2, 4
	0.6	μV/°C typ	For Gains of 8, 16, 32, 64, 128
ANALOG INPUTS/REFERENCE INPUTS			Specifications for AIN and REF IN Unless Noted
Input Common-Mode Rejection (CMR)	90	dB min	At DC. Typically 102 dB
Normal-Mode 50 Hz Rejection[8]	100	dB min	For Filter Notches of 10 Hz, 25 Hz, 50 Hz, ±0.02 × f_{NOTCH}
Normal-Mode 60 Hz Rejection[8]	100	dB min	For Filter Notches of 10 Hz, 30 Hz, 60 Hz, ±0.02 × f_{NOTCH}
Common-Mode 50 Hz Rejection[8]	150	dB min	For Filter Notches of 10 Hz, 25 Hz, 50 Hz, ±0.02 × f_{NOTCH}
Common-Mode 60 Hz Rejection[8]	150	dB min	For Filter Notches of 10 Hz, 30 Hz, 60 Hz, ±0.02 × f_{NOTCH}
Common-Mode Voltage Range[9]	AGND to AV_{DD}	V min to V max	AIN for BUFFER = 0 and REF IN
Absolute AIN/REF IN Voltage[9]	AGND – 30 mV	V min	AIN for BUFFER = 0 and REF IN
	AV_{DD} + 30 mV	V max	
Absolute/Common-Mode AIN Voltage[9]	AGND + 50 mV	V min	BUFFER = 1. A Version
	AV_{DD} – 1.5 V	V max	
AIN Input Current[8]	1	nA max	A Version
AIN Sampling Capacitance[8]	7	pF max	
AIN Differential Voltage Range[10]	0 to $+V_{REF}$/GAIN[11]	nom	Unipolar Input Range (B/U Bit of Filter High Register = 1)
	$±V_{REF}$/GAIN	nom	Bipolar Input Range (B/U Bit of Filter High Register = 0)
AIN Input Sampling Rate, f_S	GAIN × $f_{CLK\ IN}$/64		For Gains of 1, 2, 4
	$f_{CLK\ IN}$/8		For Gains of 8, 16, 32, 64, 128
REF IN(+) – REF IN(–) Voltage	+2.5	V nom	±1% for Specified Performance. Functional with Lower V_{REF}
REF IN Input Sampling Rate, f_S	$f_{CLK\ IN}$/64		
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs Except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = +5 V
V_{INL}, Input Low Voltage	0.4	V max	DV_{DD} = +3.3 V
V_{INH}, Input High Voltage	2.4	V min	DV_{DD} = +5 V
V_{INH}, Input High Voltage	2.0	V min	DV_{DD} = +3.3 V
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = +5 V
V_{INL}, Input Low Voltage	0.4	V max	DV_{DD} = +3.3 V
V_{INH}, Input High Voltage	3.5	V min	DV_{DD} = +5 V
V_{INH}, Input High Voltage	2.5	V min	DV_{DD} = +3.3 V
LOGIC OUTPUTS (Including MCLK OUT)			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 800 μA Except for MCLK OUT.[12] DV_{DD} = +5 V
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 100 μA Except for MCLK OUT.[12] DV_{DD} = +3.3 V
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 200 μA Except for MCLK OUT.[12] DV_{DD} = +5 V
V_{OH}, Output High Voltage	DV_{DD} – 0.6 V	V min	I_{SOURCE} = 100 μA Except for MCLK OUT.[12] DV_{DD} = +3.3 V
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[13]	9	pF typ	
Data Output Coding	Binary		Unipolar Mode
	Offset Binary		Bipolar Mode

NOTES

[1]Temperature range is as follows: A Versions: –40°C to +85°C.

[2]A calibration is effectively a conversion so these errors will be of the order of the conversion noise shown in Tables I to IV. This applies after calibration at the temperature of interest.

[3]Recalibration at any temperature will remove these drift errors.

[4]Positive Full-Scale Error includes Zero-Scale Errors (Unipolar Offset Error or Bipolar Zero Error) and applies to both unipolar and bipolar input ranges.

[5]Full-Scale Drift includes Zero-Scale Drift (Unipolar Offset Drift or Bipolar Zero Drift) and applies to both unipolar and bipolar input ranges.

[6]Gain Error does not include Zero-Scale Errors. It is calculated as Full-Scale Error—Unipolar Offset Error for unipolar ranges and Full-Scale Error—Bipolar Zero Error for bipolar ranges.

AD7714-3–SPECIFICATIONS (AV_{DD} = +3.3 V, DV_{DD} = +3.3 V, REF IN(+) = +1.25 V; REF IN(–) = AGND; $f_{CLK\ IN}$ = 2.4576 MHz unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	24	Bits min	Guaranteed by Design. Bipolar Mode. For Filter Notches ≤ 60 Hz
	22	Bits min	For Filter Notch = 100 Hz
	18	Bits min	For Filter Notch = 250 Hz
	15	Bits min	For Filter Notch = 500 Hz
	12	Bits min	For Filter Notch = 1 kHz
Output Noise	See Tables I to IV		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity	±0.0015	% of FSR max	Filter Notches ≤ 60 Hz
Unipolar Offset Error	See Note 2		
Unipolar Offset Drift[3]	0.4	μV/°C typ	For Gains of 1, 2, 4
	0.1	μV/°C typ	For Gains of 8, 16, 32, 64, 128
Bipolar Zero Error	See Note 2		
Bipolar Zero Drift[3]	0.4	μV/°C typ	For Gains of 1, 2, 4
	0.1	μV/°C typ	For Gains of 8, 16, 32, 64, 128
Positive Full-Scale Error[4]	See Note 2		
Full-Scale Drift[3, 5]	0.4	μV/°C typ	For Gains of 1, 2, 4
	0.1	μV/°C typ	For Gains of 8, 16, 32, 64, 128
Gain Error[6]	See Note 2		
Gain Drift[3, 7]	0.2	ppm of FSR/°C typ	
Bipolar Negative Full-Scale Error	±0.003	% of FSR max	Typically ±0.0004%
Bipolar Negative Full-Scale Drift[3]	1	μV/°C typ	For Gains of 1, 2, 4
	0.6	μV/°C typ	For Gains of 8, 16, 32, 64, 128
ANALOG INPUTS/REFERENCE INPUTS			Specifications for AIN and REF IN Unless Noted
Input Common-Mode Rejection (CMR)	90	dB min	At DC. Typically 102 dB.
Normal-Mode 50 Hz Rejection[8]	100	dB min	For Filter Notches of 10 Hz, 25 Hz, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
Normal-Mode 60 Hz Rejection[8]	100	dB min	For Filter Notches of 10 Hz, 30 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode 50 Hz Rejection[8]	150	dB min	For Filter Notches of 10 Hz, 25 Hz, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode 60 Hz Rejection[8]	150	dB min	For Filter Notches of 10 Hz, 30 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode Voltage Range[9]	AGND to AV_{DD}	V min to V max	AIN for BUFFER = 0 and REF IN
Absolute AIN/REF IN Voltage[9]	AGND – 30 mV	V min	AIN for BUFFER = 0 and REF IN
	AV_{DD} + 30 mV	V max	
Absolute/Common-Mode AIN Voltage[9]	AGND + 50 mV	V min	BUFFER = 1
	AV_{DD} – 1.5 V	V max	
AIN Input Current[8]	1	nA max	
AIN Sampling Capacitance[8]	7	pF max	
AIN Differential Voltage Range[10]	0 to $+V_{REF}$/GAIN[11]	nom	Unipolar Input Range (B/U Bit of Filter High Register = 1)
	$\pm V_{REF}$/GAIN	nom	Bipolar Input Range (B/U Bit of Filter High Register = 0)
AIN Input Sampling Rate, f_S	GAIN × $f_{CLK\ IN}$/64		For Gains of 1, 2, 4
	$f_{CLK\ IN}$/8		For Gains of 8, 16, 32, 64, 128
REF IN(+) – REF IN(–) Voltage	+1.25	V nom	±1% for Specified Performance. Part Functions with Lower V_{REF}
REF IN Input Sampling Rate, f_S	$f_{CLK\ IN}$/64		
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs Except MCLK IN			
V_{INL}, Input Low Voltage	0.4	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.4	V max	
V_{INH}, Input High Voltage	2.5	V min	
LOGIC OUTPUTS (Including MCLK OUT)			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 100 μA Except for MCLK OUT[12]
V_{OH}, Output High Voltage	DV_{DD} – 0.6	V min	I_{SOURCE} = 100 μA Except for MCLK OUT[12]
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[13]	9	pF typ	
Data Output Coding	Binary		Unipolar Mode
	Offset Binary		Bipolar Mode

NOTES

[7]Gain Error Drift does not include Unipolar Offset Drift/Bipolar Zero Drift. It is effectively the drift of the part if zero-scale calibrations only were performed as is the case with background calibration.

[8]These numbers are guaranteed by design and/or characterization.

[9]The common-mode voltage range on the input pairs applies provided the absolute input voltage specification is obeyed.

[10]The input voltage range on the analog inputs is given here with respect to the voltage on the respective negative input of its differential or pseudo-differential pair. See Table VII for which inputs form differential pairs.

[11]V_{REF} = REF IN(+) – REF IN(–).

[12]These logic output levels apply to the MCLK OUT output only when it is loaded with a single CMOS load.

[13]Sample tested at +25°C to ensure compliance.

[14]See Burnout Current section.

AD7714–SPECIFICATIONS (AV_{DD} = + 3.3 V to +5 V, DV_{DD} = +3.3 V to +5 V, REF IN(+) = +1.25 V (AD7714-3) or +2.5 V (AD7714-5); REF IN(–) = AGND; MCLK IN = 1 MHz to 2.4576 MHz unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions	Units	Conditions/Comments
TRANSDUCER BURNOUT[14]			
Current	1	µA nom	
Initial Tolerance	±10	% typ	
Drift	0.1	%/°C typ	
SYSTEM CALIBRATION			
Positive Full-Scale Calibration Limit[15]	$(1.05 \times V_{REF})$/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit[15]	$-(1.05 \times V_{REF})$/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[16]	$-(1.05 \times V_{REF})$/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span[16]	$0.8 \times V_{REF}$/GAIN	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	$(2.1 \times V_{REF})$/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} Voltage (AD7714-3)	+3 to +3.6	V	For Specified Performance
AV_{DD} Voltage (AD7714-5)	+4.75 to +5.25	V	For Specified Performance
DV_{DD} Voltage	+3 to +5.25	V	For Specified Performance
Power Supply Currents			
AV_{DD} Current			AV_{DD} = 3.3 V or 5 V. BST Bit of Filter High Register = 0[17]
	0.27	mA max	Typically 0.2 mA. BUFFER = 0 V. $f_{CLK\ IN}$ = 1 MHz or 2.4576 MHz
	0.6	mA max	Typically 0.4 mA. BUFFER = DV_{DD}. $f_{CLK\ IN}$ = 1 MHz or 2.4576 MHz
			AV_{DD} = 3.3 V or 5 V. BST Bit of Filter High Register = 1[17]
	0.5	mA max	Typically 0.3 mA. BUFFER = 0 V. $f_{CLK\ IN}$ = 2.4576 MHz
	1.1	mA max	Typically 0.8 mA. BUFFER = DV_{DD}. $f_{CLK\ IN}$ = 2.4576 MHz
DV_{DD} Current[18]			Digital I/Ps = 0 V or DV_{DD}. External MCLK IN
	0.23	mA max	Typically 0.15 mA. DV_{DD} = 3.3 V. $f_{CLK\ IN}$ = 1 MHz
	0.4	mA max	Typically 0.3 mA. DV_{DD} = 5 V. $f_{CLK\ IN}$ = 1 MHz
	0.5	mA max	Typically 0.4 mA. DV_{DD} = 3.3 V. $f_{CLK\ IN}$ = 2.4576 MHz
	0.8	mA max	Typically 0.6 mA. DV_{DD} = 5 V. $f_{CLK\ IN}$ = 2.4576 MHz
Power Supply Rejection[19]	See Note 20	dB typ	
Normal-Mode Power Dissipation[18]			AV_{DD} = DV_{DD} = +3.3 V. Digital I/Ps = 0 V or DV_{DD}. External MCLK IN
	1.65	mW max	Typically 1.25 mW. BUFFER = 0 V. $f_{CLK\ IN}$ = 1 MHz. BST Bit = 0
	2.75	mW max	Typically 1.8 mW. BUFFER = +3.3 V. $f_{CLK\ IN}$ = 1 MHz. BST Bit = 0
	2.55	mW max	Typically 2 mW. BUFFER = 0 V. $f_{CLK\ IN}$ = 2.4576 MHz. BST Bit = 0
	3.65	mW max	Typically 2.6 mW. BUFFER = +3.3 V. $f_{CLK\ IN}$ = 2.4576 MHz. BST Bit = 0
Normal-Mode Power Dissipation			AV_{DD} = DV_{DD} = +5 V. Digital I/Ps = 0 V or DV_{DD}. External MCLK IN
	3.35	mW max	Typically 2.5 mW. BUFFER = 0 V. $f_{CLK\ IN}$ = 1 MHz. BST Bit = 0
	5	mW max	Typically 3.5 mW. BUFFER = +5 V. $f_{CLK\ IN}$ = 1 MHz. BST Bit = 0
	5.35	mW max	Typically 4 mW. BUFFER = 0 V. $f_{CLK\ IN}$ = 2.4576 MHz. BST Bit = 0
	7	mW max	Typically 5 mW. BUFFER = +5 V. $f_{CLK\ IN}$ = 2.4576 MHz. BST Bit = 0
Standby (Power-Down) Current[21]	40	µA max	External MCLK IN = 0 V or DV_{DD}. Typically 20 µA. V_{DD} = +5 V
Standby (Power-Down) Current[21]	10	µA max	External MCLK IN = 0 V or DV_{DD}. Typically 5 µA. V_{DD} = +3.3 V

NOTES

[15]After calibration, if the input voltage exceeds positive full scale, the converter will output all 1s. If the input is less than negative full scale, then the device outputs all 0s.

[16]These calibration and span limits apply provided the absolute voltage on the analog inputs does not exceed AV_{DD} + 30 mV or go more negative than AGND – 30 mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

[17]For higher gains (≥8) at $f_{CLK\ IN}$ = 2.4576 MHz, the BST bit of the Filter High Register must be set to 1. For other conditions, it can be set to 0.

[18]When using a crystal or ceramic resonator across the MCLK pins as the clock source for the device, the DV_{DD} current and power dissipation will vary depending on the crystal or resonator type (see Clocking and Oscillator Circuit section).

[19]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 5 Hz, 10 Hz, 25 Hz or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 6 Hz, 10 Hz, 30 Hz or 60 Hz.

[20]PSRR depends on gain. For Gain of 1 : 70 dB typ: For Gain of 2 : 75 dB typ; For Gain of 4 : 80 dB typ; For Gains of 8 to 128 : 85 dB typ.

[21]If the external master clock continues to run in standby mode, the standby current increases to 150 µA typical with 5 V supplies and 75 µA typical with 3.3 V supplies. When using a crystal or ceramic resonator across the MCLK pins as the clock source for the device, the internal oscillator continues to run in standby mode and the power dissipation depends on the crystal or resonator type (see Standby Mode section).

Specifications subject to change without notice.

AD7714Y–SPECIFICATIONS

($AV_{DD} = DV_{DD}$ = +2.7 V to +3.3 V or 4.75 V to 5.25 V, REF IN(+) = +1.25 V; with AV_{DD} = 3 V and +2.5 V with AV_{DD} = 5 V; REF IN(–) = AGND; MCLK IN = 2.4576 MHz unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Y Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	24	Bits min	Guaranteed by Design. For Filter Notches ≤ 60 Hz
	22	Bits min	For Filter Notch = 100 Hz
	18	Bits min	For Filter Notch = 250 Hz
	15	Bits min	For Filter Notch = 500 Hz
	12	Bits min	For Filter Notch = 1 kHz
Output Noise	See Tables I to IV		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity	±0.001	% of FSR max	Filter Notches ≤ 60 Hz.
Unipolar Offset Error	See Note 2		
Unipolar Offset Drift[3]	0.4	µV/°C typ	For Gains of 1, 2, 4
	0.1	µV/°C typ	For Gains of 8, 16, 32, 64, 128
Bipolar Zero Error	See Note 2		
Bipolar Zero Drift[3]	0.4	µV/°C typ	For Gains of 1, 2, 4
	0.1	µV/°C typ	For Gains of 8, 16, 32, 64, 128
Positive Full-Scale Error[4]	See Note 2		
Full-Scale Drift[3, 5]	0.4	µV/°C typ	For Gains of 1, 2, 4
	0.1	µV/°C typ	For Gains of 8, 16, 32, 64, 128
Gain Error[6]	See Note 2		
Gain Drift[3, 7]	0.2	ppm of FSR/°C typ	
Bipolar Negative Full-Scale Error[2]	±0.0015	% of FSR max	AV_{DD} = 5 V. Typically ±0.0004%
	±0.003	% of FSR max	AV_{DD} = 3 V. Typically ±0.0004%
Bipolar Negative Full-Scale Drift[3]	1	µV/°C typ	For Gains of 1 to 4
	0.6	µV/°C typ	For Gains of 8 to 128
ANALOG INPUTS/REFERENCE INPUTS			Specifications for AIN and REF IN Unless Noted
Input Common-Mode Rejection (CMR)[8]	90	dB min	At DC. Typically 102 dB.
Normal-Mode 50 Hz Rejection[8]	100	dB min	For Filter Notches of 10 Hz, 25 Hz, 50 Hz, ±0.02 × f_{NOTCH}
Normal-Mode 60 Hz Rejection[8]	100	dB min	For Filter Notches of 10 Hz, 30 Hz, 60 Hz, ±0.02 × f_{NOTCH}
Common-Mode 50 Hz Rejection[8]	150	dB min	For Filter Notches of 10 Hz, 25 Hz, 50 Hz, ±0.02 × f_{NOTCH}
Common-Mode 60 Hz Rejection[8]	150	dB min	For Filter Notches of 10 Hz, 30 Hz, 60 Hz, ±0.02 × f_{NOTCH}
Absolute/Common-Mode REF IN Voltage[8]	AGND to AV_{DD}	V min to V max	
Absolute/Common-Mode AIN Voltage[8, 9]	AGND – 30 mV	V min	BUF Bit of Setup Register = 0
	AV_{DD} + 30 mV	V max	
Absolute/Common-Mode AIN Voltage[8, 9]	AGND + 50 mV	V min	BUF Bit of Setup Register = 1
	AV_{DD} – 1.5 V	V max	
AIN DC Input Current[8]	1	nA max	
AIN Sampling Capacitance[8]	7	pF max	
AIN Differential Voltage Range[10]	0 to $+V_{REF}$/GAIN[11]	nom	Unipolar Input Range (B/U Bit of Filter High Register = 1)
	$\pm V_{REF}$/GAIN	nom	Bipolar Input Range (B/U Bit of Filter High Register = 0)
AIN Input Sampling Rate, f_S	GAIN × $f_{CLK\ IN}$/64		For Gains of 1 to 4
	$f_{CLK\ IN}$/8		For Gains of 8 to 128
Reference Input Range			
REF IN(+) – REF IN(–) Voltage	1/1.75	V min/max	AV_{DD} = 2.7 V to 3.3 V. V_{REF} = 1.25 ±1% for Specified Performance
REF IN(+) – REF IN(–) Voltage	1/3.5	V min/max	AV_{DD} = 4.75 V to 5.25 V. V_{REF} = 2.5 ±1% for Specified Performance
REF IN Input Sampling Rate, f_S	$f_{CLK\ IN}$/64		
LOGIC INPUTS			
Input Current	±10	µA max	
All Inputs Except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = 5 V
	0.4	V max	DV_{DD} = 3 V
V_{INH}, Input High Voltage	2.4	V min	DV_{DD} = 5 V
	2	V min	DV_{DD} = 3 V
SCLK & DIN Only (Schmitt Triggered Input)			DV_{DD} = 5 V NOMINAL
V_{T+}	1.4/3	V min/V max	
V_{T-}	0.8/1.4	V min/V max	
$V_{T+} - V_{T-}$	0.4/0.8	V min/V max	
SCLK & DIN Only (Schmitt Triggered Input)			DV_{DD} = 3 V NOMINAL
V_{T+}	1/2.5	V min/V max	
V_{T-}	0.4/1.1	V min/V max	
$V_{T+} - V_{T-}$	0.375/0.8	V min/V max	
MCLK In Only			DV_{DD} = 5 V NOMINAL
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	3.5	V min	
MCLK In Only			DV_{DD} = 3 V NOMINAL
V_{INL}, Input Low Voltage	0.4	V max	
V_{INH}, Input High Voltage	2.5	V min	
LOGIC OUTPUTS (Including MCLK OUT)			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 800 µA with DV_{DD} = 5 V. Except for MCLK OUT[12]
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 100 µA with DV_{DD} = 3 V. Except for MCLK OUT[12]
V_{OH}, Output High Voltage	4	V min	I_{SOURCE} = 200 µA with DV_{DD} = 5 V. Except for MCLK OUT[12]

Parameter	Y Versions	Units	Conditions/Comments
LOGIC OUTPUTS (Continued))			
V_{OH}, Output High Voltage	DV_{DD} – 0.6	V min	I_{SOURCE} = 100 μA with DV_{DD} = 3 V. Except for MCLK OUT[12]
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[13]	9	pF typ	
Data Output Coding	Binary		Unipolar Mode
	Offset Binary		Bipolar Mode
TRANSDUCER BURNOUT[14]			
Current	1	μA nom	
Initial Tolerance	±10	% typ	
Drift	0.1	%/°C typ	
SYSTEM CALIBRATION			
Positive Full-Scale Calibration Limit[15]	$(1.05 \times V_{REF})$/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit[15]	$-(1.05 \times V_{REF})$/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[16]	$-(1.05 \times V_{REF})$/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span[16]	$0.8 \times V_{REF}$/GAIN	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	$(2.1 \times V_{REF})$/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} Voltage	+2.7 to +3.3 or	V	
	+4.75 to +5.25	V	For Specified Performance
DV_{DD} Voltage	+2.7 to +5.25	V	For Specified Performance
Power Supply Currents			
AV_{DD} Current			AV_{DD} = 3 V or 5 V. BST Bit of Filter High Register = 0[17], CLKDIS = 1
	0.28	mA max	Typically 0.22 mA. BUFFER = 0 V. $f_{CLK\ IN}$ = 1 MHz or 2.4576 MHz
	0.6	mA max	Typically 0.45 mA. BUFFER = DV_{DD}. $f_{CLK\ IN}$ = 1 MHz or 2.4576 MHz
			AV_{DD} = 3 V or 5 V. BST Bit of Filter High Register = 1[17]
	0.5	mA max	Typically 0.38 mA. BUFFER = 0 V. $f_{CLK\ IN}$ = 2.4576 MHz
	1.1	mA max	Typically 0.8 mA. BUFFER = DV_{DD}. $f_{CLK\ IN}$ = 2.4576 MHz
DV_{DD} Current[18]			Digital I/Ps = 0 V or DV_{DD}. External MCLK IN, CLKDIS = 1
	0.080	mA max	Typically 0.06 mA. DV_{DD} = 3 V. $f_{CLK\ IN}$ = 1 MHz
	0.16	mA max	Typically 0.13 mA. DV_{DD} = 5 V. $f_{CLK\ IN}$ = 1 MHz
	0.18	mA max	Typically 0.15 mA. DV_{DD} = 3 V. $f_{CLK\ IN}$ = 2.4576 MHz
	0.35	mA max	Typically 0.3 mA. DV_{DD} = 5 V. $f_{CLK\ IN}$ = 2.4576 MHz
Power Supply Rejection[19]	See Note 20	dB typ	
Normal-Mode Power Dissipation[18]			AV_{DD} = DV_{DD} = +3 V. Digital I/Ps = 0 V or DV_{DD}. External MCLK IN BST Bit of Filter High Register = 0[17]
	1.05	mW max	Typically 0.84 mW. BUFFER = 0 V. $f_{CLK\ IN}$ = 1 MHz. BST Bit = 0
	2.04	mW max	Typically 1.53 mW. BUFFER = +3 V. $f_{CLK\ IN}$ = 1 MHz. BST Bit = 0
	1.35	mW max	Typically 1.11 mW. BUFFER = 0 V. $f_{CLK\ IN}$ = 2.4576 MHz. BST Bit = 0
	2.34	mW max	Typically 1.9 mW. BUFFER = +3 V. $f_{CLK\ IN}$ = 2.4576 MHz. BST Bit = 0
Normal-Mode Power Dissipation			AV_{DD} = DV_{DD} = +5 V. Digital I/Ps = 0 V or DV_{DD}. External MCLK IN
	2.1	mW max	Typically 1.75 mW. BUFFER = 0 V. $f_{CLK\ IN}$ = 1 MHz. BST Bit = 0
	3.75	mW max	Typically 2.9 mW. BUFFER = +5 V. $f_{CLK\ IN}$ = 1 MHz. BST Bit = 0
	3.1	mW max	Typically 2.6 mW. BUFFER = 0 V. $f_{CLK\ IN}$ = 2.4576 MHz. BST Bit = 0
	4.75	mW max	Typically 3.75 mW. BUFFER = +5 V. $f_{CLK\ IN}$ = 2.4576 MHz. BST Bit = 0
Standby (Power-Down) Current[21]	18	μA max	External MCLK IN = 0 V or DV_{DD}. Typically 9 μA. V_{DD} = +5 V
Standby (Power-Down) Current[21]	10	μA max	External MCLK IN = 0 V or DV_{DD}. Typically 4 μA. V_{DD} = +3 V

NOTES

[1]Temperature range is as follows: Y Version: –40°C to +105°C.
[2]A calibration is effectively a conversion so these errors will be of the order of the conversion noise shown in Tables I to IV. This applies after calibration at the temperature of interest.
[3]Recalibration at any temperature will remove these drift errors.
[4]Positive Full-Scale Error includes Zero-Scale Errors (Unipolar Offset Error or Bipolar Zero Error) and applies to both unipolar and bipolar input ranges.
[5]Full-Scale Drift includes Zero-Scale Drift (Unipolar Offset Drift or Bipolar Zero Drift) and applies to both unipolar and bipolar input ranges.
[6]Gain Error does not include Zero-Scale Errors. It is calculated as Full-Scale Error—Unipolar Offset Error for unipolar ranges and Full-Scale Error—Bipolar Zero Error for bipolar ranges.
[7]Gain Error Drift does not include Unipolar Offset Drift/Bipolar Zero Drift. It is effectively the drift of the part if zero-scale calibrations only were performed as is the case with background calibration.
[8]These numbers are guaranteed by design and/or characterization.
[9]The common-mode voltage range on the input pairs applies provided the absolute input voltage specification is obeyed.
[10]The input voltage range on the analog inputs is given here with respect to the voltage on the respective negative input of its differential or pseudo-differential pair. See Table VII for which inputs form differential pairs.
[11]V_{REF} = REF IN(+) – REF IN(–).
[12]These logic output levels apply to the MCLK OUT output only when it is loaded with a single CMOS load.
[13]Sample tested at +25°C to ensure compliance.
[14]See Burnout Current section.
[15]After calibration, if the input voltage exceeds positive full scale, the converter will output all 1s. If the input is less than negative full scale, then the device outputs all 0s.
[16]These calibration and span limits apply provided the absolute voltage on the analog inputs does not exceed AV_{DD} + 30 mV or go more negative than AGND – 30 mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.
[17]For higher gains (≥8) at $f_{CLK\ IN}$ = 2.4576 MHz, the BST bit of the Filter High Register must be set to 1. For other conditions, it can be set to 0.
[18]When using a crystal or ceramic resonator across the MCLK pins as the clock source for the device, the DV_{DD} current and power dissipation will vary depending on the crystal or resonator type (see Clocking and Oscillator Circuit section).
[19]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 5 Hz, 10 Hz, 25 Hz or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 6 Hz, 10 Hz, 30 Hz or 60 Hz.
[20]PSRR depends on gain.

Gain	1	2	4	8–128
AV_{DD} = 3 V	86 dB	78 dB	85 dB	93 dB
AV_{DD} = 5 V	90 dB	78 dB	84 dB	91 dB

[21]If the external master clock continues to run in standby mode, the standby current increases to 150 μA typical with 5 V supplies and 75 μA typical with 3.3 V supplies. When using a crystal or ceramic resonator across the MCLK pins as the clock source for the device, the internal oscillator continues to run in standby mode and the power dissipation depends on the crystal or resonator type (see Standby Mode section).

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2]

($AV_{DD} = DV_{DD}$ = +2.7 V to +5.25 V; AGND = DGND = 0 V; f_{CLKIN} = 2.5 MHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} (A, Y Versions)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	400	kHz min	Master Clock Frequency: Crystal/Resonator or Externally Supplied
	2.5	MHz max	For Specified Performance
$t_{CLK\ IN\ LO}$	$0.4 \times t_{CLK\ IN}$	ns min	Master Clock Input Low Time. $t_{CLK\ IN} = 1/f_{CLK\ IN}$
$t_{CLK\ IN\ HI}$	$0.4 \times t_{CLK\ IN}$	ns min	Master Clock Input High Time
t_{DRDY}	$500 \times t_{CLK\ IN}$	ns nom	$\overline{DRDY}$ High Time
t_1	100	ns min	$\overline{SYNC}$ Pulsewidth
t_2	100	ns min	$\overline{RESET}$ Pulsewidth
Read Operation			
t_3	0	ns min	$\overline{DRDY}$ to $\overline{CS}$ Setup Time
t_4	0	ns min	$\overline{CS}$ Falling Edge to SCLK Active Edge Setup Time[5]
t_5[6]	0	ns min	SCLK Active Edge to Data Valid Delay[5]
	80	ns max	DV_{DD} = +5 V
	100	ns max	DV_{DD} = +3 V
t_6	100	ns min	SCLK High Pulsewidth
t_7	100	ns min	SCLK Low Pulsewidth
t_8	0	ns min	$\overline{CS}$ Rising Edge to SCLK Active Edge Hold Time[5]
t_9[7]	10	ns min	Bus Relinquish Time after SCLK Active Edge[5]
	60	ns max	DV_{DD} = +5 V
	100	ns max	DV_{DD} = +3 V
t_{10}	100	ns max	SCLK Active Edge to $\overline{DRDY}$ High[5, 8]
Write Operation			
t_{11}	0	ns min	$\overline{CS}$ Falling Edge to SCLK Active Edge Setup Time[5]
t_{12}	30	ns min	Data Valid to SCLK Edge Setup Time
t_{13}	20	ns min	Data Valid to SCLK Edge Hold Time
t_{14}	100	ns min	SCLK High Pulsewidth
t_{15}	100	ns min	SCLK Low Pulsewidth
t_{16}	0	ns min	$\overline{CS}$ Rising Edge to SCLK Edge Hold Time

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.

[2]See Figures 6 and 7. Timing applies for all grades.

[3]CLKIN Duty Cycle range is 45% to 55%. CLKIN must be supplied whenever the AD7714 is not in standby mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[4]The AD7714 is production tested with f_{CLKIN} at 2.4576 MHz (1 MHz for some I_{DD} tests). It is guaranteed by characterization to operate at 400 kHz.

[5]SCLK active edge is falling edge of SCLK with POL = 1; SCLK active edge is rising edge of SCLK with POL = 0.

[6]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

[7]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 100 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

[8]$\overline{DRDY}$ returns high after the first read from the device after an output update. The same data can be read again, if required, while $\overline{DRDY}$ is high although care should be taken that subsequent reads do not occur close to the next output update.

Specifications subject to change without notice.

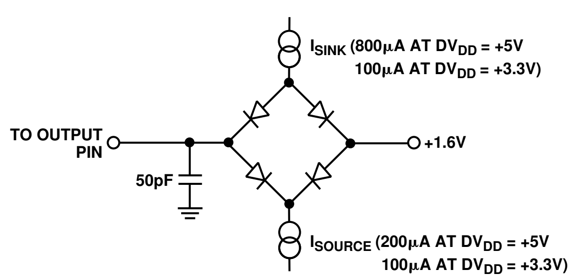


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

ORDERING GUIDE

Model	AV_{DD} Supply	Temperature Range	Package Option*
AD7714AN-5	5 V	–40°C to +85°C	N-24
AD7714AR-5	5 V	–40°C to +85°C	R-24
AD7714ARS-5	5 V	–40°C to +85°C	RS-28
AD7714AN-3	3 V	–40°C to +85°C	N-24
AD7714AR-3	3 V	–40°C to +85°C	R-24
AD7714ARS-3	3 V	–40°C to +85°C	RS-28
AD7714YN	3 V/5 V	–40°C to +105°C	N-24
AD7714YR	3 V/5 V	–40°C to +105°C	R-24
AD7714YRU	3 V/5 V	–40°C to +105°C	RU-24
AD7714AChips-5	5 V	–40°C to +85°C	Die
AD7714AChips-3	3 V	–40°C to +85°C	Die
EVAL-AD7714-5EB	5 V	Evaluation Board	
EVAL-AD7714-3EB	3 V	Evaluation Board	

*N = Plastic DIP; R = SOIC; RS = SSOP; RU = Thin Shrink Small Outline.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND . . . . –0.3 V to +7 V
AV_{DD} to DGND . . . . –0.3 V to +7 V
DV_{DD} to AGND . . . . –0.3 V to +7 V
DV_{DD} to DGND . . . . –0.3 V to +7 V
Analog Input Voltage to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND . . . –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND . . . . . –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND . . . . –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
  Commercial (A Version) . . . . –40°C to +85°C
  Extended (Y Version) . . . . –40°C to +105°C
Storage Temperature Range . . . . –65°C to +150°C
Junction Temperature . . . . +150°C
Plastic DIP Package, Power Dissipation . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . 105°C/W
  Lead Temperature (Soldering, 10 sec) . . . . +260°C
SOIC Package, Power Dissipation . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . 75°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . +215°C
    Infrared (15 sec) . . . . +220°C
SSOP Package, Power Dissipation . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . 109°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . +215°C
    Infrared (15 sec) . . . . +220°C
TSSOP Package, Power Dissipation . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . 128°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . +215°C
    Infrared (15 sec) . . . . +220°C

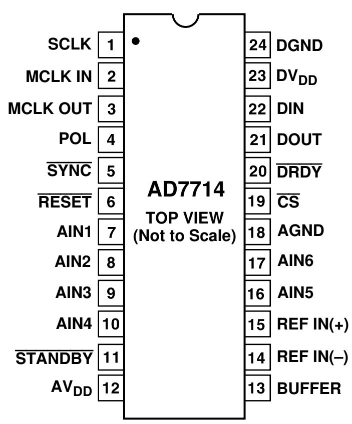
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

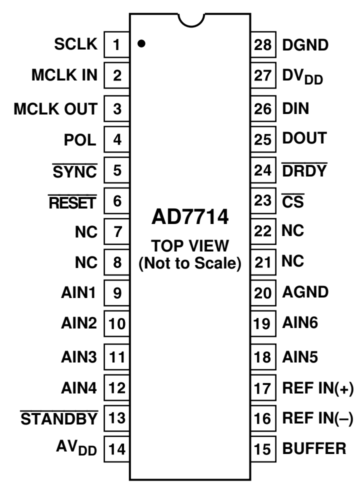
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

DIP and SOIC/TSSOP



SSOP



NC = NO CONNECT

PIN FUNCTION DESCRIPTION

DIP/SOIC PIN NUMBERS

Pin No.	Mnemonic	Function
1	SCLK	Serial Clock. Logic Input. An external serial clock is applied to this input to access serial data from the AD7714. This serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7714 in smaller batches of data.
2	MCLK IN	Master Clock signal for the device. This can be provided in the form of a crystal/resonator or external clock. A crystal/resonator can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The part is specified with clock input frequencies of both 1 MHz and 2.4576 MHz.
3	MCLK OUT	When the master clock for the device is a crystal/resonator, the crystal/resonator is connected between MCLK IN and MCLK OUT. If an external clock is applied to the MCLK IN, MCLK OUT provides an inverted clock signal. This clock can be used to provide a clock source for external circuits.
4	POL	Clock Polarity. Logic Input. With this input low, the first transition of the serial clock in a data transfer operation is from a low to a high. In microcontroller applications, this means that the serial clock should idle low between data transfers. With this input high, the first transition of the serial clock in a data transfer operation is from a high to a low. In microcontroller applications, this means that the serial clock should idle high between data transfers.
5	$\overline{\text{SYNC}}$	Logic Input which allows for synchronization of the digital filters and analog modulators when using a number of AD7714s. While $\overline{\text{SYNC}}$ is low, the nodes of the digital filter, the filter control logic and the calibration control logic are reset and the analog modulator is also held in its reset state. $\overline{\text{SYNC}}$ does not affect the digital interface and does not reset $\overline{\text{DRDY}}$ if it is low.
6	$\overline{\text{RESET}}$	Logic Input. Active low input which resets the control logic, interface logic, digital filter and analog modulator of the part to power-on status.
7	AIN1	Analog Input Channel 1. Programmable-gain analog input which can be used as a pseudo-differential input when used with AIN6 or as the positive input of a differential analog input pair when used with AIN2 (see Communications Register section).
8	AIN2	Analog Input Channel 2. Programmable-gain analog input which can be used as a pseudo-differential input when used with AIN6 or as the negative input of a differential analog input pair when used with AIN1 (see Communications Register section).
9	AIN3	Analog Input Channel 3. Programmable-gain analog input which can be used as a pseudo-differential input when used with AIN6 or as the positive input of a differential analog input pair when used with AIN4 (see Communications Register section).
10	AIN4	Analog Input Channel 4. Programmable-gain analog input which can be used as a pseudo-differential input when used with AIN6 or as the negative input of a differential analog input pair when used with AIN3 (see Communications Register section).
11	$\overline{\text{STANDBY}}$	Logic Input. Taking this pin low shuts down the analog and digital circuitry, reducing current consumption to typically 5 µA.
12	AV_{DD}	Analog Positive Supply Voltage, A Grade Versions: +3.3 V nominal (AD7714-3) or +5 V nominal (AD7714-5); Y Grade Versions: 3 V or 5 V nominal.
13	BUFFER	Buffer Option Select. Logic Input. With this input low, the on-chip buffer on the analog input (after the multiplexer and before the analog modulator) is shorted out. With the buffer shorted out the current flowing in the AV_{DD} line is reduced to 270 µA. With this input high, the on-chip buffer is in series with the analog input allowing the inputs to handle higher source impedances.
14	REF IN(–)	Reference Input. Negative input of the differential reference input to the AD7714. The REF IN(–) can lie anywhere between AV_{DD} and AGND provided REF IN(+) is greater than REF IN(–).
15	REF IN(+)	Reference Input. Positive input of the differential reference input to the AD7714. The reference input is differential with the provision that REF IN(+) must be greater than REF IN(–). REF IN(+) can lie anywhere between AV_{DD} and AGND.
16	AIN5	Analog Input Channel 5. Programmable-gain analog input which is the positive input of a differential analog input pair when used with AIN6 (see Communications Register section).
17	AIN6	Analog Input Channel 6. Reference point for AIN1 through AIN4 in pseudo-differential mode or as the negative input of a differential input pair when used with AIN5 (see Communications Register section).
18	AGND	Ground reference point for analog circuitry.

PIN FUNCTION DESCRIPTION (Continued)

Pin No.	Mnemonic	Function
19	$\overline{CS}$	Chip Select. Active low Logic Input used to select the AD7714. With this input hard-wired low, the AD7714 can operate in its three-wire interface mode with SCLK, DIN and DOUT used to interface to the device. $\overline{CS}$ can be used to select the device in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the AD7714.
20	$\overline{DRDY}$	Logic output. A logic low on this output indicates that a new output word is available from the AD7714 data register. The $\overline{DRDY}$ pin will return high upon completion of a read operation of a full output word. If no data read has taken place, after an output update, the $\overline{DRDY}$ line will return high for $500 \times t_{CLK\ IN}$ cycles prior to the next output update. This gives an indication of when a read operation should not be attempted to avoid reading from the data register as it is being updated. $\overline{DRDY}$ is also used to indicate when the AD7714 has completed its on-chip calibration sequence.
21	DOUT	Serial Data Output with serial data being read from the output shift register on the part. This output shift register can contain information from the calibration registers, mode register, communications register, filter selection registers or data register depending on the register selection bits of the Communications Register.
22	DIN	Serial Data Input with serial data being written to the input shift register on the part. Data from this input shift register is transferred to the calibration registers, mode register, communications register or filter selection registers depending on the register selection bits of the Communications Register.
23	DV_{DD}	Digital Supply Voltage, A Grade Versions: +3.3 V or +5 V nominal; Y Grade Versions: 3 V or 5 V nominal.
24	DGND	Ground reference point for digital circuitry.

TERMINOLOGY*

INTEGRAL NONLINEARITY

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

POSITIVE FULL-SCALE ERROR

Positive Full-Scale Error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal AIN(+) voltage (AIN(–) + V_{REF}/GAIN – 3/2 LSBs). It applies to both unipolar and bipolar analog input ranges.

UNIPOLAR OFFSET ERROR

Unipolar Offset Error is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(–) + 0.5 LSB) when operating in the unipolar mode.

BIPOLAR ZERO ERROR

This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal AIN(+) voltage (AIN(–) – 0.5 LSB) when operating in the bipolar mode.

GAIN ERROR

This is a measure of the span error of the ADC. It includes full-scale errors but not zero-scale errors. For unipolar input ranges it is defined as (full-scale error – unipolar offset error) while for bipolar input ranges it is defined as (full-scale error – bipolar zero error).

*AIN(–) refers to the negative input of the differential input pairs or to AIN6 when referring to the pseudo-differential input configurations.

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(–) – V_{REF}/GAIN + 0.5 LSB) when operating in the bipolar mode.

POSITIVE FULL-SCALE OVERRANGE

Positive Full-Scale Overrange is the amount of overhead available to handle input voltages on AIN(+) input greater than AIN(–) + V_{REF}/GAIN (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages on AIN(+) below AIN(–) – V_{REF}/GAIN without overloading the analog modulator or overflowing the digital filter. Note that the analog input will accept negative voltage peaks even in the unipolar mode provided that AIN(+) is greater than AIN(–) and greater than AGND – 30 mV.

OFFSET CALIBRATION RANGE

In the system calibration modes, the AD7714 calibrates its offset with respect to the analog input. The Offset Calibration Range specification defines the range of voltages that the AD7714 can accept and still calibrate offset accurately.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7714 can accept in the system calibration mode and still calibrate full scale correctly.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7714's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full scale that the AD7714 can accept and still calibrate gain accurately.

AD7714-5 OUTPUT NOISE

Table Ia shows the output rms noise and effective resolution for some typical notch and –3 dB frequencies for the AD7714-5 with $f_{CLK\ IN}$ = 2.4576 MHz while Table Ib gives the information for $f_{CLK\ IN}$ = 1 MHz. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5 V and with BUFFER = 0. These numbers are typical and are generated at an analog input voltage of 0 V. The numbers in brackets in each table are for the effective resolution of the part (rounded to the nearest 0.5 LSB). The effective resolution of the device is defined as the ratio of the output rms noise to the input full scale (i.e., $2 \times V_{REF}/GAIN$). It should be noted that it is not calculated using peak-to-peak output noise numbers. Peak-to-peak noise numbers can be up to 6.6 times the rms numbers while effective resolution numbers based on peak-to-peak noise can be 2.5 bits below the effective resolution based on rms noise as quoted in the tables.

The output noise from the part comes from two sources. The first is the electrical noise in the semiconductor devices used in the implementation of the modulator (device noise). Secondly, when the analog input signal is converted into the digital domain, quantization noise is added. The device noise is at a low level and is largely independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. Consequently, lower filter notch settings (below 100 Hz approximately for $f_{CLK\ IN}$ = 2.4576 MHz and below 40 Hz approximately for $f_{CLK\ IN}$ = 1 MHz) tend to be device noise dominated while higher notch settings are dominated by quantization noise. Changing the filter notch and cutoff frequency in the quantization-noise dominated region results in a more dramatic improvement in noise performance than it does in the device-noise dominated region as shown in Table I. Furthermore, quantization noise is added after the PGA, so effective resolution is largely independent of gain for the higher filter notch frequencies. Meanwhile, device noise is added in the PGA and, therefore, effective resolution reduces at high gains for lower notch frequencies. Additionally, in the device-noise dominated region, the output noise (in μV) is largely independent of reference voltage while in the quantization-noise dominated region, the noise is proportional to the value of the reference. It is possible to do post-filtering on the device to improve the output data rate for a given –3 dB frequency and also to further reduce the output noise.

At the lower filter notch settings (below 60 Hz for $f_{CLK\ IN}$ = 2.4576 MHz and below 25 Hz for $f_{CLK\ IN}$ = 1 MHz), the no missing codes performance of the device is at the 24-bit level. At the higher settings, more codes will be missed until at 1 kHz notch setting for $f_{CLK\ IN}$ = 2.4576 MHz (400 Hz for $f_{CLK\ IN}$ = 1 MHz), no missing codes performance is only guaranteed to the 12-bit level.

Table Ia. AD7714-5 Output Noise/Resolution vs. Gain and First Notch for $f_{CLK\ IN}$ = 2.4576 MHz, BUFFER = 0

Filter First Notch & O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in μV (Effective Resolution in Bits)															
		Gain of 1		Gain of 2		Gain of 4		Gain of 8		Gain of 16		Gain of 32		Gain of 64		Gain of 128	
5 Hz	1.31 Hz	0.87	(22.5)	0.48	(22.5)	0.24	(22.5)	0.2	(21.5)	0.18	(20.5)	0.17	(20)	0.17	(19)	0.17	(18)
10 Hz	2.62 Hz	1.0	(22.5)	0.78	(21.5)	0.48	(21.5)	0.33	(21)	0.25	(20.5)	0.25	(19.5)	0.25	(18.5)	0.25	(17.5)
25 Hz	6.55 Hz	1.8	(21.5)	1.1	(21)	0.63	(21)	0.5	(20)	0.44	(19.5)	0.41	(18.5)	0.38	(17.5)	0.38	(16.5)
30 Hz	7.86 Hz	2.5	(21)	1.31	(21)	0.84	(20.5)	0.57	(20)	0.46	(19.5)	0.43	(18.5)	0.4	(17.5)	0.4	(16.5)
50 Hz	13.1 Hz	4.33	(20)	2.06	(20)	1.2	(20)	0.64	(20)	0.54	(19)	0.46	(18.5)	0.46	(17.5)	0.46	(16.5)
60 Hz	15.72 Hz	5.28	(20)	2.36	(20)	1.33	(20)	0.87	(19.5)	0.63	(19)	0.62	(18)	0.6	(17)	0.56	(16)
100 Hz	26.2 Hz	12.1	(18.5)	5.9	(18.5)	2.86	(19)	1.91	(18.5)	1.06	(18)	0.83	(17.5)	0.82	(16.5)	0.76	(15.5)
250 Hz	65.5 Hz	127	(15.5)	58	(15.5)	29	(15.5)	15.9	(15.5)	6.7	(15.5)	3.72	(15.5)	1.96	(15.5)	1.5	(14.5)
500 Hz	131 Hz	533	(13)	267	(13)	137	(13)	66	(13)	38	(13)	20	(13)	8.6	(13)	4.4	(13)
1 kHz	262 Hz	2,850	(11)	1,258	(11)	680	(11)	297	(11)	131	(11)	99	(10.5)	53	(10.5)	28	(10.5)

Table Ib. AD7714-5 Output Noise/Resolution vs. Gain and First Notch for $f_{CLK\ IN}$ = 1 MHz, BUFFER = 0

Filter First Notch & O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in μV (Effective Resolution in Bits)															
		Gain of 1		Gain of 2		Gain of 4		Gain of 8		Gain of 16		Gain of 32		Gain of 64		Gain of 128	
2 Hz	0.52 Hz	0.75	(22.5)	0.56	(22)	0.31	(22)	0.19	(21.5)	0.17	(21)	0.14	(20)	0.14	(19)	0.14	(18)
4 Hz	1.05 Hz	1.04	(22)	0.88	(21.5)	0.45	(21.5)	0.28	(21)	0.21	(20.5)	0.21	(19.5)	0.21	(18.5)	0.21	(17.5)
10 Hz	2.62 Hz	1.66	(21.5)	1.01	(21.5)	0.77	(20.5)	0.41	(20.5)	0.37	(19.5)	0.35	(19)	0.35	(18)	0.35	(17)
25 Hz	6.55 Hz	5.2	(20)	2.06	(20)	1.4	(20)	0.86	(19.5)	0.63	(19)	0.61	(18)	0.59	(17)	0.59	(16)
30 Hz	7.86 Hz	7.1	(19.5)	3.28	(19.5)	1.42	(19.5)	1.07	(19)	0.78	(18.5)	0.64	(18)	0.61	(17)	0.61	(16)
50 Hz	13.1 Hz	19.4	(18)	9.11	(18)	4.2	(18)	2.45	(18)	1.56	(17.5)	1.1	(17)	0.82	(16.5)	0.8	(15.5)
60 Hz	15.72 Hz	25	(17.5)	16	(17.5)	6.5	(17.5)	2.9	(17.5)	1.93	(17.5)	1.4	(17)	1.1	(16)	0.98	(15.5)
100 Hz	26.2 Hz	102	(15.5)	58	(15.5)	25	(15.5)	13.5	(15.5)	5.7	(15.5)	3.9	(15.5)	2.1	(15)	1.3	(15)
200 Hz	52.4 Hz	637	(13)	259	(13)	130	(13)	76	(13)	33	(13)	16	(13)	11	(13)	6	(12.5)
400 Hz	104.8 Hz	2,830	(11)	1,430	(11)	720	(11)	334	(11)	220	(10.5)	94	(10.5)	54	(10.5)	25	(10.5)

AD7714-3 OUTPUT NOISE

Table IIa shows the output rms noise and effective resolution for some typical notch and –3 dB frequencies for the AD7714-3 with $f_{CLK\ IN}$ = 2.4576 MHz while Table IIb gives the information for $f_{CLK\ IN}$ = 1 MHz. The numbers given are for the bipolar input ranges with a V_{REF} of +1.25 V and BUFFER = 0. These numbers are typical and are generated at an analog input voltage of 0 V. The numbers in brackets in each table are for the effective resolution of the part (rounded to the nearest 0.5 LSB). The effective resolution of the device is defined as the ratio of the output rms noise to the input full scale (i.e., $2 \times V_{REF}/GAIN$). It should be noted that it is not calculated using peak-to-peak output noise numbers. Peak-to-peak noise numbers can be up to 6.6 times the rms numbers while effective resolution numbers based on peak-to-peak noise can be 2.5 bits below the effective resolution based on rms noise as quoted in the tables.

The output noise from the part comes from two sources. The first is the electrical noise in the semiconductor devices used in the implementation of the modulator (device noise). Secondly, when the analog input signal is converted into the digital domain, quantization noise is added. The device noise is at a low level and is largely independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. Consequently, lower filter notch settings (below 100 Hz approximately for $f_{CLK\ IN}$ = 2.4576 MHz and below 40 Hz approximately for $f_{CLK\ IN}$ = 1 MHz) tend to be device noise dominated while higher notch settings are dominated by quantization noise. Changing the filter notch and cutoff frequency in the quantization noise dominated region results in a more dramatic improvement in noise performance than it does in the device-noise dominated region as shown in Table II. Furthermore, quantization noise is added after the PGA, so effective resolution is largely independent of gain for the higher filter notch frequencies. Meanwhile, device noise is added in the PGA and, therefore, effective resolution suffers a little at high gains for lower notch frequencies. Additionally, in the device-noise dominated region, the output noise (in µV) is largely independent of reference voltage while in the quantization-noise dominated region, the noise is proportional to the value of the reference. It is possible to do post-filtering on the device to improve the output data rate for a given –3 dB frequency and also to further reduce the output noise.

At the lower filter notch settings (below 60 Hz for $f_{CLK\ IN}$ = 2.4576 MHz and below 25 Hz for $f_{CLK\ IN}$ = 1 MHz), the no missing codes performance of the device is at the 24-bit level. At the higher settings, more codes will be missed until at 1 kHz notch setting for $f_{CLK\ IN}$ = 2.4576 MHz (400 Hz for $f_{CLK\ IN}$ = 1 MHz), no missing codes performance is only guaranteed to the 12-bit level.

Table IIa. AD7714-3 Output Noise/Resolution vs. Gain and First Notch for $f_{CLK\ IN}$ = 2.4576 MHz, BUFFER = 0

Filter First Notch & O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in µV (Effective Resolution in Bits)															
		Gain of 1		Gain of 2		Gain of 4		Gain of 8		Gain of 16		Gain of 32		Gain of 64		Gain of 128	
5 Hz	1.31 Hz	1.07	(21)	0.68	(21)	0.29	(21)	0.24	(20)	0.22	(19.5)	0.22	(18.5)	0.22	(17.5)	0.22	(16.5)
10 Hz	2.62 Hz	1.69	(20.5)	1.1	(20)	0.56	(20)	0.35	(19.5)	0.33	(19)	0.33	(18)	0.33	(17)	0.33	(16)
25 Hz	6.55 Hz	3.03	(19.5)	1.7	(19.5)	0.89	(19.5)	0.55	(19)	0.49	(18.5)	0.46	(17.5)	0.46	(16.5)	0.45	(15.5)
30 Hz	7.86 Hz	3.55	(19.5)	2.1	(19)	1.1	(19)	0.61	(18.5)	0.58	(18)	0.57	(17)	0.55	(16)	0.55	(15)
50 Hz	13.1 Hz	4.72	(19)	2.3	(19)	1.5	(18.5)	0.84	(18.5)	0.7	(18)	0.68	(17)	0.67	(16)	0.66	(15)
60 Hz	15.72 Hz	5.12	(19)	3.1	(18.5)	1.6	(18)	0.98	(18)	0.9	(17.5)	0.7	(17)	0.69	(16)	0.68	(15)
100 Hz	26.2 Hz	9.68	(18)	5.6	(18)	2.4	(18)	1.3	(18)	1.1	(17)	0.95	(16.5)	0.88	(15.5)	0.9	(14.5)
250 Hz	65.5 Hz	44	(16)	31	(15.5)	15	(15.5)	5.8	(15.5)	3.7	(15.5)	2.4	(15)	1.8	(14.5)	1.8	(13.5)
500 Hz	131 Hz	304	(13)	129	(13)	76	(13)	33	(13)	20	(13)	11	(13)	6.3	(12.5)	3	(12.5)
1 kHz	262 Hz	1410	(11)	715	(11)	350	(11)	177	(11)	101	(10.5)	51	(10.5)	31	(10.5)	12	(10.5)

Table IIb. AD7714-3 Output Noise/Resolution vs. Gain and First Notch for $f_{CLK\ IN}$ = 1 MHz, BUFFER = 0

Filter First Notch & O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in µV (Effective Resolution in Bits)															
		Gain of 1		Gain of 2		Gain of 4		Gain of 8		Gain of 16		Gain of 32		Gain of 64		Gain of 128	
2 Hz	0.52 Hz	0.86	(21.5)	0.58	(21)	0.32	(21)	0.21	(20.5)	0.2	(19.5)	0.2	(18.5)	0.2	(17.5)	0.2	(16.5)
4 Hz	1.05 Hz	1.26	(21)	0.74	(20.5)	0.44	(20.5)	0.35	(20)	0.3	(19)	0.3	(18)	0.3	(17)	0.3	(16)
10 Hz	2.62 Hz	1.68	(20.5)	1.33	(20)	0.73	(20)	0.5	(19)	0.49	(18.5)	0.49	(17.5)	0.48	(16.5)	0.47	(15.5)
25 Hz	6.55 Hz	3.82	(19.5)	2.0	(19.5)	1.2	(19)	0.88	(18.5)	0.66	(18)	0.57	(17)	0.55	(16)	0.55	(15)
30 Hz	7.86 Hz	4.88	(19)	2.1	(19)	1.3	(19)	0.93	(18.5)	0.82	(17.5)	0.69	(17)	0.68	(16)	0.66	(15)
50 Hz	13.1 Hz	11	(18)	4.8	(18)	2.4	(18)	1.4	(18)	1.4	(17)	0.73	(16.5)	0.71	(15.5)	0.7	(15)
60 Hz	15.72 Hz	14.7	(17.5)	7.5	(17.5)	3.8	(17.5)	2.6	(17)	1.5	(16.5)	0.95	(16.5)	0.88	(15)	0.9	(14.5)
100 Hz	26.2 Hz	61	(15.5)	30	(15.5)	12	(15.5)	6.1	(15.5)	2.9	(15.5)	2.4	(15)	1.8	(14.5)	1.8	(13.5)
200 Hz	52.4 Hz	275	(13)	130	(13)	65	(13)	33	(13)	17	(13)	11	(13)	6.3	(12.5)	3	(12.5)
400 Hz	104.8 Hz	1435	(11)	720	(11)	362	(11)	175	(11)	110	(10.5)	51	(10.5)	31	(10.5)	12	(10.5)

BUFFERED MODE NOISE

Table III shows the typical output rms noise and effective resolution for some typical notch and –3 dB frequencies for the AD7714-5 with $f_{CLK\ IN}$ = 2.4576 MHz and BUFFER = +5 V. Table IV gives the information for the AD7714-3 again with $f_{CLK\ IN}$ = 2.4576 MHz and BUFFER = +5 V. The numbers given are for the bipolar input ranges and are generated with a differential analog input voltage of 0 V. For the AD7714-5, the V_{REF} voltage is +2.5 V while for the AD7714 the V_{REF} voltage is +1.25 V. The numbers in brackets in each table are for the effective resolution of the part (rounded to the nearest 0.5 LSB). The effective resolution of the device is defined as the ratio of the output rms noise to the input full scale (i.e., $2 \times V_{REF}/GAIN$). It should be noted that it is not calculated using peak-to-peak output noise numbers. Peak-to-peak noise numbers can be up to 6.6 times the rms numbers while effective resolution numbers based on peak-to-peak noise can be 2.5 bits below the effective resolution based on rms noise as quoted in the tables.

Table III. AD7714-5 Buffered Mode Output Noise/Resolution for $f_{CLK\ IN}$ = 2.4576 MHz

Filter First Notch & O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in μV (Effective Resolution in Bits)															
		Gain of 1		Gain of 2		Gain of 4		Gain of 8		Gain of 16		Gain of 32		Gain of 64		Gain of 128	
5 Hz	1.31 Hz	0.99	(22.5)	0.68	(22)	0.46	(21.5)	0.26	(21)	0.26	(20)	0.26	(19)	0.26	(18)	0.26	(17)
10 Hz	2.62 Hz	1.5	(21.5)	0.95	(21.5)	0.63	(21)	0.41	(20.5)	0.39	(19.5)	0.36	(18.5)	0.36	(17.5)	0.36	(16.5)
25 Hz	6.55 Hz	2.5	(21)	1.7	(20.5)	0.88	(20.5)	0.75	(19.5)	0.57	(19)	0.57	(18)	0.57	(17)	0.56	(16)
30 Hz	7.86 Hz	2.9	(20.5)	1.8	(20.5)	1	(20)	0.87	(19.5)	0.75	(18.5)	0.72	(17.5)	0.72	(16.5)	0.71	(15.5)
50 Hz	13.1 Hz	4.2	(20)	2.5	(20)	1.5	(19.5)	1.1	(19)	0.94	(18.5)	0.94	(17.5)	0.94	(16.5)	0.87	(15.5)
60 Hz	15.72 Hz	6.1	(19.5)	2.9	(19.5)	2	(19.5)	1.2	(19)	1	(18.5)	0.97	(17.5)	0.95	(16.5)	0.94	(15.5)
100 Hz	26.2 Hz	13.8	(18.5)	6.5	(18.5)	3.5	(18.5)	2.2	(18)	1.3	(18)	1.2	(17)	1.3	(16)	1.1	(15)
250 Hz	65.5 Hz	87	(16)	56	(15.5)	25	(15.5)	11	(15.5)	5.7	(15.5)	3.6	(15.5)	2.4	(15)	2.1	(14)
500 Hz	131 Hz	508	(13.5)	241	(13.5)	117	(13.5)	73	(13)	34	(13)	16	(13)	8.5	(13)	5.2	(13)
1 kHz	262 Hz	2860	(11)	1700	(10.5)	745	(10.5)	480	(10.5)	197	(10.5)	94	(10.5)	53	(10.5)	23	(10.5)

Table IV. AD7714-3 Buffered Mode Output Noise/Resolution for $f_{CLK\ IN}$ = 2.4576 MHz

Filter First Notch & O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in μV (Effective Resolution in Bits)															
		Gain of 1		Gain of 2		Gain of 4		Gain of 8		Gain of 16		Gain of 32		Gain of 64		Gain of 128	
5 Hz	1.31 Hz	1.16	(21)	0.76	(20.5)	0.34	(20)	0.29	(20)	0.29	(19)	0.28	(18)	0.26	(17)	0.26	(16)
10 Hz	2.62 Hz	1.7	(20.5)	1	(20.5)	0.7	(20)	0.46	(19.5)	0.45	(18.5)	0.4	(17.5)	0.4	(16.5)	0.4	(15.5)
25 Hz	6.55 Hz	3.5	(19.5)	1.8	(19.5)	1.1	(19)	0.74	(18.5)	0.63	(18)	0.6	(17)	0.6	(16)	0.6	(15)
30 Hz	7.86 Hz	3.7	(19.5)	2.2	(19)	1.3	(19)	0.76	(18.5)	0.68	(18)	0.66	(17)	0.66	(16)	0.66	(15)
50 Hz	13.1 Hz	4.5	(19)	3	(18.5)	1.7	(18.5)	1.0	(18)	0.92	(17.5)	0.9	(16.5)	0.89	(15.5)	0.89	(14.5)
60 Hz	15.72 Hz	5.3	(19)	3.3	(18.5)	1.8	(18.5)	1.1	(18)	1	(17)	0.96	(16.5)	0.96	(15.5)	0.96	(14.5)
100 Hz	26.2 Hz	10	(18)	4.9	(18)	3.1	(17.5)	1.5	(17.5)	1.2	(17)	1.2	(16)	1.2	(15)	1.2	(14)
250 Hz	65.5 Hz	47	(15.5)	29	(15.5)	15	(15.5)	7.5	(15.5)	4.7	(15)	2.6	(15)	2.5	(14)	1.6	(13.5)
500 Hz	131 Hz	300	(13.5)	171	(13)	74	(13)	35	(13)	21	(13)	8.6	(13)	5.6	(13)	3.1	(12.5)
1 kHz	262 Hz	1722	(10.5)	735	(10.5)	380	(10.5)	230	(10.5)	93	(10.5)	55	(10.5)	30	(10.5)	12	(10.5)

ON-CHIP REGISTERS

The AD7714 contains eight on-chip registers which can be accessed via the serial port of the part. The first of these is a Communications Register which controls the channel selection, decides whether the next operation is a read or write operation and also decides which register the next read or write operation accesses. All communications to the part must start with a write operation to the Communications Register. After power-on or $\overline{\text{RESET}}$, the device expects a write to its Communications Register. The data written to this register determines whether the next operation to the part is a read or a write operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part starts with a write operation to the Communications Register followed by a write to the selected register. A read operation from any other register on the part (including the output data register) starts with a write operation to the Communications Register followed by a read operation from the selected register. The communications register also controls channel selection and the $\overline{\text{DRDY}}$ status is also available by reading from the Communications Register. The second register is a Mode Register which determines calibration mode and gain setting. The third register is labelled the Filter High Register and this determines the word length, bipolar/unipolar operation and contains the upper 4 bits of the filter selection word. The fourth register is labelled the Filter Low Register and contains the lower 8 bits of the filter selection word. The fifth register is a Test Register which is accessed when testing the device. The sixth register is the Data Register from which the output data from the part is accessed. The final registers allow access to the part's calibration registers. The Zero Scale Calibration Register allows access to the zero scale calibration coefficients for the selected input channel while the Full Scale Calibration Register allows access to the full scale calibration coefficients for the selected input channel. The registers are discussed in more detail in the following sections.

Communications Register (RS2-RS0 = 0, 0, 0)

The Communications Register is an 8-bit register from which data can either be read or to which data can be written. All communications to the part must start with a write operation to the Communications Register. The data written to the Communications Register determines whether the next operation is a read or write operation and to which register this operation takes place. Once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the Communications Register. This is the default state of the interface, and on power-up or after a $\overline{\text{RESET}}$, the AD7714 is in this default state waiting for a write operation to the Communications Register. In situations where the interface sequence is lost, if a write operation of sufficient duration (containing at least 32 serial clock cycles) takes place with DIN high, the AD7714 returns to this default state. Table V outlines the bit designations for the Communications Register.

Table V. Communications Register

0/$\overline{\text{DRDY}}$	RS2	RS1	RS0	R/$\overline{\text{W}}$	CH2	CH1	CH0

0/$\overline{\text{DRDY}}$ For a write operation, a 0 must be written to this bit so that the write operation to the Communications Register actually takes place. If a 1 is written to this bit, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a 0 is written to this bit. Once a 0 is written to this bit, the next 7 bits will be loaded to the Communications Register. For a read operation, this bit provides the status of the $\overline{\text{DRDY}}$ flag from the part. The status of this bit is the same as the $\overline{\text{DRDY}}$ output pin.

RS2–RS0 Register Selection Bits. RS2 is the MSB of the three selection bits. The three bits select to which one of eight on-chip registers the next read or write operation takes place as shown in Table VI along with the register size.

Table VI. Register Selection

RS2	RS1	RS0	Register	Register Size
0	0	0	Communications Register	8 Bits
0	0	1	Mode Register	8 Bits
0	1	0	Filter High Register	8 Bits
0	1	1	Filter Low Register	8 Bits
1	0	0	Test Register	8 Bits
1	0	1	Data Register	16 Bits or 24 Bits
1	1	0	Zero-Scale Calibration Register	24 Bits
1	1	1	Full-Scale Calibration Register	24 Bits

CH2–CH0 Channel Select. These three bits select a channel either for conversion or for access to calibration coefficients as outlined in Table VII. There are three pairs of calibration registers on the part. In fully differential mode, the part has three input channels so each channel has its own pair of calibration registers. In pseudo-differential mode, the AD7714 has five input channels with some of the input channel combinations sharing calibration registers. With CH2, CH1 and CH0 at a logic 1, the part looks at the AIN6 input internally shorted to itself. This can be used as a test method to evaluate the noise performance of the part with no external noise sources. In this mode, the AIN6 input should be connected to an external voltage within the allowable common-mode range for the part. The Power-On or RESET status of these bits is 1,0,0 selecting the differential pair AIN1 and AIN2.

Table VII. Channel Selection

CH2	CH1	CH0	AIN(+)	AIN(–)	Type	Calibration Register Pair
0	0	0	AIN1	AIN6	Pseudo Differential	Register Pair 0
0	0	1	AIN2	AIN6	Pseudo Differential	Register Pair 1
0	1	0	AIN3	AIN6	Pseudo Differential	Register Pair 2
0	1	1	AIN4	AIN6	Pseudo Differential	Register Pair 2
1	0	0	AIN1	AIN2	Fully Differential	Register Pair 0
1	0	1	AIN3	AIN4	Fully Differential	Register Pair 1
1	1	0	AIN5	AIN6	Fully Differential	Register Pair 2
1	1	1	AIN6	AIN6	Test Mode	Register Pair 2

Mode Register (RS2-RS0 = 0, 0, 1); Power On/Reset Status: 00 Hex

The Mode Register is an eight bit register from which data can either be read or to which data can be written. Table VIII outlines the bit designations for the Mode Register.

Table VIII. Mode Register

MD2	MD1	MD0	G2	G1	G0	BO	FSYNC

MD2	MD1	MD0	Operating Mode
0	0	0	Normal Mode; this is the normal mode of operation of the device whereby the device is performing normal conversions. This is the default condition of these bits after Power-On or $\overline{\text{RESET}}$.
0	0	1	Self-Calibration; this activates self-calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. This is a one step calibration sequence and when complete the part returns to Normal Mode with MD2, MD1 and MD0 returning to 0, 0, 0. The $\overline{\text{DRDY}}$ output or bit goes high when calibration is initiated and returns low when this self-calibration is complete and a new valid word is available in the data register. The zero-scale calibration is performed at the selected gain on internally shorted (zeroed) inputs and the full-scale calibration is performed at the selected gain on an internally-generated V_{REF}/Selected Gain.
0	1	0	Zero-Scale System Calibration; this activates zero scale system calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. Calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. The $\overline{\text{DRDY}}$ output or bit goes high when calibration is initiated and returns low when this zero-scale calibration is complete and a new valid word is available in the data register. At the end of the calibration, the part returns to Normal Mode with MD2, MD1 and MD0 returning to 0, 0, 0.
0	1	1	Full-Scale System Calibration; this activates full-scale system calibration on the selected input channel. Calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. Once again, the $\overline{\text{DRDY}}$ output or bit goes high when calibration is initiated and returns low when this full-scale calibration is complete and a new valid word is available in the data register. At the end of the calibration, the part returns to Normal Mode with MD2, MD1 and MD0 returning to 0, 0, 0.

MD2	MD1	MD0	Operating Mode (continued)
1	0	0	System-Offset Calibration; this activates system-offset calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. This is a one step calibration sequence and when complete the part returns to Normal Mode with MD2, MD1 and MD0 returning to 0, 0, 0. The $\overline{DRDY}$ output or bit goes high when calibration is initiated and returns low when this system offset calibration is complete and a new valid word is available in the data register. For this calibration type, the zero-scale calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. The full-scale calibration is performed at the selected gain on an internally generated V_{REF}/Selected Gain.
1	0	1	Background Calibration; this activates background calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. If the background calibration mode is on, then the AD7714 provides continuous self-calibration of the shorted (zeroed) inputs. This calibration takes place as part of the conversion sequence, extending the conversion time and reducing the word rate by a factor of six. Its major advantage is that the user does not have to worry about recalibrating the offset of the device when there is a change in the ambient temperature or supplies. In this mode, the zero-scale calibration is performed at the selected gain on internally shorted (zeroed) inputs. The calibrations are interleaved with normal conversions and the calibration registers of the device are automatically updated. Because the background calibration does not perform full-scale calibrations, a self-calibration should be performed before placing the part in the background calibration mode.
1	1	0	Zero-Scale Self-Calibration; this activates zero-scale self-calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. This zero-scale self-calibration is performed at the selected gain on internally shorted (zeroed) inputs. This is a one step calibration sequence and when complete the part returns to Normal Mode with MD2, MD1 and MD0 returning to 0, 0, 0. The $\overline{DRDY}$ output or bit goes high when calibration is initiated and returns low when this zero-scale self-calibration is complete and a new valid word is available in the data register.
1	1	1	Full-Scale Self-Calibration; this activates full-scale self-calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. This full-scale self-calibration is performed at the selected gain on an internally-generated V_{REF}/Selected Gain. This is a one step calibration sequence and when complete the part returns to Normal Mode with MD2, MD1 and MD0 returning to 0, 0, 0. The $\overline{DRDY}$ output or bit goes high when calibration is initiated and returns low when this full-scale self-calibration is complete and a new valid word is available in the data register.

G2	G1	G0	Gain Setting
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

BO			Burnout Current. A 0 in this bit turns off the on-chip burnout currents. This is the default (Power-On or RESET) status of this bit. A 1 in this bit activates the burnout currents. When active, the burnout currents connect to the selected analog input pair, one to the AIN(+) input and one to the AIN(–) input.
FSYNC			Filter Synchronization. When this bit is high, the nodes of the digital filter, the filter control logic and the calibration control logic are held in a reset state and the analog modulator is also held in its reset state. When this bit goes low, the modulator and filter start to process data and a valid word is available in 3 × 1/(output update rate), i.e., the settling time of the filter. This FSYNC bit does not affect the digital interface and does not reset the $\overline{DRDY}$ output if it is low.

Filter Registers. Power On/Reset Status: Filter High Register: 01 Hex. Filter Low Register: 40 Hex.
There are two 8-bit Filter Registers on the AD7714 from which data can either be read or to which data can be written. Tables IX and X outline the bit designations for the Filter Registers.

Table IX. Filter High Register (RS2–RS0 = 0, 1, 0)

$\overline{B}$/U	WL	BST	ZERO	FS11	FS10	FS9	FS8	A Versions
$\overline{B}$/U	WL	BST	CLKDIS	FS11	FS10	FS9	FS8	Y Versions

Table X. Filter Low Register (RS2–RS0 = 0, 1, 1)

FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0	All Versions

$\overline{B}$/U	Bipolar/Unipolar Operation. A 0 in this bit selects Bipolar Operation. This is the default (Power-On or RESET) status of this bit. A 1 in this bit selects unipolar operation.
WL	Word Length. A 0 in this bit selects 16-bit word length when reading from the data register (i.e., $\overline{DRDY}$ returns high after 16 serial clock cycles in the read operation). This is the default (Power-On or RESET) status of this bit. A 1 in this bit selects 24-bit word length.
BST	Current Boost. A 0 in this bit reduces the current taken by the analog front end. When the part is operated with $f_{CLK\ IN}$ = 1 MHz or at gains of 1 to 4 with $f_{CLK\ IN}$ = 2.4576 MHz, this bit should be 0 to reduce the current drawn from AV_{DD}, although the device will operate just as well with this bit at a 1. When the AD7714 is operated at gains of 8 to 128 with $f_{CLK\ IN}$ = 2.4576 MHz, this bit **must be** 1 to ensure correct operation of the device. The Power-On or RESET status of this bit is 0.
ZERO	To ensure correct operation of the A Versions of the part, a 0 **must be** written to this bit.
CLKDIS	Master Clock Disable Bit. A Logic 1 in this bit disables the master clock from appearing at the MCLKOUT pin. When disabled, the MCLKOUT pin is forced low. This feature allows the user the flexibility of using the MCLKOUT as a clock source for other devices in the system or for turning off the MCLKOUT as a power saving feature. When using an external master clock or the MCLKIN pin, the AD7714 continues to have internal clocks and will convert normally with its CLKDIS bit active. When using a crystal oscillator or ceramic resonator across the MCLK IN or MCLKOUT pins, the AD7714 clock is stopped and no conversions take place when the CLKDIS bit is active.
FS11–FS0	Filter Selection. The on-chip digital filter provides a $Sinc^3$ (or $(Sinx/x)^3$) filter response. The 12 bits of data programmed into these bits determine the filter cut-off frequency, the position of the first notch of the filter and the data rate for the part. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device. The first notch of the filter occurs at a frequency determined by the relationship: filter first notch frequency = $(f_{CLK\ IN}/128)/code$ where *code* is the decimal equivalent of the code in bits FS0 to FS11 and is in the range 19 to 4,000. With the nominal $f_{CLK\ IN}$ of 2.4576 MHz, this results in a first notch frequency range from 4.8 Hz to 1.01 kHz. To ensure correct operation of the AD7714, the value of the code loaded to these bits must be within this range. Failure to do this will result in unspecified operation of the device. Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I through IV show the effect of the filter notch frequency and gain on the effective resolution of the AD7714. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz then a new word is available at a 50 Hz rate or every 20 ms. If the first notch is at 1 kHz, a new word is available every 1 ms. The settling time of the filter to a full-scale step input change is worst case 4 × 1/(output data rate). For example, with the first filter notch at 50 Hz, the settling time of the filter to a full-scale step input change is 80 ms max. This settling time can be reduced to 3 × 1/(output data rate) by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with the $\overline{SYNC}$ input low or the FSYNC bit high, the settling time will be 3 × 1/(output data rate) from when $\overline{SYNC}$ returns high or FSYNC returns low. If a change of channel takes place, the settling time is 3 × 1/(output data rate) regardless of the $\overline{SYNC}$ or FSYNC status as the part issues an internal $\overline{SYNC}$ command when requested to change channels. The –3 dB frequency is determined by the programmed first notch frequency according to the relationship: filter –3 dB frequency = 0.262 × filter first notch frequency.

Test Register (RS2–RS0 = 1, 0, 0)
The part contains a Test Register which is used in testing the device. The user is advised not to change the status of any of the bits in this register from the default (Power-On or RESET) status of all 0s as the part will be placed in one of its test modes and will not operate correctly. If the part enters one of its test modes, exercising $\overline{\text{RESET}}$ will exit the part from the mode. An alternative scheme for getting the part out of one of its test modes, is to reset the interface by writing 32 successive 1s to the part and then write all 0s to the Test Register.

Data Register (RS2–RS0 = 1, 0, 1)
The Data Register on the part is a read-only register which contains the most up-to-date conversion result from the AD7714. The register can be programmed to be either 16-bits or 24-bits wide, determined by the status of the WL bit of the Mode Register. If the Communications Register data sets up the part for a write operation to this register, a write operation must actually take place in order to return the part to where it is expecting a write operation to the Communications Register (the default state of the interface). However, the 16 or 24 bits of data written to the part will be ignored by the AD7714.

Zero-Scale Calibration Register (RS2–RS0 = 1, 1, 0); Power On/Reset Status: 1F4000 Hex
The AD7714 contains three zero-scale calibration registers, labelled Zero-Scale Calibration Register 0 to Zero Scale Calibration Register 2. The three registers are totally independent of each other such that in fully differential mode there is a zero-scale register for each of the input channels. Each of these registers is a 24-bit read/write register and, when writing to the registers, 24 bits must be written; otherwise no data will be transferred to the register. The register is used in conjunction with the associated full-scale calibration register to form a register pair. These register pairs are associated with input channel pairs as outlined in Table VII.

While the part is set up to allow access to these registers over the digital interface, the part itself no longer has access to the register coefficients to correctly scale the output data. As a result, there is a possibility that after accessing the calibration registers (either read or write operation) the first output data read from the part may contain incorrect data. In addition, a read or write operation to the calibration register should not be attempted while a calibration is in progress. These eventualities can be avoided by taking either the $\overline{\text{SYNC}}$ input low or the FSYNC bit of the Mode Register high before the calibration register operation and taking them either high or low respectively after the operation is complete.

Full-Scale Calibration Register (RS2–RS0 = 1, 1, 1); Power On/Reset Status: 5761AB Hex
The AD7714 contains three full-scale calibration registers, labelled Full-Scale Calibration Register 0 to Full-Scale Calibration Register 2. The three registers are totally independent of each other such that in fully differential mode there is a full-scale register for each of the input channels. Each of these registers is a 24-bit read/write register and, when writing to the registers, 24 bits must be written, otherwise no data will be transferred to the register. The register is used in conjunction with the associated zero-scale calibration register to form a register pair. These register pairs are associated with input channel pairs as outlined in Table VII.

While the part is set up to allow access to these registers over the digital interface, the part itself no longer has access to the coefficients to correctly scale the output data. As a result, there is a possibility that after accessing the calibration registers (either read or write operation) the first output data read from the part may contain incorrect data. In addition, a read or write operation to the calibration register should not be attempted while a calibration is in progress. These eventualities can be avoided by taking either the $\overline{\text{SYNC}}$ input low or the FSYNC bit of the Mode Register high before the calibration register operation and taking them either high or low respectively after the operation is complete.

CALIBRATION OPERATIONS

The AD7714 contains a number of calibration options as outlined previously. Table XI summarizes the calibration types, the operations involved and the duration of the operations. There are two methods of determining the end of calibration. The first is to monitor when $\overline{\text{DRDY}}$ returns low at the end of the sequence. $\overline{\text{DRDY}}$ not only indicates when the sequence is complete but also that the part has a valid new sample in its data register. This valid new sample is the result of a normal conversion which follows the calibration sequence. The second method of determining when calibration is complete is to monitor the MD2, MD1 and MD0 bits of the Mode Register. When these bits return to 0, 0, 0 following a calibration command, it indicates that the calibration sequence is complete. This method does not give any indication of there being a valid new result in the data register. However, it gives an earlier indication that calibration is complete than $\overline{\text{DRDY}}$. The time to when the Mode Bits (MD2, MD1 and MD0) return to 0, 0, 0 represents the duration of the calibration. The sequence to when $\overline{\text{DRDY}}$ goes low also includes a normal conversion and a pipeline delay, t_P ($2000 \times t_{CLK\ IN}$), to correctly scale the results of this first conversion. The time for both methods is given in the table.

Table XI. Calibration Operations

Calibration Type	MD2, MD1, MD0	Calibration Sequence	Duration to Mode Bits	Duration to $\overline{\text{DRDY}}$
Self Calibration	0, 0, 1	Internal ZS Cal @ Selected Gain + Internal FS Cal @ Selected Gain	6 × 1/Output Rate	9 × 1/Output Rate + t_P
ZS System Calibration	0, 1, 0	ZS Cal on AIN @ Selected Gain	3 × 1/Output Rate	4 × 1/Output Rate + t_P
FS System Calibration	0, 1, 1	FS Cal on AIN @ Selected Gain	3 × 1/Output Rate	4 × 1/Output Rate + t_P
System-Offset Calibration	1, 0, 0	ZS Cal on AIN @ Selected Gain + Internal FS Cal @ Selected Gain	6 × 1/Output Rate	9 × 1/Output Rate + t_P
Background Calibration	1, 0, 1	Internal ZS Cal @ Selected Gain + Normal Conversion	Bits Not Reset	6 × 1/Output Rate
ZS Self Calibration	1, 1, 0	Internal ZS Cal @ Selected Gain	3 × 1/Output Rate	6 × 1/Output Rate + t_P
FS Self Calibration	1, 1, 1	Internal FS Cal @ Selected Gain	3 × 1/Output Rate	6 × 1/Output Rate + t_P

CIRCUIT DESCRIPTION

The AD7714 is a sigma-delta A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in weigh-scale, pressure transducer, industrial control or process control applications. It contains a sigma-delta (or charge-balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter and a bidirectional serial communications port. The part consumes only 500 µA of power supply current and features a standby mode which requires only 10 µA, making it ideal for battery-powered or loop-powered instruments. The part comes in two versions, the AD7714-5, which is specified for operation from a nominal +5 V analog supply (AV_{DD}), and the AD7714-3, which is specified for operation from a nominal +3.3 V analog supply. Both versions can be operated with a digital supply (DV_{DD}) voltage of either +3.3 V or +5 V. AD7714Y grade parts operate with a nominal AV_{DD} of 3 V or 5 V and can be operated with a digital supply voltage of either 3 V or 5 V.

The part contains three programmable-gain fully differential analog input channels that can be reconfigured as five pseudo-differential inputs. The gain range on all channels is from 1 to 128, allowing the part to accept unipolar signals of between 0 mV to +20 mV and 0 V to +2.5 V. In bipolar mode, the part handles genuine bipolar signals of ±20 mV and quasi-bipolar signals up to ±2.5 V when the reference input voltage equals +2.5 V. With a reference voltage of +1.25 V, the input ranges are from 0 mV to +10 mV to 0 V to +1.25 V in unipolar mode, while in bipolar mode, the part handles genuine bipolar signals of ±10 mV and quasi-bipolar signals up to ±1.25 V.

The part employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The sigma-delta modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this sigma-delta modulator with the input sampling frequency of the modulator being modified to give the higher gains. A $sinc^3$ digital low-pass filter processes the output of the sigma-delta modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The first notch of this digital filter, its –3 dB frequency and its output rate can be programmed via the filter high and filter low registers. With a master clock frequency of 2.4576 MHz, the programmable range for this first notch frequency and output rate is from 4.8 Hz to 1.01 kHz giving a programmable range for the –3 dB frequency of 1.26 Hz to 265 Hz.

The basic connection diagram for the part is shown in Figure 2. This shows both the AV_{DD} and DV_{DD} pins of the AD7714 being driven from the analog +3 V or +5 V supply. Some applications will have AV_{DD} and DV_{DD} driven from separate supplies. In the connection diagram shown, the AD7714's analog inputs are configured as three fully differential inputs. The part is set up for unbuffered mode on the these analog inputs. An AD780, precision +2.5 V reference, provides the reference source for the part. On the digital side, the part is configured for three-wire operation with $\overline{CS}$ tied to DGND. A quartz crystal or ceramic resonator provides the master clock source for the part. It may be necessary to connect capacitors on the crystal or resonator to ensure that it does not oscillate at overtones of its fundamental operating frequency. The values of capacitors will vary depending on the manufacturer's specifications.

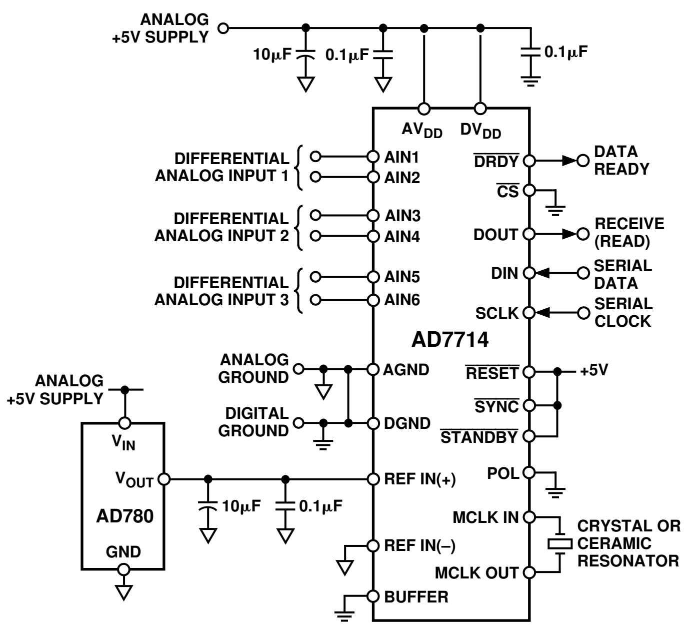


Figure 2. Basic Connection Diagram

ANALOG INPUT

Analog Input Ranges

The AD7714 contains six analog input pins (labelled AIN1 to AIN6) which can be configured as either three fully differential input channels or five pseudo-differential input channels. Bits CH0, CH1 and CH2 of the Communications Register configure the analog input arrangement and the channel selection is as outlined previously in Table VII. The input pairs (either differential or pseudo-differential) provide programmable-gain, input channels which can handle either unipolar or bipolar input signals. It should be noted that the bipolar input signals are referenced to the respective AIN(–) input of the input pair.

In unbuffered mode, the common-mode range of these inputs is from AGND to AV_{DD} provided that the absolute value of the analog input voltage lies between AGND – 30 mV and AV_{DD} + 30 mV. This means that in unbuffered mode the part can handle both unipolar and bipolar input ranges for all gains. In buffered mode, the analog inputs can handle much larger source impedances, but the absolute input voltage range is restricted to between AGND + 50 mV to AV_{DD} – 1.5 V which also places restrictions on the common-mode range. This means that in buffered mode there are some restrictions on the allowable gains for bipolar input ranges. Care must be taken in setting up the common-mode voltage and input voltage range so that the above limits are not exceeded, otherwise there will be a degradation in linearity performance.

In unbuffered mode, the analog inputs look directly into the 7 pF input sampling capacitor, C_{SAMP}. The dc input leakage current in this unbuffered mode is 1 nA maximum. As a result, the analog inputs see a dynamic load which is switched at the input sample rate (see Figure 3). This sample rate depends on master clock frequency and selected gain. C_{SAMP} is charged to AIN(+) and discharged to AIN(–) every input sample cycle. The effective on-resistance of the switch, R_{SW}, is typically 7 kΩ.

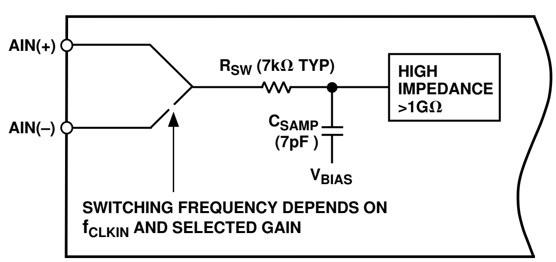


Figure 3. Unbuffered Analog Input Structure

C_{SAMP} must be charged through R_{SW} and through any external source impedances every input sample cycle. Therefore, in unbuffered mode, source impedances mean a longer charge time for C_{SAMP} and this may result in gain errors on the part. Table XII shows the allowable external resistance/capacitance values, for unbuffered mode, such that no gain error to the 16-bit level is introduced on the part. Table XIII shows the allowable external resistance/capacitance values, once again for unbuffered mode, such that no gain error to the 20-bit level is introduced.

Table XII. External R, C Combination for No 16-Bit Gain Error (Unbuffered Mode Only)

Gain	External Capacitance (pF)					
	0	50	100	500	1000	5000
1	368 kΩ	90.6 kΩ	54.2 kΩ	14.6 kΩ	8.2 kΩ	2.2 kΩ
2	177.2 kΩ	44.2 kΩ	26.4 kΩ	7.2 kΩ	4 kΩ	1.12 kΩ
4	82.8 kΩ	21.2 kΩ	12.6 kΩ	3.4 kΩ	1.94 kΩ	540 Ω
8–128	35.2 kΩ	9.6 kΩ	5.8 kΩ	1.58 kΩ	880 Ω	240 Ω

Table XIII. External R, C Combination for No 20-Bit Gain Error (Unbuffered Mode Only)

Gain	External Capacitance (pF)					
	0	50	100	500	1000	5000
1	290 kΩ	69 kΩ	40.8 kΩ	10.4 kΩ	5.6 kΩ	1.4 kΩ
2	141 kΩ	33.8 kΩ	20 kΩ	5 kΩ	2.8 kΩ	700 Ω
4	63.6 kΩ	16 kΩ	9.6 kΩ	2.4 kΩ	1.34 kΩ	340 Ω
8–128	26.8 kΩ	7.2 kΩ	4.4 kΩ	1.1 kΩ	600 Ω	160 Ω

In buffered mode, the analog inputs look into the high impedance inputs stage of the on-chip buffer amplifier. C_{SAMP} is charged via this buffer amplifier such that source impedances do not affect the charging of C_{SAMP}. This buffer amplifier has an offset leakage current of 1 nA. In this buffered mode, large source impedances result in a dc offset voltage developed across the source impedance but not in a gain error.

Input Sample Rate

The modulator sample frequency for the AD7714 remains at $f_{CLK\ IN}/128$ (19.2 kHz @ $f_{CLK\ IN}$ = 2.4576 MHz) regardless of the selected gain. However, gains greater than 1 are achieved by a combination of multiple input samples per modulator cycle and a scaling of the ratio of reference capacitor to input capacitor. As a result of the multiple sampling, the input sample rate of the device varies with the selected gain (see Table XIV). In buffered mode, the input is buffered before the input sampling capacitor. In unbuffered mode, where the analog input looks directly into the sampling capacitor, the effective input impedance is $1/C_{SAMP} \times f_S$ where C_{SAMP} is the input sampling capacitance and f_S is the input sample rate.

Table XIV. Input Sampling Frequency vs. Gain

Gain	Input Sampling Freq (f_S)
1	$f_{CLK\ IN}/64$ (38.4 kHz @ $f_{CLK\ IN}$ = 2.4576 MHz)
2	$2 \times f_{CLK\ IN}/64$ (76.8 kHz @ $f_{CLK\ IN}$ = 2.4576 MHz)
4	$4 \times f_{CLK\ IN}/64$ (153.6 kHz @ $f_{CLK\ IN}$ = 2.4576 MHz)
8	$8 \times f_{CLK\ IN}/64$ (307.2 kHz @ $f_{CLK\ IN}$ = 2.4576 MHz)
16	$8 \times f_{CLK\ IN}/64$ (307.2 kHz @ $f_{CLK\ IN}$ = 2.4576 MHz)
32	$8 \times f_{CLK\ IN}/64$ (307.2 kHz @ $f_{CLK\ IN}$ = 2.4576 MHz)
64	$8 \times f_{CLK\ IN}/64$ (307.2 kHz @ $f_{CLK\ IN}$ = 2.4576 MHz)
128	$8 \times f_{CLK\ IN}/64$ (307.2 kHz @ $f_{CLK\ IN}$ = 2.4576 MHz)

Burnout Current

The AD7714 contains two 1 μA currents, one source current from AV_{DD} to AIN(+) and one sink from AIN(–) to AGND. The currents are either both on or off depending on the BO bit of the Mode Register. These currents can be used in checking that a transducer has not burned out nor gone open-circuit before attempting to take measurements on that channel. If the currents are turned on, allowed flow in the transducer, a measurement of the input voltage on the analog input taken and the voltage measured is full scale, it indicates that the transducer has gone open-circuit; if the voltage measured is zero, it indicates that the transducer has gone short-circuit. For normal operation, these burnout currents are turned off by writing a 0 to the BO bit. For the source current to work correctly, the applied voltage on AIN(+) should not go within 500 mV of AV_{DD}. For the sink current to work correctly, the applied voltage on the AIN(–) input should not go within 500 mV of AGND.

Bipolar/Unipolar Inputs

The analog inputs on the AD7714 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that the part can handle negative voltages on its analog inputs, since the analog input cannot go more negative than –30 mV to ensure correct operation of the part. The input channels are either fully differential or pseudo-differential (all other channels referenced to AIN6). In either case, the input channels are arranged in pairs with an AIN(+) and AIN(–). As a result, the voltage to which the unipolar and bipolar signals on the AIN(+) input are referenced is the voltage on the respective AIN(–) input. For example, if AIN(–) is +2.5 V and the AD7714 is configured for unipolar operation with a gain of 2 and a V_{REF} of +2.5 V, the input voltage range on the AIN(+) input is +2.5 V to +3.75 V. If AIN(–) is +2.5 V and the AD7714 is configured for bipolar mode with a gain of 2 and a V_{REF} of +2.5 V, the analog input range on the AIN(+) input is +1.25 V to +3.75 V (i.e., 2.5 V ± 1.25 V). If AIN(–) is at AGND, the part cannot be configured for bipolar ranges in excess of ±30 mV.

Bipolar or unipolar options are chosen by programming the $\overline{B}$/U bit of the Filter High Register. This programs the selected channel for either unipolar or bipolar operation. Programming the channel for either unipolar or bipolar operation does not change any of the input signal conditioning; it simply changes the data output coding and the points on the transfer function where calibrations occur.

REFERENCE INPUT

The AD7714's reference inputs, REF IN(+) and REF IN(–), provide a differential reference input capability. The common-mode range for these differential inputs is from AGND to AV_{DD}. The nominal reference voltage, V_{REF} (REF IN(+) –REF IN(–)), for specified operation is +2.5 V for the AD7714-5 and +1.25 V for the AD7714-3. The part is functional with V_{REF} voltages down to 1 V but with degraded performance as the output noise will, in terms of LSB size, be larger. REF IN(+) must always be greater than REF IN(–) for correct operation of the AD7714.

Both reference inputs provide a high impedance, dynamic load similar to the analog inputs in unbuffered mode. The maximum dc input leakage current is ±1 nA over temperature and source resistance may result in gain errors on the part. In this case, the sampling switch resistance is 5 kΩ typ and the reference capacitor (C_{REF}) varies with gain. The sample rate on the reference inputs is $f_{CLK\ IN}/64$ and does not vary with gain. For gains of 1 to 8, C_{REF} is 8 pF; for a gain of 16, it is 5.5 pF, for a gain of 32, it is 4.25 pF, for a gain of 64, it is 3.625 pF and for a gain of 128, it is 3.3125 pF.

The output noise performance outlined in Tables I through IV is for an analog input of 0 V and is unaffected by noise on the reference. To obtain the same noise performance as shown in the noise tables over the full input range requires a low noise reference source for the AD7714. If the reference noise in the bandwidth of interest is excessive, it will degrade the performance of the AD7714. In applications where the excitation voltage for the bridge transducer on the analog input also derives the reference voltage for the part, the effect of the noise in the excitation voltage will be removed as the application is ratiometric. Recommended reference voltage sources for the AD7714-5 and AD7714Y grade with AV_{DD} = 5 V include the AD780, REF43 and REF192 while the recommended reference sources for the AD7714-3 and AD7714Y with AV_{DD} = 3 V include the AD589 and AD1580. It is generally recommended to decouple the output of these references to further reduce the noise level.

DIGITAL FILTERING

The AD7714 contains an on-chip low-pass digital filter which processes the output of the part's sigma-delta modulator. Therefore, the part not only provides the analog-to-digital conversion function but it also provides a level of filtering. There are a number of system differences when the filtering function is provided in the digital domain rather than the analog domain and the user should be aware of these.

First, since digital filtering occurs after the A-to-D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this. Also, the digital filter can be made programmable far more readily than an analog filter. Depending on the digital filter design, this gives the user the capability of programming cutoff frequency and output update rate.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. To alleviate this problem, the AD7714 has overrange headroom built into the sigma-delta modulator and digital filter which allows overrange excursions of 5% above the analog input range. If noise signals are larger than this, consideration should be given to analog input filtering, or to reducing the input channel voltage so that its full scale is half that of the analog input channel full scale. This will provide an overrange capability greater than 100% at the expense of reducing the dynamic range by 1 bit (50%).

In addition, the digital filter does not provide any rejection at integer multiples of the digital filter's sample frequency. However, the input sampling on the part provides attenuation at multiples of the digital filter's sampling frequency so that the unattenuated bands actually occur around multiples of the input sampling frequency f_S (as defined in Table XIV). Thus, the unattenuated bands occur at $n \times f_S$ (where n = 1, 2, 3. . .). At these frequencies, there are frequency bands, $\pm f_{3\ dB}$ wide ($f_{3\ dB}$ is the cutoff frequency of the digital filter) at either side where noise passes unattenuated to the output.

Filter Characteristics

The AD7714's digital filter is a low-pass filter with a $(\sin x/x)^3$ response (also called sinc^3). The transfer function for this filter is described in the z-domain by:

$$H(z) = \left[\frac{1}{N} \times \frac{1 - Z^{-N}}{1 - Z^{-1}} \right]^3$$

and in the frequency domain by:

$$\left| H(f) \right| = \left| \frac{1}{N} \times \frac{Sin\,(N.\pi.f/f_S)}{Sin\,(\pi.f/f_S)} \right|^3$$

Figure 4 shows the filter frequency response for a cutoff frequency of 2.62 Hz which corresponds to a first filter notch frequency of 10 Hz. The plot is shown from dc to 65 Hz. This response is repeated at either side of the input sampling frequency and at either side of multiples of the input sampling frequency.

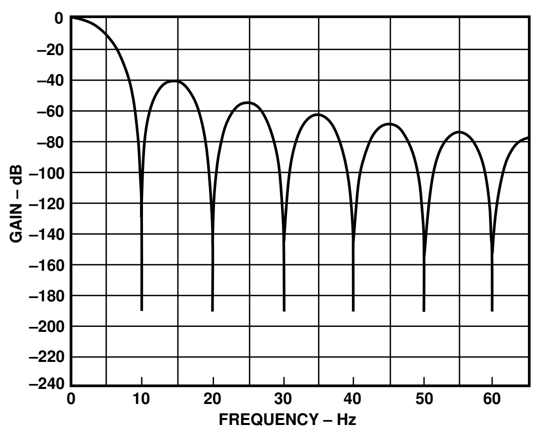


Figure 4. Frequency Response of AD7714 Filter

The response of the filter is similar to that of an averaging filter but with a sharper roll-off. The output rate for the digital filter corresponds with the positioning of the first notch of the filter's frequency response. Thus, for the plot of Figure 4 where the output rate is 10 Hz, the first notch of the filter is at 10 Hz. The notches of this $(\sin x/x)^3$ filter are repeated at multiples of the first notch. The filter provides attenuation of better than 100 dB at these notches. For the example given, if the first notch is at 10 Hz, there will be notches (and hence >100 dB rejection) at both 50 Hz and 60 Hz.

The cutoff frequency of the digital filter is determined by the value loaded to bits FS0 to FS11 in the Filter High and Filter Low Registers. Programming a different cutoff frequency via FS0 – FS11 does not alter the profile of the filter response; it changes the frequency of the notches as outlined in the Filter Registers section. The output update and first notch correspond and are determined by the relationship:

$$Output\ Rate = f_{CLK\ IN}/(N.128)$$

where *N* is the decimal equivalent of the word loaded to the FS0 to FS11 bits of the Filter Registers

while the –3 dB frequency is determined by the relationship:

$$-3\ dB\ frequency = 0.262 \times filter\ first\ notch\ frequency$$

The filter provides a linear phase response with a group delay determined by:

$$Group\ Delay = -3\pi.(N.f/f_{MOD})$$

where *N* is the decimal equivalent of the word loaded to the FS0 to FS11 bits of the Filter Registers and $f_{MOD} = f_{CLK\ IN}/128$.

Since the AD7714 contains this on-chip, low-pass filtering, a settling time is associated with step function inputs and data on the output will be invalid after a step change until the settling time has elapsed. The settling time depends upon the output rate chosen for the filter. The settling time of the filter to a full-scale step input can be up to four times the output data period. For a synchronized step input (using the $\overline{SYNC}$ or FSYNC functions) the settling time is three times the output data period. When changing channels on the part, the change from one channel to the other is synchronized so the output settling time is also three times the output data period. Thus, in switching between channels, the output data register is not updated until the settling time of the filter has elapsed.

Post-Filtering

The on-chip modulator provides samples at a 19.2 kHz output rate with $f_{CLK\ IN}$ at 2.4576 MHz. The on-chip digital filter decimates these samples to provide data at an output rate that corresponds to the programmed output rate of the filter. Since the output data rate is higher than the Nyquist criterion, the output rate for a given bandwidth will satisfy most application requirements. However, there may be some applications that require a higher data rate for a given bandwidth and noise performance. Applications that need this higher data rate will require some post-filtering following the part's digital filter.

For example, if the required bandwidth is 7.86 Hz but the required update rate is 100 Hz, the data can be taken from the AD7714 at the 100 Hz rate giving a –3 dB bandwidth of 26.2 Hz. Post-filtering can be applied to this to reduce the bandwidth and output noise, to the 7.86 Hz bandwidth level, while maintaining an output rate of 100 Hz.

Post-filtering can also be used to reduce the output noise from the device for bandwidths below 1.26 Hz. At a gain of 128 and a bandwidth of 1.26 Hz, the output rms noise is 140 nV. This is essentially device noise or white noise and since the input is chopped, the noise has a primarily flat frequency response. By reducing the bandwidth below 1.26 Hz, the noise in the resultant passband can be reduced. A reduction in bandwidth by a factor of 2 results in a reduction of approximately 1.25 in the output rms noise. This additional filtering will result in a longer settling time.

ANALOG FILTERING

The digital filter does not provide any rejection at integer multiples of the input sampling frequency, as outlined earlier. However, due to the AD7714's high oversampling ratio, these bands occupy only a small fraction of the spectrum and most broadband noise is filtered. This means that the analog filtering requirements in front of the AD7714 are considerably reduced versus a conventional converter with no on-chip filtering. In addition, because the part's common-mode rejection performance of 100 dB extends out to several kHz, common-mode noise in this frequency range will be substantially reduced.

Depending on the application, however, it may be necessary to provide attenuation prior to the AD7714 in order to eliminate unwanted frequencies from these bands which the digital filter will pass. It may also be necessary in some applications to provide analog filtering in front of the AD7714 to ensure that differential noise signals outside the band of interest do not saturate the analog modulator.

If passive components are placed in front of the AD7714, in unbuffered mode, care must be taken to ensure that the source impedance is low enough so as not to introduce gain errors in the system. This significantly limits the amount of passive anti-aliasing filtering which can be provided in front of the AD7714 when it is used in unbuffered mode. However, when the part is used in buffered mode, large source impedances will simply result in a small dc offset error (a 10 kΩ source resistance will cause an offset error of less than 10 μV). Therefore, if the system requires any significant source impedances to provide passive analog filtering in front of the AD7714, it is recommended that the part be operated in buffered mode.

CALIBRATION

The AD7714 provides a number of calibration options which can be programmed via the MD2, MD1 and MD0 bits of the Mode Register. The different calibration options are outlined in the Mode Register and Calibration Sequences sections. A calibration cycle may be initiated at any time by writing to these bits of the Mode Register. Calibration on the AD7714 removes offset and gain errors from the device. A calibration routine should be initiated on the device whenever there is a change in the ambient operating temperature or supply voltage. It should also be initiated if there is a change in the selected gain, filter notch or bipolar/unipolar input range.

The AD7714 gives the user access to the on-chip calibration registers allowing the microprocessor to read the device's calibration coefficients and also to write its own calibration coefficients to the part from prestored values in E^2PROM. This gives the microprocessor much greater control over the AD7714's calibration procedure. It also means that the user can verify that the device has performed its calibration correctly by comparing the coefficients after calibration with prestored values in E^2PROM. The values in these calibration registers are 24-bit wide. In addition, the span and offset for the part can be adjusted by the user.

There is a significant variation in the value of these coefficients across the different output update rates, gains and unipolar/bipolar operation. Internally in the AD7714, these coefficients are normalized before being used to scale the words coming out of the digital filter. The offset calibration register contains a value which, when normalized, is subtracted from all conversion results. The full-scale calibration register contains a value which, when normalized, is multiplied by all conversion results. The offset calibration coefficient is subtracted from the result prior to the multiplication by the full-scale coefficient. This means that the full-scale coefficient is effectively a span or gain coefficient.

The AD7714 offers self-calibration, system calibration and background calibration facilities. For full calibration to occur on the selected channel, the on-chip microcontroller must record the modulator output for two different input conditions. These are "zero-scale" and "full-scale" points. These points are derived by performing a conversion on the different input voltages provided to the input of the modulator during calibration. As a result, the accuracy of the calibration can only be as good as the noise level which the part provides in normal mode. The result of the "zero-scale" calibration conversion is stored in the Zero Scale Calibration Register for the appropriate channel. The result of the "full-scale" calibration conversion is stored in the Full-Scale Calibration Register for the appropriate channel. With these readings, the microcontroller can calculate the offset and the gain slope for the input to output transfer function of the converter. Internally, the part works with 33 bits of resolution to determine its conversion result of either 16 bits or 24 bits.

Self-Calibration

A self-calibration is initiated on the AD7714 by writing the appropriate values (0, 0, 1) to the MD2, MD1 and MD0 bits of the Mode Register. In the self-calibration mode with a unipolar input range, the zero-scale point used in determining the calibration coefficients is with the inputs of the differential pair internally shorted on the part (i.e., AIN(+) = AIN(–) = Internal Bias Voltage). The PGA is set for the selected gain (as per G2, G1, G0 bits in the Mode Register) for this zero-scale calibration conversion. The full-scale calibration conversion is performed at the selected gain on an internally-generated voltage of V_{REF}/Selected Gain.

The duration time of the calibration is 6 × 1/Output Rate. This is made up of 3 × 1/Output Rate for the zero-scale calibration and 3 × 1/Output Rate for the full-scale calibration. At this time the MD2, MD1 and MD0 bits in the Mode Register return to 0, 0, 0. This gives the earliest indication that the calibration sequence is complete. The $\overline{DRDY}$ line goes high when calibration is initiated and does not return low until there is a valid new word in the data register. The duration time from the calibration command being issued to $\overline{DRDY}$ going low is 9 × 1/Output Rate. This is made up of 3 × 1/Output Rate for the zero-scale calibration, 3 × 1/Output Rate for the full-scale calibration and 3 × 1/Output Rate for a conversion on the analog input. If $\overline{DRDY}$ is low before (or goes low during) the calibration command write to the Mode Register, it may take up to one modulator cycle (MCLK IN/128) before $\overline{DRDY}$ goes high to indicate that calibration is in progress. Therefore, $\overline{DRDY}$ should be ignored for up to one modulator cycle after the last bit of the calibration command is written to the Mode Register.

For bipolar input ranges in the self-calibrating mode, the sequence is very similar to that just outlined. In this case, the two points are exactly the same as above but since the part is configured for bipolar operation, the output code for zero differential input is 800000 Hex in 24-bit mode.

The part also offers ZS Self-Calibration and FS Self-Calibration options. In these cases, the part performs just a zero-scale or full-scale calibration respectively and not a full calibration of the part. A full-scale calibration should not be carried out unless the part contains valid zero-scale coefficients. These calibrations are initiated on the AD7714 by writing the appropriate values (1, 1, 0 for ZS Self-Calibration and 1, 1, 1 for FS Self Calibration) to the MD2, MD1 and MD0 bits of the Mode Register. The zero-scale or full-scale calibration is exactly the same as that described for the full self-calibration. In these cases, the duration of the calibration is 3 × 1/Output Rate. At this time the MD2, MD1 and MD0 bits in the Mode Register return to 0, 0, 0. This gives the earliest indication that the calibration sequence is complete. The $\overline{DRDY}$ line goes high when calibration is initiated and does not return low until there is a valid new word in the data register. The time from the calibration command being issued to $\overline{DRDY}$ going low is 6 × 1/Output Rate. This is made up of 3 × 1/Output Rate for the zero-scale or full-scale calibration and 3 × 1/Output Rate for a conversion on the analog input. If $\overline{DRDY}$ is low before (or goes low during) the calibration command write to the Mode Register, it may take up to one modulator cycle (MCLK IN/128) before $\overline{DRDY}$ goes high to indicate that calibration is in progress. Therefore, $\overline{DRDY}$ should be ignored for up to one modulator cycle after the last bit of the calibration command is written to the Mode Register.

The fact that the self-calibration can be performed as a two step calibration offers another feature. After the sequence of a full self calibration has been completed, additional offset or gain calibrations can be performed by themselves to adjust the part's zero point or gain. Calibrating one of the parameters, either offset or gain, will not affect the other parameter.

System Calibration

System calibration allows the AD7714 to compensate for system gain and offset errors as well as its own internal errors. System calibration performs the same slope factor calculations as self-calibration but uses voltage values presented by the system to the AIN inputs for the zero- and full-scale points. Full System calibration requires a two-step process, a ZS System Calibration followed by a FS System Calibration.

For a full system calibration, the zero-scale point must be presented to the converter first. It must be applied to the converter before the calibration step is initiated and remain stable until the step is complete. Once the system zero scale has been set up at the analog input, a ZS System Calibration is then initiated by writing the appropriate values (0, 1, 0) to the MD2, MD1 and MD0 bits of the Mode Register. The zero-scale system calibration is performed at the selected gain. The duration of the calibration is 3 × 1/Output Rate. At this time, the MD2, MD1 and MD0 bits in the Mode Register return to 0, 0, 0. This gives the earliest indication that the calibration sequence is complete. The $\overline{DRDY}$ line goes high when calibration is initiated and does not return low until there is a valid new word in the data register. The time from the calibration command being issued to $\overline{DRDY}$ going low is 4 × 1/Output Rate. This is made up of 3 × 1/Output Rate for the zero-scale system calibration and 1/Output Rate for a conversion on the analog input. This conversion on the analog input is on the same voltage as the zero-scale system calibration and, therefore, the resultant word in the data register from this conversion should be a zero-scale reading. If $\overline{DRDY}$ is low before (or goes low during) the calibration command write to the Mode Register, it may take up to one modulator cycle (MCLK IN/128) before $\overline{DRDY}$ goes high to indicate that calibration is in progress. Therefore, $\overline{DRDY}$ should be ignored for up to one modulator cycle after the last bit of the calibration command is written to the Mode Register.

After the zero-scale point is calibrated, the full-scale point is applied to AIN and the second step of the calibration process is initiated by again writing the appropriate values (0, 1, 1) to MD2, MD1 and MD0. Again the full-scale voltage must be set up before the calibration is initiated, and it must remain stable throughout the calibration step. The full-scale system calibration is performed at the selected gain. The duration of the calibration is 3 × 1/Output Rate. At this time, the MD2, MD1 and MD0 bits in the Mode Register return to 0, 0, 0. This gives the earliest indication that the calibration sequence is complete. The $\overline{DRDY}$ line goes high when calibration is initiated and does not return low until there is a valid new word in the data register. The time from the calibration command being issued to $\overline{DRDY}$ going low is 4 × 1/Output Rate. This is made up of 3 × 1/Output Rate for the full-scale system calibration and 1/Output Rate for a conversion on the analog input. This conversion on the analog input is on the same voltage as the full-scale system calibration and, therefore, the resultant word in the data register from this conversion should be a full-scale reading. If $\overline{DRDY}$ is low before (or goes low during) the calibration command write to the Mode Register, it may take up to one modulator cycle (MCLK IN/128) before $\overline{DRDY}$ goes high to indicate that calibration is in progress. Therefore, $\overline{DRDY}$ should be ignored for up to one modulator cycle after the last bit of the calibration command is written to the Mode Register.

In the unipolar mode, the system calibration is performed between the two endpoints of the transfer function; in the bipolar mode, it is performed between midscale (zero differential voltage) and positive full scale.

The fact that the system calibration is a two step calibration offers another feature. After the sequence of a full system calibration has been completed, additional offset or gain calibrations can be performed by themselves to adjust the system zero reference point or the system gain. Calibrating one of the parameters, either system offset or system gain, will not affect the other parameter. A full-scale calibration should not be carried out unless the part contains valid zero-scale coefficients.

System calibration can also be used to remove any errors from source impedances on the analog input when the part is used in unbuffered mode. A simple R, C antialiasing filter on the front end may introduce a gain error on the analog input voltage but the system calibration can be used to remove this error.