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8-/10-Channel, Low Voltage, Low Power, Σ-Δ ADCs

AD7708/AD7718

FEATURES

8-/10-Channel, High Resolution Σ-Δ ADCs
AD7708 Has 16-Bit Resolution
AD7718 Has 24-Bit Resolution
Factory-Calibrated
Single Conversion Cycle Setting
Programmable Gain Front End
Simultaneous 50 Hz and 60 Hz Rejection
***VREF Select*™ Allows Absolute and Ratiometric Measurement Capability**
Operation Can Be Optimized for
Analog Performance ($\overline{CHOP}$ = 0) or
Channel Throughput ($\overline{CHOP}$ = 1)

INTERFACE

3-Wire Serial
SPI™, QSPI™, MICROWIRE™, and DSP-Compatible
Schmitt Trigger on SCLK

POWER

Specified for Single 3 V and 5 V Operation
Normal: 1.28 mA Typ @ 3 V
Power-Down: 30 μA (32 kHz Crystal Running)
On-Chip Functions
Rail-to-Rail Input Buffer and PGA
2-Bit Digital I/O Port

APPLICATIONS

Industrial Process Control
Instrumentation
Pressure Transducers
Portable Instrumentation
Smart Transmitters

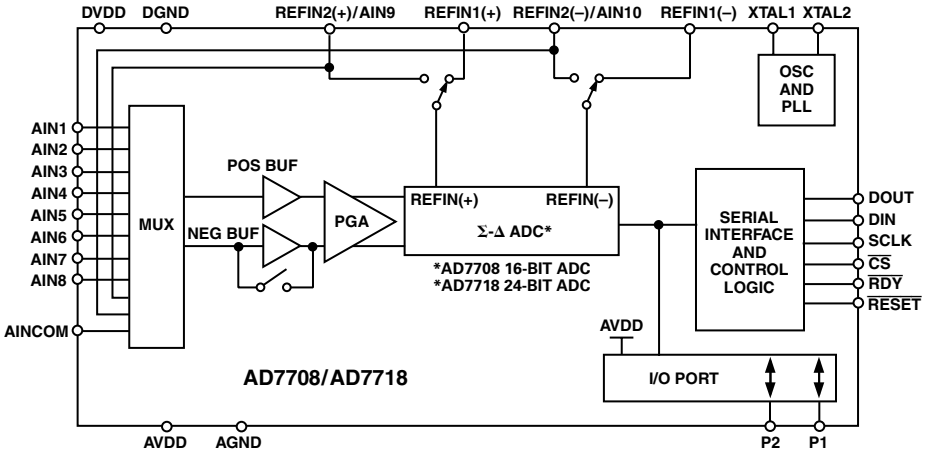
GENERAL DESCRIPTION

The AD7708/AD7718 are complete analog front-ends for low frequency measurement applications. The AD7718 contains a 24-bit Σ-Δ ADC with PGA and can be configured as 4/5 fully-differential input channels or 8/10 pseudo-differential input channels. Two pins on the device are configurable as analog inputs or reference inputs. The AD7708 is a 16-bit version of the AD7718. Input signal ranges from 20 mV to 2.56 V can be directly converted using these ADCs. Signals can be converted directly from a transducer without the need for signal conditioning.

The device operates from a 32 kHz crystal with an on-board PLL generating the required internal operating frequency. The output data rate from the part is software programmable. The peak-to-peak resolution from the part varies with the programmed gain and output data rate.

The part operates from a single 3 V or 5 V supply. When operating from 3 V supplies, the power dissipation for the part is 3.84 mW typ. Both parts are pin-for-pin compatible allowing an upgradable path from 16 to 24 bits without the need for hardware modifications. The AD7708/AD7718 are housed in 28-lead SOIC and TSSOP packages.

FUNCTIONAL BLOCK DIAGRAM



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AD7718 SPECIFICATIONS[1] (AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, REFIN(+) = 2.5 V; REFIN(–) = AGND; AGND = DGND = 0 V; XTAL1/XTAL2 = 32.768 kHz Crystal Input Buffer Enabled. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Grade	Unit	Test Conditions
AD7718 (CHOP DISABLED)			
Output Update Rate	16.06	Hz min	CHOP = 1
	1.365	kHz max	
No Missing Codes[2]	24	Bits min	
Resolution	13	Bits p-p	±20 mV Range, SF = 69
	18	Bits p-p	±2.56 V Range, SF = 69
Output Noise and Update Rates	See Tables in ADC Description		
Integral Nonlinearity	±10	ppm of FSR max	2 ppm Typical
Offset Error[3]	Table VII	µV typ	Offset Error is in the order of the noise for the programmed gain and update rate following a calibration
Offset Error Drift vs. Temp[4]	±200	nV/°C typ	
Full-Scale Error[3]	±10	µV typ	
Gain Drift vs. Temp[4]	±0.5	ppm/°C typ	
Negative Full-Scale Error	±0.003	% FSR max	
ANALOG INPUTS			
Differential Input Full-Scale Voltage	±1.024 × REFIN/GAIN	V nom	REFIN Refers to Both REFIN1 and REFIN2. REFIN = REFIN(+) –REFIN(–) GAIN = 1 to 128
Absolute AIN Voltage Limits	AGND + 100 mV	V min	AIN1–AIN10 and AINCOM with
	AV_{DD} – 100 mV	V max	NEGBUF = 1
Absolute AINCOM Voltage Limits	AGND – 30 mV	V min	NEGBUF = 0
	AV_{DD} + 30 mV	V max	
Analog Input Current			AIN1–AIN10 and AINCOM with NEGBUF = 1
DC Input Current[2]	±1	nA max	
DC Bias Current Drift	±5	pA/°C typ	
AINCOM Input Current			NEGBUF = 0
DC Input Current[2]	±125	nA/V typ	±2.56 V Range
DC Bias Current Drift	±2	pA/V/°C typ	
Normal-Mode Rejection[2]			
@ 50 Hz	100	dB min	50 Hz ± 1 Hz, SF Word = 82
@ 60 Hz	100	dB min	60 Hz ± 1 Hz, SF Word = 68
Common-Mode Rejection			
@ DC	90	dB min	100 dB typ, Analog Input = 1 V, Input Range = ±2.56 V 110 dB typ on ±20 mV Range
@ 50 Hz	100	dB typ	50 Hz ± 1 Hz, SF Word = 82
@ 60 Hz	100	dB typ	60 Hz ± 1 Hz, SF Word = 68
REFERENCE INPUTS (REFIN1 AND REFIN2)			
REFIN(+) to REFIN(–) Voltage	2.5	V nom	REFIN Refers to Both REFIN1 and REFIN2
REFIN(+) to REFIN(–) Range[2]	1	V min	
	AV_{DD}	V max	
REFIN Common-Mode Range	AGND – 30 mV	V min	
	AV_{DD} + 30 mV	V max	
Reference DC Input Current	0.5	µA/V typ	
Reference DC Input Current Drift	±0.1	nA/V/°C typ	
Normal-Mode Rejection[2]			
@ 50 Hz	100	dB min	50 Hz ± 1 Hz, SF Word = 82
@ 60 Hz	100	dB min	60 Hz ± 1 Hz, SF Word = 68
Common-Mode Rejection			Input Range = ±2.56 V
@ DC	100	dB typ	Analog Input = 1 V. Input Range = ±2.56 V
@ 50 Hz	100	dB typ	
@ 60 Hz	100	dB typ	

AD7718–SPECIFICATIONS[1] (AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, REFIN(+) = 2.5 V ; REFIN(–) = AGND; AGND = DGND = 0 V; XTAL1/XTAL2 = 32.768 kHz Crystal Input Buffer Enabled. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Grade	Unit	Test Conditions
AD7718 (CHOP ENABLED)			
Output Update Rate	5.4	Hz min	$\overline{CHOP}$ = 0
	105	Hz max	
No Missing Codes[2]	24	Bits min	20 Hz Update Rate
Resolution	13	Bits p-p	±20 mV Range, 20 Hz Update Rate
	18	Bits p-p	±2.56 V Range, 20 Hz Update Rate
Output Noise and Update Rates	See Tables in ADC Description		
Integral Nonlinearity	±10	ppm of FSR max	2 ppm Typical
Offset Error[3]	±3	µV typ	
Offset Error Drift vs. Temp[4]	10	nV/°C typ	
Full-Scale Error[3]	±10	µV/°C typ	
Gain Drift vs. Temp[4]	±0.5	ppm/°C typ	
ANALOG INPUTS			
Differential Input Full-Scale Voltage	±1.024 × REFIN/GAIN	V nom	REFIN Refers to Both REFIN1 and REFIN2. REFIN = REFIN(+) REFIN(–) GAIN = 1 to 128
Range Matching	±2	µV typ	Analog Input = 18 mV
Absolute AIN Voltage Limits	AGND + 100 mV	V min	AIN1–AIN10 and AINCOM with
	AV_{DD} – 100 mV	V max	NEGBUF = 1
Absolute AINCOM Voltage Limits	AGND – 30 mV	V min	NEGBUF = 0
	AV_{DD} + 30 mV	V max	
Analog Input Current			AIN1–AIN10 and AINCOM with NEGBUF = 1
DC Input Current[2]	±1	nA max	
DC Input Current Drift	±5	pA/°C typ	
AINCOM Input Current			NEGBUF = 0
DC Input Current[2]	±125	nA/V typ	±2.56 V Range
DC Bias Current Drift	±2	pA/V/°C typ	
Normal-Mode Rejection[2]			
@ 50 Hz	100	dB min	50 Hz ± 1 Hz, SF Word = 82
@ 60 Hz	100	dB min	60 Hz ± 1 Hz, SF Word = 68
Common-Mode Rejection			
@ DC	90	dB min	100 dB typ, Analog Input = 1 V, Input Range = ±2.56 V 110 dB typ on ±20 mV Range
@ 50 Hz[2]	100	dB min	50 Hz ± 1 Hz, 20 Hz Update Rate
@ 60 Hz[2]	100	dB min	60 Hz ± 1 Hz, 20 Hz Update Rate
REFERENCE INPUTS (REFIN1 AND REFIN2)			
REFIN(+) to REFIN(–) Voltage	2.5	V nom	REFIN Refers to Both REFIN1 and REFIN2
REFIN(+) to REFIN(–) Range[2]	1	V min	
	AV_{DD}	V max	
REFIN Common-Mode Range	AGND – 30 mV	V min	
	AV_{DD} + 30 mV	V max	
Reference DC Input Current[2]	±0.5	µA/V typ	
Reference DC Input Current Drift	±0.01	nA/V/°C typ	
Normal-Mode Rejection[2]			
@ 50 Hz	100	dB min	50 Hz ± 1 Hz, SF Word = 82
@ 60 Hz	100	dB min	60 Hz ± 1 Hz, SF Word = 68
Common-Mode Rejection[2]			Input Range = ±2.56 V
@ DC	110	dB typ	Analog Input = 1 V
@ 50 Hz	110	dB typ	50 Hz ± 1 Hz, 20 Hz Update Rate
@ 60 Hz	110	dB typ	60 Hz ± 1 Hz, 20 Hz Update Rate
LOGIC INPUTS[5]			
All Inputs Except SCLK and XTAL1[2]			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = 5 V
V_{INL}, Input Low Voltage	0.4	V max	DV_{DD} = 3 V
V_{INH}, Input High Voltage	2.0	V min	DV_{DD} = 3 V or 5 V

Parameter	B Grade	Unit	Test Conditions
LOGIC INPUTS (Continued)			
SCLK Only (Schmitt-Triggered Input)[2]			
$V_{T(+)}$	1.4/2	V min/V max	DV_{DD} = 5 V
$V_{T(-)}$	0.8/1.4	V min/V max	DV_{DD} = 5 V
$V_{T(+)} - V_{T(-)}$	0.3/0.85	V min/V max	DV_{DD} = 5 V
$V_{T(+)}$	0.95/2	V min/V max	DV_{DD} = 3 V
$V_{T(-)}$	0.4/1.1	V min/V max	DV_{DD} = 3 V
$V_{T(+)}–V_{T(-)}$	0.3/0.85	V min/V max	DV_{DD} = 3 V
XTAL1 Only[2]			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = 5 V
V_{INH}, Input High Voltage	3.5	V min	DV_{DD} = 5 V
V_{INL}, Input Low Voltage	0.4	V max	DV_{DD} = 3 V
V_{INH}, Input High Voltage	2.5	V min	DV_{DD} = 3 V
Input Currents	±10	μA max	Logic Input = DV_{DD}
	–70	μA max	Logic Input = DGND, Typical –40 μA @ 5 V and –20 μA at 3 V
Input Capacitance	10	pF typ	All Digital Inputs
LOGIC OUTPUTS (Excluding XTAL2)[5]			
V_{OH}, Output High Voltage[2]	DV_{DD} – 0.6	V min	DV_{DD} = 3 V, I_{SOURCE} = 100 μA
V_{OL}, Output Low Voltage[2]	0.4	V max	DV_{DD} = 3 V, I_{SINK} = 100 μA
V_{OH}, Output High Voltage[2]	4	V min	DV_{DD} = 5 V, I_{SOURCE} = 200 μA
V_{OL}, Output Low Voltage[2]	0.4	V max	DV_{DD} = 5 V, I_{SINK} = 1.6 mA
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance	±10	pF typ	
Data Output Coding	Binary		Unipolar Mode
	Offset Binary		Bipolar Mode
SYSTEM CALIBRATION[2]			
Full-Scale Calibration Limit	1.05 × FS	V max	
Zero-Scale Calibration Limit	–1.05 × FS	V min	
Input Span	0.8 × FS	V min	
	2.1 × FS	V max	
START-UP TIME			
From Power-On	300	ms typ	
From Power-Down Mode	1	ms typ	Oscillator Enabled
	300	ms typ	Oscillator Powered Down
POWER REQUIREMENTS			
Power Supply Voltages	AV_{DD} and DV_{DD} can be operated independently of each other.		
AV_{DD}–AGND	2.7/3.6	V min/max	AV_{DD} = 3 V nom
	4.75/5.25	V min/max	AV_{DD} = 5 V nom
DV_{DD}–DGND	2.7/3.6	V min/max	DV_{DD} = 3 V nom
	4.75/5.25	V min	DV_{DD} = 5 V nom
DI_{DD} (Normal Mode)	0.55	mA max	DV_{DD} = 3 V, 0.43 mA typ
	0.65	mA max	DV_{DD} = 5 V, 0.5 mA typ
AI_{DD} (Normal Mode)	1.1	mA max	AV_{DD} = 3 V or 5 V, 0.85 mA typ
DI_{DD} (Power-Down Mode)	10	μA max	DV_{DD} = 3 V, 32.768 kHz Osc. Running
	2	μA max	DV_{DD} = 3 V, Oscillator Powered Down
	30	μA max	DV_{DD} = 5 V, 32.768 kHz Osc. Running
	8	μA max	DV_{DD} = 5 V, Oscillator Powered Down
AI_{DD} (Power-Down Mode)	1	μA max	AV_{DD} = 3 V or 5 V
Power Supply Rejection (PSR)			Input Range = ±2.56 V, AIN = 1 V
Chop Disabled	70	dB min	95 dB typ
Chop Enabled	100	dB typ	

NOTES
[1]Temperature range is –40°C to +85°C.
[2]Not production tested, guaranteed by design and/or characterization data at release.
[3]Following a self-calibration this error will be in the order of the noise for the programmed gain and update selected. A system calibration will completely remove this error.
[4]Recalibration at any temperature will remove these errors.
[5]I/O Port Logic Levels are with respect to AV_{DD} and AGND.

Specifications are subject to change without notice.

AD7708 SPECIFICATIONS[1] (AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, REFIN(+) = 2.5 V; REFIN(–) = AGND; AGND = DGND = 0 V; XTAL1/XTAL2 = 32.768 kHz Crystal Input Buffers Enabled. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Grade	Unit	Test Conditions
AD7708 (CHOP DISABLED)			
Output Update Rate	16.06	Hz min	$\overline{CHOP}$ = 1
	1.365	kHz max	
No Missing Codes[2]	16	Bits min	
Resolution	13	Bits p-p	±20 mV Range, SF Word = 69
	16	Bits p-p	±2.56 V Range, SF Word = 69
Output Noise and Update Rates	See Tables in ADC Description		
Integral Nonlinearity	±15	ppm of FSR max	2ppm Typical
Offset Error[3]	±0.65	LSB typ	Following a Self-Calibration
Offset Error Drift vs. Temp[4]	±200	nV/°C typ	
Full-Scale Error[3]	±0.75	LSB typ	
Gain Drift vs. Temp[4]	±0.5	ppm/°C typ	
Negative Full-Scale Error	±0.003	% FSR typ	
ANALOG INPUTS			
Differential Input Full-Scale Voltage	±1.024 × REFIN/GAIN	V nom	REFIN Refers to Both REFIN1 and REFIN2. REFIN = REFIN(+) – REFIN(–) GAIN = 1 to 128
Absolute AIN Voltage Limits	AGND + 100 mV	V min	AIN1–AIN10 and AINCOM with
	AV_{DD} – 100 mV	V max	NEGBUF = 1
Absolute AINCOM Voltage Limits	AGND – 30 mV	V min	NEGBUF = 0
	AV_{DD} + 30 mV	V max	
Analog Input Current			AIN1–AIN10 and AINCOM with NEGBUF = 1
DC Input Current[2]	±1	nA max	
DC Bias Current Drift	±5	pA/°C typ	
AINCOM Input Current			NEGBUF = 0
DC Input Current[2]	±125	nA/V typ	±2.56 V Range
DC Bias Current Drift	±2	pA/V/°C typ	
Normal-Mode Rejection[2]			
@ 50 Hz	100	dB min	50 Hz ± 1 Hz, SF Word = 82
@ 60 Hz	100	dB min	60 Hz ± 1 Hz, SF Word = 68
Common-Mode Rejection			
@ DC	90	dB min	100 dB typ, Analog Input = 1 V, Input Range = ±2.56 V 110 dB typ on ±20 mV Range
@ 50 Hz	100	dB typ	50 Hz ± 1 Hz, SF Word = 82
@ 60 Hz	100	dB typ	60 Hz ± 1 Hz, SF Word = 68
REFERENCE INPUTS (REFIN1 AND REFIN2)			
REFIN(+) to REFIN(–) Voltage	2.5	V nom	REFIN Refers to Both REFIN1 and REFIN2
REFIN(+) to REFIN(–) Range[2]	1	V min	
	AV_{DD}	V max	
REFIN Common-Mode Range	AGND – 30 mV	V min	
	AV_{DD} + 30 mV	V max	
Reference DC Input Current	0.5	µA/V typ	
Reference DC Input Current Drift	±0.1	nA/V/°C typ	
Normal-Mode Rejection[2]			
@ 50 Hz	100	dB min	50 Hz ± 1 Hz, SF Word = 82
@ 60 Hz	100	dB min	60 Hz ± 1 Hz, SF Word = 68
Common-Mode Rejection			Input Range = ±2.56 V
@ DC	100	dB typ	Analog Input = 1 V. Input Range = ±2.56 V
@ 50 Hz	100	dB typ	
@ 60 Hz	100	dB typ	

Parameter	B Grade	Unit	Test Conditions
AD7708 (CHOP ENABLED)			
Output Update Rate	5.4	Hz min	$\overline{CHOP}$ = 1
	105	Hz max	0.732 ms Increments
No Missing Codes[2]	16	Bits min	20 Hz Update Rate
Resolution	13	Bits p-p	±20 mV Range, 20 Hz Update Rate
	16	Bits p-p	±2.56 V Range, 20 Hz Update Rate
Output Noise and Update Rates	See Tables in ADC Description		
Integral Nonlinearity	±15	ppm of FSR max	2 ppm Typical
Offset Error[3]	±3	µV typ	Calibration is Accurate to ±0.5 LSB
Offset Error Drift vs. Temp[4]	10	nV/°C typ	
Full-Scale Error[3]	±0.75	LSB typ	Includes Positive and Negative ERRORS
Gain Drift vs. Temp[4]	±0.5	ppm/°C typ	
ANALOG INPUTS			
Differential Input Full-Scale Voltage	±1.024 × REFIN/GAIN	V nom	REFIN Refers to Both REFIN1 and REFIN2. REFIN = REFIN(+) REFIN(–) GAIN = 1 to 128
Range Matching	±2	µV typ	Analog Input = 18 mV
Absolute AIN Voltage Limits	AGND + 100 mV	V min	AIN1–AIN10 and AINCOM with
	AV_{DD} – 100 mV	V max	NEGBUF = 1
Absolute AINCOM Voltage Limits	AGND – 30 mV	V min	NEGBUF = 0
	AV_{DD} + 30 mV	V max	
Analog Input Current			AIN1–AIN10 and AINCOM with NEGBUF = 1
DC Input Current[2]	±1	nA max	
DC Input Current Drift	±5	pA/°C typ	
AINCOM Input Current			NEGBUF = 0
DC Input Current[2]	±125	nA/V typ	
DC Bias Current Drift	±2	pA/V/°C typ	
Normal-Mode Rejection[2]			
@ 50 Hz	100	dB min	50 Hz ± 1 Hz, SF Word = 82
@ 60 Hz	94	dB min	60 Hz ± 1 Hz, SF Word = 68
Common-Mode Rejection			
@ DC	90	dB min	100 dB typ, Analog Input = 1 V, Input Range = ±2.56 V 110 dB typ on ±20 mV Range
@ 50 Hz[2]	100	dB min	50 Hz ± 1 Hz, 20 Hz Update Rate
@ 60 Hz[2]	100	dB min	60 Hz ± 1 Hz, 20 Hz Update Rate
REFERENCE INPUTS (REFIN1 AND REFIN2)			
REFIN(+) to REFIN(–) Voltage	2.5 V	nom	REFIN Refers to Both REFIN1 and REFIN2
REFIN(+) to REFIN(–) Range[2]	1	V min	
	AV_{DD}	V max	
REFIN Common-Mode Range	AGND – 30 mV	V min	
	AV_{DD} + 30 mV	V max	
Reference DC Input Current[2]	±0.5	µA/V typ	
Reference DC Input Current Drift	±0.01	nA/V/°C typ	
Normal-Mode Rejection[2]			
@ 50 Hz	100	dB min	50 Hz ± 1 Hz, SF Word = 82
@ 60 Hz	100	dB min	60 Hz ± 1 Hz, SF Word = 68
Common-Mode Rejection			Input Range = ±2.56 V
@ DC	110	dB typ	Analog Input = 1 V
@ 50 Hz	110	dB typ	50 Hz ± 1 Hz, 20 Hz Update Rate
@ 60 Hz	110	dB typ	60 Hz ± 1 Hz, 20 Hz Update Rate
LOGIC INPUTS[5]			
All Inputs Except SCLK and XTAL1[2]			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = 5 V
	0.4	V max	DV_{DD} = 3 V
V_{INH}, Input High Voltage	2.0	V min	DV_{DD} = 3 V or 5 V

AD7708–SPECIFICATIONS[1]

Parameter	B Grade	Unit	Test Conditions
LOGIC INPUTS (Continued)			
SCLK Only (Schmitt-Triggered Input)[2]			
$V_{T(+)}$	1.4/2	V min/V max	DV_{DD} = 5 V
$V_{T(-)}$	0.8/1.4	V min/V max	DV_{DD} = 5 V
$V_{T(+)}–V_{T(-)}$	0.3/0.85	V min/V max	DV_{DD} = 5 V
$V_{T(+)}$	0.95/2	V min/V max	DV_{DD} = 3 V
$V_{T(-)}$	0.4/1.1	V min/V max	DV_{DD} = 3 V
$V_{T(+)}–V_{T(-)}$	0.3/0.85	V min/V max	DV_{DD} = 3 V
XTAL1 Only[2]			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = 5 V
V_{INH}, Input High Voltage	3.5	V min	DV_{DD} = 5 V
V_{INL}, Input Low Voltage	0.4	V max	DV_{DD} = 3 V
V_{INH}, Input High Voltage	2.5	V min	DV_{DD} = 3 V
Input Currents	±10	µA max	Logic Input = DV_{DD}
	–70	µA max	Logic Input = DGND, Typical –40 µA @ 5 V and –20 µA at 3 V
Input Capacitance	10	pF typ	All Digital Inputs
LOGIC OUTPUTS (Excluding XTAL2)[5]			
V_{OH}, Output High Voltage[2]	DV_{DD} – 0.6	V min	DV_{DD} = 3 V, I_{SOURCE} = 100 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	DV_{DD} = 3 V, I_{SINK} = 100 µA
V_{OH}, Output High Voltage[2]	4	V min	DV_{DD} = 5 V, I_{SOURCE} = 200 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	DV_{DD} = 5 V, I_{SINK} = 1.6 mA
Floating State Leakage Current	±10	µA max	
Floating State Output Capacitance	±10	pF typ	
Data Output Coding	Binary		Unipolar Mode
	Offset Binary		Bipolar Mode
SYSTEM CALIBRATION[2]			
Full-Scale Calibration Limit	1.05 × FS	V max	
Zero-Scale Calibration Limit	–1.05 × FS	V min	
Input Span	0.8 × FS	V min	
	2.1 × FS	V max	
START-UP TIME			
From Power-On	300	ms typ	
From Power-Down Mode	1	ms typ	
	300	ms typ	Oscillator Powered Down
POWER REQUIREMENTS			
Power Supply Voltages	AV_{DD} and DV_{DD} can be operated independently of each other.		
AV_{DD}–AGND	2.7/3.6	V min/max	AV_{DD} = 3 V nom
	4.75/5.25	V min/max	AV_{DD} = 5 V nom
DV_{DD}–DGND	2.7/3.6	V min/max	DV_{DD} = 3 V nom
	4.75/5.25	V min	DV_{DD} = 5 V nom
DI_{DD} (Normal Mode)	0.55	mA max	DV_{DD} = 3 V, 0.43 mA typ
	0.65	mA	DV_{DD} = 5 V, 0.5 mA typ
AI_{DD} (Normal Mode)	1.1	mA	AV_{DD} = 3 V or 5 V, 0.85 mA typ
DI_{DD} (Power-Down Mode)	10	µA max	DV_{DD} = 3 V, 32.768 kHz Osc. Running
	2	µA max	DV_{DD} = 3 V, Oscillator Powered Down
	30	µA max	DV_{DD} = 5 V, 32.768 kHz Osc. Running
	8	µA max	DV_{DD} = 5 V, Oscillator Powered Down
AI_{DD} (Power-Down Mode)	1	µA max	AV_{DD} = 3 V or 5 V
Power Supply Rejection (PSR)			Input Range = ±2.56 V, AIN = 1 V
Chop Disabled	70	dB min	95 dB typ
Chop Enabled	100	dB typ	

NOTES

[1]Temperature range is –40°C to +85°C.

[2]Not production tested, guaranteed by design and/or characterization data at release.

[3]Following a self-calibration this error will be in the order of the noise for the programmed gain and update selected. A system calibration will completely remove this error.

[4]Recalibration at any temperature will remove these errors.

[5]I/O Port Logic Levels are with respect to AV_{DD} and AGND.

Specifications are subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (AV_{DD} = 2.7 V to 3.6 V or AV_{DD} = 5 V ± 5%; DV_{DD} = 2.7 V to 3.6 V or DV_{DD} = 5 V ± 5%; AGND = DGND = 0 V; XTAL = 32.768 kHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD} unless otherwise noted.

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Unit	Conditions/Comments
t_1	32.768	kHz typ	Crystal Oscillator Frequency
t_2	50	ns min	$\overline{\text{RESET}}$ Pulsewidth
Read Operation			
t_3	0	ns min	$\overline{\text{RDY}}$ to $\overline{\text{CS}}$ Setup Time
t_4	0	ns min	$\overline{\text{CS}}$ Falling Edge to SCLK Active Edge Setup Time[3]
t_5[4]	0	ns min	SCLK Active Edge to Data Valid Delay[3]
	60	ns max	DV_{DD} = 4.5 V to 5.5 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_{5A}[4, 5]	0	ns min	$\overline{\text{CS}}$ Falling Edge to Data Valid Delay[3]
	60	ns max	DV_{DD} = 4.5 V to 5.5 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_6	100	ns min	SCLK High Pulsewidth
t_7	100	ns min	SCLK Low Pulsewidth
t_8	0	ns min	$\overline{\text{CS}}$ Rising Edge to SCLK Inactive Edge Hold Time[3]
t_9[6]	10	ns min	Bus Relinquish Time after SCLK Inactive Edge[3]
	80	ns max	
t_{10}	100	ns max	SCLK Active Edge to $\overline{\text{RDY}}$ High[3, 7]
Write Operation			
t_{11}	0	ns min	$\overline{\text{CS}}$ Falling Edge to SCLK Active Edge Setup Time[3]
t_{12}	30	ns min	Data Valid to SCLK Edge Setup Time
t_{13}	25	ns min	Data Valid to SCLK Edge Hold Time
t_{14}	100	ns min	SCLK High Pulsewidth
t_{15}	100	ns min	SCLK Low Pulsewidth
t_{16}	0	ns min	$\overline{\text{CS}}$ Rising Edge to SCLK Edge Hold Time

NOTES

[1]Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.

[2]See Figures 1 and 2.

[3]SCLK active edge is falling edge of SCLK.

[4]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

[5]This specification only comes into play if CS goes low while SCLK is low. It is required primarily for interfacing to DSP machines.

[6]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the load circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

[7]$\overline{\text{RDY}}$ returns high after the first read from the device after an output update. The same data can be read again, if required, while $\overline{\text{RDY}}$ is high, although care should be taken that subsequent reads do not occur close to the next output update.

Specifications subject to change without notice.

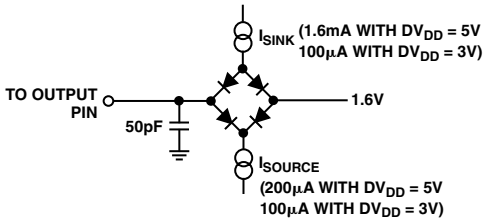


Figure 1. Load Circuit for Timing Characterization

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3 V to +7 V
AV_{DD} to DGND ..... –0.3 V to +7 V
DV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
AGND to DGND ..... –0.05 V to +0.05 V
AV_{DD} to DV_{DD} ..... –5 V to +5 V
Analog Input Voltage to AGND .... –0.3 V to AV_{DD} +0.3 V
Reference Input Voltage to AGND .. –0.3 V to AV_{DD} +0.3 V
Total AIN/REFIN Current (Indefinite) ..... 30 mA
Digital Input Voltage to DGND .... –0.3 V to DV_{DD} +0.3 V
Digital Output Voltage to DGND ... –0.3 V to DV_{DD} +0.3 V
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
SOIC Package
  θ_{JA} Thermal Impedance ..... 71.4°C/W
  θ_{JC} Thermal Impedance ..... 23°C/W
TSSOP Package
  θ_{JA} Thermal Impedance ..... 97.9°C/W
  θ_{JC} Thermal Impedance ..... 14°C/W
Lead Temperature, Soldering
  Vapor Phase (60 sec) ..... 215°C
  Infrared (15 sec) ..... 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7708BR	–40°C to +85°C	SOIC	R-28
AD7708BRU	–40°C to +85°C	TSSOP	RU-28
EVAL-AD7708EB			Evaluation Board
AD7718BR	–40°C to +85°C	SOIC	R-28
AD7718BRU	–40°C to +85°C	TSSOP	RU-28
EVAL-AD7718EB			Evaluation Board

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7708/AD7718 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

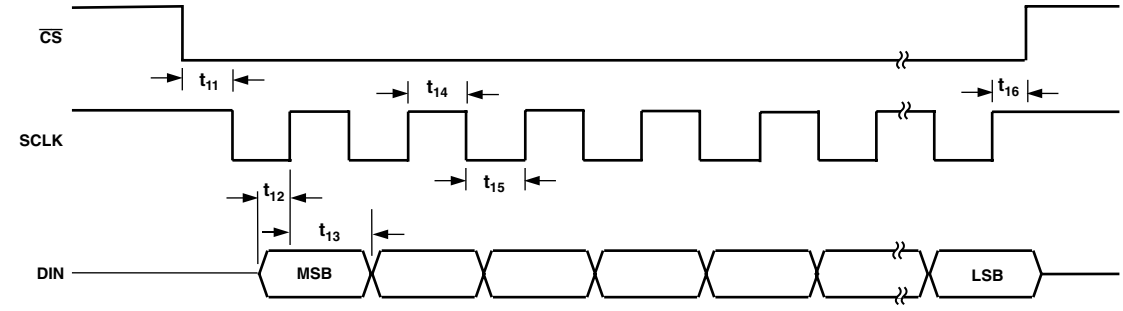


Figure 2. Write Cycle Timing Diagram

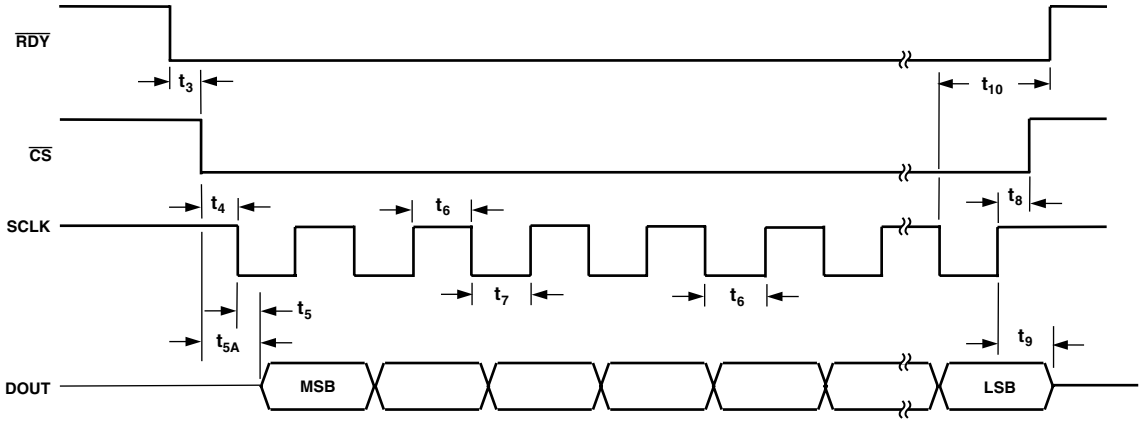


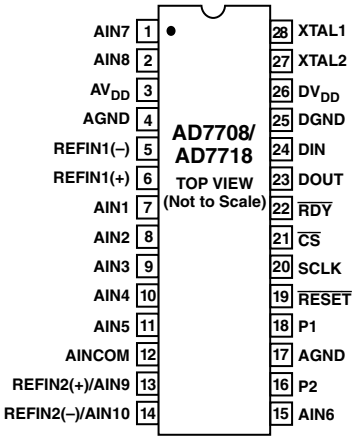
Figure 3. Read Cycle Timing Diagram

PIN FUNCTION DESCRIPTIONS

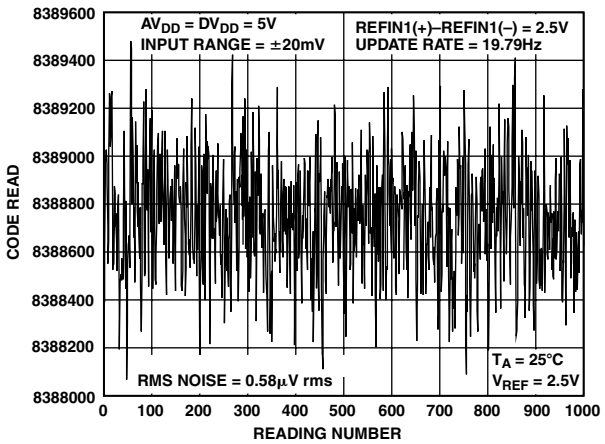
Pin No	Mnemonic	Function
1	AIN7	Analog Input Channel 7. Programmable-gain analog input that can be used as a pseudo-differential input when used with AINCOM, or as the positive input of a fully-differential input pair when used with AIN8. (See ADC Control Register section.)
2	AIN8	Analog Input Channel 8. Programmable-gain analog input that can be used as a pseudo-differential input when used with AINCOM, or as the negative input of a fully-differential input pair when used with AIN7. (See ADC Control Register section.)
3	AV_{DD}	Analog Supply Voltage
4	AGND	Analog Ground
5	REFIN1(–)	Negative Reference Input. This reference input can lie anywhere between AGND and AV_{DD} – 1 V.
6	REFIN1(+)	Positive reference input. REFIN(+) can lie anywhere between AV_{DD} and AGND. The nominal reference voltage [REFIN(+)–REFIN(–)] is 2.5 V but the part is functional with a reference range from 1 V to AV_{DD}.
7	AIN1	Analog Input Channel 1. Programmable-gain analog input that can be used as a pseudo-differential input when used with AINCOM, or as the positive input of a fully-differential input pair when used with AIN2. (See ADC Control Register Section.)
8	AIN2	Analog Input Channel 2. Programmable-gain analog input that can be used as a pseudo-differential input when used with AINCOM, or as the negative input of a fully-differential input pair when used with AIN1. (See ADC Control Register section.)
9	AIN3	Analog Input Channel 3. Programmable-gain analog input that can be used as a pseudo-differential input when used with AINCOM, or as the positive input of a fully-differential input pair when used with AIN4. (See ADC Control Register section.)
10	AIN4	Analog Input Channel 4. Programmable-gain analog input that can be used as a pseudo-differential input when used with AINCOM, or as the negative input of a fully-differential input pair when used with AIN3. (See ADC Control Register section.)
11	AIN5	Analog Input Channel 5. Programmable-gain analog input that can be used as a pseudo-differential input when used with AINCOM, or as the positive input of a fully-differential input pair when used with AIN6. (See ADC Control Register section ADCCON.)
12	AINCOM	All analog inputs are referenced to this input when configured in pseudo-differential input mode.
13	REFIN2(+)/AIN9	Positive reference input/analog input. This input can be configured as a reference input with the same characteristics as REFIN1(+) or as an additional analog input. When configured as an analog input this pin provides a programmable-gain analog input that can be used as a pseudo-differential input when used with AINCOM, or as the positive input of a fully-differential input pair when used with AIN10. (See ADC Control Register section.)
14	REFIN2(–)/AIN10	Negative reference input/analog input. This pin can be configured as a reference or analog input. When configured as a reference input it provides the negative reference input for REFIN2. When configured as an analog input it provides a programmable-gain analog input that can be used as a pseudo-differential input when used with AINCOM, or as the negative input of a fully-differential input pair when used with AIN9. (See ADC Control Register section.)
15	AIN6	Analog Input Channel 6. Programmable-gain analog input that can be used as a pseudo-differential input when used with AINCOM, or as the negative input of a fully-differential input pair when used with AIN5. (See ADC Control Register section.)
16	P2	P2 can act as a general-purpose Input/Output bit referenced between AV_{DD} and AGND. There is a weak pull-up to AV_{DD} internally on this pin.
17	AGND	It is recommended that this pin be tied directly to AGND.
18	P1	P1 can act as a general-purpose Input/Output bit referenced between AV_{DD} and AGND. There is a weak pull-up to AV_{DD} internally on this pin.
19	$\overline{\text{RESET}}$	Digital input used to reset the ADC to its power-on-reset status. This pin has a weak pull-up internally to DV_{DD}.
20	SCLK	Serial clock input for data transfers to and from the ADC. The SCLK has a Schmitt-trigger input making an opto-isolated interface more robust. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the AD7708/AD7718 in smaller batches of data.

Pin No	Mnemonic	Function
21	$\overline{CS}$	Chip Select Input. This is an active low logic input used to select the AD7708/AD7718. $\overline{CS}$ can be used to select the AD7708/AD7718 in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low, allowing the AD7708/AD7718 to be operated in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device.
22	$\overline{RDY}$	$\overline{RDY}$ is a logic low status output from the AD7708/AD7718. $\overline{RDY}$ is low when valid data exists in the data register for the selected channel. This output returns high on completion of a read operation from the data register. If data is not read, $\overline{RDY}$ will return high prior to the next update indicating to the user that a read operation should not be initiated. The $\overline{RDY}$ pin also returns low following the completion of a calibration cycle. $\overline{RDY}$ does not return high after a calibration until the mode bits are written to enabling a new conversion or calibration.
23	DOUT	Serial data output with serial data being read from the output shift register of the ADC. The output shift register can contain data from any of the on-chip data, calibration or control registers.
24	DIN	Serial Data Input with serial data being written to the input shift register on the AD7708/AD7718 Data in this shift register is transferred to the calibration or control registers within the ADC depending on the selection bits of the Communications register.
25	DGND	Ground Reference Point for the Digital Circuitry.
26	DV_{DD}	Digital Supply Voltage, 3 V or 5 V Nominal.
27	XTAL2	Output from the 32 kHz Crystal Oscillator or Resonator Inverter.
28	XTAL1	Input to the 32 kHz Crystal Oscillator or Resonator Inverter.

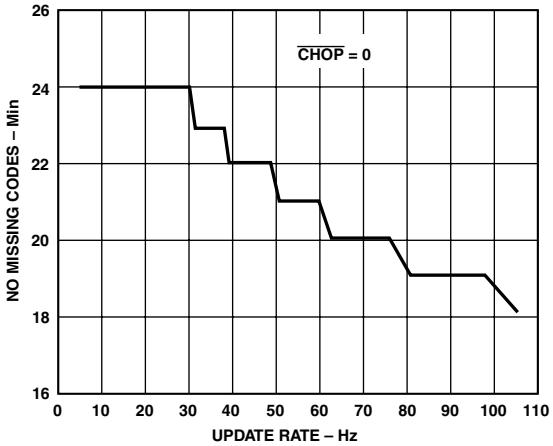
PIN CONFIGURATION



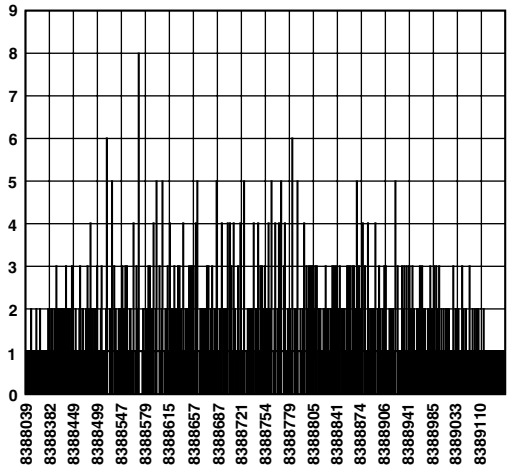
AD7708/AD7718–Typical Performance Characteristics



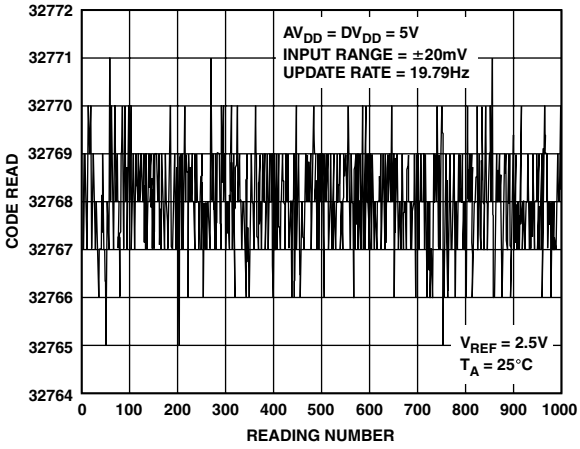
TPC 1. AD7718 Typical Noise Plot on ±20 mV Input Range with 19.79 Hz Update Rate



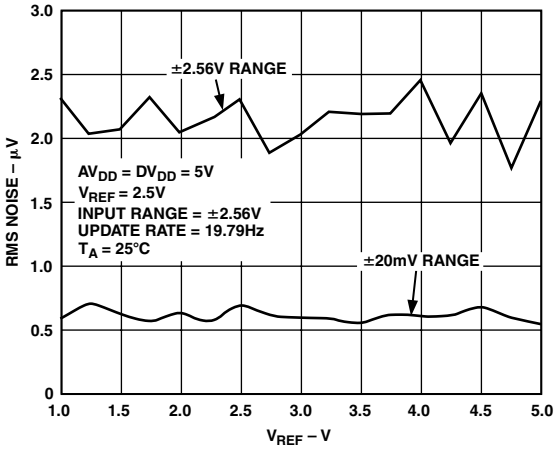
TPC 4. AD7718 No-Missing Codes Performance



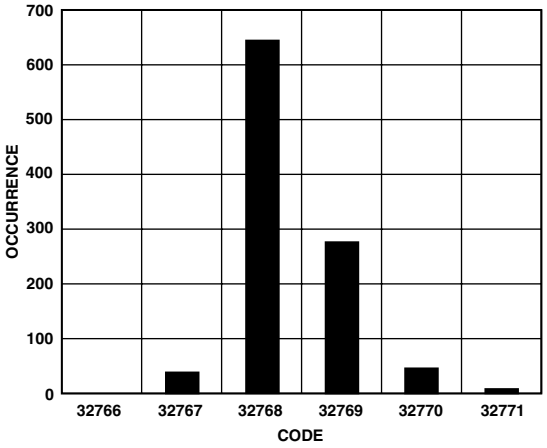
TPC 2. AD7718 Noise Distribution Histogram



TPC 5. AD7708 Typical Noise Plot on ±20 mV Input Range



TPC 3. RMS Noise vs. Reference Input (AD7718 andAD7708)



TPC 6. AD7708 Noise Histogram

ADC CIRCUIT INFORMATION

The AD7708/AD7718 incorporates a 10-channel multiplexer with a sigma-delta ADC, on-chip programmable gain amplifier and digital filtering intended for the measurement of wide dynamic range, low frequency signals such as those in weigh-scale, strain-gauge, pressure transducer, or temperature measurement applications. The AD7708 offers 16-bit resolution while the AD7718 offers 24-bit resolution. The AD7718 is a pin-for-pin compatible version of the AD7708. The AD7718 offers a direct upgradable path from a 16-bit to a 24-bit system without requiring any hardware changes and only minimal software changes.

These parts can be configured as four/five fully-differential input channels or as eight/ten pseudo-differential input channels referenced to AINCOM. The channel is buffered and can be programmed for one of eight input ranges from ±20 mV to ±2.56 V. Buffering the input channel means that the part can handle significant source impedances on the analog input and that R, C filtering (for noise rejection or RFI reduction) can be placed on the analog inputs if required. These input channels are intended to convert signals directly from sensors without the need for external signal conditioning.

The ADC employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The sigma-delta modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A Sinc^3 programmable low-pass filter is then employed to decimate the modulator output data stream to give a valid data conversion result at programmable output rates. The signal chain has two modes of operation, CHOP enabled and CHOP disabled. The $\overline{\text{CHOP}}$ bit in the mode register enables and disables the chopping scheme.

Signal Chain Overview (CHOP Enabled, CHOP = 0)

With CHOP = 0, chopping is enabled, this is the default and gives optimum performance in terms of drift performance. With chopping enabled, the available output rates vary from 5.35 Hz (186.77 ms) to 105.03 Hz (9.52 ms). A block diagram of the ADC input channel with chop enabled is shown in Figure 4.

The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (which results from the analog-to-digital conversion) so that the noise is pushed toward one-half of the modulator frequency. The output of the sigma-delta modulator feeds directly into the digital filter. The digital filter then band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a band limited, low noise output from the AD7708/AD7718 ADC. The AD7708/AD7718 filter is a low-pass, Sinc^3 or (sinx/x)^3 filter whose primary function is to remove the quantization noise introduced at the modulator. The cutoff frequency and decimated output data rate of the filter are programmable via the SF word loaded to the filter register. The complete signal chain is chopped resulting in excellent dc offset and offset drift specifications and is extremely beneficial in applications where drift, noise rejection, and optimum EMI rejection are important factors. With chopping, the ADC repeatedly reverses its inputs. The decimated digital output words from the Sinc^3 filters, therefore, have a positive offset and negative offset term included. As a result, a final summing stage is included so that each output word from the filter is summed and averaged with the previous filter output to produce a new valid output result to be written to the ADC data register. The programming of the Sinc^3 decimation factor is restricted to an 8-bit register SF, the actual decimation factor is the register value times 8. The decimated output rate from the Sinc^3 filter (and the ADC conversion rate) will therefore be

$$f_{ADC} = \frac{1}{3} \times \frac{1}{8 \times SF} \times f_{MOD}$$

where

f_{ADC} in the ADC conversion rate.

SF is the decimal equivalent of the word loaded to the filter register.

f_{MOD} is the modulator sampling rate of 32.768 kHz.

The chop rate of the channel is half the output data rate:

$$f_{CHOP} = \frac{1}{2 \times f_{ADC}}$$

As shown in the block diagram, the Sinc^3 filter outputs alternately contain $+V_{OS}$ and $-V_{OS}$, where V_{OS} is the respective channel offset. This offset is removed by performing a running average of two. This average by two means that the settling time to any change in programming of the ADC will be twice the normal conversion time, while an asynchronous step change on the analog input will not be fully reflected until the third subsequent output.

$$t_{SETTLE} = \frac{2}{f_{ADC}} = 2 \times t_{ADC}$$

The allowable range for SF is 13 to 255 with a default of 69 (45H). The corresponding conversion rates, conversion times, and settling times are shown in Table I. Note that the conversion time increases by 0.732 ms for each increment in SF.

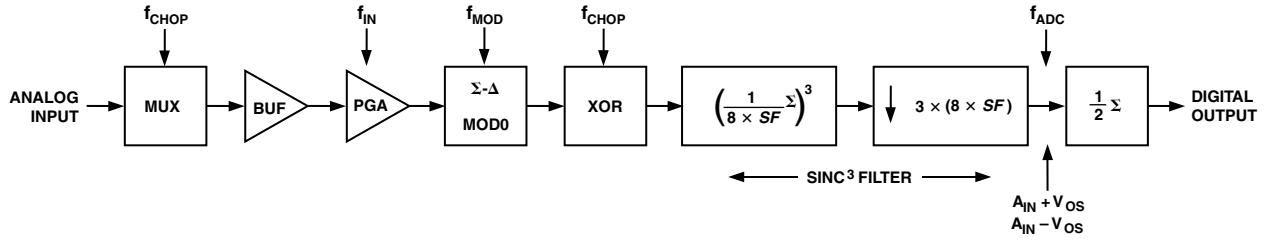


Figure 4. ADC Channel Block Diagram with CHOP Enabled

Table I. ADC Conversion and Settling Times for Various SF Words with $\overline{CHOP}$ = 0

SF Word	Data Update Rate f_{ADC} (Hz)	Settling Time t_{SETTLE} (ms)
13	105.3	19.04
23	59.36	33.69
27	50.56	39.55
45	30.3	65.9
69 (Default)	19.79	101.07
91	15	133.1
182	7.5	266.6
255	5.35	373.54

The overall frequency response is the product of a $sinc^3$ and a sinc response. There are $sinc^3$ notches at integer multiples of $3 \times f_{ADC}$ and there are sinc notches at odd integer multiples of $f_{ADC}/2$. The 3 dB frequency for all values of SF obeys the following equation:

$$f\,(3\ dB) = 0.24 \times f_{ADC}$$

Normal-mode rejection is the major function of the digital filter on the AD7708/AD7718. The normal mode 50 ±1 Hz rejection with an SF word of 82 is typically –100 dB. The 60 ± 1 Hz rejection with SF = 68 is typically –100 dB. Simultaneous 50 Hz and 60 Hz rejection of better than 60 dB is achieved with an SF of 69. Choosing an SF word of 69 places notches at both 50 Hz and 60 Hz. Figures 5 to 9 show the filter rejection for a selection of SF words.

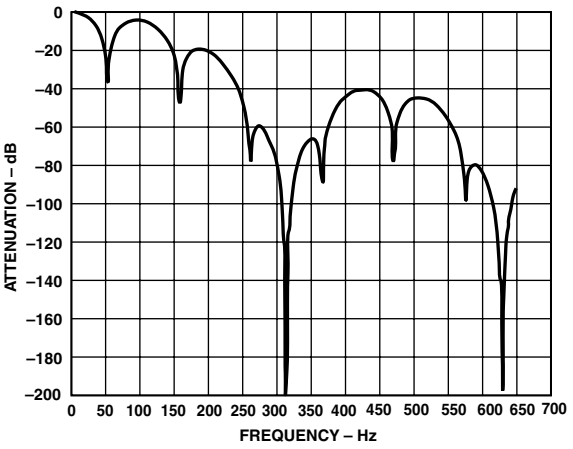
The frequency response of the filter H (f) is as follows:

$$\left(\frac{1}{SF \times 8} \times \frac{\sin\left(SF \times 8 \times \pi \times f/f_{MOD}\right)}{\sin\left(\pi \times f/f_{MOD}\right)}\right)^3 \times \left(\frac{1}{2} \times \frac{\sin\left(2 \times \pi \times f/f_{OUT}\right)}{\sin\left(\pi \times f/f_{OUT}\right)}\right)$$

where

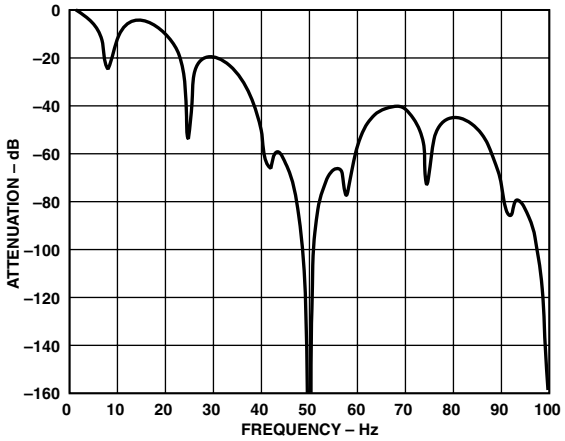
f_{MOD} = 32,768 Hz,
SF = value programmed into SF Register,
$f_{OUT} = f_{MOD}/(SF \times 8 \times 3)$.

The following plots show the filter frequency response for a variety of update rates from 5 Hz to 105 Hz.



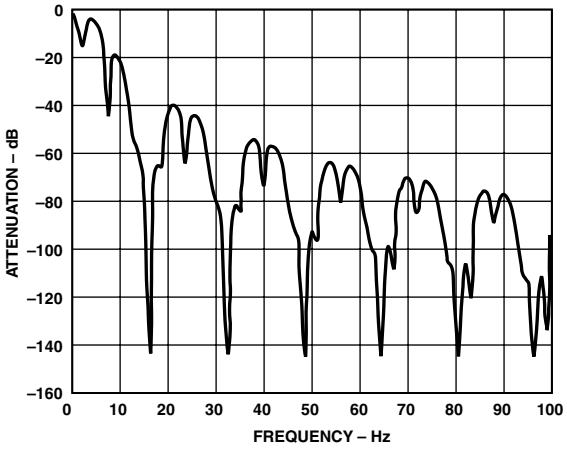
SF = 13
OUTPUT DATA RATE = 105Hz
INPUT BANDWIDTH = 25.2Hz
FIRST NOTCH = 52.5Hz
50Hz REJECTION = –23.6dB, 50Hz±1Hz REJECTION = –20.5dB
60Hz REJECTION = –14.6dB, 60Hz±1Hz REJECTION = –13.6dB

Figure 5. Filter Profile with SF = 13



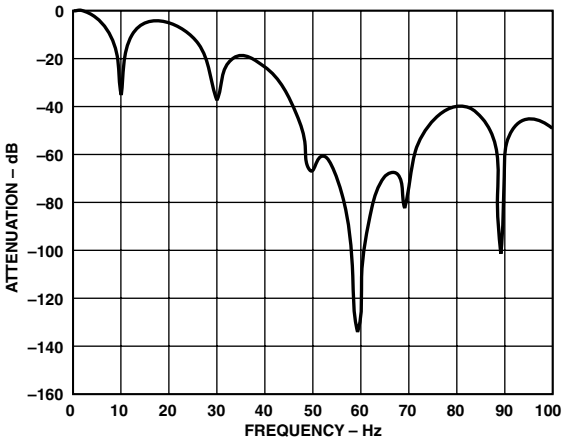
SF = 82
OUTPUT DATA RATE = 16.65Hz
INPUT BANDWIDTH = 4Hz
50Hz REJECTION = –171dB, 50Hz±1Hz REJECTION = –100dB
60Hz REJECTION = –58dB, 60Hz±1Hz REJECTION = –53dB

Figure 6. Filter Profile with SF = 82



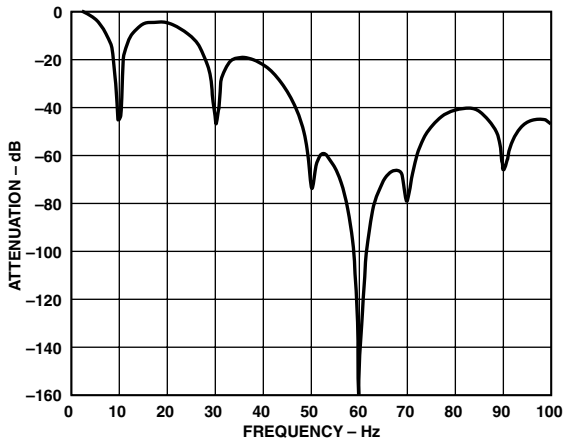
SF = 255
OUTPUT DATA RATE = 5.35Hz
INPUT BANDWIDTH = 1.28Hz
50Hz REJECTION = –93dB, 50Hz±1Hz REJECTION = –93dB
60Hz REJECTION = –74dB, 60Hz±1Hz REJECTION = –68dB

Figure 7. Filter Profile with SF = 255



SF = 69
OUTPUT DATA RATE = 19.8Hz
INPUT BANDWIDTH = 4.74Hz
FIRST NOTCH = 9.9Hz
50Hz REJECTION = –66dB, 50Hz±1Hz REJECTION = –60dB
60Hz REJECTION = –117dB, 60Hz±1Hz REJECTION = –94dB

Figure 8. Filter Profile with Default SF = 69 Giving Filter Notches at Both 50 Hz and 60 Hz



SF = 68
OUTPUT DATA RATE = 20.07Hz
INPUT BANDWIDTH = 4.82Hz
50Hz REJECTION = –74dB, 50Hz±1Hz REJECTION = –54.6dB
60Hz REJECTION = –147dB, 60Hz±1Hz REJECTION = –101dB

Figure 9. Filter Profile with SF = 68

ADC NOISE PERFORMANCE CHOP ENABLED ($\overline{CHOP}$ = 0)

Tables II to V show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for a selection of output update rates. The numbers are typical and generated at a differential input voltage of 0 V with AV_{DD} = DV_{DD} = 5 V and using a 2.5 V reference. The output update rate is selected via the SF7–SF0 bits in the Filter Register. It is important to note that the peak-to-peak resolution figures represent the resolution for which there will be no code flicker within a six-sigma limit. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. Secondly, when the analog input is converted into the digital domain, quantization noise is added. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. The numbers in the tables are given for the bipolar input ranges. For the unipolar ranges the rms noise numbers will be the same as the bipolar range, but the peak-to-peak resolution is now based on half the signal range which effectively means losing one bit of resolution.

Table II. Typical Output RMS Noise vs. Input Range and Update Rate for AD7718 with Chop Enabled ($\overline{CHOP}$ = 0); Output RMS Noise in μV

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	1.50	1.50	1.60	1.75	3.50	4.50	6.70	11.75
23	59.36	1.0	1.02	1.06	1.15	1.22	1.77	3.0	5.08
27	50.56	0.95	0.95	0.98	1.00	1.10	1.66		5.0
69	19.79	0.60	0.65	0.65	0.65	0.65	0.95	1.40	2.30
255	5.35	0.35	0.35	0.37	0.37	0.37	0.51	0.82	1.25

Table III. Peak-to-Peak Resolution vs. Input Range and Update Rate for AD7718 with Chop Enabled ($\overline{CHOP}$ = 0); Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	12	13	14	15	15	15.5	16	16
23	59.36	12.5	13.5	14.5	15	16	17	17	17
27	50.56	12.5	13.5	14.5	15.5	16.5	17	17	17
69	19.79	13	14	15	16	17	17.5	18	18.5
255	5.35	14	15	16	17	18	18.5	18.8	19.2

Table IV. Typical Output RMS Noise vs. Input Range and Update Rate for AD7708 with Chop Enabled ($\overline{CHOP}$ = 0); Output RMS Noise in μV

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	1.50	1.50	1.60	1.75	3.50	4.50	6.70	11.75
23	59.36	1.0	1.02	1.06	1.15	1.22	1.77	3.0	5.08
27	50.56	0.95	0.95	0.98	1.00	1.10	1.66		5.0
69	19.79	0.60	0.65	0.65	0.65	0.65	0.95	1.40	2.30
255	5.35	0.35	0.35	0.37	0.37	0.37	0.51	0.82	1.25

Table V. Peak-to-Peak Resolution vs. Input Range and Update Rate for AD7708 with Chop Enabled ($\overline{CHOP}$ = 0); Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	12	13	14	15	15	15.5	16	16
23	59.35	12.5	13.5	14.5	15	16	16	16	16
27	50.56	12.5	13.5	14.5	15.5	16	16	16	16
69	19.79	13	14	15	16	16	16	16	16
255	5.35	14	15	16	16	16	16	16	16

SIGNAL CHAIN OVERVIEW CHOP DISABLED ($\overline{CHOP}$ = 1)

With $\overline{CHOP}$ =1 chopping is disabled. With chopping disabled the available output rates vary from 16.06 Hz (62.26 ms) to 1365.33 Hz (0.73 ms). The range of applicable SF words is from 3 to 255. When switching between channels with chop disabled, the channel throughput is increased by a factor of two over the case where chop is enabled. When used in multiplexed applications operation with chop disabled will offer the best throughput time when cycling through all channels. The drawback with chop disabled is that the drift performance is degraded and calibration is required following a gain change or significant temperature change. A block diagram of the ADC input channel with chop disabled is shown in Figure 10. The signal chain includes a mux, buffer, PGA, sigma-delta modulator, and digital filter. The modulator bit stream is applied to a Sinc^3 filter. The programming of the Sinc^3 decimation factor is restricted to an 8-bit register SF, the actual decimation factor is the register value times 8. The decimated output rate from the Sinc^3 filter (and the ADC conversion rate) will therefore be:

$$f_{ADC} = \frac{f_{MOD}}{8 \times SF}$$

where

f_{ADC} is the ADC conversion rate,
SF is the decimal equivalent of the word loaded to the filter register, valid range is from 3 to 255,
f_{MOD} is the modulator sampling rate of 32.768 kHz.

The settling time to a step input is governed by the digital filter. A synchronized step change will require a settling time of three times the programmed update rate, a channel change can be treated as a synchronized step change. An unsynchronized step change will require four outputs to reflect the new analog input at its output.

$$t_{SETTLE} = \frac{3}{f_{ADC}} = 3 \times t_{ADC}$$

The allowable range for SF is 3 to 255 with a default of 69 (45H). The corresponding conversion rates, conversion times, and settling times are shown in Table VI. Note that the conversion time increases by 0.245 ms for each increment in SF.

Table VI. ADC Conversion and Settling Times for Various SF Words with $\overline{CHOP}$ = 1

SF Word	Data Update Rate f_{ADC} (Hz)	Settling Time t_{SETTLE} (ms)
03	1365.33	2.20
68	60.2	49.8
69 (Default)	59.36	50.54
75	54.6	54.93
82	49.95	60
151	27.13	110.6
255	16.06	186.76

The frequency response of the digital filter H (f) is as follows:

$$\left(\frac{1}{SF \times 8} \times \frac{\sin(SF \times 8 \times \pi \times f/f_{MOD})}{\sin(\pi \times f/f_{MOD})}\right)^3$$

where

f_{MOD} = 32,768 Hz,
SF = value programmed into SF SFR.

The following shows plots of the filter frequency response using different SF words for output data rates of 16 Hz to 1.36 kHz.

There are sinc^3 notches at integer multiples of the update rate. The 3 dB frequency for all values of SF obeys the following equation:

$$f\,(3\ dB) = 0.262 \times f_{ADC}$$

The following plots show frequency response of the AD7708/AD7718 digital filter for various filter words. The AD7708/AD7718 are targeted at multiplexed applications. One of the key requirements in these applications is to optimize the SF word to obtain the maximum filter rejection at 50 Hz and 60 Hz while minimizing the channel throughput rate. Figure 12 shows the AD7708/AD7718 optimized throughput while maximizing 50 Hz and 60 Hz rejection. This is achieved with an SF word of 75. In Figure 13, by using a higher SF word of 151, 50 Hz and 60 Hz rejection can be maximized at 60 dB with a channel throughput rate of 110 ms. An SF word of 255 gives maximum rejection at both 50 Hz and 60 Hz but the channel throughput rate is restricted to 186 ms as shown in Figure 14.

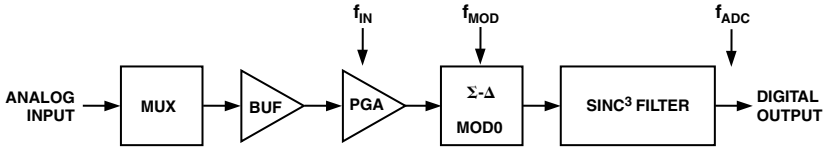
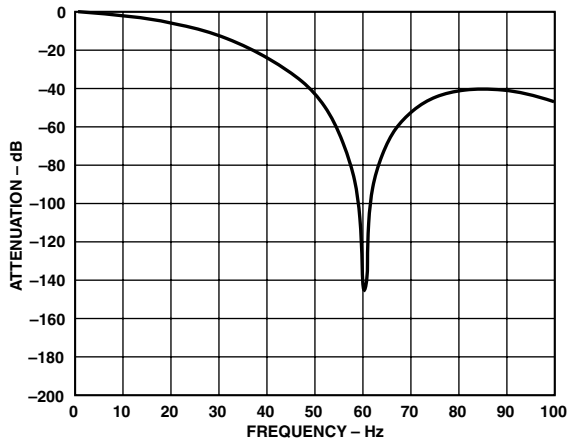
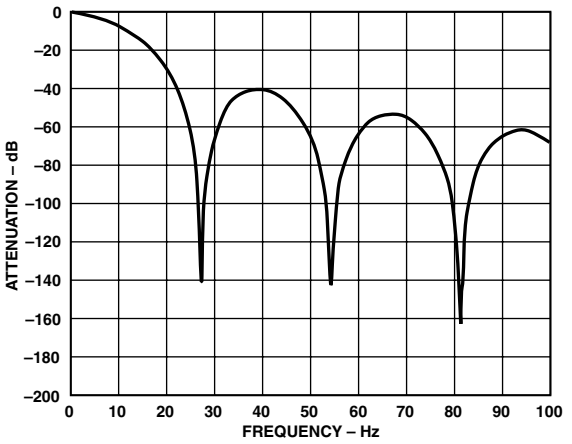


Figure 10. ADC Channel Block Diagram with CHOP Disabled



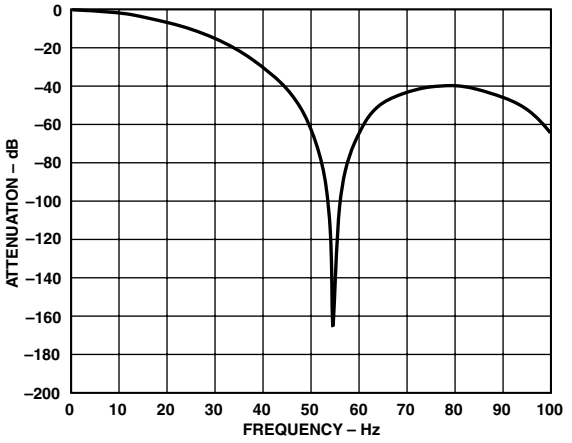
SF = 68
OUTPUT DATA RATE = 60.2Hz
SETTLING TIME = 49.8ms
INPUT BANDWIDTH = 15.5Hz
50Hz REJECTION = –43dB, 50Hz±1Hz REJECTION = –40dB
60Hz REJECTION = –147dB, 60Hz±1Hz REJECTION = –101dB

Figure 11. Frequency Response Operating with the SF Word of 68



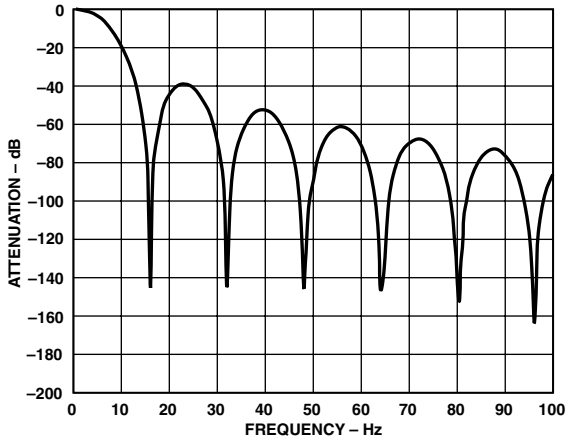
SF = 151
OUTPUT DATA RATE = 27.12Hz
SETTLING TIME = 110ms
INPUT BANDWIDTH = 27.12Hz
50Hz REJECTION = –65.4dB, 50Hz±1Hz REJECTION = –60dB
60Hz REJECTION = –63dB, 60Hz±1Hz REJECTION = –60dB

Figure 13. Optimizing Filter Response for Maximum Simultaneous 50 Hz and 60 Hz Rejection



SF = 75
OUTPUT DATA RATE = 54.6Hz
SETTLING TIME = 55ms
INPUT BANDWIDTH = 14.3Hz
50Hz REJECTION = –62.5dB, 50Hz±1Hz REJECTION = –57dB
60Hz REJECTION = –63dB, 60Hz±1Hz REJECTION = –60dB

Figure 12. Optimizing Filter Response for Throughput while Maximizing the Simultaneous 50 Hz and 60 Hz Rejection



SF = 255
OUTPUT DATA RATE = 16.06Hz
SETTLING TIME = 186ms
INPUT BANDWIDTH = 4.21Hz
50Hz REJECTION = –87dB, 50Hz±1Hz REJECTION = –77dB
60Hz REJECTION = –72dB, 60Hz±1Hz REJECTION = –68dB

Figure 14. Frequency with Maximum SF Word = 255

ADC NOISE PERFORMANCE CHOP DISABLED ($\overline{\text{CHOP}}$ = 1)

Tables VII to X show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for some typical output update rates. The numbers are typical and generated at a differential input voltage of 0 V. The output update rate is selected via the SF7–SF0 bits in the Filter Register. It is important to note that the peak-to-peak resolution figures represent the resolution for which there will be no code flicker within a six-sigma limit. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. Secondly, when the analog input is converted into the digital domain, quantization noise is added. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. The numbers in the tables are given for the bipolar input ranges. For the unipolar ranges the rms noise numbers will be the same as the bipolar range, but the peak-to-peak resolution is now based on half the signal range which effectively means losing 1 bit of resolution.

Table VII. Typical Output RMS Noise vs. Input Range and Update Rate for AD7718 with Chop Disabled ($\overline{CHOP}$ = 1); Output RMS Noise in μV

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
03	1365.33	30.31	29.02	58.33	112.7	282.44	361.72	616.89	1660
13	315.08	2.47	2.49	2.37	3.87	7.18	12.61	16.65	32.45
66	62.06	0.743	0.852	0.9183	0.8788	0.8795	1.29	1.99	3.59
69	59.38	0.961	0.971	0.949	0.922	0.923	1.32	2.03	3.73
81	50.57	0.894	0.872	0.872	0.806	0.793	1.34	2.18	2.96
255	16.06	0.475	0.468	0.434	0.485	0.458	0.688	1.18	1.78

Table VIII. Peak-to-Peak Resolution vs. Input Range and Update Rate for AD7718 with Chop Disabled ($\overline{CHOP}$ = 1); Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
03	1365.33	8	9	9	9	9	9	9	9
13	315.08	11	12	14	14	14	14	15	15
66	62.06	13	14	15	16	17	17	18	18
69	59.36	13	14	15	16	17	17	18	18
81	50.57	13	14	15	16	17	17	18	18
255	16.06	14	15	16	17	18	18	19	19

Table IX. Typical Output RMS Noise vs. Input Range and Update Rate for AD7708 with Chop Disabled ($\overline{CHOP}$ = 1); Output RMS Noise in μV

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
03	1365.33	30.31	29.02	58.33	112.7	282.44	361.72	616.89	1660
13	315.08	2.47	2.49	2.37	3.87	7.18	12.61	16.65	32.45
66	62.06	0.743	0.852	0.9183	0.8788	0.8795	1.29	1.99	3.59
69	59.38	0.961	0.971	0.949	0.922	0.923	1.32	2.03	3.73
81	50.57	0.894	0.872	0.872	0.806	0.793	1.34	2.18	2.96
255	16.06	0.475	0.468	0.434	0.485	0.458	0.688	1.18	1.78

Table X. Peak-to-Peak Resolution vs. Input Range and Update Rate for AD7708 with Chop Disabled ($\overline{CHOP}$ = 1); Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
03	1365.33	8	9	9	9	9	9	9	9
13	315.08	11	12	14	14	14	14	15	15
66	62.06	13	14	15	16	16	16	16	16
69	59.36	13	14	15	16	16	16	16	16
81	50.57	13	14	15	16	16	16	16	16
255	16.06	14	15	16	16	16	16	16	16

ON-CHIP REGISTERS

The AD7708 and AD7718 are controlled and configured via a number of on-chip registers which are shown in Figure 15. The first of these registers is the communications register which is used to control all operations on these converters. All communications with these parts must start with a write to the communications register to specify the next operation to be performed. After a power-on or RESET, the device defaults to waiting for a write to the communications register. The STATUS register contains information pertaining to the operating conditions of the converter. The STATUS register is a read only register. The MODE register is used to configure the conversion mode, calibration, chop enable/disable, reference select, channel configuration and buffered or unbuffered operation on the AINCOM analog input. The MODE register is a read/write register. The ADC Control register is a read/write register used to select the active channel and program its input range and bipolar/unipolar operation. The I/O control register is a read/write register used to configure the operation of the 2-pin I/O port. The filter register is a read/write register used to program the data update rate of the converter. The ADC Data register is a read only register that contains the result of a data conversion on the selected channel. The ADC offset registers are read/write registers that contain the offset calibration data. There are five offset registers, one for each of the fully differential input channels. When configured for pseudo-differential input mode the channels share offset registers. The ADC gain registers are read/write registers that contain the gain calibration data. There are five ADC gain registers, one for each of the fully differential input channels. When configured for pseudo differential input mode the channels share gain registers. The ADC contains Test registers for factory use only, the user is advised not to alter the operating conditions of these registers. The ID register is a read only register and is used for silicon identification purposes. The following sections contains more in-depth detail on all of these registers. In the following descriptions, *SET* implies a Logic 1 state and *CLEARED* implies a Logic 0 state unless otherwise stated.

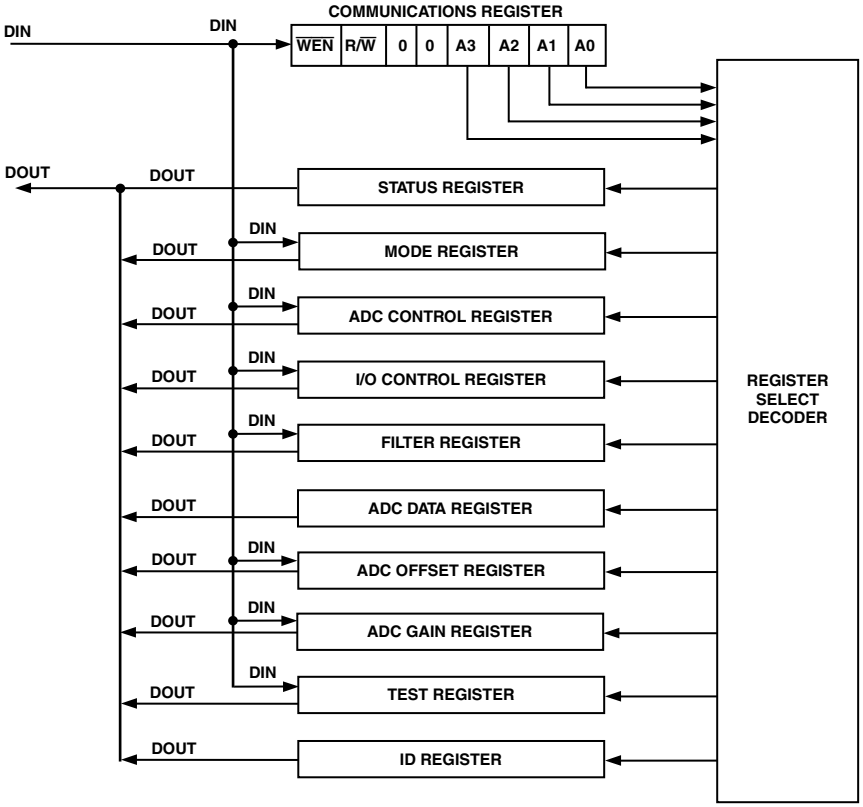


Figure 15. On-Chip Registers

Table XI. Registers—Quick Reference Guide

Register Name	Type	Size	Power-On/Reset Default Value	Function
Communications	Write Only	8 Bits	Not Applicable	All operations to other registers are initiated through the Communications Register. This controls whether subsequent operations are read or write operations and also selects the register for that subsequent operation.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
WEN	R/$\overline{W}$	0(0)	0(0)	A3(0)	A2(0)	A1(0)	A0(0)

Register Name	Type	Size	Power-On/Reset Default Value	Function
Status Register	Read Only	8 Bits	00 Hex	Provides status information on conversions, calibrations and error conditions.

MSB							LSB
RDY	0	CAL	0	ERR	0	0	LOCK

Register Name	Type	Size	Power-On/Reset Default Value	Function
Mode Register	Read/Write	8 Bits	00 Hex	Controls functions such as mode of operation, channel configuration, oscillator operation in power-down.

MSB							LSB
$\overline{CHOP}$	NEGBUF	REFSEL	CHCON	OSCPD	MD2	MD1	MD0

ADC (ADCCON)

Register Name	Type	Size	Power-On/Reset Default Value	Function
Control Register	Read/Write	8 Bits	07 Hex	This register is used to select the active channel input, configure the operating input range, and select unipolar or bipolar operation.

MSB							LSB
CH3	CH2	CH1	CH0	U/$\overline{B}$	RN2	RN1	RN0

I/O (IOCON)

Register Name	Type	Size	Power-On/Reset Default Value	Function
I/O Control Register	Read/Write	8 Bits	00 Hex	This register is used to control and configure the I/O port.

MSB							LSB
0	0	P2DIR	P1DIR	0	0	P2DAT	P1DAT

Register Name	Type	Size	Power-On/Reset Default Value	Function
Filter Register	Read/Write	8 Bits	45 Hex	This register determines the amount of averaging performed by the sinc filter and consequently determines the data update rate of the AD7708/AD7718. The filter register determines the update rate for operation with CHOP enabled and CHOP disabled.

MSB							LSB
SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0

AD7718 ADC (DATA)				
Data Register	Read Only	24 Bits	000000 Hex	Provides the most up-to-date conversion result for the selected channel on the AD7718.
AD7708 (DATA)				
Data Register	Read Only	16 Bits	0000 Hex	Provides the most up-to-date conversion result for the selected channel on the AD7708.

Table XI. Registers—Quick Reference Guide (continued)

Power-On/Reset Register Name	Type	Size	Default Value	Function
AD7718 Offset Register	Read/Write	24 Bits	800 000 Hex	Contains a 24-bit word which is the offset calibration coefficient for the part. The contents of this register are used to provide offset correction on the output from the digital filter. There are five Offset Registers on the part and these are associated with input channels as outlined in the ADCCON register.
AD7718 Gain Register	Read/Write	24 Bits	5XXXX5 Hex	Contains a 24-bit word which is the gain calibration coefficient for the part. The contents of this register are used to provide gain correction on the output from the digital filter. There are five Gain Registers on the part and these are associated with input channels as outlined in the ADCCON register.
AD7708 Offset Register	Read/Write	16 Bits	8000 Hex	Contains a 16-bit word which is the offset calibration coefficient for the part. The contents of this register are used to provide offset correction on the output from the digital filter. There are five Offset Registers on the part and these are associated with input channels as outlined in the ADCCON register.
AD7708 Gain Register	Read/Write	16 Bits	5XXX Hex	Contains a 16-bit word which is the gain calibration coefficient for the part. The contents of this register are used to provide gain correction on the output from the digital filter. There are five Gain Registers on the part and these are associated with input channels as outlined in the ADCCON register.
AD7708 ID Register	Read	8 Bits	5X Hex	Contains an 8-bit byte which is the identifier for the part.
AD7718 ID Register	Read	8 Bits	4X Hex	Contains an 8-bit byte which is the identifier for the part.
Test Registers	Read/Write	16 Bits	0000 Hex	Controls the test modes of the part that are used when testing the part. **The user is advised not to change the contents of these registers.**

Communications Register (A3, A2, A1, A0 = 0, 0, 0, 0)

The Communications Register is an 8-bit write-only register. All communications to the part must start with a write operation to the Communications Register. The data written to the Communications Register determines whether the next operation is a read or write operation, the type of read operation, and on which register this operation takes place. For read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the Communications Register. This is the default state of the interface and, on power-up or after a $\overline{\text{RESET}}$, the AD7708/AD7718 is in this default state waiting for a write operation to the Communications Register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high returns the AD7708/AD7718 to this default state by resetting the part. Table XII outlines the bit designations for the Communications Register. CR0 through CR7 indicate the bit location, CR denoting the bits are in the Communications Register. CR7 denotes the first bit of the data stream.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}$ (0)	R/$\overline{\text{W}}$ (0)	0 (0)	0 (0)	A3 (0)	A2 (0)	A1 (0)	A0 (0)

Table XII. Communications Register Bit Designations

Bit Location	Bit Mnemonic	Description
CR7	$\overline{\text{WEN}}$	Write Enable Bit. A 0 must be written to this bit so the write operation to the Communications Register actually takes place. If a 1 is written to this bit, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a 0 is written to this bit. Once a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits will be loaded to the Communications Register.
CR6	R/$\overline{\text{W}}$	A zero in this bit location indicates that the next operation will be a write to a specified register. A one in this position indicates that the next operation will be a read from the designated register.
CR5	0	A zero must be written to this bit position to ensure correct operation of the AD7708/AD7718.
CR4	0	A zero must be written to this bit position to ensure correct operation of the AD7708/AD7718.
CR3–CR0	A3–A0	Register Address Bits. These address bits are used to select which of the AD7708/AD7718's registers are being accessed during this serial interface communication. A3 is the MSB of the three selection bits.

Table XIII. Register Selection Table

A3	A2	A1	A0	Register
0	0	0	0	Communications Register during a Write Operation
0	0	0	0	Status Register during a Read Operation
0	0	0	1	Mode Register
0	0	1	0	ADC Control Register
0	0	1	1	Filter Register
0	1	0	0	ADC Data Register
0	1	0	1	ADC Offset Register
0	1	1	0	ADC Gain Register
0	1	1	1	I/O Control Register
1	0	0	0	Undefined
1	0	0	1	Undefined
1	0	1	0	Undefined
1	0	1	1	Undefined
1	1	0	0	Test 1 Register
1	1	0	1	Test 2 Register
1	1	1	0	Undefined
1	1	1	1	ID Register