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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Bridge Transducer ADC

AD7730/AD7730L

KEY FEATURES
Resolution of 230,000 Counts (Peak-to-Peak)
Offset Drift: 5 nV/°C
Gain Drift: 2 ppm/°C
Line Frequency Rejection: >150 dB
Buffered Differential Inputs
Programmable Filter Cutoffs
Specified for Drift Over Time
Operates with Reference Voltages of 1 V to 5 V

ADDITIONAL FEATURES
Two-Channel Programmable Gain Front End
On-Chip DAC for Offset/TARE Removal
***FAST*Step™ Mode**
AC or DC Excitation
Single Supply Operation

APPLICATIONS
Weigh Scales
Pressure Measurement

GENERAL DESCRIPTION

The AD7730 is a complete analog front end for weigh-scale and pressure measurement applications. The device accepts low-level signals directly from a transducer and outputs a serial digital word. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by a low pass programmable digital filter, allowing adjustment of filter cutoff, output rate and settling time.

The part features two buffered differential programmable gain analog inputs as well as a differential reference input. The part operates from a single +5 V supply. It accepts four unipolar analog input ranges: 0 mV to +10 mV, +20 mV, +40 mV and +80 mV and four bipolar ranges: ±10 mV, ±20 mV, ±40 mV and ±80 mV. The peak-to-peak resolution achievable directly from the part is 1 in 230,000 counts. An on-chip 6-bit DAC allows the removal of TARE voltages. Clock signals for synchronizing ac excitation of the bridge are also provided.

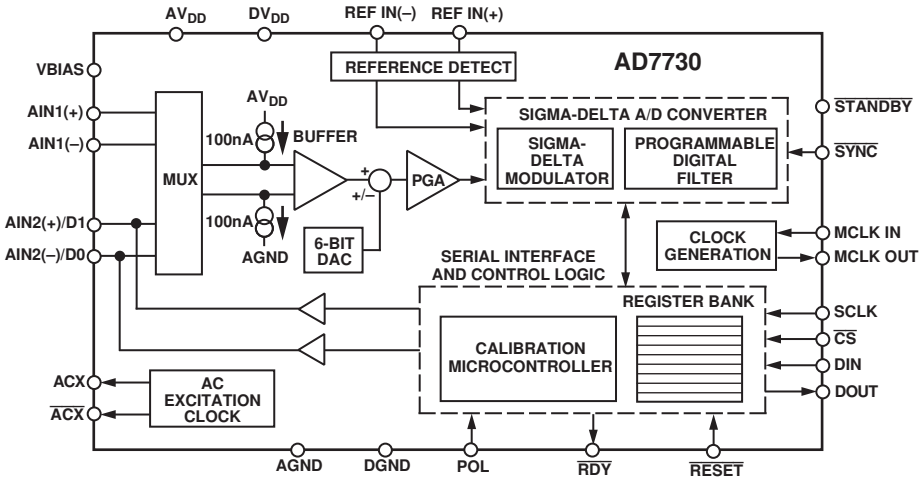
The serial interface on the part can be configured for three-wire operation and is compatible with microcontrollers and digital signal processors. The AD7730 contains self-calibration and system calibration options, and features an offset drift of less than 5 nV/°C and a gain drift of less than 2 ppm/°C.

The AD7730 is available in a 24-pin plastic DIP, a 24-lead SOIC and 24-lead TSSOP package. The AD7730L is available in a 24-lead SOIC and 24-lead TSSOP package.

NOTE

The description of the functions and operation given in this data sheet apply to both the AD7730 and AD7730L. Specifications and performance parameters differ for the parts. Specifications for the AD7730L are outlined in Appendix A.

FUNCTIONAL BLOCK DIAGRAM



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REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/461-3113

AD7730–SPECIFICATIONS

(AV_{DD} = +5 V, DV_{DD} = +3 V or +5 V; REF IN(+) = AV_{DD}; REF IN(–) = AGND = DGND = 0 V; f_{CLKIN} = 4.9152 MHz. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version[1]	Units	Conditions/Comments
STATIC PERFORMANCE (CHP = 1)			
No Missing Codes[2]	24	Bits min	
Output Noise and Update Rates[2]	See Tables I & II		
Integral Nonlinearity	18	ppm of FSR max	
Offset Error[2]	See Note 3		Offset Error and Offset Drift Refer to Both
Offset Drift vs. Temperature[2]	5	nV/°C typ	Unipolar Offset and Bipolar Zero Errors
Offset Drift vs. Time[4]	25	nV/1000 Hours typ	
Positive Full-Scale Error[2, 5]	See Note 3		
Positive Full-Scale Drift vs Temp[2, 6, 7]	2	ppm of FS/°C max	
Positive Full-Scale Drift vs Time[4]	10	ppm of FS/1000 Hours typ	
Gain Error[2, 8]	See Note 3		
Gain Drift vs. Temperature[2, 6, 9]	2	ppm/°C max	
Gain Drift vs. Time[4]	10	ppm/1000 Hours typ	
Bipolar Negative Full-Scale Error[2]	See Note 3		
Negative Full-Scale Drift vs. Temp[2, 6]	2	ppm of FS/°C max	
Power Supply Rejection	120	dB typ	Measured with Zero Differential Voltage
Common-Mode Rejection (CMR)	120	dB min	At DC. Measured with Zero Differential Voltage
Analog Input DC Bias Current[2]	50	nA max	
Analog Input DC Bias Current Drift[2]	100	pA/°C typ	
Analog Input DC Offset Current[2]	10	nA max	
Analog Input DC Offset Current Drift[2]	50	pA/°C typ	
STATIC PERFORMANCE (CHP = 0)[2]			
No Missing Codes	24	Bits min	SKIP = 0[10]
Output Noise and Update Rates	See Tables III & IV		
Integral Nonlinearity	18	ppm of FSR max	
Offset Error	See Note 3		Offset Error and Offset Drift Refer to Both
Offset Drift vs. Temperature[6]	0.5	µV/°C typ	Unipolar Offset and Bipolar Zero Errors
Offset Drift vs. Time[4]	2.5	µV/1000 Hours typ	
Positive Full-Scale Error[5]	See Note 3		
Positive Full-Scale Drift vs. Temp[6, 7]	0.6	µV/°C typ	
Positive Full-Scale Drift vs. Time[4]	3	µV/1000 Hours typ	
Gain Error[8]	See Note 3		
Gain Drift vs. Temperature[6, 9]	2	ppm/°C typ	
Gain Drift vs. Time[4]	10	ppm/1000 Hours typ	
Bipolar Negative Full-Scale Error	See Note 3		
Negative Full-Scale Drift vs. Temp	0.6	µV/°C typ	
Power Supply Rejection	90	dB typ	Measured with Zero Differential Voltage
Common-Mode Rejection (CMR) on AIN	100	dB typ	At DC. Measured with Zero Differential Voltage
CMR on REF IN	120	dB typ	At DC. Measured with Zero Differential Voltage
Analog Input DC Bias Current	60	nA max	
Analog Input DC Bias Current Drift	150	pA/°C typ	
Analog Input DC Offset Current	30	nA max	
Analog Input DC Offset Current Drift	100	pA/°C typ	
ANALOG INPUTS/REFERENCE INPUTS			
Normal-Mode 50 Hz Rejection[2]	88	dB min	From 49 Hz to 51 Hz
Normal-Mode 60 Hz Rejection[2]	88	dB min	From 59 Hz to 61 Hz
Common-Mode 50 Hz Rejection[2]	120	dB min	From 49 Hz to 51 Hz
Common-Mode 60 Hz Rejection[2]	120	dB min	From 59 Hz to 61 Hz
Analog Inputs			
Differential Input Voltage Ranges[11]			Assuming 2.5 V or 5 V Reference with HIREF Bit Set Appropriately
	0 to +10 or ±10	mV nom	Gain = 250
	0 to +20 or ±20	mV nom	Gain = 125
	0 to +40 or ±40	mV nom	Gain = 62.5
	0 to +80 or ±80	mV nom	Gain = 31.25
Absolute/Common-Mode Voltage[12]	AGND + 1.2 V	V min	
	AV_{DD} – 0.95 V	V max	
Reference Input			
REF IN(+) – REF IN(–) Voltage	+2.5	V nom	HIREF Bit of Mode Register = 0
REF IN(+) – REF IN(–) Voltage	+5	V nom	HIREF Bit of Mode Register = 1
Absolute/Common-Mode Voltage[13]	AGND – 30 mV	V min	
	AV_{DD} + 30 mV	V max	
NO REF Trigger Voltage	0.3	V min	NO REF Bit Active If V_{REF} Below This Voltage
	0.65	V max	NO REF Bit Inactive If V_{REF} Above This Voltage

Parameter	B Version[1]	Units	Conditions/Comments
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs Except SCLK and MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = +5 V
V_{INL}, Input Low Voltage	0.4	V max	DV_{DD} = +3 V
V_{INH}, Input High Voltage	2.0	V min	
SCLK Only (Schmitt Triggered Input)			
V_{T+}	1.4/3	V min to V max	DV_{DD} = +5 V
V_{T+}	1/2.5	V min to V max	DV_{DD} = +3 V
V_{T-}	0.8/1.4	V min to V max	DV_{DD} = +5 V
V_{T-}	0.4/1.1	V min to V max	DV_{DD} = +3 V
$V_{T+} - V_{T-}$	0.4/0.8	V min to V max	DV_{DD} = +5 V
$V_{T+} - V_{T-}$	0.4/0.8	V min to V max	DV_{DD} = +3 V
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = +5 V
V_{INL}, Input Low Voltage	0.4	V max	DV_{DD} = +3 V
V_{INH}, Input High Voltage	3.5	V min	DV_{DD} = +5 V
V_{INH}, Input High Voltage	2.5	V min	DV_{DD} = +3 V
LOGIC OUTPUTS (Including MCLK OUT)			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 800 μA Except for MCLK OUT[14]; V_{DD}[15] = +5 V
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 100 μA Except for MCLK OUT[14]; V_{DD}[15] = +3 V
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 200 μA Except for MCLK OUT[14]; V_{DD}[15] = +5 V
V_{OH}, Output High Voltage	V_{DD} – 0.6 V	V min	I_{SOURCE} = 100 μA Except for MCLK OUT[14]; V_{DD}[15] = +3 V
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[2]	6	pF typ	
TRANSDUCER BURNOUT			
AIN1(+) Current	–100	nA nom	
AIN1(–) Current	100	nA nom	
Initial Tolerance @ 25°C	±10	% typ	
Drift[2]	0.1	%/°C typ	
OFFSET (TARE) DAC			
Resolution	6	Bit	
LSB Size	2.3/2.6	mV min/mV max	2.5 mV Nominal with 5 V Reference (REF IN/2000)
DAC Drift[16]	2.5	ppm/°C max	
DAC Drift vs. Time[4, 16]	25	ppm/1000 Hours typ	
Differential Linearity	–0.25/+0.75	LSB max	Guaranteed Monotonic
SYSTEM CALIBRATION			
Positive Full-Scale Calibration Limit[17]	1.05 × FS	V max	FS Is the Nominal Full-Scale Voltage (10 mV, 20 mV, 40 mV or 80 mV)
Negative Full-Scale Calibration Limit[17]	–1.05 × FS	V max	
Offset Calibration Limit[18]	–1.05 × FS	V max	
Input Span[17]	0.8 × FS	V min	
	2.1 × FS	V max	
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} – AGND Voltage	+4.75 to +5.25	V min to V max	
DV_{DD} Voltage	+2.7 to +5.25	V min to V max	With AGND = 0 V
Power Supply Currents			External MCLK. Digital I/Ps = 0 V or DV_{DD}
AV_{DD} Current (Normal Mode)	10.3	mA max	All Input Ranges Except 0 mV to +10 mV and ±10 mV
AV_{DD} Current (Normal Mode)	22.3	mA max	Input Ranges of 0 mV to +10 mV and ±10 mV Only
DV_{DD} Current (Normal Mode)	1.3	mA max	DV_{DD} of 2.7 V to 3.3 V
DV_{DD} Current (Normal Mode)	2.7	mA max	DV_{DD} of 4.75 V to 5.25 V
AV_{DD} + DV_{DD} Current (Standby Mode)	25	μA max	Typically 10 μA. External MCLK IN = 0 V or DV_{DD}
Power Dissipation			AV_{DD} = DV_{DD} = +5 V. Digital I/Ps = 0 V or DV_{DD}
Normal Mode	65	mW max	All Input Ranges Except 0 mV to +10 mV and ±10 mV
	125	mW max	Input Ranges of 0 mV to +10 mV and ±10 mV Only
Standby Mode	125	μW max	Typically 50 μW. External MCLK IN = 0 V or DV_{DD}

NOTES
[1]Temperature range: –40°C to +85°C.
[2]Sample tested during initial release.
[3]The offset (or zero) numbers with CHP = 1 are typically 3 µV precalibration. Internal zero-scale calibration reduces this by about 1 µV. Offset numbers with CHP = 0 can be up to 1 mV precalibration. Internal zero-scale calibration reduces this to 2 µV typical. System zero-scale calibration reduces offset numbers with CHP = 1 and CHP = 0 to the order of the noise. Gain errors can be up to 3000 ppm precalibration with CHP = 0 and CHP = 1. Performing internal full-scale calibrations on the 80 mV range reduces the gain error to less than 100 ppm for the 80 mV and 40 mV ranges, to about 250 ppm for the 20 mV range and to about 500 ppm on the 10 mV range. System full-scale calibration reduces this to the order of the noise. Positive and negative full-scale errors can be calculated from the offset and gain errors.
[4]These numbers are generated during life testing of the part.
[5]Positive Full-Scale Error includes Offset Errors (Unipolar Offset Error or Bipolar Zero Error) and applies to both unipolar and bipolar input ranges. See Terminology.
[6]Recalibration at any temperature will remove these errors.
[7]Full-Scale Drift includes Offset Drift (Unipolar Offset Drift or Bipolar Zero Drift) and applies to both unipolar and bipolar input ranges.
[8]Gain Error is a measure of the difference between the measured and the ideal span between any two points in the transfer function. The two points used to calculate the gain error are positive full scale and negative full scale. See Terminology.
[9]Gain Error Drift is a span drift and is effectively the drift of the part if zero-scale calibrations only were performed.
[10]No Missing Codes performance with CHP = 0 and SKIP = 1 is reduced below 24 bits for SF words lower than 180 decimal.
[11]The analog input voltage range on the AIN1(+) and AIN2(+) inputs is given here with respect to the voltage on the AIN1(–) and AIN2(–) inputs respectively.
[12]The common-mode voltage range on the input pairs applies provided the absolute input voltage specification is obeyed.
[13]The common-mode voltage range on the reference input pair (REF IN(+) and REF IN(–)) applies provided the absolute input voltage specification is obeyed.
[14]These logic output levels apply to the MCLK OUT output only when it is loaded with a single CMOS load.
[15]V_{DD} refers to DV_{DD} for all logic outputs expect D0, D1, ACX and $\overline{ACX}$ where it refers to AV_{DD}. In other words, the output logic high for these four outputs is determined by AV_{DD}.
[16]This number represents the total drift of the channel with a zero input and the DAC output near full scale.
[17]After calibration, if the input voltage exceeds positive full scale, the converter will output all 1s. If the input is less than negative full scale, the device outputs all 0s.
[18]These calibration and span limits apply provided the absolute input voltage specification is obeyed. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (AV_{DD} = +4.75 V to +5.25 V; DV_{DD} = +2.7 V to +5.25 V; AGND = DGND = 0 V; $f_{CLK\,IN}$ = 4.9152 MHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD} unless otherwise noted).

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Units	Conditions/Comments
Master Clock Range	1	MHz min	For Specified Performance
	5	MHz max	
t_1	50	ns min	$\overline{SYNC}$ Pulsewidth
t_2	50	ns min	$\overline{RESET}$ Pulsewidth
Read Operation			
t_3	0	ns min	$\overline{RDY}$ to $\overline{CS}$ Setup Time
t_4	0	ns min	$\overline{CS}$ Falling Edge to SCLK Active Edge Setup Time[3]
t_5[4]	0	ns min	SCLK Active Edge to Data Valid Delay[3]
	60	ns max	DV_{DD} = +4.75 V to +5.25 V
	80	ns max	DV_{DD} = +2.75 V to +3.3 V
t_{5A}[4, 5]	0	ns min	$\overline{CS}$ Falling Edge to Data Valid Delay
	60	ns max	DV_{DD} = +4.75 V to +5.25 V
	80	ns max	DV_{DD} = +2.7 V to +3.3 V
t_6	100	ns min	SCLK High Pulsewidth
t_7	100	ns min	SCLK Low Pulsewidth
t_8	0	ns min	$\overline{CS}$ Rising Edge to SCLK Inactive Edge Hold Time[3]
t_9[6]	10	ns min	Bus Relinquish Time after SCLK Inactive Edge[3]
	80	ns max	
t_{10}	100	ns max	SCLK Active Edge to $\overline{RDY}$ High[3, 7]
Write Operation			
t_{11}	0	ns min	$\overline{CS}$ Falling Edge to SCLK Active Edge Setup Time[3]
t_{12}	30	ns min	Data Valid to SCLK Edge Setup Time
t_{13}	25	ns min	Data Valid to SCLK Edge Hold Time
t_{14}	100	ns min	SCLK High Pulsewidth
t_{15}	100	ns min	SCLK Low Pulsewidth
t_{16}	0	ns min	$\overline{CS}$ Rising Edge to SCLK Edge Hold Time

NOTES
[1]Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.
[2]See Figures 18 and 19.
[3]SCLK active edge is falling edge of SCLK with POL = 1; SCLK active edge is rising edge of SCLK with POL = 0.
[4]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[5]This specification only comes into play if $\overline{CS}$ goes low while SCLK is low (POL = 1) or if $\overline{CS}$ goes low while SCLK is high (POL = 0). It is primarily required for interfacing to DSP machines.
[6]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.
[7]$\overline{RDY}$ returns high after the first read from the device after an output update. The same data can be read again, if required, while $\overline{RDY}$ is high, although care should be taken that subsequent reads do not occur close to the next output update.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3 V to +7 V
AV_{DD} to DGND ..... –0.3 V to +7 V
DV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
AGND to DGND ..... –5 V to +0.3 V
AV_{DD} to DV_{DD} ..... –2 V to +5 V
Analog Input Voltage to AGND .... –0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND .. –0.3 V to AV_{DD} + 0.3 V
AIN/REF IN Current (Indefinite) ..... 30 mA
Digital Input Voltage to DGND .... –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND ... –0.3 V to DV_{DD} + 0.3 V
Output Voltage (ACX, $\overline{ACX}$, D0, D1) to DGND
..... –0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Plastic DIP Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 105°C/W
Lead Temperature (Soldering, 10 sec) ..... +260°C
TSSOP Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 128°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C
SOIC Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

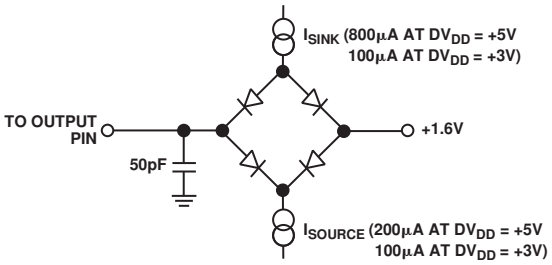


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7730 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

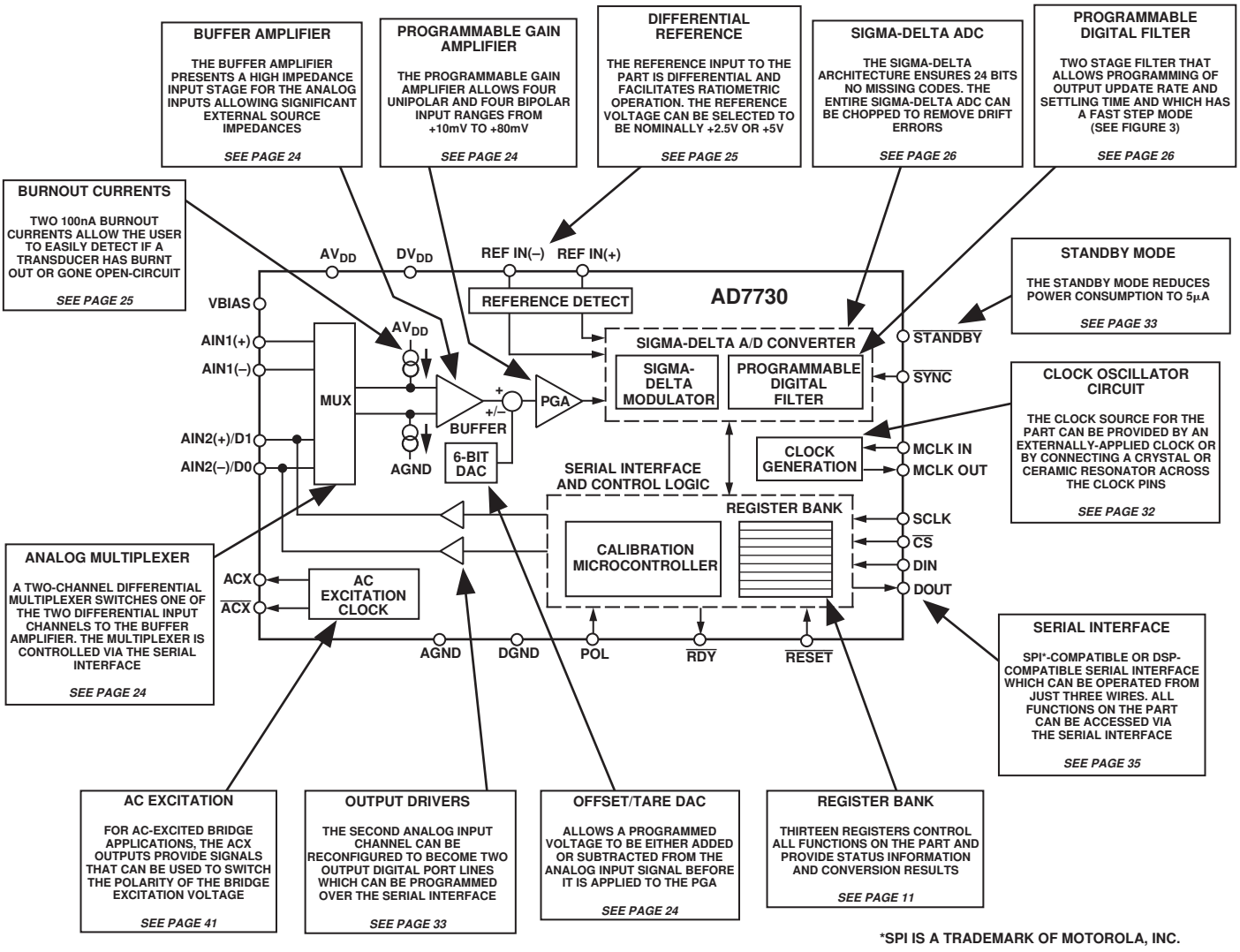


Figure 2. Detailed Functional Block Diagram

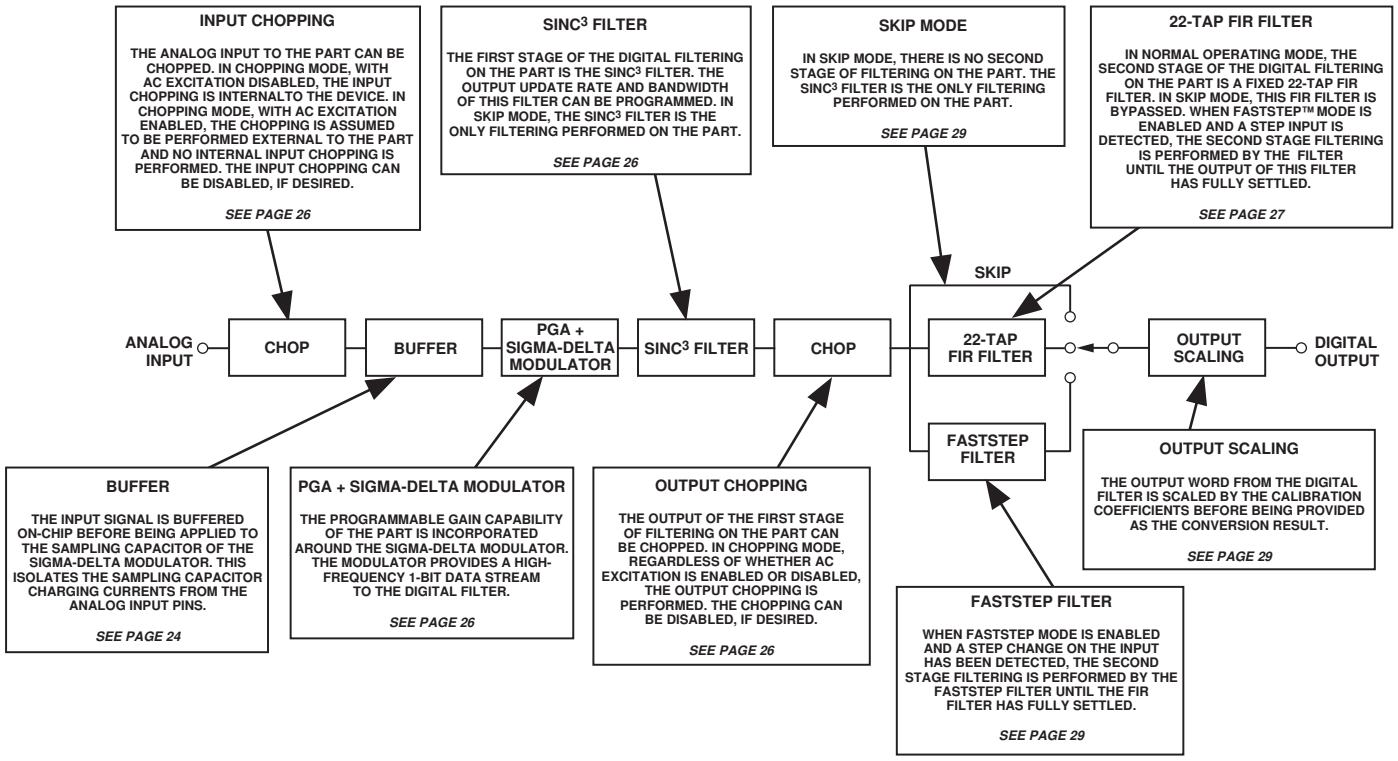
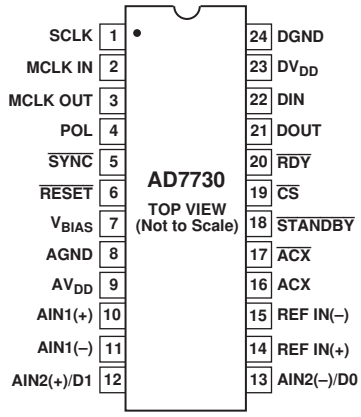


Figure 3. Signal Processing Chain

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	SCLK	Serial Clock. Schmitt-Triggered Logic Input. An external serial clock is applied to this input to transfer serial data to or from the AD7730. This serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the AD7730 in smaller batches of data.
2	MCLK IN	Master Clock signal for the device. This can be provided in the form of a crystal/resonator or external clock. A crystal/resonator can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The AD7730 is specified with a clock input frequency of 4.9152 MHz while the AD7730L is specified with a clock input frequency of 2.4576 MHz.

Pin No.	Mnemonic	Function
3	MCLK OUT	When the master clock for the device is a crystal/resonator, the crystal/resonator is connected between MCLK IN and MCLK OUT. If an external clock is applied to the MCLK IN, MCLK OUT provides an inverted clock signal. This clock can be used to provide a clock source for external circuits and MCLK OUT is capable of driving one CMOS load. If the user does not require it, MCLK OUT can be turned off with the CLKDIS bit of the Mode Register. This ensures that the part is not burning unnecessary power driving capacitance on the MCLK OUT pin.
4	POL	Clock Polarity. Logic Input. This determines the polarity of the serial clock. If the active edge for the processor is a high-to-low SCLK transition, this input should be low. In this mode, the AD7730 puts out data on the DATA OUT line in a read operation on a low-to-high transition of SCLK and clocks in data from the DATA IN line in a write operation on a high-to-low transition of SCLK. In applications with a noncontinuous serial clock (such as most microcontroller applications), this means that the serial clock should idle low between data transfers. If the active edge for the processor is a low-to-high SCLK transition, this input should be high. In this mode, the AD7730 puts out data on the DATA OUT line in a read operation on a high-to-low transition of SCLK and clocks in data from the DATA IN line in a write operation on a low-to-high transition of SCLK. In applications with a noncontinuous serial clock (such as most microcontroller applications), this means that the serial clock should idle high between data transfers.
5	$\overline{\text{SYNC}}$	Logic Input that allows for synchronization of the digital filters and analog modulators when using a number of AD7730s. While $\overline{\text{SYNC}}$ is low, the nodes of the digital filter, the filter control logic and the calibration control logic are reset and the analog modulator is also held in its reset state. $\overline{\text{SYNC}}$ does not affect the digital interface but does reset $\overline{\text{RDY}}$ to a high state if it is low. While $\overline{\text{SYNC}}$ is asserted, the Mode Bits may be set up for a subsequent operation which will commence when the $\overline{\text{SYNC}}$ pin is deasserted.
6	$\overline{\text{RESET}}$	Logic Input. Active low input that resets the control logic, interface logic, digital filter, analog modulator and all on-chip registers of the part to power-on status. Effectively, everything on the part except for the clock oscillator is reset when the $\overline{\text{RESET}}$ pin is exercised.
7	V_{BIAS}	Analog Output. This analog output is an internally-generated voltage used as an internal operating bias point. This output is not for use external to the AD7730 and it is recommended that the user does not connect anything to this pin.
8	AGND	Ground reference point for analog circuitry.
9	AV_{DD}	Analog Positive Supply Voltage. The AV_{DD} to AGND differential is 5 V nominal.
10	AIN1(+)	Analog Input Channel 1. Positive input of the differential, programmable-gain primary analog input pair. The differential analog input ranges are 0 mV to +10 mV, 0 mV to +20 mV, 0 mV to +40 mV and 0 mV to +80 mV in unipolar mode, and ±10 mV, ±20 mV, ±40 mV and ±80 mV in bipolar mode.
11	AIN1(–)	Analog Input Channel 1. Negative input of the differential, programmable gain primary analog input pair.
12	AIN2(+)/D1	Analog Input Channel 2 or Digital Output 1. This pin can be used either as part of a second analog input channel or as a digital output bit as determined by the DEN bit of the Mode Register. When selected as an analog input, it is the positive input of the differential, programmable-gain secondary analog input pair. The analog input ranges are 0 mV to +10 mV, 0 mV to +20 mV, 0 mV to +40 mV and 0 mV to +80 mV in unipolar mode and ±10 mV, ±20 mV, ±40 mV and ±80 mV in bipolar mode. When selected as a digital output, this output can programmed over the serial interface using bit D1 of the Mode Register.
13	AIN2(–)/D0	Analog Input Channel 2 or Digital Output 0. This pin can be used either as part of a second analog input channel or as a digital output bit as determined by the DEN bit of the Mode Register. When selected as an analog input, it is the negative input of the differential, programmable-gain secondary analog input pair. When selected as a digital output, this output can programmed over the serial interface using bit D0 of the Mode Register.
14	REF IN(+)	Reference Input. Positive terminal of the differential reference input to the AD7730. REF IN(+) can lie anywhere between AV_{DD} and AGND. The nominal reference voltage (the differential voltage between REF IN(+) and REF IN(–)) should be +5 V when the HIREF bit of the Mode Register is 1 and +2.5 V when the HIREF bit of the Mode Register is 0.
15	REF IN(–)	Reference Input. Negative terminal of the differential reference input to the AD7730. The REF IN(–) potential can lie anywhere between AV_{DD} and AGND.
16	ACX	Digital Output. Provides a signal that can be used to control the reversing of the bridge excitation in ac-excited bridge applications. When ACX is high, the bridge excitation is taken as normal and when ACX is low, the bridge excitation is reversed (chopped). If AC = 0 (ac mode turned off) or CHP = 0 (chop mode turned off), the ACX output remains high.
17	$\overline{\text{ACX}}$	Digital Output. Provides a signal that can be used to control the reversing of the bridge excitation in ac-excited bridge applications. This output is the complement of ACX. In ac mode, this means that it toggles in anti-phase with ACX . If AC = 0 (ac mode turned off) or CHP = 0 (chop mode turned off), the $\overline{\text{ACX}}$ output remains low. When toggling, it is guaranteed to be nonoverlapping with ACX. The non-overlap interval, when both ACX and $\overline{\text{ACX}}$ are low, is one master clock cycle.

Pin No.	Mnemonic	Function
18	$\overline{\text{STANDBY}}$	Logic Input. Taking this pin low shuts down the analog and digital circuitry, reducing current consumption to the 5 μA range. The on-chip registers retain all their values when the part is in standby mode.
19	$\overline{\text{CS}}$	Chip Select. Active low Logic Input used to select the AD7730. With this input hardwired low, the AD7730 can operate in its three-wire interface mode with SCLK, DIN and DOUT used to interface to the device. $\overline{\text{CS}}$ can be used to select the device in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the AD7730.
20	$\overline{\text{RDY}}$	Logic Output. Used as a status output in both conversion mode and calibration mode. In conversion mode, a logic low on this output indicates that a new output word is available from the AD7730 data register. The $\overline{\text{RDY}}$ pin will return high upon completion of a read operation of a full output word. If no data read has taken place after an output update, the $\overline{\text{RDY}}$ line will return high prior to the next output update, remain high while the update is taking place and return low again. This gives an indication of when a read operation should not be initiated to avoid initiating a read from the data register as it is being updated. In calibration mode, $\overline{\text{RDY}}$ goes high when calibration is initiated and it returns low to indicate that calibration is complete. A number of different events on the AD7730 set the $\overline{\text{RDY}}$ high and these are outlined in Table XVIII.
21	DOUT	Serial Data Output with serial data being read from the output shift register on the part. This output shift register can contain information from the calibration registers, mode register, status register, filter register, DAC register or data register, depending on the register selection bits of the Communications Register.
22	DIN	Serial Data Input with serial data being written to the input shift register on the part. Data from this input shift register is transferred to the calibration registers, mode register, communications register, DAC register or filter registers depending on the register selection bits of the Communications Register.
23	DV_{DD}	Digital Supply Voltage, +3 V or +5 V nominal.
24	DGND	Ground reference point for digital circuitry.

TERMINOLOGY

INTEGRAL NONLINEARITY

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

POSITIVE FULL-SCALE ERROR

Positive Full-Scale Error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal AIN(+) voltage (AIN(–) + V_{REF}/GAIN – 3/2 LSBs). It applies to both unipolar and bipolar analog input ranges. Positive full-scale error is a summation of offset error and gain error.

UNIPOLAR OFFSET ERROR

Unipolar Offset Error is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(–) + 0.5 LSB) when operating in the unipolar mode.

BIPOLAR ZERO ERROR

This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal AIN(+) voltage (AIN(–) – 0.5 LSB) when operating in the bipolar mode.

GAIN ERROR

This is a measure of the span error of the ADC. It is a measure of the difference between the measured and the ideal span between any two points in the transfer function. The two points used to calculate the gain error are full scale and zero scale.

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(–) – V_{REF}/GAIN + 0.5 LSB) when operating in the bipolar mode. Negative full-scale error is a summation of zero error and gain error.

POSITIVE FULL-SCALE OVERRANGE

Positive Full-Scale Overrange is the amount of overhead available to handle input voltages on AIN(+) input greater than AIN(–) + V_{REF}/GAIN (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages on AIN(+) below AIN(–) – V_{REF}/GAIN without overloading the analog modulator or overflowing the digital filter.

OFFSET CALIBRATION RANGE

In the system calibration modes, the AD7730 calibrates its offset with respect to the analog input. The Offset Calibration Range specification defines the range of voltages the AD7730 can accept and still accurately calibrate offset.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7730 can accept in the system calibration mode and still calibrate full scale correctly.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7730's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages, from zero to full scale, the AD7730 can accept and still accurately calibrate gain.

OUTPUT NOISE AND RESOLUTION SPECIFICATION

The AD7730 can be programmed to operate in either chop mode or nonchop mode. The chop mode can be enabled in ac-excited or dc-excited applications; it is optional in dc-excited applications, but chop mode must be enabled in ac-excited applications. These options are discussed in more detail in later sections. The chop mode has the advantage of lower drift numbers and better noise immunity, but the noise is approximately 20% higher for a given –3 dB frequency and output data rate. It is envisaged that the majority of weigh-scale users of the AD7730 will operate the part in chop mode to avail themselves of the excellent drift performance and noise immunity when chopping is enabled. The following tables outline the noise performance of the part in both chop and nonchop modes over all input ranges for a selection of output rates. Settling time refers to the time taken to get an output that is 100% settled to new value.

Output Noise (CHP = 1)

This mode is the primary mode of operation of the device. Table I shows the output rms noise for some typical output update rates and –3 dB frequencies for the AD7730 when used in chopping mode (CHP of Filter Register = 1) with a master clock frequency of 4.9152 MHz. These numbers are typical and are generated at a differential analog input voltage of 0 V. The output update rate is selected via the SF0 to SF11 bits of the Filter Register. Table II, meanwhile, shows the output peak-to-peak resolution in counts for the same output update rates. The numbers in brackets are the effective peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB). It is important to note that the numbers in Table II represent the resolution for which there will be no code flicker within a six-sigma limit. They are not calculated based on rms noise, but on peak-to-peak noise.

The numbers are generated for the bipolar input ranges. When the part is operated in unipolar mode, the output noise will be the same as the equivalent bipolar input range. As a result, the numbers in Table I will remain the same for unipolar ranges while the numbers in Table II will change. To calculate the numbers for Table II for unipolar input ranges simply divide the peak-to-peak resolution number in counts by two or subtract one from the peak-to-peak resolution number in bits.

Table I. Output Noise vs. Input Range and Update Rate (CHP = 1)

Typical Output RMS Noise in nV

Output Data Rate	–3 dB Frequency	SF Word	Settling Time Normal Mode	Settling Time Fast Mode	Input Range = ±80 mV	Input Range = ±40 mV	Input Range = ±20 mV	Input Range = ±10 mV
50 Hz	1.97 Hz	2048	460 ms	60 ms	115	75	55	40
100 Hz	3.95 Hz	1024	230 ms	30 ms	155	105	75	60
150 Hz	5.92 Hz	683	153 ms	20 ms	200	135	95	70
200 Hz*	7.9 Hz	512	115 ms	15 ms	225	145	100	80
400 Hz	15.8 Hz	256	57.5 ms	7.5 ms	335	225	160	110

*Power-On Default

Table II. Peak-to-Peak Resolution vs. Input Range and Update Rate (CHP = 1)

Peak-to-Peak Resolution in Counts (Bits)

Output Data Rate	–3 dB Frequency	SF Word	Settling Time Normal Mode	Settling Time Fast Mode	Input Range = ±80 mV	Input Range = ±40 mV	Input Range = ±20 mV	Input Range = ±10 mV
50 Hz	1.97 Hz	2048	460 ms	60 ms	230k (18)	175k (17.5)	120k (17)	80k (16.5)
100 Hz	3.95 Hz	1024	230 ms	30 ms	170k (17.5)	125k (17)	90k (16.5)	55k (16)
150 Hz	5.92 Hz	683	153 ms	20 ms	130k (17)	100k (16.5)	70k (16)	45k (15.5)
200 Hz*	7.9 Hz	512	115 ms	15 ms	120k (17)	90k (16.5)	65k (16)	40k (15.5)
400 Hz	15.8 Hz	256	57.5 ms	7.5 ms	80k (16.5)	55k (16)	40k (15.5)	30k (15)

*Power-On Default

Output Noise (CHP = 0)

Table III shows the output rms noise for some typical output update rates and –3 dB frequencies for the AD7730 when used in nonchopping mode (CHP of Filter Register = 0) with a master clock frequency of 4.9152 MHz. These numbers are typical and are generated at a differential analog input voltage of 0 V. The output update rate is selected via the SF0 to SF11 bits of the Filter Register. Table IV, meanwhile, shows the output peak-to-peak resolution in counts for the same output update rates. The numbers in brackets are the effective peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB). It is important to note that the numbers in Table IV represent the resolution for which there will be no code flicker within a six-sigma limit. They are not calculated based on rms noise, but on peak-to-peak noise.

The numbers are generated for the bipolar input ranges. When the part is operated in unipolar mode, the output noise will be the same as the equivalent bipolar input range. As a result, the numbers in Table III will remain the same for unipolar ranges while the numbers in Table IV will change. To calculate the number for Table IV for unipolar input ranges simply divide the peak-to-peak resolution number in counts by two or subtract one from the peak-to-peak resolution number in bits.

Table III. Output Noise vs. Input Range and Update Rate (CHP = 0)

Typical Output RMS Noise in nV

Output Data Rate	–3 dB Frequency	SF Word	Settling Time Normal Mode	Settling Time Fast Mode	Input Range = ±80 mV	Input Range = ±40 mV	Input Range = ±20 mV	Input Range = ±10 mV
150 Hz	5.85 Hz	2048	166 ms	26.6 ms	160	110	80	60
200 Hz	7.8 Hz	1536	125 ms	20 ms	190	130	95	75
300 Hz	11.7 Hz	1024	83.3 ms	13.3 ms	235	145	100	80
600 Hz	23.4 Hz	512	41.6 ms	6.6 ms	300	225	135	110
1200 Hz	46.8 Hz	256	20.8 ms	3.3 ms	435	315	210	150

Table IV. Peak-to-Peak Resolution vs. Input Range and Update Rate (CHP = 0)

Peak-to-Peak Resolution in Counts (Bits)

Output Data Rate	–3 dB Frequency	SF Word	Settling Time Normal Mode	Settling Time Fast Mode	Input Range = ±80 mV	Input Range = ±40 mV	Input Range = ±20 mV	Input Range = ±10 mV
150 Hz	5.85 Hz	2048	166 ms	26.6 ms	165k (17.5)	120k (17)	80k (16.5)	55k (16)
200 Hz	7.8 Hz	1536	125 ms	20 ms	140k (17)	100k (16.5)	70k (16)	45k (15.5)
300 Hz	11.7 Hz	1024	83.3 ms	13.3 ms	115k (17)	90k (16.5)	65k (16)	40k (15.5)
600 Hz	23.4 Hz	512	41.6 ms	6.6 ms	90k (16.5)	60k (16)	50k (15.5)	30k (15)
1200 Hz	46.8 Hz	256	20.8 ms	3.3 ms	60k (16)	43k (15.5)	32k (15)	20k (14.5)

ON-CHIP REGISTERS

The AD7730 contains thirteen on-chip registers which can be accessed via the serial port of the part. These registers are summarized in Figure 4 and in Table V and described in detail in the following sections.

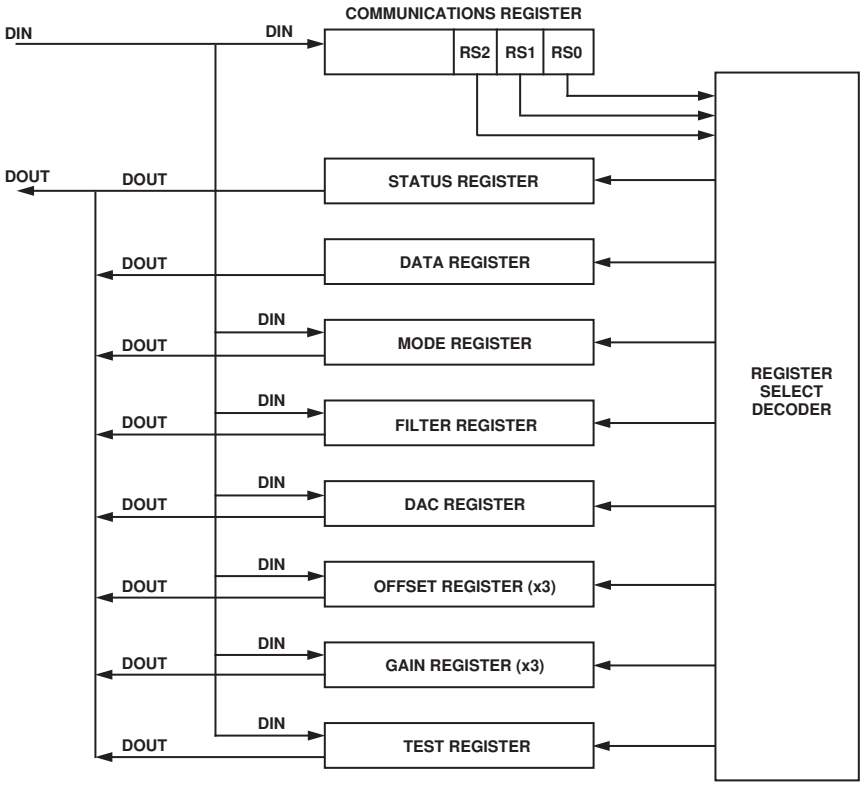


Figure 4. Register Overview

Table V. Summary of On-Chip Registers

Register Name	Type	Size	Power-On/Reset Default Value	Function
Communications Register	Write Only	8 Bits	Not Applicable	All operations to other registers are initiated through the Communications Register. This controls whether subsequent operations are read or write operations and also selects the register for that subsequent operation. Most subsequent operations return control to the Communications Register except for the continuous read mode of operation.
$\overline{WEN}$ ZERO RW1 RW0 ZERO RS2 RS1 RS0				
Status Register	Read Only	8 Bits	CX Hex	Provides status information on conversions, calibrations, settling to step inputs, standby operation and the validity of the reference voltage.
$\overline{RDY}$ $\overline{STDY}$ STBY NOREF MS3 MS2 MS1 MS0				
Data Register	Read Only	16 Bits or 24 Bits	000000 Hex	Provides the most up-to-date conversion result from the part. Register length can be programmed to be 16 bits or 24 bits.
Mode Register	Read/Write	16 Bits	01B0 Hex	Controls functions such as mode of operation, unipolar/bipolar operation, controlling the function of AIN2(+)/D1 and AIN2(-)/D0, burnout current, Data Register word length and disabling of MCLK OUT. It also contains the reference selection bit, the range selection bits and the channel selection bits.
MD2 MD1 MD0 $\overline{B}$/U DEN D1 D0 WL HIREF ZERO RN1 RN0 CLKDIS BO CH1 CH0				
Filter Register	Read/Write	24 Bits	200010 Hex	Controls the amount of averaging in the first stage filter, selects the fast step and skip modes and controls the ac excitation and chopping modes on the part.
SF11 SF10 SF9 SF8 SF7 SF6 SF5 SF4 SF3 SF2 SF1 SF0 ZERO ZERO SKIP FAST ZERO ZERO AC CHP DL3 DL2 DL1 DL0				
DAC Register	Read/Write	8 Bits	20 Hex	Provides control of the amount of correction performed by the Offset/TARE DAC.
ZERO ZERO DAC5 DAC4 DAC3 DAC2 DAC1 DAC0				
Offset Register	Read/Write	24 Bits	800000 Hex	Contains a 24-bit word which is the offset calibration coefficient for the part. The contents of this register are used to provide offset correction on the output from the digital filter. There are three Offset Registers on the part and these are associated with the input channels as outlined in Table XIII.
Gain Register	Read/Write	24 Bits	59AEE7 Hex	Contains a 24-bit word which is the gain calibration coefficient for the part. The contents of this register are used to provide gain correction on the output from the digital filter. There are three Gain Registers on the part and these are associated with the input channels as outlined in Table XIII.
Test Register	Read/Write	24 Bits	000000 Hex	Controls the test modes of the part which are used when testing the part. **The user is advised not to change the contents of this register.**

Communications Register (RS2–RS0 = 0, 0, 0)

The Communications Register is an 8-bit write-only register. All communications to the part must start with a write operation to the Communications Register. The data written to the Communications Register determines whether the next operation is a read or write operation, the type of read operation, and to which register this operation takes place. For single-shot read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the Communications Register. This is the default state of the interface, and on power-up or after a $\overline{\text{RESET}}$, the AD7730 is in this default state waiting for a write operation to the Communications Register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high, returns the AD7730 to this default state by resetting the part. Table VI outlines the bit designations for the Communications Register. CR0 through CR7 indicate the bit location, CR denoting the bits are in the Communications Register. CR7 denotes the first bit of the data stream.

Table VI. Communications Register

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}$	ZERO	RW1	RW0	ZERO	RS2	RS1	RS0

Bit Location	Bit Mnemonic	Description
CR7	$\overline{\text{WEN}}$	Write Enable Bit. A 0 must be written to this bit so the write operation to the Communications Register actually takes place. If a 1 is written to this bit, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a 0 is written to this bit. Once a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits will be loaded to the Communications Register.
CR6	ZERO	A zero **must** be written to this bit to ensure correct operation of the AD7730.
CR5, CR4	RW1, RW0	Read/Write Mode Bits. These two bits determine the nature of the subsequent read/write operation. Table VII outlines the four options.

Table VII. Read/Write Mode

RW1	RW0	Read/Write Mode
0	0	Single Write to Specified Register
0	1	Single Read of Specified Register
1	0	Start Continuous Read of Specified Register
1	1	Stop Continuous Read Mode

With 0, 0 written to these two bits, the next operation is a write operation to the register specified by bits RS2, RS1, RS0. Once the subsequent write operation to the specified register has been completed, the part returns to where it is expecting a write operation to the Communications Register.

With 0,1 written to these two bits, the next operation is a read operation of the register specified by bits RS2, RS1, RS0. Once the subsequent read operation to the specified register has been completed, the part returns to where it is expecting a write operation to the Communications Register.

Writing 1,0 to these bits, sets the part into a mode of continuous reads from the register specified by bits RS2, RS1, RS0. The most likely registers with which the user will want to use this function are the Data Register and the Status Register. Subsequent operations to the part will consist of read operations to the specified register without any intermediate writes to the Communications Register. This means that once the next read operation to the specified register has taken place, the part will be in a mode where it is expecting another read from that specified register. The part will remain in this continuous read mode until 30 Hex has been written to the Communications Register.

When 1,1 is written to these bits (and 0 written to bits CR3 through CR0), the continuous read mode is stopped and the part returns to where it is expecting a write operation to the Communications Register. Note, the part continues to look at the DIN line on each SCLK edge during continuous read mode to determine when to stop the continuous read mode. Therefore, the user must be careful not to inadvertently exit the continuous read mode or reset the AD7730 by writing a series of 1s to the part. The easiest way to avoid this is to place a logic 0 on the DIN line while the part is in continuous read mode. Once the part is in continuous read mode, the user should ensure that an integer multiple of 8 serial clocks should have taken place before attempting to take the part out of continuous read mode.

Bit Location	Bit Mnemonic	Description
CR3	ZERO	A zero **must** be written to this bit to ensure correct operation of the AD7730.
CR2–CR0	RS2–RS0	Register Selection Bits. RS2 is the MSB of the three selection bits. The three bits select which register type the next read or write operation operates upon as shown in Table VIII.

Table VIII. Register Selection

RS2	RS1	RS0	Register
0	0	0	Communications Register (Write Operation)
0	0	0	Status Register (Read Operation)
0	0	1	Data Register
0	1	0	Mode Register
0	1	1	Filter Register
1	0	0	DAC Register
1	0	1	Offset Register
1	1	0	Gain Register
1	1	1	Test Register

Status Register (RS2–RS0 = 0, 0, 0); Power-On/Reset Status: CX Hex

The Status Register is an 8-bit read-only register. To access the Status Register, the user must write to the Communications Register selecting either a single-shot read or continuous read mode and load bits RS2, RS1, RS0 with 0, 0, 0. Table IX outlines the bit designations for the Status Register. SR0 through SR7 indicate the bit location, SR denoting the bits are in the Status Register. SR7 denotes the first bit of the data stream. Figure 5 shows a flowchart for reading from the registers on the AD7730. The number in brackets indicates the power-on/reset default status of that bit.

Table IX. Status Register

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
$\overline{\text{RDY}}$ (1)	$\overline{\text{STDY}}$ (1)	STBY (0)	NOREF (0)	MS3 (X)	MS2 (X)	MS1 (X)	MS0 (X)

Bit Location	Bit Mnemonic	Description
SR7	RDY	Ready Bit. This bit provides the status of the RDY flag from the part. The status and function of this bit is the same as the RDY output pin. A number of events set the RDY bit high as indicated in Table XVIII.
SR6	STDY	Steady Bit. This bit is updated when the filter writes a result to the Data Register. If the filter is in *FAST*Step mode (see Filter Register section) and responding to a step input, the STDY bit remains high as the initial conversion results become available. The RDY output and bit are set low on these initial conversions to indicate that a result is available. If the STDY is high, however, it indicates that the result being provided is not from a fully settled second-stage FIR filter. When the FIR filter has fully settled, the STDY bit will go low coincident with RDY. If the part is never placed into its *FAST*Step mode, the STDY bit will go low at the first Data Register read and it is not cleared by subsequent Data Register reads. A number of events set the STDY bit high as indicated in Table XVIII. STDY is set high along with RDY by all events in the table except a Data Register read.
SR5	STBY	Standby Bit. This bit indicates whether the AD7730 is in its Standby Mode or normal mode of operation. The part can be placed in its standby mode using the STANDBY input pin or by writing 011 to the MD2 to MD0 bits of the Mode Register. The power-on/reset status of this bit is 0 assuming the STANDBY pin is high.
SR4	NOREF	No Reference Bit. If the voltage between the REF IN(+) and REF IN(–) pins is below 0.3 V, or either of these inputs is open-circuit, the NOREF bit goes to 1. If NOREF is active on completion of a conversion, the Data Register is loaded with all 1s. If NOREF is active on completion of a calibration, updating of the calibration registers is inhibited.
SR3–SR0	MS3–MS0	These bits are for factory use. The power-on/reset status of these bits vary, depending on the factory-assigned number.

Data Register (RS2–RS0 = 0, 0, 1); Power On/Reset Status: 000000 Hex

The Data Register on the part is a read-only register which contains the most up-to-date conversion result from the AD7730. Figure 5 shows a flowchart for reading from the registers on the AD7730. The register can be programmed to be either 16 bits or 24 bits wide, determined by the status of the WL bit of the Mode Register. The RDY output and RDY bit of the Status Register are set low when the Data Register is updated. The RDY pin and RDY bit will return high once the full contents of the register (either 16 bits or 24 bits) have been read. If the Data Register has not been read by the time the next output update occurs, the RDY pin and RDY bit will go high for at least $100 \times t_{CLK\ IN}$, indicating when a read from the Data Register should not be initiated to avoid a transfer from the Data Register as it is being updated. Once the updating of the Data Register has taken place, RDY returns low.

If the Communications Register data sets up the part for a write operation to this register, a write operation must actually take place in order to return the part to where it is expecting a write operation to the Communications Register (the default state of the interface). However, the 16 or 24 bits of data written to the part will be ignored by the AD7730.

Mode Register (RS2–RS0 = 0, 1, 0); Power On/Reset Status: 01B0 Hex

The Mode Register is a 16-bit register from which data can be read or to which data can be written. This register configures the operating modes of the AD7730, the input range selection, the channel selection and the word length of the Data Register. Table X outlines the bit designations for the Mode Register. MR0 through MR15 indicate the bit location, MR denoting the bits are in the Mode Register. MR15 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit. Figure 5 shows a flowchart for reading from the registers on the AD7730 and Figure 6 shows a flowchart for writing to the registers on the part.

Table X. Mode Register

MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8
MD2 (0)	MD1 (0)	MD0 (0)	$\overline{B}$/U (0)	DEN (0)	D1 (0)	D0 (0)	WL (1)
MR7	**MR6**	**MR5**	**MR4**	**MR3**	**MR2**	**MR1**	**MR0**
HIREF (1)	ZERO (0)	RN1 (1)	RN0 (1)	CLKDIS (0)	BO (0)	CH1 (0)	CH0 (0)

Bit Location	Bit Mnemonic	Description
MR15–MR13	MD2–MD0	Mode Bits. These three bits determine the mode of operation of the AD7730 as outlined in Table XI. The modes are independent, such that writing new mode bits to the Mode Register will exit the part from the mode in which it is operating and place it in the new requested mode immediately after the Mode Register write. The function of the mode bits is described in more detail below.

Table XI. Operating Modes

MD2	MD1	MD0	Mode of Operation
0	0	0	Sync (Idle) Mode Power-On/Reset Default
0	0	1	Continuous Conversion Mode
0	1	0	Single Conversion Mode
0	1	1	Power-Down (Standby) Mode
1	0	0	Internal Zero-Scale Calibration
1	0	1	Internal Full-Scale Calibration
1	1	0	System Zero-Scale Calibration
1	1	1	System Full-Scale Calibration

MD2	MD1	MD0	Operating Mode
0	0	0	Sync (Idle) Mode. In this mode, the modulator and filter are held in reset mode and the AD7730 is not processing any new samples or data. Placing the part in this mode is equivalent to exerting the $\overline{\text{SYNC}}$ input pin. However, exerting the $\overline{\text{SYNC}}$ pin does not actually force these mode bits to 0, 0, 0. The part returns to this mode after a calibration or after a conversion in Single Conversion Mode. This is the default condition of these bits after Power-On/Reset.
0	0	1	Continuous Conversion Mode. In this mode, the AD7730 is continuously processing data and providing conversion results to the Data Register at the programmed output update rate (as determined by the Filter Register). For most applications, this would be the normal operating mode of the AD7730.
0	1	0	Single Conversion Mode. In this mode, the AD7730 performs a single conversion, updates the Data Register, returns to the Sync Mode and resets the mode bits to 0, 0, 0. The result of the single conversion on the AD7730 in this mode will not be provided until the full settling time of the filter has elapsed.
0	1	1	Power-Down (Standby) Mode. In this mode, the AD7730 goes into its power-down or standby state. Placing the part in this mode is equivalent to exerting the $\overline{\text{STANDBY}}$ input pin. However, exerting $\overline{\text{STANDBY}}$ does not actually force these mode bits to 0, 1, 1.
1	0	0	Zero-Scale Self-Calibration Mode. This activates zero-scale self-calibration on the channel selected by CH1 and CH0 of the Mode Register. This zero-scale self-calibration is performed at the selected gain on internally shorted (zeroed) inputs. When this zero-scale self-calibration is complete, the part updates the contents of the appropriate Offset Calibration Register and returns to Sync Mode with MD2, MD1 and MD0 returning to 0, 0, 0. The $\overline{\text{RDY}}$ output and bit go high when calibration is initiated and return low when this zero-scale self-calibration is complete to indicate that the part is back in Sync Mode and ready for further operations.
1	0	1	Full-Scale Self-Calibration Mode. This activates full-scale self-calibration on the channel selected by CH1 and CH0 of the Mode Register. This full-scale self-calibration is performed at the selected gain on an internally-generated full-scale signal. When this full-scale self-calibration is complete, the part updates the contents of the appropriate Gain Calibration Register and Offset Calibration Register and returns to Sync Mode with MD2, MD1 and MD0 returning to 0, 0, 0. The $\overline{\text{RDY}}$ output and bit go high when calibration is initiated and return low when this full-scale self-calibration is complete to indicate that the part is back in Sync Mode and ready for further operations.
1	1	0	Zero-Scale System Calibration Mode. This activates zero scale system calibration on the channel selected by CH1 and CH0 of the Mode Register. Calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. When this zero-scale system calibration is complete, the part updates the contents of the appropriate Offset Calibration Register and returns to Sync Mode with MD2, MD1 and MD0 returning to 0, 0, 0. The $\overline{\text{RDY}}$ output and bit go high when calibration is initiated and return low when this zero-scale calibration is complete to indicate that the part is back in Sync Mode and ready for further operations.
1	1	1	Full-Scale System Calibration Mode. This activates full-scale system calibration on the selected input channel. Calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. When this full-scale system calibration is complete, the part updates the contents of the appropriate Gain Calibration Register and returns to Sync Mode with MD2, MD1 and MD0 returning to 0, 0, 0. The $\overline{\text{RDY}}$ output and bit go high when calibration is initiated and return low when this full-scale calibration is complete to indicate that the part is back in Sync Mode and ready for further operations.

Bit Location	Bit Mnemonic	Description
MR12	B/U	Bipolar/Unipolar Bit. A 0 in this bit selects bipolar operation and the output coding is 00 . . . 000 for negative full-scale input, 10 . . . 000 for zero input, and 11 . . . 111 for positive full-scale input. A 1 in this bit selects unipolar operation and the output coding is 00 . . . 000 for zero input and 11 . . . 111 for positive full-scale input.
MR11	DEN	Digital Output Enable Bit. With this bit at 1, the AIN2(+)/D1 and AIN2(–)/D0 pins assume their digital output functions and the output drivers connected to these pins are enabled. In this mode, the user effectively has two port bits which can be programmed over the serial interface.
MR10–MR9	D1–D0	Digital Output Bits. These bits determine the digital outputs on the AIN2(+)/D1 and AIN2(–)/D0 pins, respectively, when the DEN bit is a 1. For example, a 1 written to the D1 bit of the Mode Register (with the DEN bit also a 1) will put a logic 1 on the AIN2(+)/D1 pin. This logic 1 will remain on this pin until a 0 is written to the D1 bit (in which case the AIN2(+)/D1 pin goes to a logic 0) or the digital output function is disabled by writing a 0 to the DEN bit.
MR8	WL	Data Word Length Bit. This bit determines the word length of the Data Register. A 0 in this bit selects 16-bit word length when reading from the data register (i.e., RDY returns high after 16 serial clock cycles in the read operation). A 1 in this bit selects 24-bit word length for the Data Register.
MR7	HIREF	High Reference Bit. This bit should be set in accordance with the reference voltage which is being used on the part. If the reference voltage is 5 V, the HIREF bit should be set to 1. If the reference voltage is 2.5 V, the HIREF bit should be set to a 0. With the HIREF bit set correctly for the appropriate applied reference voltage, the input ranges are 0 mV to +10 mV, +20 mV, +40 mV and +80 mV for unipolar operation and ±10 mV, ±20 mV, ±40 mV and ±80 mV for bipolar operation. It is possible for a user with a 2.5 V reference to set the HIREF bit to a 1. In this case, the part is operating with a 2.5 V reference but assumes it has a 5 V reference. As a result, the input ranges on the part become 0 to +5 mV, +10 mV, +20 mV and +40 mV for unipolar operation and ±5 mV, ±10 mV, ±20 mV and ±40 mV for bipolar operation. However, the output noise from the part (in nV) will remain unchanged so the resolution of the part (in counts) will halve.
MR6	ZERO	A zero **must** be written to this bit to ensure correct operation of the AD7730.
MR5–MR4	RN1–RN0	Input Range Bits. These bits determine the analog input range for the selected analog input. The different input ranges are outlined in Table XII. The table is valid for a reference voltage of 5 V with the HIREF bit at 1, or for a reference voltage of 2.5 V with the HIREF bit at a logic 0. **Table XII. Input Range Selection** **RN1** / **RN0** / **Input Range** $\overline{B}$**/U Bit = 0** / **Input Range** $\overline{B}$**/U Bit = 1** 0 / 0 / –10 mV to +10 mV / 0 mV to +10 mV 0 / 1 / –20 mV to +20 mV / 0 mV to +20 mV 1 / 0 / –40 mV to +40 mV / 0 mV to +40 mV 1 / 1 / –80 mV to +80 mV / 0 mV to +80 mV Power-On/Reset Default Note that the input range given in the above table is the range that appears at the input of the PGA after the DAC offset value has been applied. If the DAC adjusts out no offset (DAC Register is 0010 0000), then this is also the input voltage range at the analog input pins. If, for example, the DAC subtracts out 50 mV of offset and the part is being operated in bipolar mode with RN1 and RN0 at 0, 0, the actual input voltage range at the analog input is +40 mV to +60 mV.
MR3	CLKDIS	Master Clock Disable Bit. A 1 in the bit disables the master clock from appearing at the MCLK OUT pin. When disabled, the MCLK OUT pin is forced low. It allows the user the flexibility of using the MCLK OUT as a clock source for other devices in the system or of turning off the MCLK OUT as a power saving feature. When using an external master clock at the MCLK IN pin, the AD7730 continues to have internal clocks and will convert normally with the CLKDIS bit active. When using a crystal oscillator or ceramic resonator across the MCLK IN and MCLK OUT pins, the AD7730 clock is stopped and no conversions take place when the CLKDIS bit is active.

Bit Location	Bit Mnemonic	Description
MR2	BO	Burnout Current Bit. A 1 in this bit activates the burnout currents. When active, the burnout currents connect to the selected analog input pair, one source current to the AIN(+) input and one sink current to the AIN(–) input. A 0 in this bit turns off the on-chip burnout currents.
MR1–MR0	CH1–CH0	Channel Selection Bits. These bits select the analog input channel to be converted or calibrated as outlined in Table XIII. With CH1 at 1 and CH0 at 0, the part looks at the AIN1(–) input internally shorted to itself. This can be used as a test method to evaluate the noise performance of the part with no external noise sources. In this mode, the AIN1(–) input should be connected to an external voltage within the allowable common-mode range of the part. The Offset and Gain Calibration Registers on the part are paired. There are three pairs of calibration registers labelled Register Pair 0 through Register Pair 2. These are assigned to the input channel pairs as outlined in Table XIII.

Table XIII. Channel Selection

		Input Channel Pair		
CH1	CH0	Positive Input	Negative Input	Calibration Register Pair
0	0	AIN1(+)	AIN1(–)	Register Pair 0
0	1	AIN2(+)	AIN2(–)	Register Pair 1
1	0	AIN1(–)	AIN1(–)	Register Pair 0
1	1	AIN1(–)	AIN2(–)	Register Pair 2

Filter Register (RS2-RS0 = 0, 1, 1); Power-On/Reset Status: 200010 Hex

The Filter Register is a 24-bit register from which data can be read or to which data can be written. This register determines the amount of averaging performed by the filter and the mode of operation of the filter. It also sets the chopping mode and the delay associated with chopping the inputs. Table XIV outlines the bit designations for the Filter Register. FR0 through FR23 indicate the bit location, FR denoting the bits are in the Filter Register. FR23 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit. Figure 5 shows a flowchart for reading from the registers on the AD7730 and Figure 6 shows a flowchart for writing to the registers on the part.

Table XIV. Filter Register

FR23	FR22	FR21	FR20	FR19	FR18	FR17	FR16
SF11 (0)	SF10 (0)	SF9 (1)	SF8 (0)	SF7 (0)	SF6 (0)	SF5 (0)	SF4 (0)
FR15	FR14	FR13	FR12	FR11	FR10	FR9	FR8
SF3 (0)	SF2 (0)	SF1 (0)	SF0 (0)	ZERO (0)	ZERO (0)	SKIP (0)	FAST (0)
FR7	FR6	FR5	FR4	FR3	FR2	FR1	FR0
ZERO (0)	ZERO (0)	AC (0)	CHP (1)	DL3 (0)	DL2 (0)	DL1 (0)	DL0 (0)

Bit Location	Bit Mnemonic	Description
FR23–FR12	SF11–SF0	Sinc^3 Filter Selection Bits. The AD7730 contains two filters: a sinc^3 filter and an FIR filter. The 12 bits programmed to SF11 through SF0 set the amount of averaging the sinc^3 filter performs. As a result, the number programmed to these 12 bits affects the –3 dB frequency and output update rate from the part (see Filter Architecture section). The allowable range for SF words depends on whether the part is operated with CHOP on or off and SKIP on or off. Table XV outlines the SF ranges for different setups. All output update rates will be one-half those quoted in Table XV for the AD7730L operating with a 2.4576 MHz clock.

Table XV. SF Ranges

CHOP	SKIP	SF Range	Output Update Rate Range (Assuming 4.9152 MHz Clock)
0	0	2048 to 150	150 Hz to 2.048 kHz
1	0	2048 to 75	50 Hz to 1.365 kHz
0	1	2048 to 40	150 Hz to 7.6 kHz
1	1	2048 to 20	50 Hz to 5.12 kHz

Bit Location	Bit Mnemonic	Description
FR11–FR10	ZERO	A zero **must** be written to these bits to ensure correct operation of the AD7730.
FR9	SKIP	FIR Filter Skip Bit. With a 0 in this bit, the AD7730 performs two stages of filtering before shipping a result out of the filter. The first is a $sinc^3$ filter followed by a 22-tap FIR filter. With a 1 in this bit, the FIR filter on the part is bypassed and the output of the $sinc^3$ is fed directly as the output result of the AD7730's filter (see Filter Architecture for more details on the filter implementation).
FR8	FAST	*FAST*Step Mode Enable Bit. A 1 in this bit enables the *FAST*Step mode on the AD7730. In this mode, if a step change on the input is detected, the FIR calculation portion of the filter is suspended and replaced by a simple moving average on the output of the $sinc^3$ filter. Initially, two outputs from the $sinc^3$ filter are used to calculate an AD7730 output. The number of $sinc^3$ outputs used to calculate the moving average output is increased (from 2 to 4 to 8 to 16) until the $\overline{\text{STDY}}$ bit goes low. When the FIR filter has fully settled after a step, the $\overline{\text{STDY}}$ bit will become active and the FIR filter is switched back into the processing loop (see Filter Architecture section for more details on the *FAST*Step mode).
FR7–FR6	ZERO	A zero **must** be written to these bits to ensure correct operation of the AD7730.
FR5	AC	AC Excitation Bit. If the signal source to the AD7730 is ac-excited, a 1 must be placed in this bit. For dc-excited inputs, this bit must be 0. The ac bit has no effect if CHP is 0. With the ac bit at 1, the AD7730 assumes that the voltage at the AIN(+)/AIN(–) and REF IN(+)/REF IN(–) input terminals are reversed on alternate input sampling cycles (i.e. chopped). Note that when the AD7730 is performing internal zero-scale or full-scale calibrations, the ac bit is treated as a 0, i.e., the device performs these self-calibrations with dc excitation.
FR4	CHP	Chop Enable Bit. This bit determines if the chopping mode on the part is enabled. A 1 in this bit location enables chopping on the part. When the chop mode is enabled, the part is effectively chopped at its input and output to remove all offset and offset drift errors on the part. If offset performance with time and temperature are important parameters in the design, it is recommended that the user enable chopping on the part. If the input signal is dc-excited, the user has the option of operating the part in either chop or nonchop mode. If the input signal is ac-excited, both the ac bit and the CHP bit must be set to 1. The chop rate on the ACX and $\overline{\text{ACX}}$ signals is one half of the programmed output rate of the part and thus the chopping frequency varies with the programmed output rate.
FR3–FR0	DL3–DL0	Delay Selection Bits. These four bits program the delay (in modulator cycles) to be inserted after each chop edge when the CHP bit is 1. One modulator cycle is MCLK IN/16 and is 3.25 µs at MCLK IN = 4.9152 MHz. A delay should only be required when in ac mode. Its purpose is to cater for external delays between the switching signals (ACX and $\overline{\text{ACX}}$) and when the analog inputs are actually switched and settled. During the specified number of cycles (between 0 and 15), the modulator is held in reset and the filter does not accept any inputs. If CHP = 1, the output rate is (MCLK IN/ $16 \times (DL + 3 \times SF)$ where DL is the value loaded to bits DL0–DL3. The chop rate is always one half of the output rate. This chop period takes into account the programmed delay and the fact that the $sinc^3$ filter must settle every chop cycle. With CHP = 0, the output rate is 1/SF.

DAC Register (RS2–RS0 = 1, 0, 0); Power On/Reset Status: 20 Hex
The DAC Register is an 8-bit register from which data can either be read or to which data can be written. This register provides the code for the offset-compensation DAC on the part. Table XVI outlines the bit designations for the DAC Register. DR0 through DR7 indicate the bit location, DR denoting the bits are in the DAC Register. DR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit. Figure 5 shows a flowchart for reading from the registers on the AD7730 and Figure 6 shows a flowchart for writing to the registers on the part.

Table XVI. DAC Register

DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0
ZERO (0)	ZERO (0)	DAC5 (1)	DAC4 (0)	DAC3 (0)	DAC2 (0)	DAC1 (0)	DAC0 (0)

Bit Location	Bit Mnemonic	Description
DR7–DR6	ZERO	A zero **must** be written to these bits to ensure correct operation of the AD7730.
DR5–DR0	DAC5–DAC0	DAC Selection Bits. These bits program the output of the offset DAC. The DAC is effectively 6 bits with one sign bit (DAC5) and five magnitude bits. With DAC5 at 1, the DAC output subtracts from the analog input before it is applied to the PGA. With DAC5 at 0, the DAC output adds to the analog input before it is applied to the PGA. The DAC output is given by $(V_{REF}/62.5) \times (D/32) = (V_{REF}/2000) \times D$ where D is the decimal equivalent of bits DAC4 to DAC0. Thus, for a 5 V reference applied across the REF IN pins, the DAC resolution is 2.5 mV and offsets in the range –77.5 mV to +77.5 mV can be removed from the analog input signal before it is applied to the PGA. Note, that the HIREF bit has no effect on the DAC range or resolution, it controls the ADC range only.

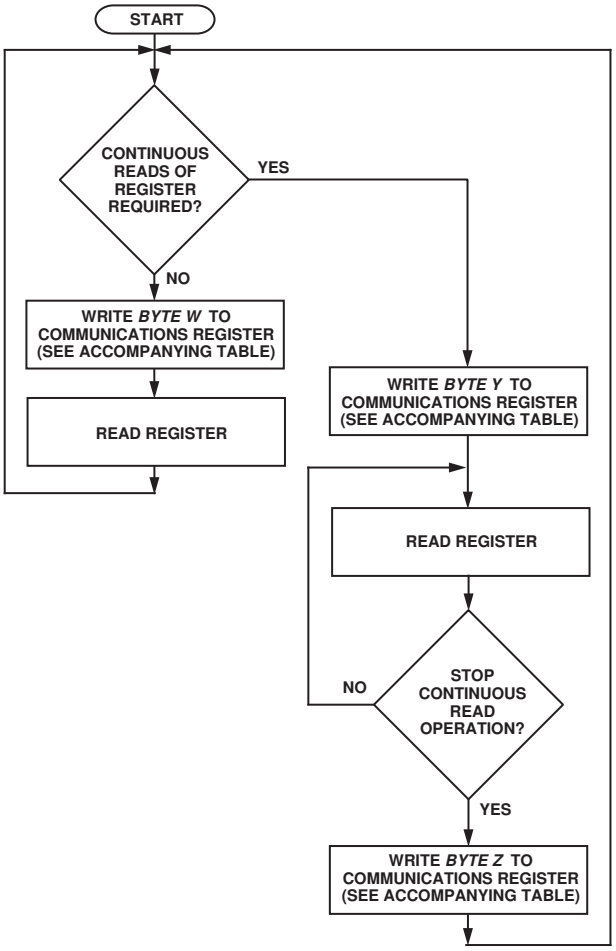
Offset Calibration Register (RS2–RS0 = 1, 0, 1); Power-On/Reset Status: 800000 Hex
The AD7730 contains three 24-bit Offset Calibration Registers, labelled Offset Calibration Register 0 to Offset Calibration Register 2, to which data can be written and from which data can be read. The three registers are totally independent of each other. The Offset Calibration Register is used in conjunction with the associated Gain Calibration Register to form a register pair. The calibration register pair used to scale the output is as outlined in Table XIII. The Offset Calibration Register is updated after an offset calibration routine (1, 0, 0 or 1, 1, 0 loaded to the MD2, MD1, MD0 bits of the Mode Register). During subsequent conversions, the contents of this register are subtracted from the filter output prior to gain scaling being performed on the word. Figure 5 shows a flowchart for reading from the registers on the AD7730 and Figure 6 shows a flowchart for writing to the registers on the part.

Gain Calibration Register (RS2–RS0 = 1, 1, 0); Power-On/Reset Status: 593CEA
The AD7730 contains three 24-bit Gain Calibration Registers, labelled Gain Calibration Register 0 to Gain Calibration Register 2, to which data can be written and from which data can be read. The three registers are totally independent of each other. The Gain Calibration Register is used in conjunction with the associated Offset Calibration Register to form a register pair. The calibration register pair used to scale the output is as outlined in Table XIII. The Gain Calibration Register is updated after a gain calibration routine (1, 0, 1 or 1, 1, 1 loaded to the MD2, MD1, MD0 bits of the Mode Register). During subsequent conversions, the contents of this register are used to scale the number which has already been offset corrected with the Offset Calibration Register contents. Figure 5 shows a flowchart for reading from the registers on the AD7730 and Figure 6 shows a flowchart for writing to the registers on the part.

Test Register (RS2–RS0 = 1, 1, 1); Power-On/Reset Status: 000000Hex
The AD7730 contains a 24-bit Test Register to which data can be written and from which data can be read. The contents of this Test Register are used in testing the device. The user is advised not to change the status of any of the bits in this register from the default (Power-On or RESET) status of all 0s as the part will be placed in one of its test modes and will not operate correctly. If the part enters one of its test modes, exercising $\overline{\text{RESET}}$ or writing 32 successive 1s to the part will exit the AD7730 from the mode and return all register contents to their power-on/reset status. Note, if the part is placed in one of its test modes, it may not be possible to read back the contents of the Test Register depending on the test mode in which the part has been placed.

READING FROM AND WRITING TO THE ON-CHIP REGISTERS

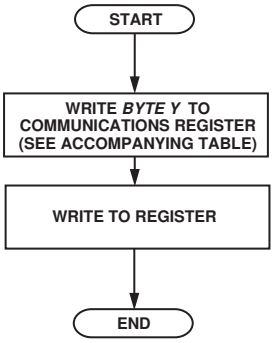
The AD7730 contains a total of thirteen on-chip registers. These registers are all accessed over a three-wire interface. As a result, addressing of registers is via a write operation to the topmost register on the part, the Communications Register. Figure 5 shows a flowchart for reading from the different registers on the part summarizing the sequence and the words to be written to access each of the registers. Figure 6 gives a flowchart for writing to the different registers on the part, again summarizing the sequence and words to be written to the AD7730.



Register	Byte W (Hex)	Byte Y (Hex)	Byte Z (Hex)
Status Register	10	20	30
Data Register	11	21	30
Mode Register	12	22	30
Filter Register	13	N/A*	N/A*
DAC Register	14	N/A*	N/A*
Offset Register	15	N/A*	N/A*
Gain Register	16	N/A*	N/A*
Test Register	17	N/A*	N/A*

*N/A= Not Applicable. Continuous reads of these registers does not make sense as the register contents would remain the same since they are only changed by a write operation.

Figure 5. Flowchart for Reading from the AD7730 Registers



Register	Byte Y (Hex)
Communications Register	00
Data Register	Read Only Register
Mode Register	02
Filter Register	03
DAC Register	04
Offset Register	05
Gain Register	06
Test Register	User is advised not to change contents of Test Register.

Figure 6. Flowchart for Writing to the AD7730 Registers

CALIBRATION OPERATION SUMMARY

The AD7730 contains a number of calibration options as outlined previously. Table XVII summarizes the calibration types, the operations involved and the duration of the operations. There are two methods of determining the end of calibration. The first is to monitor the hardware RDY pin using either interrupt-driven or polling routines. The second method is to do a software poll of the RDY bit in the Status Register. This can be achieved by setting up the part for continuous reads of the Status Register once a calibration has been initiated. The RDY pin and RDY bit go high on initiating a calibration and return low at the end of the calibration routine. At this time, the MD2, MD1, MD0 bits of the Mode Register have returned to 0, 0, 0. The FAST and SKIP bits are treated as 0 for the calibration sequence so the full filter is always used for the calibration routines. See Calibration section for full detail.

Table XVII. Calibration Operations

Calibration Type	MD2, MD1, MD0	Duration to $\overline{RDY}$ Low (CHP = 1)	Duration to $\overline{RDY}$ Low (CHP = 0)	Calibration Sequence
Internal Zero-Scale	1, 0, 0	22 × 1/Output Rate	24 × 1/Output Rate	Calibration on internal shorted input with PGA set for selected input range. The ac bit is ignored for this calibration sequence. The sequence is performed with dc excitation. The Offset Calibration Register for the selected channel is updated at the end of this calibration sequence. For full self-calibration, this calibration should be preceded by an Internal Full-Scale calibration. For applications which require an Internal Zero-Scale and System Full-Scale calibration, this Internal Zero-Scale calibration should be performed first.
Internal Full-Scale	1, 0, 1	44 × 1/Output Rate	48 × 1/Output Rate	Calibration on internally-generated input full-scale with PGA set for selected input range. The ac bit is ignored for this calibration sequence. The sequence is performed with dc excitation. The Gain Calibration Register for the selected channel is updated at the end of this calibration sequence. It is recommended that internal full-scale calibrations are performed on the 80 mV range, regardless of the subsequent operating range, to optimize the post-calibration gain error. This calibration should be followed by either an Internal Zero-Scale or System Zero-Scale calibration. This zero-scale calibration should be performed at the operating input range.
System Zero-Scale	1, 1, 0	22 × 1/Output Rate	24 × 1/Output Rate	Calibration on externally applied input voltage with PGA set for selected input range. The input applied is assumed to be the zero scale of the system. If ac = 1, the system continues to use ac excitation for the duration of the calibration. For full system calibration, this System Zero-Scale calibration should be performed first. For applications which require a System Zero-Scale and Internal Full-Scale calibration, this calibration should be preceded by the Internal Full-Scale calibration. The Offset Calibration Register for the selected channel is updated at the end of this calibration sequence.
System Full-Scale	1, 1, 1	22 × 1/Output Rate	24 × 1/Output Rate	Calibration on externally-applied input voltage with PGA set for selected input range. The input applied is assumed to be the full-scale of the system. If ac = 1, the system continues to use ac excitation for the duration of the calibration. This calibration should be preceded by a System Zero-Scale or Internal Zero-Scale calibration. The Gain Calibration Register for the selected channel is updated at the end of this calibration sequence.

CIRCUIT DESCRIPTION

The AD7730 is a sigma-delta A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low-frequency signals such as those in weigh-scale, strain-gage, pressure transducer or temperature measurement applications. It contains a sigma-delta (or charge-balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter and a bidirectional serial communications port. The part consumes 13 mA of power supply current with a standby mode which consumes only 25 μA. The part operates from a single +5 V supply. The clock source for the part can be provided via an external clock or by connecting a crystal oscillator or ceramic resonator across the MCLK IN and MCLK OUT pins.

The part contains two programmable-gain fully differential analog input channels. The part handles a total of eight different input ranges which are programmed via the on-chip registers. There are four differential unipolar ranges: 0 mV to +10 mV, 0 mV to +20 mV, 0 mV to +40 mV and 0 mV to +80 mV and four differential bipolar ranges: ±10 mV, ±20 mV, ±40 mV and ±80 mV.

The AD7730 employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The sigma-delta modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A digital low-pass filter processes the output of the sigma-delta modulator and updates the data register at a rate that can be programmed over the serial interface. The output data from the part is accessed over this serial interface. The cutoff frequency and output rate of this filter can be programmed via on-chip registers. The output noise performance and peak-to-peak resolution of the part varies with gain and with the output rate as shown in Tables I to IV.

The analog inputs are buffered on-chip allowing the part to handle significant source impedances on the analog input. This means that external R, C filtering (for noise rejection or RFI reduction) can be placed on the analog inputs if required. Both analog channels are differential, with a common-mode voltage range that comes within 1.2 V of AGND and 0.95 V of AV_{DD}. The reference input is also differential and the common-mode range here is from AGND to AV_{DD}.

The part contains a 6-bit DAC that is controlled via on-chip registers. This DAC can be used to remove TARE values of up to ±80 mV from the analog input signal range. The resolution on this TARE function is 1.25 mV for a +2.5 V reference and 2.5 mV with a +5 V reference.

The AD7730 can accept input signals from a dc-excited bridge. It can also handle input signals from an ac-excited bridge by using the ac excitation clock signals (ACX and $\overline{\text{ACX}}$) to switch the supplies to the bridge. ACX and $\overline{\text{ACX}}$ are nonoverlapping clock signals used to synchronize the external ac supplies that drive the transducer bridge. These ACX clocks are demodulated on the AD7730 input.

The AD7730 contains a number of hardware and software events that set or reset status flags and bits in registers. Table XVIII summarizes which blocks and flags are affected by the different events.

Table XVIII. Reset Events

Event	Set Registers to Default	Mode Bits	Filter Reset	Analog Power-Down	Reset Serial Interface	Set $\overline{\text{RDY}}$ Pin/Bit	Set $\overline{\text{STDY}}$ Bit
Power-On Reset	Yes	000	Yes	Yes	Yes	Yes	Yes
RESET Pin	Yes	000	Yes	No	Yes	Yes	Yes
STANDBY Pin	No	As Is	Yes	Yes	No	Yes	Yes
Mode 011 Write	No	011	Yes	Yes	No	Yes	Yes
SYNC Pin	No	As Is	Yes	No	No	Yes	Yes
Mode 000 Write	No	000	Yes	No	No	Yes	Yes
Conversion or Cal Mode Write	No	New Value	Initial Reset	No	No	Yes	Yes
Clock 32 1s	Yes	000	Yes	No	Yes	Yes	Yes
Data Register Read	No	As Is	No	No	No	Yes	No

ANALOG INPUT

Analog Input Channels

The AD7730 contains two differential analog input channels, a primary input channel, AIN1, and a secondary input channel, AIN2. The input pairs provide programmable gain, differential channels which can handle either unipolar or bipolar input signals. It should be noted that the bipolar input signals are referenced to the respective AIN(–) input of the input pair. The secondary input channel can also be reconfigured as two digital output port bits.

A two-channel differential multiplexer switches one of the two input channels to the on-chip buffer amplifier. This multiplexer is controlled by the CH0 and CH1 bits of the Mode Register. When the analog input channel is switched, the $\overline{\text{RDY}}$ output goes high and the settling time of the part must elapse before a valid word from the new channel is available in the Data Register (indicated by $\overline{\text{RDY}}$ going low).

Buffered Inputs

The output of the multiplexer feeds into a high impedance input stage of the buffer amplifier. As a result, the analog inputs can handle significant source impedances. This buffer amplifier has an input bias current of 50 nA (CHP = 1) and 60 nA (CHP = 0). This current flows in each leg of the analog input pair. The offset current on the part is the difference between the input bias on the legs of the input pair. This offset current is less than 10 nA (CHP = 1) and 30 nA (CHP = 0). Large source resistances result in a dc offset voltage developed across the source resistance on each leg, but matched impedances on the analog input legs will reduce the offset voltage to that generated by the input offset current.

Analog Input Ranges

The absolute input voltage range is restricted to between AGND + 1.2 V to AV_{DD} – 0.95 V, which also places restrictions on the common-mode range. Care must be taken in setting up the common-mode voltage and input voltage range so these limits are not exceeded, otherwise there will be a degradation in linearity performance.

In some applications, the analog input range may be biased either around system ground or slightly below system ground. In such cases, the AGND of the AD7730 must be biased negative with respect to system ground so the analog input voltage does not go within 1.2 V of AGND. Care should taken to ensure that the differential between either AV_{DD} or DV_{DD} and this biased AGND does not exceed 5.5 V. This is discussed in more detail in the Applications section.

Programmable Gain Amplifier

The output from the buffer amplifier is summed with the output of the 6-bit Offset DAC before it is applied to the input of the on-chip programmable gain amplifier (PGA). The PGA can handle four different unipolar input ranges and four bipolar ranges. With the HIREF bit of the Mode Register at 0 and a +2.5 V reference (or the HIREF bit at 1 and a +5 V reference), the unipolar ranges are 0 mV to +10 mV, 0 mV to +20 mV, 0 mV to +40 mV, and 0 mV to +80 mV, while the bipolar ranges are ±10 mV, ±20 mV, ±40 mV and ±80 mV. These are the nominal ranges that should appear at the input to the on-chip PGA.

Offset DAC

The purpose of the Offset DAC is to either add or subtract an offset so the input range at the input to the PGA is as close as possible to the nominal. If the output of the 6-bit Offset DAC is 0 V, the differential voltage ranges that appear at the analog input to the part will also appear at the input to the PGA. If, however, the Offset DAC has an output voltage other than 0 V, the input range to the analog inputs will differ from that applied to the input of the PGA.

The Offset DAC has five magnitude bits and one sign bit. The sign bit determines whether the value loaded to the five magnitude bits is added to or subtracted from the voltage at the analog input pins. Control of the Offset DAC is via the DAC Register which is discussed previously in the On-Chip Registers section. With a 5 V reference applied between the REF IN pins, the resolution of the Offset DAC is 2.5 mV with a range that allows addition or subtraction of 77.5 mV. With a 2.5 V reference applied between the REF IN pins, the resolution of the Offset DAC is 1.25 mV with a range that allows addition or subtraction of 38.75 mV.

Following is an example of how the Offset DAC works. If the differential input voltage range the user had at the analog input pins was +20 mV to +30 mV, the Offset DAC should be programmed to subtract 20 mV of offset so the input range to the PGA is 0 mV to +10 mV. If the differential input voltage range the user had at the analog input pins was –60 mV to +20 mV, the Offset DAC should be programmed to add 20 mV of offset so the input range to the PGA is ±40 mV.

Bipolar/Unipolar Inputs

The analog inputs on the AD7730 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that the part can handle negative voltages with respect to system ground on its analog inputs unless the AGND of the part is also biased below system ground. Unipolar and bipolar signals on the AIN(+) input are referenced to the voltage on the respective AIN(–) input. For example, if AIN(–) is +2.5 V and the AD7730 is configured for an analog input range of 0 to +10 mV with no DAC offset correction, the input voltage range on the AIN(+) input is +2.5 V to +2.51 V. Similarly, if AIN(–) is +2.5 V and the AD7730 is configured for an analog input range of ±80 mV with no DAC offset correction, the analog input range on the AIN(+) input is +2.42 V to +2.58 V (i.e., 2.5 V ± 80 mV).

Bipolar or unipolar options are chosen by programming the $\overline{\text{B}}$/U bit of the Mode Register. This programs the selected channel for either unipolar or bipolar operation. Programming the channel for either unipolar or bipolar operation does not change any of the input signal conditioning; it simply changes the data output coding and the points on the transfer function where calibrations occur. When the AD7730 is configured for unipolar operation, the output coding is natural (straight) binary with a zero differential voltage resulting in a code of 000 . . . 000, a midscale voltage resulting in a code of 100 . . . 000 and a full-scale input voltage resulting in a code of 111 . . . 111. When the AD7730 is configured for bipolar operation, the coding is offset binary with a negative full scale voltage resulting in a code of 000 . . . 000, a zero differential voltage resulting in a code of 100 . . . 000 and a positive full scale voltage resulting in a code of 111 . . . 111.

Burnout Currents

The AD7730 contains two 100 nA constant current generators, one source current from AV_{DD} to AIN(+) and one sink current from AIN(–) to AGND. The currents are switched to the selected analog input pair. Both currents are either on or off, depending on the BO bit of the Mode Register. These currents can be used in checking that a transducer is still operational before attempting to take measurements on that channel. If the currents are turned on, allowed flow in the transducer, a measurement of the input voltage on the analog input taken and the voltage measured is full scale, it indicates that the transducer has gone open-circuit. If the voltage measured is 0 V, it indicates that the transducer has gone short circuit. For normal operation, these burnout currents are turned off by writing a 0 to the BO bit. The current sources work over the normal absolute input voltage range specifications.

REFERENCE INPUT

The AD7730's reference inputs, REF IN(+) and REF IN(–), provide a differential reference input capability. The common-mode range for these differential inputs is from AGND to AV_{DD}. The nominal reference voltage, V_{REF} (REF IN(+)—REF IN(–)), for specified operation is +2.5 V with the HIREF bit at 0 V and +5 V with the HIREF bit at 1. The part is also functional with V_{REF} of +2.5 V with the HIREF bit at 1. This results in a halving of all input ranges. The resolution in nV will be unaltered but will appear halved in terms of counts.

Both reference inputs provide a high impedance, dynamic load. The typical average dc input leakage current over temperature is 8.5 µA with HIREF = 1 and V_{REF} = +5 V, and 2.5 µA with HIREF = 0 and V_{REF} = +2.5 V. Because the input impedance of each reference input is dynamic, external resistance/capacitance combinations on these inputs may result in gain errors on the part.

The AD7730 can be operated in either ac or dc mode. If the bridge excitation is fixed dc, the AD7730 should be operated in dc mode. If the analog input and the reference inputs are externally chopped before being applied to the part the AD7730 should be operated in ac mode and not dc mode. In ac mode, it is assumed that both the analog inputs and reference inputs are chopped and as a result change phase every alternate chopping cycle. If the chopping is synchronized by the AD7730 (using the ACX signals to control the chopping) the part then takes into account the reversal of the analog input and reference input signals.

The output noise performance outlined in Tables I through IV is for an analog input of 0 V and is unaffected by noise on the reference. To obtain the same noise performance as shown in the noise tables over the full input range requires a low noise reference source for the AD7730. If the reference noise in the bandwidth of interest is excessive, it will degrade the performance of the AD7730. In applications where the excitation voltage for the bridge transducer on the analog input also drives the reference voltage for the part, the effect of the noise in the excitation voltage will be removed as the application is ratiometric. Figure 7 shows how the reference voltage can be connected in a ratiometric fashion in a dc-excited bridge application. In this case, the excitation voltage for the AD7730 and the transducer is a dc voltage. The HIREF bit of the Mode Register should be set to 1. Figure 8 meanwhile shows how the reference can be connected in a ratiometric fashion in an ac-excited bridge

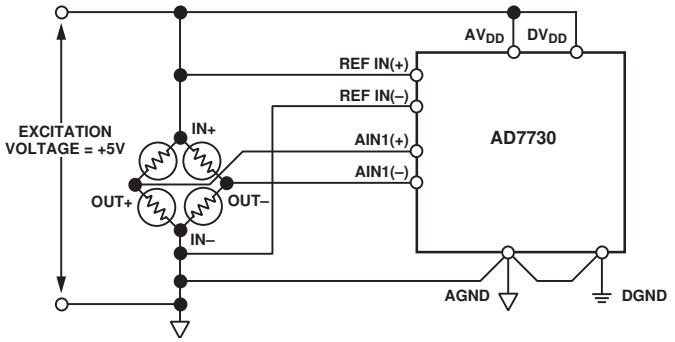


Figure 7. Ratiometric Generation of Reference in DC-Excited Bridge Application

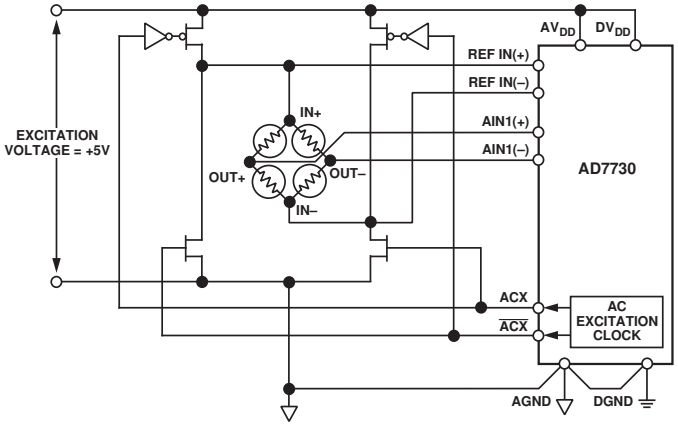


Figure 8. Ratiometric Generation of Reference in AC-Excited Bridge Application

application. In this case, both the reference voltage for the part and the excitation voltage for the transducer are chopped. Once again, the HIREF bit should be set to 1.

If the AD7730 is not used in a ratiometric application, a low noise reference should be used. Recommended 2.5 V reference voltage sources for the AD7730 include the AD780, REF43 and REF192. If any of these references are used as the reference source for the AD7730, the HIREF bit should be set to 0. It is generally recommended to decouple the output of these references to further reduce the noise level.

Reference Detect

The AD7730 includes on-chip circuitry to detect if the part has a valid reference for conversions or calibrations. If the voltage between the REF IN(+) and REF IN(–) pins goes below 0.3 V or either the REF IN(+) or REF IN(–) inputs is open circuit, the AD7730 detects that it no longer has a valid reference. In this case, the NO REF bit of the Status Register is set to a 1.

If the AD7730 is performing normal conversions and the NO REF bit becomes active, the part places all ones in the Data Register. Therefore, it is not necessary to continuously monitor the status of the NO REF bit when performing conversions. It is only necessary to verify its status if the conversion result read from the Data Register is all 1s.