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8-Channel, 16-Bit, Simultaneous Sampling ADC with Power Scaling, 110.8 kHz BW

Data Sheet **AD7761**

FEATURES

- Precision ac and dc performance
- 8-channel simultaneous sampling
  - 256 kSPS ADC output data rate per channel
  - 97.7 dB dynamic range
  - 110.8 kHz input bandwidth (−3 dB bandwidth (BW))
  - −120 dB THD, typical
  - ±1 LSB INL, ±1 LSB offset error, ±5 LSB gain error
- Optimized power dissipation vs. noise vs. input bandwidth
  - Selectable power, speed, and input bandwidth
    - Fast: highest speed; 110.8 kHz BW, 51.5 mW per channel
    - Median: half speed, 55.4 kHz BW, 27.5 mW per channel
    - Focus: lowest power, 13.8 kHz BW, 9.375 mW per channel
  - Input BW range: dc to 110.8 kHz
  - Programmable input bandwidth/sampling rates
- Cyclic redundancy check (CRC) error checking on data interface
- Daisy-chaining
- Linear phase digital filter
  - Low latency sinc5 filter
  - Wideband brick wall filter: ±0.005 dB ripple to 102.4 kHz
- Analog input precharge buffers
- Power supply
  - AVDD1 = 5 V, AVDD2 = 2.25 V to 5.0 V
  - IOVDD = 2.5 V to 3.3 V or IOVDD = 1.8 V
- 64-lead LQFP package, no exposed pad
- Temperature range: −40°C to +105°C

APPLICATIONS

- Data acquisition systems: USB/PXI/Ethernet
- Instrumentation and industrial control loops
- Audio test and measurement
- Vibration and asset condition monitoring
- 3-phase power quality analysis
- Sonar
- High precision medical electroencephalogram (EEG)/ electromyography (EMG)/electrocardiogram (ECG)

FUNCTIONAL BLOCK DIAGRAM

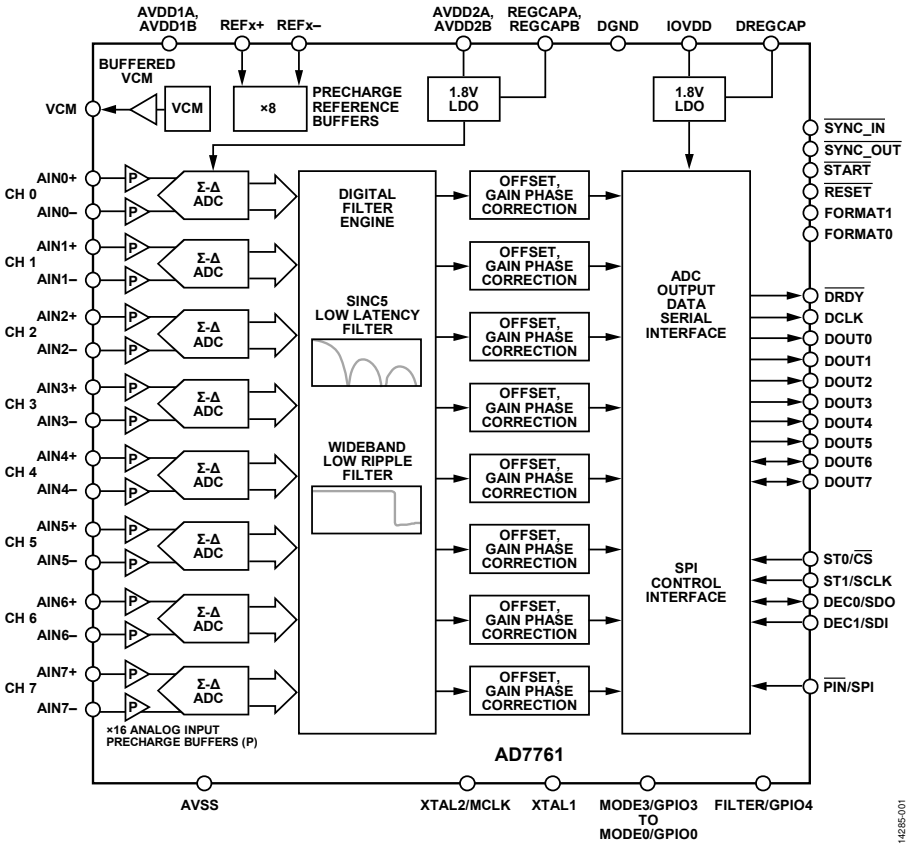

Figure 1.

Rev. 0 **Document Feedback**

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User Guides

- UG-949: Evaluation Board for the AD7761 16-Bit, 8-Channel, Simultaneous Sampling, 256 kSPS, Sigma-Delta ADC with Power Scaling

REFERENCE MATERIALS

Press

- Sigma-Delta A/D Converters Improve Signal Quality Monitoring in Instrumentation, Energy and Healthcare Applications

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- AD7761 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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REVISION HISTORY

4/16—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD7761 is an 8-channel, simultaneous sampling Σ-Δ analog-to-digital converter (ADC) with a Σ-Δ modulator and digital filter per channel, enabling synchronized sampling of ac and dc signals.

The AD7761 achieves 97.7 dB dynamic range at a maximum input bandwidth of 110.8 kHz, combined with typical performance of ±1 LSB integral nonlinearity (INL), ±1 LSB offset error, and ±5 LSB gain error.

The AD7761 user can trade off input bandwidth, output data rate, and power dissipation. Select one of three power modes to optimize for noise targets and power consumption. The flexibility of the AD7761 allows it to become a reusable platform for low power dc and high performance ac measurement modules.

The AD7761 has three modes: fast mode (256 kSPS maximum, 110.8 kHz input bandwidth, 51.5 mW per channel), median mode (128 kSPS maximum, 55.4 kHz input bandwidth, 27.5 mW per channel) and focus mode (32 kSPS maximum, 13.8 kHz input bandwidth, 9.375 mW per channel).

The AD7761 offers extensive digital filtering capabilities, such as a wideband, low ±0.005 dB pass-band ripple, antialiasing low-pass filter with sharp roll-off, and 105 dB attenuation at the Nyquist frequency.

Frequency domain measurements can use the wideband linear phase filter. This filter has a flat pass band (±0.005 dB ripple) from dc to 102.4 kHz at 256 kSPS, from dc to 51.2 kHz at 128 kSPS, or from dc to 12.8 kHz at 32 kSPS.

The AD7761 also offers sinc response via a sinc5 filter, a low latency path for low bandwidth, and low noise measurements. The wideband and sinc5 filters can be selected and run on a per channel basis.

Within these filter options, the user can improve the dynamic range by selecting from decimation rates of ×32, ×64, ×128, ×256, ×512, and ×1024. The ability to vary the decimation filtering optimizes noise performance to the required input bandwidth.

Embedded analog functionality on each ADC channel makes design easier, such as a precharge buffer on each analog input that reduces analog input current and a precharge reference buffer per channel reduces input current and glitches on the reference input terminals.

The device operates with a 5 V AVDD1A and AVDD1B supply, a 2.25 V to 5.0 V AVDD2A and AVDD2B supply, and a 2.5 V to 3.3 V or 1.8 V IOVDD supply (see the 1.8 V IOVDD Operation section for specific requirements for operating at 1.8 V IOVDD).

The device requires an external reference; the absolute input reference voltage range is 1 V to AVDD1 − AVSS.

For the purposes of clarity within this data sheet, the AVDD1A and AVDD1B supplies are referred to as AVDD1 and the AVDD2A and AVDD2B supplies are referred to as AVDD2. For the negative supplies, AVSS refers to the AVSS1A, AVSS1B, AVSS2A, AVSS2B, and AVSS pins.

The specified operating temperature range is −40°C to +105°C. The device is housed in a 10 mm × 10 mm 64-lead LQFP package with a 12 mm × 12 mm printed circuit board (PCB) footprint.

Throughout this data sheet, multifunction pins, such as XTAL2/MCLK, are referred to either by the entire pin name or by a single function of the pin, for example MCLK, when only that function is relevant.

SPECIFICATIONS

AVDD1A = AVDD1B = 4.5 V to 5.5 V, AVDD2A = AVDD2B = 2.0 V to 5.5 V, IOVDD = 1.72 V to 1.88 V and 2.25 V to 3.6 V, AVSS = DGND = 0 V, REFx+ = 4.096 V and REFx− = 0 V, MCLK = 32.768 MHz, analog input precharge buffers on, reference precharge buffers off, wideband filter, $f_{CHOP} = f_{MOD}/32$, T_A = −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPEED AND PERFORMANCE					
Output Data Rate (ODR), per Channel[1]	Fast	8		256	kSPS
	Median	4		128	kSPS
	Focus	1		32	kSPS
−3 dB Bandwidth	Fast, wideband filter			110.8	kHz
	Median, wideband filter			55.4	kHz
	Focus, wideband filter			13.8	kHz
Data Output Coding			Twos complement, MSB first		
No Missing Codes[2]		16			Bits
DYNAMIC PERFORMANCE					
	Decimation by 32, 256 kSPS ODR				
Dynamic Range	Shorted input, wideband filter	97.3	97.7		dB
Signal-to-Noise Ratio (SNR)	1 kHz, −0.5 dBFS, sine wave input				
	Sinc5 filter	97.3	97.9		dB
	Wideband filter	97.3	97.7		dB
Signal-to-Noise-and-Distortion Ratio (SINAD)	1 kHz, −0.5 dBFS, sine wave input	97.3	97.7		dB
Total Harmonic Distortion (THD)	1 kHz, −0.5 dBFS, sine wave input		−120	−107	dB
Spurious-Free Dynamic Range (SFDR)			126		dBc
INTERMODULATON DISTORTION (IMD)	f_{INA} = 9.7 kHz, f_{INB} = 10.3 kHz				
	Second order		−125		dB
	Third order		−124		dB
ACCURACY					
INL[3]	Endpoint method		±1	± 1.5	LSB
Offset Error[4]			±1	±2	LSB
Gain Error[4]	T_A = 25°C		±5	±40	LSB
Gain Drift vs. Temperature[2]			±0.01	±0.02	LSB/°C
VCM PIN					
Output	With respect to AVSS		(AVDD1 − AVSS)/2		V
Load Regulation	$\Delta V_{OUT}/\Delta I_L$		400		µV/mA
Voltage Regulation	Applies to the following VCM output options only: $V_{CM} = \Delta V_{OUT}/\Delta(AVDD1 - AVSS)/2$, V_{CM} = 1.65 V, and V_{CM} = 2.5 V		5		µV/V
Short-Circuit Current			30		mA
ANALOG INPUTS	See the Analog Input section				
Differential Input Voltage Range	V_{REF} = (REFx+) − (REFx−)	$-V_{REF}$		$+V_{REF}$	V
Input Common-Mode Range[2]		AVSS		AVDD1	V
Absolute Analog Input Voltage Limits[2]		AVSS		AVDD1	V
Analog Input Current					
Unbuffered	Differential component		±48		µA/V
	Common-mode component		±17		µA/V
Precharge Buffer On[5]			−20		µA
Input Current Drift					
Unbuffered			±5		nA/V/°C
Precharge Buffer On			±31		nA/°C

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
EXTERNAL REFERENCE					
Reference Voltage	V_{REF} = (REFx+) − (REFx−)	1		AVDD1 − AVSS	V
Absolute Reference Voltage Limits[2]	Precharge reference buffers off	AVSS − 0.05		AVDD1 + 0.05	V
	Precharge reference buffers on	AVSS		AVDD1	V
Average Reference Current	Fast mode				
	Precharge reference buffers off		±72		µA/V/channel
	Precharge reference buffers on		±16		µA/V/channel
Average Reference Current Drift	Fast mode				
	Precharge reference buffers off		±1.7		nA/V/°C
	Precharge reference buffers on		±49		nA/V/°C
Common-Mode Rejection			95		dB
DIGITAL FILTER RESPONSE					
Low Ripple Wideband Filter	FILTER = 0				
Decimation Rate	Up to six selectable decimation rates	32		1024	
Group Delay	Latency		34/ODR		sec
Settling Time	Complete settling		68/ODR		sec
Pass-Band Ripple[2]				±0.005	dB
Pass Band	±0.005 dB bandwidth		0.4 × ODR		Hz
	−0.1 dB bandwidth		0.409 × ODR		Hz
	−3 dB bandwidth		0.433 × ODR		Hz
Stop Band Frequency	Attenuation > 105 dB		0.499 × ODR		Hz
Stop Band Attenuation			105		dB
Sinc5 Filter	FILTER = 1				
Decimation Rate	Up to six selectable decimation rates	32		1024	
Group Delay	Latency		3/ODR		sec
Settling Time	Complete settling		7/ODR		sec
Pass Band	−3 dB bandwidth		0.204 × ODR		Hz
REJECTION					
AC Power Supply Rejection Ratio (PSRR)	V_{IN} = 0.1 V, AVDD1 = 5 V, AVDD2 = 5 V, IOVDD = 2.5 V				
AVDD1			90		dB
AVDD2			100		dB
IOVDD			75		dB
DC PSRR	V_{IN} = 1 V				
AVDD1			100		dB
AVDD2			118		dB
IOVDD			90		dB
Analog Input Common-Mode Rejection Ratio (CMRR)					
DC	V_{IN} = 0.1 V		95		dB
AC	Up to 10 kHz		95		dB
Crosstalk	−0.5 dBFS input on adjacent channels		−120		dB
CLOCK					
Crystal Frequency		8	32.768	34	MHz
External Clock (MCLK)	See the Clock Selection section		32.768		MHz
Duty Cycle	For data sheet performance		50:50		%
MCLK Pulse Width[2]	Functionality				
Logic Low		12.2			ns
Logic High		12.2			ns
CMOS Clock Input Voltage	See the logic inputs parameter				
High, V_{INH}					
Low, V_{INL}					

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LVDS Clock[2]	R_L = 100 Ω				
Differential Input Voltage		100		650	mV
Common-Mode Input Voltage		800		1575	mV
Absolute Input Voltage				1.88	V
ADC RESET[2]					
ADC Start-Up Time After Reset[6]	Time to first $\overline{DRDY}$, fast mode, decimation by 32		1.58	1.66	ms
Minimum $\overline{RESET}$ Low Pulse Width	t_{MCLK} = 1/MCLK	2 × t_{MCLK}			
LOGIC INPUTS					
Input Voltage[2]					
High, V_{INH}		0.65 × IOVDD			V
Low, V_{INL}	2.25 V < IOVDD < 3.6 V			0.7	V
	1.72 V < IOVDD < 1.88 V			0.4	V
Hysteresis[2]	2.25 V < IOVDD < 3.6 V	0.04		0.09	V
	1.72 V < IOVDD < 1.88 V	0.04		0.2	V
Leakage Current		−10	+0.03	+10	µA
	$\overline{RESET}$ pin[7]	−10		+10	µA
LOGIC OUTPUTS					
Output Voltage[2]					
High, V_{OH}	I_{SOURCE} = 200 µA	0.8 × IOVDD			V
Low, V_{OL}	I_{SINK} = 400 µA			0.4	V
Leakage Current	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF
SYSTEM CALIBRATION[2]					
Full-Scale Calibration Limit				1.05 × V_{REF}	V
Zero-Scale Calibration Limit		−1.05 × V_{REF}			V
Input Span		0.4 × V_{REF}		2.1 × V_{REF}	V
POWER REQUIREMENTS					
Power Supply Voltage					
AVDD1 − AVSS		4.5	5.0	5.5	V
AVDD2 − AVSS		2.0	2.25 to 5.0	5.5	V
AVSS − DGND		−2.75		0	V
IOVDD − DGND		1.72	1.8 or 2.5 to 3.3	3.6	V
POWER SUPPLY CURRENTS	Maximum output data rate, CMOS MCLK, eight DOUTx signals, all supplies at maximum voltages, all channels in Channel Mode A				
Eight Channels Active					
Fast Mode					
AVDD1 Current	Precharge reference buffers off/on		36/57.5	40/64	mA
AVDD2 Current			37.5	40	mA
IOVDD Current	Wideband filter		63	69	mA
	Sinc5 filter[2]		27	29	mA
Median Mode					
AVDD1 Current	Precharge reference buffers off/on		18.5/29		mA
AVDD2 Current			21.3		mA
IOVDD Current	Wideband filter		34		mA
	Sinc5 filter		16		mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Focus Mode					
AVDD1 Current	Precharge reference buffers off/on		5.1/8		mA
AVDD2 Current			9.3		mA
IOVDD Current	Wideband filter		12.5		mA
	Sinc5 filter		8		mA
Four Channels Active[2]					
Fast Mode					
AVDD1 Current	Precharge reference buffers off/on		18.2/28.8	20.3/32.5	mA
AVDD2 Current			18.8	20.3	mA
IOVDD Current	Wideband filter		43.5	47.7	mA
	Sinc5 filter		17	18.6	mA
Median Mode					
AVDD1 Current	Precharge reference buffers off/on		9.3/14.7		mA
AVDD2 Current			10.7		mA
IOVDD Current	Wideband filter		24.5		mA
	Sinc5 filter		11		mA
Focus Mode					
AVDD1 Current	Precharge reference buffers off/on		2.7/4.1		mA
AVDD2 Current			4.7		mA
IOVDD Current	Wideband filter		10		mA
	Sinc5 filter		6.5		mA
Two Channels Active[2]					
Fast Mode					
AVDD1 Current	Precharge reference buffers off/on		9.3/14.7	10.5/16.6	mA
AVDD2 Current			9.5	10.5	mA
IOVDD Current	Wideband filter		34	36.7	mA
	Sinc5 filter		12	13.5	mA
Median Mode					
AVDD1 Current	Precharge reference buffers off/on		4.8/7.5		mA
AVDD2 Current			5.5		mA
IOVDD Current	Wideband filter		19.5		mA
	Sinc5 filter		8.5		mA
Focus Mode					
AVDD1 Current	Precharge reference buffers off/on		1.52/2.2		mA
AVDD2 Current			2.4		mA
IOVDD Current	Wideband filter		8.6		mA
	Sinc5 filter		5.8		mA
Standby Mode	All channels disabled (sinc5 filter enabled)		6.5	8	mA
Sleep Mode	Full power-down (serial peripheral interface (SPI) mode only)		0.73	1.2	mA
Crystal Excitation Current	Extra current in IOVDD when using an external crystal compared to using the CMOS MCLK		540		µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER DISSIPATION	External CMOS MCLK, all channels active, MCLK = 32.768 MHz, all channels in Channel Mode A				
Full Operating Mode	Analog precharge buffers on				
Wideband Filter					
Fast	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off[2]		412	446	mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on[2]		600	645	mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off		631	681	mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 1.88 V, precharge reference buffers off[2]		524	571	mW
Median	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off		220		mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on		320		mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off		341		mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 1.88 V, precharge reference buffers off		284		mW
Focus	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off		75		mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on		107		mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off		124		mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 1.88 V, precharge reference buffers off		99		mW
Sinc5 Filter[2]					
Fast	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off		325	355	mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on		475	525	mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off		501	545	mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 1.88 V, precharge reference buffers off		455	495	mW
Median	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off		175		mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on		260		mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off		277		mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 1.88 V, precharge reference buffers off		248		mW

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Focus	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off		65		mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on		95		mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off		108		mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 1.88 V, precharge reference buffers off		94		mW
Standby Mode	All channels disabled; AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V		14.5		mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V		21		mW
	AVDD1 = AVDD2 = 5.5 V, IOVDD = 3.6 V		23.5	29	mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 1.88 V		12.5		mW
Sleep Mode	Full power-down (SPI mode only); AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V		1.8		mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V		2.5		mW
	AVDD1 = AVDD2 = 5.5 V, IOVDD = 3.6 V		2.7	6.5	mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 1.88 V		1.5		mW

[1] The output data rate ranges refer to the programmable decimation rates available on the AD7761 for a fixed MCLK rate of 32.768 MHz. Varying MCLK rates allow users a wider variation of ODR.
[2] These specifications are not production tested but are supported by characterization data at initial product release.
[3] The maximum INL specification is guaranteed by design and characterization testing prior to release. This specification is not production tested.
[4] Following a system zero-scale calibration, the offset error is in the order of the noise for the programmed output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed output data rate.
[5] −25 µA is measured when the analog input is close to either the AVDD1 or AVSS rail. The input current reduces as the common-mode voltage approaches (AVDD1 − AVSS)/2. The analog input current scales with the MCLK frequency and device power mode.
[6] For lower MCLK rates or higher decimation rates, use Table 31 and Table 32 to calculate any additional delay before the first $\overline{DRDY}$ pulse.
[7] The $\overline{RESET}$ pin has an internal pull-up device to IOVDD.

TIMING SPECIFICATIONS

AVDD1A = AVDD1B = 5 V, AVDD2A = AVDD2B = 5 V, IOVDD = 2.25 V to 3.6 V, Input Logic 0 = DGND, Input Logic 1 = IOVDD; C_{LOAD} = 10 pF on the DCLK pin, C_{LOAD} = 20 pF on the other digital outputs; REFx+ = 4.096 V, T_A = −40°C to +105°C. See Table 4 and Table 5 for timing specifications at 1.8 V IOVDD.

Table 2. Data Interface Timing[1]

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
MCLK	Master clock		1.15		34	MHz
f_{MOD}	Modulator frequency	Fast mode		MCLK/4		Hz
		Median mode		MCLK/8		Hz
		Focus mode		MCLK/32		Hz
t_1	$\overline{DRDY}$ high time	$t_{DCLK} = t_8 + t_9$	t_{DCLK} − 10%	28		ns
t_2	DCLK rising edge to $\overline{DRDY}$ rising edge				2	ns
t_3	DCLK rising to $\overline{DRDY}$ falling		−3.5		0	ns
t_4	DCLK rise to DOUTx valid				1.5	ns
t_5	DCLK rise to DOUTx invalid		−3			ns
t_6	DOUTx valid to DCLK falling		9.5	$t_{DCLK}/2$		ns
t_7	DCLK falling edge to DOUTx invalid		9.5	$t_{DCLK}/2$		ns
t_8	DCLK high time, DCLK = MCLK/1	50:50 CMOS clock	$t_{DCLK}/2$	$t_{DCLK}/2$	$(t_{DCLK}/2) + 5$	ns
	t_{8a} = DCLK = MCLK/2	t_{MCLK} = 1/MCLK		t_{MCLK}		ns
	t_{8b} = DCLK = MCLK/4			$2 \times t_{MCLK}$		ns
	t_{8c} = DCLK = MCLK/8			$4 \times t_{MCLK}$		ns

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_9	DCLK low time DCLK = MCLK/1	50:50 CMOS clock	$(t_{DCLK}/2) - 5$	$t_{MCLK}/2$	$t_{DCLK}/2$	ns
	t_{9a} = DCLK = MCLK/2			t_{MCLK}		ns
	t_{9b} = DCLK = MCLK/4			$2 \times t_{MCLK}$		ns
	t_{9c} = DCLK = MCLK/8			$4 \times t_{MCLK}$		ns
t_{10}	MCLK rising to DCLK rising	CMOS clock			30	ns
t_{11}	Setup time of DOUT6 and DOUT7		14			ns
t_{12}	Hold time of DOUT6 and DOUT7		0			ns
t_{13}	$\overline{START}$ low time		$1 \times t_{MCLK}$			ns
t_{14}	MCLK to $\overline{SYNC\_OUT}$ valid	CMOS clock				
		$\overline{SYNC\_OUT}$ RETIME_EN bit disabled; measured from falling edge of MCLK	4.5		22	ns
		$\overline{SYNC\_OUT}$ RETIME_EN bit enabled; measured from rising edge of MCLK	9.5		27.5	ns
t_{15}	$\overline{SYNC\_IN}$ setup time	CMOS clock	0			ns
t_{16}	$\overline{SYNC\_IN}$ hold time	CMOS clock	10			ns

[1] These specifications are not production tested but are supported by characterization data at initial product release.

Table 3. SPI Control Interface Timing[1]

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{17}	SCLK period		100			ns
t_{18}	$\overline{CS}$ falling edge to SCLK rising edge		26.5			ns
t_{19}	SCLK falling edge to $\overline{CS}$ rising edge		27			ns
t_{20}	$\overline{CS}$ falling edge to data output enable		22.5		40.5	ns
t_{21}	SCLK high time		20	50		ns
t_{22}	SCLK low time		20	50		ns
t_{23}	SCLK falling edge to SDO valid				15	ns
t_{24}	SDO hold time after SCLK falling		7			ns
t_{25}	SDI setup time		0			ns
t_{26}	SDI hold time		6			ns
t_{27}	SCLK enable time		0			ns
t_{28}	SCLK disable time		0			ns
t_{29}	$\overline{CS}$ high time		10			ns
t_{30}	$\overline{CS}$ low time	f_{MOD} = MCLK/4	$1.1 \times t_{MCLK}$			ns
		f_{MOD} = MCLK/8	$2.2 \times t_{MCLK}$			ns
		f_{MOD} = MCLK/32	$8.8 \times t_{MCLK}$			ns

[1] These specifications are not production tested but are supported by characterization data at initial product release.

1.8 V IOVDD TIMING SPECIFICATIONS

AVDD1A = AVDD1B = 5 V, AVDD2A = AVDD2B = 5 V, IOVDD = 1.72 V to 1.88 V (DREGCAP tied to IOVDD), Input Logic 0 = DGND, Input Logic 1 = IOVDD, C_{LOAD} = 10 pF on DCLK pin, C_{LOAD} = 20 pF on other digital outputs, T_A = −40°C to +105°C.

Table 4. Data Interface Timing[1]

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
MCLK	Master clock		1.15		34	MHz
f_{MOD}	Modulator frequency	Fast mode		MCLK/4		Hz
		Median mode		MCLK/8		Hz
		Focus mode		MCLK/32		Hz
t_1	$\overline{DRDY}$ high time		t_{DCLK} − 10%	28		ns
t_2	DCLK rising edge to $\overline{DRDY}$ rising edge				2	ns

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_3	DCLK rising to $\overline{DRDY}$ falling		−4.5		0	ns
t_4	DCLK rise to DOUTx valid				2.0	ns
t_5	DCLK rise to DOUTx invalid		−4			ns
t_6	DOUTx valid to DCLK falling		8.5	$t_{DCLK}/2$		ns
t_7	DCLK falling edge to DOUTx invalid		8.5	$t_{DCLK}/2$		ns
t_8	DCLK high time, DCLK = MCLK/1	50:50 CMOS clock	$t_{DCLK}/2$	$t_{DCLK}/2$	$(t_{DCLK}/2) + 5$	ns
	t_{8a} = DCLK = MCLK/2			t_{MCLK}		ns
	t_{8b} = DCLK = MCLK/4			$2 \times t_{MCLK}$		ns
	t_{8c} = DCLK = MCLK/8			$4 \times t_{MCLK}$		ns
t_9	DCLK low time DCLK = MCLK/1	50:50 CMOS clock	$(t_{DCLK}/2) - 5$	$t_{MCLK}/2$	$t_{DCLK}/2$	ns
	t_{9a} = DCLK = MCLK/2			t_{MCLK}		ns
	t_{9b} = DCLK = MCLK/4			$2 \times t_{MCLK}$		ns
	t_{9c} = DCLK = MCLK/8			$4 \times t_{MCLK}$		ns
t_{10}	MCLK rising to DCLK rising	CMOS clock			37	ns
t_{11}	Setup time DOUT6 and DOUT7		14			ns
t_{12}	Hold time DOUT6 and DOUT7		0			ns
t_{13}	$\overline{START}$ low time		$1 \times t_{MCLK}$			ns
t_{14}	MCLK to $\overline{SYNC\_OUT}$ valid	CMOS clock				
		$\overline{SYNC\_OUT}$ RETIME_EN bit disabled; measured from falling edge of MCLK	10		31	ns
		$\overline{SYNC\_OUT}$ RETIME_EN bit enabled; measured from rising edge of MCLK	15		37	ns
t_{15}	$\overline{SYNC\_IN}$ setup time	CMOS clock	0			ns
t_{16}	$\overline{SYNC\_IN}$ hold time	CMOS clock	11			ns

[1] These specifications are not production tested but are supported by characterization data at initial product release.

Table 5. SPI Control Interface Timing[1]

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{17}	SCLK period		100			ns
t_{18}	$\overline{CS}$ falling edge to SCLK rising edge		31.5			ns
t_{19}	SCLK falling edge to $\overline{CS}$ rising edge		30			ns
t_{20}	$\overline{CS}$ falling edge to data output enable		29		54	ns
t_{21}	SCLK high time		20	50		ns
t_{22}	SCLK low time		20	50		ns
t_{23}	SCLK falling edge to SDO valid				16	ns
t_{24}	SDO hold time after SCLK falling		7			ns
t_{25}	SDI setup time		0			ns
t_{26}	SDI hold time		10			ns
t_{27}	SCLK enable time		0			ns
t_{28}	SCLK disable time		0			ns
t_{29}	$\overline{CS}$ high time		10			ns
t_{30}	$\overline{CS}$ low time	f_{MOD} = MCLK/4	$1.1 \times t_{MCLK}$			ns
		f_{MOD} = MCLK/8	$2.2 \times t_{MCLK}$			ns
		f_{MOD} = MCLK/32	$8.8 \times t_{MCLK}$			ns

[1] These specifications are not production tested but are supported by characterization data at initial product release.

Timing Diagrams

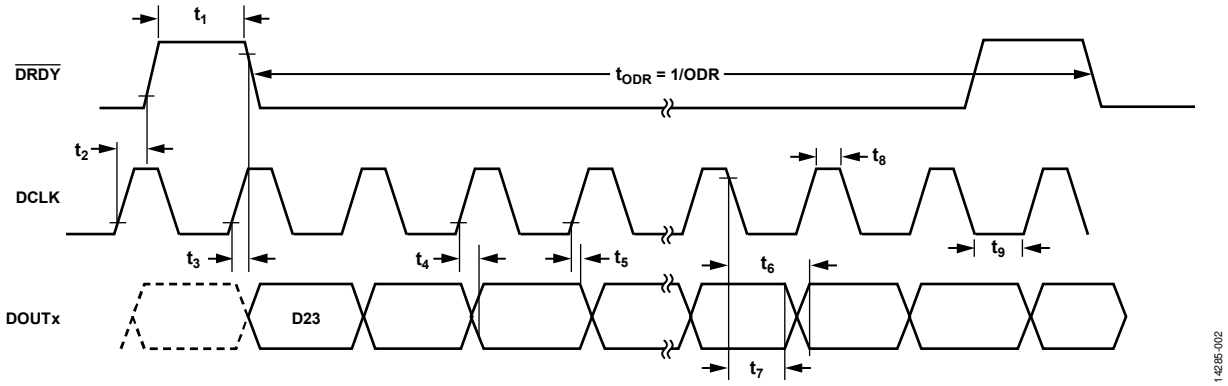

Figure 2. Data Interface Timing Diagram

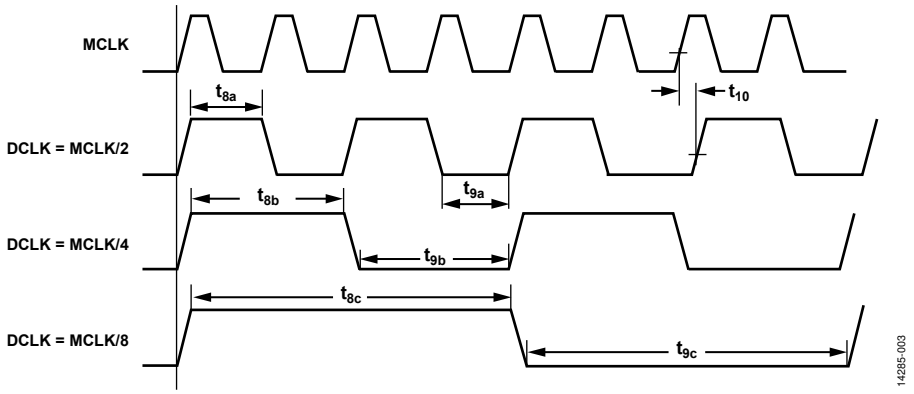

Figure 3. MCLK to DCLK Divider Timing Diagram

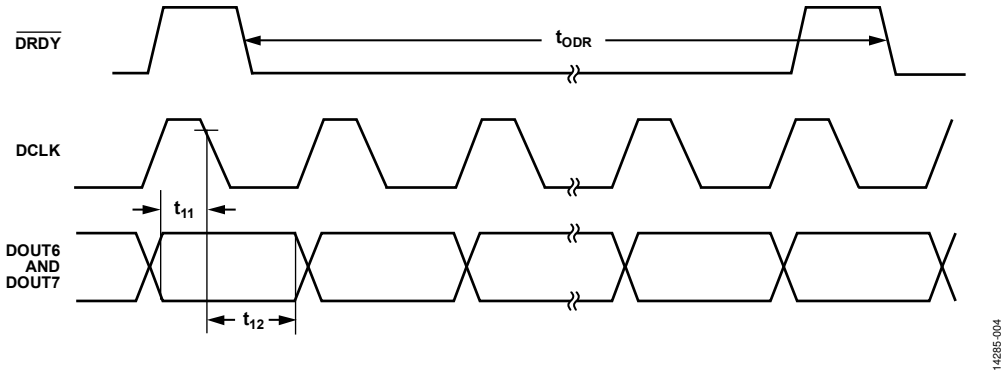

Figure 4. Daisy-Chain Setup and Hold Timing Diagram

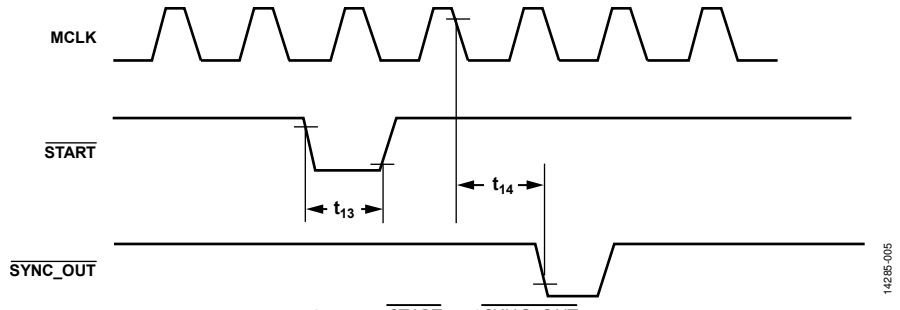

Figure 5. Asynchronous START and SYNC_OUT Timing Diagram

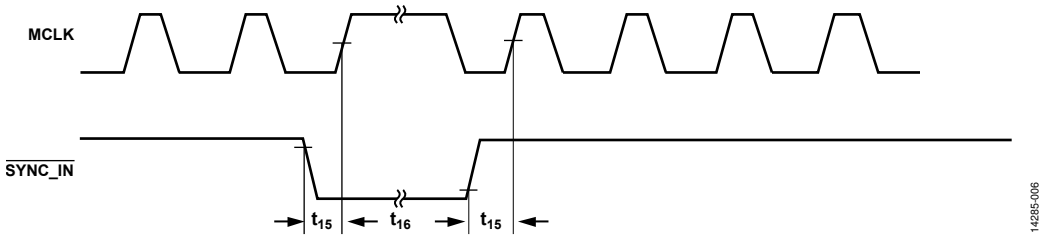

Figure 6. Synchronous $\overline{SYNC\_IN}$ Pulse Timing Diagram

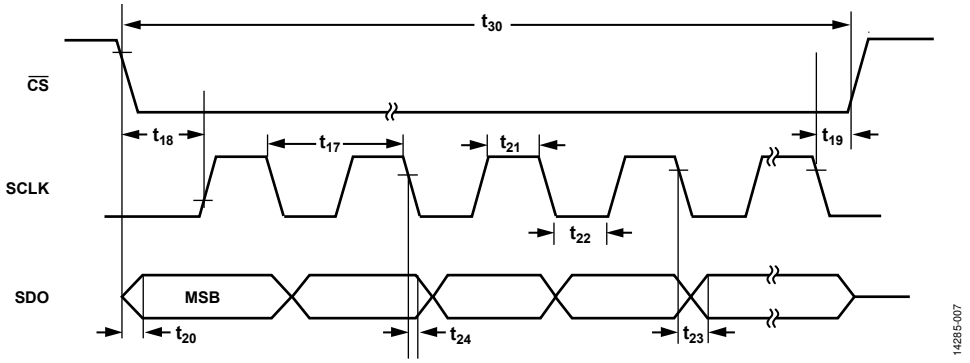

Figure 7. SPI Serial Read Timing Diagram

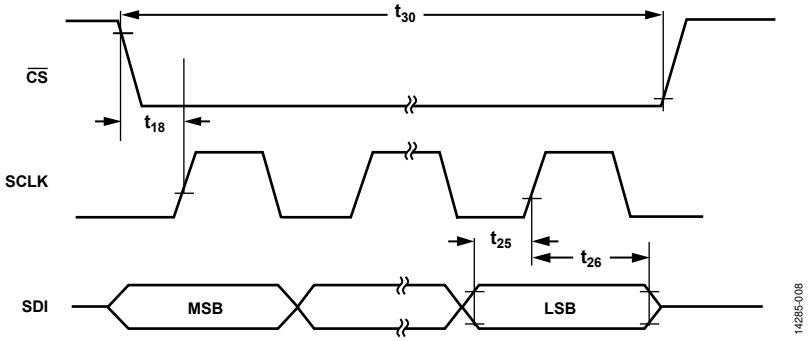

Figure 8. SPI Serial Write Timing Diagram

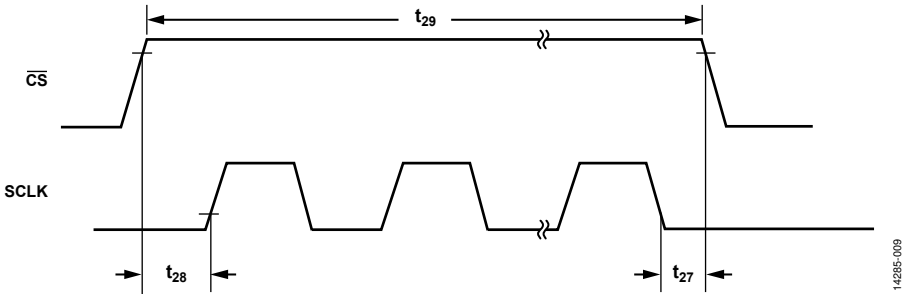

Figure 9. SCLK Enable and Disable Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVDD1, AVDD2 to AVSS[1]	−0.3 V to +6.5 V
AVDD1 to DGND	−0.3 V to +6.5 V
IOVDD to DGND	−0.3 V to +6.5 V
IOVDD, DREGCAP to DGND (IOVDD Tied to DREGCAP for 1.8 V Operation)	−0.3 V to +2.25 V
IOVDD to AVSS	−0.3 V to +7.5 V
AVSS to DGND	−3.25 V to +0.3 V
Analog Input Voltage to AVSS	−0.3 V to AVDD1 + 0.3 V
Reference Input Voltage to AVSS	−0.3 V to AVDD1 + 0.3 V
Digital Input Voltage to DGND	−0.3 V to IOVDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to IOVDD + 0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Pb-Free Temperature, Soldering Reflow (10 sec to 30 sec)	260°C
Maximum Junction Temperature	150°C
Maximum Package Classification Temperature	260°C

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit	JEDEC Board Layers
64-Lead LQFP	38	9.2	°C/W	2P2S[1]

2P2S is a JEDEC standard PCB configuration per JEDEC Standard JESD51-7.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

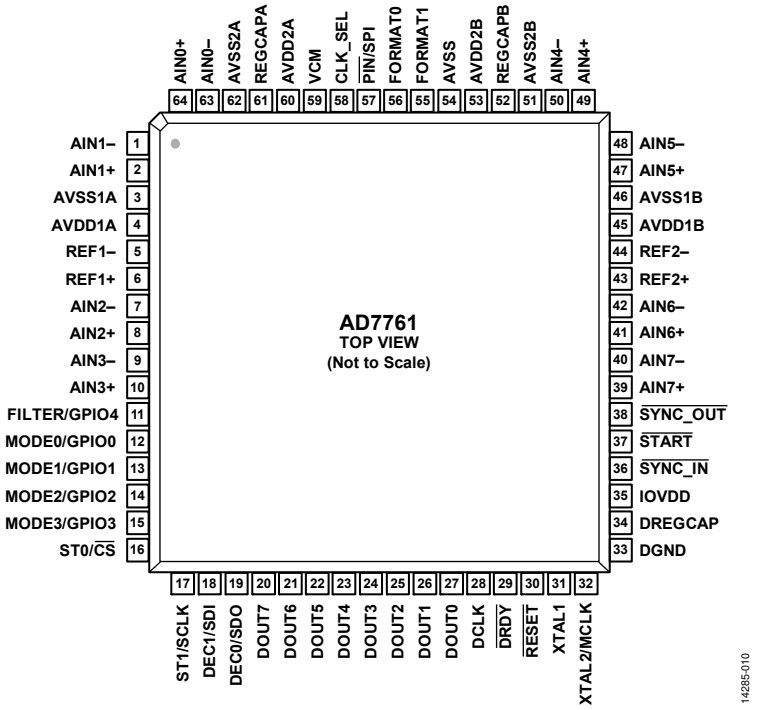

Figure 10. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	AIN1−	AI	Negative Analog Input to ADC Channel 1.
2	AIN1+	AI	Positive Analog Input to ADC Channel 1.
3	AVSS1A	P	Negative Analog Supply. This pin is nominally 0 V.
4	AVDD1A	P	Analog Supply Voltage, 5 V ± 10% with Respect to AVSS.
5	REF1−	AI	Reference Input Negative. REF1− is the negative reference terminal for Channel 0 to Channel 3. The REF1− voltage range is from AVSS to (AVDD1 − 1 V). Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 3.
6	REF1+	AI	Reference Input Positive. REF1+ is the positive reference terminal for Channel 0 to Channel 3. The REF1+ voltage range is from (AVSS + 1 V) to AVDD1. Apply an external reference differential between REF1+ and REF1− in the range from 1 V to |AVDD1 − AVSS|. Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 3.
7	AIN2−	AI	Negative Analog Input to ADC Channel 2.
8	AIN2+	AI	Positive Analog Input to ADC Channel 2.
9	AIN3−	AI	Negative Analog Input to ADC Channel 3.
10	AIN3+	AI	Positive Analog Input to ADC Channel 3.
11	FILTER/GPIO4	DI/O	Filter Select/General-Purpose Input/Output 4. In pin control mode, this pin selects the filter type. Set this pin to Logic 1 for the sinc5 filter. This sinc5 filter is a low latency filter, and is best for dc applications or where a user has specialized postfiltering implemented off chip. Set this pin to Logic 0 for the wideband low ripple filter response. This filter has a steep transition band and 105 dB stop band attenuation. Full attenuation at Nyquist (ODR/2) means that no aliasing occurs at ODR/2 out to the first chopping zone. When in SPI control mode, this pin can be used as a general-purpose input/output (GPIO4).

Pin No.	Mnemonic	Type[1]	Description
12, 13, 14, 15	MODE0/GPIO0, MODE1/GPIO1, MODE2/GPIO2, MODE3/GPIO3	DI/DI/O	Mode Selection/General-Purpose Input/Output Pin 0 to Pin 3. In pin control mode, the MODEx pins set the mode of operation for all ADC channels, controlling power consumption, DCLK frequency, and the ADC conversion type, allowing one-shot conversion operation. In SPI control mode, the GPIOx pins, in addition to the FILTER/GPIO4 pin, form five general-purpose input/output pins (GPIO4 to GPIO0).
16	ST0/$\overline{CS}$	DI	Standby 0/Chip Select Input. In pin control mode, a Logic 1 places Channel 0 to Channel 3 into standby mode. In SPI control mode, this pin is the active low chip select input to the SPI control interface.
17	ST1/SCLK	DI	Standby 1/Serial Clock Input. In pin control mode, a Logic 1 places Channel 4 to Channel 7 into standby mode. In SPI control mode, this pin is the serial clock input pin for the SPI control interface.
18	DEC1/SDI	DI	Decimation Rate Control Input 1/Serial Data Input. In pin control mode, the DEC0 and DEC1 pins configure the decimation rate for all ADC channels. In SPI control mode, this pin is the serial data input pin used to write data to the AD7761 register bank.
19	DEC0/SDO	DI/O	Decimation Rate Control Input 0/Serial Data Output. In pin control mode, the DEC0 and DEC1 pins configure the decimation rate for all ADC channels. In SPI control mode, this pin is the serial data output pin, allowing readback from the AD7761 registers.
20	DOUT7	DI/O	Conversion Data Output 7. This pin is synchronous to DCLK and framed by $\overline{DRDY}$. This pin acts as a digital input from a separate AD7761 device if configured in a synchronized multidevice daisy chain when the FORMATx pins are configured as 01. To use the AD7761 in a daisy chain, hardwire the FORMATx pins as either 01, 10, or 11, depending on the best interfacing format for the application. When FORMATx is set to 10 or 11, connect this pin to ground through a pull-down resistor.
21	DOUT6	DI/O	Conversion Data Output 6. This pin is synchronous to DCLK and framed by $\overline{DRDY}$. This pin acts as a digital input from a separate AD7761 device if configured in a synchronized multidevice daisy chain. To use this pin in a daisy chain, hardwire the FORMATx pins as either 01, 10, or 11, depending on the best interfacing format for the application.
22	DOUT5	DO	Conversion Data Output 5. This pin is synchronous to DCLK and framed by $\overline{DRDY}$.
23	DOUT4	DO	Conversion Data Output 4. This pin is synchronous to DCLK and framed by $\overline{DRDY}$.
24	DOUT3	DO	Conversion Data Output 3. This pin is synchronous to DCLK and framed by $\overline{DRDY}$.
25	DOUT2	DO	Conversion Data Output 2. This pin is synchronous to DCLK and framed by $\overline{DRDY}$.
26	DOUT1	DO	Conversion Data Output 1. This pin is synchronous to DCLK and framed by $\overline{DRDY}$.
27	DOUT0	DO	Conversion Data Output 0. This pin is synchronous to DCLK and framed by $\overline{DRDY}$
28	DCLK	DO	ADC Conversion Data Clock. This pin clocks conversion data out to the digital host (DSP/FPGA). This pin is synchronous with $\overline{DRDY}$ and any conversion data output on DOUT0 to DOUT7 and is derived from the MCLK signal. This pin is unrelated to the control SPI interface.
29	$\overline{DRDY}$	DO	Data Ready. Periodic signal output framing the conversion results from the eight ADCs. This pin is synchronous to DCLK and DOUT0 to DOUT7.
30	$\overline{RESET}$	DI	Hardware Asynchronous Reset Input. After the device is fully powered up, it is recommended to perform a hard or soft reset.
31	XTAL1	DI	Input 1 for Crystal or Connection to an LVDS Clock. When CLK_SEL is 0, connect XTAL1 to DGND.
32	XTAL2/MCLK	DI	Input 2 for CMOS or Crystal/LVDS Sampling Clock. See the CLK_SEL pin for the details of this configuration. External crystal: XTAL2 is connected to the external crystal. LVDS: a second LVDS input is connected to this pin. CMOS clock: this pin operates as an MCLK input. CMOS input with logic level of IOVDD/DGND.
33	DGND	P	Digital Ground. This pin is nominally 0 V.
34	DREGCAP	AO	Digital Low Dropout (LDO) Regulator Output. Decouple this pin to DGND with a high quality, low ESR, 10 µF capacitor. For optimum performance, use a decoupling capacitor with an ESR specification between 50 mΩ and 400 mΩ. This pin is not for use in circuits external to the AD7761. For 1.8 V IOVDD operation, connect this pin to IOVDD via an external trace to provide power to the digital processing core.

Pin No.	Mnemonic	Type[1]	Description
35	IOVDD	P	Digital Supply. This pin sets the logic levels for all interface pins. IOVDD also powers the digital processing core via the digital LDO when IOVDD is at least 2.25 V. For 1.8 V IOVDD operation, connect this pin to DREGCAP via an external trace to provide power to the digital processing core.
36	$\overline{\text{SYNC\_IN}}$	DI	Synchronization Input. $\overline{\text{SYNC\_IN}}$ receives the synchronous signal from $\overline{\text{SYNC\_OUT}}$. It is used in the synchronization of any AD7761 that requires simultaneous sampling or is in a daisy chain. Ignore the $\overline{\text{START}}$ and $\overline{\text{SYNC\_OUT}}$ functions if the $\overline{\text{SYNC\_IN}}$ pin is connected to the system synchronization pulse. This signal pulse must be synchronous to the MCLK clock domain.
37	$\overline{\text{START}}$	DI	Start Signal. The $\overline{\text{START}}$ pulse synchronizes the AD7761 to other devices. The signal can be asynchronous. The AD7761 samples the input and then outputs a $\overline{\text{SYNC\_OUT}}$ pulse. This $\overline{\text{SYNC\_OUT}}$ pulse must be routed to the $\overline{\text{SYNC\_IN}}$ pin of this device, and any other AD7761 devices that must be synchronized together. This means that the user does not need to run the ADCs and their digital host from the same clock domain, which is useful when there are long traces or back planes between the ADC and the controller. If this pin is not used, it must be tied to a Logic 1 through a pull-up resistor.
38	$\overline{\text{SYNC\_OUT}}$	DO	Synchronization Output. This pin operates only when the $\overline{\text{START}}$ input is used. When using the $\overline{\text{START}}$ input feature, the $\overline{\text{SYNC\_OUT}}$ pin must be connected to $\overline{\text{SYNC\_IN}}$ via an external trace. $\overline{\text{SYNC\_OUT}}$ is a digital output that is synchronous to the MCLK signal; the synchronization signal driven in on $\overline{\text{START}}$ is internally synchronized to the MCLK signal and is driven out on $\overline{\text{SYNC\_OUT}}$. $\overline{\text{SYNC\_OUT}}$ can also be routed to other AD7761 devices requiring simultaneous sampling and/or daisy-chaining, ensuring synchronization of devices related to the MCLK clock domain. It must then be wired to drive the $\overline{\text{SYNC\_IN}}$ pin on the same AD7761 and on the other AD7761 devices.
39	AIN7+	AI	Positive Analog Input to ADC Channel 7.
40	AIN7−	AI	Negative Analog Input to ADC Channel 7.
41	AIN6+	AI	Positive Analog Input to ADC Channel 6.
42	AIN6−	AI	Negative Analog Input to ADC Channel 6.
43	REF2+	AI	Reference Input Positive. REF2+ is the positive reference terminal for Channel 4 to Channel 7. The REF2+ voltage range is from (AVSS + 1 V) to AVDD1. Apply an external reference differential between REF2+ and REF2− in the range from 1 V to |AVDD1 − AVSS|. Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 46.
44	REF2−	AI	Reference Input Negative. REF2− is the negative reference terminal for Channel 4 to Channel 7. The REF2− voltage range is from AVSS to (AVDD1 − 1 V). Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 46.
45	AVDD1B	P	Analog Supply Voltage. This pin is 5 V ± 10% with respect to AVSS.
46	AVSS1B	P	Negative Analog Supply. This pin is nominally 0 V.
47	AIN5+	AI	Positive Analog Input to ADC Channel 5.
48	AIN5−	AI	Negative Analog Input to ADC Channel 5.
49	AIN4+	AI	Positive Analog Input to ADC Channel 4.
50	AIN4−	AI	Negative Analog Input to ADC Channel 4.
51	AVSS2B	P	Negative Analog Supply. This pin is nominally 0 V.
52	REGCAPB	AO	Analog LDO Regulator Output. Decouple this pin to AVSS with a 1 µF capacitor.
53	AVDD2B	P	Analog Supply Voltage. This pin is 2 V to 5.5 V with respect to AVSS.
54	AVSS	P	Negative Analog Supply. This pin is nominally 0 V.
55, 56	FORMAT1, FORMAT0	DI	Format Selection Pins. Hardwire the FORMATx pins to the required values in pin control and SPI control mode. These pins set the number of DOUTx pins used to output ADC conversion data. The FORMATx pins are checked by the AD7761 on power-up; the AD7761 then remains in this data output configuration.
57	$\overline{\text{PIN}}$/SPI	DI	Pin Control/SPI Control. This pin sets the control method. Logic 0 = pin control mode for the AD7761. Pin control mode allows pin strapped configuration of the AD7761 by tying logic input pins to the required logic levels. Tie the logic pins (MODE0 to MODE4, DEC0 and DEC1, and FILTER) as required for the configuration. Logic 1 = SPI control mode for the AD7761. Use the SPI control interface signals ($\overline{\text{CS}}$, SCLK, SDI, and SDO) for reading and writing to the AD7761 memory map.

Pin No.	Mnemonic	Type[1]	Description
58	CLK_SEL	DI	Clock Select. 0 = pull this pin low for the CMOS clock option. The clock is applied to Pin 32 (connect Pin 31 to DGND). 1 = pull this pin high for the crystal or LVDS clock option. The crystal or LVDS clock is applied to Pin 31 and Pin 32. The LVDS option is available only in SPI control mode. A write is required to enable the LVDS clock option.
59	VCM	AO	Common-Mode Voltage Output. This pin outputs (AVDD1 − AVSS)/2, which is 2.5 V by default in pin control mode. Configure this pin to (AVDD1 − AVSS)/2, 2.5 V, 2.14 V, or 1.65 V in SPI control mode. When driving capacitive loads larger than 0.1 µF, it is recommended to place a 50 Ω series resistor between this pin and the capacitive load for stability.
60	AVDD2A	P	Analog Supply Voltage. This pin is 2 V to 5.5 V with respect to AVSS.
61	REGCAPA	AO	Analog LDO Regulator Output. Decouple this pin to AVSS with a 1 µF capacitor.
62	AVSS2A	P	Negative Analog Supply. This pin is nominally 0 V.
63	AIN0−	AI	Negative Analog Input to ADC Channel 0.
64	AIN0+	AI	Positive Analog Input to ADC Channel 0.

[1] AI is analog input, P is power, DI/O is digital input/output, DI is digital input, DO is digital output, and AO is analog output.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 5 V, AVDD2 = 2.5 V, AVSS = 0 V, IOVDD = 2.5 V, V_{REF} = 4.096 V, T_A = 25°C, wideband filter, decimation = ×32, MCLK = 32.768 MHz, analog input precharge buffers on, precharge reference buffers off, unless otherwise noted.

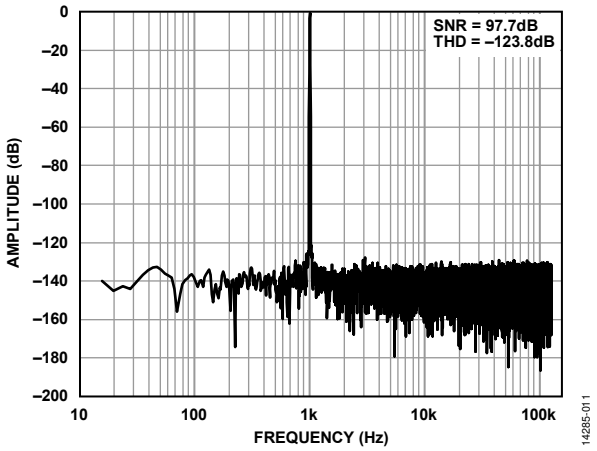

Figure 11. FFT, Fast Mode, Wideband Filter, –0.5 dBFS

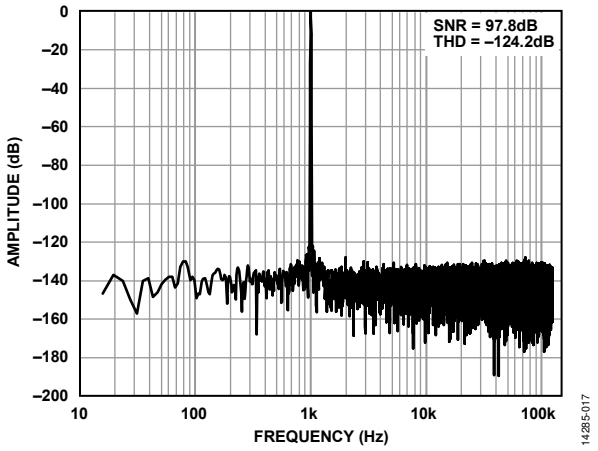

Figure 14. FFT, Fast Mode, Sinc5 Filter, –0.5 dBFS

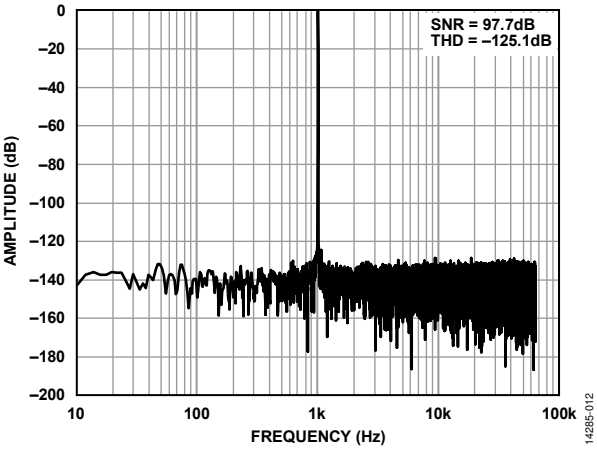

Figure 12. FFT, Median Mode, Wideband Filter, –0.5 dBFS

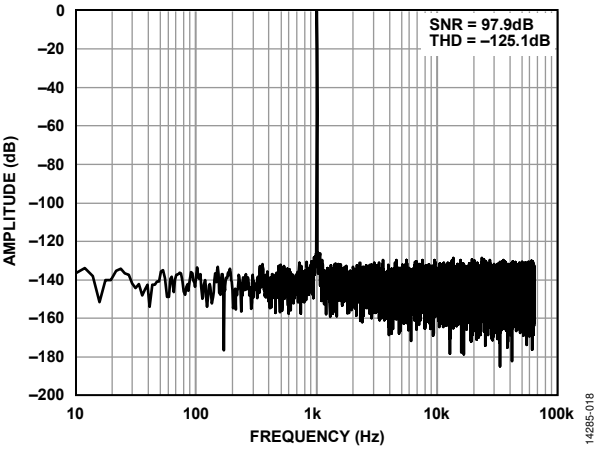

Figure 15. FFT, Median Mode, Sinc5 Filter, –0.5 dBFS

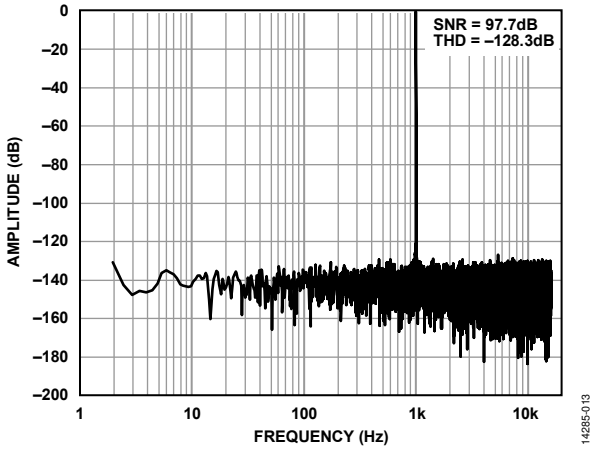

Figure 13. FFT, Focus Mode, Wideband Filter, –0.5 dBFS

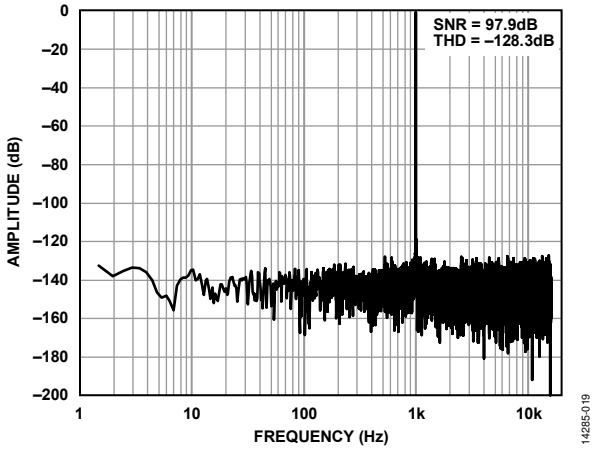

Figure 16. FFT, Focus Mode, Sinc5 Filter, –0.5 dBFS

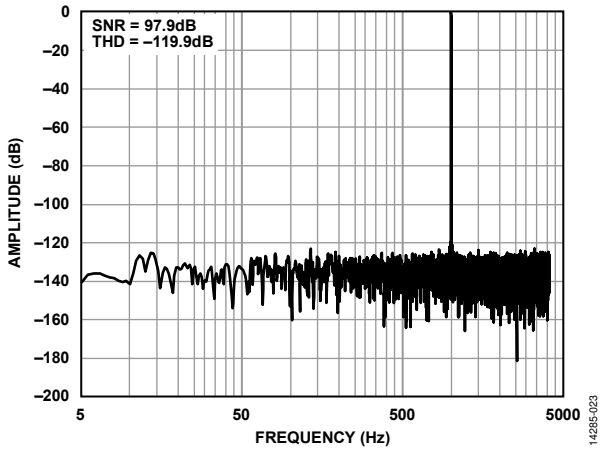

Figure 17. FFT One-Shot Mode, Sinc5 Filter, Median Mode, Decimation = ×64, −0.5 dBFS, $\overline{SYNC\_IN}$ Frequency = MCLK/4000

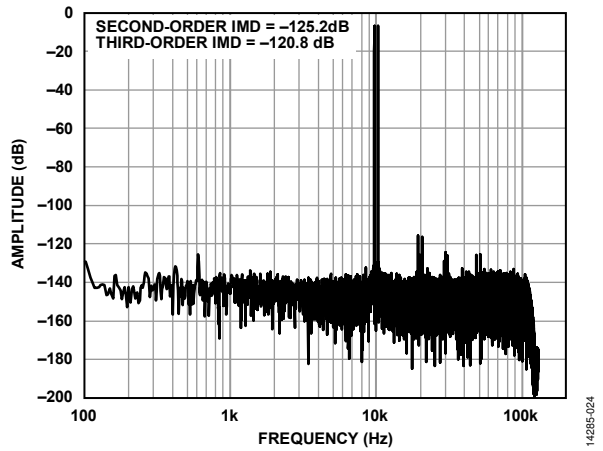

Figure 18. IMD with Input Signals at 9.7 kHz and 10.3 kHz

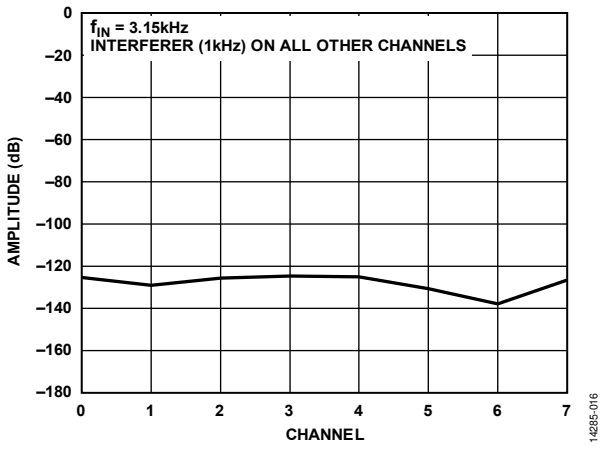

Figure 19. Crosstalk

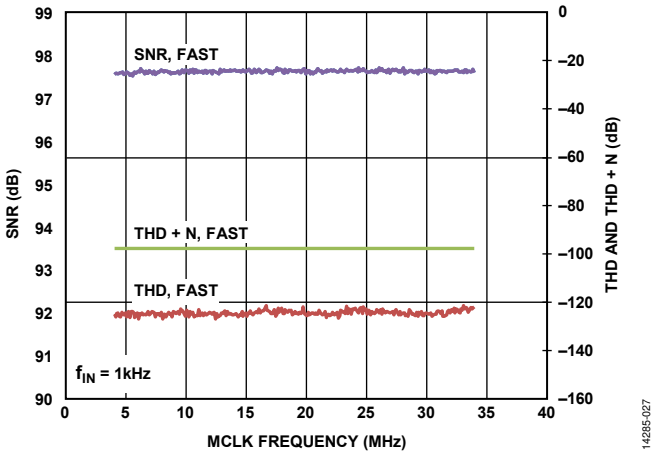

Figure 20. SNR, THD, THD + N vs. MCLK Frequency

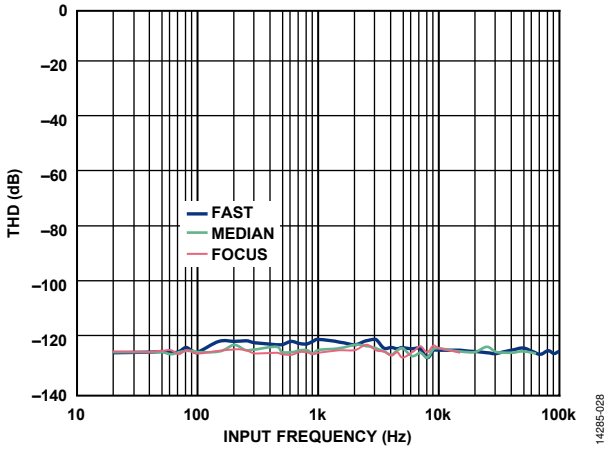

Figure 21. THD vs. Input Frequency, Three Power Modes, Wideband Filter

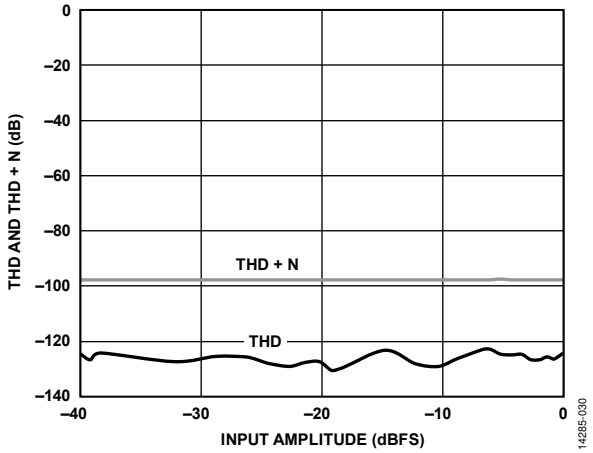

Figure 22. THD and THD + N vs. Input Amplitude, Wideband Filter, Fast Mode

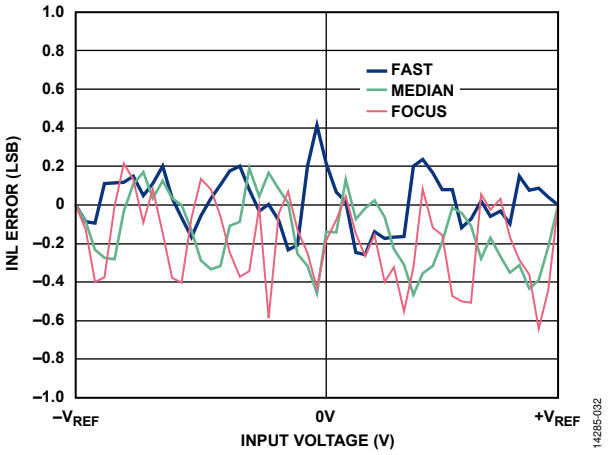

Figure 23. INL Error vs. Input Voltage

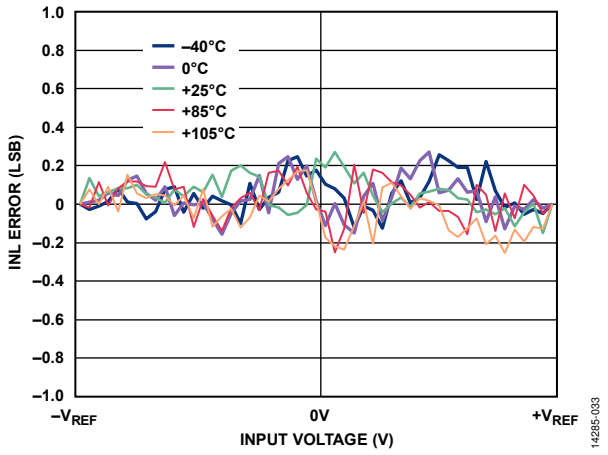

Figure 24. INL Error vs. Input Voltage for Various Temperatures, Fast Mode

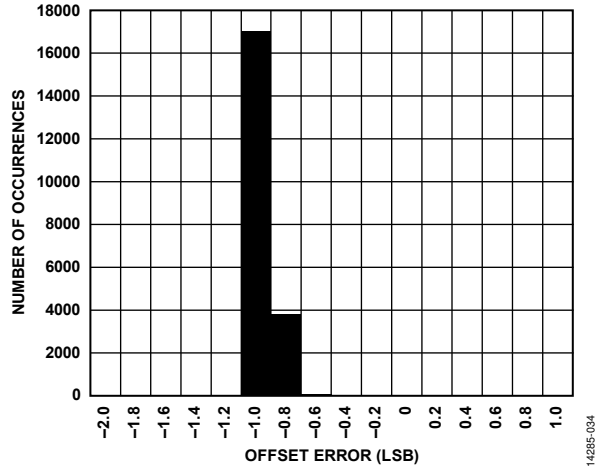

Figure 25. Offset Error Distribution (Approximately 2500 Devices Sampled)

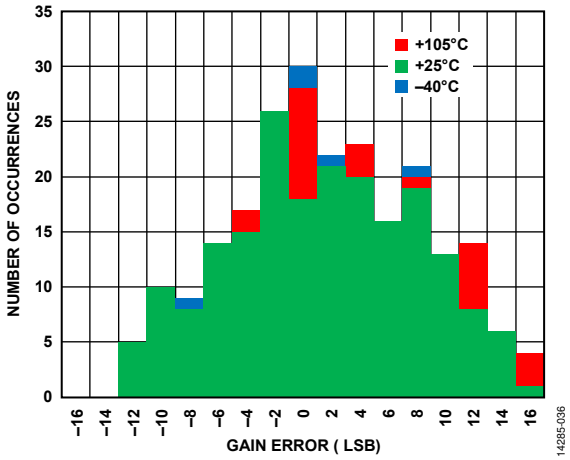

Figure 26. Gain Error Distribution (100 Devices Sampled)

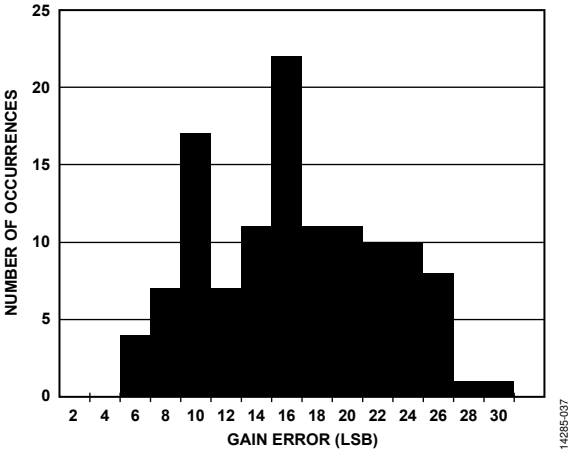

Figure 27. Channel to Channel Gain Error Matching (100 Devices Sampled)

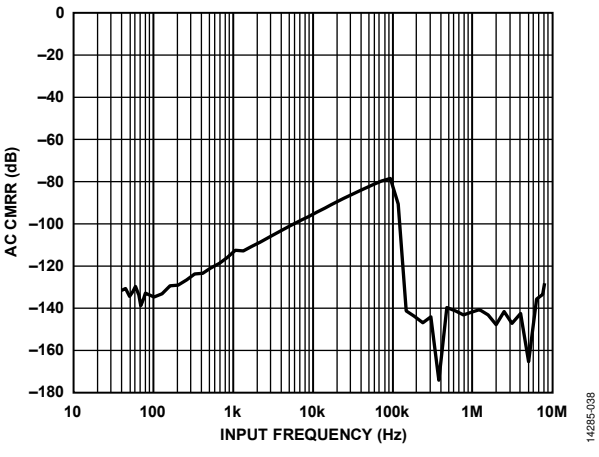

Figure 28. AC CMRR vs. Input Frequency

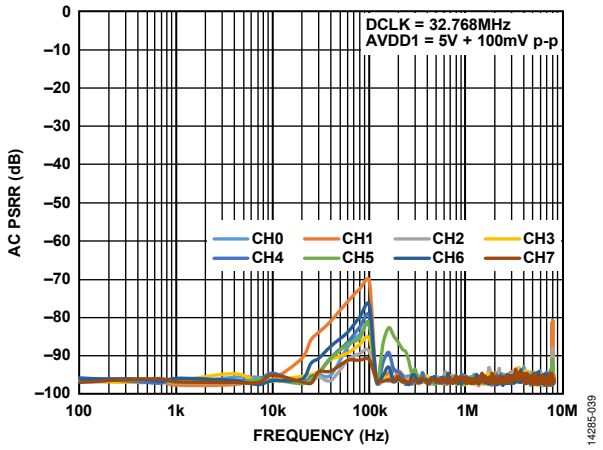

Figure 29. AC PSRR vs. Frequency, AVDD1

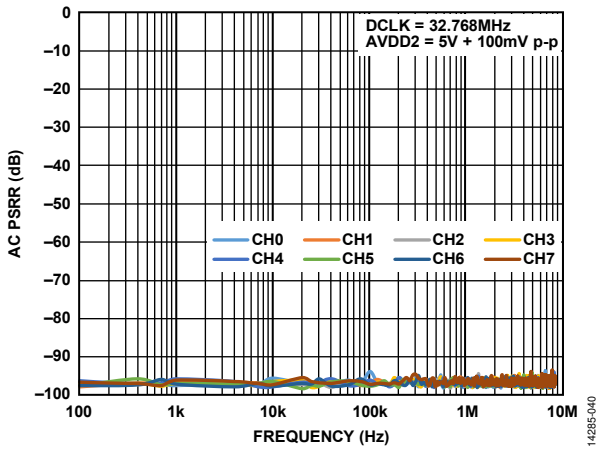

Figure 30. AC PSRR vs. Frequency, AVDD2

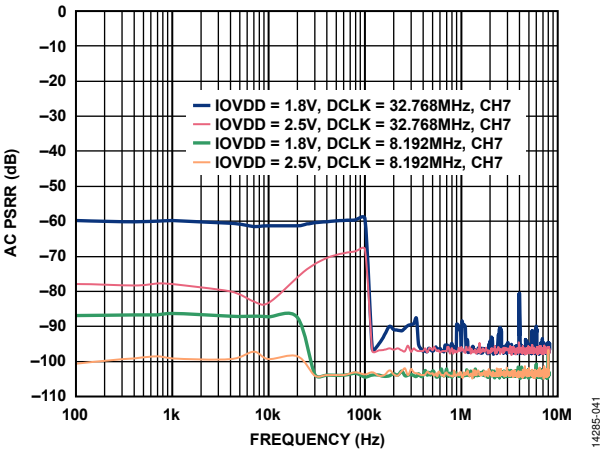

Figure 31. AC PSRR vs. Frequency, IOVDD

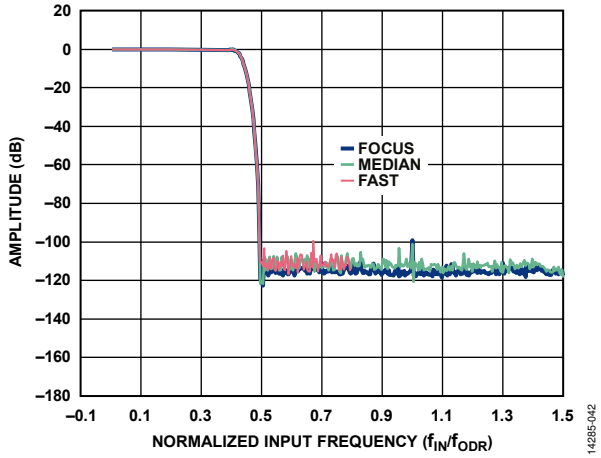

Figure 32. Wideband Filter Profile, Amplitude vs. f_{IN}/f_{ODR}

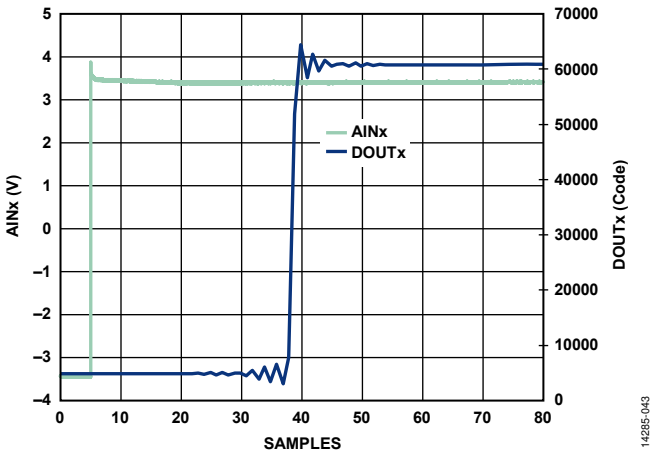

Figure 33. Step Response, Wideband Filter

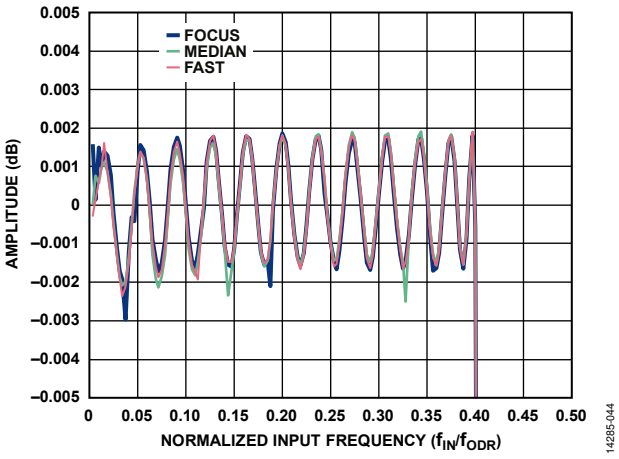

Figure 34. Wideband Filter Ripple

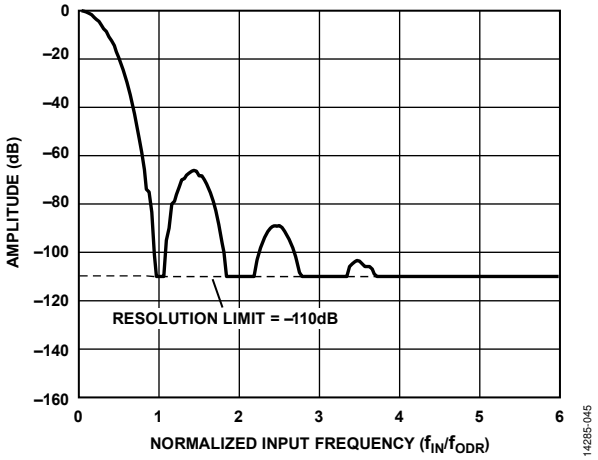

Figure 35. Sinc5 Filter Profile, Amplitude vs. f_{IN}/f_{ODR}

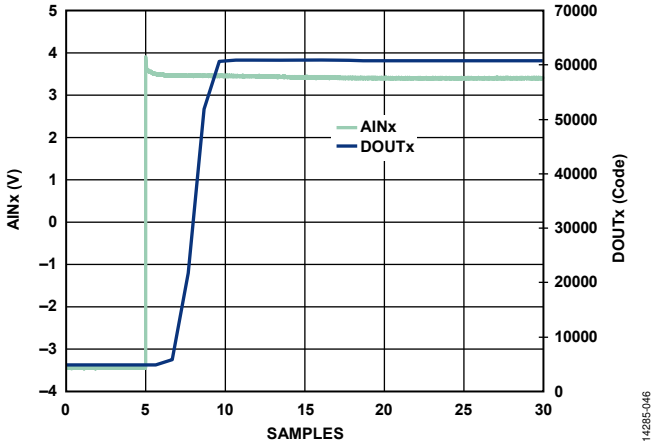

Figure 36. Step Response, Sinc5 Filter

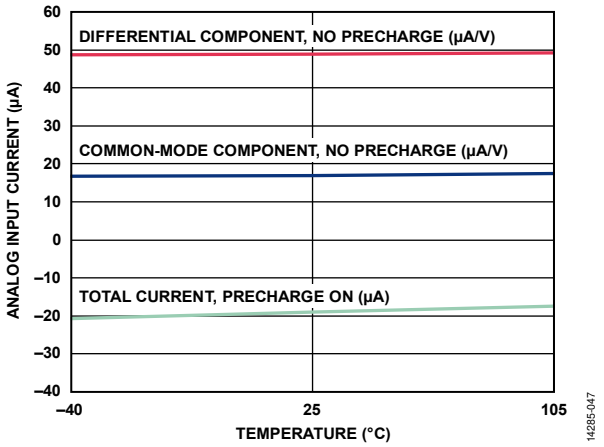

Figure 37. Analog Input Current vs. Temperature, Analog Input Precharge Buffers On/Off

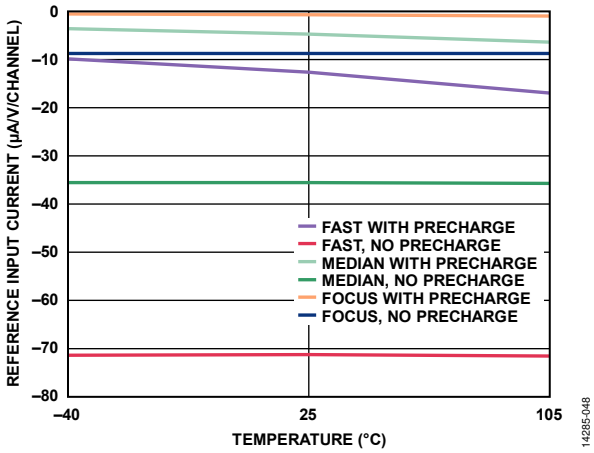

Figure 38. Reference Input Current vs. Temperature, Reference Precharge Buffers On/Off

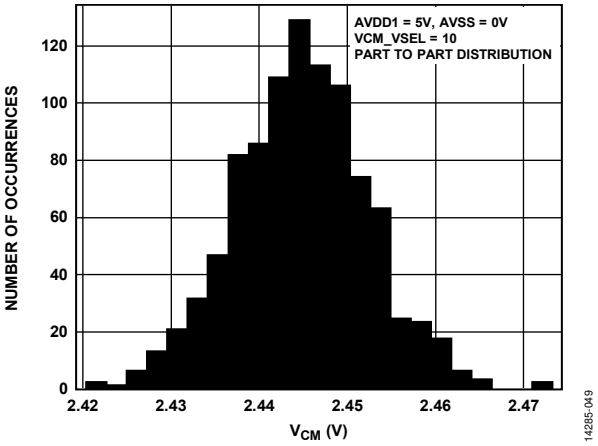

Figure 39. VCM Output Voltage Distribution

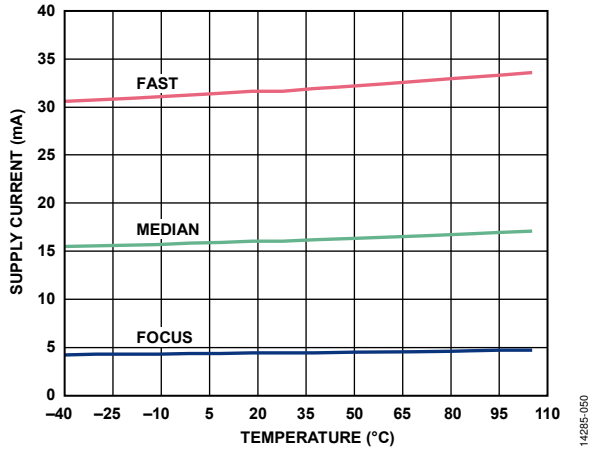

Figure 40. Supply Current vs. Temperature, AVDD1

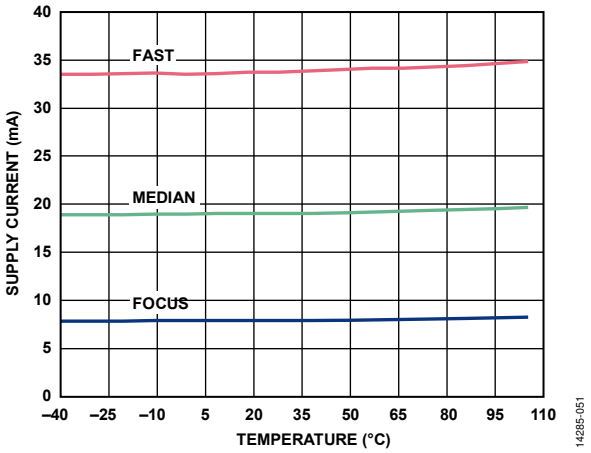

Figure 41. Supply Current vs. Temperature, AVDD2

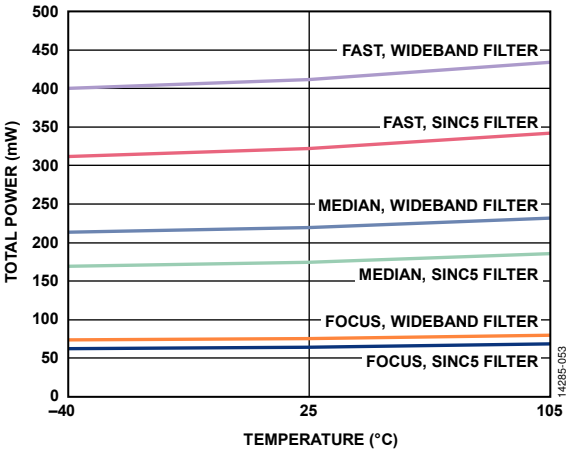

Figure 43. Total Power vs. Temperature

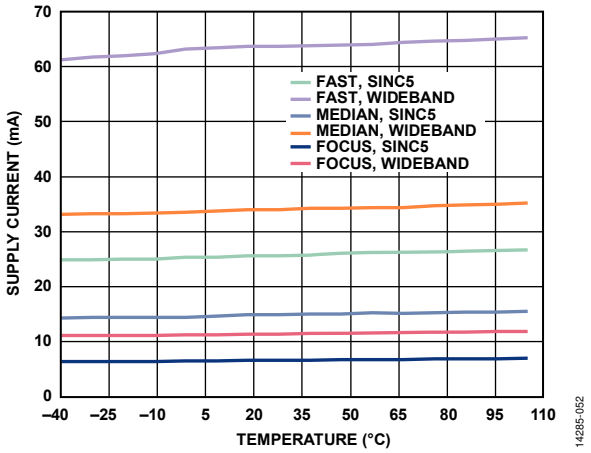

Figure 42. Supply Current vs. Temperature, IOVDD