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# 8-/4-Channel, 24-Bit, Simultaneous Sampling ADCs with Power Scaling, 110.8 kHz BW

Data Sheet

# AD7768/AD7768-4

## FEATURES

- Precision ac and dc performance
- 8-/4-channel simultaneous sampling
  - 256 kSPS maximum ADC output data rate per channel
  - 108 dB dynamic range
  - 110.8 kHz maximum input bandwidth (−3 dB bandwidth)
  - −120 dB total harmonic distortion (THD) typical
  - ±2 ppm of full-scale range (FSR) integral nonlinearity (INL), ±50 µV offset error, ±30 ppm gain error
- Optimized power dissipation vs. noise vs. input bandwidth
  - Selectable power, speed, and input bandwidth (BW) modes
    - Fast: highest speed; 110.8 kHz BW, 51.5 mW per channel
    - Median: half speed, 55.4 kHz BW, 27.5 mW per channel
    - Eco: lowest power, 13.8 kHz BW, 9.375 mW per channel
  - Input BW range: dc to 110.8 kHz
  - Programmable input bandwidth/sampling rates
- Cyclic redundancy check (CRC) error checking on data interface
- Daisy-chaining
- Linear phase digital filter
  - Low latency sinc5 filter
  - Wideband brick wall filter: ±0.005 dB pass-band ripple from dc to 102.4 kHz
- Analog input precharge buffers
- Power supply
  - AVDD1 = 5.0 V, AVDD2 = 2.25 V to 5.0 V
  - IOVDD = 2.5 V to 3.3 V or IOVDD = 1.8 V
- 64-lead LQFP package, no exposed pad
- Temperature range: −40°C to +105°C

## APPLICATIONS

- Data acquisition systems: USB/PXI/Ethernet
- Instrumentation and industrial control loops
- Audio test and measurement
- Vibration and asset condition monitoring
- 3-phase power quality analysis
- Sonar
- High precision medical electroencephalogram (EEG)/electromyography (EMG)/electrocardiogram (ECG)

## FUNCTIONAL BLOCK DIAGRAM

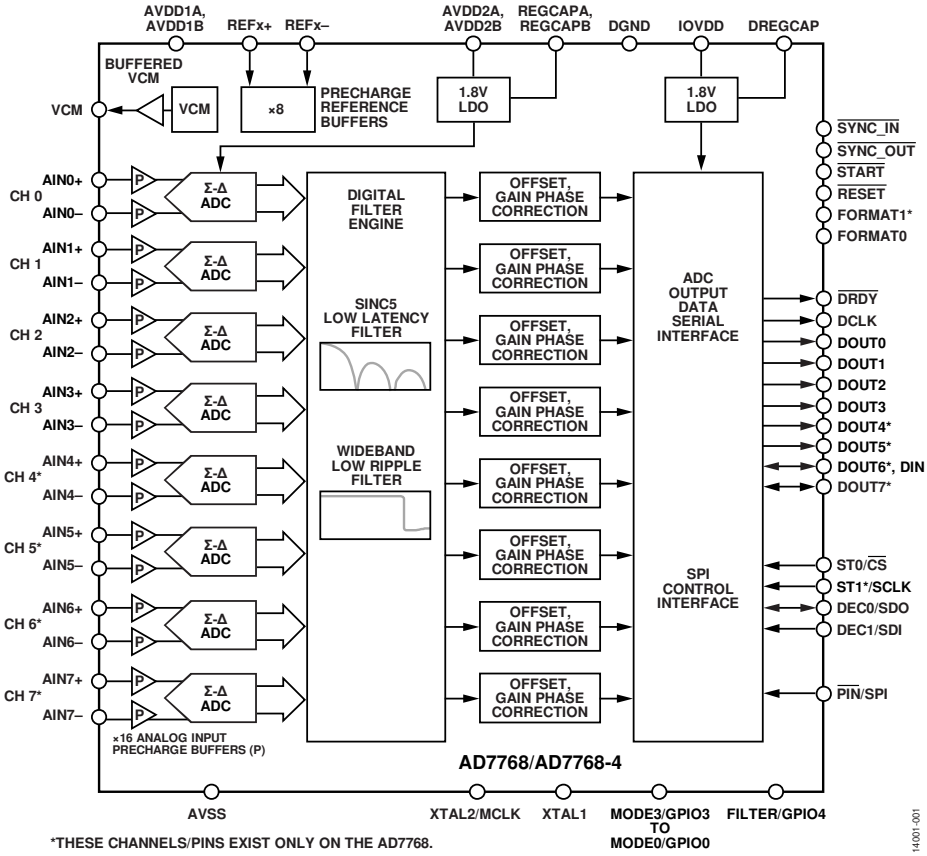


*Figure 1.*


**Rev. A** Document Feedback





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**1/16—Revision 0: Initial Version**

# GENERAL DESCRIPTION

The AD7768/AD7768-4 are 8-channel and 4-channel, simultaneous sampling sigma-delta (Σ-Δ) analog-to-digital converters (ADCs), respectively, with a Σ-Δ modulator and digital filter per channel, enabling synchronized sampling of ac and dc signals.

The AD7768/AD7768-4 achieve 108 dB dynamic range at a maximum input bandwidth of 110.8 kHz, combined with typical performance of ±2 ppm INL, ±50 µV offset error, and ±30 ppm gain error.

The AD7768/AD7768-4 user can trade off input bandwidth, output data rate, and power dissipation, and select one of three power modes to optimize for noise targets and power consumption. The flexibility of the AD7768/AD7768-4 allows them to become reusable platforms for low power dc and high performance ac measurement modules.

The AD7768/AD7768-4 have three modes: fast mode (256 kSPS maximum, 110.8 kHz input bandwidth, 51.5 mW per channel), median mode (128 kSPS maximum, 55.4 kHz input bandwidth, 27.5 mW per channel) and eco mode (32 kSPS maximum, 13.8 kHz input bandwidth, 9.375 mW per channel).

The AD7768/AD7768-4 offer extensive digital filtering capabilities, such as a wideband, low ±0.005 dB pass-band ripple, antialiasing low-pass filter with sharp roll-off, and 105 dB stop band attenuation at the Nyquist frequency.

Frequency domain measurements can use the wideband linear phase filter. This filter has a flat pass band (±0.005 dB ripple) from dc to 102.4 kHz at 256 kSPS, from dc to 51.2 kHz at 128 kSPS, or from dc to 12.8 kHz at 32 kSPS.

The AD7768/AD7768-4 also offer sinc response via a sinc5 filter, a low latency path for low bandwidth, and low noise measurements. The wideband and sinc5 filters can be selected and run on a per channel basis.

Within these filter options, the user can improve the dynamic range by selecting from decimation rates of ×32, ×64, ×128, ×256, ×512, and ×1024. The ability to vary the decimation filtering optimizes noise performance to the required input bandwidth.

Embedded analog functionality on each ADC channel makes design easier, such as a precharge buffer on each analog input that reduces analog input current and a reference precharge buffer per channel reduces input current and glitches on the reference input terminals.

The device operates with a 5 V AVDD1A and AVDD1B supply, a 2.25 V to 5.0 V AVDD2A and AVDD2B supply, and a 2.5 V to 3.3 V or 1.8 V IOVDD supply (see the 1.8 V IOVDD Operation section for specific requirements for operating at 1.8 V IOVDD).

The device requires an external reference; the absolute input reference voltage range is 1 V to AVDD1 − AVSS.

For the purposes of clarity within this document, the AVDD1A and AVDD1B supplies are referred to as AVDD1 and the AVDD2A and AVDD2B supplies are referred to as AVDD2. For the negative supplies, AVSS refers to the AVSS1A, AVSS1B, AVSS2A, AVSS2B, and AVSS pins.

The specified operating temperature range is −40°C to +105°C. The device is housed in a 10 mm × 10 mm 64-lead LQFP package with a 12 mm × 12 mm printed circuit board (PCB) footprint.

Throughout this data sheet, multifunction pins, such as XTAL2/MCLK, are referred to either by the entire pin name or by a single function of the pin, for example MCLK, when only that function is relevant.

# SPECIFICATIONS

AVDD1A = AVDD1B = 4.5 V to 5.5 V, AVDD2A = AVDD2B = 2.0 V to 5.5 V, IOVDD = 2.25 V to 3.6 V, AVSS = DGND = 0 V, REFx+ = 4.096 V and REFx− = 0 V, MCLK = 32.768 MHz, analog input precharge buffers on, reference precharge buffers off, wideband filter, $f_{CHOP}$ = $f_{MOD}/32$, $T_A$ = −40°C to +105°C, unless otherwise noted. See Table 2 for specifications at 1.8 V IOVDD.

**Table 1.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ADC SPEED AND PERFORMANCE | | | | | |
| Output Data Rate (ODR), per Channel[1] | Fast | 8 | | 256 | kSPS |
| | Median | 4 | | 128 | kSPS |
| | Eco | 1 | | 32 | kSPS |
| −3 dB Bandwidth | Fast, wideband filter | | | 110.8 | kHz |
| | Median, wideband filter | | | 55.4 | kHz |
| | Eco, wideband filter | | | 13.8 | kHz |
| Data Output Coding | | | Twos complement, MSB first | | |
| No Missing Codes[2] | | 24 | | | Bits |
| DYNAMIC PERFORMANCE | For 1.8 V operation, see Table 2; for dynamic range and SNR across all decimation rates, see Table 12 and Table 13 | | | | |
| Fast | Decimation by 32, 256 kSPS ODR | | | | |
| Dynamic Range | Shorted input, wideband filter | 106.2 | 108 | | dB |
| Signal-to-Noise Ratio (SNR) | 1 kHz, −0.5 dBFS, sine wave input | | | | |
| | Sinc5 filter | 109 | 111 | | dB |
| | Wideband filter | 106 | 107.8 | | dB |
| Signal-to-Noise-and-Distortion Ratio (SINAD) | 1 kHz, −0.5 dBFS, sine wave input | 104.7 | 107.5 | | dB |
| Total Harmonic Distortion (THD) | 1 kHz, −0.5 dBFS, sine wave input | | −120 | −107 | dB |
| Spurious-Free Dynamic Range (SFDR) | | | 128 | | dBc |
| Median | Decimation by 32, 128 kHz ODR | | | | |
| Dynamic Range | Shorted input, wideband filter | 106.2 | 108 | | dB |
| SNR | Sinc5 filter, 1 kHz, −0.5 dBFS, sine wave input | 109 | 111 | | dB |
| | Wideband filter, 1 kHz, −0.5 dBFS, sine wave input | 106 | 107.8 | | dB |
| SINAD | 1 kHz, −0.5 dBFS, sine wave input | 105.8 | 107.5 | | dB |
| THD | 1 kHz, −0.5 dBFS, sine wave input | | −120 | −113 | dB |
| SFDR | | | 128 | | dBc |
| Eco | Decimation by 32, 32 kHz ODR | | | | |
| Dynamic Range | Shorted input, wideband filter | 106.2 | 108 | | dB |
| SNR | Sinc5 filter, 1 kHz, −0.5 dBFS, sine wave input | 109 | 111 | | dB |
| | Wideband filter, 1 kHz, −0.5 dBFS, sine wave input | 106 | 107.8 | | dB |
| SINAD | 1 kHz, −0.5 dBFS, sine wave input | 105.8 | 107.5 | | dB |
| THD | 1 kHz, −0.5 dBFS, sine wave input | | −120 | −113 | dB |
| SFDR | | | 128 | | dBc |
| INTERMODULATON DISTORTION (IMD)[3] | fa = 9.7 kHz, fb = 10.3 kHz | | | | |
| | Second order | | −125 | | dB |
| | Third order | | −125 | | dB |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ACCURACY | See Table 2 for 1.8 V operation | | | | |
| INL | Endpoint method | | ±2 | ±7 | ppm of FSR |
| Offset Error[4] | DCLK frequency ≤ 24 MHz | | ±50 | ±115 | µV |
| | 24 MHz to 32.768 MHz DCLK frequency[2] | | ±75 | ±150 | µV |
| Offset Error Drift | DCLK frequency ≤ 24 MHz | | ±250 | | nV/°C |
| | 24 MHz to 32.768 MHz DCLK frequency | | ±750 | | nV/°C |
| Gain Error[4] | $T_A$ = 25°C | | ±30 | ±70 | ppm of FSR |
| Gain Drift vs. Temperature[2] | | | ±0.5 | ±1 | ppm/°C |
| VCM PIN | | | | | |
| Output | With respect to AVSS | | (AVDD1 − AVSS)/2 | | V |
| Load Regulation ($\Delta V_{OUT}/\Delta I_L$) | | | 400 | | µV/mA |
| Voltage Regulation | Applies to the following VCM output options only: $V_{CM} = \Delta V_{OUT}/\Delta(AVDD1 - AVSS)/2$; $V_{CM}$ = 1.65 V; and $V_{CM}$ = 2.5 V | | 5 | | µV/V |
| Short-Circuit Current | | | 30 | | mA |
| ANALOG INPUTS | See the Analog Inputs section | | | | |
| Differential Input Voltage Range | $V_{REF}$ = (REFx+) − (REFx−) | $-V_{REF}$ | | $+V_{REF}$ | V |
| Input Common-Mode Range[2] | | AVSS | | AVDD1 | V |
| Absolute Analog Input Voltage Limits[2] | | AVSS | | AVDD1 | V |
| Analog Input Current | Fast mode | | | | |
| Unbuffered | Differential component | | ±48 | | µA/V |
| | Common-mode component | | ±17 | | µA/V |
| Precharge Buffer On[5] | | | −20 | | µA |
| Input Current Drift | Fast mode; see Figure 62 | | | | |
| Unbuffered | | | ±5 | | nA/V/°C |
| Precharge Buffer On | | | ±31 | | nA/°C |
| EXTERNAL REFERENCE | | | | | |
| Reference Voltage | $V_{REF}$ = (REFx+) − (REFx−) | 1 | | AVDD1 − AVSS | V |
| Absolute Reference Voltage Limits[2] | Reference precharge buffers off | AVSS − 0.05 | | AVDD1 + 0.05 | V |
| | Reference precharge buffer on | AVSS | | AVDD1 | V |
| Average Reference Current | Fast mode; see Figure 63 | | | | |
| | Reference precharge buffers off | | ±72 | | µA/V/channel |
| | Reference precharge buffers on | | ±16 | | µA/V/channel |
| Average Reference Current Drift | Fast mode; see Figure 63 | | | | |
| | Reference precharge buffers off | | ±1.7 | | nA/V/°C |
| | Reference precharge buffers on | | ±49 | | nA/V/°C |
| Common-Mode Rejection | | | 95 | | dB |
| DIGITAL FILTER RESPONSE | | | | | |
| Low Ripple Wideband Filter | FILTER = 0 | | | | |
| Decimation Rate | Up to six selectable decimation rates; see the Decimation Rate Control section | 32 | | 1024 | |
| Group Delay | Latency | | 34/ODR | | sec |
| Settling Time | Complete settling, see Table 35 | | 68/ODR | | sec |
| Pass-Band Ripple[2] | From dc to 102.4 kHz at 256 kSPS | | | ±0.005 | dB |
| Pass Band | ±0.005 dB bandwidth | | 0.4 × ODR | | Hz |
| | −0.1 dB bandwidth | | 0.409 × ODR | | Hz |
| | −3 dB bandwidth | | 0.433 × ODR | | Hz |
| Stop Band Frequency | Attenuation > 105 dB | | 0.499 × ODR | | Hz |
| Stop Band Attenuation | See the Wideband Low Ripple Filter section | | 105 | | dB |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Sinc5 Filter | FILTER = 1 | | | | |
| Decimation Rate | Up to six selectable decimation rates; see the Decimation Rate Control section | 32 | | 1024 | |
| Group Delay | Latency | | 3/ODR | | sec |
| Settling Time | Complete settling, see Table 36 | | 7/ODR | | sec |
| Pass Band | −3 dB bandwidth | | 0.204 × ODR | | Hz |
| REJECTION | | | | | |
| AC Power Supply Rejection Ratio (PSRR) | $V_{IN}$ = 0.1 V, AVDD1 = 5 V, AVDD2 = 5 V, IOVDD = 2.5 V | | | | |
| AVDD1 | | | 90 | | dB |
| AVDD2 | | | 100 | | dB |
| IOVDD | | | 75 | | dB |
| DC PSRR | $V_{IN}$ = 1 V | | | | |
| AVDD1 | | | 100 | | dB |
| AVDD2 | | | 118 | | dB |
| IOVDD | | | 90 | | dB |
| Analog Input Common-Mode Rejection Ratio (CMRR) | | | | | |
| DC | $V_{IN}$ = 0.1 V | 95 | | | dB |
| AC | Up to 10 kHz | | 95 | | dB |
| Crosstalk | −0.5 dBFS input on adjacent channels | | −120 | | dB |
| CLOCK | | | | | |
| Crystal Frequency | | 8 | 32.768 | 34 | MHz |
| External Clock (MCLK) | See the Timing Specifications section | | 32.768 | | MHz |
| Duty Cycle | For data sheet performance | | 50:50 | | % |
| MCLK Pulse Width[2] | Functionality | | | | |
| Logic Low | | 12.2 | | | ns |
| Logic High | | 12.2 | | | ns |
| CMOS Clock Input Voltage | See the logic inputs parameter | | | | |
| High, $V_{INH}$ | | | | | |
| Low, $V_{INL}$ | | | | | |
| LVDS Clock[2] | $R_L$ = 100 Ω | | | | |
| Differential Input Voltage | | 100 | | 650 | mV |
| Common-Mode Input Voltage | | 800 | | 1575 | mV |
| Absolute Input Voltage | | | | 1.88 | V |
| ADC RESET[2] | | | | | |
| ADC Start-Up Time After Reset[6] | Time to first $\overline{DRDY}$, fast mode, decimation by 32 | | 1.58 | 1.66 | ms |
| Minimum $\overline{RESET}$ Low Pulse Width | $t_{MCLK}$ = 1/MCLK | 2 × $t_{MCLK}$ | | | |
| LOGIC INPUTS | See Table 2 for 1.8 V operation | | | | |
| Input Voltage[2] | | | | | |
| High, $V_{INH}$ | | 0.65 × IOVDD | | | V |
| Low, $V_{INL}$ | | | | 0.7 | V |
| Hysteresis[2] | | 0.04 | | 0.09 | V |
| Leakage Current | | −10 | +0.03 | +10 | µA |
| | $\overline{RESET}$ pin[7] | −10 | | +10 | µA |
| LOGIC OUTPUTS | See Table 2 for 1.8 V operation | | | | |
| Output Voltage[2] | | | | | |
| High, $V_{OH}$ | $I_{SOURCE}$ = 200 µA | 0.8 × IOVDD | | | V |
| Low, $V_{OL}$ | $I_{SINK}$ = 400 µA | | | 0.4 | V |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Leakage Current | Floating state | −10 | | +10 | µA |
| Output Capacitance | Floating state | | 10 | | pF |
| SYSTEM CALIBRATION[2] | | | | | |
| Full-Scale Calibration Limit | | | | $1.05 \times V_{REF}$ | V |
| Zero-Scale Calibration Limit | | $-1.05 \times V_{REF}$ | | | V |
| Input Span | | $0.4 \times V_{REF}$ | | $2.1 \times V_{REF}$ | V |
| POWER REQUIREMENTS | | | | | |
| Power Supply Voltage | | | | | |
| AVDD1 – AVSS | | 4.5 | 5.0 | 5.5 | V |
| AVDD2 – AVSS | | 2.0 | 2.25 to 5.0 | 5.5 | V |
| AVSS – DGND | | −2.75 | | 0 | V |
| IOVDD – DGND | See Table 2 for 1.8 V operation | 2.25 | 2.5 to 3.3 | 3.6 | V |
| POWER SUPPLY CURRENTS | Maximum output data rate, CMOS MCLK, eight DOUTx signals, all supplies at maximum voltages, all channels in Channel Mode A except where otherwise specified | | | | |
| AD7768 | Eight channels active | | | | |
| Fast Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 36/57.5 | 40/64 | mA |
| AVDD2 Current | | | 37.5 | 40 | mA |
| IOVDD Current | Wideband filter | | 63 | 67 | mA |
| | Sinc5 filter | | 27 | 29 | mA |
| Median Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 18.5/29 | 20.5/32.5 | mA |
| AVDD2 Current | | | 21.3 | 23 | mA |
| IOVDD Current | Wideband filter | | 34 | 37 | mA |
| | Sinc5 filter | | 16 | 18 | mA |
| Eco Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 5.1/8 | 5.8/9 | mA |
| AVDD2 Current | | | 9.3 | 10.1 | mA |
| IOVDD Current | Wideband filter | | 12.5 | 13.7 | mA |
| | Sinc5 filter | | 8 | 9 | mA |
| AD7768-4 | Four Channels Active | | | | |
| Fast Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 18.2/28.8 | 20.3/32.5 | mA |
| AVDD2 Current | | | 18.8 | 20.3 | mA |
| IOVDD Current | Wideband filter[2] | | 43.5 | 46.8 | mA |
| | Wideband filter, SPI mode only; Channel Mode A set to sinc5 filter[8] | | 37 | 40 | mA |
| | Sinc5 filter[2] | | 17 | 18.6 | mA |
| Median Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 9.3/14.7 | 10.5/16.6 | mA |
| AVDD2 Current | | | 10.7 | 11.7 | mA |
| IOVDD Current | Wideband filter[2] | | 24.4 | 26.4 | mA |
| | Wideband filter, SPI mode only; Channel Mode A set to sinc5 filter[8] | | 21 | 23 | mA |
| | Sinc5 filter[2] | | 11 | 12.3 | mA |
| Eco Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 2.7/4.1 | 3.1/4.7 | mA |
| AVDD2 Current | | | 4.7 | 5.3 | mA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| IOVDD Current | Wideband filter[2] | | 10 | 11.1 | mA |
| | Wideband filter, SPI mode only; Channel Mode A set to sinc5 filter[8] | | 9 | 10 | mA |
| | Sinc5 filter[2] | | 6.5 | 7.6 | mA |
| AD7768 and AD7768-4—Two Channels Active[2] | Serial peripheral interface (SPI) control mode only; see the Channel Standby section for details on disabling channels | | | | |
| Fast Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 9.3/14.7 | 10.5/16.6 | mA |
| AVDD2 Current | | | 9.5 | 10.5 | mA |
| IOVDD Current | Wideband filter | | 33.7 | 36.3 | mA |
| | Wideband filter; disabled channels in Channel Mode A, and set to sinc5 filter mode[8] | | 23.4 | 25.5 | mA |
| | Sinc5 filter | | 11.9 | 13.3 | mA |
| Median Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 4.8/7.5 | 5.5/8.6 | mA |
| AVDD2 Current | | | 5.5 | 6.2 | mA |
| IOVDD Current | Wideband filter | | 19.4 | 21.1 | mA |
| | Wideband filter; disabled channels in Channel Mode A, and set to sinc5 filter mode[8] | | 14.1 | 15.5 | mA |
| | Sinc5 filter | | 8.5 | 9.6 | mA |
| Eco Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 1.52/2.2 | 1.77/2.6 | mA |
| AVDD2 Current | | | 2.4 | 3 | mA |
| IOVDD Current | Wideband filter | | 8.6 | 9.7 | mA |
| | Wideband filter; disabled channels in Channel Mode A, and set to sinc5 filter mode[8] | | 7.2 | 8 | mA |
| | Sinc5 filter | | 5.8 | 6.7 | mA |
| Standby Mode | All channels disabled (sinc5 filter enabled) | | 6.5 | 8 | mA |
| Sleep Mode[2] | Full power-down (SPI control mode only) | | 0.73 | 1.2 | mA |
| Crystal Excitation Current | Extra current in IOVDD when using an external crystal compared to using the CMOS MCLK | | 540 | | µA |
| POWER DISSIPATION | External CMOS MCLK, all channels active, MCLK = 32.768 MHz, all channels in Channel Mode A except where otherwise specified | | | | |
| Full Operating Mode | Analog precharge buffers on | | | | |
| AD7768 | | | | | |
| Wideband Filter | | | | | |
| Fast | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, reference precharge buffers off[2] | | 412 | 446 | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, reference precharge buffers on[2] | | 600 | 645 | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, reference precharge buffers off | | 631 | 681 | mW |
| Median | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, reference precharge buffers off[2] | | 220 | 240 | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, reference precharge buffers on[2] | | 320 | 345 | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, reference precharge buffers off | | 341 | 372 | mW |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Eco | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, reference precharge buffers off[2] | | 75 | 85 | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, reference precharge buffers on[2] | | 107 | 118 | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, reference precharge buffers off | | 124 | 137 | mW |
| Sinc5 Filter | | | | | |
| Fast | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, reference precharge buffers off[2] | | 325 | 355 | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, reference precharge buffers on[2] | | 475 | 525 | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, reference precharge buffers off | | 501 | 545 | mW |
| Median | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, reference precharge buffers off[2] | | 175 | 195 | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, reference precharge buffers on[2] | | 260 | 285 | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, reference precharge buffers off | | 277 | 304 | mW |
| Eco | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, reference precharge buffers off[2] | | 65 | 72 | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, reference precharge buffers on[2] | | 95 | 105 | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, reference precharge buffers off | | 108 | 120 | mW |
| AD7768-4 | | | | | |
| Wideband Filter | | | | | |
| Fast | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, reference precharge buffers off | | 235 | | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, reference precharge buffers on | | 336 | | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, reference precharge buffers off[2] | | 360 | 392 | mW |
| | SPI mode only; AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, reference precharge buffers off, Channel Mode A set to sinc5 filter[8] | | 337 | 368 | mW |
| Median | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, reference precharge buffers off | | 127 | | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, reference precharge buffers on | | 181 | | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, reference precharge buffers off[2] | | 198 | 218 | mW |
| | SPI mode only; AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, reference precharge buffers off, Channel Mode A set to sinc5 filter[8] | | 186 | 205 | mW |
| Eco | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, reference precharge buffers off | | 49 | | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, reference precharge buffers on | | 66 | | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, reference precharge buffers off[2] | | 77 | 87 | mW |
| | SPI mode only; AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, reference precharge buffers off, Channel Mode A set to sinc5 filter[8] | | 73 | 83 | mW |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Sinc5 Filter | | | | | |
| Fast | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, reference precharge buffers off | | 168 | | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, reference precharge buffers on | | 248 | | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, reference precharge buffers off | | 265 | 291 | mW |
| Median | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, reference precharge buffers off | | 94 | | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, reference precharge buffers on | | 137 | | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, reference precharge buffers off | | 150 | 167 | mW |
| Eco | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, reference precharge buffers off | | 40 | | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, reference precharge buffers on | | 55 | | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, reference precharge buffers off | | 64 | 74 | mW |
| Standby Mode | All channels disabled (sinc5 filter enabled), AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V[2] | | | 18 | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V[2] | | | 26 | mW |
| | AVDD1 = AVDD2 = 5.5 V, IOVDD = 3.6 V | | | 29 | mW |
| Sleep Mode[2] | Full power-down (SPI control mode), AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V | | 1.8 | 4 | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V | | 2.5 | 5 | mW |
| | AVDD1 = AVDD2 = 5.5 V, IOVDD = 3.6 V | | 2.7 | 6.5 | mW |

[1] The output data rate ranges refer to the programmable decimation rates available on the AD7768/AD7668-4 for a fixed MCLK rate of 32.768 MHz. Varying MCLK rates allow users a wider variation of ODR.
[2] These specifications are not production tested but are supported by characterization data at initial product release.
[3] See the Terminology section for more information about the fa and fb input frequencies.
[4] Following a system zero-scale calibration, the offset error is in the order of the noise for the programmed output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed output data rate.
[5] −25 µA is measured when the analog input is close to either the AVDD1 or AVSS rail. The input current reduces as the common-mode voltage approaches (AVDD1 − AVSS)/2. The analog input current scales with the MCLK frequency and device power mode. See Figure 85 and Figure 86 for more details on how the analog input current scales with input voltage.
[6] For lower MCLK rates or higher decimation rates, use Table 35 and Table 36 to calculate any additional delay before the first $\overline{\text{DRDY}}$ pulse.
[7] The $\overline{\text{RESET}}$ pin has an internal pull-up device to IOVDD.
[8] Configuring Channel Mode A to the sinc5 filter and/or assigning disabled channels to Channel Mode A allows a lower power consumption to be achieved. To do this, the user must be operating in SPI control mode because it requires assigning channels to different channel modes (only possible in SPI control mode). If using pin control mode, all channels, whether active or in standby, are assigned to the same channel group and use the same filter type. This means that, in pin control mode, a higher current consumption is seen from disabled channels than can be achieved in SPI mode. See the Channel Modes section for more details.

## 1.8 V IOVDD SPECIFICATIONS

AVDD1A = AVDD1B = 4.5 V to 5.5 V, AVDD2A = AVDD2B = 2.0 V to 5.5 V, IOVDD = 1.72 V to 1.88 V, AVSS = DGND = 0 V, REFx+ = 4.096 V and REFx− = 0 V, MCLK = 32.76 8 MHz, analog precharge buffers on, reference precharge buffers off, wideband filter, $f_{CHOP}$ = $f_{MOD}/32$, $T_A$ = −40°C to +105°C, unless otherwise noted.

**Table 2.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | For dynamic range and SNR across all decimation rates, see Table 12 and Table 13 | | | | |
| Fast | Decimation by 32, 256 kSPS ODR | | | | |
| Dynamic Range | Shorted input, wideband filter | 106.2 | 108 | | dB |
| SNR | Sinc5 filter, 1 kHz, −0.5 dBFS, sine wave input | 109 | 111 | | dB |
| | Wideband filter, 1 kHz, −0.5 dBFS, sine wave input | 106 | 107.8 | | dB |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SINAD[1] | 1 kHz, −0.5 dBFS, sine wave input | 103.8 | 107.5 | | dB |
| THD | 1 kHz, −0.5 dBFS, sine wave input | | −120 | −107 | dB |
| SFDR | | | 128 | | dBc |
| Median | Decimation by 32, 128 kHz ODR | | | | |
| Dynamic Range | Shorted input, wideband filter | 106.2 | 108 | | dB |
| SNR | 1 kHz, −0.5 dBFS, sine wave input | | | | |
| | Sinc5 filter | 109 | 111 | | dB |
| | Wideband filter | 106 | 107.8 | | dB |
| SINAD | 1 kHz, −0.5 dBFS, sine wave input | 105.8 | 107.5 | | dB |
| THD | 1 kHz, −0.5 dBFS, sine wave input | | −120 | −113 | dB |
| SFDR | | | 128 | | dBc |
| Eco | Decimation by 32, 32 kHz ODR | | | | |
| Dynamic Range | Shorted input, wideband filter | 106.2 | 108 | | dB |
| SNR | Sinc5 filter, 1 kHz, −0.5 dBFS, sine wave input | 109 | 111 | | dB |
| | Wideband filter, 1 kHz, −0.5 dBFS, sine wave input | 106 | 107.8 | | dB |
| SINAD | 1 kHz, −0.5 dBFS, sine wave input | 105.8 | 107.5 | | dB |
| THD | 1 kHz, −0.5 dBFS, sine wave input | | −120 | −113 | dB |
| SFDR | | | 128 | | dBc |
| ACCURACY[1] | | | | | |
| INL | Endpoint method | | ±2 | ±7 | ppm of FSR |
| Offset Error[2] | DCLK frequency ≤ 24 MHz | | ±50 | ±115 | µV |
| | 24 MHz to 32.768 MHz DCLK frequency | | ±75 | ±170 | µV |
| Offset Error Drift | DCLK frequency ≤ 24 MHz | | ±250 | | nV/°C |
| | 24 MHz to 32.768 MHz DCLK frequency | | ±750 | | nV/°C |
| Gain Error[2] | $T_A$ = 25°C | | ±60 | ±120 | ppm/FSR |
| Gain Drift vs. Temperature | | | ±0.5 | ±2 | ppm/°C |
| LOGIC INPUTS | | | | | |
| Input Voltage[1] | | | | | |
| High, $V_{INH}$ | | 0.65 × IOVDD | | | V |
| Low, $V_{INL}$ | | | | 0.4 | V |
| Hysteresis[1] | | 0.04 | | 0.2 | V |
| Leakage Current | | −10 | +0.03 | +10 | µA |
| | $\overline{\text{RESET}}$ pin | −10 | | +10 | µA |
| LOGIC OUTPUTS | | | | | |
| Output Voltage[1] | | | | | |
| High, $V_{OH}$ | $I_{SOURCE}$ = 200 µA | 0.8 × IOVDD | | | V |
| Low, $V_{OL}$ | $I_{SINK}$ = 400 µA | | | 0.4 | V |
| Leakage Current | Floating state | −10 | | +10 | µA |
| Output Capacitance | Floating state | | 10 | | pF |
| POWER REQUIREMENTS | | | | | |
| Power Supply Voltage | | | | | |
| AVDD1 − AVSS | | 4.5 | 5.0 | 5.5 | V |
| AVDD2 − AVSS | | 2.0 | 2.25 to 5.0 | 5.5 | V |
| AVSS − DGND | | −2.75 | | 0 | V |
| IOVDD − DGND | DREGCAP shorted to IOVDD | 1.72 | 1.8 | 1.88 | V |
| POWER SUPPLY CURRENTS[1] | Maximum output data rate, CMOS MCLK, eight DOUTx signals, all supplies at maximum voltages, all channels in Channel Mode A except where otherwise specified | | | | |
| AD7768 | Eight channels active | | | | |
| Fast Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 36/57.5 | 40/64 | mA |
| AVDD2 Current | | | 37.5 | 40 | mA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| IOVDD Current | Wideband filter | | 63 | 69 | mA |
| | Sinc5 filter | | 26 | 28.4 | mA |
| Median Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 18.5/29 | 20.5/32.5 | mA |
| AVDD2 Current | | | 21.3 | 23 | mA |
| IOVDD Current | Wideband filter | | 34 | 36.8 | mA |
| | Sinc5 filter | | 15 | 16.8 | mA |
| Eco Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 5.1/8 | 5.8/9 | mA |
| AVDD2 Current | | | 9.3 | 10.1 | mA |
| IOVDD Current | Wideband filter | | 11.6 | 12.9 | mA |
| | Sinc5 filter | | 7 | 8.1 | mA |
| AD7768-4 | Four channels active | | | | |
| Fast Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 18.2/28.8 | 20.3/32.5 | mA |
| AVDD2 Current | | | 18.8 | 20.3 | mA |
| IOVDD Current | Wideband filter | | 43.9 | 47.7 | mA |
| | Wideband filter, SPI mode only; Channel Mode A set to sinc5 filter[3] | | 36.8 | 41 | mA |
| | Sinc5 filter | | 16 | 17.7 | mA |
| Median Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 9.3/14.7 | 10.5/16.6 | mA |
| AVDD2 Current | | | 10.7 | 11.7 | mA |
| IOVDD Current | Wideband filter | | 24 | 26.1 | mA |
| | Wideband filter, SPI mode only; Channel Mode A set to sinc5 filter[3] | | 20.4 | 22.7 | mA |
| | Sinc5 filter | | 10 | 11.3 | mA |
| Eco Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 2.7/4.1 | 3.1/4.7 | mA |
| AVDD2 Current | | | 4.7 | 5.3 | mA |
| IOVDD Current | Wideband filter | | 9 | 10.2 | mA |
| | Wideband filter, SPI mode only; Channel Mode A set to sinc5 filter[3] | | 8.1 | 9.2 | mA |
| | Sinc5 filter | | 5.5 | 6.5 | mA |
| AD7768 and AD7768-4—Two Channels Active | SPI control mode only; see the Channel Standby section for details on disabling channels | | | | |
| Fast Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 9.3/14.7 | 10.5/16.6 | mA |
| AVDD2 Current | | | 9.5 | 10.5 | mA |
| IOVDD Current | Wideband filter | | 33.8 | 36.7 | mA |
| | Wideband filter, SPI mode only; disabled channels in Channel Mode A, and set to sinc5 filter[3] | | 23.1 | 25.6 | mA |
| | Sinc5 filter | | 11 | 12.3 | mA |
| Median Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 4.8/7.5 | 5.5/8.6 | mA |
| AVDD2 Current | | | 5.5 | 6.2 | mA |
| IOVDD Current | Wideband filter | | 18.9 | 20.6 | mA |
| | Wideband filter, SPI mode only; disabled channels in Channel Mode A, and set to sinc5 filter[3] | | 13.4 | 15.1 | mA |
| | Sinc5 filter | | 7.4 | 8.6 | mA |
| Eco Mode | | | | | |
| AVDD1 Current | Reference precharge buffers off/on | | 1.52/2.2 | 1.77/2.6 | mA |
| AVDD2 Current | | | 2.4 | 3 | mA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| IOVDD Current | Wideband filter | | 7.6 | 8.8 | mA |
| | Wideband filter, SPI mode only; disabled channels in Channel Mode A, and set to sinc5 filter[3] | | 6.3 | 7.2 | mA |
| | Sinc5 filter | | 4.8 | 5.8 | mA |
| Standby Mode | All channels disabled (sinc5 filter enabled) | | 6.5 | 8 | mA |
| Sleep Mode | Full power-down (SPI control mode) | | 0.73 | 1.2 | mA |
| Crystal Excitation Current | Extra current in IOVDD when using an external crystal compared to using the CMOS MCLK | | 540 | | µA |
| POWER DISSIPATION[1] | External CMOS MCLK, all channels active, AVDD1 = AVDD2 = 5.5 V, IOVDD = 1.88 V, MCLK = 32.768 MHz, all channels in Channel Mode A except where otherwise noted | | | | |
| Full Operating Mode | Analog precharge buffers on | | | | |
| AD7768 | Eight channels active | | | | |
| Wideband Filter | | | | | |
| Fast | Reference precharge buffers off | | 524 | 571 | mW |
| | Reference precharge buffers on | | 638 | 704 | mW |
| Median | Reference precharge buffers off | | 284 | 309 | mW |
| | Reference precharge buffers on | | 342 | 375 | mW |
| Eco | Reference precharge buffers off | | 98.5 | 109 | mW |
| | Reference precharge buffers on | | 118 | 130 | mW |
| Sinc5 Filter | | | | | |
| Fast | Reference precharge buffers off | | 455 | 495 | mW |
| Median | Reference precharge buffers off | | 248 | 271 | mW |
| Eco | Reference precharge buffers off | | 94 | 105 | mW |
| AD7768-4 | Four channels active | | | | |
| Wideband Filter | | | | | |
| Fast | Reference precharge buffers off | | 287 | 314 | mW |
| | Reference precharge buffers on | | 345 | 381 | mW |
| Median | Reference precharge buffers off | | 156 | 172 | mW |
| | Reference precharge buffers on | | 185 | 206 | mW |
| Eco | Reference precharge buffers off | | 58 | 66 | mW |
| | Reference precharge buffers on | | 66 | 75 | mW |
| Sinc5 Filter | | | | | |
| Fast | Reference precharge buffers off | | 234 | 257 | mW |
| Median | Reference precharge buffers off | | 129 | 144 | mW |
| Eco | Reference precharge buffers off | | 51 | 59 | mW |
| Standby Mode | All channels disabled (sinc5 filter enabled) | | | 17 | mW |
| Sleep Mode | Full power-down (SPI control mode) | | 1.5 | 4.5 | mW |

[1] These specifications are not production tested but are supported by characterization data at initial product release.
[2] Following a system zero-scale calibration, the offset error is in the order of the noise for the programmed output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed output data rate.
[3] This configuration of setting Channel Mode A to the sinc5 filter and/or assigning disabled channels to Channel Mode A allows a lower power consumption to be achieved due to the disabling of internal clocks on the disabled only and sinc5 only channel modes. This configuration requires assigning sinc5 and wideband filters to different channels, or channel modes, and is only available in SPI control mode. In pin control mode, all channels, whether active or in standby, effectively use the same channel mode. See the Channel Modes section for more details.

## TIMING SPECIFICATIONS

AVDD1A = AVDD1B = 5 V, AVDD2A = AVDD2B = 5 V, IOVDD = 2.25 V to 3.6 V, Input Logic 0 = DGND, Input Logic 1 = IOVDD; $C_{LOAD}$ = 10 pF on the DCLK pin, $C_{LOAD}$ = 20 pF on the other digital outputs; REFx+ = 4.096 V, $T_A$ = −40°C to +105°C. See Table 5 and Table 6 for timing specifications at 1.8 V IOVDD.

**Table 3. Data Interface Timing[1]**

| Parameter | Description | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| MCLK | Master clock | | 1.15 | | 34 | MHz |
| $f_{MOD}$ | Modulator frequency | Fast mode | | MCLK/4 | | Hz |
| | | Median mode | | MCLK/8 | | Hz |
| | | Eco mode | | MCLK/32 | | Hz |
| $t_1$ | $\overline{DRDY}$ high time | $t_{DCLK} = t_8 + t_9$ | $t_{DCLK}$ − 10% | 28 | | ns |
| $t_2$ | DCLK rising edge to $\overline{DRDY}$ rising edge | | | | 2 | ns |
| $t_3$ | DCLK rising to $\overline{DRDY}$ falling | | −3.5 | | 0 | ns |
| $t_4$ | DCLK rise to DOUTx valid | | | | 1.5 | ns |
| $t_5$ | DCLK rise to DOUTx invalid | | −3 | | | ns |
| $t_6$ | DOUTx valid to DCLK falling | | 9.5 | $t_{DCLK}/2$ | | ns |
| $t_7$ | DCLK falling edge to DOUTx invalid | | 9.5 | $t_{DCLK}/2$ | | ns |
| $t_8$ | DCLK high time, DCLK = MCLK/1 | 50:50 CMOS clock | $t_{DCLK}/2$ | $t_{DCLK}/2$ | $(t_{DCLK}/2) + 5$ | ns |
| | $t_{8a}$ = DCLK = MCLK/2 | $t_{MCLK}$ = 1/MCLK | | $t_{MCLK}$ | | ns |
| | $t_{8b}$ = DCLK = MCLK/4 | | | $2 \times t_{MCLK}$ | | ns |
| | $t_{8c}$ = DCLK = MCLK/8 | | | $4 \times t_{MCLK}$ | | ns |
| $t_9$ | DCLK low time DCLK = MCLK/1 | 50:50 CMOS clock | $(t_{DCLK}/2) - 5$ | $t_{MCLK}/2$ | $t_{DCLK}/2$ | ns |
| | $t_{9a}$ = DCLK = MCLK/2 | | | $t_{MCLK}$ | | ns |
| | $t_{9b}$ = DCLK = MCLK/4 | | | $2 \times t_{MCLK}$ | | ns |
| | $t_{9c}$ = DCLK = MCLK/8 | | | $4 \times t_{MCLK}$ | | ns |
| $t_{10}$ | MCLK rising to DCLK rising | CMOS clock | | | 30 | ns |
| $t_{11}$ | Setup time (daisy-chain inputs) | DOUT6 and DOUT7 on the AD7768, DIN on the AD7768-4 | 14 | | | ns |
| $t_{12}$ | Hold time (daisy-chain inputs) | DOUT6 and DOUT7 on the AD7768, DIN on the AD7768-4 | 0 | | | ns |
| $t_{13}$ | $\overline{START}$ low time | | $1 \times t_{MCLK}$ | | | ns |
| $t_{14}$ | MCLK to $\overline{SYNC\_OUT}$ valid | CMOS clock | | | | |
| | | $\overline{SYNC\_OUT}$ RETIME_EN bit disabled; measured from falling edge of MCLK | 4.5 | | 22 | ns |
| | | $\overline{SYNC\_OUT}$ RETIME_EN bit enabled; measured from rising edge of MCLK | 9.5 | | 27.5 | ns |
| $t_{15}$ | $\overline{SYNC\_IN}$ setup time | CMOS clock | 0 | | | ns |
| $t_{16}$ | $\overline{SYNC\_IN}$ hold time | CMOS clock | 10 | | | ns |

[1] These specifications are not production tested but are supported by characterization data at initial product release.

**Table 4. SPI Control Interface Timing[1]**

| Parameter | Description | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{17}$ | SCLK period | | 100 | | | ns |
| $t_{18}$ | $\overline{CS}$ falling edge to SCLK rising edge | | 26.5 | | | ns |
| $t_{19}$ | SCLK falling edge to $\overline{CS}$ rising edge | | 27 | | | ns |
| $t_{20}$ | $\overline{CS}$ falling edge to data output enable | | 22.5 | | 40.5 | ns |
| $t_{21}$ | SCLK high time | | 20 | 50 | | ns |
| $t_{22}$ | SCLK low time | | 20 | 50 | | ns |
| $t_{23}$ | SCLK falling edge to SDO valid | | | | 15 | ns |
| $t_{24}$ | SDO hold time after SCLK falling | | 7 | | | ns |
| $t_{25}$ | SDI setup time | | 0 | | | ns |
| $t_{26}$ | SDI hold time | | 6 | | | ns |
| $t_{27}$ | SCLK enable time | | 0 | | | ns |

| Parameter | Description | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{28}$ | SCLK disable time | | 0 | | | ns |
| $t_{29}$ | $\overline{CS}$ high time | | 10 | | | ns |
| $t_{30}$ | $\overline{CS}$ low time | $f_{MOD}$ = MCLK/4 | 1.1 × $t_{MCLK}$ | | | ns |
| | | $f_{MOD}$ = MCLK/8 | 2.2 × $t_{MCLK}$ | | | ns |
| | | $f_{MOD}$ = MCLK/32 | 8.8 × $t_{MCLK}$ | | | ns |

[1] These specifications are not production tested but are supported by characterization data at initial product release.

## 1.8 V IOVDD TIMING SPECIFICATIONS

AVDD1A = AVDD1B = 5 V, AVDD2A = AVDD2B = 5 V, IOVDD = 1.72 V to 1.88 V (DREGCAP tied to IOVDD), Input Logic 0 = DGND, Input Logic 1 = IOVDD, $C_{LOAD}$ = 10 pF on DCLK pin, $C_{LOAD}$ = 20 pF on other digital outputs, $T_A$ = −40°C to +105°C. $t_{ODR}$ is 1/ODR.

**Table 5. Data Interface Timing[1]**

| Parameter | Description | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| MCLK | Master clock | | 1.15 | | 34 | MHz |
| $f_{MOD}$ | Modulator frequency | Fast mode | | MCLK/4 | | Hz |
| | | Median mode | | MCLK/8 | | Hz |
| | | Eco mode | | MCLK/32 | | Hz |
| $t_1$ | $\overline{DRDY}$ high time | | $t_{DCLK}$ − 10% | 28 | | ns |
| $t_2$ | DCLK rising edge to $\overline{DRDY}$ rising edge | | | | 2 | ns |
| $t_3$ | DCLK rising to $\overline{DRDY}$ falling | | −4.5 | | 0 | ns |
| $t_4$ | DCLK rise to DOUTx valid | | | | 2.0 | ns |
| $t_5$ | DCLK rise to DOUTx invalid | | −4 | | | ns |
| $t_6$ | DOUTx valid to DCLK falling | | 8.5 | $t_{DCLK}$/2 | | ns |
| $t_7$ | DCLK falling edge to DOUTx invalid | | 8.5 | $t_{DCLK}$/2 | | ns |
| $t_8$ | DCLK high time, DCLK = MCLK/1 | 50:50 CMOS clock | $t_{DCLK}$/2 | $t_{DCLK}$/2 | ($t_{DCLK}$/2) + 5 | ns |
| | $t_{8a}$ = DCLK = MCLK/2 | | | $t_{MCLK}$ | | ns |
| | $t_{8b}$ = DCLK = MCLK/4 | | | 2 × $t_{MCLK}$ | | ns |
| | $t_{8c}$ = DCLK = MCLK/8 | | | 4 × $t_{MCLK}$ | | ns |
| $t_9$ | DCLK low time DCLK=MCLK/1 | 50:50 CMOS clock | ($t_{DCLK}$/2) − 5 | $t_{MCLK}$/2 | ($t_{DCLK}$/2 | ns |
| | $t_{9a}$ = DCLK = MCLK/2 | | | $t_{MCLK}$ | | ns |
| | $t_{9b}$ = DCLK = MCLK/4 | | | 2 × $t_{MCLK}$ | | ns |
| | $t_{9c}$ = DCLK = MCLK/8 | | | 4 × $t_{MCLK}$ | | ns |
| $t_{10}$ | MCLK rising to DCLK rising | CMOS clock | | | 37 | ns |
| $t_{11}$ | Setup time (daisy-chain inputs) | DOUT6 and DOUT7 on the AD7768, DIN on the AD7768-4 | 14 | | | ns |
| $t_{12}$ | Hold time (daisy-chain inputs) | DOUT6 and DOUT7 on the AD7768, DIN on the AD7768-4 | 0 | | | ns |
| $t_{13}$ | $\overline{START}$ low time | | 1 × $t_{MCLK}$ | | | ns |
| $t_{14}$ | MCLK to $\overline{SYNC\_OUT}$ valid | CMOS clock | | | | |
| | | $\overline{SYNC\_OUT}$ RETIME_EN bit disabled; measured from falling edge of MCLK | 10 | | 31 | ns |
| | | $\overline{SYNC\_OUT}$ RETIME_EN bit enabled; measured from rising edge of MCLK | 15 | | 37 | ns |
| $t_{15}$ | $\overline{SYNC\_IN}$ setup time | CMOS clock | 0 | | | ns |
| $t_{16}$ | $\overline{SYNC\_IN}$ hold time | CMOS clock | 11 | | | ns |

[1] These specifications are not production tested but are supported by characterization data at initial product release.

**Table 6. SPI Control Interface Timing[1]**

| Parameter | Description | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{17}$ | SCLK period | | 100 | | | ns |
| $t_{18}$ | $\overline{CS}$ falling edge to SCLK rising edge | | 31.5 | | | ns |
| $t_{19}$ | SCLK falling edge to $\overline{CS}$ rising edge | | 30 | | | ns |
| $t_{20}$ | $\overline{CS}$ falling edge to data output enable | | 29 | | 54 | ns |
| $t_{21}$ | SCLK high time | | 20 | 50 | | ns |
| $t_{22}$ | SCLK low time | | 20 | 50 | | ns |
| $t_{23}$ | SCLK falling edge to SDO valid | | | | 16 | ns |
| $t_{24}$ | SDO hold time after SCLK falling | | 7 | | | ns |
| $t_{25}$ | SDI setup time | | 0 | | | ns |
| $t_{26}$ | SDI hold time | | 10 | | | ns |
| $t_{27}$ | SCLK enable time | | 0 | | | ns |
| $t_{28}$ | SCLK disable time | | 0 | | | ns |
| $t_{29}$ | $\overline{CS}$ high time | | 10 | | | ns |
| $t_{30}$ | $\overline{CS}$ low time | $f_{MOD}$ = MCLK/4 | 1.1 × $t_{MCLK}$ | | | ns |
| | | $f_{MOD}$ = MCLK/8 | 2.2 × $t_{MCLK}$ | | | ns |
| | | $f_{MOD}$ = MCLK/32 | 8.8 × $t_{MCLK}$ | | | ns |

[1] These specifications are not production tested but are supported by characterization data at initial product release.

### *Timing Diagrams*

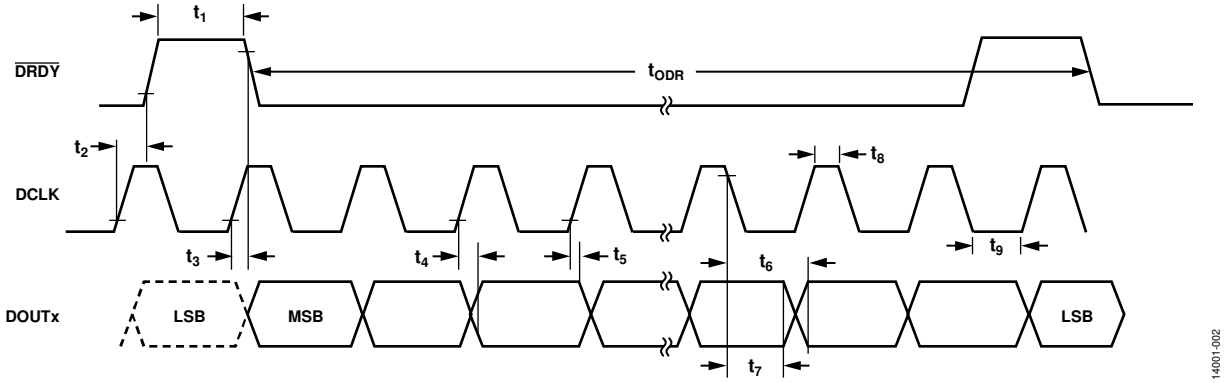


*Figure 2. Data Interface Timing Diagram*

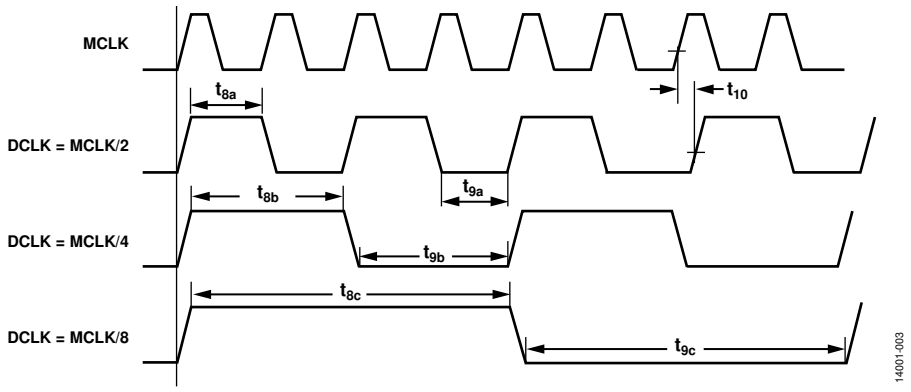


*Figure 3. MCLK to DCLK Divider Timing Diagram*

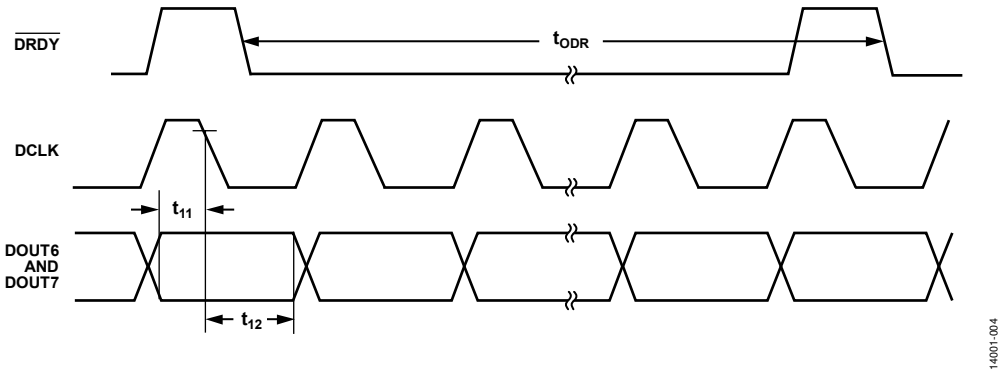


*Figure 4. Daisy-Chain Setup and Hold Timing Diagram*

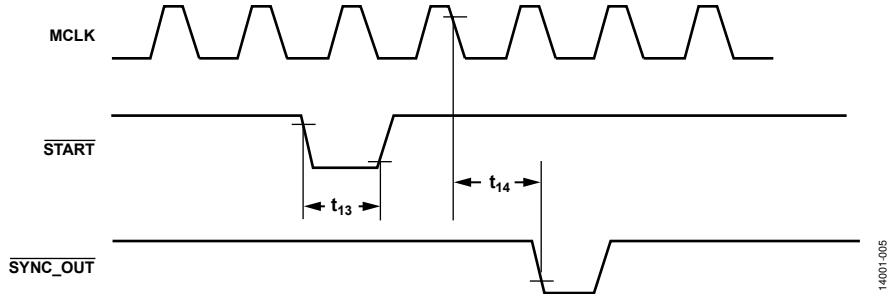


*Figure 5. Asynchronous $\overline{START}$ and $\overline{SYNC\_OUT}$ Timing Diagram*

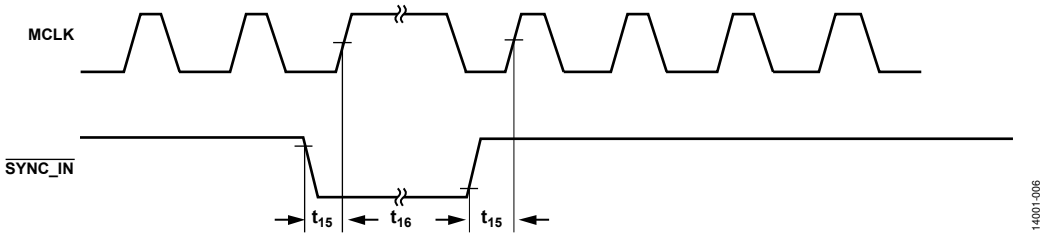


*Figure 6. Synchronous $\overline{SYNC\_IN}$ Pulse Timing Diagram*

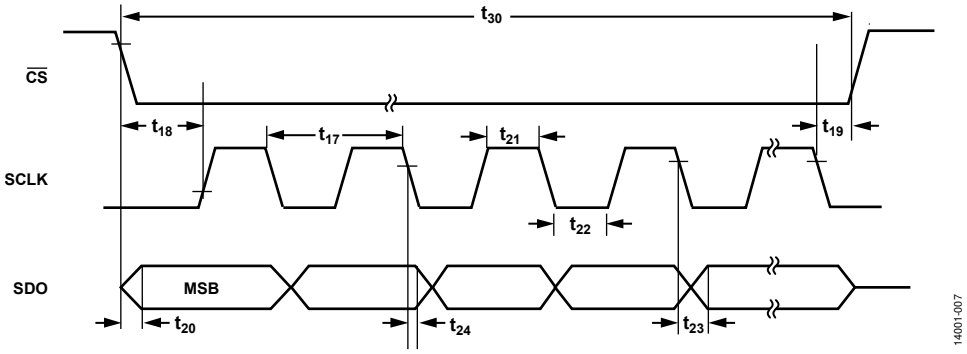


*Figure 7. SPI Serial Read Timing Diagram*

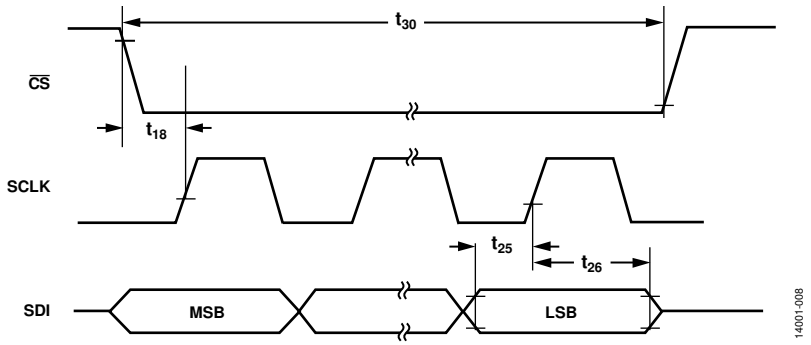


*Figure 8. SPI Serial Write Timing Diagram*

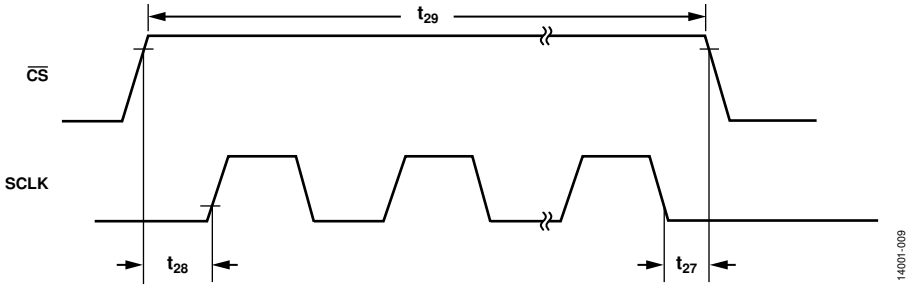


*Figure 9. SCLK Enable and Disable Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

**Table 7.**

| Parameter | Rating |
|---|---|
| AVDD1, AVDD2 to AVSS[1] | −0.3 V to +6.5 V |
| AVDD1 to DGND | −0.3 V to +6.5 V |
| IOVDD to DGND | −0.3 V to +6.5 V |
| IOVDD, DREGCAP to DGND (IOVDD Tied to DREGCAP for 1.8 V Operation) | −0.3 V to +2.25 V |
| IOVDD to AVSS | −0.3 V to +7.5 V |
| AVSS to DGND | −3.25 V to +0.3 V |
| Analog Input Voltage to AVSS | −0.3 V to AVDD1 + 0.3 V |
| Reference Input Voltage to AVSS | −0.3 V to AVDD1 + 0.3 V |
| Digital Input Voltage to DGND | −0.3 V to IOVDD + 0.3 V |
| Digital Output Voltage to DGND | −0.3 V to IOVDD + 0.3 V |
| Operating Temperature Range | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Pb-Free Temperature, Soldering Reflow (10 sec to 30 sec) | 260°C |
| Maximum Junction Temperature | 150°C |
| Maximum Package Classification Temperature | 260°C |

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 8. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit | JEDEC Board Layers |
|---|---|---|---|---|
| 64-Lead LQFP | 38 | 9.2 | °C/W | 2P2S[1] |

[1] 2P2S is a JEDEC standard PCB configuration per JEDEC Standard JESD51-7.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

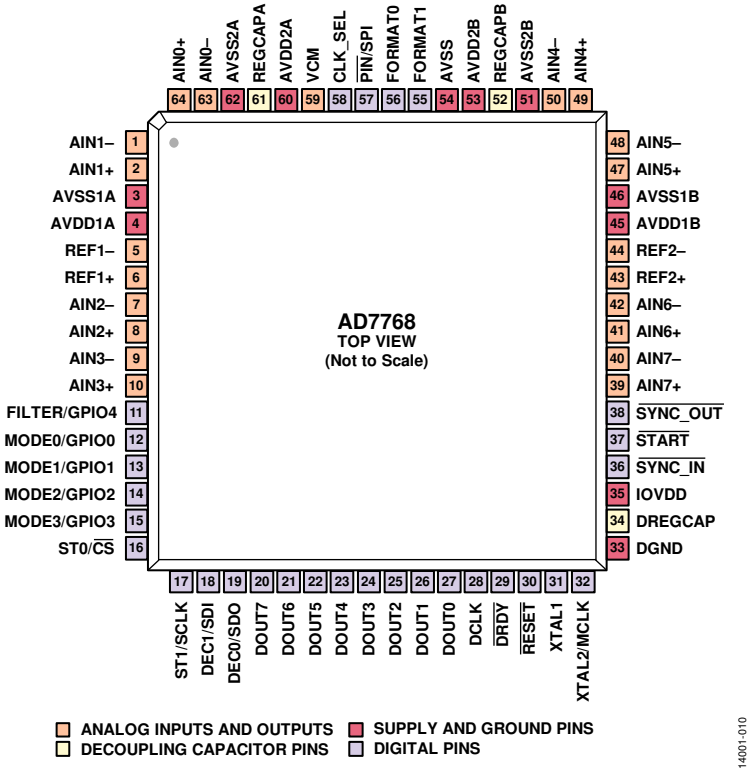


*Figure 10. AD7768 Pin Configuration*

**Table 9. Pin Function Descriptions**

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 1 | AIN1– | AI | Negative Analog Input to ADC Channel 1. |
| 2 | AIN1+ | AI | Positive Analog Input to ADC Channel 1. |
| 3 | AVSS1A | P | Negative Analog Supply. This pin is nominally 0 V. |
| 4 | AVDD1A | P | Analog Supply Voltage, 5 V ± 10% with Respect to AVSS. |
| 5 | REF1– | AI | Reference Input, Negative. REF1– is the negative reference terminal for Channel 0 to Channel 3. The REF1– voltage range is from AVSS to (AVDD1 – 1 V). Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 3. |
| 6 | REF1+ | AI | Reference Input, Positive. REF1+ is the positive reference terminal for Channel 0 to Channel 3. The REF1+ voltage range is from (AVSS + 1 V) to AVDD1. Apply an external differential reference voltage between REF1+ and REF1– in the range from 1 V to \|AVDD1 – AVSS\|. Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 3. |
| 7 | AIN2– | AI | Negative Analog Input to ADC Channel 2. |
| 8 | AIN2+ | AI | Positive Analog Input to ADC Channel 2. |
| 9 | AIN3– | AI | Negative Analog Input to ADC Channel 3. |
| 10 | AIN3+ | AI | Positive Analog Input to ADC Channel 3. |
| 11 | FILTER/GPIO4 | DI/O | Filter Select/General-Purpose Input/Output 4. In pin control mode, this pin selects the filter type.<br>Set this pin to Logic 1 for the sinc5 filter. This sinc5 filter is a low latency filter, and is best for dc applications or where a user has specialized postfiltering implemented off chip.<br>Set this pin to Logic 0 for the wideband low ripple filter response. This filter has a steep transition band and 105 dB stop band attenuation. Full attenuation at Nyquist (ODR/2) means that no aliasing occurs at ODR/2 out to the first chopping zone.<br>When in SPI control mode, this pin can be used as a general-purpose input/output (GPIO4). See Table 49 for more details. |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 12, 13, 14, 15 | MODE0/GPIO0, MODE1/GPIO1, MODE2/GPIO2, MODE3/GPIO3 | DI/DI/O | Mode Selection/General-Purpose Input/Output Pin 0 to Pin 3.<br>In pin control mode, the MODEx pins set the mode of operation for all ADC channels, controlling power consumption, DCLK frequency, and the ADC conversion type, allowing one-shot conversion operation.<br>In SPI control mode, the GPIOx pins, in addition to the FILTER/GPIO4 pin, form five general-purpose input/output pins (GPIO4 to GPIO0). See Table 49 for more details. |
| 16 | ST0/$\overline{CS}$ | DI | Standby 0/Chip Select Input.<br>In pin control mode, a Logic 1 places Channel 0 to Channel 3 into standby mode.<br>In SPI control mode, this pin is the active low chip select input to the SPI control interface. The VCM voltage output is associated with the Channel 0 circuitry. If Channel 0 is put into standby mode, the VCM voltage output is also disabled for maximum power savings. Channel 0 must be enabled while VCM is being used externally to the AD7768. |
| 17 | ST1/SCLK | DI | Standby 1/Serial Clock Input.<br>In pin control mode, a Logic 1 on this pin places Channel 4 to Channel 7 into standby mode.<br>In SPI control mode, this pin is the serial clock input pin for the SPI control interface. The crystal excitation circuitry is associated with the Channel 4 circuitry. If Channel 4 is put into standby mode, the crystal circuitry is also disabled for maximum power savings. Channel 4 must be enabled while the external crystal is used on the AD7768. |
| 18 | DEC1/SDI | DI | Decimation Rate Control Input 1/Serial Data Input.<br>In pin control mode, the DEC0 and DEC1 pins configure the decimation rate for all ADC channels. See Table 17 in the Setting the Decimation Rate section for more information.<br>In SPI control mode, this pin is the serial data input pin used to write data to the AD7768 register bank. |
| 19 | DEC0/SDO | DI/O | Decimation Rate Control Input 0/Serial Data Output.<br>In pin control mode, the DEC0 and DEC1 pins configure the decimation rate for all ADC channels. See Table 17 in the Setting the Decimation Rate section for more information.<br>In SPI control mode, this pin is the serial data output pin, allowing readback from the AD7768 registers. |
| 20 | DOUT7 | DI/O | Conversion Data Output 7. This pin is synchronous to DCLK and framed by $\overline{DRDY}$. This pin acts as a digital input from a separate AD7768 device if configured in a synchronized multidevice daisy chain when the FORMATx pins are configured as 01. To use the AD7768 in a daisy chain, hardwire the FORMATx pins as 01, 10, or 11, depending on the best interfacing format for the application. When FORMATx is set to 01, 10, or 11, and daisy-chaining is not used, connect this pin to ground through a pull-down resistor. |
| 21 | DOUT6 | DI/O | Conversion Data Output 6. This pin is synchronous to DCLK and framed by $\overline{DRDY}$. This pin acts as a digital input from a separate AD7768 device if configured in a synchronized multidevice daisy chain. To use this pin in a daisy chain, hardwire the FORMATx pins as 01, 10, or 11, depending on the best interfacing format for the application. When FORMATx is set to 01, 10, or 11, and daisy chaining is not used, connect this pin to ground through a pull-down resistor. |
| 22 | DOUT5 | DO | Conversion Data Output 5. This pin is synchronous to DCLK and framed by $\overline{DRDY}$. |
| 23 | DOUT4 | DO | Conversion Data Output 4. This pin is synchronous to DCLK and framed by $\overline{DRDY}$. |
| 24 | DOUT3 | DO | Conversion Data Output 3. This pin is synchronous to DCLK and framed by $\overline{DRDY}$. |
| 25 | DOUT2 | DO | Conversion Data Output 2. This pin is synchronous to DCLK and framed by $\overline{DRDY}$. |
| 26 | DOUT1 | DO | Conversion Data Output 1. This pin is synchronous to DCLK and framed by $\overline{DRDY}$. |
| 27 | DOUT0 | DO | Conversion Data Output 0. This pin is synchronous to DCLK and framed by $\overline{DRDY}$ |
| 28 | DCLK | DO | ADC Conversion Data Clock. This pin clocks conversion data out to the digital host (digital signal processor (DSP)/field-programmable gate array (FPGA)). This pin is synchronous with $\overline{DRDY}$ and any conversion data output on DOUT0 to DOUT7 and is derived from the MCLK signal. This pin is unrelated to the control SPI interface. |
| 29 | $\overline{DRDY}$ | DO | Data Ready. $\overline{DRDY}$ is a periodic signal output framing the conversion results from the eight ADCs. This pin is synchronous to DCLK and DOUT0 to DOUT7. |
| 30 | $\overline{RESET}$ | DI | Hardware Asynchronous Reset Input. After the device is fully powered up, it is recommended to perform a hard reset using this pin or, alternatively, to perform a soft reset by issuing a reset over the SPI control interface |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 31 | XTAL1 | DI | Input 1 for Crystal or Connection to an LVDS Clock. When CLK_SEL is 0, connect XTAL1 to DGND. The crystal excitation circuitry is associated with the Channel 4 circuitry. If Channel 4 is put into standby mode, the crystal circuitry is also disabled for maximum power savings. Channel 4 must be enabled while the external crystal is used on the AD7768. When used with an LVDS clock, connect this pin to one trace of the LVDS signal pair. When used as an LVDS input, a rising edge on this pin is detected as a rising MCLK edge by the AD7768. |
| 32 | XTAL2/MCLK | DI | Input 2 for CMOS or Crystal/LVDS Sampling Clock. See the CLK_SEL pin for the details of this configuration.<br>External crystal: XTAL2 is connected to the external crystal.<br>LVDS clock: when used with an LVDS clock, connect this pin to the second trace of the LVDS signal pair.<br>CMOS clock: this pin operates as an MCLK input. This pin is a CMOS input with a logic level of IOVDD/DGND. When used as a CMOS clock input, a rising edge on this pin is detected as a rising MCLK edge by the AD7768.<br>The crystal excitation circuitry is associated with the Channel 4 circuitry. If Channel 4 is put into standby mode, the crystal circuitry is also disabled for maximum power savings. Channel 4 must be enabled while the external crystal is used on the AD7768. |
| 33 | DGND | P | Digital Ground. This pin is nominally 0 V. |
| 34 | DREGCAP | AO | Digital Low Dropout (LDO) Regulator Output. Decouple this pin to DGND with a high quality, low ESR, 10 µF capacitor. For optimum performance, use a decoupling capacitor with an ESR specification of less than 400 mΩ. This pin is not for use in circuits external to the AD7768. For 1.8 V IOVDD operation, connect this pin to IOVDD via an external trace to provide power to the digital processing core. |
| 35 | IOVDD | P | Digital Supply. This pin sets the logic levels for all interface pins. IOVDD also powers the digital processing core via the digital LDO when IOVDD is at least 2.25 V. For 1.8 V IOVDD operation, connect this pin to DREGCAP via an external trace to provide power to the digital processing core. |
| 36 | $\overline{\text{SYNC\_IN}}$ | DI | Synchronization Input. $\overline{\text{SYNC\_IN}}$ receives the synchronous signal from $\overline{\text{SYNC\_OUT}}$. It is used in the synchronization of any AD7768 that requires simultaneous sampling or is in a daisy chain. Ignore the $\overline{\text{START}}$ and $\overline{\text{SYNC\_OUT}}$ functions if the $\overline{\text{SYNC\_IN}}$ pin is connected to the system synchronization pulse. This signal pulse must be synchronous to the MCLK clock domain. In a daisy-chained system of AD7768 devices, two successive synchronization pulses must be applied to guarantee that all ADCs are synchronized. Two synchronization pulses are also required in a system of more than one AD7768 device sharing a single MCLK signal, where the $\overline{\text{DRDY}}$ pin of only one device is used to detect new data. |
| 37 | $\overline{\text{START}}$ | DI | Start Signal. The $\overline{\text{START}}$ pulse synchronizes the AD7768 to other devices. The signal can be asynchronous. The AD7768 samples the input and then outputs a $\overline{\text{SYNC\_OUT}}$ pulse. This $\overline{\text{SYNC\_OUT}}$ pulse must be routed to the $\overline{\text{SYNC\_IN}}$ pin of this device, and any other AD7768 devices that must be synchronized together. This means that the user does not need to run the ADCs and their digital host from the same clock domain, which is useful when there are long traces or back planes between the ADC and the controller. If this pin is not used, it must be tied to a Logic 1 through a pull-up resistor. In a daisy-chained system of AD7768 devices, two successive synchronization pulses must be applied to guarantee that all ADCs are synchronized. Two synchronization pulses are also required in a system of more than one AD7768 device sharing a single MCLK signal, where the $\overline{\text{DRDY}}$ pin of only one device is used to detect new data. |
| 38 | $\overline{\text{SYNC\_OUT}}$ | DO | Synchronization Output. This pin operates only when the $\overline{\text{START}}$ input is used. When using the $\overline{\text{START}}$ input feature, the $\overline{\text{SYNC\_OUT}}$ pin must be connected to $\overline{\text{SYNC\_IN}}$ via an external trace. $\overline{\text{SYNC\_OUT}}$ is a digital output that is synchronous to the MCLK signal; the synchronization signal driven in on $\overline{\text{START}}$ is internally synchronized to the MCLK signal and is driven out on $\overline{\text{SYNC\_OUT}}$. $\overline{\text{SYNC\_OUT}}$ can also be routed to other AD7768 devices requiring simultaneous sampling and/or daisy-chaining, ensuring synchronization of devices related to the MCLK clock domain. It must then be wired to drive the $\overline{\text{SYNC\_IN}}$ pin on the same AD7768 and on the other AD7768 devices. |
| 39 | AIN7+ | AI | Positive Analog Input to ADC Channel 7. |
| 40 | AIN7− | AI | Negative Analog Input to ADC Channel 7. |
| 41 | AIN6+ | AI | Positive Analog Input to ADC Channel 6. |
| 42 | AIN6− | AI | Negative Analog Input to ADC Channel 6. |
| 43 | REF2+ | AI | Reference Input, Positive. REF2+ is the positive reference terminal for Channel 4 to Channel 7. The REF2+ voltage range is from (AVSS + 1 V) to AVDD1. Apply an external differential reference voltage between REF2+ and REF2− in the range from 1 V to \|AVDD1 − AVSS\|. Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 46. |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 44 | REF2− | AI | Reference Input, Negative. REF2− is the negative reference terminal for Channel 4 to Channel 7. The REF2− voltage range is from AVSS to (AVDD1 − 1 V). Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 46. |
| 45 | AVDD1B | P | Analog Supply Voltage. This pin is 5 V ± 10% with respect to AVSS. |
| 46 | AVSS1B | P | Negative Analog Supply. This pin is nominally 0 V. |
| 47 | AIN5+ | AI | Positive Analog Input to ADC Channel 5. |
| 48 | AIN5− | AI | Negative Analog Input to ADC Channel 5. |
| 49 | AIN4+ | AI | Positive Analog Input to ADC Channel 4. |
| 50 | AIN4− | AI | Negative Analog Input to ADC Channel 4. |
| 51 | AVSS2B | P | Negative Analog Supply. This pin is nominally 0 V. |
| 52 | REGCAPB | AO | Analog LDO Regulator Output. Decouple this pin to AVSS with a 1 µF capacitor. |
| 53 | AVDD2B | P | Analog Supply Voltage. This pin is 2 V to 5.5 V with respect to AVSS. |
| 54 | AVSS | P | Negative Analog Supply. This pin is nominally 0 V. |
| 55, 56 | FORMAT1, FORMAT0 | DI | Format Selection Pins. Hardwire the FORMATx pins to the required values in pin control and SPI control mode. These pins set the number of DOUTx pins used to output ADC conversion data. The FORMATx pins are checked by the AD7768 on power-up; the AD7768 then remains in this data output configuration (see Table 31). |
| 57 | $\overline{\text{PIN}}$/SPI | DI | Pin Control/SPI Control. This pin sets the control method.<br>Logic 0 = pin control mode for the AD7768. Pin control mode allows a pin strapped configuration of the AD7768 by tying logic input pins to required logic levels. Tie the logic pins (MODE0 to MODE4, DEC0 and DEC1, and FILTER) as required for the configuration. See the Pin Control section for more details.<br>Logic 1 = SPI control mode for the AD7768. Use the SPI control interface signals ($\overline{\text{CS}}$, SCLK, SDI, and SDO) for reading and writing to the AD7768 memory map. |
| 58 | CLK_SEL | DI | Clock Select.<br>Logic 0 = pull this pin low for the CMOS clock option. The clock is applied to Pin 32 (Connect Pin 31 to DGND).<br>Logic 1 = pull this pin high for the crystal or LVDS clock option. The crystal or LVDS clock is applied to Pin 31 and Pin 32. The LVDS option is available only in SPI control mode. A write is required to enable the LVDS clock option. |
| 59 | VCM | AO | Common-Mode Voltage Output. This pin outputs (AVDD1 − AVSS)/2 V, which is 2.5 V by default in pin control mode. Configure this pin to (AVDD1 − AVSS)/2 V, 2.5 V, 2.14 V, or 1.65 V in SPI control mode. When driving capacitive loads larger than 0.1 µF, it is recommended to place a 50 Ω series resistor between the pin and the capacitive load for stability. The VCM voltage output is associated with the Channel 0 circuitry. If Channel 0 is put into standby mode, the VCM voltage output is also disabled for maximum power savings. Channel 0 must be enabled while VCM is being used externally to the AD7768. |
| 60 | AVDD2A | P | Analog Supply Voltage. This pin is 2 V to 5.5 V with respect to AVSS. |
| 61 | REGCAPA | AO | Analog LDO Regulator Output. Decouple this pin to AVSS with a 1 µF capacitor. |
| 62 | AVSS2A | P | Negative Analog Supply. This pin is nominally 0 V. |
| 63 | AIN0− | AI | Negative Analog Input to ADC Channel 0. |
| 64 | AIN0+ | AI | Positive Analog Input to ADC Channel 0. |

[1] AI is analog input, P is power, DI/O is digital input/output, DI is digital input, DO is digital output, and AO is analog output.