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8-Channel, 24-Bit, Simultaneous Sampling ADC

Data Sheet

AD7771

FEATURES

- 8-channel, 24-bit simultaneous sampling ADC
- Single-ended or true differential inputs
- PGA per channel (gains of 1, 2, 4, and 8)
- Low dc input current
  - ±4 nA (differential)/±8 nA (single-ended)
- Up to 128 kSPS ODR per channel
- Programmable ODRs and bandwidth
- SRC for coherent sampling
  - Sampling rate resolution up to 15.2 × 10^{-6} SPS
- Low latency sinc3 and sinc5 filter paths
- Adjustable phase synchronization
- Internal 2.5 V reference
- Two power modes
  - High resolution mode
  - Low power mode
- Optimizes power dissipation and performance
- Low resolution SAR ADC for system and chip diagnostics
- Power supply
  - Bipolar (±1.65 V) or unipolar (3.3 V) supplies
  - Digital I/O supply: 1.8 V to 3.6 V
  - Performance temperature range: −40°C to +105°C
  - Functional temperature range: −40°C to +125°C
- Performance
  - Combined ac and dc performance
  - 107 dB SNR/dynamic range at 32 kSPS in high resolution mode (sinc5)
  - −109 dB THD
  - ±8 ppm of FSR INL
  - ±15 µV offset error
  - ±0.1% FS gain error
  - ±10 ppm/°C typical temperature coefficient

APPLICATIONS

- Power quality and measurement applications
- General-purpose data acquisition
- Electroencephalography (EEG)
- Industrial process control

GENERAL DESCRIPTION

The AD7771[1] is an 8-channel, simultaneous sampling analog-to-digital converter (ADC). Eight full Σ-Δ ADCs are on-chip. The AD7771 provides an ultralow input current to allow direct sensor connection. Each input channel has a programmable gain stage allowing gains of 1, 2, 4, and 8 to map lower amplitude sensor outputs into the full-scale ADC input range, maximizing the dynamic range of the signal chain. The AD7771 accepts a V_{REF} voltage from 1 V up to 3.6 V. The analog inputs accept unipolar (0 V to V_{REF}) or true bipolar ($\pm V_{REF}/2$ V) analog input signals with 3.3 V or ±1.65 V analog supply voltages, respectively. The analog inputs can be configured to accept true differential or single-ended signals to match different sensor output configurations.

Each channel contains an ADC modulator and a sinc3/sinc5, low latency digital filter. A sample rate converter (SRC) is provided to allow fine resolution control over the AD7771 output data rate (ODR). This control can be used in applications where the ODR resolution is required to maintain coherency with 0.01 Hz changes in the line frequency. The SRC is programmable through the serial port interface (SPI). The AD7771 implements two different interfaces: a data output interface and SPI control interface. The ADC data output interface is dedicated to transmitting the ADC conversion results from the AD7771 to the processor. The SPI writes to and reads from the AD7771 configuration registers and for the control and reading of data from the successive approximation register (SAR) ADC. The SPI can also be configured to output the Σ-Δ conversion data.

The AD7771 includes a 12-bit SAR ADC. This ADC can be used for AD7771 diagnostics without having to decommission one of the Σ-Δ ADC channels dedicated to system measurement functions. With the use of an external multiplexer, which can be controlled through the three general-purpose input/output pins (GPIOs), and signal conditioning, the SAR ADC can validate the Σ-Δ ADC measurements in applications where functional safety is required. In addition, the AD7771 SAR ADC includes an internal multiplexer to sense internal nodes.

The AD7771 contains a 2.5 V reference and reference buffer. The reference has a typical temperature coefficient of ±10 ppm/°C.

The AD7771 offers two modes of operation: high resolution mode and low power mode. High resolution mode provides a higher dynamic range while consuming 16.6 mW per channel; low power mode consumes only 5.25 mW per channel at a reduced dynamic range specification.

The specified operating temperature range is −40°C to +105°C, although the device is operational up to +125°C.

Note that throughout this data sheet, certain terms are used to refer to either the multifunction pins or a range of pins. The multifunction pins, such as DCLK0/SDO, are referred to either by the entire pin name or by a single function of the pin, for example, DCLK0, when only that function is relevant. In the case of ranges of pins, AVSSx refers to the following pins: AVSS1A, AVSS1B, AVSS2A, AVSS2B, AVSS3, and AVSS4.

[1] This product is protected by at least U.S. Patent No. 9,432,043.

Rev. A

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6/2017—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

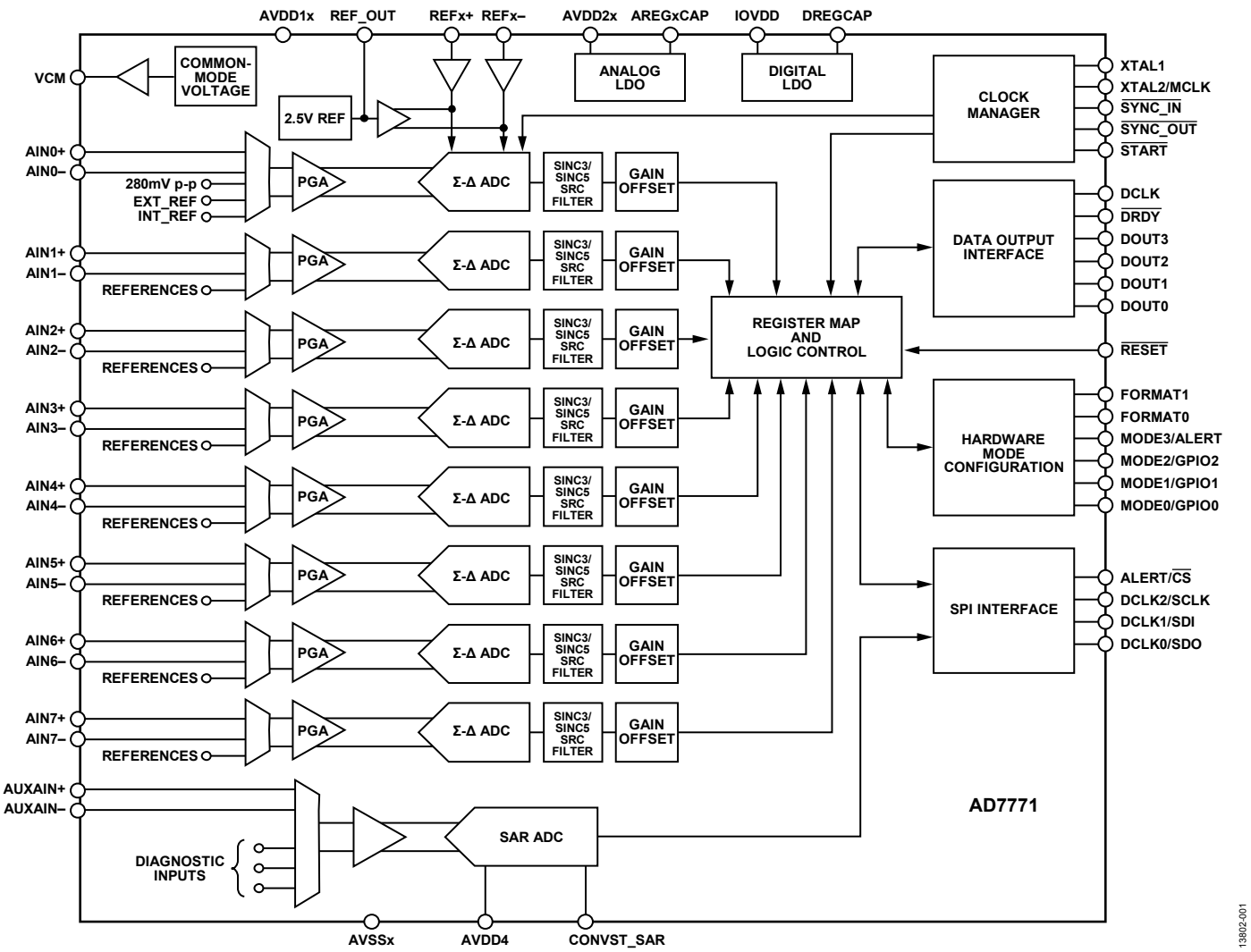

Figure 1.

SPECIFICATIONS

AVDD1x = 1.65 V, AVSSx[1] = −1.65 V (dual supply operation), AVDD1x = 3.3 V, AVSSx = analog ground (AGND) (single-supply operation), AVDD2x − AVSSx = 2.2 V to 3.6 V; IOVDD = 1.8 V to 3.6 V; DGND = 0 V, REFx+/REFx− = 2.5 V AVSSx (internal/external), master clock (MCLK) = 8192 kHz for high resolution mode and 4096 kHz for low power mode, ODR = 128 kSPS for high resolution mode and 32 kSPS for low power mode; all specifications at T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUTS					
Differential Input Voltage Range	V_{REF} = (REFx+ − REFx−)			$\pm V_{REF}/PGA_{GAIN}$	V
Single-Ended Input Voltage Range				0 to V_{REF}/PGA_{GAIN}	V
AINx± Common-Mode Input Range		AVSSx + 0.10	(AVDD1x + AVSSx)/2	AVDD1x − 0.10	V
Absolute AINx± Voltage Limits		AVSSx + 0.10		AVDD1x − 0.10	V
DC Input Current					
Differential	High resolution mode		±4		nA
	Low power mode		±1		nA
Single-Ended	High resolution mode		±8		nA
	Low power mode		±2		nA
Input Current Drift			50		pA/°C
AC Input Capacitance			8		pF
PROGRAMMABLE GAIN AMPLIFIER (PGA)					
Gain Settings (PGA_{GAIN})			1, 2, 4, or 8		
Bandwidth					
Small Signal	High resolution mode			2	MHz
	Low power mode			512	kHz
Large Signal	High resolution mode	See Figure 39, Figure 40, and Figure 44			
	Low power mode	See Figure 42, Figure 43, and Figure 47			
REFERENCE					
Internal					
Initial Accuracy	REF_OUT, T_A = 25°C	2.495	2.5	2.505	V
Temperature Coefficient			±10	±38	ppm/°C
Reference Load Current, I_L		−10		+10	mA
DC Power Supply Rejection	Line regulation		95		dB
Load Regulation, $\Delta V_{OUT}/\Delta I_L$			100		µV/mA
Voltage Noise, $e_{N\,p-p}$	0.1 Hz to 10 Hz		6.8		µV rms
Voltage Noise Density, e_N	1 kHz, 2.5 V reference		273.5		nV/√Hz
Turn On Settling Time	100 nF		1.5		ms
External					
Input Voltage	V_{REF} = (REFx+ − REFx−)	1	2.5	AVDD1x	V
Buffer Headroom		AVSSx + 0.1		AVDD1x − 0.1	V
REFx− Input Voltage			AVSSx	AVDD1x − REFx+	V
Average REFx± Input Current	Current per channel				
	Reference buffer disabled, high resolution mode		18		µA/V
	Reference buffer precharge mode (pre-Q), high resolution mode		600		nA/V
	Reference buffer disabled, low power mode		4.5		µA/V
	Reference buffer pre-Q, low power mode		100		nA/V
	Reference buffer enabled, high resolution mode		12		nA/V
	Reference buffer enabled, low power mode		5		nA/V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+105	°C
Functional[2]	T_{MIN} to T_{MAX}	−40		+125	°C
TEMPERATURE SENSOR					
Accuracy			±2		°C
DIGITAL FILTER RESPONSE					
Group Delay			See the SRC Group Delay section		
Settling Time			See the Settling Time section		
Pass Band	−0.1 dB		See the SRC Bandwidth section		
	−3 dB		See the SRC Bandwidth section		
Decimation Rate					
Sinc3		16		4095.99	
Sinc5		16		2048	
CLOCK SOURCE					
Frequency	High resolution mode	0.655		8.192	MHz
	Low power mode	1.3		4.096	MHz
Duty Cycle		45:55	50:50	55:45	%
Σ-Δ ADC					
Speed and Performance					
Resolution		24			Bits
ODR	High resolution mode			128	kSPS
	Low power mode			32	kSPS
No Missing Codes	Sinc3, up to 24 kSPS	24			Bits
	Sinc5	24			Bits
AC Accuracy					
Dynamic Range	Shorted inputs, PGA_{GAIN} = 1				
128 kSPS	High resolution mode (sinc5)		95		dB
32 kSPS	High resolution mode (sinc5)		107		dB
16 kSPS	High resolution mode (sinc3)		105.9		dB
4 kSPS	High resolution mode (sinc3)		116		dB
32 kSPS	Low power mode (sinc5)		94.5		dB
8 kSPS	Low power mode (sinc5)		106.5		dB
8 kSPS	Low power mode (sinc3)		95.8		dB
2 kSPS	Low power mode (sinc3)		111.8		dB
Total Harmonic Distortion (THD)	−0.5 dBFS, high resolution mode		−109		dB
	−0.5 dBFS, low power mode		−105		dB
Signal-to-Noise-and-Distortion Ratio (SINAD)	f_{IN} = 60 Hz		106		dB
Spurious-Free Dynamic Range (SFDR)	High resolution mode, 16 kSPS, PGA_{GAIN} = 1		132		dB
Intermodulation Distortion (IMD)	f_A = 50 Hz, f_B = 51 Hz, high resolution mode		−125		dB
	f_A = 50 Hz, f_B = 51 Hz, low power mode		−105		dB
DC Power Supply Rejection	AVDD1x = 3.3 V		−90		dB
DC Common-Mode Rejection Ratio		80			dB
Crosstalk			−120		dB
DC ACCURACY					
Integral Nonlinearity (INL)	Endpoint method				
High Resolution	PGA_{GAIN} = 1		±8	±15	ppm of FSR
	Other PGA gains		±4	±15	ppm of FSR

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Low Power	PGA_{GAIN} = 1		±9	±17	ppm of FSR
	Other PGA gains		±6	±15	ppm of FSR
Offset Error			±15	±90	µV
Offset Error Drift			0.25		µV/°C
	Over time		−2		µV/1000 hours
Offset Matching			25		µV
Gain Error			±0.1		% FS
Gain Error Drift vs. Temperature	PGA_{GAIN} = 1		±0.75		ppm/°C
Gain Matching			±0.1		%
SAR ADC					
Speed and Performance					
Resolution			12		Bits
Analog Input Range		AVSS4 + 0.1		AVDD4 − 0.1	V
Analog Input Common-Mode Range		AVSS4 + 0.1	(AVDD4 + AVSS4)/2	AVDD4 − 0.1	V
Analog Input Current			±100		nA
Throughput				256	kSPS
DC Accuracy	Differential mode				
INL			±1.5		LSB
Differential Nonlinearity (DNL)	No missing codes (12-bit)	−0.99		1	LSB
Offset			±1		LSB
Gain			12		LSB
AC Performance					
Signal-to-Noise Ratio (SNR)	1 kHz		66		dB
THD	1 kHz		−81		dB
VCM PIN					
Output (V_{CM})			(AVDD1x + AVSSx)/2		V
Load Current, I_L			1		mA
Load Regulation, $\Delta V_{OUT}/\Delta I_L$			12		mV/mA
Short-Circuit Current			5		mA
LOGIC INPUTS					
Input Voltage					
High, V_{IH}		0.7 × IOVDD			V
Low, V_{IL}				0.4	V
Hysteresis			0.1		V
Input Currents		−10		+10	µA
LOGIC OUTPUTS[3]					
Output Voltage					
High, V_{OH}	IOVDD ≥ 3 V, I_{SOURCE} = 1 mA	0.8 × IOVDD			V
	2.3 V ≤ IOVDD < 3 V, I_{SOURCE} = 500 µA	0.8 × IOVDD			V
	IOVDD < 2.3 V, I_{SOURCE} = 200 µA	0.8 × IOVDD			V
Low, V_{OL}	IOVDD ≥ 3 V, I_{SINK} = 2 mA			0.4	V
	2.3 V ≤ IOVDD < 3 V, I_{SINK} = 1 mA			0.4	V
	IOVDD < 2.3 V, I_{SINK} = 100 µA			0.4	V
Leakage Current	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF
Σ-Δ ADC Data Output Coding			Twos complement		
SAR ADC Data Output Coding			Binary		

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLIES	All Σ-Δ channels enabled				
AVDD1x – AVSSx		3.0		3.6	V
I_{AVDD1x}[4, 5]	Reference buffer pre-Q, VCM enabled, internal reference enabled				
	High resolution mode		18.3	23.7	mA
	Low power mode		5	6.4	mA
	Reference buffer enabled, VCM enabled, internal reference enabled				
	High resolution mode		20.5	26.7	mA
	Low power mode		5.5	7.1	mA
	Reference buffer disabled, VCM disabled, internal reference disabled				
	High resolution mode		14.3	18.8	mA
	Low power mode		3.9	5.1	mA
AVDD2x – AVSSx		2.2		3.6	V
I_{AVDD2x}	High resolution mode		9	9.45	mA
	Low power mode		3.5	3.7	mA
AVDD4 – AVSSx		3		3.6	V
I_{AVDD4}	SAR enabled		1.7	2	mA
	SAR disabled		1	10	µA
AVSSx – DGND		−1.8		0	V
IOVDD – DGND		1.8		3.6	V
I_{IOVDD}	High resolution mode (sinc5)		14.3	17	mA
	Low power mode (sinc5)		4.6	5.5	mA
	High resolution mode (sinc3)		12.2	14.2	mA
	Low power mode (sinc3)		2.2	4.9	mA
Power Dissipation[6]	Internal buffers bypassed, internal reference disabled, internal oscillator disabled, SAR disabled				
High Resolution Mode	128 kSPS		133	153	mW
Low Power Mode	32 kSPS		42	48.5	mW
Power-Down	All ADCs disabled		530		µW

[1] AVSSx refers to the following pins: AVSS1A, AVSS1B, AVSS2A, AVSS2B, AVDD3, and AVSS4. This term is used throughout the data sheet.
[2] At temperatures higher than 105°C, the device can be operated normally, though slight degradation on the maximum/minimum specifications is expected because these specifications are only guaranteed up to 105°C. See the Typical Performance Characteristics section for plots showing the typical performance of the device at high temperatures.
[3] The SDO pin and the DOUTx pin are configured in the default mode of strength.
[4] AVDD1x = 3.3 V, AVSSx = GND = ground, IOVDD = 1.8 V, CMOS clock.
[5] Disabling either the VCM pin or the internal reference results in a 40 µA typical current consumption reduction.
[6] Power dissipation is calculated using the maximum supply voltage, 3.6 V.

DOUTx TIMING CHARACTERISTISTICS

AVDD1x = 1.65 V, AVSSx[1] = −1.65 V (dual supply operation), AVDD1x = 3.3 V, AVSSx = AGND (single-supply operation), AVDD2 − AVSSx = 2.2 V to 3.6 V; IOVDD = 1.8 V to 3.6 V; DGND = 0 V, REFx+/REFx− = 2.5 V internal/external, MCLK = 8192 kHz; all specifications at T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Description[2]	Test Conditions/Comments	Min	Typ	Max	Unit
t_1	MCLK frequency	50:50	0.655		8.192	MHz
t_2	MCLK low time		60			ns
t_3	MCLK high time		60			ns
t_4	DCLK high time	MCLK/2	121			ns
t_5	DCLK low time	MCLK/2	121			ns
t_6	MCLK falling edge to DCLK rising edge				45	ns
t_7	MCLK falling edge to DCLK falling edge				45	ns
t_8	DCLK rising edge to $\overline{DRDY}$ rising edge		2			ns
t_9	DCLK rising edge to $\overline{DRDY}$ falling edge		1			ns
t_{10}	DOUTx setup time		20			ns
t_{11}	DOUTx hold time		20			ns

[1] AVSSx refers to the following pins: AVSS1A, AVSS1B, AVSS2A, AVSS2B, AVSS3, and AVSS4. This term is used throughout the data sheet.
[2] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

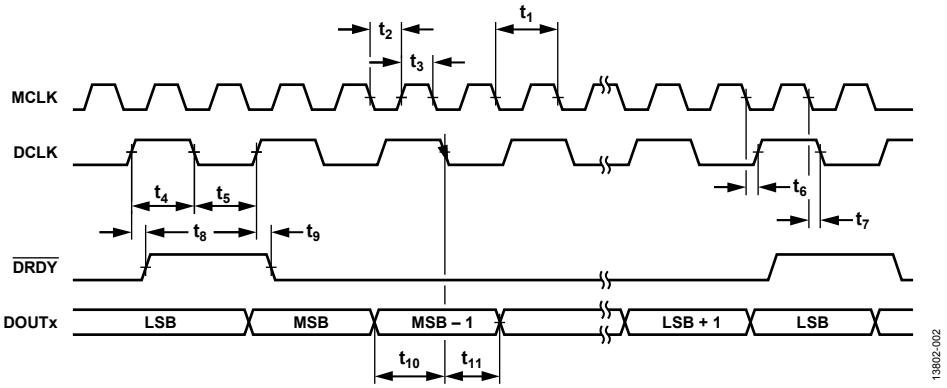

Figure 2. Data Interface Timing Diagram

SPI TIMING CHARACTERISTISTICS

AVDD1x = 1.65 V, AVSSx[1] = −1.65 V (dual supply operation), AVDD1x = 3.3 V, AVSSx = AGND, AVDD2 − AVSSx = 2.2 V to 3.6 V; IOVDD = 1.8 V to 3.6 V; DGND = 0 V, REFx+/REFx− = 2.5 V (internal/external), MCLK = 8192 kHz; all specifications at T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Description[2]	Test Conditions/Comments	Min	Typ	Max	Unit
t_{12}	SCLK period	50:50			30	MHz
t_{13}	SCLK low time		7			ns
t_{14}	SCLK high time		7			ns
t_{15}	SCLK rising edge to $\overline{CS}$ falling edge		10			ns
t_{16}	$\overline{CS}$ falling edge to SCLK rising edge		10			ns
t_{17}	SCLK rising edge to $\overline{CS}$ rising edge		10			ns
t_{18}	$\overline{CS}$ rising edge to SCLK rising edge		10			ns
t_{19}	Minimum $\overline{CS}$ high time		10			ns
t_{20}	SDI setup time		5			ns
t_{21}	SDI hold time		5			ns
t_{22A}	$\overline{CS}$ falling edge to SDO enable (SPI = Mode 0)		30			ns
t_{22B}	SCLK falling edge to SDO enable (SPI = Mode 3)		49			ns
t_{23}	SDO setup time		10			ns
t_{24}	SDO hold time		10			ns
t_{25}	$\overline{CS}$ rising edge to SDO disable		30			ns

[1] AVSSx refers to the following pins: AVSS1A, AVSS1B, AVSS2A, AVSS2B, AVSS3, and AVSS4. This term is used throughout the data sheet.
[2] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

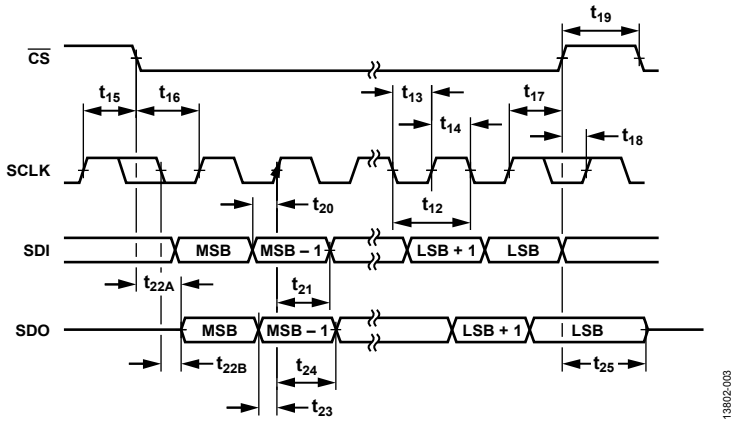

Figure 3. SPI Control Interface Timing Diagram

SYNCHRONIZATION PINS AND RESET TIMING CHARACTERISTICS

AVDD1x = 1.65 V, AVSSx[1] = −1.65 V (dual supply operation), AVDD1x = 3.3 V, AVSSx = AGND, AVDD2 − AVSSx = 2.2 V to 3.6 V; IOVDD = 1.8 V to 3.6 V; DGND = 0 V, REFx+/REFx− = 2.5 V (internal/external), MCLK = 8192 kHz; all specifications at T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Description[2]	Test Conditions/Comments	Min	Typ	Max	Unit
t_{26}	$\overline{\text{START}}$ setup time		10			ns
t_{27}	$\overline{\text{START}}$ hold time		MCLK			ns
t_{28}	MCLK falling edge to $\overline{\text{SYNC\_OUT}}$ falling edge		MCLK			ns
t_{29}	$\overline{\text{SYNC\_IN}}$ setup time		10			ns
t_{30}	$\overline{\text{SYNC\_IN}}$ hold time		MCLK			ns
$t_{INIT\_\overline{SYNC\_IN}}$	$\overline{\text{SYNC\_IN}}$ rising edge to first $\overline{\text{DRDY}}$	16 kSPS, high resolution mode	145			µs
$t_{INIT\_\overline{RESET}}$	$\overline{\text{RESET}}$ rising edge to first $\overline{\text{DRDY}}$	16 kSPS, high resolution mode	225			µs
t_{31}	$\overline{\text{RESET}}$ hold time		2 × MCLK			ns
t_{POWER_UP}	Start time	t_{POWER_UP} is not shown in Figure 4		2		ms

[1] AVSSx refers to the following pins: AVSS1A, AVSS1B, AVSS2A, AVSS2B, AVSS3, and AVSS4. This term is used throughout the data sheet.
[2] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

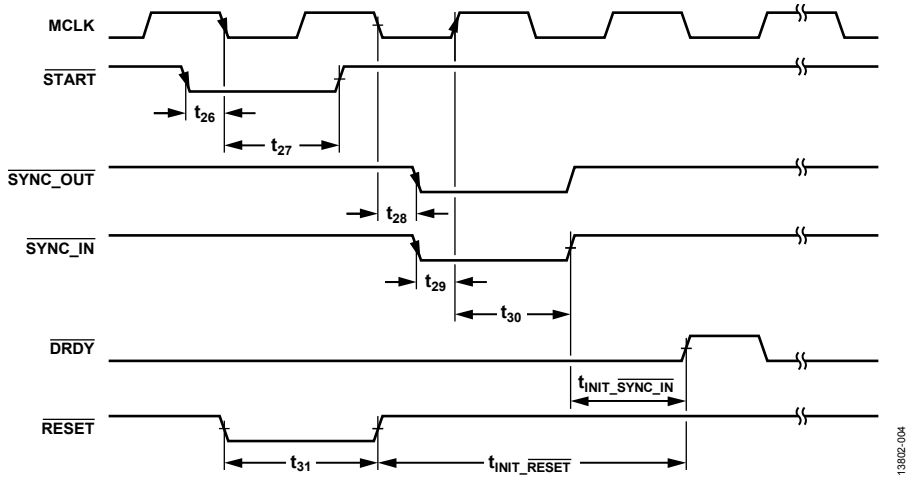

Figure 4. Synchronization Pins and Reset Control Interface Timing Diagram

SAR ADC TIMING CHARACTERISTICS

AVDD1x = 1.65 V, AVSSx[1] = −1.65 V (dual supply operation), AVDD1x = 3.3 V, AVSSx = AGND, AVDD2 − AVSSx = 2.2 V to 3.6 V; IOVDD = 1.8 V to 3.6 V; DGND = 0 V, REFx+/REFx− = 2.5 V (internal/external), MCLK = 8192 kHz; all specifications at T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter	Description[2]	Min	Typ	Max	Unit
t_{32}	Conversion time	1		3.4	µs
t_{33}	Acquisition time[3]	500			ns
t_{34}	Delay time	50			ns
t_{35}	Throughput data rate			256	kSPS

[1] AVSSx refers to the following pins: AVSS1A, AVSS1B, AVSS2A, AVSS2B, AVSS3 and AVSS4. This term is used throughout the data sheet.
[2] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[3] Direct mode enabled. If deglitch mode is enabled, add 1.5/MCLK as described in Table 30.

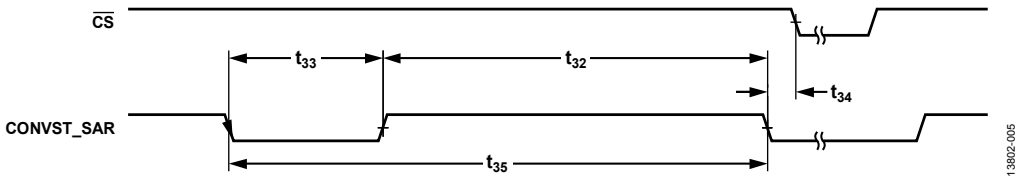

Figure 5. SAR ADC Timing Diagram

GPIO SRC UPDATE TIMING CHARACTERISTICS

AVDD1x = 1.65 V, AVSSx[1] = −1.65 V (dual supply operation), AVDD1x = 3.3 V, AVSSx = AGND, AVDD2 − AVSSx = 2.2 V to 3.6 V; IOVDD = 1.8 V to 3.6 V; DGND = 0 V, REFx+/REFx− = 2.5 V (internal/external), MCLK = 8192 kHz; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 6.

Parameter	Description[2]	Min	Typ	Max	Unit
t_{36}	GPIO2 setup time	10			ns
t_{37}	GPIO2 hold time—high resolution mode	MCLK			ns
	GPIO2 hold time—low power mode	2 × MCLK			ns
t_{38}	MCLK rising edge to GPIO1 rising edge time	20			ns
t_{39}	GPIO0 setup time	5			ns
t_{40}	GPIO0 hold time	MCLK			ns

[1] AVSSx refers to the following pins: AVSS1A, AVSS1B, AVSS2A, AVSS2B, AVSS3 and AVSS4. This term is used throughout the data sheet.
[2] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

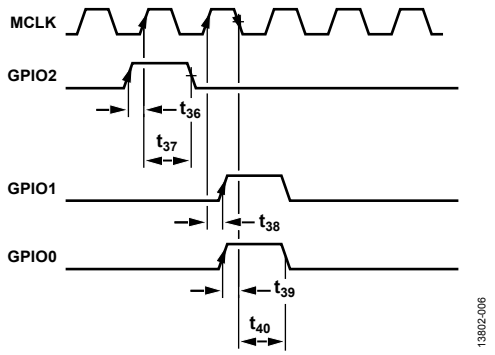

Figure 6. GPIOs for SRC Update Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Any Supply Pin to AVSSx	−0.3 V to +3.96 V
AVSSx to DGND	−1.98 V to +0.3 V
AREGxCAP to AVSSx	−0.3 V to +1.98 V
DREGCAP to DGND	−0.3 V to +1.98 V
IOVDD to DGND	−0.3 V to +3.96 V
IOVDD to AVSSx	−0.3 V to +5.94 V
AVDD4 to AVSSx	−0.3 V to +3.96 V
Analog Input Voltage	AVSSx − 0.3 V to AVDD1x + 0.3 V or 3.96 V (whichever is less)
REFx± Input Voltage	AVSSx − 0.3 V to AVDD1x + 0.3 V or 3.96 V (whichever is less)
AUXAIN±	AVSSx − 0.3 V to AVDD4 + 0.3 V or 3.96 V (whichever is less)
Digital Input Voltage to DGND	DGND − 0.3 V to IOVDD + 0.3 V or 3.96 V (whichever is less)
Digital Output Voltage to DGND	DGND − 0.3 V to IOVDD + 0.3 V or 3.96 V (whichever is less)
XTAL1 to DGND	DGND − 0.3 V to DREGCAP + 0.3 V or 1.98 V (whichever is less)
AINx±, AUXAIN±, and Digital Input Current	±10 mA
Operating Temperature Range	−40°C to +125°C
Junction Temperature, T_J Maximum	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	260°C
ESD	2 kV
Field Induced Charged Device Model (FICDM)	500 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
CP-64-15[1]					
No Thermal Vias	30.43	N/A[2]	0.13	6.59	°C/W
49 Thermal Vias	22.62	3.17	0.09	3.19	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD51.
[2] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

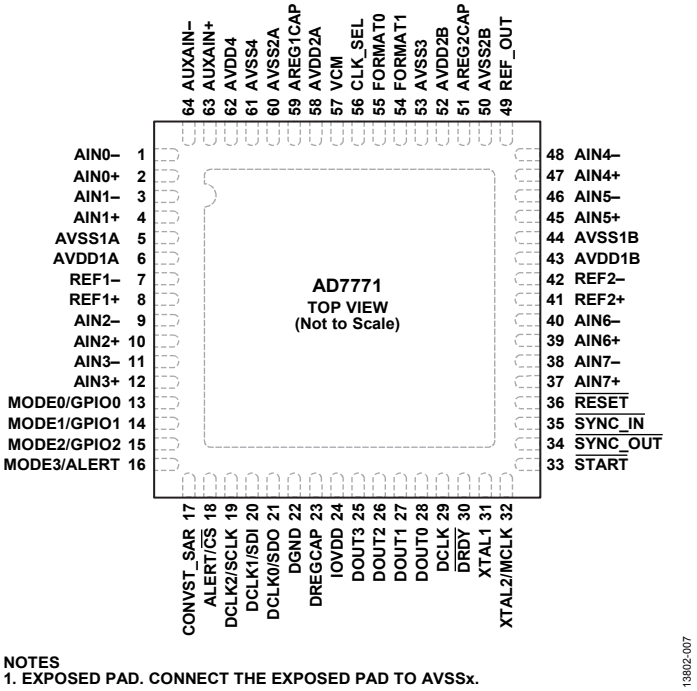

Figure 7. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Type	Direction	Description
1	AIN0−	Analog input	Input	Analog Input Channel 0, Negative.
2	AIN0+	Analog input	Input	Analog Input Channel 0, Positive.
3	AIN1−	Analog input	Input	Analog Input Channel 1, Negative.
4	AIN1+	Analog input	Input	Analog Input Channel 1, Positive.
5	AVSS1A	Supply	Supply	Negative Front-End Analog Supply for Channel 0 to Channel 3, Typical at −1.65 V (Dual Supply) and AGND (Single Supply). Connect all the AVSSx pins to the same potential.
6	AVDD1A	Supply	Supply	Positive Front-End Analog Supply for Channel 0 to Channel 3, Typical at AVSSx + 3.3 V. Connect this pin to AVDD1B.
7	REF1−	Reference	Input	Negative Reference Input 1 for Channel 0 to Channel 3, Typical at AVSSx. Connect all the REFx− pins to the same potential.
8	REF1+	Reference	Input	Positive Reference Input 1 for Channel 0 to Channel 3, Typical at REF1− + 2.5 V.
9	AIN2−	Analog input	Input	Analog Input Channel 2, Negative.
10	AIN2+	Analog input	Input	Analog Input Channel 2, Positive.
11	AIN3−	Analog input	Input	Analog Input Channel 3, Negative.
12	AIN3+	Analog input	Input	Analog Input Channel 3, Positive.
13	MODE0/GPIO0	Digital I/O	I/O	Mode 0 Input in Pin Control Mode (MODE0). See Table 14 for more details. Configurable General-Purpose Input/Output 0 in SPI Control Mode (GPIO0). If not in use, connect this pin to DGND or IOVDD.
14	MODE1/GPIO1	Digital I/O	I/O	Mode 1 Input in Pin Control Mode (MODE1). See Table 14 for more details. Configurable General-Purpose Input/Output 1 in SPI Control Mode (GPIO1). If not in use, connect this pin to DGND or IOVDD.
15	MODE2/GPIO2	Digital I/O	I/O	Mode 2 Input in Pin Control Mode (MODE2). See Table 14 for more details. Configurable General-Purpose Input/Output 2 in SPI Control Mode (GPIO2). If not in use, connect this pin to DGND or IOVDD.
16	MODE3/ALERT	Digital I/O	I/O	Mode 3 Input in Pin Control Mode (MODE3). See Table 14 for more details. Alert Output in SPI Control Mode (ALERT).

Pin No.	Mnemonic	Type	Direction	Description
17	CONVST_SAR	Digital input	Input	Σ-Δ Output Interface Selection Pin in Pin Control Mode. See Table 13 for more details. This pin also functions as the start for the SAR conversion in SPI control mode.
18	ALERT/$\overline{CS}$	Digital input	Input	Alert Output in Pin Control Mode (ALERT). Chip Select in SPI Control Mode ($\overline{CS}$).
19	DCLK2/SCLK	Digital input	Input	Data Clock Frequency Selection Pin 2 in Pin Control Mode (DCLK2). See Table 15 for more details. SPI Clock in SPI Control Mode (SCLK).
20	DCLK1/SDI	Digital input	Input	Data Clock Frequency Selection Pin 1 in Pin Control Mode (DCLK1). See Table 15 for more details. SPI Data Input in SPI Control Mode (SDI). Connect this pin to DGND if the device is configured in pin control mode with the SPI as the data output interface.
21	DCLK0/SDO	Digital output	Output	Data Clock Frequency Selection Pin 0 in Pin Control Mode (DCLK0). See Table 15 for more details. SPI Data Output in SPI Control Mode (SDO).
22	DGND	Supply	Supply	Digital Ground.
23	DREGCAP	Supply	Output	Digital Low Dropout (LDO) Output. Decouple this pin to DGND with a 1 µF capacitor.
24	IOVDD	Supply	Supply	Digital Levels Input/Output and Digital LDO (DLDO) Supply from 1.8 V to 3.6 V. IOVDD must not be lower than DREGCAP.
25	DOUT3	Digital output	I/O	Data Output Pin 3. If the device is configured in daisy-chain mode, this pin acts as an input pin. See the Daisy-Chain Mode section for more details.
26	DOUT2	Digital output	I/O	Data Output Pin 2. If the device is configured in daisy-chain mode, this pin acts as an input pin. See the Daisy-Chain Mode section for more details.
27	DOUT1	Digital output	Output	Data Output Pin 1.
28	DOUT0	Digital output	Output	Data Output Pin 0.
29	DCLK	Digital output	Output	Data Output Clock.
30	$\overline{DRDY}$	Digital output	Output	Data Output Ready Pin.
31	XTAL1	Clock	Input	Crystal 1 Input Connection. If CMOS is used as a clock source, tie this pin to DGND. See Table 12 for more details.
32	XTAL2/MCLK	Clock	Input	Crystal 2 Input Connection (XTAL2). See Table 12 for more details. CMOS Clock (MCLK). See Table 12 for more details.
33	$\overline{START}$	Digital input	Input	Synchronization Pulse. This pin internally synchronizes an external $\overline{START}$ asynchronous pulse with MCLK. The synchronize signal is shifted out by the $\overline{SYNC\_OUT}$ pin. If not in use, tie this pin to DGND. See the Phase Adjustment section and the Digital Reset and Synchronization Pins section for more details.
34	$\overline{SYNC\_OUT}$	Digital output	Input	Synchronization Signal. This pin generates a synchronous pulse generated and driven by hardware (via the $\overline{START}$ pin) or by software (GENERAL_USER_CONFIG_2, Bit 0). If this pin is in use, it must be wired to the $\overline{SYNC\_IN}$ pin. See the Phase Adjustment section and the Digital Reset and Synchronization Pins section for more details.
35	$\overline{SYNC\_IN}$	Digital input	Input	Reset for the Internal Digital Block and Synchronize for Multiple Devices. See the Digital Reset and Synchronization Pins section for more details.
36	$\overline{RESET}$	Digital input	Input	Asynchronous Reset Pin. This pin resets all registers to their default value. It is recommended to generate a pulse on this pin after the device is powered up because a slow slew rate in the supplies may generate an incorrect initialization in the digital block.
37	AIN7+	Analog input	Input	Analog Input Channel 7, Positive.
38	AIN7−	Analog input	Input	Analog Input Channel 7, Negative.
39	AIN6+	Analog input	Input	Analog Input Channel 6, Positive.
40	AIN6−	Analog input	Input	Analog Input Channel 6, Negative.
41	REF2+	Reference	Input	Positive Reference Input 2 for Channel 4 to Channel 7, Typical at REF2− + 2.5 V.
42	REF2−	Reference	Input	Negative Reference Input 2 for Channel 4 to Channel 7, Typical at AVSSx. Connect all the REFx− pins to the same potential.
43	AVDD1B	Supply	Supply	Positive Front-End Analog Supply for Channel 4 to Channel 7. Connect this pin to AVDD1A.

Pin No.	Mnemonic	Type	Direction	Description
44	AVSS1B	Supply	Supply	Negative Front-End Analog Supply for Channel 4 to Channel 7, Typical at −1.65 V (Dual Supply) or AGND (Single Supply). Connect all the AVSSx pins to the same potential.
45	AIN5+	Analog input	Input	Analog Input Channel 5, Positive.
46	AIN5−	Analog input	Input	Analog Input Channel 5, Negative.
47	AIN4+	Analog input	Input	Analog Input Channel 4, Positive.
48	AIN4−	Analog input	Input	Analog Input Channel 4, Negative.
49	REF_OUT	Reference	Output	2.5 V Reference Output. Connect a 100 nF capacitor on this pin if using the internal reference.
50	AVSS2B	Supply	Supply	Negative Analog Supply. Connect all the AVSSx pins together.
51	AREG2CAP	Supply	Output	Analog LDO Output 2. Decouple this pin to AVSS2B with a 1 µF capacitor.
52	AVDD2B	Supply	Supply	Positive Analog Supply. Connect this pin to AVDD2A.
53	AVSS3	Supply	Supply	Negative Analog Ground. Connect all the AVSSx to the same potential.
54	FORMAT1	Digital input	Input	Output Data Frame 1. See Table 13 for more details.
55	FORMAT0	Digital input	Input	Output Data Frame 0. See Table 13 for more details.
56	CLK_SEL	Digital input	Input	Select Clock Source. See Table 12 for more details.
57	VCM	Analog output	Output	Common-Mode Voltage Output, Typical at (AVDD1x + AVSSx)/2.
58	AVDD2A	Supply	Input	Analog Supply from 2.2 V to 3.6 V. AVSS2x must not be lower than AREGxCAP. Connect this pin to AVDD2B.
59	AREG1CAP	Supply	Output	Analog LDO Output 1. Decouple this pin to AVSSx with a 1 µF capacitor.
60	AVSS2A	Supply	Input	Negative Analog supply. Connect all the AVSSx pins to the same potential.
61	AVSS4	Supply	Supply	Negative SAR Analog Supply and Reference. Connect all AVSSx pins to the same potential.
62	AVDD4	Supply	Supply	Positive SAR Analog Supply and Reference Source.
63	AUXAIN+	Analog input	Input	Positive SAR Analog Input Channel.
64	AUXAIN−	Analog input	Input	Negative SAR Analog Input Channel.
	EPAD	Supply	Input	Exposed Pad. Connect the exposed pad to AVSSx.

TYPICAL PERFORMANCE CHARACTERISTICS

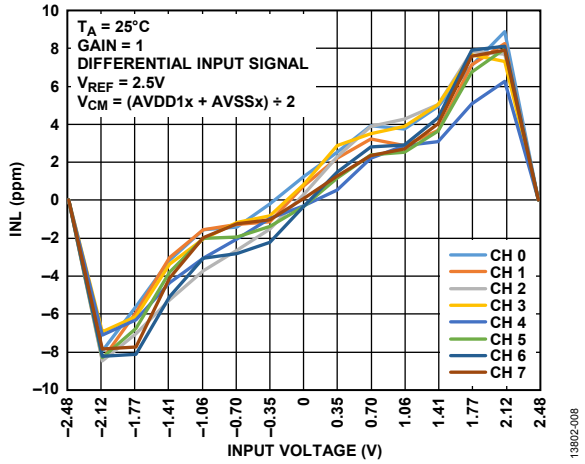

Figure 8. INL vs. Input Voltage and Channel at 64 kSPS, High Resolution Mode

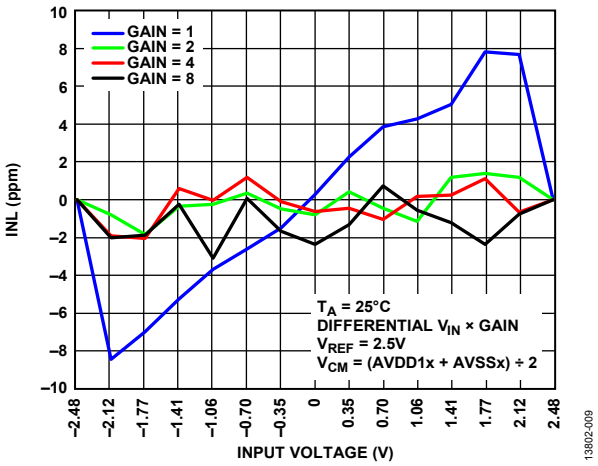

Figure 9. INL vs. Input Voltage and PGA Gain at 64 kSPS, High Resolution Mode

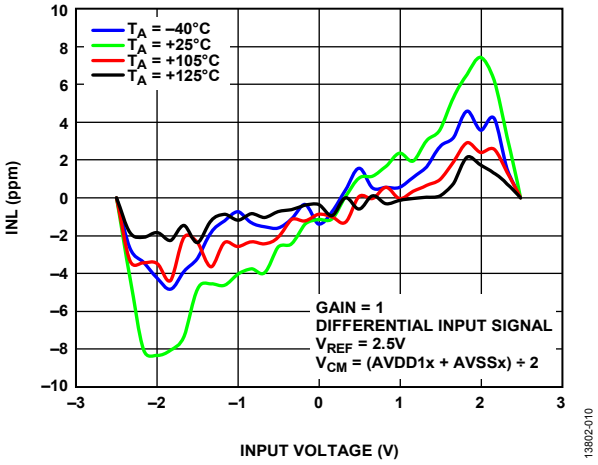

Figure 10. INL vs. Input Voltage and Temperature at 64 kSPS, High Resolution Mode

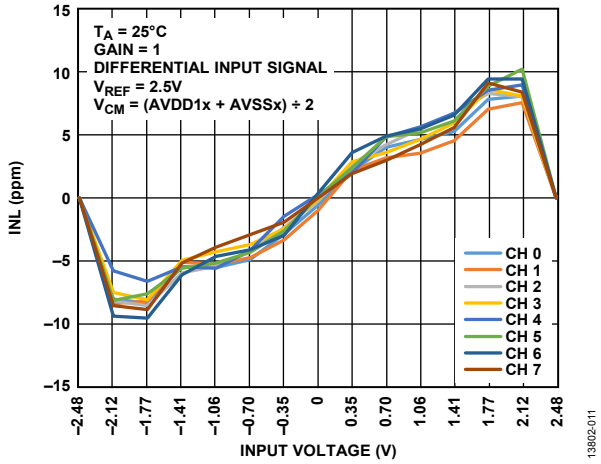

Figure 11. INL vs. Input Voltage and Channel at 16 kSPS, Low Power Mode

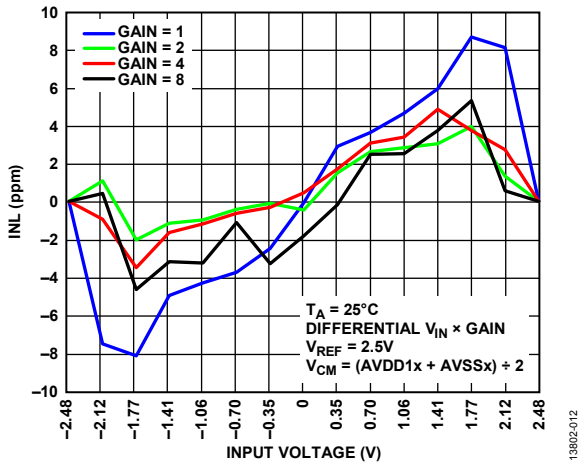

Figure 12. INL vs. Input Voltage and PGA Gain at 16 kSPS, Low Power Mode

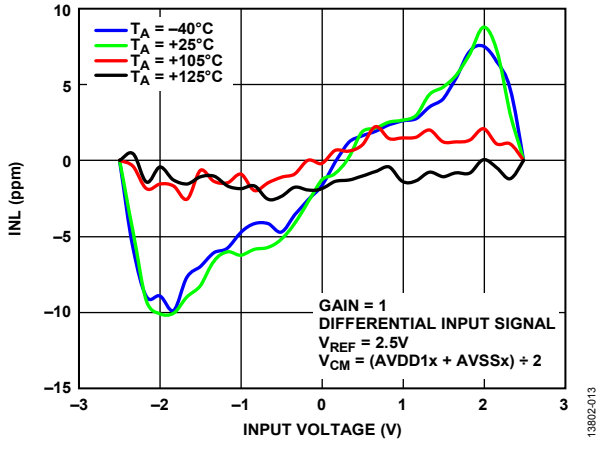

Figure 13. INL vs. Input Voltage and Temperature at 16 kSPS, Low Power Mode

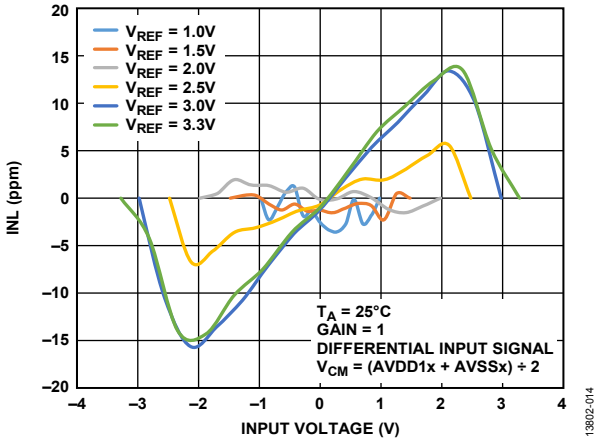

Figure 14. INL vs. Input Voltage and Reference Voltage (V_{REF}) at 64 kSPS, High Resolution Mode

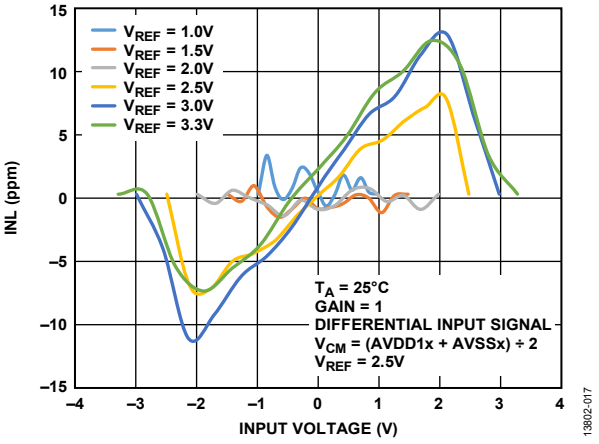

Figure 17. INL vs. Input Voltage and Reference Voltage (V_{REF}) at 16 kSPS, Low Power Mode

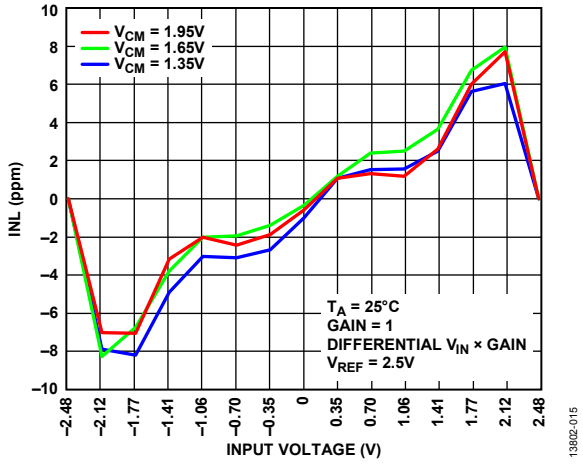

Figure 15. INL vs. Input Voltage and V_{CM} at 64 kSPS, High Resolution Mode

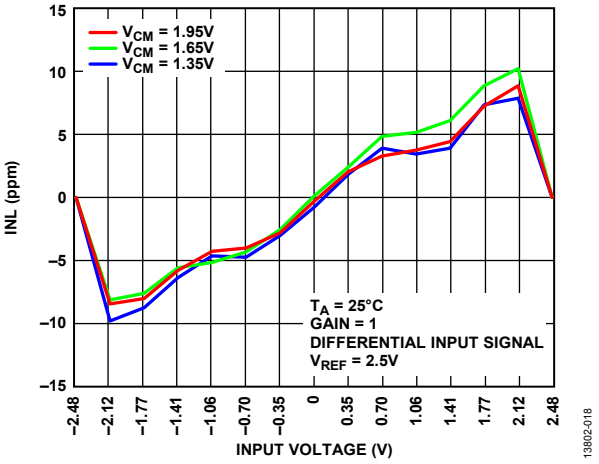

Figure 18. INL vs. Input Voltage and V_{CM} at 16 kSPS, Low Power Mode

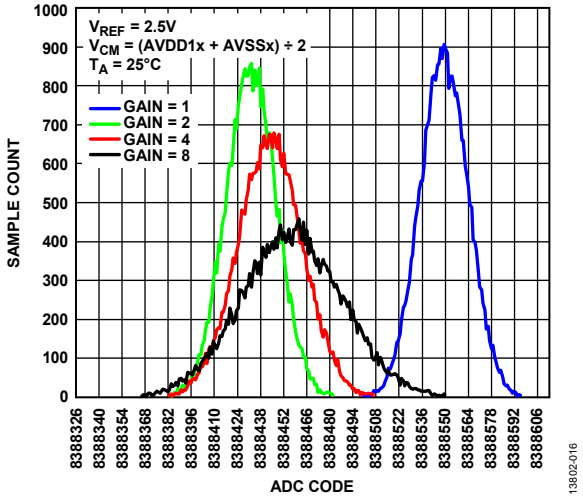

Figure 16. Noise Histogram at 16 kSPS, High Resolution Mode, Sinc3 Filter Enabled

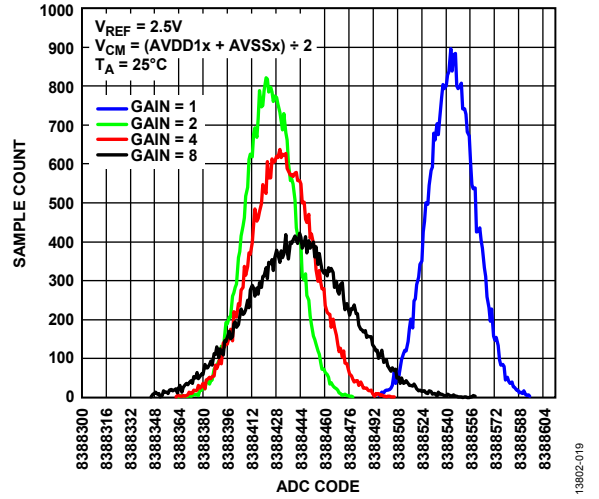

Figure 19. Noise Histogram at 4 kSPS, Low Power Mode, Sinc3 Filter Enabled

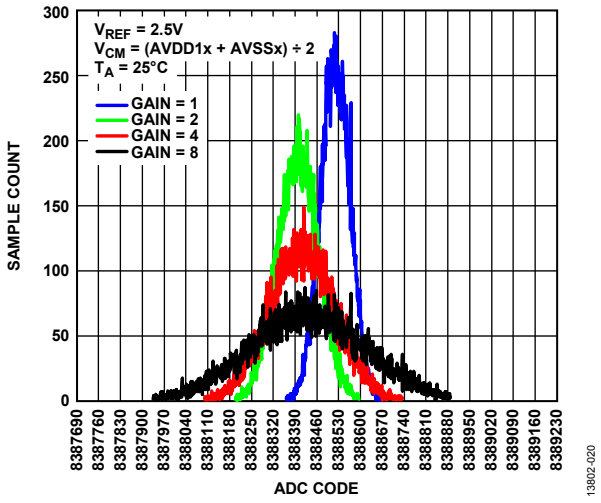

Figure 20. Noise Histogram at 64 kSPS, High Resolution Mode, Sinc5 Filter Enabled

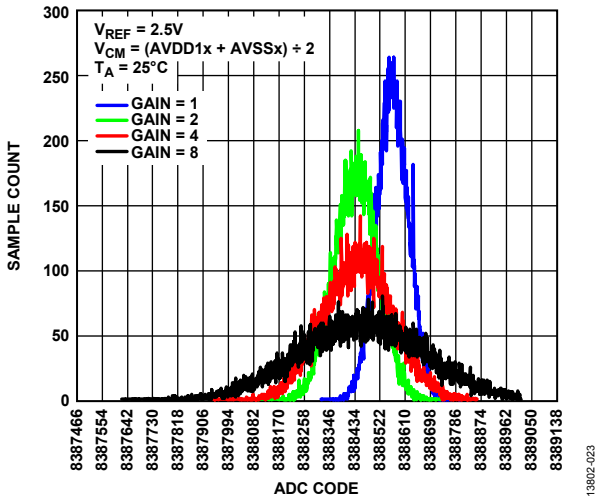

Figure 23. Noise Histogram at 16 kSPS, Low Power Mode, Sinc5 Filter Enabled

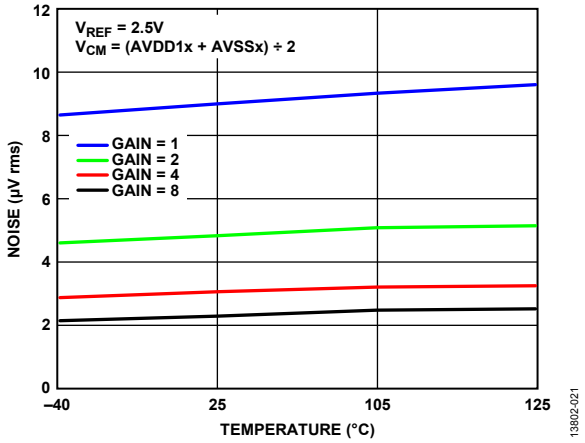

Figure 21. Noise vs. Temperature at 16 kSPS, High Resolution Mode, Sinc3 Filter Enabled

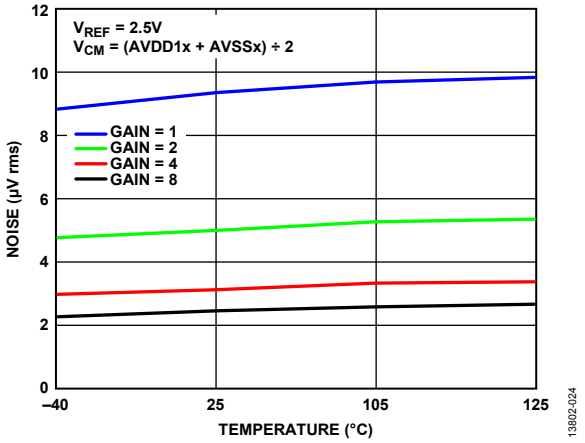

Figure 24. Noise vs. Temperature at 4 kSPS, Low Power Mode, Sinc3 Filter Enabled

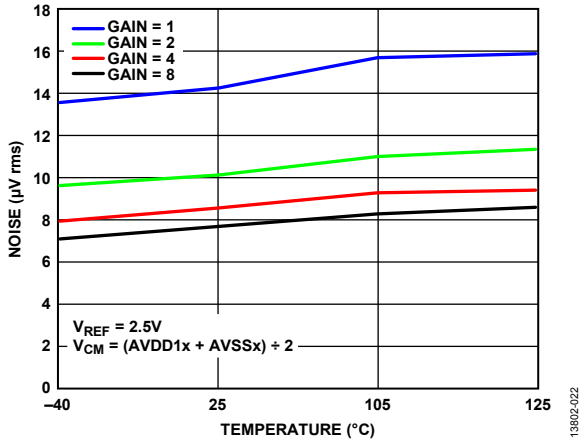

Figure 22. Noise vs. Temperature at 64 kSPS, High Resolution Mode, Sinc5 Filter Enabled

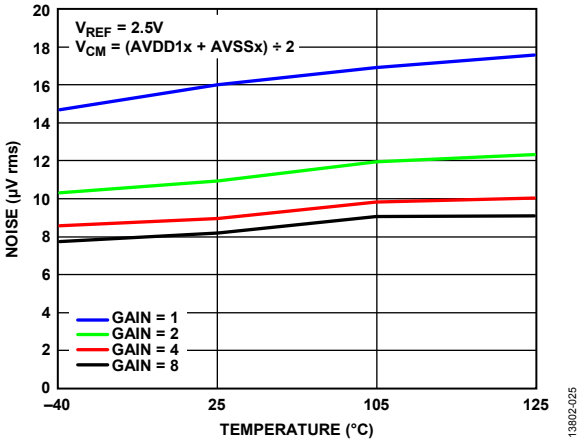

Figure 25. Noise vs. Temperature at 16 kSPS, Low Power Mode, Sinc5 Filter Enabled

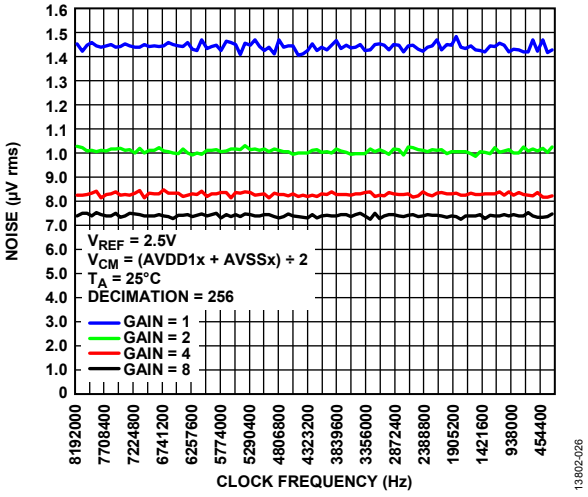

Figure 26. Noise vs. Clock Frequency, High Resolution Mode

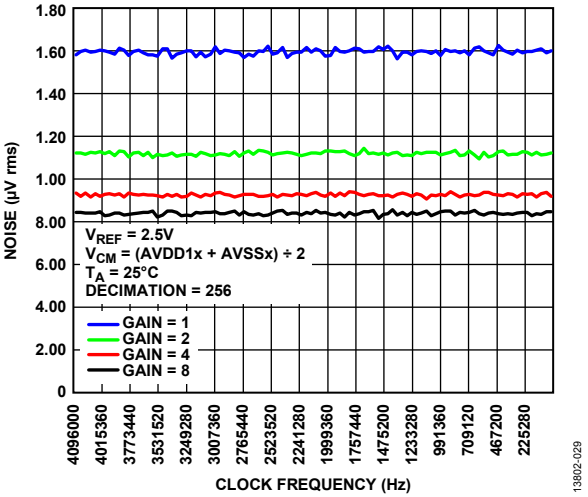

Figure 29. Noise vs. Clock Frequency, Low Power Mode

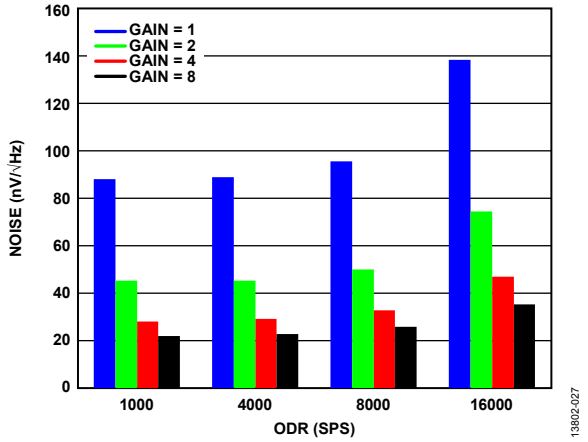

Figure 27. Noise vs. ODR, High Resolution Mode, Sinc3 Filter Enabled

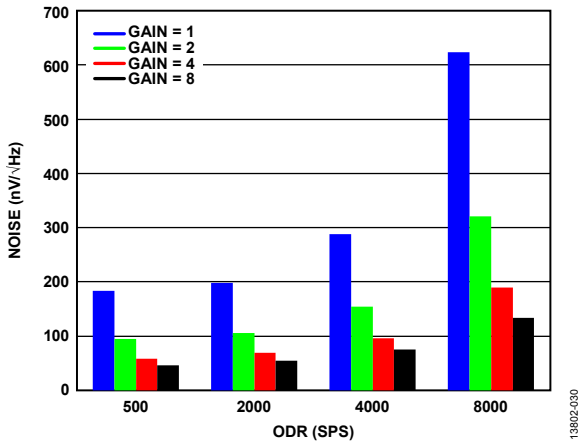

Figure 30. Noise vs. ODR, Low Power Mode, Sinc3 Filter Enabled

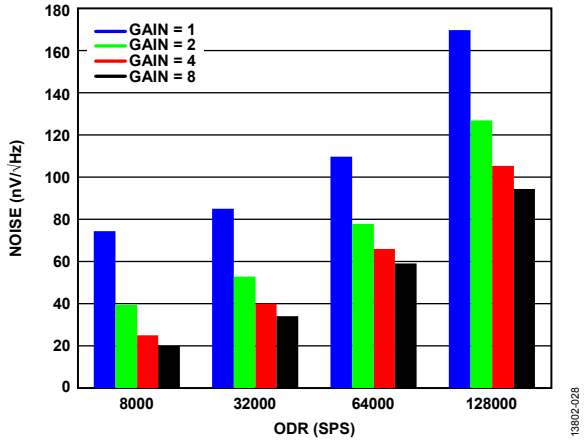

Figure 28. Noise vs. ODR, High Resolution Mode, Sinc5 Filter Enabled

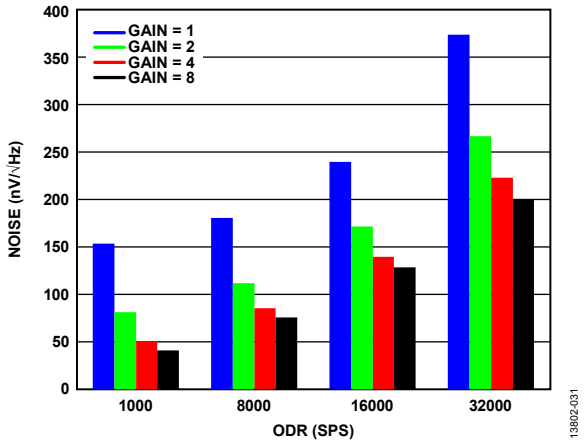

Figure 31. Noise vs. ODR, Low Power Mode, Sinc5 Filter Enabled

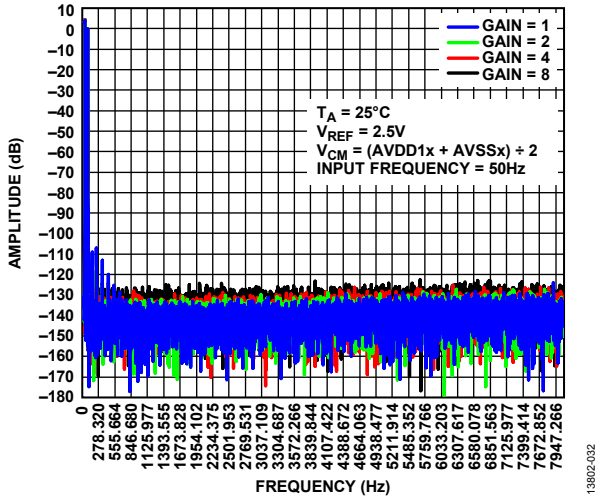

Figure 32. FFT Plot, High Resolution Mode at 16 kSPS, Input Frequency (f_{IN}) = 50 Hz, Sinc3 Filter Enabled

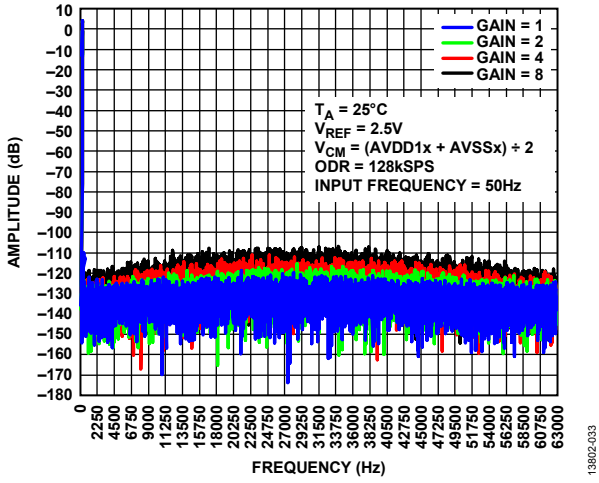

Figure 33. FFT Plot, High Resolution Mode at 128 kSPS, Input Frequency (f_{IN}) = 50 Hz, Sinc5 Filter Enabled

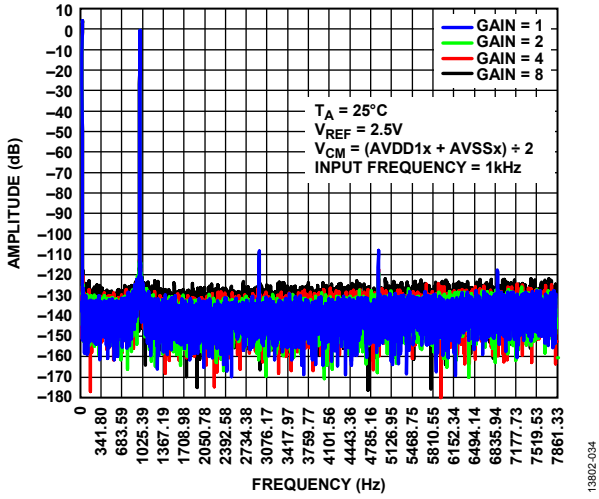

Figure 34. FFT Plot, High Resolution Mode at 16 kSPS, Input Frequency (f_{IN}) = 1 kHz, Sinc3 Filter Enabled

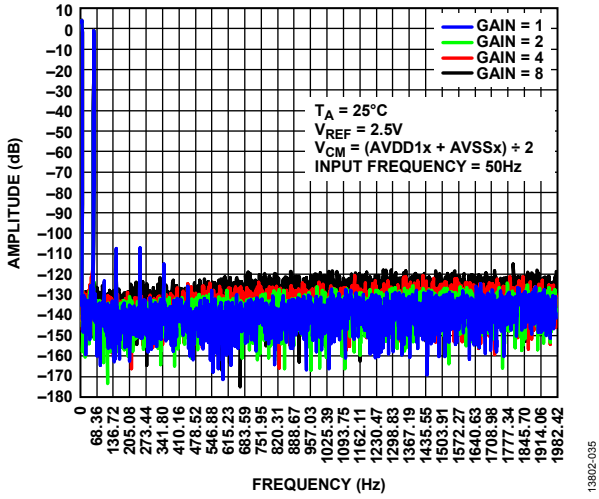

Figure 35. FFT Plot, Low Power Mode at 4 kSPS, Input Frequency (f_{IN}) = 50 Hz, Sinc3 Filter Enabled

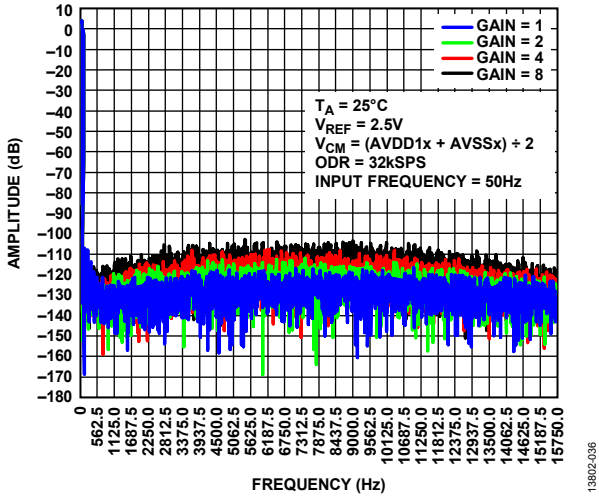

Figure 36. FFT Plot, Low Power Mode at 32 kSPS, Input Frequency (f_{IN}) = 50 Hz, Sinc5 Filter Enabled

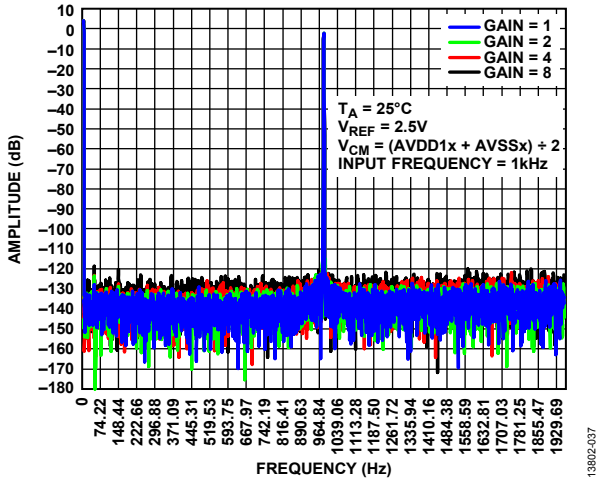

Figure 37. FFT Plot, Low Power Mode at 4 kSPS, Input Frequency (f_{IN}) = 1 kHz, Sinc3 Filter Enabled

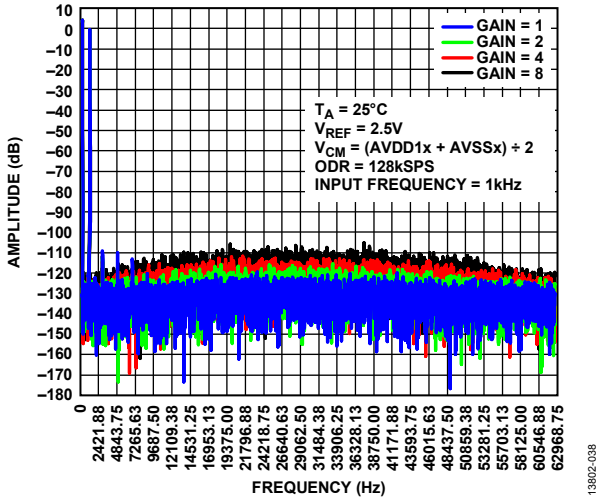

Figure 38. FFT Plot, High Resolution Mode at 128 kSPS, Input Frequency (f_{IN}) = 1 kHz, Sinc5 Filter Enabled

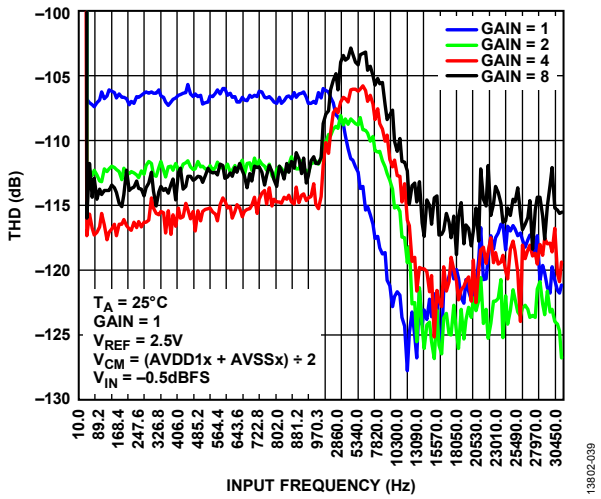

Figure 39. THD vs. Input Frequency at 64 kSPS, High Resolution Mode, Sinc5 Filter Enabled

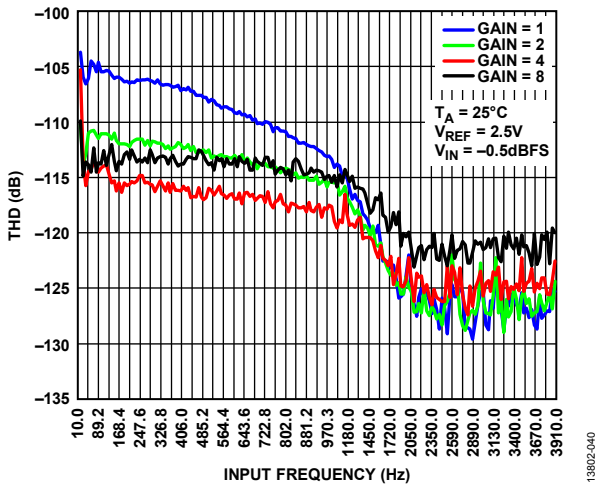

Figure 40. THD vs. Input Frequency at 16 kSPS, High Resolution Mode, Sinc3 Filter Enabled

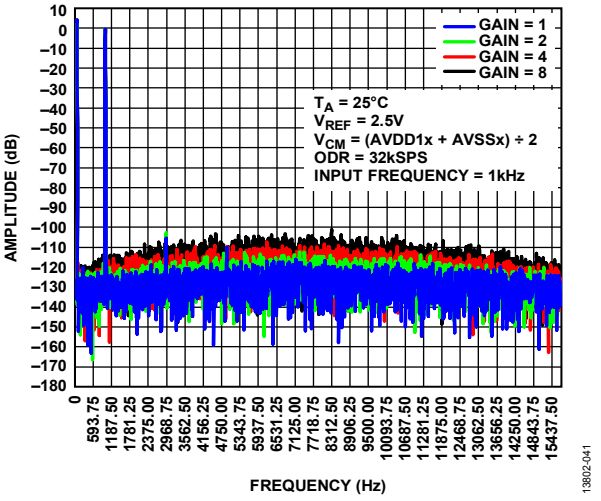

Figure 41. FFT Plot, Low Power Mode at 32 kSPS, Input Frequency (f_{IN}) = 1 kHz, Sinc5 Filter Enabled

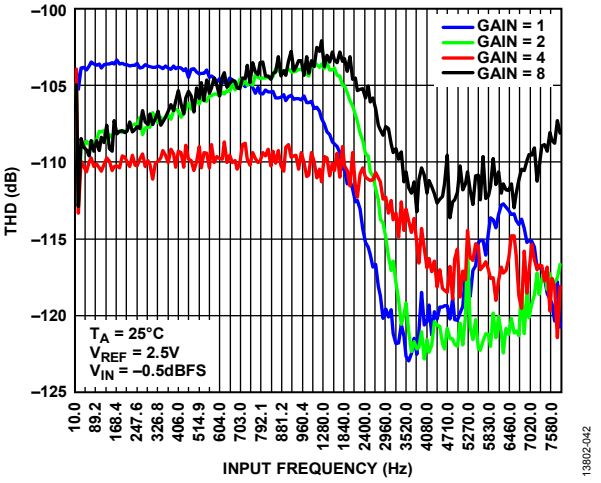

Figure 42. THD vs. Input Frequency at 16 kSPS, Low Power Mode, Sinc5 Filter Enabled

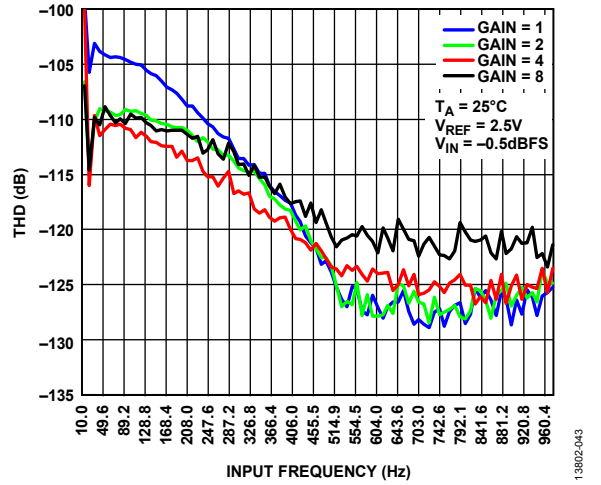

Figure 43. THD vs. Input Frequency at 4 kSPS, Low Power Mode, Sinc3 Filter Enabled

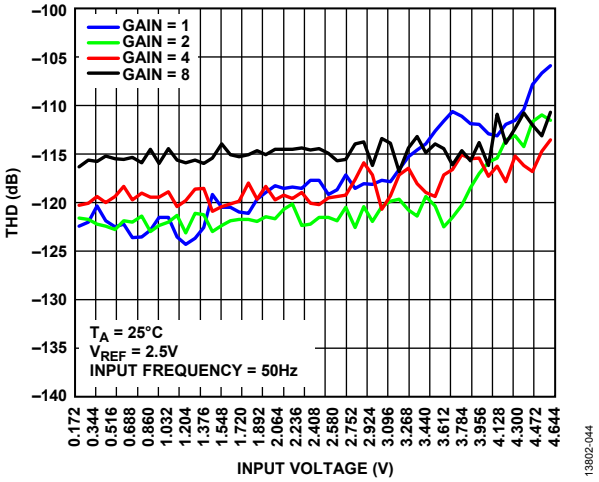

Figure 44. THD vs. Input Voltage at 64 kSPS, High Resolution Mode

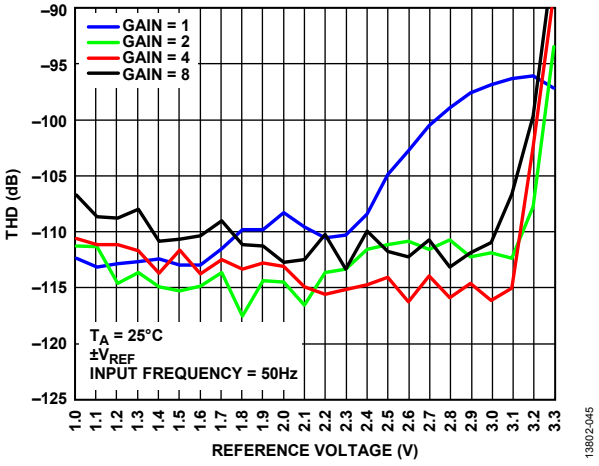

Figure 45. THD vs. Reference Voltage at 64 kSPS, High Resolution Mode

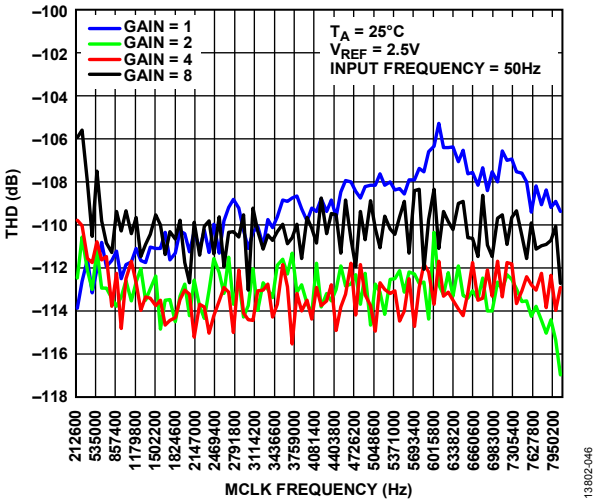

Figure 46. THD vs. Master Clock Frequency, High Resolution Mode

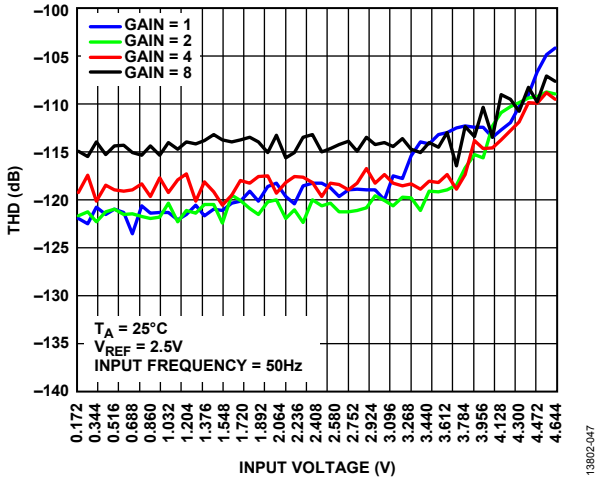

Figure 47. THD vs. Input Voltage at 16 kSPS, Low Power Mode

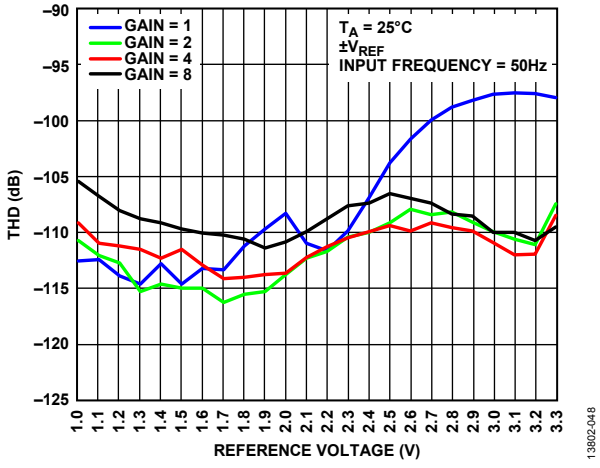

Figure 48. THD vs. Reference Voltage at 16 kSPS, Low Power Mode

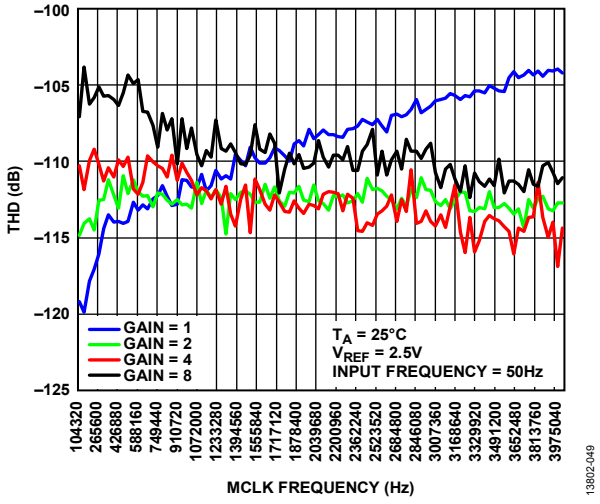

Figure 49. THD vs. Master Clock Frequency, Low Power Mode

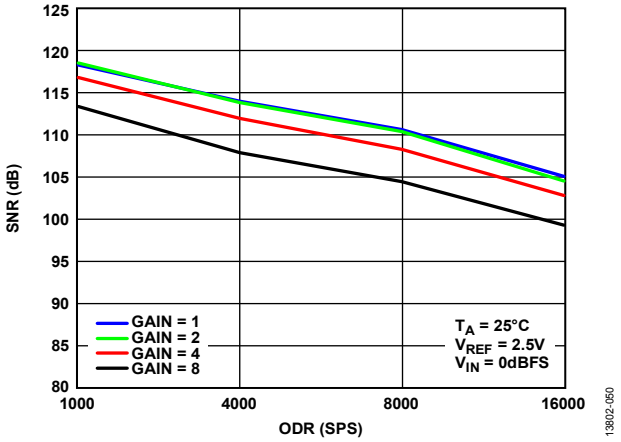

Figure 50. SNR vs. ODR at 16 kSPS, High Resolution Mode (AVDDx = 3.6 V, IOVDD = 3.6 V)

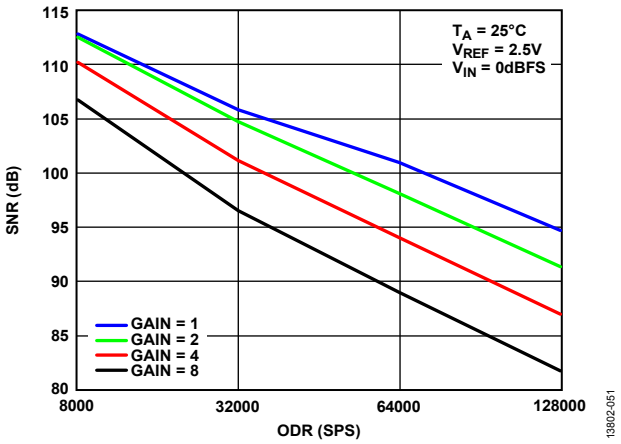

Figure 51. SNR vs. ODR at 64 kSPS, High Resolution Mode (AVDDx = 3.6 V, IOVDD = 3.6 V)

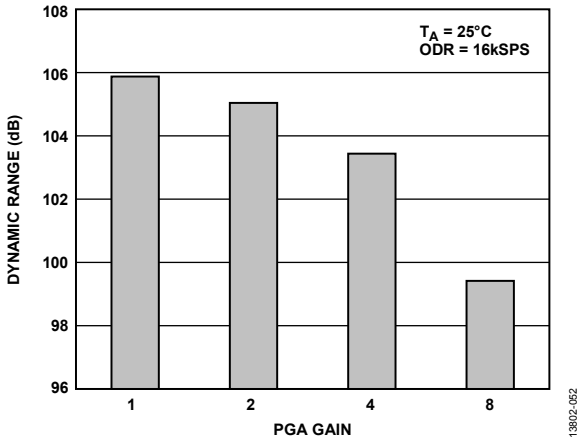

Figure 52. Dynamic Range vs. PGA Gain at 16 kSPS, High Resolution Mode

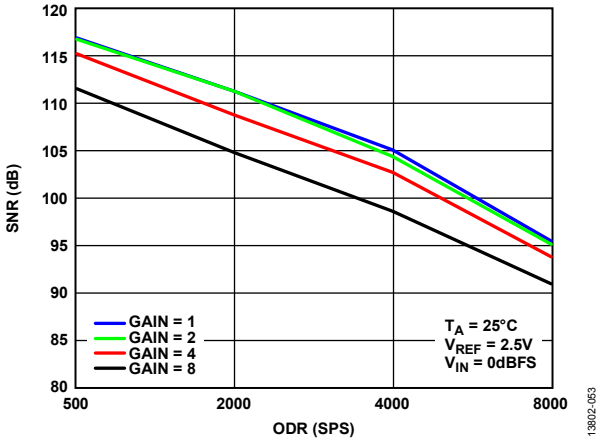

Figure 53. SNR vs. ODR at 4 kSPS, Low Power Mode (AVDDx = 3.6 V, IOVDD = 3.6 V)

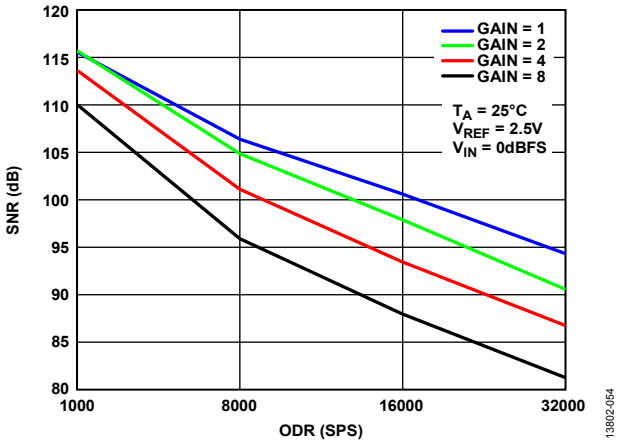

Figure 54. SNR vs. ODR at 16 kSPS, Low Power Mode (AVDDx = 3.6 V, IOVDD = 3.6 V)

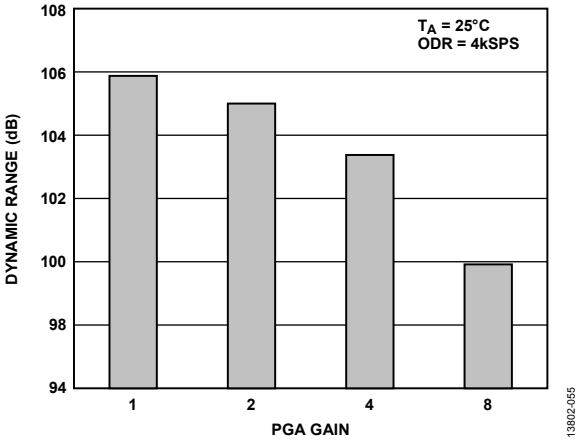

Figure 55. Dynamic Range vs. PGA Gain at 4 kSPS, Low Power Mode

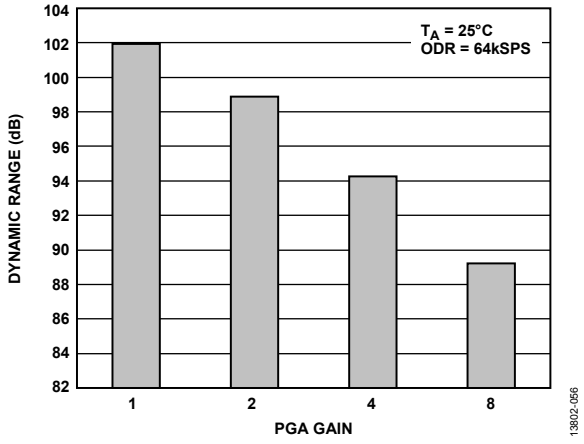

Figure 56. Dynamic Range vs. PGA Gain at 64 kSPS, High Resolution Mode

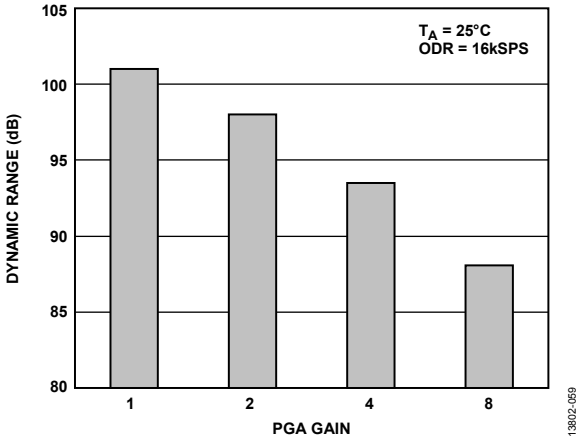

Figure 59. Dynamic Range vs. PGA Gain at 16 kSPS, Low Power Mode

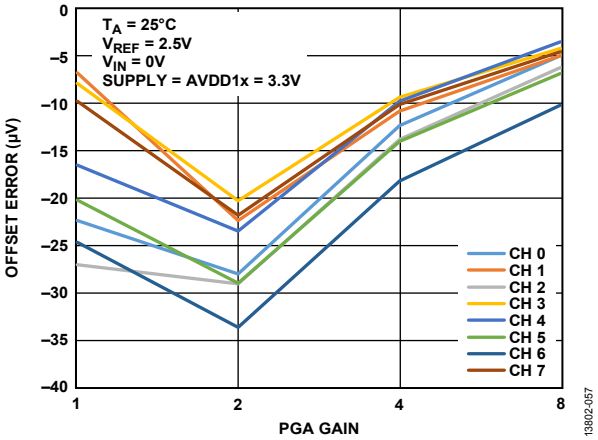

Figure 57. Offset Error vs. PGA Gain at 64 kSPS, High Resolution Mode

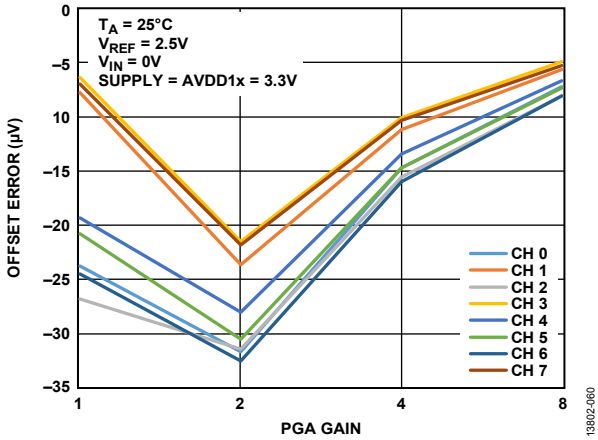

Figure 60. Offset Error vs. PGA Gain at 16 kSPS, Low Power Mode

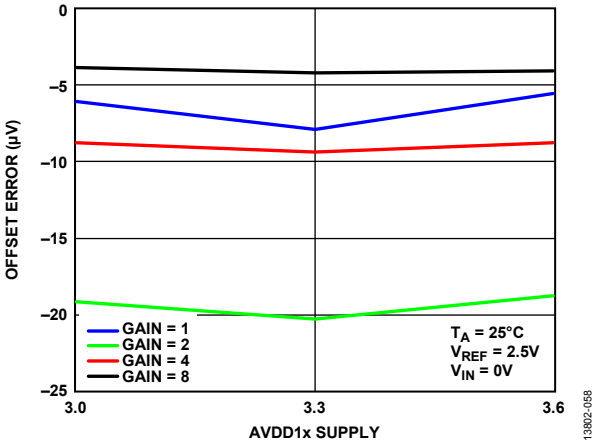

Figure 58. Offset Error vs. AVDD1x Supply, High Resolution Mode

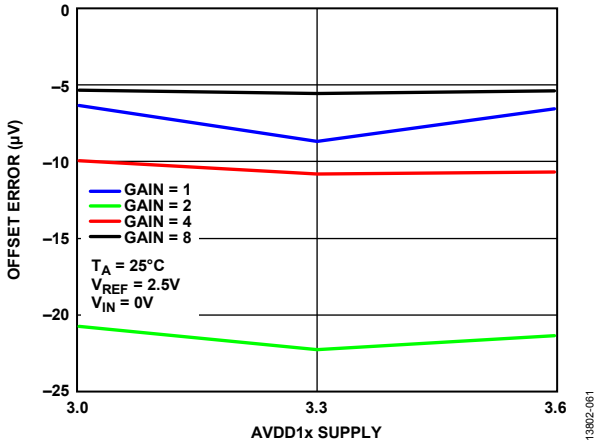

Figure 61. Offset Error vs. AVDD1x Supply, Low Power Mode