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FEATURES

- Up to 23 effective bits
- RMS noise: 40 nV @ 4.17 Hz, 85 nV @ 16.7 Hz
- Current: 400 μ A typical
- Power-down: 1 μ A maximum
- Low noise, programmable gain, instrumentation amp
- Band gap reference with 4 ppm/ $^{\circ}$ C drift typical
- Update rate: 4.17 Hz to 470 Hz
- Six differential analog inputs
- Internal clock oscillator
- Simultaneous 50 Hz/60 Hz rejection
- Reference detect
- Programmable current sources
- On-chip bias voltage generator
- Burnout currents
- Low-side power switch
- Power supply: 2.7 V to 5.25 V
- Temperature range:
 - B grade: -40° C to $+105^{\circ}$ C
 - C grade: -40° C to $+125^{\circ}$ C
- Independent interface power supply
- 24-lead TSSOP
- 3-wire serial interface
 - SPI[®], QSPI[™], MICROWIRE[™], and DSP compatible
 - Schmitt trigger on SCLK

APPLICATIONS

- Temperature measurement
- Pressure measurement
- Weigh scales
- Strain gage transducers
- Gas analysis

- Industrial process control
- Instrumentation
- Blood analysis
- Smart transmitters
- Liquid/gas chromatography
- 6-digit DVM

GENERAL DESCRIPTION

The AD7794/AD7795 are low power, low noise, complete analog front ends for high precision measurement applications. They contain a low noise, 24-/16-bit Σ - Δ ADC with six differential inputs. The on-chip low noise instrumentation amplifier means that signals of small amplitude can be interfaced directly to the ADC.

Each device contains a precision, low noise, low drift internal band gap reference, and can also accept up to two external differential references. Other on-chip features include programmable excitation current sources, burnout currents, and a bias voltage generator that is used to set the common-mode voltage of a channel to $AV_{DD}/2$. The low-side power switch can be used to power down bridge sensors between conversions, minimizing the system's power consumption. The AD7794/AD7795 can operate with either an internal clock or an external clock. The output data rate from each part can vary from 4.17 Hz to 470 Hz.

Both parts operate with a power supply from 2.7 V to 5.25 V. The B-grade parts (AD7794 and AD7795) are specified for a temperature range of -40° C to $+105^{\circ}$ C while the C-grade part (AD7794) is specified for a temperature range of -40° C to $+125^{\circ}$ C. They consume a current of 400 μ A typical and are housed in a 24-lead TSSOP.

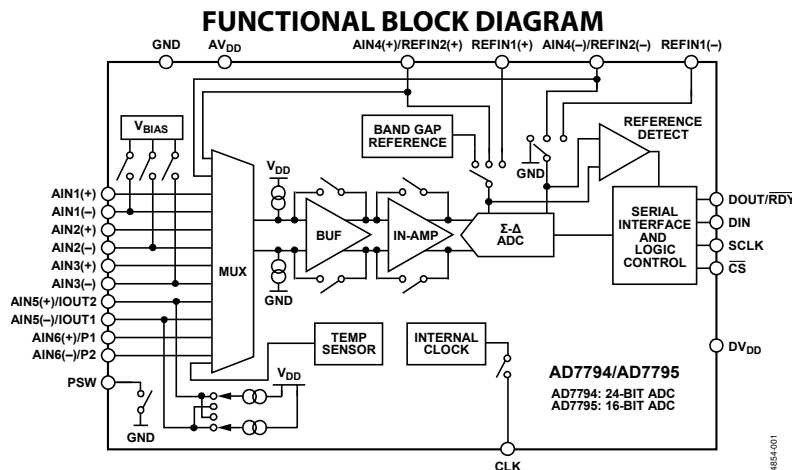


Figure 1.

Rev. D

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TABLE OF CONTENTS

Features	1	Full-Scale Register	25
Applications	1	ADC Circuit Information.....	26
General Description	1	Overview	26
Functional Block Diagram	1	Digital Interface	28
Revision History	2	Circuit Description.....	31
Specifications.....	3	Analog Input Channel	31
Timing Characteristics.....	8	Instrumentation Amplifier.....	31
Timing Diagrams.....	9	Bipolar/Unipolar Configuration	31
Absolute Maximum Ratings.....	10	Data Output Coding	32
ESD Caution.....	10	Burnout Currents	32
Pin Configuration and Function Descriptions.....	11	Excitation Currents	32
RMS Noise and Resolution Specifications	13	Bias Voltage Generator	32
Chop Enabled.....	13	Reference	32
Chop Disabled	15	Reference Detect.....	33
Typical Performance Characteristics	16	Reset	33
On-Chip Registers	17	AV _{DD} Monitor	33
Communications Register.....	17	Calibration.....	33
Status Register	18	Grounding and Layout	34
Mode Register	19	Applications Information	35
Configuration Register	22	Flowmeter.....	35
Data Register	24	Outline Dimensions	36
ID Register.....	24	Ordering Guide	36
IO Register.....	24		
Offset Register.....	25		

REVISION HISTORY

3/07—Rev. C to Rev. D

Changes to Specifications Endnote 1	7
Changes to Status Register Section	18
Changes to Ordering Guide	36

10/06—Rev. B to Rev. C

Updated Format	Universal
Added AD7794 C-Grade Part.....	Universal
Changes to Specifications	3
Changes to Ordering Guide	36

6/06—Rev. A to Rev. B

Added AD7795	Universal
Changes to Features.....	1
Changes to Table 1.....	3
Changes to RMS Noise and Resolution Specifications Section.....	12
Changes to Table 19.....	20
Changes to ADC Circuit Information Section	25
Changes to Ordering Guide	35

4/05—Rev. 0 to Rev. A

Changes to Absolute Maximum Ratings.....	9
Changes to Figure 21.....	25
Changes to Data Output Coding Section.....	28
Changes to Calibration Section	30
Changes to Ordering Guide	33

10/04—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 2.7\text{ V to }5.25\text{ V}$, $DV_{DD} = 2.7\text{ V to }5.25\text{ V}$, $GND = 0\text{ V}$, all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 1.

Parameter ¹	AD7794/AD7795	Unit	Test Conditions/Comments
CHOP ENABLED			
Output Update Rate	4.17 to 470	Hz nom	Settling time = 2/output update rate
No Missing Codes ²			
AD7794	24	Bits min	$f_{ADC} \leq 242\text{ Hz}$
AD7795	16	Bits min	
Resolution			See the RMS Noise and Resolution Specifications section
RMS Noise and Update Rates			See the RMS Noise and Resolution Specifications section
Integral Nonlinearity	± 15	ppm of FSR max	
Offset Error ³	± 1	$\mu\text{V typ}$	
Offset Error Drift vs. Temperature ⁴	± 10	$\text{nV}/^\circ\text{C typ}$	
Full-Scale Error ^{3, 5}	± 10	$\mu\text{V typ}$	
Gain Drift vs. Temperature ⁴	± 1	$\text{ppm}/^\circ\text{C typ}$	Gain = 1 to 16, external reference
	± 3	$\text{ppm}/^\circ\text{C typ}$	Gain = 32 to 128, external reference
Power Supply Rejection	100	dB min	$A_{IN} = 1\text{ V/gain}$, gain ≥ 4 , external reference
ANALOG INPUTS			
Differential Input Voltage Ranges	$\pm V_{REF}/\text{gain}$	V nom	$V_{REF} = \text{REFIN}(+) - \text{REFIN}(-)$, or internal reference, gain = 1 to 128
Absolute AIN Voltage Limits ²			
Unbuffered Mode	$GND - 30\text{ mV}$ $AV_{DD} + 30\text{ mV}$	V min V max	Gain = 1 or 2
Buffered Mode	$GND + 100\text{ mV}$ $AV_{DD} - 100\text{ mV}$	V min V max	Gain = 1 or 2
In-Amp Active	$GND + 300\text{ mV}$ $AV_{DD} - 1.1$	V min V max	Gain = 4 to 128
Common-Mode Voltage, V_{CM}	0.5	V min	$V_{CM} = (\text{AIN}(+) + \text{AIN}(-))/2$, gain = 4 to 128
Analog Input Current			
Buffered Mode or In-Amp Active			
Average Input Current ²			
AD7794B/AD7795B	± 1 ± 250 ± 1	nA max pA max nA max	Gain = 1 or 2, update rate < 100 Hz Gain = 4 to 128, update rate < 100 Hz $\text{AIN6}(+)/\text{AIN6}(-)$
AD7794C	± 3 ± 2 ± 3	nA max nA max nA max	Gain = 1 or 2, update rate < 100 Hz Gain = 4 to 128, update rate < 100 Hz $\text{AIN6}(+)/\text{AIN6}(-)$
Average Input Current Drift	± 2	$\text{pA}/^\circ\text{C typ}$	
Unbuffered Mode			Gain = 1 or 2
Average Input Current	± 400	$\text{nA}/\text{V typ}$	Input current varies with input voltage
Average Input Current Drift	± 50	$\text{pA}/\text{V}/^\circ\text{C typ}$	
Normal Mode Rejection ^{2, 6}			
Internal Clock			
@ 50 Hz, 60 Hz	65	dB min	80 dB typ, $50 \pm 1\text{ Hz}$, $60 \pm 1\text{ Hz}$, $\text{FS}[3:0] = 1010$
@ 50 Hz	80	dB min	90 dB typ, $50 \pm 1\text{ Hz}$, $\text{FS}[3:0] = 1001$
@ 60 Hz	90	dB min	100 dB typ, $60 \pm 1\text{ Hz}$, $\text{FS}[3:0] = 1000$
External Clock			
@ 50 Hz, 60 Hz	80	dB min	90 dB typ, $50 \pm 1\text{ Hz}$, $60 \pm 1\text{ Hz}$, $\text{FS}[3:0] = 1010$
@ 50 Hz	94	dB min	100 dB typ, $50 \pm 1\text{ Hz}$, $\text{FS}[3:0] = 1001$
@ 60 Hz	90	dB min	100 dB typ, $60 \pm 1\text{ Hz}$, $\text{FS}[3:0] = 1000$

AD7794/AD7795

Parameter ¹	AD7794/AD7795	Unit	Test Conditions/Comments
Common-Mode Rejection AD7794B/AD7795B			
@ DC	100	dB min	A _{IN} = 1 V/gain, gain ≥ 4
@ 50 Hz, 60 Hz ²	100	dB min	50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010
@ 50 Hz, 60 Hz ²	100	dB min	50 ± 1 Hz, FS[3:0] = 1001; 60 ± 1 Hz, FS[3:0] = 1000
AD7794C			
@ DC	97	dB min	A _{IN} = 1 V/gain, gain ≥ 4
@ 50 Hz, 60 Hz ²	97	dB min	50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010
@ 50 Hz, 60 Hz ²	97	dB min	50 ± 1 Hz, FS[3:0] = 1001; 60 ± 1 Hz, FS[3:0] = 1000
CHOP DISABLED			
Output Update Rate	4.17 to 470	Hz nom	Settling time = 1/output update rate
No Missing Codes ²			
AD7794	24	Bits min	f _{ADC} ≤ 123 Hz
AD7795	16	Bits min	
Resolution			See the RMS Noise and Resolution Specifications section
RMS Noise and Update Rates			See the RMS Noise and Resolution Specifications section
Integral Nonlinearity	±15	ppm of FSR max	
Offset Error ³	±100/gain	μV typ	Without calibration
Offset Error Drift vs. Temperature ⁴	±100/gain	nV/°C typ	Gain = 1 to 16
	10	nV/°C typ	Gain = 32 to 128
Full-Scale Error ^{3, 5}	±10	μV typ	
Gain Drift vs. Temperature ⁴	±1	ppm/°C typ	Gain = 1 to 16, external reference
	±3	ppm/°C typ	Gain = 32 to 128, external reference
Power Supply Rejection	100	dB typ	A _{IN} = 1 V/gain, gain ≥ 4, external reference
ANALOG INPUTS			
Differential Input Voltage Ranges	±V _{REF} /gain	V nom	V _{REF} = REFIN(+) – REFIN(-), or internal reference, gain = 1 to 128
Absolute AIN Voltage Limits ²			
Unbuffered Mode	GND – 30 mV AV _{DD} + 30 mV	V min V max	Gain = 1 or 2
Buffered Mode	GND + 100 mV AV _{DD} – 100 mV	V min V max	Gain = 1 or 2
In-Amp Active	GND + 300 mV AV _{DD} – 1.1	V min V max	Gain = 4 to 128
Common-Mode Voltage, V _{CM}	0.2 + (gain/2 × (A _{IN} (+) – A _{IN} (-))) AV _{DD} – 0.2 – (gain/2 × (A _{IN} (+) – A _{IN} (-)))	V min V max	AMP – CM = 1, V _{CM} = (A _{IN} (+) + A _{IN} (-))/2, gain = 4 to 128
Analog Input Current			
Buffered Mode or In-Amp Active			
Average Input Current ²			
AD7794B/AD7795B	±1 ±250	nA max pA max	Gain = 1 or 2 Gain = 4 to 128
AD7794C	±1 ±3 ±2 ±3	nA max nA max nA max nA max	A _{IN} 6(+)/A _{IN} 6(-) Gain = 1 or 2 Gain = 4 to 128 A _{IN} 6(+)/A _{IN} 6(-)
Average Input Current Drift	±2	pA/°C typ	
Unbuffered Mode			
Average Input Current	±400	nA/V typ	Input current varies with input voltage
Average Input Current Drift	±50	pA/V/°C typ	

Parameter ¹	AD7794/AD7795	Unit	Test Conditions/Comments
Normal Mode Rejection ^{2, 6}			
Internal Clock			
@ 50 Hz, 60 Hz	60	dB min	70 dB typ, 50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010
@ 50 Hz	78	dB min	90 dB typ, 50 ± 1 Hz, FS[3:0] = 1001
@ 60 Hz	86	dB min	100 dB typ, 60 ± 1 Hz, FS[3:0] = 1000
External Clock			
@ 50 Hz, 60 Hz	60	dB min	70 dB typ, 50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010
@ 50 Hz	94	dB min	100 dB typ, 50 ± 1 Hz, FS[3:0] = 1001
@ 60 Hz	90	dB min	100 dB typ, 60 ± 1 Hz, FS[3:0] = 1000
Common-Mode Rejection			
AD7794B/AD7795B			
@ DC	100	dB min	A _{IN} = 1 V/gain, with gain = 4, AMP-CM Bit = 1
@ 50 Hz, 60 Hz ²	100	dB min	50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010
@ 50 Hz, 60 Hz ²	100	dB min	50 ± 1 Hz, FS[3:0] = 1001; 60 ± 1 Hz, FS[3:0] = 1000
AD7794C			
@ DC	97	dB min	A _{IN} = 1 V/gain, with gain = 4, AMP-CM Bit = 1
@ 50 Hz, 60 Hz ²	97	dB min	50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010
@ 50 Hz, 60 Hz ²	97	dB min	50 ± 1 Hz, FS[3:0] = 1001; 60 ± 1 Hz, FS[3:0] = 1000
CHOP ENABLED or DISABLED			
REFERENCE INPUT			
Internal Reference			
Internal Reference Initial Accuracy	1.17 ± 0.01%	V min/max	A _{VDD} = 4 V, T _A = 25°C
Internal Reference Drift ²	4	ppm/°C typ	
	15	ppm/°C max	
Power Supply Rejection	85	dB typ	
External Reference			
External REF _{IN} Voltage	2.5	V nom	REF _{IN} = REF _{IN} (+) – REF _{IN} (–)
Reference Voltage Range ²	0.1	V min	
	A _{VDD}	V max	When V _{REF} = A _{VDD} , the differential input must be limited to 0.9 × V _{REF} /gain if the in-amp is active
Absolute REF _{IN} Voltage Limits ²	GND – 30 mV	V min	
	A _{VDD} + 30 mV	V max	
Average Reference Input Current	400	nA/V typ	
Average Reference Input Current Drift	±0.03	nA/V/°C typ	
Normal Mode Rejection ²			Same as for analog inputs
Common-Mode Rejection	100	dB typ	
Reference Detect Levels	0.3	V min	
	0.65	V max	NOXREF bit active if V _{REF} < 0.3 V
EXCITATION CURRENT SOURCES (IEXC1 and IEXC2)			
Output Current	10/210/1000	μA nom	
Initial Tolerance at 25°C	±5	% typ	
Drift	200	ppm/°C typ	
Current Matching	±0.5	% typ	Matching between IEXC1 and IEXC2, V _{OUT} = 0 V
Drift Matching	50	ppm/°C typ	
Line Regulation (A _{VDD})	2	%/V typ	A _{VDD} = 5 V ± 5%
Load Regulation	0.2	%/V typ	
Output Compliance	A _{VDD} – 0.65	V max	Current sources programmed to 10 μA or 210 μA
	A _{VDD} – 1.1	V max	Current sources programmed to 1 mA
	GND – 30 mV	V min	

AD7794/AD7795

Parameter ¹	AD7794/AD7795	Unit	Test Conditions/Comments
BIAS VOLTAGE GENERATOR			
V_{BIAS}	$AV_{DD}/2$	V nom	
V_{BIAS} Generator Start-Up Time		ms/nF typ	Dependent on the capacitance connected to AIN; See Figure 11
TEMPERATURE SENSOR			
Accuracy	± 2	$^{\circ}\text{C}$ typ	Applies if user calibrates the temperature sensor
Sensitivity	0.81	mV/ $^{\circ}\text{C}$ typ	
LOW-SIDE POWER SWITCH			
R_{ON}	7	Ω max	$AV_{DD} = 5\text{ V}$
	9	Ω max	$AV_{DD} = 3\text{ V}$
Allowable Current ²	30	mA max	Continuous current
DIGITAL OUTPUTS (P1 and P2)			
V_{OH} , Output High Voltage ²	$AV_{DD} - 0.6$	V min	$AV_{DD} = 3\text{ V}$, $I_{SOURCE} = 100\ \mu\text{A}$
V_{OL} , Output Low Voltage ²	0.4	V max	$AV_{DD} = 3\text{ V}$, $I_{SINK} = 100\ \mu\text{A}$
V_{OH} , Output High Voltage ²	4	V min	$AV_{DD} = 5\text{ V}$, $I_{SOURCE} = 200\ \mu\text{A}$
V_{OL} , Output Low Voltage ²	0.4	V max	$AV_{DD} = 5\text{ V}$, $I_{SINK} = 800\ \mu\text{A}$
INTERNAL/EXTERNAL CLOCK			
Internal Clock			
Frequency ²	$64 \pm 3\%$	kHz min/max	
Duty Cycle	50:50	% typ	
External Clock			
Frequency	64	kHz nom	A 128 kHz external clock can be used if the divide-by-2 function is used (Bit CLK1 = CLK0 = 1)
Duty Cycle	45:55 to 55:45	% typ	Applies for external 64 kHz clock, a 128 kHz clock can have a less stringent duty cycle
LOGIC INPUTS			
\overline{CS}^2			
V_{INL} , Input Low Voltage	0.8	V max	$DV_{DD} = 5\text{ V}$
	0.4	V max	$DV_{DD} = 3\text{ V}$
V_{INH} , Input High Voltage	2.0	V min	$DV_{DD} = 3\text{ V}$ or 5 V
SCLK (Schmitt-Triggered Input), CLK, and DIN ²			
AD7794B/AD7795B			
$V_{T(+)}$	1.4/2	V min/max	$DV_{DD} = 5\text{ V}$
$V_{T(-)}$	0.8/1.7	V min/max	$DV_{DD} = 5\text{ V}$
$V_{T(+)}$ to $V_{T(-)}$	0.1/0.17	V min/max	$DV_{DD} = 5\text{ V}$
$V_{T(+)}$	0.9/2	V min/max	$DV_{DD} = 3\text{ V}$
$V_{T(-)}$	0.4/1.35	V min/max	$DV_{DD} = 3\text{ V}$
$V_{T(+)}$ to $V_{T(-)}$	0.06/0.13	V min/max	$DV_{DD} = 3\text{ V}$
AD7794C			
$V_{T(+)}$	1.35/2.05	V min/max	$DV_{DD} = 5\text{ V}$
$V_{T(-)}$	0.8/1.9	V min/max	$DV_{DD} = 5\text{ V}$
$V_{T(+)}$ to $V_{T(-)}$	0.1/0.19	V min/max	$DV_{DD} = 5\text{ V}$
$V_{T(+)}$	0.9/2	V min/max	$DV_{DD} = 3\text{ V}$
$V_{T(-)}$	0.4/1.35	V min/max	$DV_{DD} = 3\text{ V}$
$V_{T(+)}$ to $V_{T(-)}$	0.06/0.15	V min/max	$DV_{DD} = 3\text{ V}$
Input Currents	± 10	μA max	$V_{IN} = DV_{DD}$ or GND
Input Capacitance	10	pF typ	All digital inputs

Parameter ¹	AD7794/AD7795	Unit	Test Conditions/Comments
LOGIC OUTPUT (INCLUDING CLK)			
V_{OH} , Output High Voltage ²	$DV_{DD} - 0.6$	V min	$DV_{DD} = 3\text{ V}$, $I_{SOURCE} = 100\ \mu\text{A}$
V_{OL} , Output Low Voltage ²	0.4	V max	$DV_{DD} = 3\text{ V}$, $I_{SINK} = 100\ \mu\text{A}$
V_{OH} , Output High Voltage ²	4	V min	$DV_{DD} = 5\text{ V}$, $I_{SOURCE} = 200\ \mu\text{A}$
V_{OL} , Output Low Voltage ²	0.4	V max	$DV_{DD} = 5\text{ V}$, $I_{SINK} = 1.6\text{ mA}$ (DOUT/RDY), 800 μA (CLK)
Floating-State Leakage Current	± 10	μA max	
Floating-State Output Capacitance	10	pF typ	
Data Output Coding	Offset binary		
SYSTEM CALIBRATION ²			
Full-Scale Calibration Limit	$1.05 \times \text{FS}$	V max	
Zero-Scale Calibration Limit	$-1.05 \times \text{FS}$	V min	
Input Span	$0.8 \times \text{FS}$	V min	
	$2.1 \times \text{FS}$	V max	
POWER REQUIREMENTS ⁷			
Power Supply Voltage			
AV_{DD} to GND	2.7/5.25	V min/max	
DV_{DD} to GND	2.7/5.25	V min/max	
Power Supply Currents			
I_{DD} Current	140	μA max	110 μA typ @ $AV_{DD} = 3\text{ V}$, 125 μA typ @ $AV_{DD} = 5\text{ V}$, unbuffered mode, external reference
	185	μA max	130 μA typ @ $AV_{DD} = 3\text{ V}$, 165 μA typ @ $AV_{DD} = 5\text{ V}$, buffered mode, gain = 1 or 2, external reference
	400	μA max	300 μA typ @ $AV_{DD} = 3\text{ V}$, 350 μA typ @ $AV_{DD} = 5\text{ V}$, gain = 4 to 128, external reference
	500	μA max	400 μA typ @ $AV_{DD} = 3\text{ V}$, 450 μA typ @ $AV_{DD} = 5\text{ V}$, gain = 4 to 128, internal reference
I_{DD} (Power-Down Mode)	1	μA max	AD7794B, AD7795B
	2	μA max	AD7794C

¹ Temperature range: B Grade: -40°C to $+105^{\circ}\text{C}$, C Grade: -40°C to $+125^{\circ}\text{C}$. At the 19.6 Hz and 39.2 Hz update rates, the INL, power supply rejection (PSR), common-mode rejection (CMR), and normal mode rejection (NMR) do not meet the data sheet specification if the voltage on the AIN(+) or AIN(-) pins exceeds $AV_{DD} - 1.6\text{ V}$ typically. In addition, the offset error and offset error drift degrade at these update rates when chopping is disabled. When this voltage is exceeded, the INL, for example, is reduced to 18 ppm of FS typically while the PSR is reduced to 69 dB typically. Therefore, for guaranteed performance at these update rates, the absolute voltage on the analog input pins needs to be below $AV_{DD} - 1.6\text{ V}$.

² Specification is not production tested but is supported by characterization data at initial product release.

³ Following a calibration, this error is in the order of the noise for the programmed gain and update rate selected.

⁴ Recalibration at any temperature removes these errors.

⁵ Full-scale error applies to both positive and negative full-scale, and applies at the factory calibration conditions ($AV_{DD} = 4\text{ V}$, gain = 1, $T_A = 25^{\circ}\text{C}$).

⁶ FS[3:0] are the four bits used in the mode register to select the output word rate.

⁷ Digital inputs equal to DV_{DD} or GND with excitation currents and bias voltage generator disabled.

TIMING CHARACTERISTICS

$AV_{DD} = 2.7\text{ V to }5.25\text{ V}$, $DV_{DD} = 2.7\text{ V to }5.25\text{ V}$, $GND = 0\text{ V}$, Input Logic 0 = 0 V, Input Logic 1 = DV_{DD} , unless otherwise noted.

Table 2.

Parameter ^{1, 2}	Limit at T_{MIN} , T_{MAX} (B Version)	Unit	Conditions/Comments
t_3	100	ns min	SCLK high pulse width
t_4	100	ns min	SCLK low pulse width
Read Operation			
t_1	0	ns min	\overline{CS} falling edge to DOUT/ \overline{RDY} active time
	60	ns max	$DV_{DD} = 4.75\text{ V to }5.25\text{ V}$
	80	ns max	$DV_{DD} = 2.7\text{ V to }3.6\text{ V}$
t_2^3	0	ns min	SCLK active edge to data valid delay ⁴
	60	ns max	$DV_{DD} = 4.75\text{ V to }5.25\text{ V}$
	80	ns max	$DV_{DD} = 2.7\text{ V to }3.6\text{ V}$
$t_5^{5, 6}$	10	ns min	Bus relinquish time after \overline{CS} inactive edge
	80	ns max	
t_6	0	ns min	SCLK inactive edge to \overline{CS} inactive edge
t_7	10	ns min	SCLK inactive edge to DOUT/ \overline{RDY} high
Write Operation			
t_8	0	ns min	\overline{CS} falling edge to SCLK active edge setup time ⁴
t_9	30	ns min	Data valid to SCLK edge setup time
t_{10}	25	ns min	Data valid to SCLK edge hold time
t_{11}	0	ns min	\overline{CS} rising edge to SCLK edge hold time

¹ Sample tested during initial release to ensure compliance. All input signals are specified with $t_r = t_f = 5\text{ ns}$ (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.

² See Figure 3 and Figure 4.

³ These numbers are measured with the load circuit shown in Figure 2 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

⁴ SCLK active edge is falling edge of SCLK.

⁵ These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit shown in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, therefore, are independent of external bus loading capacitances.

⁶ \overline{RDY} returns high after a read of the ADC. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while \overline{RDY} is high, although care should be taken to ensure that subsequent reads do not occur close to the next output update. In continuous read mode, the digital word can be read only once.

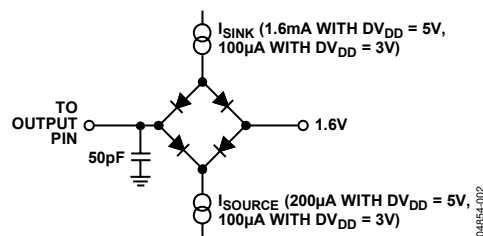


Figure 2. Load Circuit for Timing Characterization

TIMING DIAGRAMS

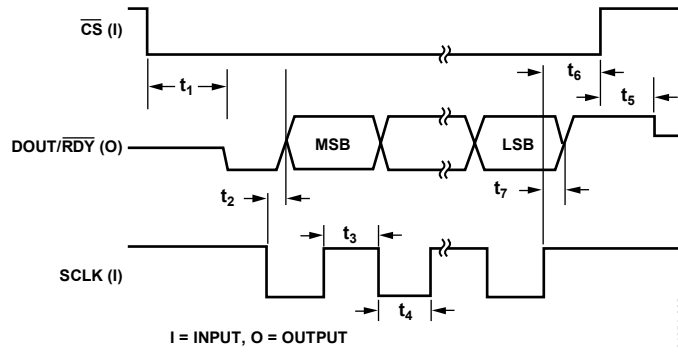


Figure 3. Read Cycle Timing Diagram

04854-003

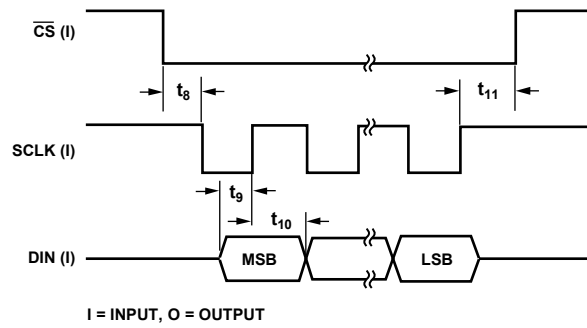


Figure 4. Write Cycle Timing Diagram

04854-004

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV _{DD} to GND	−0.3 V to +7 V
DV _{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to AV _{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to AV _{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to DV _{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to DV _{DD} + 0.3 V
AIN/Digital Input Current	10 mA
Operating Temperature Range	
B Grade	−40°C to +105°C
C Grade	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
TSSOP	
θ _{JA} Thermal Impedance	97.9°C/W
θ _{JC} Thermal Impedance	14°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

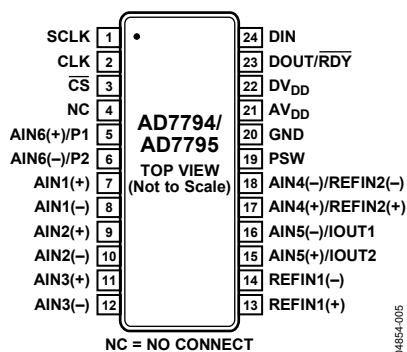


Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data.
2	CLK	Clock In/Clock Out. The internal clock can be made available at this pin. Alternatively, the internal clock can be disabled, and the ADC can be driven by an external clock. This allows several ADCs to be driven from a common clock, allowing simultaneous conversions to be performed.
3	$\overline{\text{CS}}$	Chip Select Input. This is an active low logic input used to select the ADC. $\overline{\text{CS}}$ can be used to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{\text{CS}}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device.
4	NC	No Connect.
5	AIN6(+)/P1	Analog Input/Digital Output Pin. AIN6(+) is the positive terminal of the differential analog input pair, AIN6(+)/AIN6(-). This pin can also function as a general-purpose output bit referenced between AV_{DD} and GND.
6	AIN6(-)/P2	Analog Input/Digital Output Pin. AIN6(-) is the negative terminal of the differential analog input pair, AIN6(+)/AIN6(-). This pin can also function as a general-purpose output bit referenced between AV_{DD} and GND.
7	AIN1(+)	Analog Input. AIN1(+) is the positive terminal of the differential analog input pair, AIN1(+)/AIN1(-).
8	AIN1(-)	Analog Input. AIN1(-) is the negative terminal of the differential analog input pair, AIN1(+)/AIN1(-).
9	AIN2(+)	Analog Input. AIN2(+) is the positive terminal of the differential analog input pair, AIN2(+)/AIN2(-).
10	AIN2(-)	Analog Input. AIN2(-) is the negative terminal of the differential analog input pair, AIN2(+)/AIN2(-).
11	AIN3(+)	Analog Input. AIN3(+) is the positive terminal of the differential analog input pair, AIN3(+)/AIN3(-).
12	AIN3(-)	Analog Input. AIN3(-) is the negative terminal of the differential analog input pair, AIN3(+)/AIN3(-).
13	REFIN1(+)	Positive Reference Input. An external reference can be applied between REFIN1(+) and REFIN1(-). REFIN1(+) can lie anywhere between AV_{DD} and $\text{GND} + 0.1 \text{ V}$. The nominal reference voltage, (REFIN1(+)) – REFIN1(-)), is 2.5 V, but the part functions with a reference from 0.1 V to AV_{DD} .
14	REFIN1(-)	Negative Reference Input. This reference input can lie anywhere between GND and $\text{AV}_{\text{DD}} - 0.1 \text{ V}$.
15	AIN5(+)/IOUT2	Analog Input/Output of Internal Excitation Current Source. AIN5(+) is the positive terminal of the differential analog input pair AIN5(+)/AIN5(-). Alternatively, the internal excitation current source can be made available at this pin and is programmable so that the current can be 10 μA , 210 μA , or 1 mA. Either IEXC1 or IEXC2 can be switched to this output.
16	AIN5(-)/IOUT1	Analog Input/Output of Internal Excitation Current Source. AIN5(-) is the negative terminal of the differential analog input pair, AIN5(+)/AIN5(-). Alternatively, the internal excitation current source can be made available at this pin and is programmable so that the current can be 10 μA , 210 μA , or 1 mA. Either IEXC1 or IEXC2 can be switched to this output.
17	AIN4(+)/REFIN2(+)	Analog Input/Positive Reference Input. AIN4(+) is the positive terminal of the differential analog input pair AIN4(+)/AIN4(-). This pin also functions as a positive reference input for REFIN2. REFIN2(+) can lie anywhere between AV_{DD} and $\text{GND} + 0.1 \text{ V}$. The nominal reference voltage (REFIN2(+) to REFIN2(-)) is 2.5 V, but the part functions with a reference from 0.1 V to AV_{DD} .

AD7794/AD7795

Pin No.	Mnemonic	Description
18	AIN4(-)/REFIN2(-)	Analog Input/Negative Reference Input. AIN4(-) is the negative terminal of the differential analog input pair AIN4(+)/AIN4(-). This pin also functions as the negative reference input for REFIN2. This reference input can lie anywhere between GND and $AV_{DD} - 0.1$ V.
19	PSW	Low-Side Power Switch to GND.
20	GND	Ground Reference Point.
21	AV_{DD}	Supply Voltage, 2.7 V to 5.25 V.
22	DV_{DD}	Serial Interface Supply Voltage, 2.7 V to 5.25 V. DV_{DD} is independent of AV_{DD} . Therefore, the serial interface operates at 3 V with AV_{DD} at 5 V or vice versa.
23	DOUT/ \overline{RDY}	Serial Data Output/Data Ready Output. DOUT/ \overline{RDY} serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/ \overline{RDY} operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/ \overline{RDY} falling edge can also be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/ \overline{RDY} pin. With \overline{CS} low, the data/control word information is placed on the DOUT/ \overline{RDY} pin on the SCLK falling edge and is valid on the SCLK rising edge.
24	DIN	Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers within the ADC with the register selection bits of the communications register identifying the appropriate register.

RMS NOISE AND RESOLUTION SPECIFICATIONS

The AD7794/AD7795 can be operated with chop enabled or chop disabled, allowing the ADC to be optimized for switching time or drift performance. With chop enabled, the settling time is two times the conversion time. However, the offset is continuously removed by the ADC leading to low offset and low offset drift. With chop disabled, the allowable update rates are the same as in chop enable mode. However, the settling time now equals the conversion time. With chop disabled, the offset is not removed by the ADC, so periodic offset calibrations can be required to remove offset due to drift.

CHOP ENABLED

External Reference

Table 5 shows the AD7794/AD7795 rms noise for some update rates and gain settings. The numbers given are for the bipolar input range with an external 2.5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V.

Table 6 and Table 7 show the effective resolution, while the output peak-to-peak (p-p) resolution is listed in brackets. It is important to note that the effective resolution is calculated using the rms noise, while the p-p resolution is calculated based on peak-to-peak noise. The p-p resolution represents the resolution for which there is no code flicker. These numbers are typical and are rounded to the nearest LSB.

Table 5. RMS Noise (μV) vs. Gain and Output Update Rate Using an External 2.5 V Reference with Chop Enabled

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	0.64	0.6	0.29	0.22	0.1	0.065	0.039	0.041
8.33	1.04	0.96	0.38	0.26	0.13	0.078	0.057	0.055
16.7	1.55	1.45	0.54	0.36	0.18	0.11	0.087	0.086
33.2	2.3	2.13	0.74	0.5	0.23	0.17	0.124	0.118
62	2.95	2.85	0.92	0.58	0.29	0.2	0.153	0.144
123	4.89	4.74	1.49	1	0.48	0.32	0.265	0.283
242	11.76	9.5	4.02	1.96	0.88	0.45	0.379	0.397
470	11.33	9.44	3.07	1.79	0.99	0.63	0.568	0.593

Table 6.

Effective Resolution (Bits) vs. Gain and Output Update Rate for the AD7794 Using an External 2.5 V Reference with Chop Enabled

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	23 (20.5)	22 (19.5)	22 (19.5)	21.5 (19)	21.5 (19)	21 (18.5)	21 (18.5)	20 (17.5)
8.33	22 (19.5)	21.5 (19)	21.5 (19)	21 (18.5)	21 (18.5)	21 (18.5)	20.5 (18)	19.5 (17)
16.7	21.5 (19)	20.5 (18)	21 (18.5)	20.5 (18)	20.5 (18)	20.5 (18)	20 (17.5)	19 (16.5)
33.2	21 (18.5)	20 (17.5)	20.5 (18)	20 (17.5)	20.5 (18)	20 (17.5)	19 (16.5)	18.5 (16)
62	20.5 (18)	19.5 (17)	20.5 (18)	20 (17.5)	20 (17.5)	19.5 (17)	19 (16.5)	18 (15.5)
123	20 (17.5)	19 (16.5)	19.5 (17)	19 (16.5)	19.5 (17)	19 (16.5)	18 (15.5)	17 (14.5)
242	18.5 (16)	18 (15.5)	18 (15.5)	18 (15.5)	18.5 (16)	18.5 (16)	17.5 (15)	16.5 (14)
470	18.5 (16)	18 (15.5)	18.5 (16)	18.5 (16)	18 (15.5)	18 (15.5)	17 (14.5)	16 (13.5)

Table 7.

Effective Resolution (Bits) vs. Gain and Output Update Rate for the AD7795 Using an External 2.5 V Reference with Chop Enabled

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
8.33	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
16.7	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
33.2	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
62	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)
123	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)	16 (14.5)
242	16 (16)	16 (15.5)	16 (15.5)	16 (15.5)	16 (16)	16 (16)	16 (15)	16 (14)
470	16 (16)	16 (15.5)	16 (16)	16 (16)	16 (15.5)	16 (15.5)	16 (14.5)	16 (13.5)

AD7794/AD7795

Internal Reference

Table 8 shows the AD7794/AD7795 rms noise for some of the update rates and gain settings. The numbers given are for the bipolar input range with the internal 1.17 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 9 and Table 10 show the effective resolution while the output peak-to-peak (p-p) resolution is listed in brackets.

It is important to note that the effective resolution is calculated using the rms noise while the p-p resolution is calculated based on peak-to-peak noise. The p-p resolution represents the resolution for which there is no code flicker. These numbers are typical and rounded to the nearest LSB.

Table 8. RMS Noise (μV) vs. Gain and Output Update Rate Using an Internal 1.17 V Reference with Chop Enabled

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	0.81	0.67	0.32	0.2	0.13	0.065	0.04	0.039
8.33	1.18	1.11	0.41	0.25	0.16	0.078	0.058	0.059
16.7	1.96	1.72	0.55	0.36	0.25	0.11	0.088	0.088
33.2	2.99	2.48	0.83	0.48	0.33	0.17	0.13	0.12
62	3.6	3.25	1.03	0.65	0.46	0.2	0.15	0.15
123	5.83	5.01	1.69	0.96	0.67	0.32	0.25	0.26
242	11.22	8.64	2.69	1.9	1.04	0.45	0.35	0.34
470	12.46	10.58	4.58	2	1.27	0.63	0.50	0.49

Table 9.

Effective Resolution (Bits) vs. Gain and Output Update Rate for the AD7794 Using an Internal 1.17 V Reference with Chop Enabled

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	21.5 (19)	20.5 (18)	21 (18.5)	20.5 (18)	20 (17.5)	20 (17.5)	20 (17.5)	19 (16.5)
8.33	21 (18.5)	20 (17.5)	20.5 (18)	20 (17.5)	20 (17.5)	20 (17.5)	19 (16.5)	18 (15.5)
16.7	20 (17.5)	19.5 (17)	20 (17.5)	19.5 (17)	19 (16.5)	19.5 (17)	18.5 (16)	17.5 (15)
33.2	19.5 (17)	19 (16.5)	19.5 (17)	19 (16.5)	19 (16.5)	18.5 (16)	18 (15.5)	17 (14.5)
62	19.5 (17)	18.5 (16)	19 (16.5)	19 (16.5)	18.5 (16)	18.5 (16)	18 (15.5)	17 (14.5)
123	18.5 (16)	18 (15.5)	18.5 (16)	18 (15.5)	17.5 (15)	18 (15.5)	17 (14.5)	16 (13.5)
242	17.5 (15)	17 (14.5)	17.5 (15)	17 (14.5)	17 (14.5)	17.5 (15)	16.5 (14)	15.5 (13)
470	17.5 (15)	17 (14.5)	17 (14.5)	17 (14.5)	17 (14.5)	17 (14.5)	16 (13.5)	15 (12.5)

Table 10.

Effective Resolution (Bits) vs. Gain and Output Update Rate for the AD7795 Using an Internal 1.17 V Reference with Chop Enabled

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
8.33	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)
16.7	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15)
33.2	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)	16 (14.5)
62	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)	16 (14.5)
123	16 (16)	16 (15.5)	16 (16)	16 (15.5)	16 (15)	16 (15.5)	16 (14.5)	16 (13.5)
242	16 (15)	16 (14.5)	16 (15)	16 (14.5)	16 (14.5)	16 (15)	16 (14)	15.5 (13)
470	16 (15)	16 (14.5)	16 (14.5)	16 (14.5)	16 (14.5)	16 (14.5)	16 (13.5)	15 (12.5)

CHOP DISABLED

With chop disabled, the switching time or settling time is reduced by a factor of two. However, periodic offset calibrations may now be required to remove offset and offset drift. When chop is disabled, the AMP-CM bit in the mode register should be set to 1. This limits the allowable common-mode voltage that can be used. However, the common-mode rejection degrades if the bit is not set.

Table 11 shows the rms noise of the AD7794/AD7795 for some of the update rates and gain settings with chop disabled.

The numbers given are for the bipolar input range with the internal 1.17 V reference. These numbers are typical and are generated with a differential input voltage of 0 V.

Table 12 and Table 13 show the effective resolution while the output peak-to-peak (p-p) resolution is listed in brackets. It is important to note that the effective resolution is calculated using the rms noise, while the p-p resolution is calculated based on peak-to-peak noise. The p-p resolution represents the resolution for which there is no code flicker. These numbers are typical and rounded to the nearest LSB.

Table 11. RMS Noise (μ V) vs. Gain and Output Update Rate Using an Internal 1.17 V Reference with Chop Disabled

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	1.22	0.98	0.33	0.18	0.13	0.062	0.053	0.051
8.33	1.74	1.53	0.49	0.29	0.21	0.1	0.079	0.07
16.7	2.64	2.44	0.79	0.48	0.33	0.16	0.13	0.12
33.2	4.55	3.52	1.11	0.66	0.46	0.21	0.17	0.16
62	5.03	4.45	1.47	0.81	0.58	0.27	0.2	0.22
123	8.13	7.24	2.27	1.33	0.96	0.48	0.36	0.37
242	15.12	13.18	3.77	2.09	1.45	0.64	0.5	0.47
470	17.18	14.63	8.86	2.96	1.92	0.89	0.69	0.7

Table 12.

Effective Resolution (Bits) vs. Gain and Output Update Rate for the AD7794 Using an Internal 1.17 V Reference with Chop Disabled

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	21 (18.5)	20 (17.5)	21 (18.5)	20.5 (18)	20 (17.5)	20 (17.5)	19.5 (17)	18.5 (16)
8.33	20.5 (18)	19.5 (17)	20 (17.5)	20 (17.5)	19.5 (17)	19.5 (17)	19 (16.5)	18 (15.5)
16.7	20 (17.5)	19 (16.5)	19.5 (17)	19 (16.5)	19 (16.5)	19 (16.5)	18 (15.5)	17 (14.5)
33.2	19 (16.5)	18.5 (16)	19 (16.5)	19 (16.5)	18.5 (16)	18.5 (16)	17.5 (15)	17 (14.5)
62	19 (16.5)	18 (15.5)	18.5 (16)	18.5 (16)	18 (15.5)	18 (15.5)	17.5 (15)	16.5 (14)
123	18 (15.5)	17.5 (15)	18 (15.5)	17.5 (15)	17 (14.5)	17 (14.5)	16.5 (14)	15.5 (13)
242	17 (14.5)	16.5 (14)	17 (14.5)	17 (14.5)	16.5 (14)	17 (14.5)	16 (13.5)	15 (12.5)
470	17 (14.5)	16.5 (14)	16 (13.5)	16.5 (14)	16 (13.5)	16.5 (14)	15.5 (13)	14.5 (12)

Table 13.

Effective Resolution (Bits) vs. Gain and Output Update Rate for the AD7795 Using an Internal 1.17 V Reference with Chop Disabled

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
8.33	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)
16.7	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)	16 (14.5)
33.2	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15)	16 (14.5)
62	16 (16)	16 (15.5)	16 (16)	16 (16)	16 (15.5)	16 (15.5)	16 (15)	16 (14)
123	16 (15.5)	16 (15)	16 (15.5)	16 (15)	16 (14.5)	16 (14.5)	16 (14)	15.5 (13)
242	16 (14.5)	16 (14)	16 (14.5)	16 (14.5)	16 (14)	16 (14.5)	16 (13.5)	15 (12.5)
470	16 (14.5)	16 (14)	16 (13.5)	16 (14)	16 (13.5)	16 (14)	15.5 (13)	14.5 (12)

TYPICAL PERFORMANCE CHARACTERISTICS

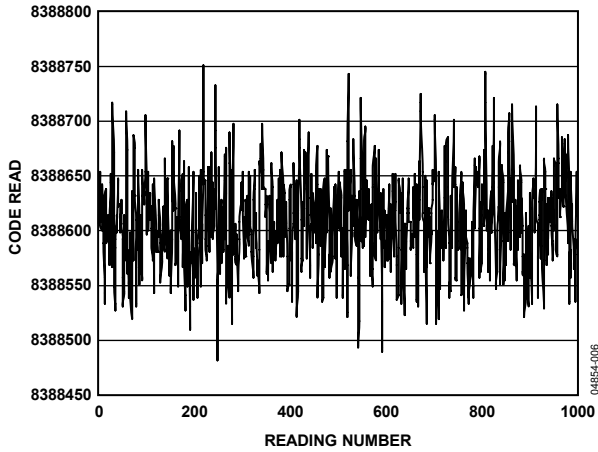


Figure 6. Typical Noise Plot for the AD7794 (Internal Reference, Gain = 64, Update Rate = 16.7 Hz, Chop Enabled)

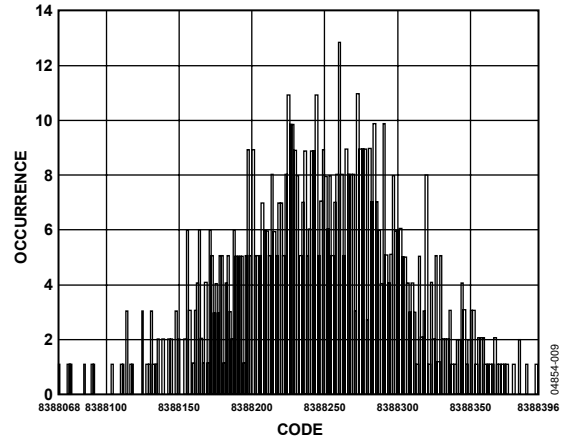


Figure 9. Noise Distribution Histogram for the AD7794 (Internal Reference, Gain = 64, Update Rate = 16.7 Hz, Chop Disabled, AMP-CM = 1)

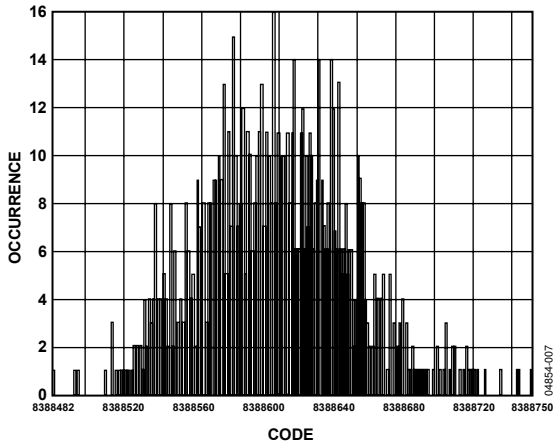


Figure 7. Noise Distribution Histogram for the AD7794 (Internal Reference, Gain = 64, Update Rate = 16.7 Hz, Chop Enabled)

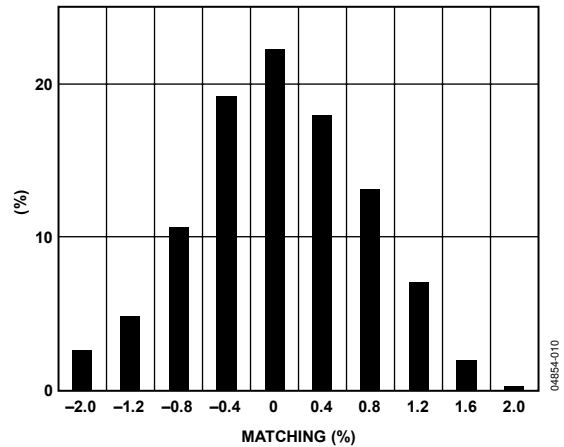


Figure 10. Excitation Current Matching (210 μ A) at Ambient Temperature

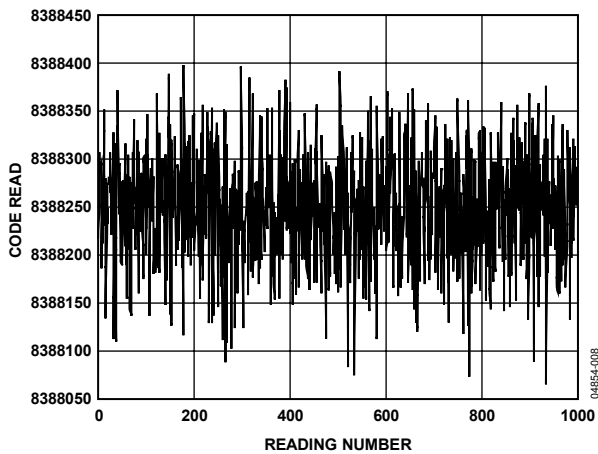


Figure 8. Typical Noise Plot for the AD7794 (Internal Reference, Gain = 64, Update Rate = 16.7 Hz, AMP-CM = 1, Chop Disabled)

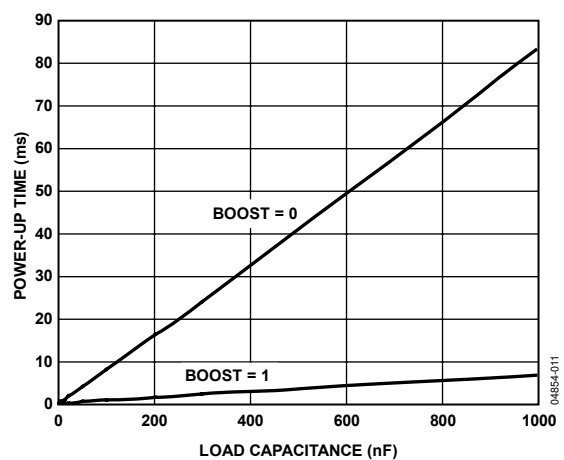


Figure 11. Bias Voltage Generator Power-Up Time vs. Load Capacitance

ON-CHIP REGISTERS

The ADC is controlled and configured via a number of on-chip registers that are described in the following sections. In the following descriptions, *set* implies a Logic 1 state and *cleared* implies a Logic 0 state, unless otherwise noted.

COMMUNICATIONS REGISTER

RS2, RS1, RS0 = 0, 0, 0

The communications register is an 8-bit write-only register. All communications to the part must start with a write operation to the communications register. The data written to the communications register determines whether the next operation is a read or write operation, and to which register this operation takes place. For read or write operations, once the subsequent read or write operation to the selected register is complete, the interface

returns to where it expects a write operation to the communications register. This is the default state of the interface and, on power-up or after a reset, the ADC is in this default state waiting for a write operation to the communications register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high returns the ADC to this default state by resetting the entire part. Table 14 outlines the bit designations for the communications register. CR0 through CR7 indicate the bit location, with CR denoting the bits are in the communications register. CR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
WEN(0)	R/W(0)	RS2(0)	RS1(0)	RS0(0)	CREAD(0)	0(0)	0(0)

Table 14. Communications Register Bit Designations

Bit No.	Mnemonic	Description
CR7	WEN	Write Enable Bit. A 0 must be written to this bit so that the write to the communications register actually occurs. If a 1 is the first bit written, the part does not clock on to subsequent bits in the register. It stays at this bit location until a 0 is written to this bit. Once a 0 is written to the WEN bit, the next seven bits are loaded to the communications register.
CR6	R/W	A 0 in this bit location indicates that the next operation is a write to a specified register. A 1 in this position indicates that the next operation is a read from the designated register.
CR5 to CR3	RS2 to RS0	Register Address Bits. These address bits are used to select which registers of the ADC are being selected during this serial interface communication. See Table 15.
CR2	CREAD	Continuous Read of the Data Register. When this bit is set to 1 (and the data register is selected), the serial interface is configured so that the data register can be read continuously, that is, the contents of the data register are automatically placed on the DOUT pin when the SCLK pulses are applied after the RDY pin goes low to indicate that a conversion is complete. The communications register does not have to be written to for data reads. To enable continuous read mode, the instruction 01011100 must be written to the communications register. To exit the continuous read mode, the instruction 01011000 must be written to the communications register while the RDY pin is low. While in continuous read mode, the ADC monitors activity on the DIN line so it can receive the instruction to exit continuous read mode. Additionally, a reset occurs if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is written to the device.
CR1 to CR0	0	These bits must be programmed to Logic 0 for correct operation.

Table 15. Register Selection

RS2	RS1	RS0	Register	Register Size
0	0	0	Communications Register During a Write Operation	8-bit
0	0	0	Status Register During a Read Operation	8-bit
0	0	1	Mode Register	16-bit
0	1	0	Configuration Register	16-bit
0	1	1	Data Register	24-bit (AD7794)/16-Bit (AD7795)
1	0	0	ID Register	8-bit
1	0	1	IO Register	8-bit
1	1	0	Offset Register	24-bit (AD7794)/16-Bit (AD7795)
1	1	1	Full-Scale Register	24-bit (AD7794)/16-Bit (AD7795)

AD7794/AD7795

STATUS REGISTER

RS2, RS1, RS0 = 0, 0, 0; Power-On/Reset = 0x80 (AD7795)/0x88 (AD7794)

The status register is an 8-bit read-only register. To access the ADC status register, the user must write to the communications register, select the next operation to be read, and load Bit RS2, Bit RS1, and Bit RS0 with 0.

Table 16 outlines the bit designations for the status register. SR0 through SR7 indicate the bit locations, with SR denoting that the bits are in the status register. SR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
RDY(1)	ERR(0)	NOXREF(0)	0(0)	0/1	CH2(0)	CH1(0)	CH0(0)

Table 16. Status Register Bit Designations

Bit No.	Mnemonic	Description
SR7	RDY	Ready Bit for ADC. <i>Cleared</i> when data is written to the ADC data register. The $\overline{\text{RDY}}$ bit is set automatically after the ADC data register has been read or a period of time before the data register is updated with a new conversion result to indicate to the user not to read the conversion data. It is also set when the part is placed in power-down mode. The end of a conversion is also indicated by the DOUT/ $\overline{\text{RDY}}$ pin. This pin can be used as an alternative to the status register for monitoring the ADC for conversion data.
SR6	ERR	ADC Error Bit. This bit is written to at the same time as the $\overline{\text{RDY}}$ bit. <i>Set</i> to indicate that the result written to the ADC data register has been clamped to all 0s or all 1s. Error sources include overrange, underrange, or the absence of a reference voltage. <i>Cleared</i> by a write operation to start a conversion.
SR5	NOXREF	No External Reference Bit. <i>Set</i> to indicate that the selected reference (REFIN1 or REFIN2) is at a voltage that is below a specified threshold. When set, conversion results are clamped to all 1s. <i>Cleared</i> to indicate that a valid reference is applied to the selected reference pins. The NOXREF bit is enabled by setting the REF_DET bit in the configuration register to 1. The ERR bit is also set if the voltage applied to the selected reference input is invalid.
SR4	0	This bit is automatically <i>cleared</i> .
SR3	0/1	This bit is automatically <i>cleared</i> on the AD7795 and is automatically <i>set</i> on the AD7794.
SR2 to SR0	CH2 to CH0	These bits indicate which channel is being converted by the ADC.

MODE REGISTER

RS2, RS1, RS0 = 0, 0, 1; Power-On/Reset = 0x000A

The mode register is a 16-bit read/write register that is used to select the operating mode, the update rate, and the clock source.

Table 17 outlines the bit designations for the mode register. MR0 through MR15 indicate the bit locations with MR

denoting that the bits are in the mode register. MR15 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit. Any write to the setup register resets the modulator and filter, and sets the $\overline{\text{RDY}}$ bit.

MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8
MD2(0)	MD1(0)	MD0(0)	PSW(0)	0(0)	0(0)	AMP-CM(0)	0(0)
MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
CLK1(0)	CLK0(0)	0(0)	CHOP-DIS(0)	FS3(1)	FS2(0)	FS1(1)	FS0(0)

Table 17. Mode Register Bit Designations

Bit No.	Mnemonic	Description															
MR15 to MR13 MR12	MD2 to MD0 PSW	Mode Select Bits. These bits select the operating mode of the AD7794/AD7795 (see Table 18). Power Switch Control Bit. <i>Set</i> by user to close the power switch PSW to GND. The power switch can sink up to 30 mA. <i>Cleared</i> by user to open the power switch. When the ADC is placed in power-down mode, the power switch is opened.															
MR11 to MR10 MR9	0 AMP-CM	These bits must be programmed with a Logic 0 for correct operation. Instrumentation Amplifier Common-Mode Bit. This bit is used in conjunction with the CHOP-DIS bit. With chop disabled, the user can operate with a wider range of common-mode voltages when AMP-CM is cleared. However, the dc common-mode rejection degrades. With AMP-CM set, the span for the common-mode voltage is reduced (see the Specifications section). However, the dc common-mode rejection is significantly better.															
MR8 MR7 to MR6	0 CLK1 to CLK0	This bit must be programmed with a Logic 0 for correct operation. These bits are used to select the clock source for the AD7794/AD7795. Either the on-chip 64 kHz clock can be used or an external clock can be used. The ability to use an external clock allows several AD7794/AD7795 devices to be synchronized. Also, 50 Hz/60 Hz rejection is improved when an accurate external clock drives the AD7794/AD7795.															
		<table border="1"> <thead> <tr> <th>CLK1</th> <th>CLK0</th> <th>ADC Clock Source</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Internal 64 kHz clock. Internal clock is not available at the CLK pin.</td> </tr> <tr> <td>0</td> <td>1</td> <td>Internal 64 kHz clock. This clock is made available at the CLK pin.</td> </tr> <tr> <td>1</td> <td>0</td> <td>External 64 kHz. The external clock can have a 45:55 duty cycle (see the Specifications section for the external clock).</td> </tr> <tr> <td>1</td> <td>1</td> <td>External clock. The external clock is divided by 2 within the AD7794/AD7795.</td> </tr> </tbody> </table>	CLK1	CLK0	ADC Clock Source	0	0	Internal 64 kHz clock. Internal clock is not available at the CLK pin.	0	1	Internal 64 kHz clock. This clock is made available at the CLK pin.	1	0	External 64 kHz. The external clock can have a 45:55 duty cycle (see the Specifications section for the external clock).	1	1	External clock. The external clock is divided by 2 within the AD7794/AD7795.
CLK1	CLK0	ADC Clock Source															
0	0	Internal 64 kHz clock. Internal clock is not available at the CLK pin.															
0	1	Internal 64 kHz clock. This clock is made available at the CLK pin.															
1	0	External 64 kHz. The external clock can have a 45:55 duty cycle (see the Specifications section for the external clock).															
1	1	External clock. The external clock is divided by 2 within the AD7794/AD7795.															
MR5 MR4	0 CHOP-DIS	This bit must be programmed with a Logic 0 for correct operation. This bit is used to enable or disable chop. On power-up or following a reset, CHOP-DIS is <i>cleared</i> so chop is enabled. When CHOP-DIS is <i>set</i> , chop is disabled. This bit is used in conjunction with the AMP-CM bit. When chop is disabled, the AMP-CM bit should be <i>set</i> . This limits the common-mode voltage that can be used by the ADC, but the dc common-mode rejection does not degrade.															
MR3 to MR0	FS3 to FS0	Filter Update Rate Select Bits (see Table 19).															

AD7794/AD7795

Table 18. Operating Modes

MD2	MD1	MD0	Mode
0	0	0	<p>Continuous Conversion Mode (Default).</p> <p>In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register. RDY goes low when a conversion is complete. The user can read these conversions by placing the device in continuous read mode whereby the conversions are automatically placed on the DOUT line when SCLK pulses are applied. Alternatively, the user can instruct the ADC to output the conversion by writing to the communications register. After power-on, the first conversion is available after a period of $2/f_{ADC}$ when chop is enabled or $1/f_{ADC}$ when chop is disabled. Subsequent conversions are available at a frequency of f_{ADC} with chop either enabled or disabled.</p>
0	0	1	<p>Single Conversion Mode.</p> <p>When single conversion mode is selected, the ADC powers up and performs a single conversion. The oscillator requires 1 ms to power up and settle. The ADC then performs the conversion, which takes a time of $2/f_{ADC}$ when chop is enabled, or $1/f_{ADC}$ when chop is disabled. The conversion result is placed in the data register, RDY goes low, and the ADC returns to power-down mode. The conversion remains in the data register and RDY remains active (low) until the data is read or another conversion is performed.</p>
0	1	0	<p>Idle Mode.</p> <p>In idle mode, the ADC filter and modulator are held in a reset state although the modulator clocks are still provided.</p>
0	1	1	<p>Power-Down Mode.</p> <p>In power-down mode, all the AD7794/AD7795 circuitry is powered down including the current sources, power switch, burnout currents, bias voltage generator, and clock circuitry.</p>
1	0	0	<p>Internal Zero-Scale Calibration.</p> <p>An internal short is automatically connected to the enabled channel. A calibration takes two conversion cycles to complete when chop is enabled and one conversion cycle when chop is disabled. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel.</p>
1	0	1	<p>Internal Full-Scale Calibration.</p> <p>A full-scale input voltage is automatically connected to the selected analog input for this calibration. When the gain equals 1, a calibration takes two conversion cycles to complete when chop is enabled and one conversion cycle when chop is disabled. For higher gains, four conversion cycles are required to perform the full-scale calibration when chop is enabled and 2 conversion cycles when chop is disabled. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. Internal full-scale calibrations cannot be performed when the gain equals 128. With this gain setting, a system full-scale calibration can be performed. A full-scale calibration is required each time the gain of a channel is changed to minimize the full-scale error.</p>
1	1	0	<p>System Zero-Scale Calibration.</p> <p>User should connect the system zero-scale input to the channel input pins as selected by the CH2 bit, CH1 bit, and CH0 bit. A system offset calibration takes two conversion cycles to complete when chop is enabled and one conversion cycle when chop is disabled. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel.</p>
1	1	1	<p>System Full-Scale Calibration.</p> <p>User should connect the system full-scale input to the channel input pins as selected by the CH2 bit, CH1 bit, and CH0 bit. A calibration takes two conversion cycles to complete when chop is enabled and one conversion cycle when chop is disabled. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. A full-scale calibration is required each time the gain of a channel is changed.</p>

Table 19. Update Rates Available (Chop Enabled)¹

FS3	FS2	FS1	FS0	f _{ADC} (Hz)	T _{SETTLE} (ms)	Rejection @ 50 Hz/60 Hz (Internal Clock)
0	0	0	0	x	x	
0	0	0	1	470	4	
0	0	1	0	242	8	
0	0	1	1	123	16	
0	1	0	0	62	32	
0	1	0	1	50	40	
0	1	1	0	39	48	
0	1	1	1	33.2	60	
1	0	0	0	19.6	101	90 dB (60 Hz only)
1	0	0	1	16.7	120	80 dB (50 Hz only)
1	0	1	0	16.7	120	65 dB (50 Hz and 60 Hz)
1	0	1	1	12.5	160	66 dB (50 Hz and 60 Hz)
1	1	0	0	10	200	69 dB (50 Hz and 60 Hz)
1	1	0	1	8.33	240	70 dB (50 Hz and 60 Hz)
1	1	1	0	6.25	320	72 dB (50 Hz and 60 Hz)
1	1	1	1	4.17	480	74 dB (50 Hz and 60 Hz)

¹ With chop disabled, the update rates remain unchanged, but the settling time for each update rate is reduced by a factor of 2. The rejection at 50 Hz/60 Hz for a 16.6 Hz update rate degrades to 60 dB.

AD7794/AD7795

CONFIGURATION REGISTER

RS2, RS1, RS0 = 0, 1, 0; Power-On/Reset = 0x0710

The configuration register is a 16-bit read/write register that is used to configure the ADC for unipolar or bipolar mode, enable or disable the buffer, enable or disable the burnout currents, select the gain, and select the analog input channel.

Table 20 outlines the bit designations for the filter register.

CON0 through CON15 indicate the bit locations. CON denotes that the bits are in the configuration register. CON15 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

CON15	CON14	CON13	CON12	CON11	CON10	CON9	CON8
VBIAS1(0)	VBIAS0(0)	BO(0)	U/B(0)	BOOST(0)	G2(1)	G1(1)	G0(1)
CON7	CON6	CON5	CON4	CON3	CON2	CON1	CON0
REFSEL1(0)	REFSELO(0)	REF_DET(0)	BUF(1)	CH3(0)	CH2(0)	CH1(0)	CH0(0)

Table 20. Configuration Register Bit Designations

Bit No.	Mnemonic	Description																																													
CON15 to CON14	VBIAS1 to VBIAS0	Bias Voltage Generator Enable. The negative terminal of the analog inputs can be biased up to $AV_{DD}/2$. These bits are used in conjunction with the BOOST bit.																																													
		<table border="1"> <thead> <tr> <th>VBIAS1</th> <th>VBIAS0</th> <th>Bias Voltage</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Bias voltage generator disabled</td> </tr> <tr> <td>0</td> <td>1</td> <td>Bias voltage generator connected to AIN1(-)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Bias voltage generator connected to AIN2(-)</td> </tr> <tr> <td>1</td> <td>1</td> <td>Bias voltage generator connected to AIN3(-)</td> </tr> </tbody> </table>	VBIAS1	VBIAS0	Bias Voltage	0	0	Bias voltage generator disabled	0	1	Bias voltage generator connected to AIN1(-)	1	0	Bias voltage generator connected to AIN2(-)	1	1	Bias voltage generator connected to AIN3(-)																														
		VBIAS1	VBIAS0	Bias Voltage																																											
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1	0	Bias voltage generator connected to AIN2(-)																																													
1	1	Bias voltage generator connected to AIN3(-)																																													
CON13	BO	Burnout Current Enable Bit. This bit must be programmed with a Logic 0 for correct operation. When this bit is set to 1 by the user, the 100 nA current sources in the signal path are enabled. When BO = 0, the burnout currents are disabled. The burnout currents can be enabled only when the buffer or in-amp is active.																																													
CON12	U/B	Unipolar/Bipolar Bit. Set by user to enable unipolar coding, that is, zero differential input results in 0x000000 output and a full-scale differential input results in 0xFFFF output. Cleared by the user to enable bipolar coding. Negative full-scale differential input results in an output code of 0x000000, zero differential input results in an output code of 0x800000, and positive full-scale differential input results in an output code of 0xFFFF.																																													
CON11	BOOST	This bit is used in conjunction with the VBIAS1 and VBIAS0 bits. When set, the current consumed by the bias voltage generator is increased, which reduces its power-up time.																																													
CON10 to CON8	G2 to G0	Gain Select Bits. Written by the user to select the ADC input range as follows:																																													
		<table border="1"> <thead> <tr> <th>G2</th> <th>G1</th> <th>G0</th> <th>Gain</th> <th>ADC Input Range (2.5 V Reference)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1 (in-amp not used)</td> <td>2.5 V</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>2 (in-amp not used)</td> <td>1.25 V</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>4</td> <td>625 mV</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>8</td> <td>312.5 mV</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>16</td> <td>156.2 mV</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>32</td> <td>78.125 mV</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>64</td> <td>39.06 mV</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>128</td> <td>19.53 mV</td> </tr> </tbody> </table>	G2	G1	G0	Gain	ADC Input Range (2.5 V Reference)	0	0	0	1 (in-amp not used)	2.5 V	0	0	1	2 (in-amp not used)	1.25 V	0	1	0	4	625 mV	0	1	1	8	312.5 mV	1	0	0	16	156.2 mV	1	0	1	32	78.125 mV	1	1	0	64	39.06 mV	1	1	1	128	19.53 mV
		G2	G1	G0	Gain	ADC Input Range (2.5 V Reference)																																									
		0	0	0	1 (in-amp not used)	2.5 V																																									
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CON7 to CON6	REFSEL1/REFSELO	Reference Select Bits. The reference source for the ADC is selected using these bits.																																													
		<table border="1"> <thead> <tr> <th>REFSEL1</th> <th>REFSELO</th> <th>Reference Source</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>External reference applied between REFIN1(+) and REFIN1(-)</td> </tr> <tr> <td>0</td> <td>1</td> <td>External reference applied between REFIN2(+) and REFIN2(-)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Internal 1.17 V reference</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> </tbody> </table>	REFSEL1	REFSELO	Reference Source	0	0	External reference applied between REFIN1(+) and REFIN1(-)	0	1	External reference applied between REFIN2(+) and REFIN2(-)	1	0	Internal 1.17 V reference	1	1	Reserved																														
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Bit No.	Mnemonic	Description																																																																																																
CON5	REF_DET	Enables the reference detect function. When <i>set</i> , the NOXREF bit in the status register indicates when the external reference being used by the ADC is open circuit or less than 0.5 V. When <i>cleared</i> , the reference detect function is disabled.																																																																																																
CON4	BUF	Configures the ADC for buffered or unbuffered mode of operation. If <i>cleared</i> , the ADC operates in unbuffered mode, lowering the power consumption of the device. If <i>set</i> , the ADC operates in buffered mode, allowing the user to place source impedances on the front end without contributing gain errors to the system. For gains of 1 and 2, the buffer can be enabled or disabled. For higher gains, the buffer is automatically enabled. With the buffer disabled, the voltage on the analog input pins can be from 30 mV below GND to 30 mV above AV _{DD} . When the buffer is enabled, it requires some headroom so the voltage on any input pin must be limited to 100 mV within the power supply rails.																																																																																																
CON3 to CON0	CH3 to CH0	Channel Select Bits. Written by the user to select the active analog input channel to the ADC.																																																																																																
		<table border="1"> <thead> <tr> <th>CH3</th> <th>CH2</th> <th>CH1</th> <th>CH0</th> <th>Channel</th> <th>Calibration Pair</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>AIN1(+)/AIN1(-)</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>AIN2(+)/AIN2(-)</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>AIN3(+)/AIN3(-)</td> <td>2</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>AIN4(+)/AIN4(-)</td> <td>3</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>AIN5(+)/AIN5(-)</td> <td>3</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>AIN6(+)/AIN6(-)</td> <td>3</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>Temp Sensor</td> <td>Automatically selects the internal 1.17 V reference and sets the gain to 1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>AV_{DD} Monitor</td> <td>Automatically selects the internal 1.17 V reference and sets the gain to 1/6</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>AIN1(-)/AIN1(-)</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>Reserved</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>Reserved</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>Reserved</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>Reserved</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>Reserved</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	CH3	CH2	CH1	CH0	Channel	Calibration Pair	0	0	0	0	AIN1(+)/AIN1(-)	0	0	0	0	1	AIN2(+)/AIN2(-)	1	0	0	1	0	AIN3(+)/AIN3(-)	2	0	0	1	1	AIN4(+)/AIN4(-)	3	0	1	0	0	AIN5(+)/AIN5(-)	3	0	1	0	1	AIN6(+)/AIN6(-)	3	0	1	1	0	Temp Sensor	Automatically selects the internal 1.17 V reference and sets the gain to 1	0	1	1	1	AV _{DD} Monitor	Automatically selects the internal 1.17 V reference and sets the gain to 1/6	1	0	0	0	AIN1(-)/AIN1(-)	0	1	0	0	1	Reserved		1	0	1	1	Reserved		1	1	0	0	Reserved		1	1	0	1	Reserved		1	1	1	0	Reserved		1	1	1	1	Reserved	
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AD7794/AD7795

DATA REGISTER

RS2, RS1, RS0 = 0, 1, 1; Power-On/Reset = 0x0000(AD7795), 0x000000 (AD7794)

The conversion result from the ADC is stored in this data register. This is a read-only register. On completion of a read operation from this register, the RDY bit/pin is set.

ID REGISTER

RS2, RS1, RS0 = 1, 0, 0; Power-On/Reset = 0xXF

The identification number for the AD7794/AD7795 is stored in the ID register. This is a read-only register.

IO REGISTER

RS2, RS1, RS0 = 1, 0, 1; Power-On/Reset = 0x00

The IO register is an 8-bit read/write register that is used to enable the excitation currents and select the value of the excitation currents.

Table 21 outlines the bit designations for the IO register. IO0 through IO7 indicate the bit locations. IO denotes that the bits are in the IO register. IO7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
0(0)	IOEN(0)	IO2DAT(0)	IO1DAT(0)	IEXCDIR1(0)	IEXCDIR0(0)	IEXCEN1(0)	IEXCEN0(0)

Table 21. IO Register Bit Designations

Bit No.	Mnemonic	Description															
IO7	0	This bit must be programmed with a Logic 0 for correct operation.															
IO6	IOEN	Configures Pin AIN6(+)/P1 and Pin AIN6(-)/P2 as analog input pins or digital output pins. When this bit is <i>set</i> , the pins are configured as Digital Output Pin P1 and Digital Output Pin P2. When this bit is <i>cleared</i> , these pins are configured as Analog Input Pin AIN6(+) and Analog Input Pin AIN6(-).															
IO5 to IO4	IO2DAT/IO1DAT	P2/P1 Data. When IOEN is <i>set</i> , the data for Digital Output Pin P1 and Digital Output Pin P2 is written to Bit IO2DAT and Bit IO1DAT.															
IO3 to IO2	IEXCDIR1 to IEXCDIR0	Direction of Current Sources Select Bits.															
		<table border="1"> <thead> <tr> <th>IEXCDIR1</th> <th>IEXCDIR0</th> <th>Current Source Direction</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Current Source IEXC1 connected to Pin IOUT1. Current Source IEXC2 connected to Pin IOUT2.</td> </tr> <tr> <td>0</td> <td>1</td> <td>Current Source IEXC1 connected to Pin IOUT2. Current Source IEXC2 connected to Pin IOUT1.</td> </tr> <tr> <td>1</td> <td>0</td> <td>Both current sources connected to Pin IOUT1. Permitted only when the current sources are set to 10 μA or 210 μA.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Both current sources connected to Pin IOUT2. Permitted only when the current sources are set to 10 μA or 210 μA.</td> </tr> </tbody> </table>	IEXCDIR1	IEXCDIR0	Current Source Direction	0	0	Current Source IEXC1 connected to Pin IOUT1. Current Source IEXC2 connected to Pin IOUT2.	0	1	Current Source IEXC1 connected to Pin IOUT2. Current Source IEXC2 connected to Pin IOUT1.	1	0	Both current sources connected to Pin IOUT1. Permitted only when the current sources are set to 10 μ A or 210 μ A.	1	1	Both current sources connected to Pin IOUT2. Permitted only when the current sources are set to 10 μ A or 210 μ A.
IEXCDIR1	IEXCDIR0	Current Source Direction															
0	0	Current Source IEXC1 connected to Pin IOUT1. Current Source IEXC2 connected to Pin IOUT2.															
0	1	Current Source IEXC1 connected to Pin IOUT2. Current Source IEXC2 connected to Pin IOUT1.															
1	0	Both current sources connected to Pin IOUT1. Permitted only when the current sources are set to 10 μ A or 210 μ A.															
1	1	Both current sources connected to Pin IOUT2. Permitted only when the current sources are set to 10 μ A or 210 μ A.															
IO3 to IO2	IEXCEN1 to IEXCEN0	These bits are used to enable and disable the current sources. They also select the value of the excitation currents.															
		<table border="1"> <thead> <tr> <th>IEXCEN1</th> <th>IEXCEN0</th> <th>Current Source Value</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Excitation currents disabled</td> </tr> <tr> <td>0</td> <td>1</td> <td>10 μA</td> </tr> <tr> <td>1</td> <td>0</td> <td>210 μA</td> </tr> <tr> <td>1</td> <td>1</td> <td>1 mA</td> </tr> </tbody> </table>	IEXCEN1	IEXCEN0	Current Source Value	0	0	Excitation currents disabled	0	1	10 μ A	1	0	210 μ A	1	1	1 mA
IEXCEN1	IEXCEN0	Current Source Value															
0	0	Excitation currents disabled															
0	1	10 μ A															
1	0	210 μ A															
1	1	1 mA															

OFFSET REGISTER

RS2, RS1, RS0 = 1, 1, 0; Power-On/Reset = 0x8000 (AD7795), 0x800000 (AD7794)

The offset register is a 16-bit register on the AD7795 and a 24-bit register on the AD7794. The offset register holds the offset calibration coefficient for the ADC and its power-on reset value is 0x8000/0x800000, for the AD7794/AD7795, respectively. The AD7794/AD7795 each have four offset registers. Channel AIN1 to Channel AIN3 have dedicated offset registers while the AIN4, AIN5, and AIN6 channels share an offset register. Each of these registers is a read/write register. The register is used in conjunction with its associated full-scale register to form a register pair. The power-on reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user. The AD7794/AD7795 must be placed in power-down mode or idle mode when writing to the offset register.

FULL-SCALE REGISTER

RS2, RS1, RS0 = 1, 1, 1; Power-On/Reset = 0x5XXX (AD7795), 0x5XXX00 (AD7794)

The full-scale register is a 16-bit register on the AD7795 and a 24-bit register on the AD7794. The full-scale register holds the full-scale calibration coefficient for the ADC. The AD7794/AD7795 each have four full-scale registers. The AIN1, AIN2, and AIN3 channels have dedicated full-scale registers, while the AIN4, AIN5, and AIN6 channels share a register. The full-scale registers are read/write registers. However, when writing to the full-scale registers, the ADC must be placed in power-down mode or idle mode. These registers are configured on power-on with factory calibrated full-scale calibration coefficients, the calibration being performed at gain = 1. Therefore, every device has different default coefficients. The coefficients are different, depending on whether the internal reference or an external reference is selected. The default value is automatically overwritten if an internal or system full-scale calibration is initiated by the user or the full-scale register is written to.