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Touch Screen Controller

Data Sheet

AD7877

FEATURES

- 4-wire touch screen interface
- LCD noise reduction feature (STOPACQ pin)
- Automatic conversion sequencer and timer
- User-programmable conversion parameters
- On-chip temperature sensor: −40°C to +85°C
- On-chip 2.5 V reference
- On-chip 8-bit DAC
- 3 auxiliary analog inputs
- 1 dedicated and 3 optional GPIOs
- 2 direct battery measurement channels (0.5 V to 5 V)
- 3 interrupt outputs
- Touch-pressure measurement
- Wake up on touch function
- Specified throughput rate of 125 kSPS
- Single supply, V_{CC} of 2.7 V to 5.25 V
- Separate V_{DRIVE} level for serial interface
- Shutdown mode: 1 µA maximum
- 32-lead, LFCSP, 5 mm × 5 mm package
- 25-ball,WLCSP, 2.5 mm × 2.8 mm package
- Qualified for automotive applications

APPLICATIONS

- Personal digital assistants
- Smart hand-held devices
- Touch screen monitors
- Point-of-sale terminals
- Medical devices
- Cell phones
- Pagers

FUNCTIONAL BLOCK DIAGRAM

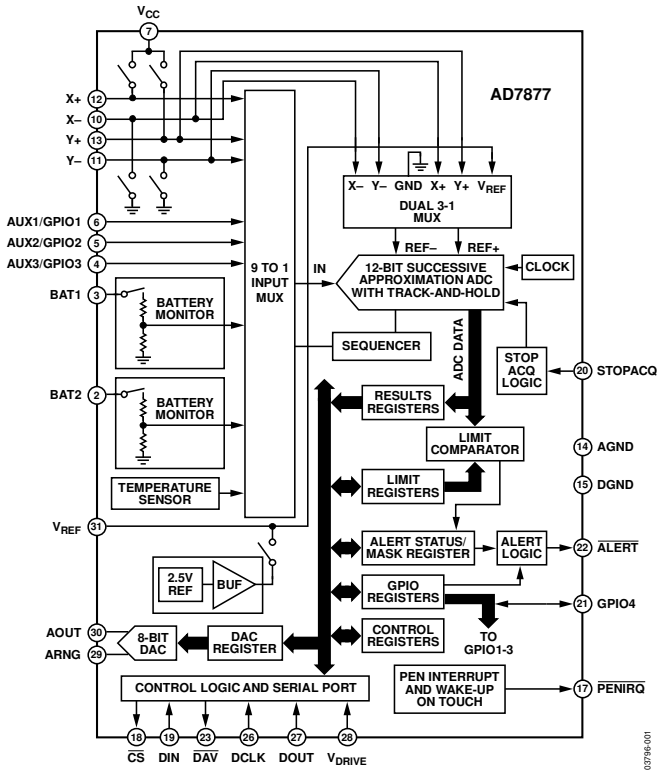

Figure 1.

GENERAL DESCRIPTION

The AD7877 is a 12-bit, successive approximation ADC with a synchronous serial interface and low on resistance switches for driving touch screens. The AD7877 operates from a single 2.7 V to 5.25 V power supply (functional operation to 2.2 V), and features throughput rates of 125 kSPS. The AD7877 features direct battery measurement on two inputs, temperature and touch-pressure measurement.

The AD7877 also has an on-board reference of 2.5 V. When not in use, it can be shut down to conserve power. An external reference can also be applied and varied from 1 V to $+V_{CC}$, with an analog input range of 0 V to V_{REF}. The device includes a shutdown mode that reduces its current consumption to less than 1 µA.

To reduce the effects of noise from LCDs, the acquisition phase of the on-board ADC is controlled via the STOPACQ pin. User-programmable conversion controls include variable acquisition time and first conversion delay. Up to 16 averages can be taken per conversion. There is also an on-board DAC for LCD back-light or contrast control. The AD7877 runs in either slave or master mode using a conversion sequencer and timer. It is ideal for battery-powered systems such as personal digital assistants with resistive touch screens and other portable equipment.

The part is available in a 32-lead lead frame chip scale package (LFCSP), and a 25-ball wafer level chip scale package (WLCSP).

Rev. E Document Feedback

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AD7877* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-738: Using the AD7877 Touch Screen Controller and the Intel PXA250 Processor Under Windows CE.NET
- AN-753: Configuring the AD7877
- AN-766: Using the Noise Reduction Feature on the AD7877

Data Sheet

- AD7877: Touch Screen Controller Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD7877 Input Touch Screen Controller Linux Driver

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD7877 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7877 EngineerZone Discussions.

SAMPLE AND BUY

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TABLE OF CONTENTS

REVISION HISTORY

12/14—Rev. D to Rev. E

Added Figure 50; Renumbered Sequentially ... 44
Updated Outline Dimensions ... 44
Changes to Ordering Guide ... 45

12/11—Rev. C to Rev. D

Change to Features Section ... 1
Updated Outline Dimensions ... 44
Changes to Ordering Guide ... 44
Added Automotive Products Section ... 44

9/09—Rev. B to Rev. C

Changes to Offset Error and Gain Error Parameters ... 3
Added V_{BAT} to GND Parameter ... 6
Changes to Pin 23 Description ... 7
Changes to Power Management (Control Register 2, Bits[7:6]) Section ... 22
Changes to Bit 7 Description (Table 17) ... 36
Updated Outline Dimensions ... 44
Changes Ordering Guide ... 44

6/06—Rev. A to Rev. B

Added Wafer Level Chip Scale Package ... Universal
Changes to Table 3 ... 6
Changes to Figure 21 ... 11
Change to Figure 25 ... 12
Changes to Figure 38 and Figure 39 ... 23
Change to Figure 40 ... 24
Changes to Data Available Output ($\overline{DAV}$) Section ... 24
Updated Outline Dimensions ... 42
Changes to Ordering Guide ... 42

11/04—Rev. 0 to Rev. A

Changes to Absolute Maximum Ratings ... 6
Changes to Figure 4 ... 7
Changes to Table 4 ... 7
Changes to Grounding and Layout section ... 32
Changes to Figure 42 ... 32
Changes to Ordering Guide ... 43

7/04—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 2.7 V to 3.6 V, V_{REF} = 2.5 V internal or external, f_{DCLK} = 2 MHz, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC ACCURACY					
Resolution	12			Bits	
No Missing Codes	11	12		Bits	
Integral Nonlinearity (INL)[1]			±2	LSB	LSB size = 610 µV
Differential Nonlinearity (DNL)[1]					Minimum LSB size = 610 µV
Negative DNL			−0.99	LSB	
Positive DNL			+2	LSB	
Offset Error[1]		±5		LSB	Specified for 11bits
Gain Error[1]		±3		LSB	Specified for 11 bits; external reference
Noise		70		µV rms	
Power Supply Rejection		70		dB	
Internal Clock Frequency		2		MHz	
SWITCH DRIVERS					
On Resistance[1]					
Y+, X+		14		Ω	
Y−, X−		14		Ω	
ANALOG INPUTS					
Input Voltage Ranges	0		V_{REF}	V	
DC Leakage Current		±0.1		µA	
Input Capacitance		30		pF	
Accuracy		0.3		%	All channels, internal V_{REF}
REFERENCE INPUT/OUTPUT					
Internal Reference Voltage	2.44		2.55	V	
Internal Reference Tempco		±50		ppm/°C	
V_{REF} Input Voltage Range	1		V_{CC}	V	
DC Leakage Current			±1	µA	
V_{REF} Input Impedance		1		GΩ	$\overline{CS}$ = GND or V_{CC}; typically 25 Ω when the on-board reference is enabled
TEMPERATURE MEASUREMENT					
Temperature Range	−40		+85	°C	
Resolution					
Differential Method[2]		1.6		°C	
Single Conversion Method[3]		0.3		°C	
Accuracy					
Differential Method[2]		±4		°C	0°C to 70°C
Single Conversion Method[3]		±2		°C	Calibrated at 25°C
BATTERY MONITOR					
Input Voltage Range	0.5		5	V	@ V_{REF} = 2.5 V
Input Impedance		14		kΩ	Sampling, 1 GΩ when the battery monitor is off
Accuracy		1	3.2	%	External/internal reference, see Figure 26

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DAC					
Resolution		8		Bits	
Integral Nonlinearity		±1		Bits	
Differential Nonlinearity		±1			Guaranteed monotonic by design
Voltage Mode					
Output Voltage Range		0 – V_{CC}/2		V	DAC register Bit 2 = 0, Bit 0 = 0
		0 – V_{CC}		V	DAC register Bit 2 = 0, Bit 0 = 1
Slew Rate		−0.4, +0.5		V/µs	
Output Settling Time		12	15	µs	0 to 3/4 scale, R_{LOAD} = 10 kΩ, C_{LOAD} = 50 pF
Capacitive Load Stability		50	100	pF	R_{LOAD} = 10 kΩ
Output Impedance		75		kΩ	Power-down mode
Short-Circuit Current		21		mA	
Current Mode					
Output Current Range	0		1000	µA	DAC register, Bit 2 = 1; full-scale current is set by R_{RNG}
Output Impedance			Open		Power-down mode
LOGIC INPUTS					
Input High Voltage, V_{INH}	0.7 V_{DRIVE}			V	
Input Low Voltage, V_{INL}			0.3 V_{DRIVE}	V	
Input Current, I_{IN}			±1	µA	Typically 10 nA, V_{IN} = 0 V or V_{CC}
Input Capacitance, C_{IN}[4]			10	pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2			V	I_{SOURCE} = 250 µA, V_{CC}/V_{DRIVE} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 250 µA
Floating-State Leakage Current			±10	µA	
Floating-State Output Capacitance[4]			10	pF	
Output Coding					Straight (natural) binary
CONVERSION RATE					
Conversion Time		8		µs	$\overline{CS}$ high to $\overline{DAV}$ low
Throughput Rate		125		kSPS	
POWER REQUIREMENTS					
V_{CC} (Specified Performance)	2.7		3.6	V	Functional from 2.2 V to 5.25 V
V_{DRIVE}	1.65		V_{CC}	V	
I_{CC}					Digital inputs = 0 V or V_{CC}
Converting Mode		240	380	µA	ADC on, internal reference off, V_{CC} = 3.6 V
		650	900	µA	ADC on, internal reference on, V_{CC} = 3.6 V
		900		µA	ADC on, internal reference on, DAC on
Static		150		µA	ADC on, but not converting, internal reference off, V_{CC} = 3.6 V
Shutdown Mode			1	µA	

[1] See the Terminology section.
[2] Difference between Temp0 and Temp1 measurement. No calibration necessary.
[3] Temperature drift is −2.1 mV/°C.
[4] Sample tested @ 25°C to ensure compliance.

TIMING SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted, V_{CC} = 2.7 V to 5.25 V, V_{REF} = 2.5 V. Sample tested at 25°C to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.6 V.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{DCLK}[1]	10	kHz min	
	20	MHz max	
t_1	16	ns min	$\overline{CS}$ falling edge to first DCLK rising edge
t_2	20	ns min	DCLK high pulse width
t_3	20	ns min	DCLK low pulse width
t_4	12	ns min	DIN setup time
t_5	12	ns min	DIN hold time
t_6[2]	16	ns max	$\overline{CS}$ falling edge to DOUT, three-state disabled
t_7[2]	16	ns max	DCLK falling edge to DOUT valid
t_8[3]	16	ns max	$\overline{CS}$ rising edge to DOUT high impedance
t_9	0	ns min	$\overline{CS}$ rising edge to DCLK ignored

[1] Mark/space ratio for the DCLK input is 40/60 to 60/40.
[2] Measured with the load circuit of Figure 3 and defined as the time required for the output to cross 0.4 V or 2.0 V.
[3] t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit shown in Figure 3. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

TIMING DIAGRAMS

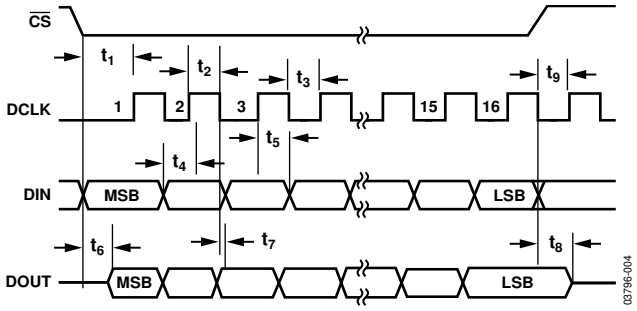

Figure 2. Detailed Timing Diagram

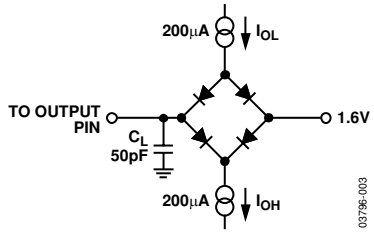

Figure 3. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{CC} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{CC} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{CC} + 0.3 V
V_{REF} to GND	−0.3 V to V_{CC} + 0.3 V
V_{BAT} to GND	−0.3 V to V_{CC} +5 V
Input Current to Any Pin Except Supplies[1]	10 mA
ESD Rating (IEC 1000-4-2, Air Discharge)	
Tablet Pins (X+, X−, Y+, Y−)	4 kV
Other Pins	2 kV
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
LFCSP Package	
Power Dissipation	450 mW
θ_{JA} Thermal Impedance	135.7°C/W
IR Reflow Peak Temperature	220°C
Pb-Free Parts Only	260°C (±0.5°C)
Lead Temperature (Soldering 10 sec)	300°C

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

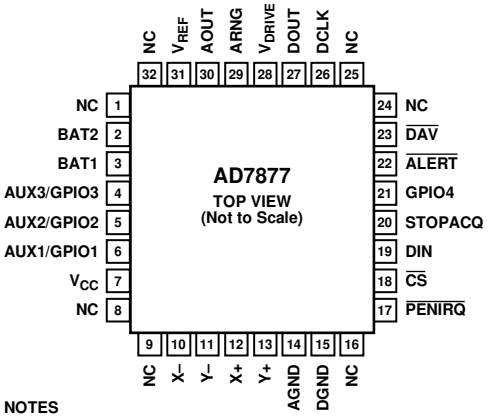

Figure 4. LFCSP Pin Configuration

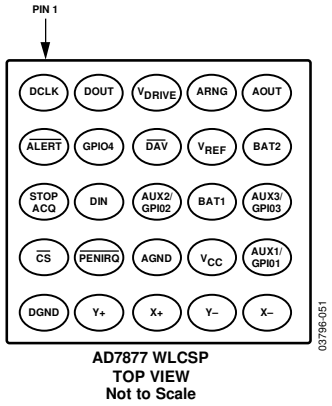

Figure 5. WLCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9, 16, 24, 25, 32	NC	No Connect.
2	BAT2	Battery Monitor Input. ADC Input Channel 7.
3	BAT1	Battery Monitor Input. ADC Input Channel 6.
4	AUX3/GPIO3	Auxiliary Analog Input. ADC Input Channel 5. Can be reconfigured as GPIO pin.
5	AUX2/GPIO2	Auxiliary Analog Input. ADC Input Channel 4. Can be reconfigured as GPIO pin.
6	AUX1/GPIO1	Auxiliary Analog Input. ADC Input Channel 3. Can be reconfigured as GPIO pin.
7	V_{CC}	Power Supply Input. The V_{CC} range for the AD7877 is from 2.2 V to 5.25 V.
10	X–	Touch Screen Position Input.
11	Y–	Touch Screen Position Input. ADC Input Channel 2.
12	X+	Touch Screen Position Input. ADC Input Channel 0.
13	Y+	Touch Screen Position Input. ADC Input Channel 1.
14	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7877. All analog input signals and any external reference signal should be referred to this voltage.
15	DGND	Digital Ground. Ground reference for all digital circuitry on the AD7877. Refer all digital input signals to this voltage.
17	$\overline{\text{PENIRQ}}$	Pen Interrupt. Digital active low output (has a 50 kΩ internal pull-up resistor).
18	$\overline{\text{CS}}$	Chip Select Input. Active low logic input. This input provides the dual function of initiating conversions on the AD7877 and enabling the serial input/output register.
19	DIN	SPI® Serial Data Input. Data to be written to the AD7877 registers are provided on this input and clocked into the register on the rising edge of DCLK.
20	STOPACQ	Stop Acquisition Pin. A signal applied to this pin can be monitored by the AD7877, so that acquisition of new data by the ADC is halted while the signal is active. Used to reduce the effect of noise from an LCD screen on the touch screen measurements.
21	GPIO4	Dedicated General-Purpose Logic Input/Output Pin.
22	$\overline{\text{ALERT}}$	Digital Active Low Output. Interrupt output that goes low if a GPIO data bit is set, or if the AUX1, TEMP1, BAT1, or BAT2 measurements are out of range.
23	$\overline{\text{DAV}}$	Data Available Output. Active low logic output. Asserts low when new data is available in the AD7877 results registers.
26	DCLK	External Clock Input. Logic input. DCLK provides the serial clock for accessing data from the part.
27	DOUT	Serial Data Output. Logic output. The conversion result from the AD7877 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the DCLK input. This output is high impedance when $\overline{\text{CS}}$ is high.

Pin No.	Mnemonic	Description
28	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines the operating voltage for the serial interface of the AD7877.
29	ARNG	When the DAC is in current output mode, a resistor from ARNG to GND sets the output range.
30	AOUT	Analog Output Voltage or Current from DAC.
31	V_{REF}	Reference Output for the AD7877. The internal 2.5 V reference is available on this pin for use external to the device. The reference output must be buffered before it is applied elsewhere in a system. To reduce system noise effects, it is strongly recommended to place a capacitor of 100 nF between the V_{REF} pin and GND. Alternatively, an external reference can be applied to this input. The voltage range for the external reference is 1.0 V to V_{CC}. For the specified performance, it is 2.5 V on the AD7877.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 2.7 V, V_{REF} = 2.5 V, f_{SAMPLE} = 125 kHz, f_{DCLK} = 16 × f_{SAMPLE} = 2 MHz, unless otherwise noted.

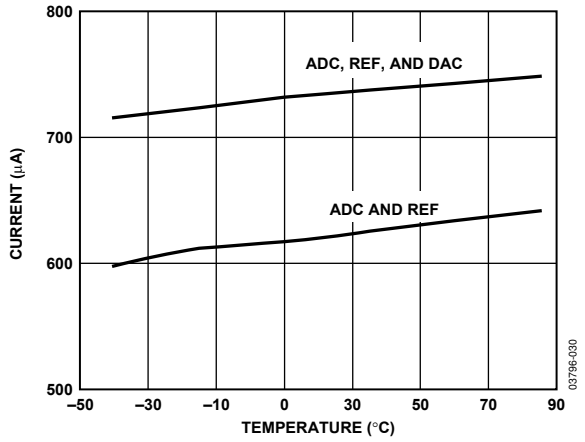

Figure 6. Supply Current vs. Temperature

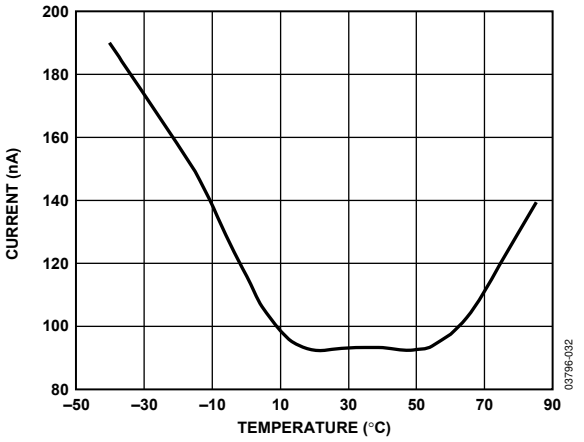

Figure 9. Full Power-Down I_{DD} vs. Temperature

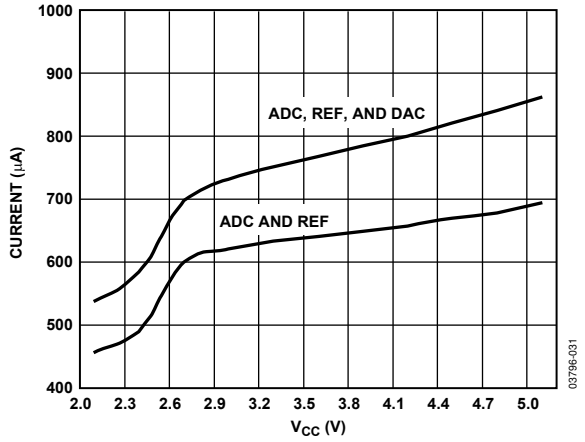

Figure 7. Supply Current vs. V_{CC}

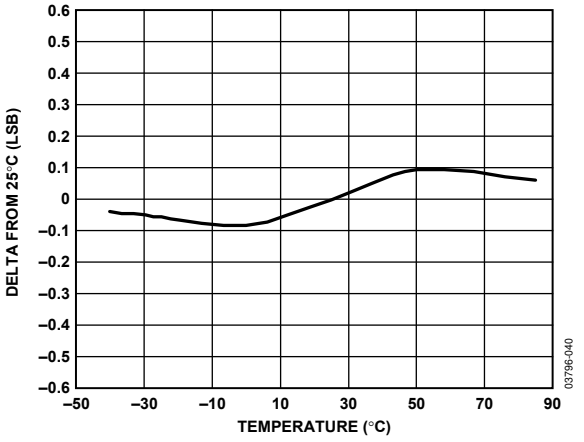

Figure 10. Change in ADC Offset vs. Temperature

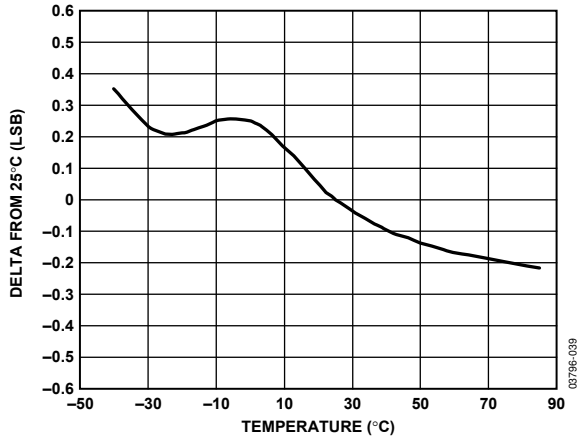

Figure 8. Change in ADC Gain vs. Temperature

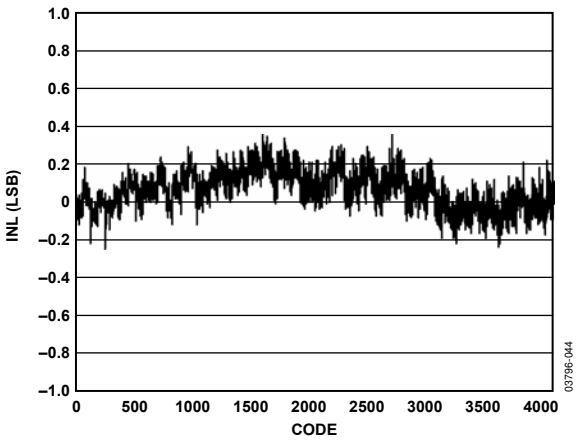

Figure 11. ACD INL Plot

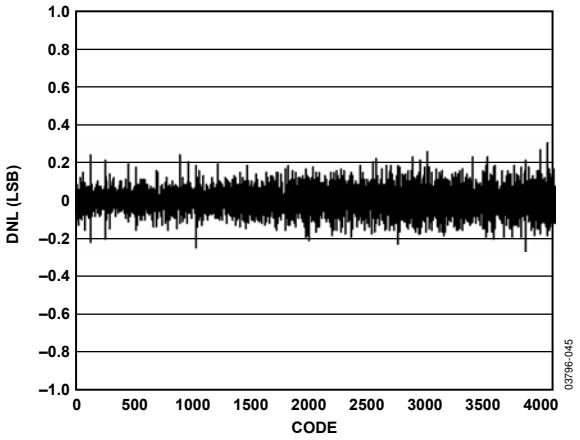

Figure 12. ADC DNL Plot

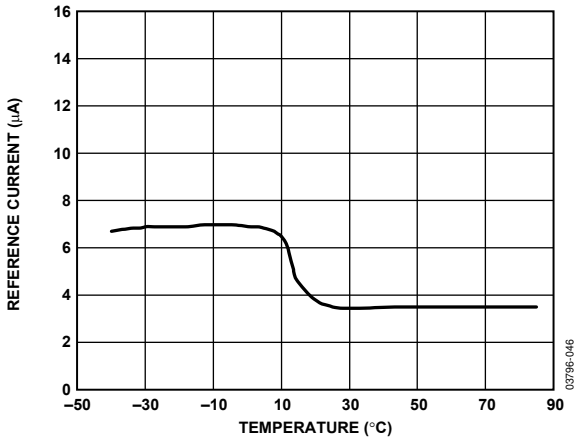

Figure 15. External Reference Current vs. Temperature

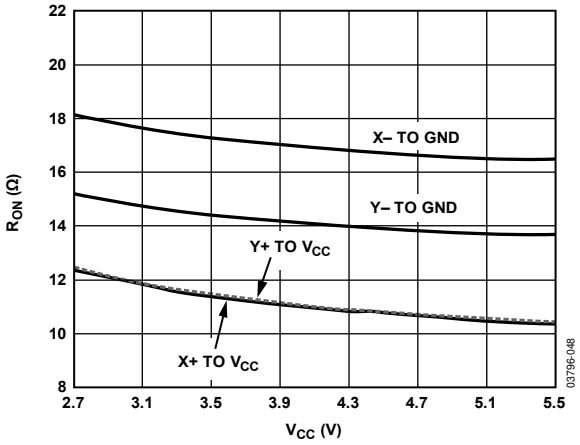

Figure 13. Switch On Resistance vs. V_{CC}
(X+, Y+: V_{CC} to Pin; X–, Y–: Pin to GND)

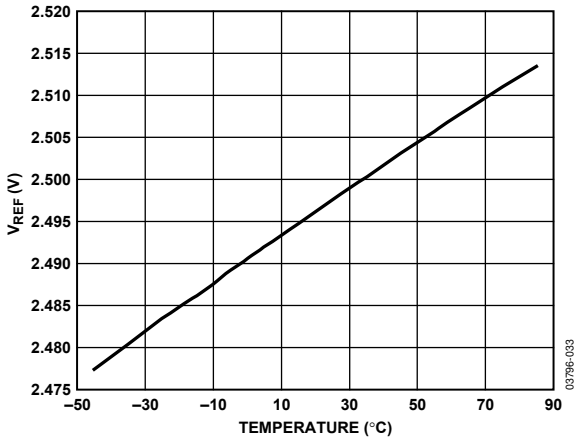

Figure 16. Internal V_{REF} vs. Temperature

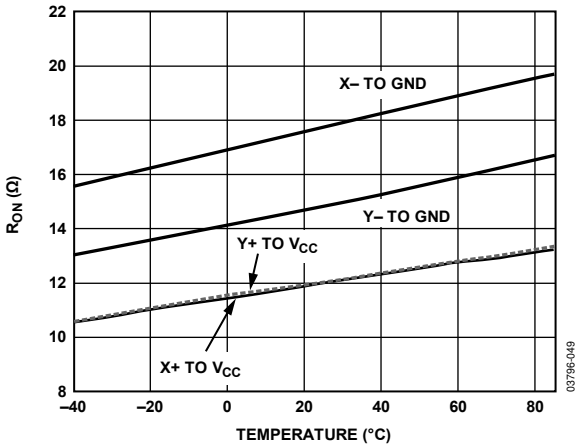

Figure 14. Switch On Resistance vs. Temperature
(X+, Y+: V_{CC} to Pin; X–, Y–: Pin to GND)

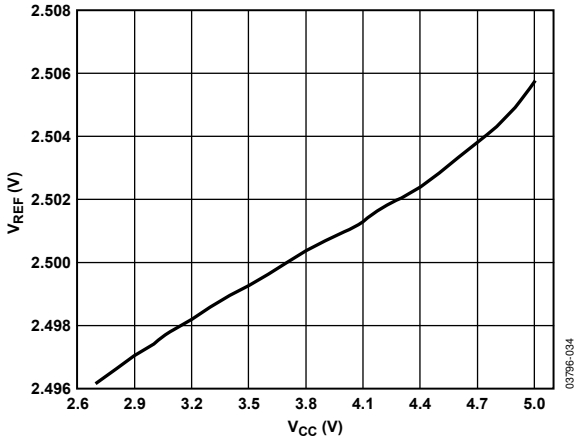

Figure 17. Internal V_{REF} vs. V_{CC}

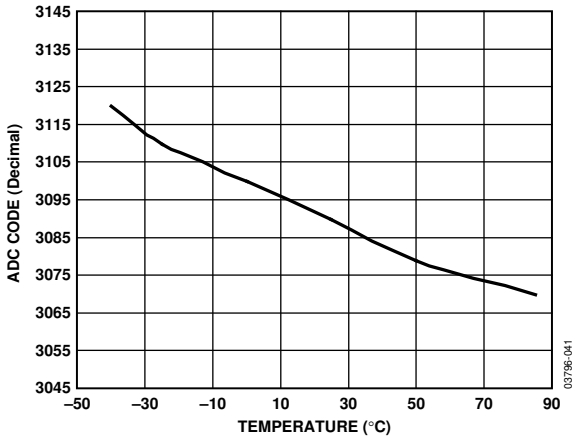

Figure 18. ADC Code vs. Temperature (2.7 V Supply)

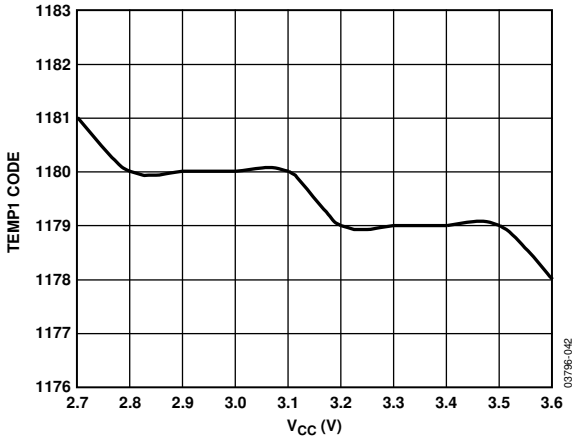

Figure 19. Temp1 vs. V_{CC}

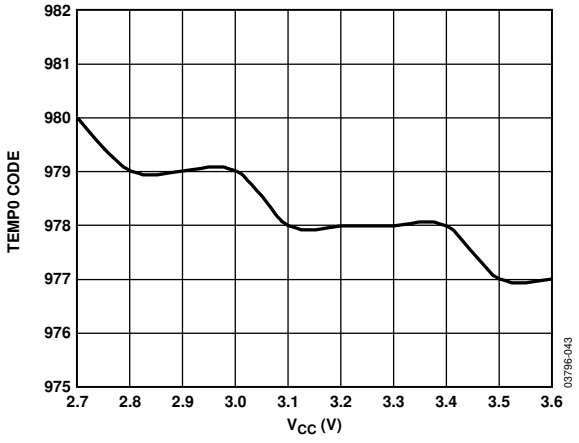

Figure 20. Temp0 vs. V_{CC}

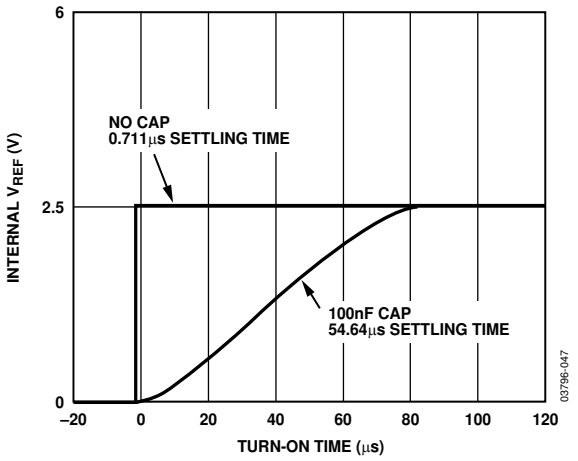

Figure 21. Internal V_{REF} vs. Turn-On Time

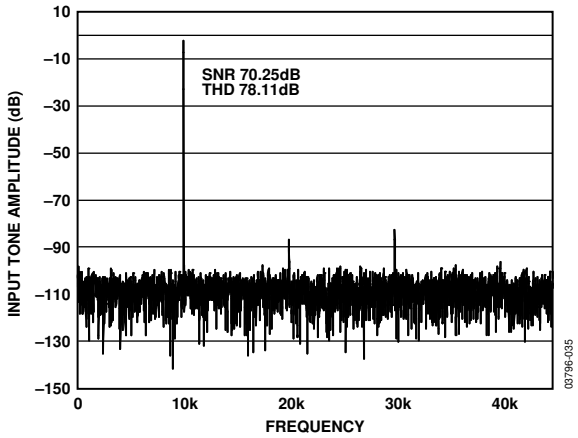

Figure 22. Typical FFT Plot for the Auxiliary Channels of the AD7877 at 90 kHz Sample Rate and 10 kHz Input Frequency

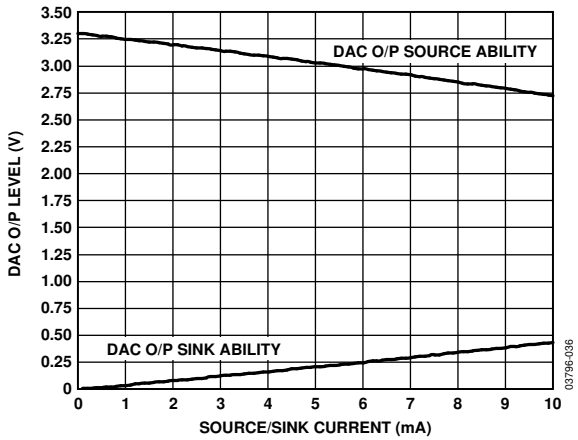

Figure 23. DAC Source and Sink Current Capability

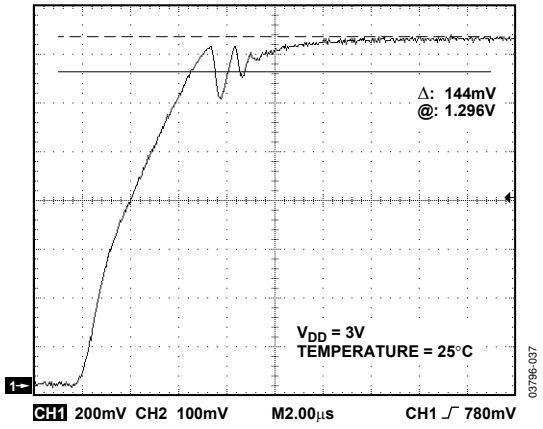

Figure 24. DAC Output Settling Time (Zero Scale to Half Scale)

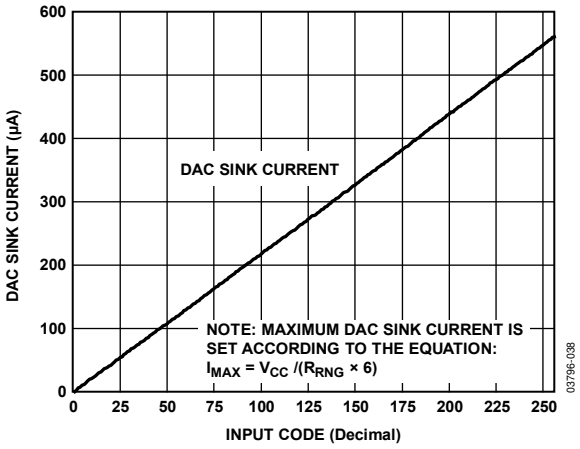

Figure 25. DAC Sink Current vs. Input Code with R_{RNG} = 1 kΩ

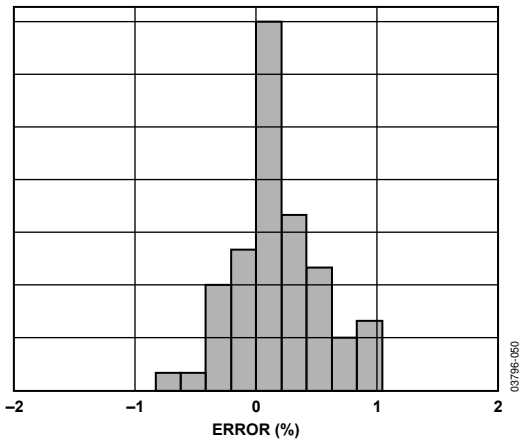

Figure 26. Typical Accuracy for Battery Channel (25°C)

TERMINOLOGY

Integral Nonlinearity (INL)
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale at 1 LSB below the first code transition, and full scale at 1 LSB above the last code transition.

Differential Nonlinearity (DNL)
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (00…000) to (00…001) from the ideal (AGND + 1 LSB).

Gain Error
The deviation of the last code transition (111…110) to (111…111) from the ideal (V_{REF} − 1 LSB) after the offset error has been adjusted out.

On Resistance
A measure of the ohmic resistance between the drain and the source of the switch drivers.

CIRCUIT INFORMATION

The AD7877 is a complete, 12-bit data acquisition system for digitizing positional inputs from a touch screen in PDAs and other devices. In addition, it can monitor two battery voltages, ambient temperature, and three auxiliary analog voltages, with high and low limit comparisons on three of the inputs, and has up to four general-purpose logic I/O pins.

The core of the AD7877 is a high speed, low power, 12-bit analog-to-digital converter (ADC) with input multiplexer, on-chip track-and-hold, and on-chip clock. The results of conversions are stored in 11 results registers, and the results from one auxiliary input and two battery inputs can be compared with high and low limits stored in limit registers to generate an out-of-limit $\overline{\text{ALERT}}$. The AD7877 also contains low resistance analog switches to switch the X and Y excitation voltages to the touch screen, a STOPACQ pin to control the ADC acquisition period, 2.5 V reference, on-chip temperature sensor, and 8-bit DAC to control LCD contrast. The high speed SPI serial bus provides control of, and communication with, the device.

Operating from a single supply from 2.2 V to 5 V, the AD7877 offers throughput rates of up to 125 kHz. The device is available in a 5 mm × 5 mm, 32-lead, lead frame chip scale package (LFCSP), and in a 2.5 mm × 2.8 mm, wafer level chip scale package (WLCSP), with a 5 × 5 ball grid array.

The data acquisition system of the AD7877 has a number of advanced features:

- Input channel sequenced automatically or selected by the host.
- STOPACQ feature to reduce noise from LCD.
- Averaging of from 1 to 16 conversions for noise reduction.
- Programmable acquisition time.
- Power management.
- Programmable ADC power-up delay before first conversion.
- Choice of internal or external reference.
- Conversion at preprogrammed intervals.

TOUCH SCREEN PRINCIPLES

A 4-wire touch screen consists of two flexible, transparent, resistive-coated layers that are normally separated by a small air gap. The X layer has conductive electrodes running down the left and right edges, allowing the application of an excitation voltage across the X layer from left to right.

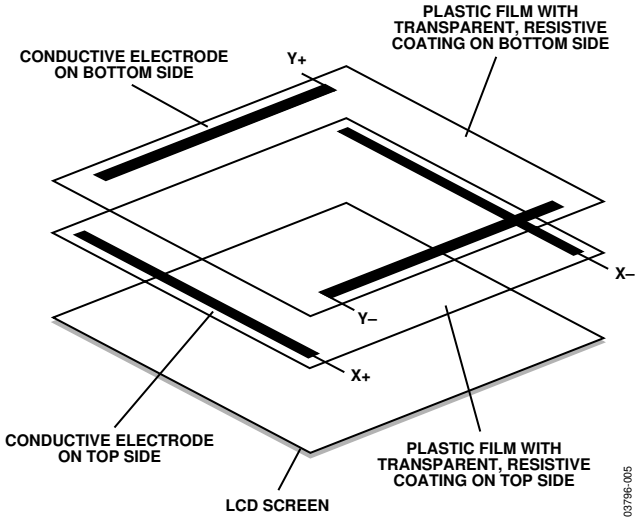

Figure 27. Basic Construction of a Touch Screen

The Y layer has conductive electrodes running along the top and bottom edges, allowing the application of an excitation voltage down the Y layer from top to bottom.

Provided that the layers are of uniform resistivity, the voltage at any point between the two electrodes is proportional to the horizontal position for the X layer and the vertical position for the Y layer.

When the screen is touched, the two layers make contact. If only the X layer is excited, the voltage at the point of contact, and therefore the horizontal position, can be sensed at one of the Y layer electrodes. Similarly, if only the Y layer is excited, the voltage, and therefore the vertical position, can be sensed at one of the X layer electrodes. By switching alternately between X and Y excitation and measuring the voltages, the X and Y coordinates of the contact point can be found.

In addition to measuring the X and Y coordinates, it is also possible to estimate the touch pressure by measuring the contact resistance between the X and Y layers. The AD7877 is designed to facilitate this measurement.

Figure 28 shows an equivalent circuit of the analog input structure of the AD7877, showing the touch screen switches, the main analog multiplexer, the ADC with analog and differential reference inputs, and the dual 3-to-1 multiplexer that selects the reference source for the ADC.

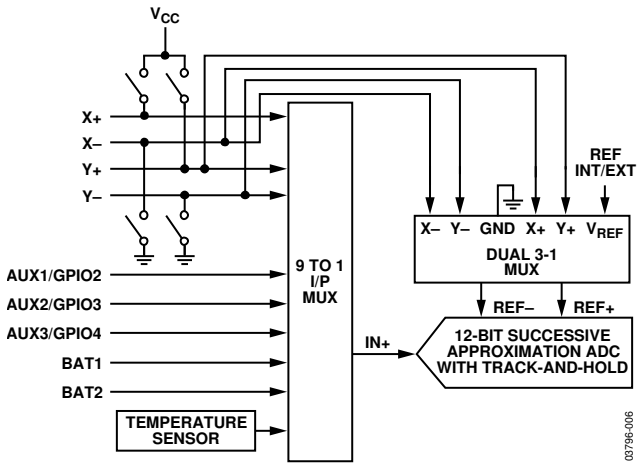

Figure 28. Analog Input Structure

The AD7877 can be set up to automatically convert either specific input channels or a sequence of channels. The results of the ADC conversions are stored in the results registers. See the Serial Interface section for details.

When measuring the ancillary analog inputs (AUX1 to AUX3, BAT1 and BAT2), the ADC uses the internal reference, or an external reference applied to the V_{REF} pin, and the measurement is referred to GND.

MEASURING TOUCH SCREEN INPUTS

When measuring the touch screen inputs, it is possible to measure using the internal (or external) reference, or to use the touch screen excitation voltage as the reference and perform a ratiometric, differential measurement. The differential method is the default and is selected by clearing the SER/$\overline{DFR}$ bit (Bit 11) in Control Register 1. The single-ended method is selected by setting this bit.

Single-Ended Method

Figure 29 illustrates the single-ended method for the Y position. For the X position, the excitation voltage is applied to X+ and X– and the voltage measured at Y+.

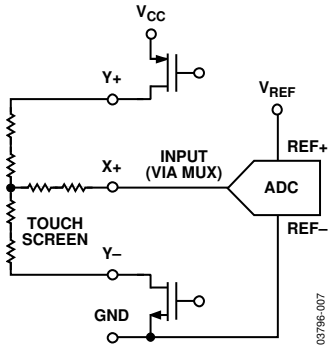

Figure 29. Single-Ended Conversion of Touch Screen Inputs

The voltage seen at the input to the ADC in Figure 29 is

$$V_{IN} = V_{CC} \times \frac{R_{Y}-}{R_{YTOTAL}} \quad (1)$$

The advantage of the single-ended method is that the touch screen excitation voltage can be switched off once the signal is acquired. Because a screen can draw over 1 mA, this is a significant consideration for a battery-powered system.

The disadvantages of the single-ended method are as follows:

- It can be used only if V_{CC} is close to V_{REF}. If V_{CC} is greater than V_{REF}, some positions on the screen are outside the range of the ADC. If V_{CC} is less than V_{REF}, the full range of the ADC is not used.
- The ratio of V_{CC} to V_{REF} must be known. If V_{REF} and/or V_{CC} vary relative to one another, this can introduce errors.
- Voltage drops across the switches can introduce errors. Touch screens can have a total end-to-end resistance ranging from 200 Ω to 900 Ω. Taking the lowest screen resistance of 200 Ω and a typical switch resistance of 14 Ω can reduce the apparent excitation voltage to 200/228 × 100 = 87% of its actual value. In addition, the voltage drop across the low-side switch adds to the ADC input voltage. This introduces an offset into the input voltage, thus, it can never reach zero.

The single-ended method is adequate for applications that use a fairly blunt and imprecise instrument for an input device, such as a finger.

Ratiometric Method

The ratiometric method illustrated in Figure 30 shows the negative input of the ADC reference tied to Y– and the positive input connected to Y+. Thus, the screen excitation voltage provides the reference for the ADC. The input of the ADC is connected to X+ to determine the Y position.

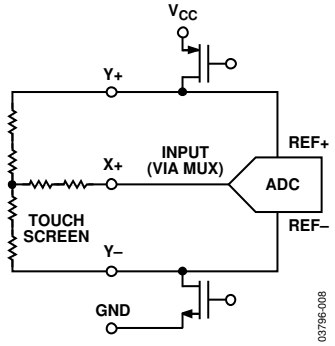

Figure 30. Ratiometric Conversion of Touch Screen Inputs

For greater accuracy, the ratiometric method has two significant advantages:

- The reference to the ADC is provided from the actual voltage across the screen; therefore, when the voltage drops across the switches, it has no effect.
- Because the measurement is ratiometric, it does not matter if the voltage across the screen varies in the long term. However, it must not change after the signal has been acquired.

The disadvantage of the ratiometric method is that the screen must be powered up at all times because it provides the reference voltage for the ADC.

TOUCH-PRESSURE MEASUREMENT

The pressure applied to the touch screen via a pen or finger can also be measured with the AD7877 using some simple calculations. The contact resistance between the X and Y plates is measured providing a good indication of the size of the depressed area and, therefore, the applied pressure. The area of the spot that is touched is proportional to the size of the object touching it. The size of this resistance (R_{TOUCH}) can be calculated using two different methods.

First Method

The first method requires the user to know the total resistance of the X-plate tablet (R_X). Three touch screen conversions are required:

- Measurement of the X position, $X_{POSITION}$ (Y+ input).
- Measurement of the Y− input with the excitation voltage applied to Y+ and X− (Z1 measurement).
- Measurement of the X+ input with the excitation voltage applied to Y+ and X− (Z2 measurement).

These three measurements are illustrated in Figure 31.

The AD7877 has two special ADC channel settings that configure the X and Y switches for Z1 and Z2 measurement and store the results in the Z1 and Z2 results registers. The Z1 measurement is ADC Channel 1010b, and the result is stored in the register with Read Address 11010b. The Z2 measurement is ADC Channel 0010b, and the result is stored in the register with Read Address 10010b.

The touch resistance can then be calculated using the following equation:

$$R_{TOUCH} = (R_{XPlate}) \times (X_{POSITION}/4096 \times [Z2/Z1) - 1] \quad (2)$$

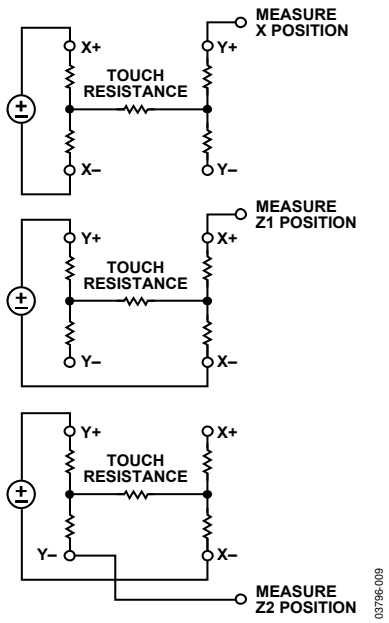

Figure 31. Three Measurements Required for Touch Pressure

Second Method

The second method requires the user to know the resistance of the X-plate and Y-plate tablets. Three touch screen conversions are required, a measurement of the X position ($X_{POSITION}$), Y position ($Y_{POSITION}$), and Z1 position.

The following equation also calculates the touch resistance:

$$R_{TOUCH} = R_{XPlate} \times (X_{POSITION}/4096) \times [(4096/Z1) - 1] - R_{YPlate} \times [1 - (Y_{POSITION}/4096)] \quad (3)$$

STOPACQ PIN

As previously explained in the Touch Screen Principles section, touch screens are composed of two resistive layers, normally placed over an LCD screen. Because these layers are in close proximity to the LCD screen, noise can be coupled from the screen onto these resistive layers, causing errors in the touch screen positional measurements.

For example, a jitter might be noticeable in the cursor on-screen. In most LCD touch screen systems, a signal, such as an LCD invert signal or other control signal, is present, and noise is usually coupled onto the touch screen during the active period of this signal (see Figure 32).

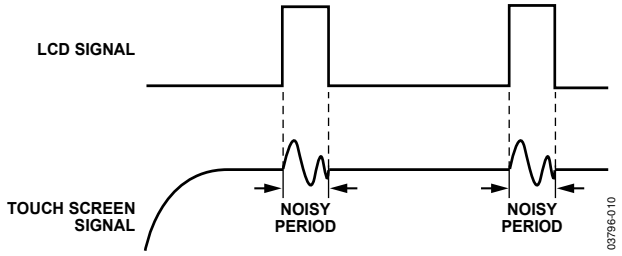

Figure 32. Effect of LCD Noise on Touch Screen Measurements

It is only during the sample or acquisition phase of the ADC operation of the AD7877 that noise from the LCD screen has an effect on the ADC measurements. During the hold or conversion phase, the noise has no effect, because the voltage at the input of the ADC has already been acquired. Therefore, to minimize the effect of noise on the touch screen measurements, the ADC acquisition phase should be halted.

The LCD control signal should be applied to the STOPACQ pin. To ensure that acquisition never occurs during the noisy period when the LCD signal is active, the AD7877 monitors this signal. No acquisitions take place when the control signal is active. Any acquisition that is in progress when the signal becomes active is aborted and restarts when the signal becomes inactive again.

To accommodate signals of different polarities on the STOPACQ pin, a user-programmable register bit is used to indicate whether the signal is active high or low. The POL bit is Bit 3 in Control Register 2, Address 0x02. Setting POL to 1 indicates that the signal on STOPACQ is active high; setting POL to 0 indicates that it is active low. POL defaults to 0 on power-up. To disable monitoring of STOPACQ, the pin should be tied low if POL = 1, or tied high if POL = 0. Under no circumstances should the pin be left floating.

The signal on STOPACQ has no effect while the ADC is in conversion mode, or during the first conversion delay time. (See the Control Registers section for details on the first conversion delay.)

When enabled, the STOPACQ monitoring function is implemented on all input channels to the ADC: AUX1, AUX2, BAT1, BAT2, TEMP1, and TEMP2, as well as on the touch screen input channels.

TEMPERATURE MEASUREMENT

Two temperature measurement options are available on the AD7877: the single conversion method and the differential conversion method. The single conversion method requires only a single measurement on ADC Channel 1000b. Whereas differential conversion requires two measurements, one on ADC Channel 1000b and a second on ADC Channel 1001b. The results are stored in the results registers with Address 11000b (TEMP1) and Address 11001b (TEMP2). The AD7877 does not provide an explicit output of the temperature reading; the system must perform some external calculations. Both methods are based on an on-chip diode measurement.

Single Conversion Method

The single conversion method makes use of the fact that the temperature coefficient of a silicon diode is approximately −2.1 mV/°C. However, this small change is superimposed on the diode forward voltage, which can have a wide tolerance. It is, therefore, necessary to calibrate by measuring the diode voltage at a known temperature to provide a baseline from which the change in forward voltage with temperature can be measured. This method provides a resolution of approximately 0.3°C and a predicted accuracy of ±2.5°C.

The temperature limit comparison is performed on the result in the TEMP1 results register, which is simply the measurement of the diode forward voltage. The values programmed into the high and low limits should be referenced to the calibrated diode forward voltage to make accurate limit comparisons. An example is shown in the Limit Comparison section.

Differential Conversion Method

The differential conversion method is a 2-point measurement. The first measurement is performed with a fixed bias current into a diode (when the TEMP1 channel is selected), and the second measurement is performed with a fixed multiple of the bias current into the same diode (when the TEMP2 channel is selected). The voltage difference in the diode readings is proportional to absolute temperature and is given by the following formula:

$$\Delta V_{BE} = (kT/q) \times (ln\ N) \quad (4)$$

where:
V_{BE} represents the diode voltage.
N is the bias current multiple (typical value for AD7877 = 120).
k is Boltzmann's constant.
q is the electron charge.

This method provides a resolution of approximately 1.6°C, and a guaranteed accuracy of ±4°C without calibration. Determination of the N value on a part-by-part basis improves accuracy.

Assuming a current multiple of 120, which is a typical value for the AD7877, taking Boltzmann's constant, k = 1.38054 × 10^{-23} electrons V/°K, the electron charge q = 1.602189 × 10^{-19}, then T, the ambient temperature in Kelvin, would be calculated as follows:

$$\Delta V_{BE} = (kT/q) \times (ln\ N)$$
$$T°k = (\Delta V_{BE} \times q)/(k \times ln\ N)$$
$$= (\Delta V_{BE} \times 1.602189 \times 10^{-19})/(1.38054 \times 10^{-23} \times 4.65)$$
$$T°C = 2.49 \times 120 \times \Delta V_{BE} - 273$$

ΔV_{BE} is calculated from the difference in readings from the first conversion to the second conversion. The user must perform the calculations to get ΔV_{BE}, and then calculate the temperature value in degrees. Figure 33 shows a block diagram of the temperature measurement circuit.

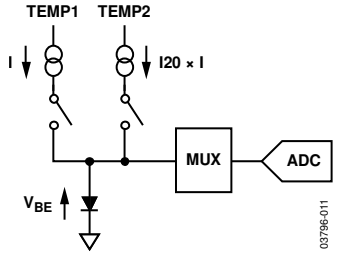

Figure 33. Block Diagram of Temperature Measurement Circuit

Temperature Calculations

If an explicit temperature reading in °C is required, then this is calculated as follows for the single measurement method:

1. Calculate the scale factor of the ADC in degrees per LSB:

   Degrees per LSB = *ADC LSB size*/−2.1 mV = (V_{REF}/4096)/−2.1 mV

2. Save the ADC output, D_{CAL}, at the calibration temperature, T_{CAL}.

3. Take ADC reading, D_{AMB}, at the temperature to be measured, T_{AMB}.

4. Calculate the difference in degrees between T_{CAL} and T_{AMB} using

   $\Delta T = (D_{AMB} - D_{CAL}) \times$ *degrees per LSB*

5. Add ΔT to T_{CAL}

Example:

The internal 2.5 V reference is used.

1. *Degrees per LSB* = (2.5/4096)/−2.1 × 10^{-3} = −0.291
2. The ADC output is 983 decimal at 25°C, equivalent to a diode forward voltage of 0.6 V.
3. The ADC output at T_{AMB} is 880.
4. ΔT = (880 − 983) × −0.291 = 30°
5. T_{AMB} = 25 + 30 = 55°C

To calculate the temperature explicitly using the differential method:

1. Calculate the LSB size of the ADC in V:

   LSB = V_{REF}/4096

2. Subtract TEMP1 from TEMP2 and multiply by LSB size to get ΔV_{BE}.

3. Multiply by 2490 and subtract 273 to obtain the temperature in °C.

Example:

The internal 2.5 V reference is used.

1. *LSB size* = 2.5 V/4096 = 6.1 × 10^{-4} V(610 µV)
2. *TEMP1* = 880 and *TEMP2* = 1103:
   ΔV_{BE} = (1103 − 880) × 6.1× 10^{-4} = 0.136 V
3. *T* = 0.136 × 2490 − 273 = 65°C

BATTERY MEASUREMENT

The AD7877 can monitor battery voltages from 0.5 V to 5 V on two inputs, BAT1 and BAT2. Figure 34 shows a block diagram of a battery voltage monitored through the BAT1 pin. The voltage to the V_{CC} pin of the AD7877 is maintained at the desired supply voltage via the dc/dc regulator while the input to the regulator is monitored. This voltage on BAT1 is divided down by 2 internally, so that a 5 V battery voltage is presented to the ADC as 2.5 V. To conserve power, the divider circuit is on only during the sampling of a voltage on BAT1. The BAT2 input circuitry is identical.

The BAT1 input is ADC Channel 0110b and the result is stored in Register 10110b. The BAT2 input is ADC Channel 0111b and the result is stored in Register 10111b.

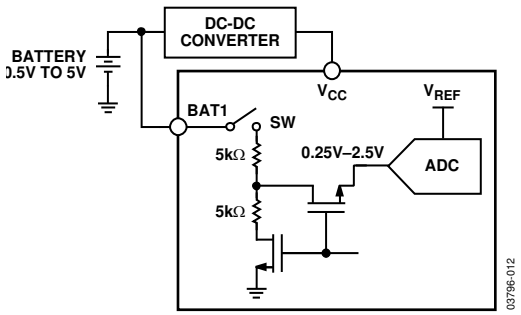

Figure 34. Block Diagram of Battery Measurement Circuit

Figure 34 shows the ADC using the internal reference of 2.5 V. The maximum battery voltage that the AD7877 can measure changes when a different reference voltage is used. The maximum voltage that is measurable is $V_{REF} \times 2$, because this voltage gives a full-scale output from the ADC. If a smaller reference is used, such as 2 V, then the maximum measurable battery voltage is 4 V. If a larger reference is used, such as 3.5 V, then the maximum measurable battery voltage is 7 V. The internal reference is particularly suited for use when measuring lithium-ion batteries, wherein the minimum voltage is about 2.7 V and the maximum voltage is about 4.2 V. A proper choice of external reference ensures that other voltage ranges can be accommodated.

AUXILIARY INPUTS

The AD7877 has three auxiliary analog inputs, AUX1 to AUX3. These channels have a full-scale input range from 0 V to V_{REF}. The ADC channel addresses for AUX1 to AUX3 are 0011b, 0100b, and 0101b, and the results are stored in Register 10011b, Register 10100b, and Register 10101b. These pins can also be reconfigured as general-purpose logic inputs/outputs, as described in the GPIO Configuration section.

LIMIT COMPARISON

The AUX1 measurement, the two battery measurements, and the TEMP1 measurement can all be compared with high and low limits, and an out-of-limit result that generates an alarm output at the $\overline{\text{ALERT}}$ pin. The limits are stored in registers with addresses from 00100b to 01011b. After a measurement from any one of the four channels is converted, it is compared with the corresponding high and low limits. An out-of-limit result sets one of the status bits in the alert status/enable register. For details on these and other registers, see the Register Maps and Detailed Register Descriptions sections. For details on writing and reading data, see the Serial Interface section.

As described in the Single Conversion Method section, the temperature comparison is made using the result of the TEMP1 measurement, that is, the diode forward voltage. Because the temperature coefficient of the diode is known but the actual forward voltage can have a wide tolerance, it is not possible to program the high and low limit registers with predetermined values.

Instead, it is necessary to calibrate the temperature measurement, calculate the TEMP1 readings at the high and low limit temperatures, and then program those values into the limit registers, as follows:

1. Calculate

   $LSB\ per\ degree = -2.1\ mV/(V_{REF}/4096)$.

2. Save the calibration reading D_{CAL} at the calibration temperature, T_{CAL}.
3. Subtract T_{CAL} from limit temperatures T_{HIGH} and T_{LOW} to get the difference in degrees between the limit temperatures and the calibration temperature.
4. Multiply this value by LSB per degree to obtain the value in LSBs.
5. Add these values to the digital value at the calibration temperature to get the digital high and low limit values.

Example:

The internal 2.5 V reference is used.

1. $T_{HIGH} = +65°C$ and $T_{LOW} = -10°C$.
2. $LSB\ per\ degree = -2.1 \times 10^{-3}/(2.5/4096) = -3.44$.
3. $D_{CAL} = 983$ decimal at 25°C.
4. $D_{HIGH} = (65 - 25) \times -3.44 + 983 = 845$.
5. $D_{LOW} = (-10 - 25) \times -3.44 + 983 = 1103$.

CONTROL REGISTERS

Control Register 1 contains the ADC channel address, the SER/$\overline{\text{DFR}}$ bit (to choose single or differential methods of touch screen measurement), the register read address, and the ADC mode bits. Control Register 1 should always be the last register to be programmed prior to starting conversions. Its power-on default value is 0x00. To change any parameter after conversion has begun, the part should first be put into Mode 00, the changes made, and then Control Register 1 reprogrammed, ensuring that it is always the last register to be programmed before conversions begin.

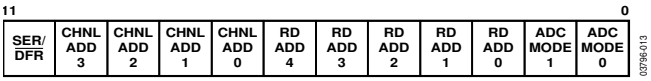

Figure 35. Control Register 1

Control Register 2 sets the timer, reference, polarity, first conversion delay, averaging, and acquisition time. Its power-on default value is 0x00. See the Detailed Register Descriptions section for more information on the control registers.

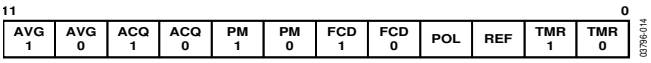

Figure 36. Control Register 2

CONTROL REGISTER 1

ADC Mode (Control Register 1, Bits[1:0])

These bits select the operating mode of the ADC. The AD7877 has three operating modes. These are selected by writing to the mode bits in Control Register 1. If the mode bits are 00, no conversion is performed.

Table 5. Control Registera 1 Mode Selection

MODE1	MODE0	Function
0	0	Do not convert (default)
0	1	Single-channel conversion, AD7877 in slave mode
1	0	Sequence 0, AD7877 in slave mode
1	1	Sequence 1, AD7877 in master mode

If the mode bits are 01, a single conversion is performed on the channel selected by writing to the channel bits of Control Register 1 (Bit 7 to Bit 10). At the end of the conversion, if the TMR bits in Control Register 2 are set to 00, the mode bits revert to 00 and the ADC returns to no convert mode until a new conversion is initiated by the host. Setting the TMR bits to a value other than 00 causes the conversion to be repeated, as described in the Timer (Control Register 2, Bits[1:0]) section. The flowchart in Figure 38 shows how the AD7877 operates in Mode 01.

The AD7877 can also be programmed to convert a sequence of selected channels automatically. The two modes for this type of conversion are slave mode and master mode.

For slave mode operation, the channels to be digitized are selected by setting the corresponding bits in Sequencer Register 0. Conversion is initiated by writing 10b to the mode bits of Control Register 1. The ADC then digitizes the selected channels and stores the results in the corresponding results registers. At the end of the conversion, if the TMR bits in Control Register 2 are set to 00, the mode bits revert to 00 and the ADC returns to no convert mode until a new conversion is initiated by the host. Setting the TMR bits to a code other than 00 causes the conversion sequence to be repeated. The flowchart in Figure 39 shows how the AD7877 operates in Mode 10.

For master mode operation, the channels to be digitized are written to Sequencer Register 1. Master mode is then selected by writing 11 to the mode bits in Control Register 1. In this mode, the wake-up on touch feature is active, so conversion does not begin immediately. The AD7877 waits until the screen is touched before beginning the sequence of conversions. The ADC then digitizes the selected channels, and the results are written to the results registers. The AD7877 waits for the screen to be touched again, or for a timer event if the screen remains touched, before beginning another sequence of conversions. The flowchart in Figure 40 shows how the AD7877 operates in Mode 11.

ADC Channel (Control Register 1, Bits[10:7])

The ADC channel is selected by Bits [10:7] of Control Register 1 (CHADD3 to CHADD0). In addition, the SER/$\overline{\text{DFR}}$ bit, Bit 11, selects between single-ended and differential conversion. A complete list of channel addresses is given in Table 6.

For Mode 0 (single-channel) conversion, the channel is selected by writing the appropriate CHADD3 to CHADD0 code to Control Register 1.

For sequential channel conversion, channels to be converted are selected by setting bits corresponding to the channel number in Sequencer Register 1 for slave mode sequencing or Sequencer Register 2 for master mode sequencing.

For both single-channel and sequential conversion, normal (single-ended) conversion is selected by clearing the SER/$\overline{\text{DFR}}$ bit in Control Register 1. Ratiometric (differential) conversion is selected by setting the SER/$\overline{\text{DFR}}$ bit.

Table 6. Codes for Selecting Input Channel and Normal or Ratiometric Conversion

Channel	SER/$\overline{DFR}$	CHADD(3:0)	Analog Input	X Switches	Y Switches	+REF	−REF
0	0	0 0 0 0	X+ (Y position)	Off	On	Y+	Y−
1	0	0 0 0 1	Y+ (X position)	On	Off	X+	X−
2	0	0 0 1 0	Y− (Z2)	X+ off, X− on	Y+ on, Y− off	Y+	X−
3	0	0 01 1	AUX1	Off	Off	V_{REF}	GND
4	0	0 1 00	AUX2	Off	Off	V_{REF}	GND
5	0	0 1 0 1	AUX3	Off	Off	V_{REF}	GND
6	0	0 1 1 0	BAT1	Off	Off	V_{REF}	GND
7	0	0 1 1 1	BAT2	Off	Off	V_{REF}	GND
8	0	1 0 0 0	TEMP1	Off	Off	V_{REF}	GND
9	0	1 0 0 1	TEMP2	Off	Off	V_{REF}	GND
10	0	1 0 1 0	X+ (Z1)	X+ OFF, X− ON	Y+ on Y− off	Y+	X−
-	0	1 0 1 1	Invalid address				
-	0	1 1 0 0	Invalid address				
-	0	1 1 0 1	Invalid address				
-	0	1 1 1 0	Invalid address				
-	0	1 1 1 1	Invalid address				
0	1	0 0 0 0	X+ (Y position)	Off	On	V_{REF}	GND
1	1	0 0 0 1	Y+ (X position)	On	Off	V_{REF}	GND
2	1	0 0 1 0	Y− (Z2)	X+ off, X− on	Y+ on, Y− off	V_{REF}	GND
3	1	0 0 1 1	AUX1	Off	Off	V_{REF}	GND
4	1	0 1 0 0	AUX2	Off	Off	V_{REF}	GND
5	1	0 1 0 1	AUX3	Off	Off	V_{REF}	GND
6	1	0 1 1 0	BAT1	Off	Off	V_{REF}	GND
7	1	0 1 1 1	BAT2	Off	Off	V_{REF}	GND
8	1	1 0 0 0	TEMP1	Off	Off	V_{REF}	GND
9	1	1 0 0 1	TEMP2	Off	Off	V_{REF}	GND
10	1	1 0 1 0	X+ (Z1)	X+ off, X− on	Y+ on, Y− off	V_{REF}	GND
-	1	10 1 1	Invalid address				
-	1	1 1 0 0	Invalid address				
-	1	1 1 0 1	Invalid address				
-	1	1 1 1 0	Invalid address				
-	1	1 1 1 1	Invalid address				

CONTROL REGISTER 2

Timer (Control Register 2, Bits[1:0])

The TMR bits in Control Register 2 enable the ADC to repeatedly perform a conversion or conversion sequence either once only or at intervals of 512 µs, 1.024 ms, or 8.19 ms. In slave mode, the timer starts as soon as the conversion sequence is finished. In master mode, the timer starts at the end of a conversion sequence only if the screen remains touched. If the touch is released at any stage, then the timer stops and, the next time the screen is touched, a conversion sequence begins immediately.

Table 7. Control Register 2 Timer Selection

TMR1	TMR0	Function
0	0	Convert only once (default)
0	1	Every 1024 clocks (512 µs)
1	0	Every 2048 clocks (1.024 ms)
1	1	Every 16,384 clocks (8.19 ms)

Int/Ext Reference (Control Register 2, Bit[2])

If the REF bit in Control Register 2 is 0 (default value), the internal reference is selected. Buffer any connection made to V_{REF} while the internal reference is selected (for example, to supply a reference to other circuits). An external power supply should not be connected to this pin while REF is equal to 0, because it might overdrive the internal reference. Because the internal reference is 2.5 V, it operates only with supply voltages down to 2.7 V. Below this value, use an external reference.

If the REF bit is 1, the V_{REF} pin becomes an input and the internal reference is powered down. This overrides any setting of the PM bits with regard to the reference. An external reference can then be applied to the REF pin.

STOPACQ Polarity (Control Register 2, Bit[3])

This bit should be set according to the polarity of the signal applied to the STOPACQ pin. If that signal is active high, that is, no acquisitions should occur during the high period of the signal, then the POL bit should be set to 1. If the signal is active low, then the POL bit should be 0. The default value for POL is 0.

First Conversion Delay (Control Register 2, Bits[5:4])

The first conversion delay (FCD) bits in Control Register 2 program a delay of 500 ns (default), 128 µs, 1.024 ms, or 8.19 ms before the first conversion, to allow the ADC time to power up. This delay also occurs before conversion of the X and Y coordinate channels, to allow extra time for screen settling, and after the last conversion in a sequence, to precharge $\overline{\text{PENIRQ}}$. If the signal on the STOPACQ pin is being monitored and goes active during the FCD, it is ignored until after the FCD period.

Table 8. First Conversion Delay Selection

FCD1	FCD	Function
0	0	1 clock delay (500 ns)
0	1	256 clock delays (128 µs)
1	0	2048 clock delays (1.024 ms)
1	1	16,384 clock delays (8.19 ms)

Power Management (Control Register 2, Bits[7:6])

The power management (PM) bits in Control Register 2 allow the power management features of the ADC to be programmed. If the PM bits are 00, the ADC is powered down permanently. This overrides any setting of the mode bits in Control Register 1. If the PM bits are 01, the ADC and the reference both power down when the ADC is not converting. If the PM bits are 10, the ADC and reference are powered up continuously. If the PM bits are 11, the ADC, but not the reference, powers down when the ADC is not converting. If the AD7879 is in full power mode (PM=10), the master sequencer should not be used. PM bits must be set to 01 or 11 when using the master sequencer.

Table 9. Power Management Selection

PM1	PM0	Function
0	0	Power down continuously (default)
0	1	Power down ADC and reference when ADC is not converting (powers up with FCD at start of a conversion)
1	0	Powered up continuously
1	1	Power down ADC when ADC is not converting (powers up with FCD at start of conversion)

Acquisition Time (Control Register 2, Bits[9:8])

The ACQ bits in Control Register 2 allow the selection of acquisition times for the ADC of 2 µs (default), 4 µs, 8 µs, or 16 µs. The user can program the ADC with an acquisition time suitable for the type of signal being sampled. For example, signals with large RC time constants can require longer acquisition times.

Table 10. Acquisition Time Selection

ACQ1	ACQ0	Function
0	0	4 clock periods (2 µs)
0	1	8 clock periods (4 µs)
1	0	16 clock periods (8 µs)
1	1	32 clock periods (16 µs)

Averaging (Control Register 2, Bits[11:10])

Signals from touch screens can be extremely noisy. The AVG bits in Control Register 2 allow multiple conversions to be performed on each input channel and averaged to reduce noise. A single conversion can be selected (no averaging), which is the default, or 4, 8, or 16 conversions can be averaged. Only the final averaged result is written into the results register.

Table 11. Averaging Selection

AVG1	AVG0	Function
0	0	ADC performs 1 average per channel
0	1	ADC performs 4 averages per channel
1	0	ADC performs 8 averages per channel
1	1	ADC performs 16 averages per channel

SEQUENCER REGISTERS

There are two sequencer registers on the AD7877. Sequencer Register 0 controls the measurements performed during a slave mode sequence. Sequencer Register 1 controls the measurements performed during a master mode sequence.

To include a measurement in a slave mode or master mode sequence, the relevant bit must be set in Sequencer Register 0 or Sequencer Register 1. Setting Bit 11 includes a measurement on ADC Channel 0 in the sequence, which is the Y positional measurement. Setting Bit 10 includes a measurement on ADC Channel 1 (X+ measurement), and so on, through Bit 1 for Channel 10. Figure 37 illustrates the correspondence between the bits in the sequencer registers and the various measurements. Bit 0 in both sequencer registers is not used. See also the Detailed Register Descriptions section.

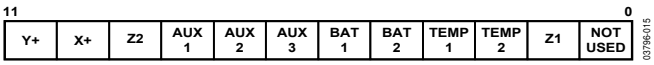

Figure 37. Sequencer Register

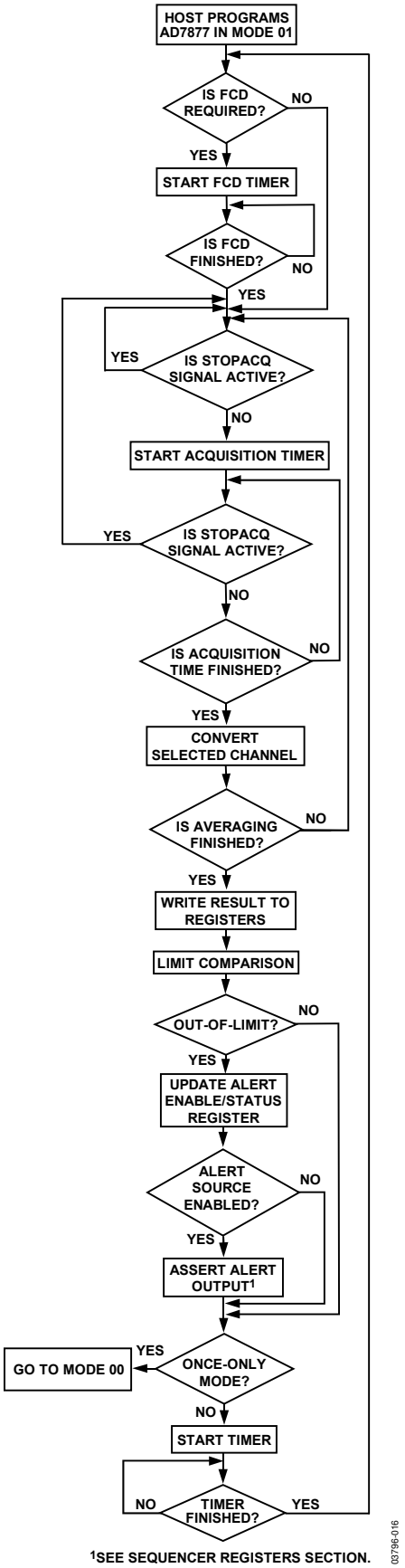

Figure 38. Single Channel Operation

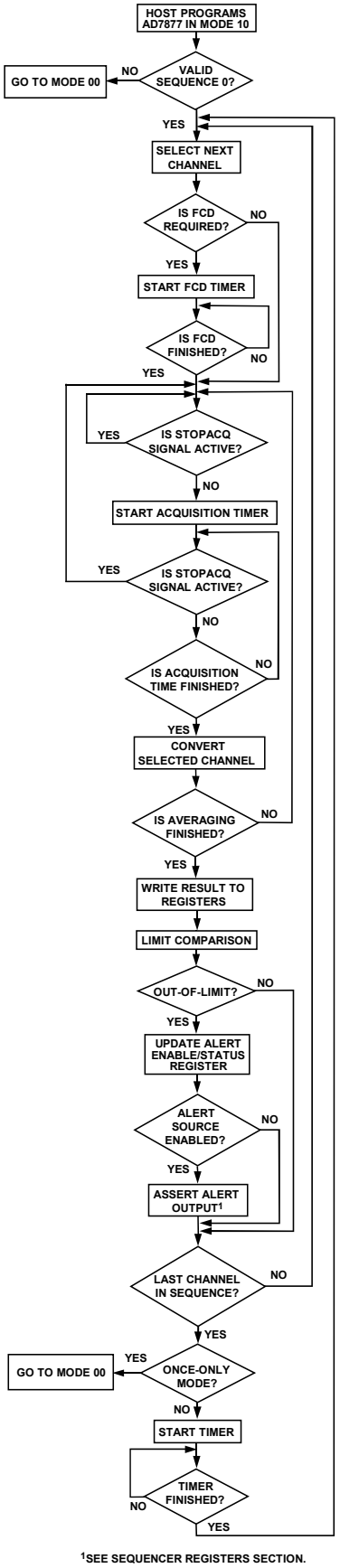

Figure 39. Slave Mode Sequencer Operation

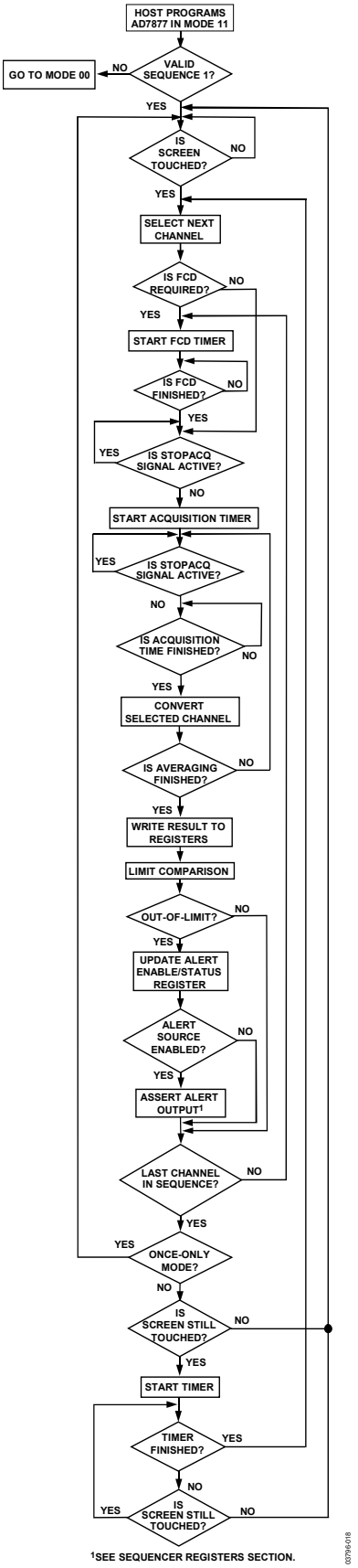

Figure 40. Master Mode Sequencer Operation

INTERRUPTS

Data Available Output ($\overline{DAV}$)

The data available output ($\overline{DAV}$) indicates that new ADC data is available in the results registers. While the ADC is idle or is converting, $\overline{DAV}$ is high. Once the ADC has finished converting and new data has been written to the results registers, $\overline{DAV}$ goes low. Taking $\overline{DAV}$ low to read the registers resets $\overline{DAV}$ to a high condition. $\overline{DAV}$ is also reset, if a new conversion is started by the AD7877 because the timer expired. The host should attempt to read the results registers only when $\overline{DAV}$ is low.

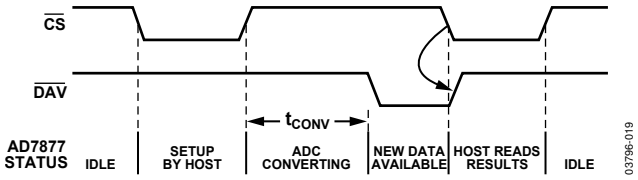

Figure 41. Operation of $\overline{DAV}$ Output

$\overline{DAV}$ is useful as a host interrupt in master mode. In this mode, the host can program the AD7877 to automatically perform a sequence of conversions, and can be interrupted by $\overline{DAV}$ at the end of each conversion sequence.

When the on-board timer is programmed to perform automatic conversions, a limited time is available to the host to read the results registers before another sequence of conversions begins. The $\overline{DAV}$ signal is reset high when the timer expires, and the host should not access the results registers while $\overline{DAV}$ is high.

Figure 42 shows the worst-case timings for reading the results registers after $\overline{DAV}$ has gone low. The timer is set at a minimum, and the conversion sequence includes all 11 possible ADC channels. t_1 is the time taken for acquisition and conversion on one ADC channel. t_2 shows the minimum timer delay, that is, 1024 clock periods. t_3 is the time taken to read all 11 result registers. If the host wants to read all 11 registers, then it must do so before the timer expires. t_4 is the maximum time allowable between $\overline{DAV}$ going low and the host beginning to read the results registers. If t_4 is exceeded, then all registers cannot be read before the start of a new conversion, and incorrect data could be read by the host.

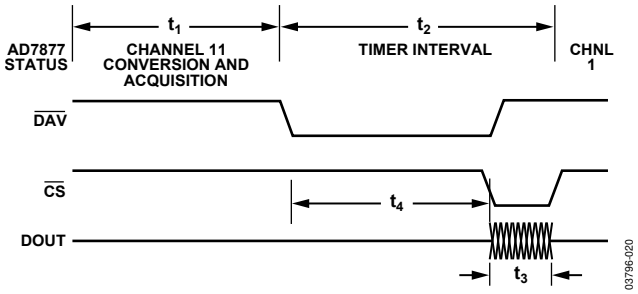

Figure 42. Timing for Reads after $\overline{DAV}$ Goes Low