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TABLE OF CONTENTS

Features	1	Auxiliary Input	18
Applications	1	Battery Input	18
Functional Block Diagram	1	Limit Comparison	18
General Description	1	GPIO	18
Revision History	2	Conversion Timing	20
Specifications	3	Register Map	21
SPI Timing Specifications (AD7879/AD7889)	4	Detailed Register Descriptions	22
I ² C Timing Specifications (AD7879-1/AD7889-1)	5	Control Registers	26
Absolute Maximum Ratings	6	Control Register 1	26
Thermal Resistance	6	Control Register 2	28
ESD Caution	6	Control Register 3	30
Pin Configurations and Function Descriptions	7	Interrupts	31
Typical Performance Characteristics	9	Synchronizing the AD7879/AD7889 to the Host CPU	32
Terminology	12	Serial Interface	33
Theory of Operation	13	SPI Interface	33
Touch Screen Principles	13	I ² C-Compatible Interface	35
Measuring Touch Screen Inputs	14	Grounding and Layout	38
Touch Pressure Measurement	15	Lead Frame Chip Scale Packages	38
Temperature Measurement	15	WLCSP Assembly Considerations	38
Median and Averaging Filters	17	Outline Dimensions	39
AUX/VBAT/GPIO Pin	18	Ordering Guide	40
REVISION HISTORY		Changes to Pin Configurations and Function Descriptions Section ..	7
8/2016—Rev. C to Rev. D		Added Table 7	8
Changed CP-16-10 to CP-16-20	Throughout	Changes to First Method Section	15
Changes to General Description Section	1	Changes to Median and Averaging Filters Section	17
Changes to Figure 7, Figure 8, and Table 7	8	Changes to GPIO Interrupt Enable (Bit 12, Control Register 3, Address 0x03) Section	19
Moved Figure 34; Renumbered Sequentially	30	Changes to Table 13	22
Updated Outline Dimensions	39	Changes to ADC Channel (Control Register 1, Bits[14:12]) Section	26
Changes to Ordering Guide	39	Changes to Power Management (Control Register 2, Bits[15:14]) Section	27
11/2010—Rev. B to Rev. C		Changes to <u>DAV</u> —Data Available Interrupt Section	29
Changes to Table 2	3	Changes to <u>INT</u> —Out-of-Limit Interrupt Section	29
Added Conversion Timing Section	20	Changes to Writing Data Section	31
Added Figure 34	29	Changes to Reading Data Section and Figure 40	32
1/2010—Rev. A to Rev. B		Changes to Figure 41	33
Updated Outline Dimensions	37	Changes to Writing Data over the I ² C Bus Section	34
Changes to Ordering Guide	38	Changes to Figure 44	35
3/2009—Rev. 0 to Rev. A		Updated Outline Dimensions	37
Added AD7889 and Backside-Coated WLCSP	Universal	Changes to Ordering Guide	38
Change to Battery Monitor, Input Voltage Range Parameter	3	10/2008—Revision 0: Initial Version	
Changes to Table 4	6		
Added Thermal Resistance Section and Table 5; Renumbered Sequentially	6		

SPECIFICATIONS

$V_{CC} = 1.6\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC ACCURACY					
Resolution	12			Bits	
No Missing Codes	11	12		Bits	
Integral Nonlinearity (INL) ¹			±3	LSB	LSB size = 390 μV
Differential Nonlinearity (DNL) ¹					LSB size = 390 μV
Negative DNL			-0.99	LSB	
Positive DNL			2	LSB	
Offset Error ^{1,2}		±2	±6	LSB	
Gain Error ^{1,2}			±4	LSB	
Noise ³		70		$\mu\text{V rms}$	
Power Supply Rejection ³		60		dB	
Internal Clock Frequency		2		MHz	
Internal Clock Accuracy	1.8		2.2	MHz	
SWITCH DRIVERS					
On Resistance ¹					
Y+, X+		6		Ω	
Y-, X-		5		Ω	
ANALOG INPUTS					
Input Voltage Range	0		V_{CC}	V	
DC Leakage Current		±0.1		μA	
Input Capacitance		30		pF	
Accuracy		0.3		%	
TEMPERATURE MEASUREMENT					
Temperature Range	-40		+85	$^\circ\text{C}$	
Resolution		0.3		$^\circ\text{C}$	
Accuracy ²		±2		$^\circ\text{C}$	Calibrated at 25 $^\circ\text{C}$
BATTERY MONITOR					
Input Voltage Range	0.5		5	V	
Input Impedance ³		16		$\text{k}\Omega$	
Accuracy		2	5	%	Uncalibrated accuracy
LOGIC INPUTS (DIN, SCL, $\overline{\text{CS}}$, SDA, GPIO)					
Input High Voltage, V_{INH}	$0.7 \times V_{CC}$			V	
Input Low Voltage, V_{INL}			$0.3 \times V_{CC}$	V	
Input Current, I_{IN}		0.01		μA	$V_{\text{IN}} = 0\text{ V or }V_{CC}$
Input Capacitance, C_{IN} ³		10		pF	
LOGIC OUTPUTS (DOUT, GPIO, SCL, SDA, INT)					
Output High Voltage, V_{OH}	$V_{CC} - 0.2$			V	
Output Low Voltage, V_{OL}			0.4	V	
Floating State Leakage Current		±0.1		μA	
Floating State Output Capacitance ²		5		pF	
CONVERSION RATE³					
Conversion Time		9.5		μs	Including 2 μs of acquisition time, median and averaging (MAV) filter off; 2 μs of additional time is required if the MAV filter is on
Throughput Rate		105		kSPS	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
V_{CC}	1.6	2.6	3.6	V	Specified performance
I_{CC}					Digital inputs = 0 V or V_{CC}
Converting Mode		480	650	μA	ADC on, PM = 10
Static		406		μA	ADC and temperature sensor are off; the reference and oscillator are on; PM = 01 or 11
Shutdown Mode		0.5	6	μA	PM = 00

¹ See the Terminology section.
² Guaranteed by characterization; not production tested.
³ Sample tested at 25°C to ensure compliance.

SPI TIMING SPECIFICATIONS (AD7879/AD7889)

V_{CC} = 1.6 V to 3.6 V, T_A = -40°C to +85°C, unless otherwise noted. Sample tested at 25°C to ensure compliance. All input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.4 V.

Table 2.

Parameter ¹	Limit	Unit	Description
f_{SCL}	5	MHz max	
t_1	5	ns min	\overline{CS} falling edge to first SCL falling edge
t_2	20	ns min	SCL high pulse width
t_3	20	ns min	SCL low pulse width
t_4	15	ns min	DIN setup time
t_5	15	ns min	DIN hold time
t_6	20	ns max	DOUT access time after SCL falling edge
t_7	16	ns max	\overline{CS} rising edge to DOUT high impedance
t_8	15	ns min	SCL rising edge to \overline{CS} high

¹ Guaranteed by design; not production tested.

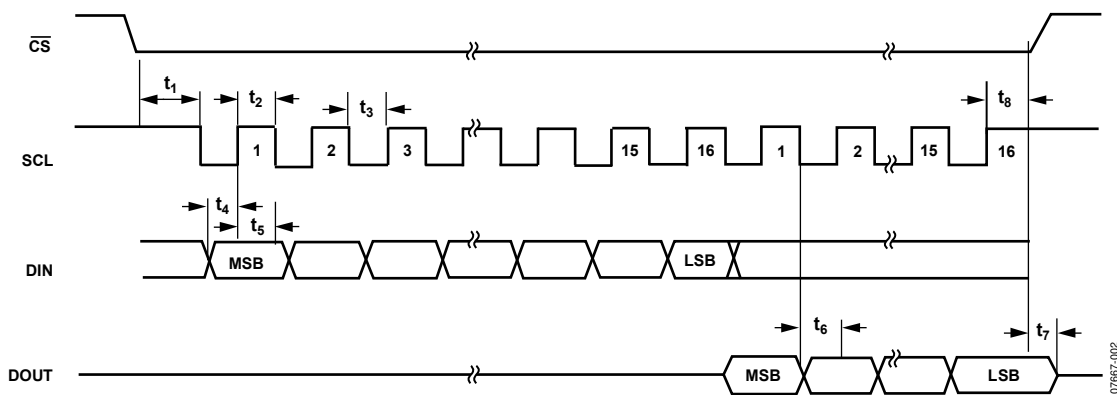


Figure 2. Detailed SPI Timing Diagram

I²C TIMING SPECIFICATIONS (AD7879-1/AD7889-1)

V_{CC} = 1.6 V to 3.6 V, T_A = -40°C to +85°C, unless otherwise noted. Sample tested at 25°C to ensure compliance. All input signals are timed from a voltage level of 1.4 V.

Table 3.

Parameter ¹	Limit	Unit	Description
f _{SCL}	400	kHz max	
t ₁	0.6	μs min	Start condition hold time, t _{HD; STA}
t ₂	1.3	μs min	Clock low period, t _{LOW}
t ₃	0.6	μs min	Clock high period, t _{HIGH}
t ₄	100	ns min	Data setup time, t _{SU; DAT}
t ₅	300	ns min	Data hold time, t _{HD; DAT}
t ₆	0.6	μs min	Stop condition setup time, t _{SU; STO}
t ₇	0.6	μs min	Start condition setup time, t _{SU; STA}
t ₈	1.3	μs min	Bus-free time between stop and start conditions, t _{BUF}
t _R	300	ns max	Clock/data rise time
t _F	300	ns max	Clock/data fall time

¹ Guaranteed by design; not production tested.

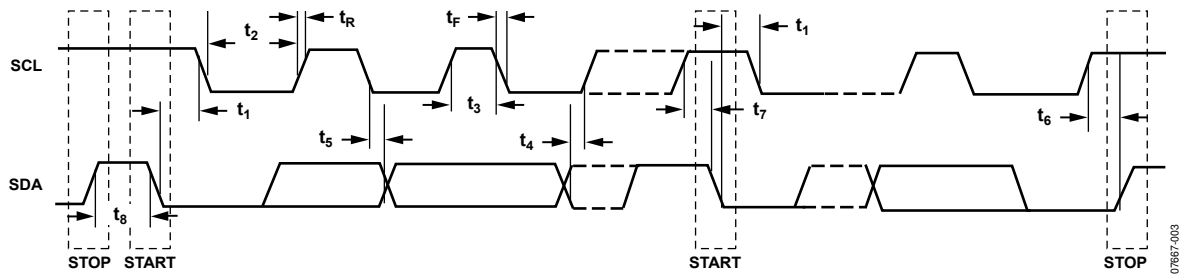


Figure 3. Detailed I²C Timing Diagram

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Rating
V_{CC} to GND	-0.3 V to +3.6 V
Analog Input Voltage to GND	-0.3 V to $V_{CC} + 0.3$ V
AUX/VBAT to GND	-0.3 V to +5 V
Digital Input Voltage to GND	-0.3 V to $V_{CC} + 0.3$ V
Digital Output Voltage to GND	-0.3 V to $V_{CC} + 0.3$ V
Input Current to Any Pin Except Supplies ¹	10 mA
ESD Rating (X+, Y+, X-, Y-)	
Air Discharge Human Body Model	15 kV
Contact Human Body Model	10 kV
ESD Rating (All Other Pins)	
Human Body Discharge	4 kV
Field-Induced Charged Device Model	1 kV
Machine Model	0.2 kV
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Power Dissipation	
WLCSP (4-Layer Board)	866 mW
LFCSP (4-Layer Board)	2.138 W
IR Reflow Peak Temperature	260°C ($\pm 0.5^\circ\text{C}$)
Lead Temperature (Soldering 10 sec)	300°C

¹ Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type ¹	θ_{JA}	Unit
12-Ball WLCSP	75	°C/W
16-Lead LFCSP	30.4	°C/W

¹ 4-layer board.

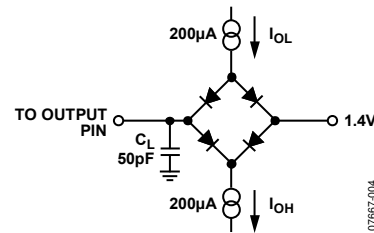


Figure 4. Circuit Used for Digital Timing

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

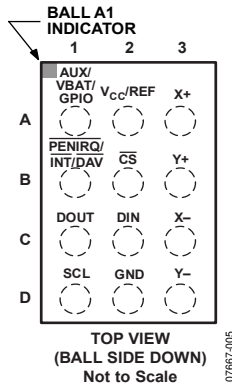


Figure 5. AD7879/AD7889 WLCSP Pin Configuration

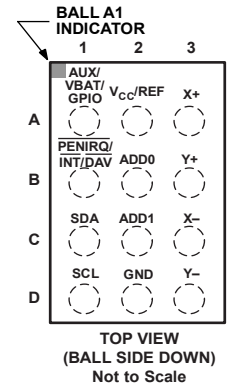
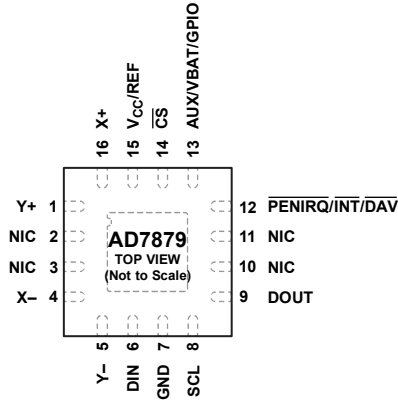


Figure 6. AD7879-1/AD7889-1 WLCSP Pin Configuration

Table 6. WLCSP Pin Function Descriptions

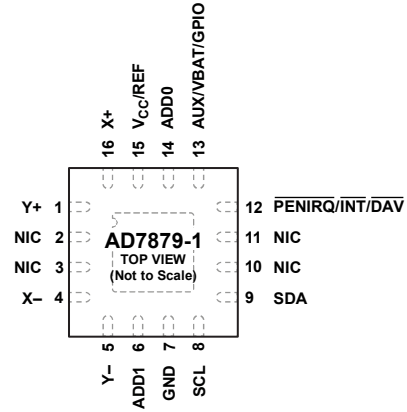
Pin No.		Mnemonic	Description
AD7879/ AD7889	AD7879-1/ AD7889-1		
1A	1A	AUX/VBAT/GPIO	This pin can be programmed as an auxiliary input to the ADC (AUX), as a battery measurement input to the ADC (VBAT), or as a GPIO.
1B	1B	$\overline{\text{PENIRQ}}/\overline{\text{INT}}/\overline{\text{DAV}}$	Interrupt Output. This pin is asserted when the screen is touched ($\overline{\text{PENIRQ}}$), when a measurement exceeds the preprogrammed limits ($\overline{\text{INT}}$), or when new data is available in the registers ($\overline{\text{DAV}}$). This pin is active low and has an internal 50 kΩ pull-up resistor.
1C	Not applicable	DOUT	SPI Serial Data Output for the AD7879/AD7889.
Not applicable	1C	SDA	I ² C Serial Data Input and Output for the AD7879-1/AD7889-1.
1D	1D	SCL	Serial Interface Clock Input.
2A	2A	V _{CC} /REF	Power Supply Input and ADC Reference.
2B	Not applicable	$\overline{\text{CS}}$	Chip Select for the SPI Serial Interface on the AD7879/AD7889. This pin is active low.
Not applicable	2B	ADD0	I ² C Address Bit 0 for the AD7879-1/AD7889-1. Tie this pin high or low to determine an address for the AD7879-1/AD7889-1 (see Table 25).
2C	Not applicable	DIN	SPI Serial Data Input to the AD7879/AD7889.
Not applicable	2C	ADD1	I ² C Address Bit 1 for the AD7879-1/AD7889-1. Tie this pin high or low to determine an address for the AD7879-1/AD7889-1 (see Table 25).
2D	2D	GND	Ground. This pin is the ground reference point for all circuitry on the AD7879/AD7889. Refer all analog input signals and any external reference signal to this voltage.
3A	3A	X+	Touch Screen Input Channel.
3B	3B	Y+	Touch Screen Input Channel.
3C	3C	X-	Touch Screen Input Channel.
3D	3D	Y-	Touch Screen Input Channel.



NOTES
 1. NIC = NO INTERNAL CONNECTION.
 2. THE EXPOSED PAD IS NOT CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE GROUND PLANE.

Figure 7. AD7879 LFCSP Pin Configuration

07867-007



NOTES
 1. NIC = NO INTERNAL CONNECTION.
 2. THE EXPOSED PAD IS NOT CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE GROUND PLANE.

Figure 8. AD7879-1 LFCSP Pin Configuration

07867-008

Table 7. LFCSP Pin Function Descriptions

Pin No.		Mnemonic	Description
AD7879	AD7879-1		
1	1	Y+	Touch Screen Input Channel.
2, 3, 10, 11	2, 3, 10, 11	NIC	No Internal Connection.
4	4	X-	Touch Screen Input Channel.
5	5	Y-	Touch Screen Input Channel.
6	Not applicable	DIN	SPI Serial Data Input to the AD7879.
Not applicable	6	ADD1	I ² C Address Bit 1 for the AD7879-1. Tie this pin high or low to determine an address for the AD7879-1 (see Table 25).
7	7	GND	Ground. This pin is the ground reference point for all circuitry on the AD7879. Refer all analog input signals and any external reference signal to this voltage.
8	8	SCL	Serial Interface Clock Input.
9	Not applicable	DOUT	SPI Serial Data Output for the AD7879.
Not applicable	9	SDA	I ² C Serial Data Input and Output for the AD7879-1.
12	12	$\overline{\text{PENIRQ}}/\text{INT}/\text{DAV}$	Interrupt Output. This pin is asserted when the screen is touched ($\overline{\text{PENIRQ}}$), when a measurement exceeds the preprogrammed limits ($\overline{\text{INT}}$), or when new data is available in the registers (DAV). This pin is active low and has an internal 50 k Ω pull-up resistor.
13	13	AUX/VBAT/GPIO	This pin can be programmed as an auxiliary input to the ADC (AUX), as a battery measurement input to the ADC (VBAT), or as a GPIO.
14	Not applicable	$\overline{\text{CS}}$	Chip Select for the SPI Serial Interface on the AD7879/AD7889. This pin is active low.
Not applicable	14	ADD0	I ² C Address Bit 0 for the AD7879-1/AD7889-1. Tie this pin high or low to determine an address for the AD7879-1/AD7889-1 (see Table 25).
15	15	V _{cc} /REF	Power Supply Input and ADC Reference.
16	16	X+	Touch Screen Input Channel.
		EP	Exposed Pad. The exposed pad is not connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 2.6 V, f_{SCL} = 2 MHz, unless otherwise noted.

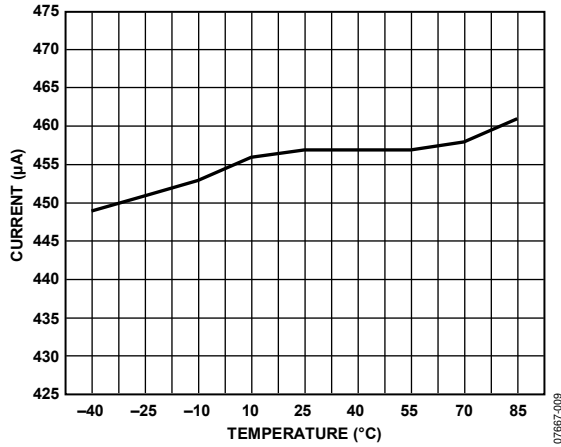


Figure 9. Supply Current vs. Temperature

07667-009

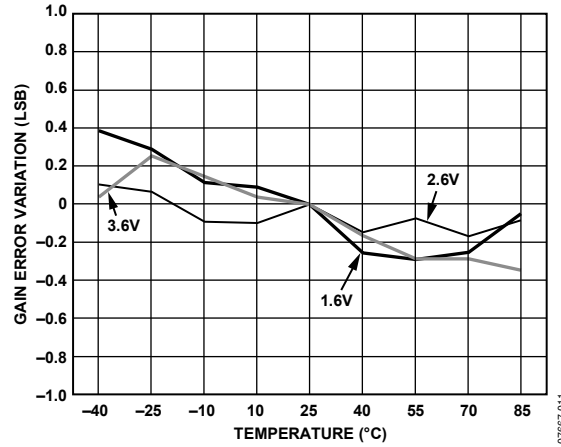


Figure 12. Change in ADC Gain vs. Temperature

07667-011

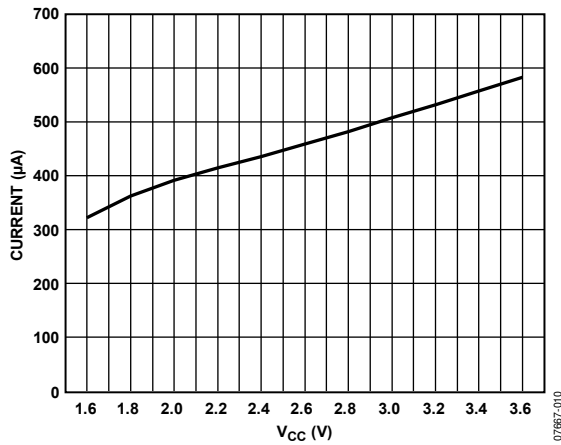


Figure 10. Supply Current vs. V_{CC}

07667-010

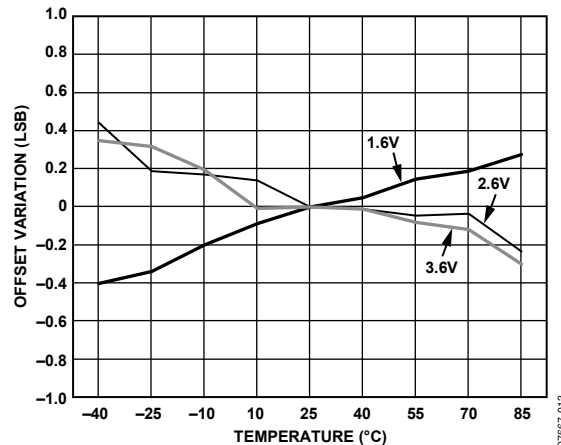


Figure 13. ADC Offset Variation vs. Temperature

07667-013

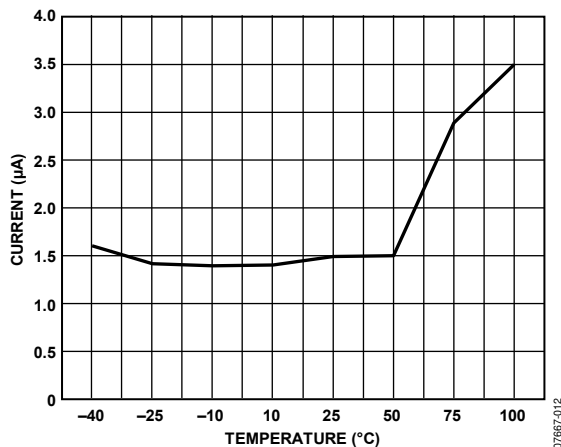


Figure 11. Full Power-Down Current (I_{BD}) vs. Temperature

07667-012

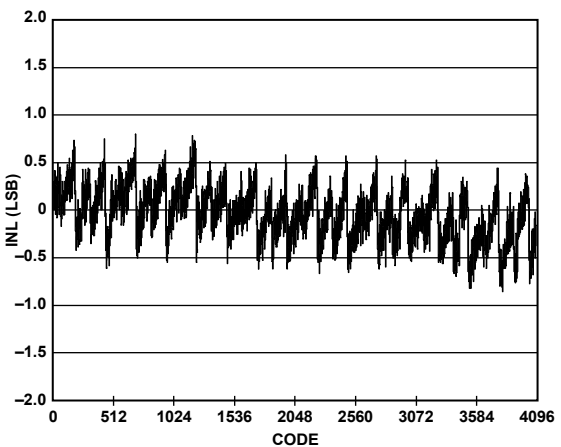


Figure 14. ADC INL

07667-014

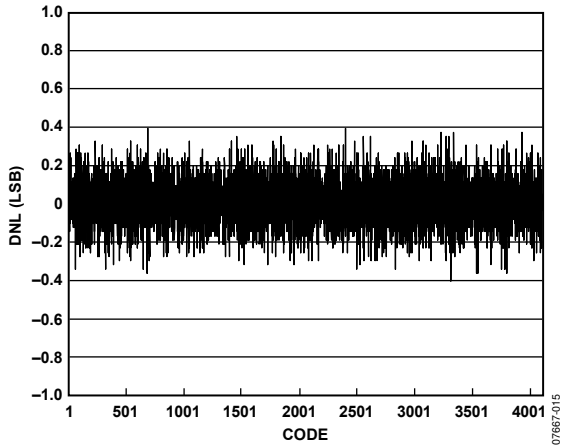


Figure 15. ADC DNL

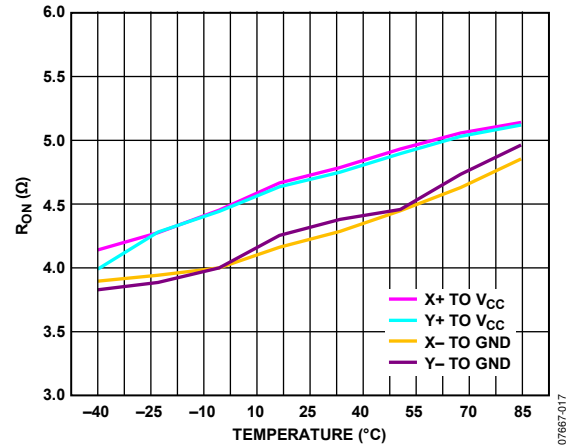


Figure 17. Switch On Resistance (R_{ON}) vs. Temperature (X+, Y+: Pin to V_{CC} ; X-, Y-: Pin to GND)

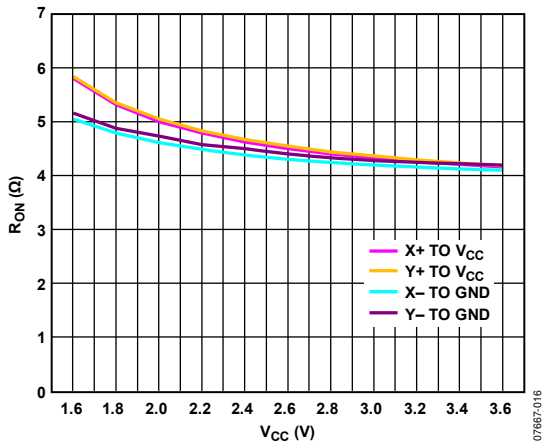


Figure 16. Switch On Resistance (R_{ON}) vs. V_{CC} (X+, Y+: Pin to V_{CC} ; X-, Y-: Pin to GND)

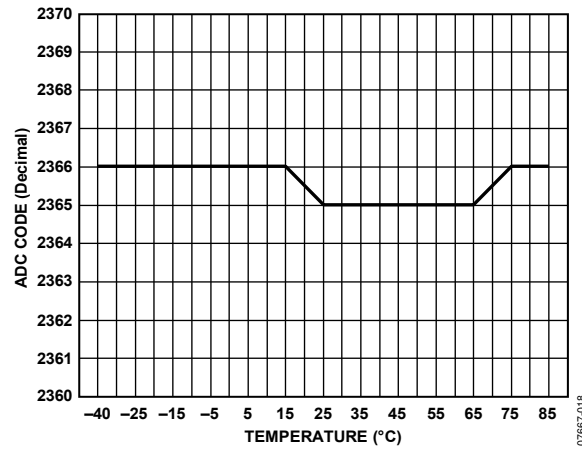


Figure 18. ADC Code vs. Temperature (Fixed Analog Input)

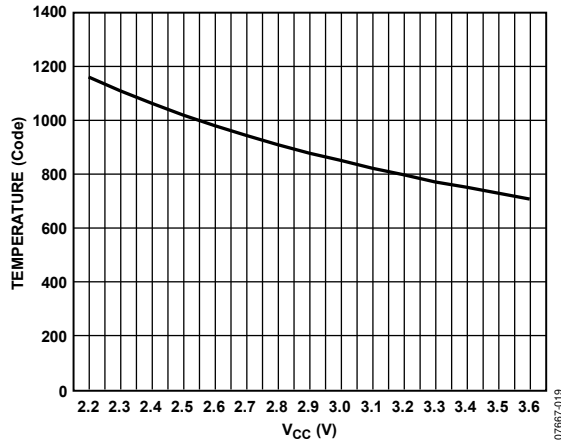


Figure 19. Temperature Code vs. V_{CC} for 25°C

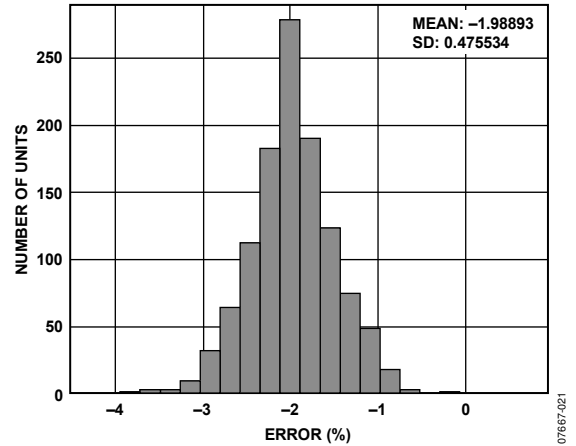


Figure 21. Typical Uncalibrated Accuracy for the Battery Channel (25°C)

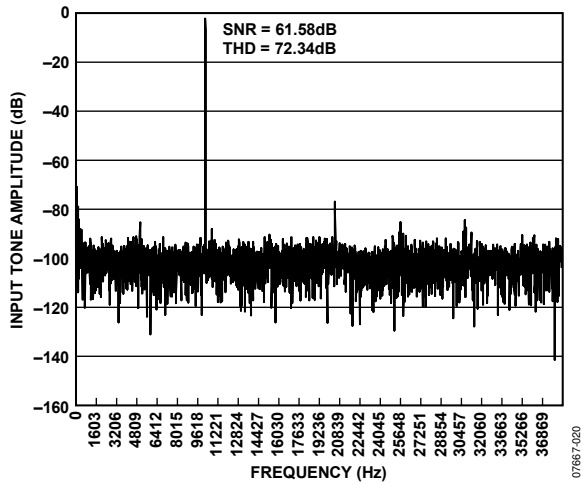


Figure 20. Typical FFT Plot for the Auxiliary Channels at a 25 kHz Sampling Rate and a 1 kHz Input Frequency

TERMINOLOGY

Differential Nonlinearity (DNL)

DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity (INL)

INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale at 1 LSB below the first code transition and full scale at 1 LSB above the last code transition.

Gain Error

Gain error is the deviation of the last code transition (111 ... 110 to 111 ... 111) from the ideal ($V_{REF} - 1 \text{ LSB}$) after the offset error has been calibrated out.

Offset Error

Offset error is the deviation of the first code transition (00 ... 000 to 00 ... 001) from the ideal (AGND + 1 LSB).

On Resistance

On resistance is a measure of the ohmic resistance between the drain and the source of the switch drivers.

THEORY OF OPERATION

The [AD7879/AD7889](#) are a complete 12-bit data acquisition system for digitizing positional inputs from a 4-wire resistive touch screen. To support this function, data acquisition on the [AD7879/AD7889](#) is highly programmable to ensure accurate and noise free results from the touch screen.

The core of the [AD7879/AD7889](#) is a high speed, low power, 12-bit ADC with an input multiplexer, on-chip track-and-hold, and an on-chip clock. Conversion results are stored in on-chip result registers. Compare the results from the auxiliary input or the battery input with high and low limits stored in the limit registers to generate an out of limit interrupt ($\overline{\text{INT}}$).

The [AD7879/AD7889](#) also contain low resistance analog switches to switch the X and Y excitation voltages to the touch screen and to the on-chip temperature sensor. The high speed SPI serial bus provides control of the devices, as well as communication with the devices. The [AD7879-1/AD7889-1](#) are available with an I²C interface.

Operating from a single supply from 1.6 V to 3.6 V, the [AD7879/AD7889](#) offer a throughput rate of 105 kHz. The device is available in a 1.6 mm × 2 mm, 12-ball wafer level chip scale package (WLCSP) and in a 4 mm × 4 mm, 16-lead, lead frame chip scale package (LFCSP).

The [AD7879/AD7889](#) have an on-chip sequencer that schedules a sequence of preprogrammed conversions. The conversion sequence starts automatically when the screen is touched or at preset intervals, using the on-board timer.

To ensure that the [AD7879/AD7889](#) work well with different touch screens, the user is able to select the acquisition time. A programmable delay ensures that the voltage on the touch screen settles before a measurement is taken.

To reduce noise in the system, the ADC takes up to 16 conversion results from each channel and writes the average of the results to the register. If there is noise present in the system, use the median filter to improve the performance of the [AD7879/AD7889](#).

TOUCH SCREEN PRINCIPLES

A 4-wire touch screen consists of two flexible, transparent, resistive coated layers typically separated by a small air gap (see Figure 22). The X layer has conductive electrodes running down the left and right edges, allowing the application of an excitation voltage across the X layer from left to right.

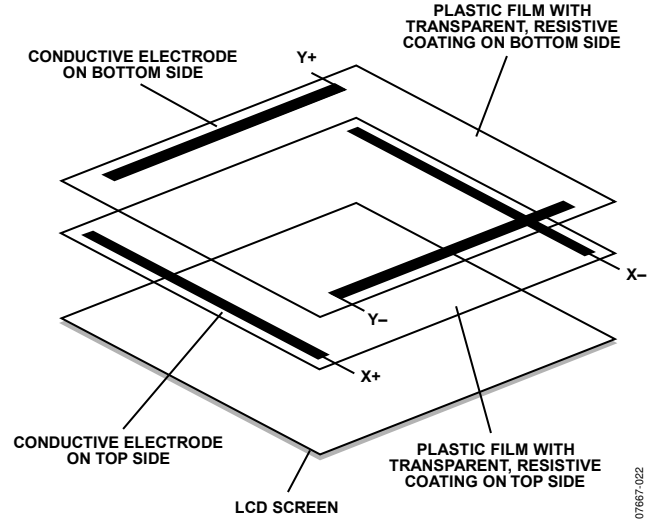


Figure 22. Basic Construction of a Touch Screen

The Y layer has conductive electrodes running along the top and bottom edges, allowing the application of an excitation voltage down the Y layer from top to bottom.

Provided that the layers are of uniform resistivity, the voltage at any point between the two electrodes is proportional to the horizontal position for the X layer and the vertical position for the Y layer.

When the screen is touched, the two layers make contact. If only the X layer is excited, the voltage at the point of contact and, therefore, the horizontal position, can be sensed at one of the Y layer electrodes. Similarly, if only the Y layer is excited, the voltage and, therefore, the vertical position, can be sensed at one of the X layer electrodes. By switching alternately between X and Y excitation and measuring the voltages, the X and Y coordinates of the contact point can be determined.

In addition to measuring the X and Y coordinates, it is also possible to estimate the touch pressure by measuring the contact resistance between the X and Y layers. The [AD7879/AD7889](#) facilitate this measurement.

Figure 23 shows an equivalent circuit of the analog input structure of the AD7879/AD7889, including the touch screen switches, the main analog multiplexer, the ADC, and the dual 3 to 1 multiplexer that selects the reference source for the ADC.

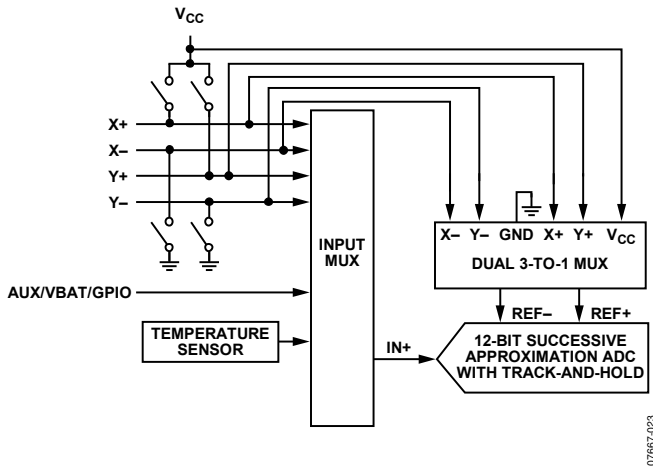


Figure 23. Analog Input Structure

The AD7879/AD7889 can be set up to automatically convert either specific input channels or a sequence of channels. The results of the ADC conversions are stored in the result registers.

When measuring the ancillary analog inputs (AUX, TEMP, or VBAT), the ADC uses a V_{CC} reference and the measurement is referred to GND.

MEASURING TOUCH SCREEN INPUTS

When measuring the touch screen inputs, it is possible to use V_{CC} as a reference or instead to use the touch screen excitation voltage as the reference and to perform a ratiometric, differential measurement. The differential method is the default method and is selected by clearing the SER/DFR bit (Bit 9 in Control Register 2) to 0. The single-ended method is selected by setting this bit to 1.

Single-Ended Method

Figure 24 shows the single-ended method for the Y position. For the X position, the excitation voltage is applied to X+ and X- and the voltage is measured at Y+.

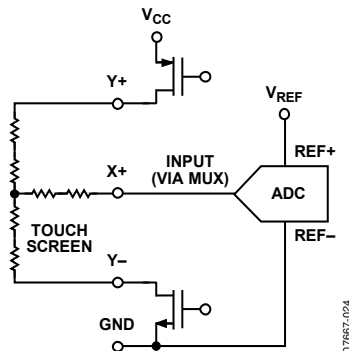


Figure 24. Single-Ended Conversion of Touch Screen Inputs

The voltage seen at the input to the ADC in Figure 24 is

$$V_{IN} = V_{CC} \times \frac{R_{Y-}}{R_{TOTAL}} \tag{1}$$

The advantage of the single-ended method is that the touch screen excitation voltage is switched off when the signal is acquired. Because a screen can draw over 1 mA, this is a significant consideration for a battery-powered system.

The disadvantage of the single-ended method is that voltage drops across the switches can introduce errors. Touch screens can have a total end-to-end resistance ranging from 200 Ω to 900 Ω. By taking the lowest screen resistance of 200 Ω and a typical switch resistance of 14 Ω, the user can reduce the apparent excitation voltage to $200/228 \times 100 = 87\%$ of its actual value. In addition, the voltage drop across the low-side switch adds to the ADC input voltage. This introduces an offset into the input voltage; thus, it can never reach 0.

Ratiometric Method

The ratiometric method illustrated in Figure 25 shows the negative input of the ADC reference connected to Y- and the positive input connected to Y+. Thus, the screen excitation voltage provides the reference for the ADC. The input of the ADC is connected to X+ to determine the Y position.

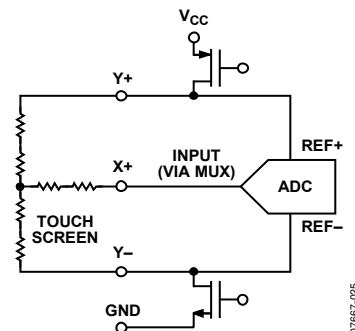


Figure 25. Ratiometric Conversion of Touch Screen Inputs

For greater accuracy, the ratiometric method has two significant advantages. One is that the reference to the ADC is provided from the actual voltage across the screen; therefore, any voltage dropped across the switches has no effect. The other advantage is that because the measurement is ratiometric, it does not matter if the voltage across the screen varies in the long term. However, it must not change after the signal has been acquired.

The disadvantage of the ratiometric method is that the screen must be powered up at all times because it provides the reference voltage for the ADC.

TOUCH PRESSURE MEASUREMENT

The pressure applied to the touch screen by a pen or a finger can also be measured with the AD7879/AD7889 by using simple calculations. The contact resistance between the X and Y plates is measured, providing a good indication of the size of the depressed area and, therefore, the applied pressure. The area of the spot that is touched is proportional to the size of the object touching it. The size of this resistance (R_{TOUCH}) can be calculated using two different methods.

First Method for Calculating the Size of R_{TOUCH}

The first method for calculating R_{TOUCH} requires the user to know the total resistance of the X-plate tablet (R_X). Three touch screen conversions are required: the measurement of the X position, $X_{POSITION}$ (Y+ input); the measurement of the X+ input with the excitation voltage applied to Y+ and X- (Z1 measurement); and the measurement of the Y- input with the excitation voltage applied to Y+ and X- (Z2 measurement). These three measurements are shown in Figure 26.

The AD7879/AD7889 has two special ADC channel settings that configure the X and Y switches for the Z1 and Z2 measurements and store the results in the Z1 and Z2 result registers. The Z1 measurement is selected by setting the CHNL ADD[2:0] bits to 101 in Control Register 1 (Address 0x01); the result is stored in the X+ (Z1) result register (Address 0x0A). The Z2 measurement is selected by setting the CHNL ADD[2:0] bits to 100 in Control Register 1 (Address 0x01); the result is stored in the Y- (Z2) result register (Address 0x0B).

The touch resistance (R_{TOUCH}) can then be calculated using Equation 2:

$$R_{TOUCH} = (R_{XPLATE}) \times (X_{POSITION}/4096) \times ((Z2/Z1) - 1) \quad (2)$$

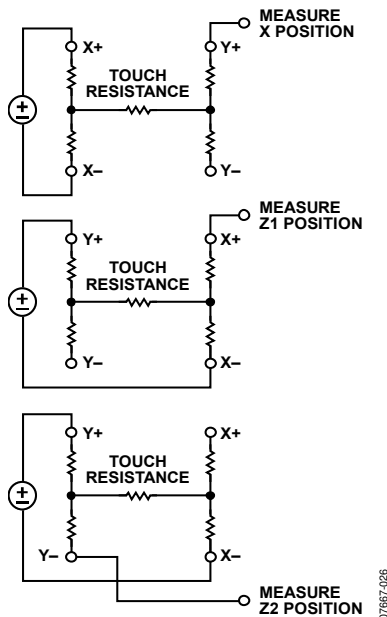


Figure 26. Three Measurements Required for Touch Pressure

Second Method for Calculating the Size of R_{TOUCH}

The second method for calculating R_{TOUCH} requires the user to know the resistance of the X-plate and Y-plate tablets. Three touch screen conversions are required: a measurement of the X position ($X_{POSITION}$), the Y position ($Y_{POSITION}$), and the Z1 position.

Equation 3 also calculates the touch resistance (R_{TOUCH}):

$$R_{TOUCH} = R_{XPLATE} \times (X_{POSITION}/4096) \times ((4096/Z1) - 1) - R_{YPLATE} \times (1 - (Y_{POSITION}/4096)) \quad (3)$$

TEMPERATURE MEASUREMENT

A temperature measurement option called the single-conversion method is available on the AD7879/AD7889. The conversion method requires only a single measurement on ADC Channel 001. The results are stored in the temperature conversion result register (Address 0x0D). The AD7879/AD7889 do not provide an explicit output of the temperature reading; the system must perform some external calculations. This method is based on an on-chip diode measurement.

The acquisition time is fixed at 16 ms for temperature measurement.

Conversion Method

The conversion method makes use of the fact that the temperature coefficient of a silicon diode is approximately $-2.1 \text{ mV}/^\circ\text{C}$. However, this small change is superimposed on the diode forward voltage, which can have a wide tolerance. Therefore, it is necessary to calibrate by measuring the diode voltage at a known temperature to provide a baseline from which the change in forward voltage with temperature can be measured. This method provides a resolution of approximately 0.3°C and a predicted accuracy of $\pm 2^\circ\text{C}$.

The temperature limit comparison is performed on the result in the temperature conversion result register (Address 0x0D), which is the measurement of the diode forward voltage. The values programmed into the high and low limits should be referenced to the calibrated diode forward voltage to make accurate limit comparisons.

Temperature Calculations

If an explicit temperature reading in degrees Celsius is required, calculate for the single measurement method as follows:

1. Calculate the scale factor of the ADC in degrees per LSB.

$$\text{Degrees per LSB} = \text{ADC LSB size} / -2.1 \text{ mV} = (V_{CC}/4096) / -2.1 \text{ mV}$$

2. Save the ADC output, D_{CAL} , at the calibration temperature, T_{CAL} .
3. Take the ADC reading, D_{AMB} , at the temperature to be measured, T_{AMB} .
4. Calculate the difference in degrees between T_{CAL} and T_{AMB} by

$$\Delta T = (D_{AMB} - D_{CAL}) \times \text{degrees per LSB}$$

5. Add ΔT to T_{CAL} .

Example

Using $V_{CC} = 2.5 \text{ V}$ as reference,

$$\text{Degrees per LSB} = (2.5/4096) / -2.1 \times 10^{-3} = -0.291$$

The ADC output is 983 decimal at 25°C, equivalent to a diode forward voltage of 0.6 V.

The ADC output at T_{AMB} is 880.

$$\Delta T = (880 - 983) \times -0.291 = 30^\circ\text{C}$$

$$T_{AMB} = 25 + 30 = 55^\circ\text{C}$$

MEDIAN AND AVERAGING FILTERS

As explained in the Touch Screen Principles section, touch screens are composed of two resistive layers, normally placed over an LCD screen. Because these layers are in close proximity to the LCD screen, noise can be coupled from the screen onto these resistive layers, causing errors in the touch screen positional measurements.

The AD7879/AD7889 contain a filtering block to process the data and discard the spurious noise before sending the information to the host. The purpose of this block is not only the suppression of noise; the on-chip filtering also greatly reduces the host processing loading.

The processing function consists of two filters that are applied to the converted results: the median filter and the averaging filter.

The median filter suppresses the isolated out of range noise and sets the number of measurements to be taken. These measurements are arranged in a temporary array, where the first value is the smallest measurement and the last value is the largest measurement. Bit 6 and Bit 5 in Control Register 2 (MED1 and MED0, respectively) set the window of the median filter and, therefore, the number of measurements taken.

Table 8. Median Filter Size

MED1	MED0	Number of Measurements
0	0	Median filter disabled
0	1	4
1	0	8
1	1	16

The averaging filter size determines the number of values to average. Bit 8 and Bit 7 in Control Register 2 (AVG1, AVG0) set the average to 2, 4, 8, or 16 samples. Only the final averaged result is written into the result register.

Table 9. Averaging Filter Size

AVG1	AVG0	Filter Size
0	0	Average of 2 middle samples
0	1	Average of 4 middle samples
1	0	Average of 8 middle samples
1	1	Average of 16 samples

When both filter values are 00, only one measurement is transferred to the register map.

The number specified with the MED1 and MED0 settings must be greater than or equal to the number specified with the AVG1 and AVG0 settings. If both settings specify the same number, the median filter is switched off.

Table 10. Median Averaging Filters (MAVF) Settings

Setting	Function
M = A	Median filter is disabled; output is the average of A converted results
M > A	Output is the average of the middle A values from the array of M measurements
M < A	Not possible because the median filter size is always larger than the averaging window size

Example

In this example, MED1, MED0 = 11 and AVG1, AVG0 = 10; the median filter has a window size of 16. This means that 16 measurements are taken and arranged in descending order in a temporary array.

The averaging window size in this example is 8. The output is the average of the middle eight values of the 16 measurements taken with the median filter.

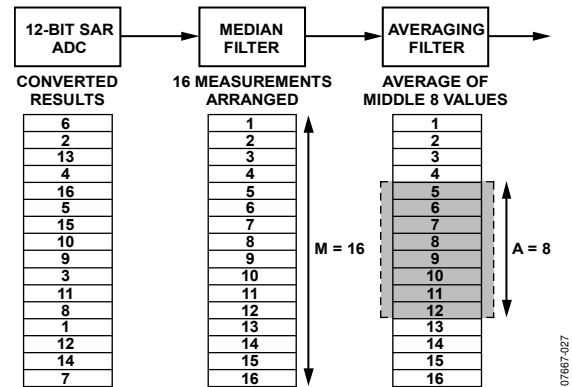


Figure 27. Median and Averaging Filter Example

It takes approximately 2 μs to sort the data in the rank filter (t_{SORT} in Figure 33); t_{SORT} adds to the update rate of the AD7879.

AUX/VBAT/GPIO PIN

The AUX/VBAT/GPIO pin on the AD7879/AD7889 can be programmed as an auxiliary input to the ADC, as a battery monitoring input or as a GPIO. To select the auxiliary measurement, set the ADC channel address to 011 (Bits[14:12] in Control Register 1, Address 0x01). To select a battery measurement, set the ADC channel address to 010. To select the GPIO function, set Bit 13 in Control Register 2 (Address 0x02) to 1.

AUXILIARY INPUT

The AD7879/AD7889 have an auxiliary analog input, AUX. When the auxiliary input function is selected, the signal on the AUX pin (AUX/VBAT/GPIO) is connected directly to the ADC input. This channel has a full-scale input range from 0 V to V_{CC} . The ADC channel address for AUX is 011 (Bits[14:12] in Control Register 1, Address 0x01), and the result is stored in the AUX/VBAT result register (Address 0x0C).

BATTERY INPUT

The AD7879/AD7889 can monitor battery voltages from 0.5 V to 5 V when the BAT measurement is selected. Figure 28 shows a block diagram of a battery voltage monitored through the VBAT pin. The voltage to the V_{CC} pin (V_{CC}/REF) of the AD7879/AD7889 is maintained at the desired supply voltage via the dc-to-dc converter, and the input to the converter is monitored. This voltage on VBAT is divided by 4 internally, so that a 5 V battery voltage is presented to the ADC as 1.25 V. To conserve power, the divider circuit is on only during the sampling of a voltage on VBAT. Note that the possible maximum input is 5 V.

The ADC channel address for VBAT is 010 (Bits[14:12] in Control Register 1, Address 0x01), and the result is stored in the AUX/VBAT result register (Address 0x0C).

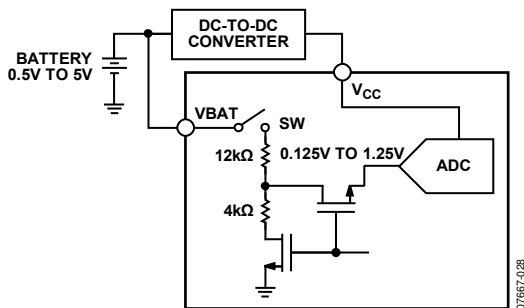


Figure 28. Block Diagram of Battery Measurement Circuit

The maximum battery voltage that the AD7879/AD7889 can measure changes when a different reference voltage is used. The maximum voltage that is measurable is $V_{CC} \times 4$ because this voltage gives a full-scale output from the ADC. Calculate the battery voltage using the following formula:

$$VBAT (V) = ((Register Value) \times V_{CC} \times 4) / 4095$$

LIMIT COMPARISON

The AUX measurement and the battery measurement can be compared with high and low limits stored on chip. An out of limit result generates an alarm output at the INT pin ($\overline{PENIRQ}/\overline{INT}/\overline{DAV}$) when the INT function is enabled. The high limit for both channels is stored in the AUX/VBAT high limit register (Address 0x04), and the low limit is stored in the AUX/VBAT low limit register (Address 0x05).

After a measurement from either AUX or VBAT is taken, it is compared with the high and low limits. The out of limit comparison sets a status bit in Control Register 3. Separate status bits for the high limit and the low limit indicate which limit was exceeded. The interrupt sources can be masked by clearing the corresponding enable bit in Control Register 3.

GPIO

The AD7879/AD7889 have one general-purpose logic input/output pin, GPIO (AUX/VBAT/GPIO). To enable GPIO, set Bit 13 in Control Register 2 to 1. If this bit is set to 0, the AUX/VBAT function is active on the pin. If the GPIO is not enabled, the other GPIO configuration bits have no effect.

The GPIO data bit is Bit 12 in Control Register 2.

Direction (Bit 11, Control Register 2, Address 0x02)

Bit 11 sets the direction of the GPIO pin (AUX/VBAT/GPIO). When GPIO DIR = 0, the pin is an output. Setting or clearing the GPIO data bit (Bit 12 in Control Register 2) outputs a value on the GPIO pin.

When GPIO DIR = 1, the pin is an input. An input value on the GPIO pin sets or clears the GPIO data bit (Bit 12 in Control Register 2). GPIO data register bits are read-only when GPIO DIR = 1.

Polarity (Bit 10, Control Register 2, Address 0x02)

When GPIO POL = 0, the GPIO pin is active low. When GPIO POL = 1, the GPIO pin is active high. How this bit affects the GPIO operation also depends on the GPIO DIR bit.

If GPIO POL = 1 and GPIO DIR = 1, a 1 at the input pin sets the corresponding GPIO data register bit to 1. A 0 at the input pin clears the corresponding GPIO data bit to 0.

If GPIO POL = 1 and GPIO DIR = 0, a 1 in the GPIO data register bit puts a 1 on the corresponding GPIO output pin. A 0 in the GPIO data register bit puts a 0 on the GPIO output pin.

If GPIO POL = 0 and GPIO DIR = 1, a 1 at the input pin sets the corresponding GPIO data bit to 0. A 0 at the input pin clears the corresponding GPIO data bit to 1.

If GPIO POL = 0 and GPIO DIR = 0, a 1 in the GPIO data register bit puts a 0 on the corresponding GPIO output pin. A 0 in the GPIO data register bit puts a 1 on the GPIO output pin.

GPIO Interrupt Enable (Bit 12, Control Register 3, Address 0x03)

The GPIO pin can operate as an interrupt source to trigger the $\overline{\text{INT}}$ output. This is controlled by Bit 12 in Control Register 3.

If the $\overline{\text{GPIO_ALERT}}$ interrupt enable bit is set to 0, the GPIO can trigger $\overline{\text{INT}}$. If this bit is set to 1, the GPIO cannot trigger $\overline{\text{INT}}$.

$\overline{\text{INT}}$ is asserted if the GPIO data register bit is set when the GPIO is configured as an input, provided that $\overline{\text{INT}}$ is enabled. $\overline{\text{INT}}$ is triggered only when the GPIO is configured as an input, that is, when $\text{GPIO_DIR} = 1$.

$\overline{\text{INT}}$ is cleared only when the GPIO signal or the GPIO enable bit changes.

CONVERSION TIMING

Conversion timing or update rate is the rate at which the AD7879/AD7889 provides converted values from the ADC so that the XY positions in the touch screen can be updated. In other words, the update rate is the timing required to give valid measurements in the sequencer.

Figure 29 shows conversion timing for a conversion sequence.

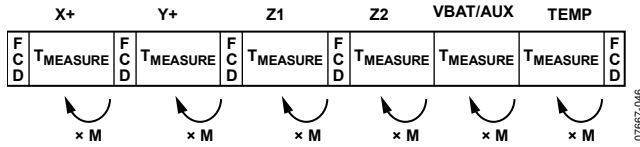


Figure 29. Conversion Timing Sequence

FCD is required before each touch screen measurement (X+, Y+, Z1, and Z2). This time is required to allow the screen inputs to settle before converting. If the sequence does not contain any screen channel (VBAT, AUX, or TEMP), only one FCD is added at the start of the sequence. At the end of the sequence, there is always another FCD.

$T_{MEASURE}$ is the time required to perform one measurement in the conversion sequence.

$$T_{MEASURE} = (ACQ (2 \mu s, 4 \mu s, 8 \mu s, 16 \mu s) + T_{CONV} (7.5 \mu s) + T_{SORT} (2 \mu s))$$

where:

ACQ is the acquisition time which is programmable in Control Register 1. For temperature measurements, ACQ is fixed at 16 μs .

T_{CONV} (typical ADC conversion time) is specified at 7.5 μs .

T_{SORT} is the time needed to sort the new sample within the median filter array. The T_{SORT} value is approximately 2 μs . If a median filter is not used ($MED = 0$), the T_{SORT} value is 0.

$$T_{MEASURE_MIN} = 9.5 \mu s (ACQ = 2 \mu s, \text{no median filter})$$

Conversion time per channel depends on the number of samples to be converted. The number of samples is programmed using the following median filter settings:

$$T_{CHANNEL} = T_{MEASURE} \times MED$$

$$T_{CHANNEL_MIN} = 9.5 \mu s (ACQ = 2 \mu s, MED = 0)$$

$$T_{CHANNEL_MAX} = 376 \mu s (ACQ = 16 \mu s, MED = 16)$$

$$Update Rate = (FCD + (T_{MEASURE} \times MED)) \times N + FCD + TMR$$

where:

MED = median filter setting (1, 4, 8, 16).

N = number of channels to be measured (1 to 6).

TMR = timer setting (0 μs to 9.4 ms).

The total update rate depends on the median filter settings and the number of channels in the conversion sequence. The timer setting (TMR) allows the user more flexibility to program the update rate.

For example, if

$$ACQ = 4 \mu s$$

$$MED = 8$$

$$N = 2$$

$$FCD = 1.024 \text{ ms}$$

$$TMR = 620 \mu s$$

$$T_{MEASURE} = 4 + 7.5 + 2 = 13.5 \mu s$$

$$T_{CHANNEL} = (13.5 \times 8) = 108 \mu s$$

$$\text{Then, Update Rate} = (1024 + 108) \times 2 + 1024 + 620 = 3.9 \text{ ms}$$

REGISTER MAP

Table 11. Register Table

Address ¹	Register Name	Description	Default Value	Type
0x00	Unused	Unused	0x0000	R/W
0x01	Control Register 1	Pen interrupt enable, channel selection for manual conversion, ADC mode, acquisition time, and conversion timer	0x0000	R/W
0x02	Control Register 2	ADC power management, GPIO control, pen interrupt mode, averaging, median filter, software reset, and FCD	0x4040	R/W
0x03	Control Register 3	Status of high/low limit comparisons for TEMP and AUX/VBAT, and enable bits to allow them to become interrupts; channel selection for slave/master mode	0x0000	R/W
0x04	AUX/VBAT high limit	AUX/VBAT high limit for comparison	0x0000	R/W
0x05	AUX/VBAT low limit	AUX/VBAT low limit for comparison	0x0000	R/W
0x06	TEMP high limit	TEMP high limit for comparison	0x0000	R/W
0x07	TEMP low limit	TEMP low limit for comparison	0x0000	R/W
0x08	X+	X+ measurement for Y position	0x0000	R
0x09	Y+	Y+ measurement for X position	0x0000	R
0x0A	X+ (Z1)	X+ measurement for touch pressure calculation (Z1)	0x0000	R
0x0B	Y- (Z2)	Y- measurement for touch pressure calculation (Z2)	0x0000	R
0x0C	AUX/VBAT	AUX/VBAT voltage measurement	0x0000	R
0x0D	TEMP	Temperature conversion measurement	0x0000	R
0x0E	Revision and device ID	Revision and device ID	0x0379 (AD7879-1/AD7889-1) 0x037A (AD7879/AD7889)	R R

¹ Do not write to addresses outside the register map.

DETAILED REGISTER DESCRIPTIONS

All addresses and default values are expressed in hexadecimal.

Table 12. Control Register 1

Address	Bit Name	Data Bit	Description	Default Value
0x01	Disable PENIRQ	15	Pen interrupt enable. 0 = $\overline{\text{PENIRQ}}$ is enabled. 1 = $\overline{\text{PENIRQ}}$ is disabled and $\overline{\text{INT}}$ is enabled.	0x0000
	CHNL ADD[2:0]	[14:12]	ADC channel address for manual conversion (ADC mode = 01). 111 = X+ input (Y position). 110 = Y+ input (X position). 101 = X+ (Z1) input for touch-pressure calculation. 100 = Y- (Z2) input (used for touch-pressure measurement). 011 = AUX input. ¹ 010 = VBAT input. ¹ 001 = temperature measurement. 000 = not applicable.	
	ADC MODE[1:0]	[11:10]	ADC mode. 00 = no conversion. 01 = single conversion. ² 10 = conversion sequence (slave mode). ² 11 = conversion sequence (master mode).	
	ACQ[1:0]	[9:8]	ADC acquisition time. 00 = 4 clock periods (2 μs). 01 = 8 clock periods (4 μs). 10 = 16 clock periods (8 μs). 11 = 32 clock periods (16 μs). Note that the acquisition time does not apply to the temperature sensor channels; the temperature channel has a constant settling time of 16 μs .	
	TMR[7:0]	[7:0]	Conversion interval timer. Starts at 550 μs (00000001) and continues to 9.440 ms (11111111) in steps of 35 μs (see Table 18). Note that, in slave mode, the conversion interval timer starts to count as soon as the conversion sequence is finished; in master mode, it starts to count again only if the screen remains touched. If the screen is released, the timer stops counting and, on the next screen touch, a conversion starts immediately.	

¹ If GPIO is enabled in Control Register 2 (Bit 13), AUX and VBAT are both ignored. If AUX and VBAT are both selected in Control Register 3 and GPIO is disabled, AUX is ignored and VBAT is measured.

² Note that these bits are cleared to 00 at the end of the conversion sequence if the conversion interval timer bits in Control Register 1 (Address 0x01) Bits[7:0] = 0x00 at the end of the conversion sequence.

Table 13. Control Register 2

Address	Bit Name	Data Bit	Description	Default Value
0x02	PM[1:0]	[15:14]	ADC power management. 00 = full shutdown; the ADC, oscillator, bias, and temperature sensor are all powered down. 01 = analog blocks to be powered down depend on the ADC mode. If ADC mode is master mode, the ADC, oscillator, bias, and temperature sensor are powered down and must wake up when the user touches the screen. If ADC mode is slave mode, the ADC and temperature sensor are powered down when not being used. They wake up automatically when required. The oscillator and bias are powered up because they are needed to measure time. This also applies to the single-conversion mode. 10 = ADC, bias, and oscillator are powered up continuously, irrespective of ADC mode. 11 = same as 01.	0x4040
	GPIO EN	13	GPIO enable. 0 = AUX/VBAT channel active. 1 = GPIO enabled on AUX/VBAT/GPIO pin.	
	GPIO DAT	12	GPIO data bit.	
	GPIO DIR	11	GPIO direction. 0 = output. 1 = input.	
	GPIO POL	10	GPIO polarity. 0 = GPIO pin is active low. 1 = GPIO pin is active high.	
	SER/DFR	9	Selects normal (single-ended) or ratiometric (differential) conversion. 0 = ratiometric (differential). 1 = normal (single-ended).	
	AVG[1:0]	[8:7]	ADC averaging. 00 = 2 middle values averaged (one measurement when median filter is disabled). 01 = 4 middle values averaged. 10 = 8 middle values averaged. 11 = 16 values averaged.	
	MED[1:0]	[6:5]	Median filter size. 00 = median filter disabled. 01 = 4 measurements. 10 = 8 measurements. 11 = 16 measurements.	
	SW/RST	4	Software reset; digital logic is reset when this bit is set.	
	FCD[3:0]	[3:0]	ADC first conversion delay. ¹ Starts at 128 μ s (default) and continues to 4.096 ms in steps of 128 μ s (see Table 22).	

¹ This delay occurs before conversion of the X and Y coordinate channels (including Z1 and Z2) to allow screen settling and before the first conversion to allow the ADC to power up.

Table 14. Control Register 3

Address	Bit Name	Data Bit	Description	Default Value
0x03	TEMP MASK	15	TEMP mask bit. 0 = temperature measurement is allowed to cause interrupt. 1 = temperature measurement is not allowed to cause interrupt.	0x0000
	AUX/VBAT MASK	14	AUX/VBAT mask bit. 0 = AUX/VBAT measurement is allowed to cause interrupt. 1 = AUX/VBAT measurement is not allowed to cause interrupt.	
	INT MODE	13	$\overline{\text{DAV}}/\overline{\text{INT}}$ mode select. 0 = enable $\overline{\text{DAV}}$ mode. 1 = enable $\overline{\text{INT}}$ mode. This bit overrides any mask bits associated with individual channels.	
	GPIO ALERT	12	GPIO interrupt enable. 0 = GPIO can cause an alert on the $\overline{\text{INT}}$ output. 1 = mask GPIO from causing an alert on the $\overline{\text{INT}}$ output.	
	AUX/VBAT LOW	11	1 = AUX/VBAT below low limit.	
	AUX/VBAT HIGH	10	1 = AUX/VBAT above high limit.	
	TEMP LOW	9	1 = TEMP below low limit.	
	TEMP HIGH	8	1 = TEMP above high limit.	
	X+	7	1 = include measurement of Y position (X+ input).	
	Y+	6	1 = include measurement of X position (Y+ input).	
	Z1	5	1 = include Z1 touch-pressure measurement (X+ input).	
	Z2	4	1 = include measurement of Z2 touch-pressure measurement (Y- input).	
	AUX	3	1 = include measurement of AUX channel. ¹	
	VBAT	2	1 = include measurement of battery monitor (VBAT). ¹	
	TEMP	1	1 = include temperature measurement.	
Not used	0	Unused.		

¹ If GPIO is enabled in Control Register 2 (Bit 13), AUX and VBAT are both ignored. If AUX and VBAT are both selected and GPIO is disabled, AUX is ignored and VBAT is measured.

Table 15. Limit Registers

Address	Register Name	Data Bit	Description	Default Value
0x04	AUX/VBAT high limit	[15:0]	User-programmable AUX/VBAT high limit register	0x0000
0x05	AUX/VBAT low limit	[15:0]	User-programmable AUX/VBAT low limit register	0x0000
0x06	TEMP high limit	[15:0]	User-programmable TEMP high limit register	0x0000
0x07	TEMP low limit	[15:0]	User-programmable TEMP low limit register	0x0000

Table 16. Measurement Result Registers (Read Only)

Address	Register Name	Data Bits	Description	Default Value
0x08	X+	[15:0]	Measured X+ input with Y excitation (Y position)	0x0000
0x09	Y+	[15:0]	Measured Y+ input with X excitation (X position)	0x0000
0x0A	X+ (Z1)	[15:0]	Measured X+ input with X– and Y+ excitation (touch-pressure calculation Z1)	0x0000
0x0B	Y– (Z2)	[15:0]	Measured Y– input with X– and Y+ excitation (touch-pressure calculation Z2)	0x0000
0x0C	AUX/VBAT	[15:0]	AUX/VBAT voltage measurement	0x0000
0x0D	TEMP	[15:0]	Temperature conversion measurement	0x0000

Table 17. Revision and Device ID Register (Read Only)

Address	Data Bits	Description	Default Value
0x0E	[15:12]	Unused	0x0379 (AD7879-1/AD7889-1)
	[11:8]	Revision and device ID bits	0x037A (AD7879/AD7889)
	[7:0]	Device ID	