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2-Channel, 2.35 V to 5.25 V, 1 MSPS, 10-/12-Bit ADCs

AD7912/AD7922

FEATURES

Fast throughput rate: 1 MSPS
Specified for V_{DD} of 2.35 V to 5.25 V
Low power:
- **4.8 mW typ at 1 MSPS with 3 V supplies**
- **15.5mW typ at 1 MSPS with 5 V supplies**

Wide input bandwidth:
- **71 dB minimum SNR at 100 kHz input frequency**

Flexible power/serial clock speed management
No pipeline delays
High speed serial interface:
- **SPI®/QSPI™/MICROWIRE™/DSP compatible**

Standby mode: 1 µA maximum
Daisy-chain mode
8-lead TSOT package
8-lead MSOP package

APPLICATIONS

Battery-powered systems:
- **Personal digital assistants**
- **Medical instruments**
- **Mobile communications**

Instrumentation and control systems
Data acquisition systems
High speed modems
Optical sensors

GENERAL DESCRIPTION

The AD7912/AD7922[1] are 10-bit and 12-bit, high speed, low power, 2-channel successive approximation ADCs, respectively. The parts operate from a single 2.35 V to 5.25 V power supply and feature throughput rates of up to 1 MSPS. The parts contain a low noise, wide bandwidth track-and-hold amplifier, which can handle input frequencies in excess of 6 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The conversion rate is determined by the SCLK signal. The input signal is sampled on the falling edge of $\overline{CS}$ and the conversion is also initiated at this point. The channel to be converted is selected through the DIN pin, and the mode of operation is controlled by $\overline{CS}$. The serial data stream from the DOUT pin has a channel identifier bit and mode identifier bit, which provide information about the converted channel and the current mode of operation.

FUNCTIONAL BLOCK DIAGRAM

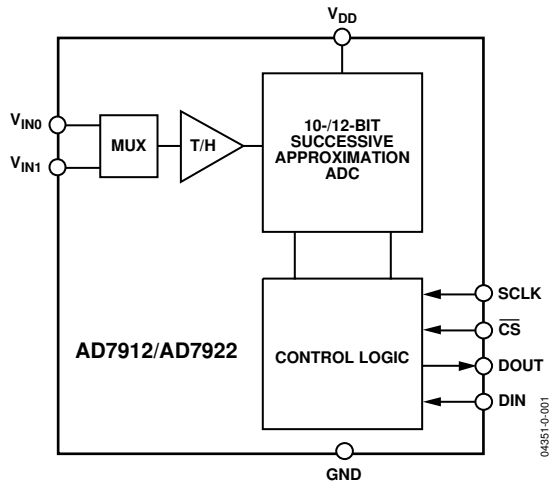

Figure 1.

Several AD7912/AD7922 can be connected together in a daisy chain. The AD7912/AD7922 feature a daisy-chain mode that allows the user to read the conversion results from the ADCs contained in the chain. The AD7912/AD7922 use advanced design techniques to achieve very low power dissipation at high throughput rates. The reference for the part is taken internally from V_{DD}, thereby allowing the widest dynamic input range to the ADC.

PRODUCT HIGHLIGHTS

1. 2-channel, 1 MSPS, 10-/12-bit ADCs in TSOT package.
2. High throughput with low power consumption.
3. Flexible power/serial clock speed management.
   The conversion rate is determined by the serial clock. The parts also feature a power-down mode to maximize power efficiency at lower throughput rates. Average power consumption is reduced when the power-down mode is used while not converting. Current consumption is 1 µA maximum and 50 nA typically when in power-down mode.
4. Daisy-chain mode.
5. No pipeline delay.
   The parts feature a standard successive approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once-off conversion control.

[1] Protected by U.S. Patent Number 6,681,332.

Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

SPECIFICATIONS

AD7912 SPECIFICATIONS

Temperature range for A Grade from −40°C to +85°C.
V_{DD} = 2.35 V to 5.25 V, f_{SCLK} = 18 MHz, f_{SAMPLE} = 1 MSPS; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	A Grade[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 100 kHz sine wave
Signal-to- Noise + Distortion (SINAD)[2]	61	dB min	
Total Harmonic Distortion (THD)[2]	−71	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	−72	dB max	
Intermodulation Distortion (IMD)[2]			
Second-Order Terms	−82	dB typ	fa = 100.73 kHz, fb = 90.7 kHz
Third-Order Terms	−83	dB typ	fa = 100.73 kHz, fb = 90.7 kHz
Aperture Delay	10	ns typ	
Aperture Jitter	30	ps typ	
Channel-to-Channel Isolation[2]	90	dB typ	
Full Power Bandwidth	8.5	MHz typ	@ 3 dB
	1.5	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity[2]	±0.5	LSB max	
Differential Nonlinearity[2]	±0.5	LSB max	Guaranteed no missed codes to 10 bits
Offset Error[2]	±0.5	LSB max	
Offset Error Match[2, 3]	±0.3	LSB max	
Gain Error[2]	±0.5	LSB max	
Gain Error Match[2, 3]	±0.3	LSB max	
Total Unadjusted Error (TUE)[2]	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	V	
DC Leakage Current	±0.3	µA max	
Input Capacitance	20	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 (V_{DD})	V min	2.35 V ≤ V_{DD} ≤ 2.7 V
	2	V min	2.7 V < V_{DD} ≤ 5.25 V
Input Low Voltage, V_{INL}	0.3	V max	V_{DD} = 2.35 V
	0.2 (V_{DD})	V max	2.35 V < V_{DD} ≤ 2.7 V
	0.8	V max	2.7 V < V_{DD} ≤ 5.25 V
Input Current, I_{IN}, SCLK Pin	±0.3	µA max	Typically 8 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±0.3	µA max	
Input Current, I_{IN}, DIN Pin	±0.3	µA max	
Input Capacitance, C_{IN}[3]	5	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA, V_{DD} = 2.35 V to 5.25 V
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±0.3	µA max	
Floating-State Output Capacitance[3]	5	pF max	
Output Coding	Straight (natural) binary		

Parameter	A Grade[1]	Unit	Test Conditions/Comments
CONVERSION RATE			
Conversion Time	777	ns max	14 SCLK cycles with SCLK at 18 MHz
Track-and-Hold Acquisition Time[2]	290	ns max	
Throughput Rate	1	MSPS max	
POWER REQUIREMENTS			
V_{DD}	2.35/5.25	V min/max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	3	mA typ	V_{DD} = 4.75 V to 5.25 V, SCLK on or off
	1.5	mA typ	V_{DD} = 2.35 V to 3.6 V, SCLK on or off
Normal Mode (Operational)	4	mA max	V_{DD} = 4.75 V to 5.25 V, f_{SAMPLE} = 1 MSPS
	2	mA max	V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = 1 MSPS
Full Power-Down Mode (Static)	1	µA max	SCLK on or off, typically 50 nA
Full Power-Down Mode (Dynamic)	0.48	mA typ	V_{DD} = 5 V, f_{SCLK} = 18 MHz, f_{SAMPLE} = 100 kSPS
	0.26	mA typ	V_{DD} = 3 V, f_{SCLK} = 18 MHz, f_{SAMPLE} = 100 kSPS
Power Dissipation[4]			
Normal Mode (Operational)	20	mW max	V_{DD} = 5 V, f_{SAMPLE} = 1 MSPS
	6	mW max	V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS
Full Power-Down	5	µW max	V_{DD} = 5 V

[1] Operational from V_{DD} = 2 V, with V_{IH} = 1.9 V minimum and V_{IL} = 0.1 V maximum.
[2] See the Terminology section.
[3] Guaranteed by characterization.
[4] See the Power vs. Throughput Rate section.

AD7922 SPECIFICATIONS

Temperature range for A Grade from −40°C to +85°C.
V_{DD} = 2.35 V to 5.25 V, f_{SCLK} = 18 MHz, f_{SAMPLE} = 1 MSPS; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	A Grade[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 100 kHz sine wave
Signal-to-Noise + Distortion (SINAD)[2]	70	dB min	
	72	dB typ	
Signal-to-Noise Ratio (SNR)[2]	71	dB min	
	72.5	dB typ	
Total Harmonic Distortion (THD)[2]	−81	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[2]	−84	dB typ	
Intermodulation Distortion (IMD)[2]			
Second-Order Terms	−84	dB typ	fa = 100.73 kHz, fb = 90.72 kHz
Third-Order Terms	−86	dB typ	fa = 100.73 kHz, fb = 90.72 kHz
Aperture Delay	10	ns typ	
Aperture Jitter	30	ps typ	
Channel-to-Channel Isolation[2]	90	dB typ	
Full Power Bandwidth	8.5	MHz typ	@ 3 dB
	1.5	MHz typ	@ 0.1dB
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity[2]	±1.5	LSB max	V_{DD} = 2.35 V to 3.6V
	±0.7	LSB typ	V_{DD} = 4.75 V to 5.25V
Differential Nonlinearity[2]			Guaranteed no missed codes to 12 bits
	−0.9/+1.5	LSB max	V_{DD} = 2.35 V to 3.6V
	−0.7/+1.2	LSB typ	V_{DD} = 4.75 V to 5.25V
Offset Error[2]	±1	LSB max	V_{DD} = 2.35 V to 3.6V
	±0.1	LSB typ	V_{DD} = 4.75 V to 5.25V
Offset Error Match[2, 3]	±0.5	LSB max	V_{DD} = 2.35 V to 3.6V
	±0.02	LSB typ	V_{DD} = 4.75 V to 5.25V
Gain Error[2]	±2	LSB max	V_{DD} = 2.35 V to 3.6V
	±0.5	LSB typ	V_{DD} = 4.75 V to 5.25V
Gain Error Match[2, 3]	±1	LSB max	V_{DD} = 2.35 V to 3.6V
	±0.2	LSB typ	V_{DD} = 4.75 V to 5.25V
Total Unadjusted Error (TUE)[2]	±1.5	LSB max	V_{DD} = 2.35 V to 3.6V
	±0.5	LSB typ	V_{DD} = 4.75 V to 5.25V
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	V	
DC Leakage Current	±0.3	µA max	
Input Capacitance	20	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 (V_{DD})	V min	2.35 V ≤ V_{DD} ≤ 2.7 V
	2	V min	2.7 V < V_{DD} ≤ 5.25 V
Input Low Voltage, V_{INL}	0.3	V max	V_{DD} = 2.35 V
	0.2 (V_{DD})	V max	2.35 V < V_{DD} ≤ 2.7 V
	0.8	V max	2.7 V < V_{DD} ≤ 5.25 V
Input Current, I_{IN}, SCLK Pin	±0.3	µA max	Typically 8 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±0.3	µA max	
Input Current, I_{IN}, DIN Pin	±0.3	µA max	
Input Capacitance, C_{IN}[3]	5	pF max	

Parameter	A Grade[1]	Unit	Test Conditions/Comments
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 2.35 V to 5.25 V
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±0.3	µA max	
Floating-State Output Capacitance[3]	5	pF max	
Output Coding	Straight (natural) binary		
CONVERSION RATE			
Conversion Time	888	ns max	16 SCLK cycles with SCLK at 18 MHz
Track-and-Hold Acquisition Time[2]	290	ns max	
Throughput Rate	1	MSPS max	See the Serial Interface section
POWER REQUIREMENTS			
V_{DD}	2.35/5.25	V min/max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	3	mA typ	V_{DD} = 4.75 V to 5.25 V, SCLK on or off
	1.5	mA typ	V_{DD} = 2.35 V to 3.6 V, SCLK on or off
Normal Mode (Operational)	4	mA max	V_{DD} = 4.75 V to 5.25 V, f_{SAMPLE} = 1 MSPS
	2	mA max	V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = 1 MSPS
Full Power-Down Mode (Static)	1	µA max	SCLK on or off, typically 50 nA
Full Power-Down Mode (Dynamic)	0.5	mA typ	V_{DD} = 5 V, f_{SCLK} = 18 MHz, f_{SAMPLE} = 100 kSPS
	0.28	mA typ	V_{DD} = 3 V, f_{SCLK} = 18 MHz, f_{SAMPLE} = 100 kSPS
Power Dissipation[4]			
Normal Mode (Operational)	20	mW max	V_{DD} = 5 V, f_{SAMPLE} = 1 MSPS
	6	mW max	V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS
Full Power-Down	5	µW max	V_{DD} = 5 V
	3	µW max	V_{DD} = 3 V

[1] Operational from V_{DD} = 2 V, with V_{IH} = 1.9 V minimum and V_{IL} = 0.1 V maximum.
[2] See the Terminology section.
[3] Guaranteed by characterization.
[4] See the Power vs. Throughput Rate section.

TIMING SPECIFICATIONS

Guaranteed by characterization.
All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
V_{DD} = 2.35 V to 5.25 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK}[1]	10	kHz min[2]	
	18	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}		AD7922
	14 × t_{SCLK}		AD7912
t_{QUIET}	30	ns min	Minimum quiet time required between bus relinquish and start of next conversion
t_1	15	ns min	Minimum $\overline{CS}$ pulse width
t_2	10	ns min	$\overline{CS}$ to SCLK setup time
t_3[3]	30	ns max	Delay from $\overline{CS}$ until DOUT three-state is disabled
t_4[3]	45	ns max	DOUT access time after SCLK falling edge
t_5	0.4 t_{SCLK}	ns min	SCLK low pulse width
t_6	0.4 t_{SCLK}	ns min	SCLK high pulse width
t_7[4]	10	ns min	SCLK to DOUT valid hold time
t_8	5	ns min	DIN setup time prior to SCLK falling edge
t_9	6	ns min	DIN hold time after SCLK falling edge
t_{10}[5]	30	ns max	SCLK falling edge to DOUT three-state
	10	ns min	SCLK falling edge to DOUT three-state
$t_{POWER-UP}$[6]	1	µs max	Power-up time from full power-down

[1] Mark/space ratio for SCLK input is 40/60 to 60/40.
[2] Minimum f_{SCLK} at which specifications are guaranteed.
[3] Measured with the load circuit in Figure 2 and defined as the time required for the output to cross V_{IH} or V_{IL} voltage.
[4] Measured with a 50 pF load capacitor.
[5] T_{10} is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_{10}, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.
[6] See the Power-Up Time section.

TIMING DIAGRAMS

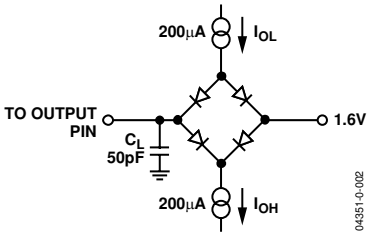

Figure 2. Load Circuit for Digital Output Timing Specifications

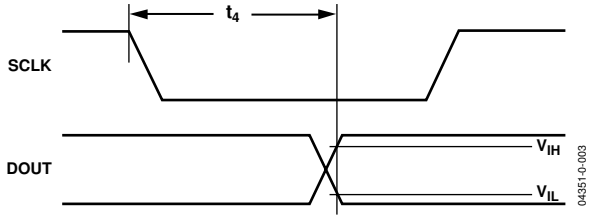

Figure 3. Access Time after SCLK Falling Edge

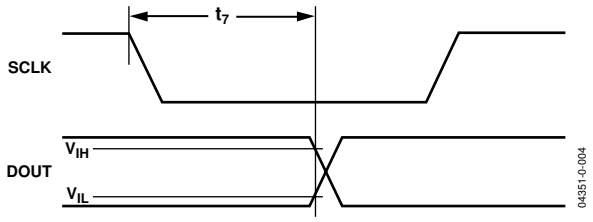

Figure 4. Hold Time after SCLK Falling Edge

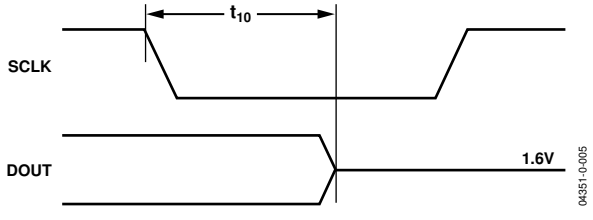

Figure 5. SCLK Falling Edge to DOUT Three-State

TIMING EXAMPLES

Figure 6 and Figure 7 show some of the timing parameters from the Timing Specifications section.

Timing Example 1

As shown in Figure 7, when f_{SCLK} = 18 MHz and the throughput is 1 MSPS, the cycle time is

$$t_2 + 12.5(1/f_{SCLK}) + t_{ACQ} = 1\ \mu s$$

With t_2 = 10 ns minimum, then t_{ACQ} is 295 ns, which satisfies the requirement of 290 ns for t_{ACQ}.

In Figure 7, t_{ACQ} is comprised of $2.5(1/f_{SCLK}) + t_{10} + t_{QUIET}$, where t_{10} = 30 ns maximum. This allows a value of 126 ns for t_{QUIET}, satisfying the minimum requirement of 30 ns.

Timing Example 2

The AD7922 can also operate with slower clock frequencies. As shown in Figure 7, when f_{SCLK} = 5 MHz and the throughput rate is 315 kSPS, the cycle time is

$$t_2 + 12.5(1/f_{SCLK}) + t_{ACQ} = 3.17\ \mu s$$

With t_2 = 10 ns minimum, then t_{ACQ} is 664 ns, which satisfies the requirement of 290 ns for t_{ACQ}.

In Figure 7, t_{ACQ} is comprised of $2.5(1/f_{SCLK}) + t_{10} + t_{QUIET}$, where t_{10} = 30 ns maximum. This allows a value of 134 ns for t_{QUIET}, satisfying the minimum requirement of 30 ns.

In this example, as with other slower clock values, the signal might already be acquired before the conversion is complete, but it is still necessary to leave 30 ns minimum t_{QUIET} between conversions. In this example, the signal should be fully acquired at approximately point C in Figure 7.

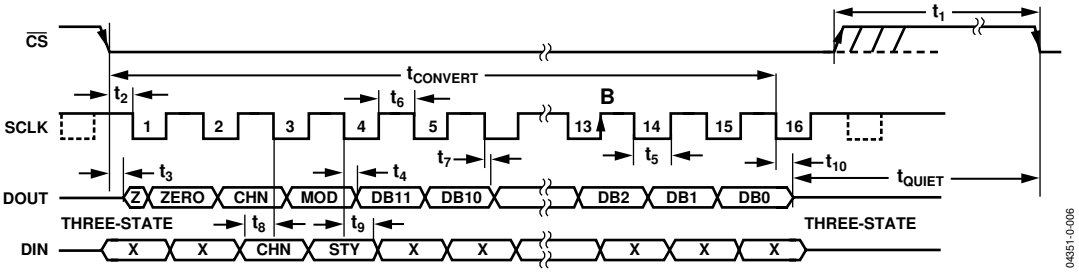

Figure 6. AD7922 Serial Interface Timing Diagram

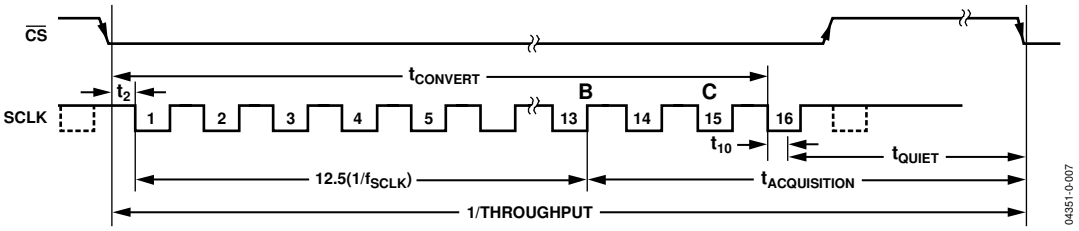

Figure 7. Serial Interface Timing Example

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial (A Grade)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSOT Package	
θ_{JA} Thermal Impedance	207°C/W
MSOP Package	
θ_{JA} Thermal Impedance	205.9°C/W
θ_{JC} Thermal Impedance	43.74°C/W
Lead Temperature Soldering	
Reflow (10 s to 30 s)	235 (0/+5)°C
ESD	1.5 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

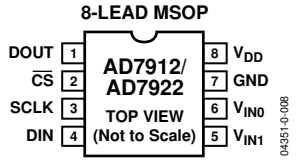

Figure 8. 8-Lead MSOP Pin Configuration

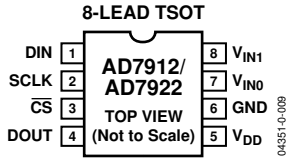

Figure 9. 8-Lead TSOT Pin Configuration

Table 5. Pin Function Descriptions

MSOP Pin No.	TSOT Pin No.	Mnemonic	Function
1	4	DOUT	Data Out. Logic output. The conversion result from the AD7912/AD7922 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK signal. For the AD7922, the data stream consists of two leading zeros, the channel identifier bit that identifies which channel the conversion result corresponds to, followed by the mode bit that indicates the current mode of operation, followed by the 12 bits of conversion data with MSB first. For the AD7912, the data stream consists of two leading zeros, the channel identifier bit that identifies which channel the conversion result corresponds to, followed by the mode bit that indicates the current mode of operation, followed by the 10 bits of conversion data with MSB first and two trailing zeros.
2	3	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7912/AD7922 and framing the serial data transfer.
3	2	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7912/AD7922's conversion process.
4	1	DIN	Data In. Logic input. The channel to be converted is provided on this input and is clocked into an internal register on the falling edge of SCLK.
6, 5	7, 8	V_{IN0}, V_{IN1}	Analog Inputs. These two single-ended analog input channels are multiplexed into the on-chip track-and-hold amplifier. The analog input channel to be converted is selected by writing to the third MSB on the DIN pin. The input range is 0 to V_{DD}.
7	6	GND	Analog Ground. Ground reference point for all circuitry on the AD7912/AD7922. All analog input signals should be referred to this GND voltage.
8	5	V_{DD}	Power Supply Input. The V_{DD} range for the AD7912/AD7922 is from 2.35 V to 5.25 V.

TERMINOLOGY

Integral Nonlinearity

The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. For the AD7912/AD7922, the endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity

The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

The deviation of the first code transition (00…000) to (00… 001) from the ideal, that is, AGND + 1 LSB.

Offset Error Match

The difference in offset error between any two channels.

Gain Error

The deviation of the last code transition (111…110) to (111…111) from the ideal, that is, V_{DD} − 1 LSB after the offset error has been adjusted out.

Gain Error Match

The difference in gain error between any two channels.

Total Unadjusted Error

A comprehensive specification that includes gain error, linearity error, and offset error.

Channel-to-Channel Isolation

A measure of the level of crosstalk between channels. It is measured by applying a full-scale sine wave signal of 20 kHz to 500 kHz to the nonselected input channel and determining how much that signal is attenuated in the selected channel with a 10 kHz signal. The figure is given worst case across both channels for the AD7912/AD7922.

Track-and-Hold Acquisition Time

The time required for the output of the track-and-hold amplifier to reach its final value within ±1 LSB after the end of conversion. The track-and-hold amplifier returns to track mode at the end of conversion. See the Serial Interface section for more details.

Signal-to-Noise + Distortion Ratio (SINAD)

The measured ratio of signal-to-noise and distortion at the output of the A/D converter. The signal is the rms value of the sine wave, and noise is the rms sum of all nonfundamental signals up to half the sampling frequency (fs/2), including harmonics but excluding dc.

Signal-to-Noise Ratio (SNR)

The measured ratio of signal to noise at the output to the A/D converter. The signal is the rms value of the sine wave input. Noise is the rms quantization error within the Nyquist bandwidth (fs/2). The rms value of a sine wave is one-half its peak-to-peak value divided by √2, and the rms value for the quantization noise is q/√12. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. For an ideal *N*-bit converter, the SNR is defined as

$$SNR = 6.02\,N + 1.76\ \text{dB}$$

Therefore, for a 12-bit converter, SNR is 74 dB; for a 10-bit converter, SNR is 62 dB.

However, various error sources in the ADC cause the measured SNR to be less than the theoretical value. These errors occur due to integral and differential nonlinearities, internal ac noise sources, and so on.

Total Harmonic Distortion (THD)

The ratio of the rms sum of harmonics to the fundamental, which is defined as

$$THD\ (\text{dB}) = 20 \log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where:

V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

The ratio of the rms value of the next largest component in the ADC output spectrum (up to fs /2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where *m*, *n* = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither *m* nor *n* is equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7912/AD7922 are tested using the CCIF standard, where two input frequencies are used (see fa and fb in the Specifications section). In this case, the second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second-order and third-order terms are specified separately. The calculation of the intermodulation distortion is as in the THD specification, where it is defined as the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dB.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 10 and Figure 11 show typical FFT plots for the AD7922 and AD7912, respectively, at a 1 MSPS sample rate and 100 kHz input frequency.

Figure 12 shows the SINAD performance versus the input frequency for various supply voltages while sampling at 1 MSPS with a SCLK frequency of 18 MHz for the AD7922.

Figure 13 shows the SNR performance versus the input frequency for various supply voltages while sampling at 1 MSPS with an SCLK frequency of 18 MHz for the AD7922.

Figure 14 and Figure 15 show INL and DNL performance for the AD7922.

Figure 16 shows a graph of the THD versus the analog input frequency for different source impedances when using a supply voltage of 3.6 V and a sampling rate of 1 MSPS. See the Analog Input section.

Figure 17 shows a graph of the THD versus the analog input frequency for various supply voltages while sampling at 1 MSPS with an SCLK frequency of 18 MHz.

Figure 18 shows the shutdown current versus the voltage supply for different operating temperatures.

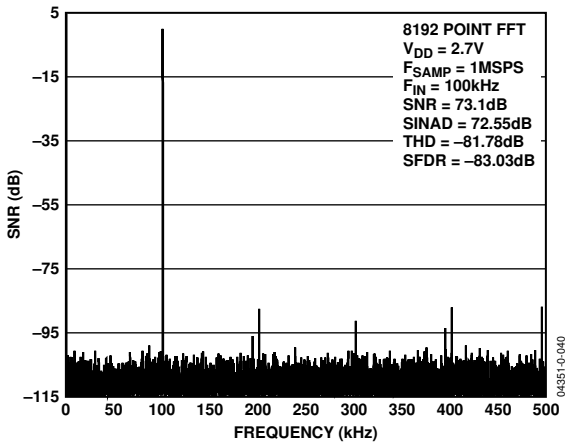

Figure 10. AD7922 Dynamic Performance at 1 MSPS

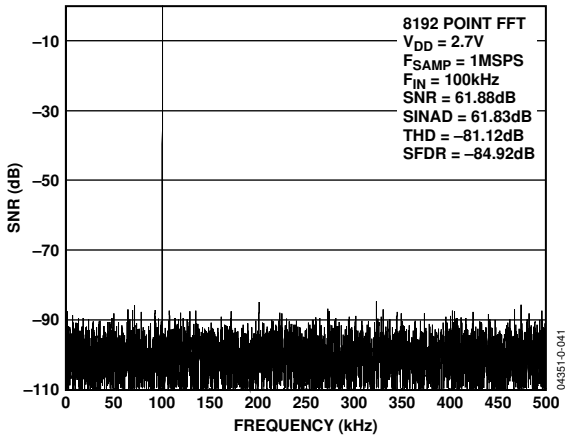

Figure 11. AD7912 Dynamic Performance at 1 MSPS

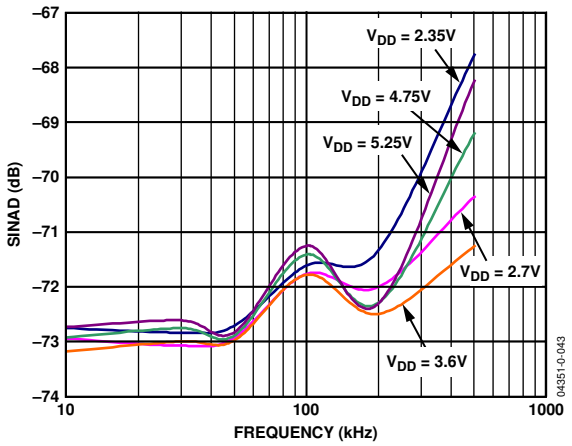

Figure 12. AD7922 SINAD vs. Input Frequency at 1 MSPS

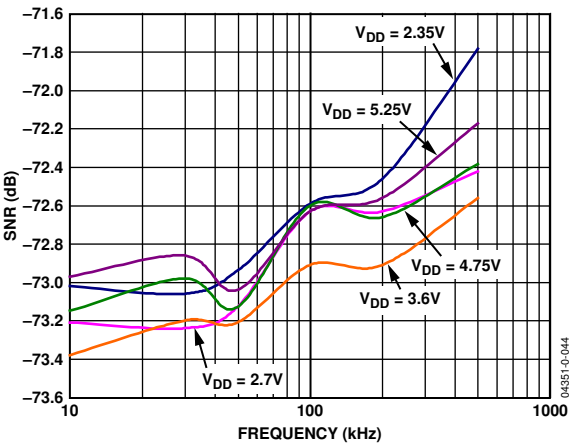

Figure 13. AD7922 SNR vs. Input Frequency at 1 MSPS

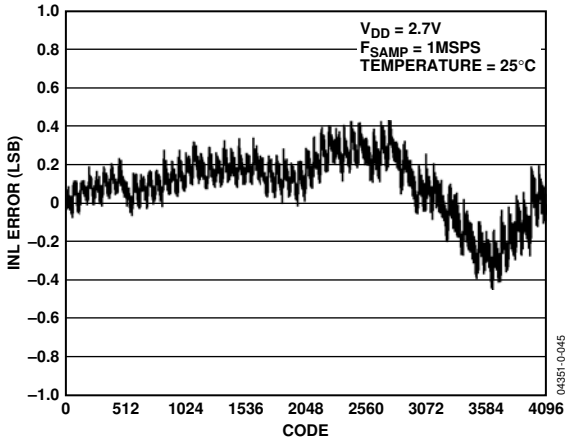

Figure 14. AD7922 INL Performance

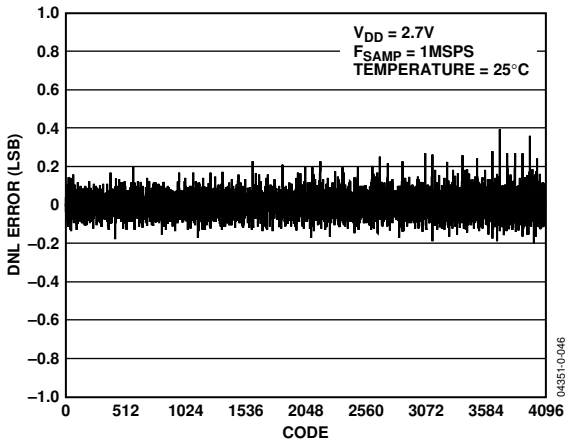

Figure 15. AD7922 DNL Performance

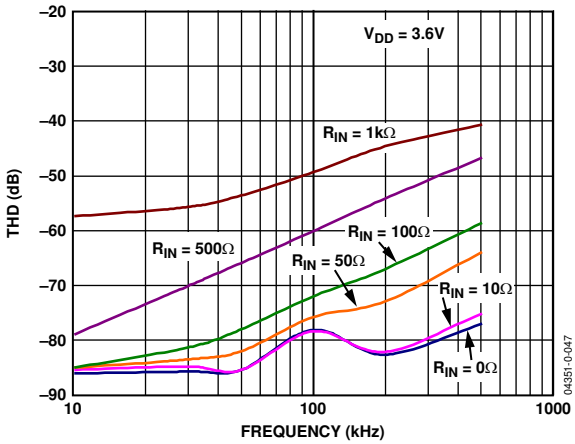

Figure 16. THD vs. Analog Input Frequency for Various Source Impedances

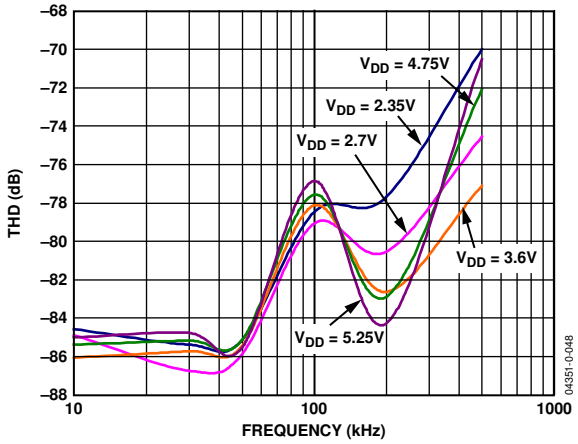

Figure 17. THD vs. Analog Input Frequency for Various Supply Voltages

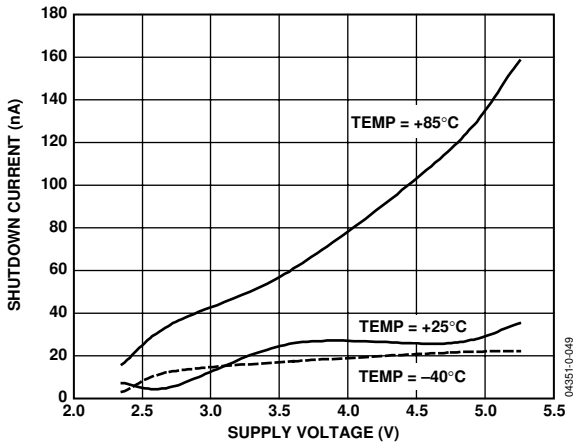

Figure 18. Shutdown Current vs. Supply Voltage

CIRCUIT INFORMATION

The AD7912/AD7922 are fast, 2-channel, 10-/12-bit, single supply, analog-to-digital converters (ADCs), respectively. The parts can be operated from a 2.35 V to 5.25 V supply. When operated from either a 5 V supply or a 3 V supply, the AD7912/AD7922 are capable of throughput rates of 1 MSPS when provided with an 18 MHz clock.

The AD7912/AD7922 provide the user with an on-chip track-and-hold, an ADC, and a serial interface, all housed in a tiny 8-lead TSOT package or 8-lead MSOP package, which offer the user considerable space-saving advantages over alternative solutions. The serial clock input accesses data from the parts, controls the transfer of data written to the ADC, and provides the clock source for the successive approximation ADC. The analog input range is 0 to V_{DD}. An external reference is not required for the ADC, and neither is there a reference on-chip. The reference for the AD7912/AD7922 is derived from the power supply and, therefore, gives the widest dynamic input range.

The AD7912/AD7922 feature a power-down option that allows power saving between conversions. The power-down feature is implemented across the standard serial interface as described in the Modes of Operation section. The AD7912/AD7922 can also be used in daisy-chain mode when several AD7912/AD7922 are connected in a daisy chain. This mode of operation is selected by controlling the logic state of the $\overline{CS}$ signal. The fourth MSB on the DOUT pin indicates if the ADC is in normal mode or daisy-chain mode.

CONVERTER OPERATION

The AD7912/AD7922 are 10-/12-bit successive approximation ADCs based around a charge redistribution DAC. Figure 19 and Figure 20 show simplified schematics of the ADC. Figure 19 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on the selected V_{IN} channel.

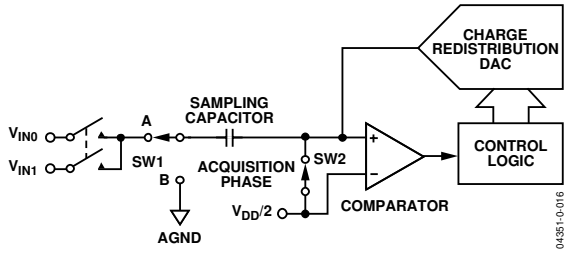

Figure 19. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 20), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 21 shows the ADC transfer function.

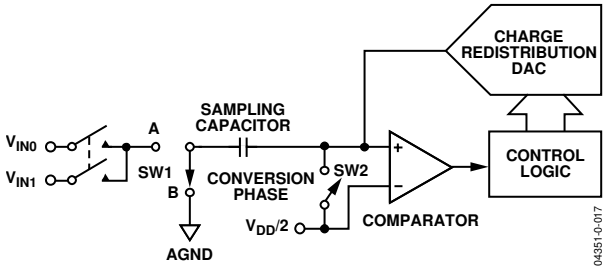

Figure 20. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7912/AD7922 is straight binary. The designed code transitions occur at the successive integer LSB values, that is, 1 LSB, 2 LSBs, and so on. The LSB size is $V_{DD}/4096$ for the AD7922 and $V_{DD}/1024$ for the AD7912. The ideal transfer characteristic for the AD7912/AD7922 is shown in Figure 21.

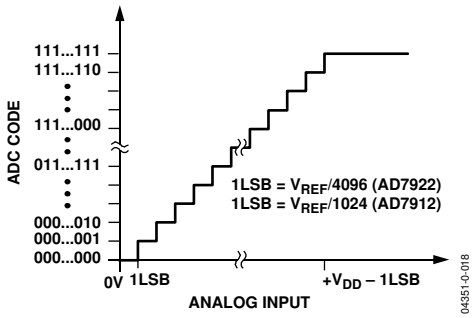

Figure 21. AD7912/AD7922 Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 22 shows a typical connection diagram for the AD7912/AD7922. V_{REF} is taken internally from V_{DD} and as such V_{DD} should be well decoupled. This provides an analog input range of 0 V to V_{DD}. The conversion result is output in a 16-bit word with two leading zeros, followed by the channel identifier bit that identifies the channel converted, followed by the mode bit that indicates the current mode of operation, and by the MSB of the 12-bit or 10-bit result. For the AD7912, the 10-bit result is followed by two trailing zeros. See the Serial Interface section.

Alternatively, because the supply current required by the AD7912/AD7922 is so low, a precision reference can be used as the supply source to the AD7912/AD7922. A REF19x voltage reference (REF195 for 5 V or REF193 for 3 V) can be used to supply the required voltage to the ADC (see Figure 22). This configuration is especially useful, if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V or 3 V (for example, 15 V). The REF19x outputs a steady voltage to the AD7912/AD7922. If the low dropout REF193 is used, the current it needs to supply to the AD7912/AD7922 is typically1.5 mA. When the ADC is converting at a rate of 1 MSPS, the REF193 needs to supply a maximum of 2 mA to the AD7912/AD7922. The load regulation of the REF193 is typically 10 ppm/mA (REF193, VS = 5 V), which results in an error of 20 ppm (60 μV) for the 2 mA drawn from it. This corresponds to a 0.082 LSB error for the AD7922 with V_{DD} = 3 V from the REF193 and a 0.061 LSB error for the AD7912.

For applications where power consumption is a concern, the power-down mode of the ADC and the sleep mode of the REF19x reference should be used to improve power performance. See the Modes of Operation section.

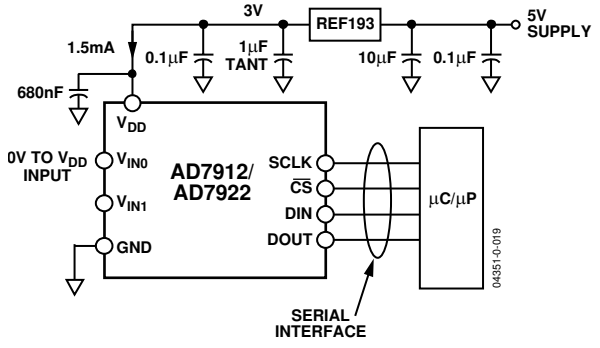

Figure 22. REF193 as Power Supply to AD7912/AD7922

Table 6 provides some typical performance data with various references used as a V_{DD} source and a 50 kHz input tone under the same setup conditions.

Table 6. AD7922 Performance for Various Voltage References IC

Reference Tied to V_{DD}	AD7922 SNR Performance (dB)
AD780 at 3 V	−73
REF193	−72.42
ADR433	−72.9
AD780 at 2.5 V	−72.86
REF192	−72.27
ADR421	−72.75

ANALOG INPUT

Figure 23 shows an equivalent circuit of the analog input structure of the AD7912/AD7922. The two diodes, D1 and D2, provide ESD protection for the analog input. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 300 mV, because this would cause these diodes to become forward biased and start conducting current into the substrate. The maximum current these diodes can conduct without causing irreversible damage to the part is 10 mA.

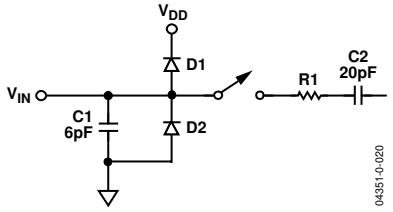

Figure 23. Equivalent Analog Input Circuit

The capacitor C1 in Figure 23 is typically about 6 pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of the track-and-hold switch and also includes the on resistance of the input multiplexer. This resistor is typically about 100 Ω. The capacitor C2 is the ADC sampling capacitor and has a capacitance of 20 pF typically.

For ac applications, removing high frequency components from the analog input signal is recommended using a band-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances can significantly affect the ac performance of the ADC. This might necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

Table 7 provides some typical performance data with various op amps used as the input buffer, and a 50 kHz input tone under the same setup conditions.

Table 7. AD7922 Performance for Various Input Buffers

Op Amp in the Input Buffer	AD7922 SNR Performance (dB) 50 kHz Input , V_{DD} = 3.6 V
Single op amps	
AD8038	−72.79
AD8510	−72.35
AD8021	−72.2
Dual op amps	
AD712	−72.68
AD8022	−72.88

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases and performance degrades (see Figure 16).

DIGITAL INPUTS

The digital inputs applied to the AD7912/AD7922 are not limited by the maximum ratings that limit the analog input. Instead, the digital inputs applied can go to 7 V and are not restricted by the V_{DD} + 0.3 V limit as on the analog input. For example, if the AD7912/AD7922 are operated with a V_{DD} of 3 V, then 5 V logic levels could be used on the digital inputs. However, it is important to note that the data output on DOUT still has 3 V logic levels when V_{DD} = 3 V. Another advantage of SCLK, DIN, and $\overline{CS}$ not being restricted by the V_{DD} + 0.3 V limit is that power supply sequencing issues are avoided. If $\overline{CS}$, DIN, or SCLK are applied before V_{DD}, then there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V were applied prior to V_{DD}.

DIN INPUT

The channel to be converted on in the next conversion is selected by writing to the DIN pin. Data on the DIN pin is loaded into the AD7912/AD7922 on the falling edge of SCLK. The data is transferred into the part on the DIN pin at the same time that the conversion result is read from the part. Only the third and fourth bits of the DIN word are used; the rest are ignored by the ADC.

The third MSB is the channel identifier bit, which identifies the channel to be converted on in the next conversion, V_{IN0} (CHN = 0) or V_{IN1} (CHN = 1).

The fourth MSB, STY, is related to the mode of operation of the device. To keep the AD7912/ AD7922 in daisy-chain mode, the CHN and STY bits have to be inverted during the conversions (STY ≠ CHN). A conversion with STY = CHN on the input forces the device to normal mode in the next cycle. See the Daisy-Chain Mode section for more details.

If the AD7912/AD7922 are not going to be used in daisy-chain mode, it is recommended to keep STY and CHN the same (STY = CHN). In that case, the channel can be selected by tying DIN either high or low during a conversion cycle.

To summarize:

CHN = 0, Channel 0 selected for next conversion.

CHN = 1, Channel 1 selected for next conversion.

CHN = STY, forces normal mode in the next cycle.

CHN ≠ STY, keeps the AD7912/AD7922 in daisy-chain mode.

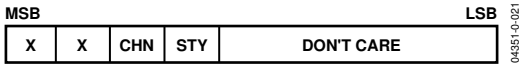

Figure 24. AD7912/AD7922 DIN Word

DOUT OUTPUT

The conversion result from the AD7912/AD7922 is provided on this output as a serial data stream. The bits are clocked out on the SCLK falling edge at the same time that the conversion is taking place.

The serial data stream for the AD7922 consists of two leading zeros followed by the bit that identifies the channel converted, the bit that indicates the current mode of operation, and the 12-bit conversion result with MSB provided first.

For the AD7912, the serial data stream consists of two leading zeros followed by the bit that identifies the channel converted, the bit that indicates the current mode of operation, and the 10-bit conversion result with MSB provided first, followed by two trailing zeros.

The CHN and MOD bits on DOUT indicate to the user the current mode of operation of the ADC. If CHN = MOD, the AD7912/AD7922 are in normal mode. Otherwise, if CHN ≠ MOD, the AD7912/AD7922 are in daisy-chain mode.

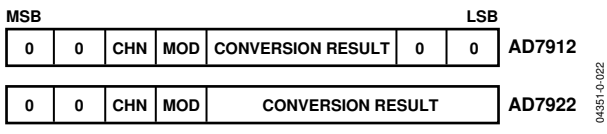

Figure 25. AD7912/AD7922 DOUT Word

MODES OF OPERATION

The three modes of operation of the AD7912/AD7922 are normal mode, power-down mode, and daisy-chain mode. The mode of operation is selected by controlling the logic state of the $\overline{CS}$ signal. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated determines whether the AD7912/AD7922 enter power-down mode or change to daisy-chain mode. Similarly, if already in daisy-chain mode, $\overline{CS}$ can control whether the device returns to normal operation or enters power-down mode. The user can also change from daisy-chain mode to normal mode by writing to the DIN pin, as outlined in the DIN Input section.

Power-down mode is designed to provide flexible power management options and to optimize the ratio of power dissipation to throughput rate for different application requirements.

Daisy-chain mode is intended for applications where fast throughput rate is not required and more than one AD7912/AD7922 have been connected in a daisy chain, as shown in Figure 33.

NORMAL MODE

Normal mode is intended for the fastest throughput rate performance. The user does not have to worry about any power-up time, because the AD7912/AD7922 remain fully powered all the time. Figure 26 shows the operation of the AD7912/AD7922 in this mode.

The conversion is initiated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. To ensure that the part remains fully powered up at all times, $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high after the 10th SCLK falling edge and before the 12th SCLK falling edge, then the device enters daisy-chain mode, as shown in Figure 27. The conversion is terminated and DOUT goes back into three-state. If $\overline{CS}$ is brought high after the 13th SCLK falling edge, but before the end of $t_{CONVERT}$, the conversion is terminated and DOUT goes back into three-state, but the part remains in normal mode.

For the AD7922, 16 serial clock cycles are required to complete the conversion and access the complete conversion result. For the AD7912, a minimum of 14 serial clock cycles are required to complete the conversion and access the complete conversion result.

$\overline{CS}$ can idle high until the next conversion or can idle low until $\overline{CS}$ returns high sometime prior to the next conversion (effectively idling $\overline{CS}$ low). Once a data transfer is complete (DOUT has returned to three-state), another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again.

POWER-DOWN MODE

Power-down mode is intended for use in applications where slower throughput rates are required. Either the ADC is powered down between each conversion, or a series of conversions can be performed at a high throughput rate and then the ADC is powered down for a relatively long duration between these bursts of several conversions. When the AD7912/AD7922 are in power-down mode, all analog circuitry is powered down.

To enter power-down mode, the conversion process must be interrupted by bringing $\overline{CS}$ high any time after the second falling edge of SCLK and before the 10th falling edge of SCLK, as shown in Figure 28. Once $\overline{CS}$ has been brought high in this window of SCLKs, then the part enters power-down mode, the conversion that was initiated by the falling edge of $\overline{CS}$ is terminated, and DOUT goes back into three-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, then the part remains in normal mode and does not power down. This helps to avoid accidental power-down due to glitches on the $\overline{CS}$ line.

To exit this mode of operation and power the AD7912/AD7922 up again, a dummy conversion is performed. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The device is fully powered up once 16 SCLKs have elapsed and valid data results from the next conversion, as shown in Figure 29. If $\overline{CS}$ is brought high before the 10th falling edge of SCLK, then the AD7912/AD7922 go back into power-down mode. This helps to avoid accidental power-up due to glitches on the $\overline{CS}$ line or an inadvertent burst of 8 SCLK cycles while $\overline{CS}$ is low. Therefore, although the device might begin to power up on the falling edge of $\overline{CS}$, it powers down again on the rising edge of $\overline{CS}$, as long as this occurs before the 10th SCLK falling edge.

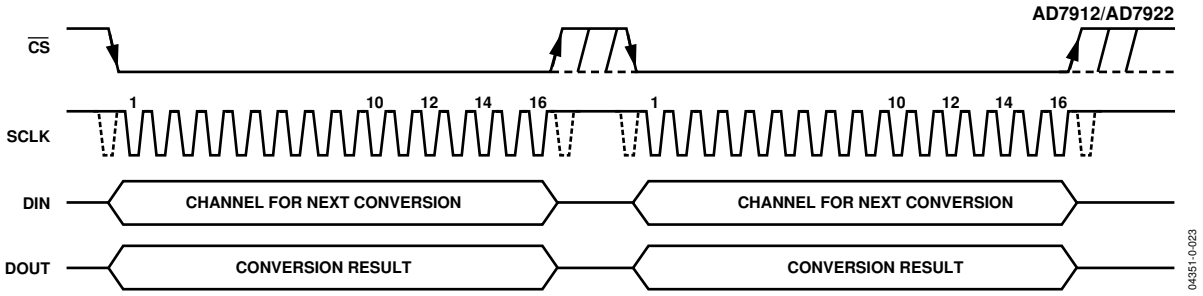

Figure 26. Normal Mode Operation

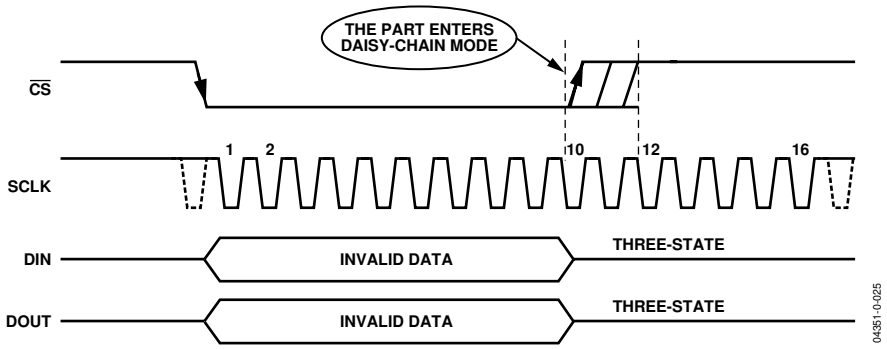

Figure 27. Entering Daisy-Chain Mode

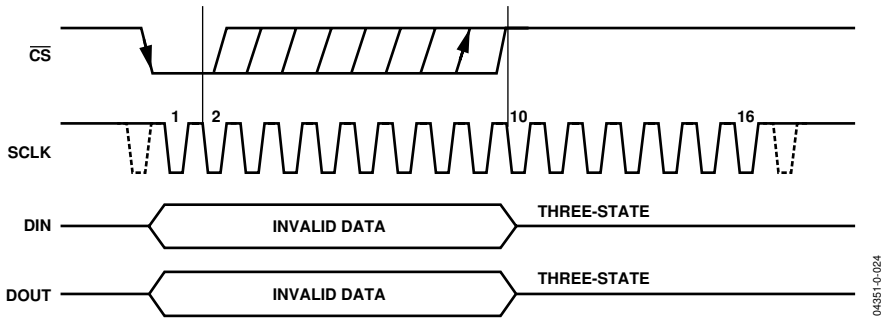

Figure 28. Entering Power- Down Mode

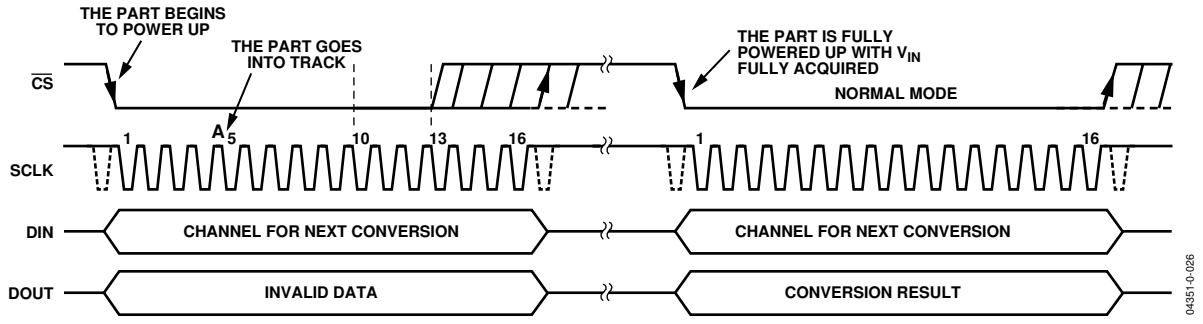

Figure 29. Exiting Power-Down Mode

POWER-UP TIME

The power-up time of the AD7912/AD7922 is 1 µs, which means that with any frequency of SCLK up to 18 MHz, one dummy cycle is always sufficient to allow the device to power up. Once the dummy cycle is complete, the ADC is fully powered up and the input signal is fully acquired. The quiet time, t_{QUIET}, must still be allowed from the point at which the bus goes back into three-state after the dummy conversion to the next falling edge of $\overline{CS}$. When running at a 1 MSPS throughput rate, the AD7912/AD7922 power up and acquire a signal within ±1 LSB in one dummy cycle, that is, 1 µs.

When powering up from power-down mode with a dummy cycle, as in Figure 29, the track-and-hold that was in hold mode while the part was powered down returns to track mode on the fifth SCLK falling edge that the part receives after the falling edge of $\overline{CS}$. This is shown as point A in Figure 29. At this point, the part starts to acquire the signal on the channel selected in the current dummy conversion.

Although at any SCLK frequency one dummy cycle is sufficient to power up the device and acquire V_{IN}, it does not necessarily mean that a full dummy cycle of 16 SCLKs must always elapse to power up the device and acquire V_{IN} fully. 1 µs is sufficient to power up the device and acquire the input signal. For example, if a 5 MHz SCLK frequency was applied to the ADC, the cycle time would be 3.2 µs. In one dummy cycle, 3.2 µs, the part would be powered up and V_{IN} acquired fully. However, after 1 µs with a 5 MHz SCLK, only five SCLK cycles would have elapsed. At this stage, the ADC would be fully powered up and the signal is acquired. Therefore, in this case, $\overline{CS}$ can be brought high after the 10th SCLK falling edge. If $\overline{CS}$ is brought high anytime after the 13th SCLK falling edge, the part enters normal mode for the next conversion. $\overline{CS}$ has to be brought low again after a time, t_{QUIET}, to initiate the conversion. However, if $\overline{CS}$ is brought high anytime after the 10th and before the 12th SCLK falling edge, the part enters daisy-chain mode.

When power supplies are first applied to the AD7912/AD7922, the ADC can power up in either power-down mode, normal mode, or daisy-chain mode. Because of this, it is best to allow a dummy cycle to elapse to ensure that the part is fully powered up before attempting a valid conversion. Likewise, if the user wants to keep the part in power-down mode while not in use and to power up in power-down mode, then the dummy cycle can be used to ensure that the device is in power-down mode by executing a cycle such as that shown in Figure 28.

Once supplies are applied to the AD7912/AD7922, the power-up time is the same as when powering up from the power-down mode. It takes the part approximately 1 µs to power up fully in normal mode. It is not necessary to wait 1 µs before executing a dummy cycle to ensure the desired mode of operation. Instead, the dummy cycle can occur directly after power is supplied to the ADC. If the first valid conversion is then performed directly after the dummy conversion, care must be taken to ensure that adequate acquisition time has been allowed. When the ADC powers up initially after supplies are applied, the track-and-hold is in hold. It returns to track on the fifth SCLK falling edge that the part receives after the falling edge of $\overline{CS}$.

DAISY-CHAIN MODE

When the ADC is in this mode of operation, the part operates as a shift register. This mode is intended for applications where more than one ADC is used, connected in a daisy-chain configuration (see Figure 33). All ADCs are addressed by the same $\overline{CS}$ signal and the same serial clock. The conversion result stored in the internal shift register in each ADC is shifted from one device to the following in the chain. See the Daisy-Chain Example in the following section for more details.

To enter daisy-chain mode, the conversion process must be interrupted by bringing $\overline{CS}$ high after the 10th falling edge of SCLK and before the 12th falling edge of SCLK, as shown in Figure 27. To ensure that the AD7912/AD7922 are placed into daisy-chain mode, $\overline{CS}$ should not be brought high until at least 20 ns after the 10th SCLK falling edge and before the 12th SCLK falling edge. Once $\overline{CS}$ has been brought high in this window of SCLKs, the part enters daisy-chain mode, the conversion that was initiated by the falling edge of $\overline{CS}$ is terminated, and DOUT goes back into three-state.

If $\overline{CS}$ is brought high between the 10th and the 12th SCLK falling edge, the part enters daisy-chain mode and the data shifted from one ADC to the next one in the chain is valid data (see Figure 34 and Figure 35). If $\overline{CS}$ is brought high between the 12th and the 13th SCLK falling edge, the part enters daisy-chain mode, but the data shifted in the chain is invalid data.

To keep the part in daisy-chain mode, the CHN and STY bits in the DIN word must be inverted relative to each other in each 16 SCLKs cycle. A conversion with the CHN and STY bits set to the same value in the DIN word while the device is in daisy-chain mode forces the part to go back into normal mode in the next cycle, as shown in Figure 30.

To exit this mode of operation, the user can perform a dummy cycle or can set the STY bit to the CHN bit value on the DIN word during a conversion cycle. When performing a dummy conversion to exit this mode, $\overline{CS}$ must be brought high anytime after the 10th SCLK falling edge and before the 13th SCLK falling edge, as shown in Figure 31. The device enters normal mode, and valid data from the channel selected in the dummy cycle results in the next conversion.

Figure 32 summarizes the modes of operation, how to change between modes, the values for the bits in the DIN and DOUT words in different modes, and in the transitions between modes.

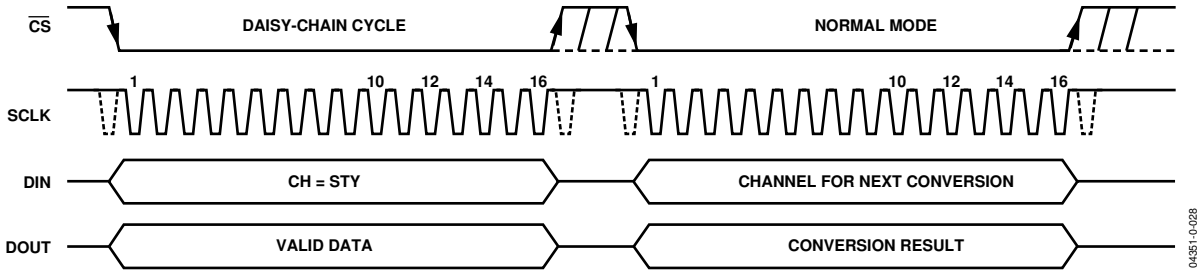

Figure 30. Exiting Daisy-Chain Mode with CH = STY in the DIN Pin

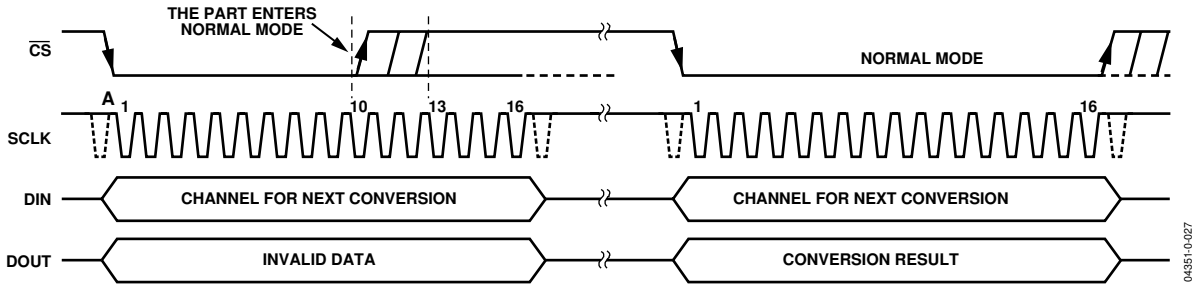

Figure 31. Exiting Daisy-Chain Mode

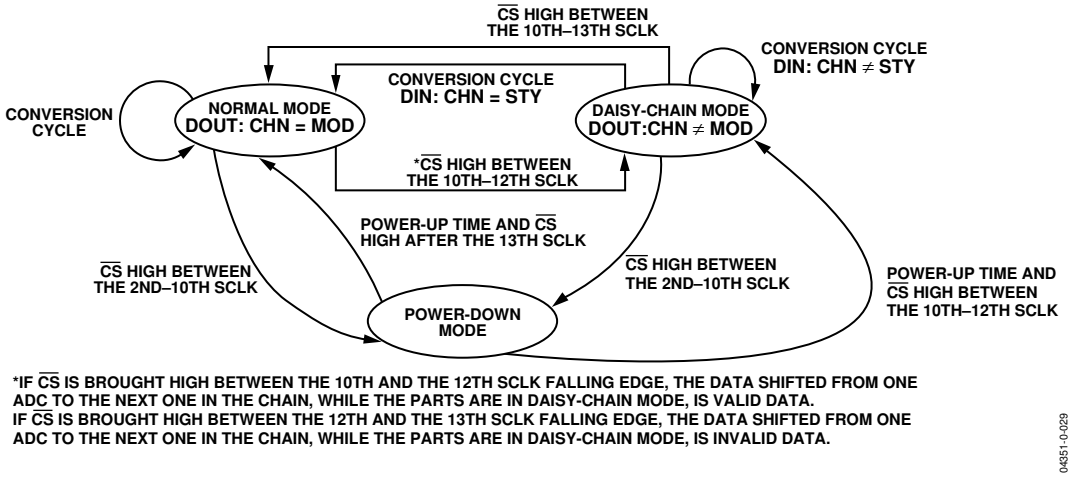

Figure 32. Transitions between Modes of Operation

DAISY-CHAIN EXAMPLE

In applications where fast throughput is not critical, connecting several ADCs in a daisy chain lets the user perform simultaneous sampling on all the ADCs contained in the chain using the minimum number of I/O lines from the µC/DSP ports.

The user needs to alternate modes of operation in the ADCs. While the parts are in normal mode, the conversion is performed and the result from each ADC is stored in its internal register. Following the conversion, the parts are placed into daisy-chain mode and the user can proceed to read the result from each ADC by shifting the data from one ADC to the next.

For clarity in the following example, only two devices are connected in a daisy chain. Both AD7912/AD7922 are addressed by the same $\overline{CS}$ and SCLK signal. The devices are configured as shown in Figure 33 for simultaneous conversion and shifting read operation later. The output of the device on the left, ADC1, feeds the input of the device on the right, ADC2.

During a normal conversion, the conversion result is stored internally and output to the DOUT pin. In daisy-chain mode, the value internally stored is output through the DOUT pin and the information provided at the DIN pin is shifted into the internal register.

When several AD7912/AD7922 are connected in a daisy chain, the sequence is as follows:

1. **Normal conversion.**
   Every AD7912/AD7922 performs a conversion on its selected channel and the result is stored in the internal shift register.

2. **Entering daisy-chain mode.**
   In this cycle, $\overline{CS}$ is brought high between the 10th and 12th SCLK falling edges and all the devices enter daisy-chain mode.

3. **Daisy-chain cycles.**
   While the AD7912/AD7922 are in daisy-chain mode, the conversion results from all the devices in the chain are read, and the parts are configured for the next conversion.

   The user needs to perform as many read cycles as there are devices in the chain. To keep all the AD7912/AD7922 in daisy-chain mode, the CHN and STY bits in the DIN input must always be inverted. Data is shifted through the devices in the chain. Data is clocked into the device in the chain by the same clock used to clock data out. The first word clocked into the DIN pin once the devices are in daisy-chain mode is eventually lost. The second word clocked into the DIN pin contains the channel configuration data for the last device in the chain, the third word clocked into the DIN pin contains the channel configuration data for the second last device in the chain, and so on. Then the selected channel for the first device in the chain is clocked in the cycle executed after all the data has been read, that is, in the short cycle used to change modes of operation. See Figure 34.

4. **Enter normal mode.**
   After reading the conversion results from the AD7912/AD7922, the devices need to be placed into normal mode to perform a new conversion. Therefore, in this cycle $\overline{CS}$ is brought high between the 10th and the 13th SCLK falling edge. The DOUT line contains invalid data and DIN contains the selected channel for the first device in the chain. The remaining devices in the chain have already set the channel for the next conversion as a result of the data shifted in during daisy-chain mode.

5. **Normal conversion.**
   A new conversion can be performed on the newly selected channels. The process can be repeated by following the previous steps.

   Figure 34 shows the timing diagram for two AD7912/AD7922 connected in a daisy chain, as shown in Figure 33. The DIN signal corresponds to the DIN pin on the first AD7912/AD7922 in the chain, and the DOUT signal corresponds to the DOUT pin on the last AD7912/AD7922 in the chain. The words clocked into the DIN pin, which set up the channel for the next conversion for the two AD7912/AD7922, are shown as COMMAND1 and COMMAND2. The first word clocked in, COMMAND3, does not remain in any of the ADCs in the chain and is eventually lost. The channel configuration data for the first device in the chain, COMMAND1, is clocked in while changing from daisy-chain mode to normal mode.

   Figure 35 is a more detailed diagram that shows the data presented on the DIN pin and clocked out on the DOUT pin for each of the AD7912/AD7922 in Figure 33. If the DOUT1 (or DIN2) signal is ignored, Figure 35 brings about Figure 34.

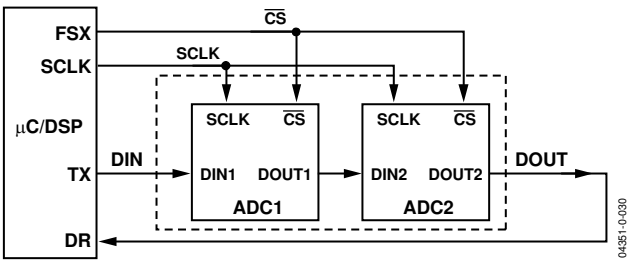

Figure 33. AD7912/AD7922 Connected in Daisy Chain

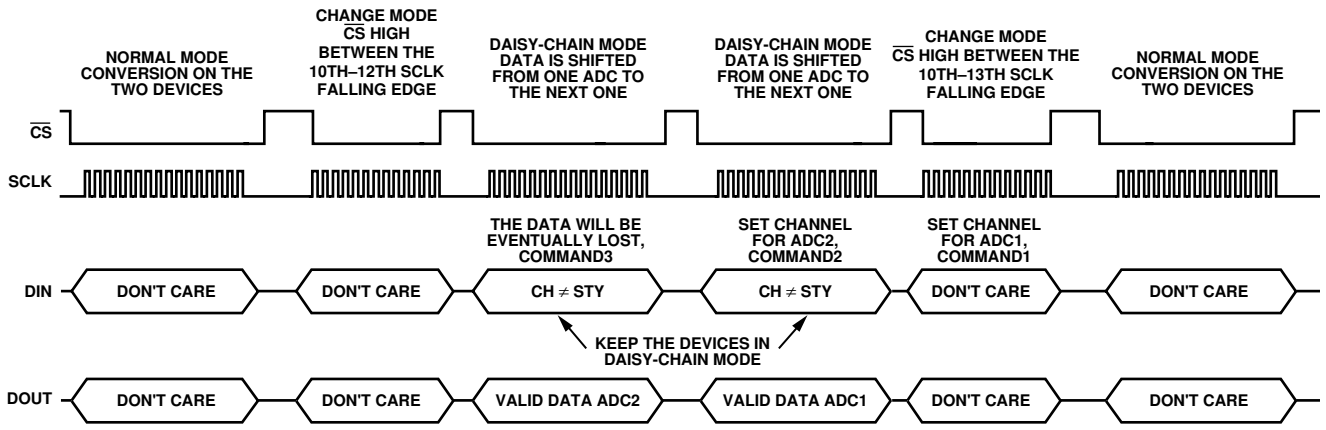

Figure 34. Daisy-Chain Diagrams—1

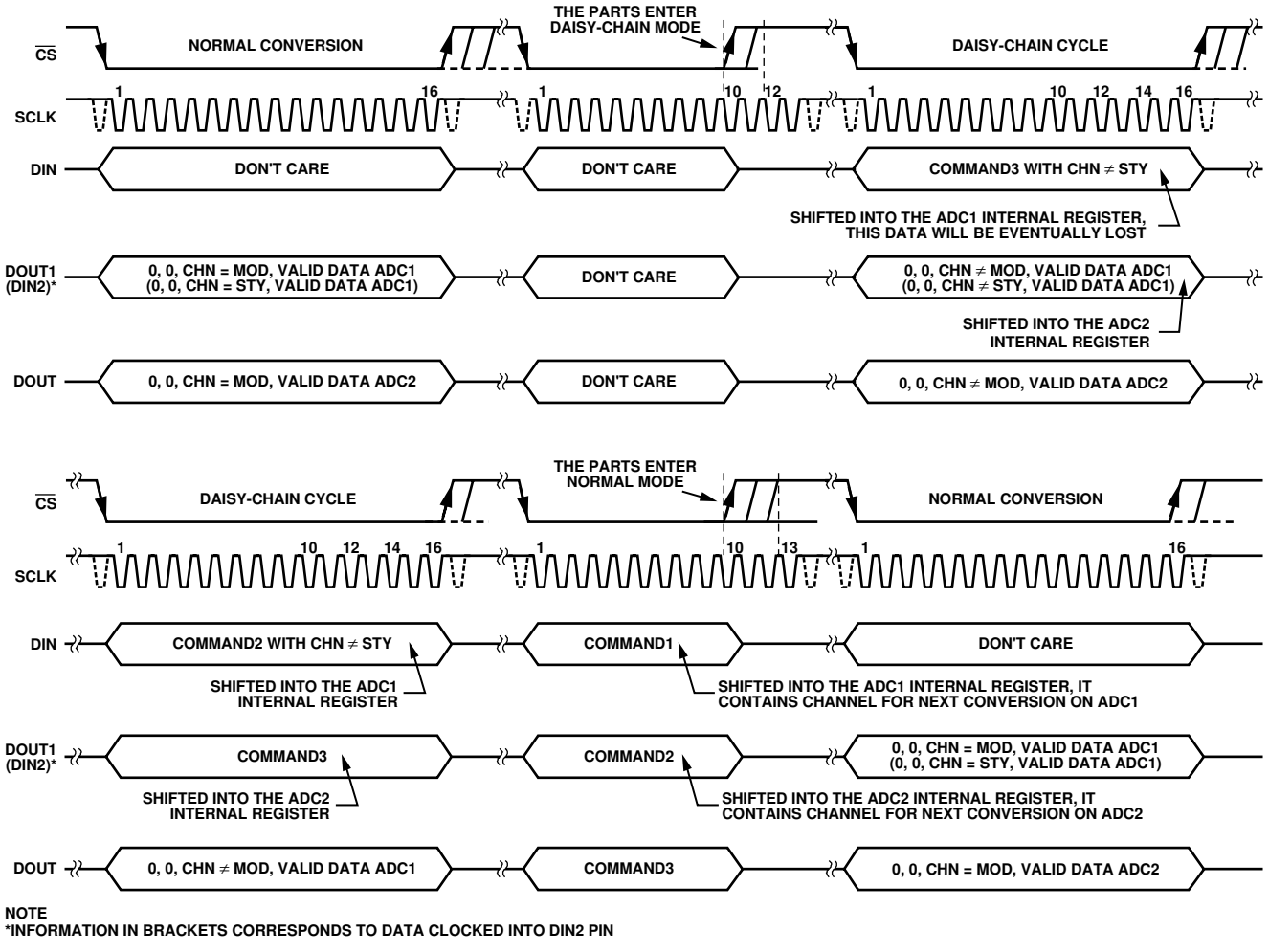

Figure 35. Daisy-Chain Diagrams—II

POWER VS. THROUGHPUT RATE

By using the power-down mode on the AD7912/AD7922 when not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 36 shows how, as the throughput rate is reduced, the device remains in its power-down state longer and the average power consumption over time drops.

For example, if the AD7912/AD7922 are operating in a continuous sampling mode with a throughput rate of 100 kSPS and a SCLK of 18 MHz (V_{DD} = 5 V), and the devices are placed in the power-down mode between conversions, then the power consumption is calculated as follows. The power dissipation during normal operation is 20 mW (V_{DD} = 5 V). If the power-up time is one dummy cycle (1 µs), and the remaining conversion time is another cycle (1 µs), then the AD7912/AD7922 dissipate 20 mW for 2 µs during each conversion cycle. If the throughput rate is 100 kSPS and the cycle time is 10 µs, then the average power dissipated during each cycle is

$$(2/10) \times (20 \text{ mW}) = 4 \text{ mW}$$

If V_{DD} = 3 V, SCLK = 18 MHz, and the device is again in power-down mode between conversions, then the power dissipation during normal operation is 6 mW. The AD7912/AD7922 now dissipate 6 mW for 2 µs during each conversion cycle. With a throughput rate of 100 kSPS, the average power dissipated during each cycle is

$$(2/10) \times (6 \text{ mW}) = 1.2 \text{ mW}$$

In the previous calculations, the power dissipation when the part is in power-down mode has not been taken into account. By placing the parts into power-down mode between conversions, the average power consumed by the ADC decreases as the throughput rate decreases, because the ADC remains in a power-down state for a longer time.

Figure 36 shows the power consumption versus throughput rate when using the power-down mode between conversions with both 5 V and 3 V supplies.

Power-down mode is intended for use with throughput rates of approximately 330 kSPS and under, because at higher sampling rates the short time spent in power-down does not affect the average power consumed by the ADC.

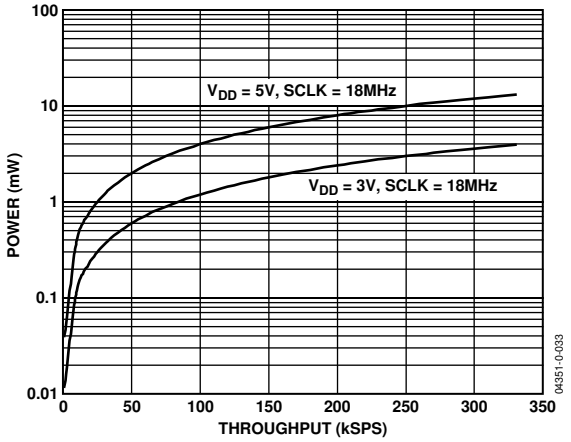

Figure 36. Power Consumption vs. Throughput Rate

SERIAL INTERFACE

Figure 37 and Figure 38 show the detailed timing diagrams for serial interfacing to the AD7922 and AD7912, respectively. The serial clock provides the conversion clock and also controls the transfer of information from the AD7912/AD7922 during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, takes the bus out of three-state. The analog input is sampled at this point and the conversion is initiated.

For the AD7922, the conversion requires 16 SCLK cycles to complete. Once 13 SCLK falling edges have elapsed, the track-and-hold goes back into track on the next SCLK rising edge, as shown in Figure 37 at Point B. On the 16th SCLK falling edge, the DOUT line goes back into three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, then the conversion is terminated and the DOUT line goes back into three-state. Otherwise, DOUT returns to three-state on the 16th SCLK falling edge, as shown in Figure 37. Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7922.

For the AD7912, the conversion requires 14 SCLK cycles to complete. Once 13 SCLK falling edges have elapsed, the track-and-hold goes back into track on the next SCLK rising edge, as shown in Figure 38 at Point B.

If the rising edge of $\overline{CS}$ occurs before 14 SCLKs have elapsed, then the conversion is terminated and the DOUT line goes back into three-state. If 16 SCLKs are considered in the cycle, DOUT returns to three-state on the 16th SCLK falling edge, as shown in Figure 38.

$\overline{CS}$ going low clocks out the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges beginning with the second leading zero. Therefore, the first falling clock edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. The final bit in the data transfer is valid on the 16th falling edge, having been clocked out on the previous (15th) falling edge.

In applications with a slower SCLK, it is possible to read in data on each SCLK rising edge. In that case, the first falling edge of SCLK clocks out the second leading zero and it can be read in the first rising edge. However, the first leading zero that is clocked out when $\overline{CS}$ goes low is missed, unless it is read on the first falling SCLK edge. The 15th falling edge of SCLK clocks out the last bit and it can be read in the 15th rising SCLK edge.

If $\overline{CS}$ goes low just after the SCLK falling edge has elapsed, $\overline{CS}$ clocks out the first leading zero as before and it can be read in the SCLK rising edge. The next SCLK falling edge clocks out the second leading zero and it can be read in the following rising edge.

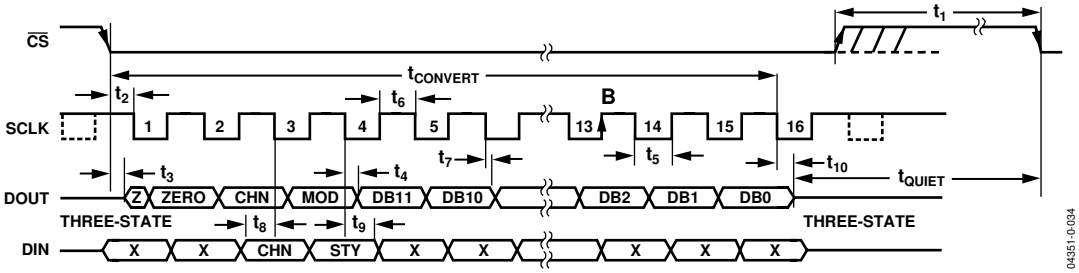

Figure 37. AD7922 Serial Interface Timing Diagram

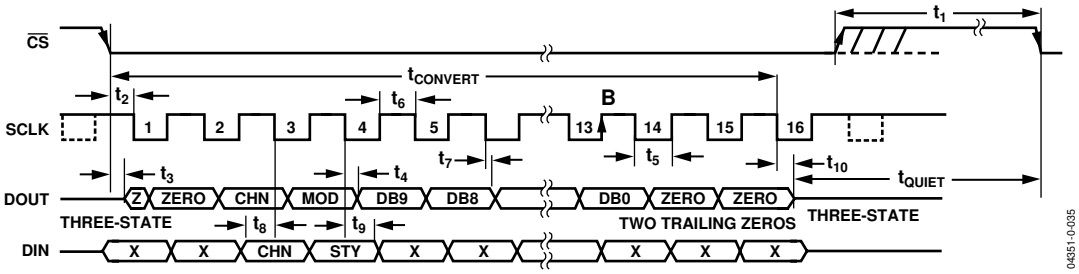

Figure 38. AD7912 Serial Interface Timing Diagram