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14-Bit, 8-Channel, 250 kSPS PulSAR ADC

Data Sheet **AD7949**

FEATURES

- 14-bit resolution with no missing codes
- 8-channel multiplexer with choice of inputs
  - Unipolar single-ended
  - Differential (GND sense)
  - Pseudobipolar
- Throughput: 250 kSPS
- INL/DNL: ±0.5/±0.25 LSB typical
- SINAD: 85 dB @ 20 kHz
- THD: −100 dB @ 20 kHz
- Analog input range: 0 V to V_{REF} with V_{REF} up to VDD
- Multiple reference types
  - Internal selectable 2.5 V or 4.096 V
  - External buffered (up to 4.096 V)
  - External (up to VDD)
- Internal temperature sensor (TEMP)
- Channel sequencer, selectable 1-pole filter, busy indicator
- No pipeline delay, SAR architecture
- Single-supply 2.3 V to 5.5 V operation with 1.8 V to 5.5 V logic interface
- Serial interface compatible with SPI, MICROWIRE, QSPI, and DSP
- Power dissipation
  - 2.9 mW @ 2.5 V/200 kSPS
  - 10.8 mW @ 5 V/250 kSPS
- Standby current: 50 nA
- 20-lead 4 mm × 4 mm LFCSP package

APPLICATIONS

- Multichannel system monitoring
- Battery-powered equipment
- Medical instruments: ECG/EKG
- Mobile communications: GPS
- Power line monitoring
- Data acquisition
- Seismic data acquisition systems
- Instrumentation
- Process control

FUNCTIONAL BLOCK DIAGRAM

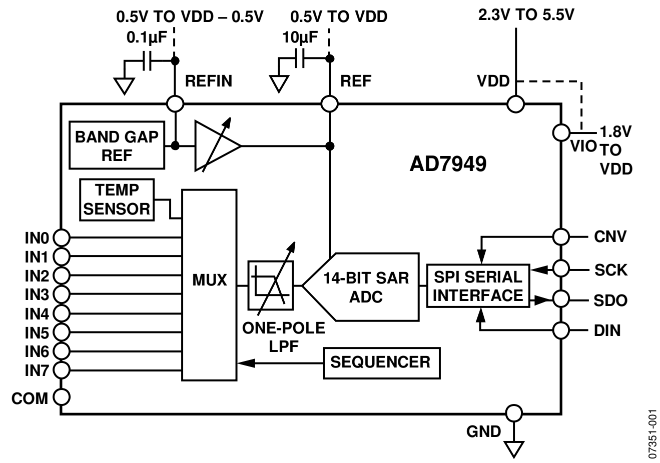

Figure 1.

Table 1. Multichannel 14-/16-Bit PulSAR® ADCs

Type	Channels	250 kSPS	500 kSPS	ADC Driver
14-Bit	8	AD7949		ADA4841-1
16-Bit	4	AD7682		ADA4841-1
16-Bit	8	AD7689	AD7699	ADA4841-1

GENERAL DESCRIPTION

The AD7949 is an 8-channel, 14-bit, charge redistribution successive approximation register (SAR) analog-to-digital converter (ADC) that operates from a single power supply, VDD.

The AD7949 contains all components for use in a multichannel, low power data acquisition system, including a true 14-bit SAR ADC with no missing codes; an 8-channel, low crosstalk multiplexer that is useful for configuring the inputs as single-ended (with or without ground sense), differential, or bipolar; an internal low drift reference (selectable 2.5 V or 4.096 V) and buffer; a temperature sensor; a selectable one-pole filter; and a sequencer that is useful when channels are continuously scanned in order.

The AD7949 uses a simple SPI interface for writing to the configuration register and receiving conversion results. The SPI interface uses a separate supply, VIO, which is set to the host logic level. Power dissipation scales with throughput.

The AD7949 is housed in a tiny 20-lead LFCSP with operation specified from −40°C to +85°C.

Rev. E Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

AD7949* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7949 Evaluation Kit

DOCUMENTATION

Application Notes

- AN-931: Understanding PulSAR ADC Support Circuitry
- AN-932: Power Supply Sequencing

Data Sheet

- AD7949-DSCC: Military Data Sheet
- AD7949-EP: Enhanced Product Data Sheet
- AD7949: 14-Bit, 8-Channel, 250 kSPS PulSAR ADC Data Sheet

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD7949 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7949 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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TABLE OF CONTENTS

REVISION HISTORY

5/15—Rev. D to Rev. E

Changed ADA4841-x to ADA4841-1, ADR43x to ADR430/ ADR431/ADR433/ADR434/ADR435, and AD44x to ADR440/ ADR441/ADR443/ADR444/ADR445 .... Throughout
Updated Outline Dimensions... 32
Changes to Ordering Guide.. 32

3/12—Rev. C to Rev. D

Changes to Figure 26 16
Changes to Internal Reference/Temperature Sensor Section 19
Changes to External Reference and Internal Buffer Section 20
Changes to Bits[5:3] Function, Table 9.. 24
Updated Outline Dimensions... 32

8/11—Rev. B to Rev. C

Changes to Internal Reference Section 18
Changes to External Reference and Internal Buffer Section and External Reference Section 19
Changes to Bits[5:3] Function, Table 9.. 22

5/09—Rev. A to Rev. B

Changes to Features Section, Applications Section, and Figure 1 1
Changes to Specifications Section.. 3
Changes to Timing Specifications Section.................................... 5
Changes to Table 5 7
Changes to Figure 4 and Table 6 8
Changes to Figure 20 11
Changes to Converter Operation Section 13
Changes to Table 7 14
Changes to Figure 25 and Figure 26 15
Changes to Bipolar Single Supply Section, Input Structure Section, and Selectable Low-Pass Filter Section 16
Changes to Input Configurations Section, Sequencer Section, and Source Resistance Section 17
Changes to Internal Reference/Temperature Sensor Section 18
Added Figure 30; Renumbered Sequentially 18
Changes to External Reference and Internal Buffer Section, External Reference Section, and Reference Decoupling Section 19
Added Figure 31 and Figure 32 19
Changes to Power Supply Section 20
Changed Reading/Writing During Conversion, Fast Hosts Section to Reading/Writing After Conversion, Any Speed Hosts 21
Changes to Configuration Register, CFG Section and Table 9 22
Added General Timing Without a Busy Indicator Section and Figure 36 23
Added General Timing with a Busy Indicator Section and Figure 37 24
Added Channel Sequencer Section, Examples Section, and Figure 38 25
Changes to Read/Write Spanning Conversion Without a Busy Indicator Section and Figure 40 26
Changes to Read/Write Spanning Conversion with a Busy Indicator Section and Figure 42 27
Changes to Evaluating AD7949 Performance Section 28
Added Exposed Pad Notation to Outline Dimensions 29
Changes to Ordering Guide.. 29

5/08—Rev. 0 to Rev. A

Changes to Ordering Guide.. 26

5/08—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, V_{REF} = VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ANALOG INPUT					
Voltage Range	Unipolar mode	0		$+V_{REF}$	V
	Bipolar mode	$-V_{REF}/2$		$+V_{REF}/2$	
Absolute Input Voltage	Positive input, unipolar and bipolar modes	−0.1		V_{REF} + 0.1	V
	Negative or COM input, unipolar mode	−0.1		+0.1	
	Negative or COM input, bipolar mode	$V_{REF}/2$ − 0.1	$V_{REF}/2$	$V_{REF}/2$ + 0.1	
Analog Input CMRR	f_{IN} = 250 kHz		68		dB
Leakage Current at 25°C	Acquisition phase		1		nA
Input Impedance[1]					
THROUGHPUT					
Conversion Rate					
Full Bandwidth[2]	VDD = 4.5 V to 5.5 V	0		250	kSPS
	VDD = 2.3 V to 4.5 V	0		200	kSPS
¼ Bandwidth[2]	VDD = 4.5 V to 5.5 V	0		62.5	kSPS
	VDD = 2.3 V to 4.5 V	0		50	kSPS
Transient Response	Full-scale step, full bandwidth			1.8	µs
	Full-scale step, ¼ bandwidth			14.5	µs
ACCURACY					
No Missing Codes		14			Bits
Integral Linearity Error		−1	±0.5	+1	LSB[3]
Differential Linearity Error		−1	±0.25	+1	LSB
Transition Noise	REF = VDD = 5 V		0.1		LSB
Gain Error[4]		−5	±0.5	+5	LSB
Gain Error Match		−1	±0.2	+1	LSB
Gain Error Temperature Drift			±1		ppm/°C
Offset Error[4]			±0.5		LSB
Offset Error Match		−1	±0.2	+1	LSB
Offset Error Temperature Drift			±1		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±0.2		LSB
AC ACCURACY[5]					
Dynamic Range			85.6		dB[6]
Signal-to-Noise	f_{IN} = 20 kHz, V_{REF} = 5 V	84.5	85.5		dB
	f_{IN} = 20 kHz, V_{REF} = 4.096 V internal REF		85		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V internal REF		84		dB
SINAD	f_{IN} = 20 kHz, V_{REF} = 5 V	84	85		dB
	f_{IN} = 20 kHz, V_{REF} = 5 V, −60 dB input		33.5		dB
	f_{IN} = 20 kHz, V_{REF} = 4.096 V internal REF		85		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V internal REF		84		dB
Total Harmonic Distortion	f_{IN} = 20 kHz		−100		dB
Spurious-Free Dynamic Range	f_{IN} = 20 kHz		108		dB
Channel-to-Channel Crosstalk	f_{IN} = 100 kHz on adjacent channel(s)		−125		dB
SAMPLING DYNAMICS					
−3 dB Input Bandwidth	Full bandwidth		1.7		MHz
	¼ bandwidth		0.425		MHz
Aperture Delay	VDD = 5 V		2.5		ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INTERNAL REFERENCE					
REF Output Voltage	2.5 V, @ 25°C	2.490	2.500	2.510	V
	4.096 V, @ 25°C	4.086	4.096	4.106	V
REFIN Output Voltage[7]	2.5 V, @ 25°C		1.2		V
	4.096 V, @ 25°C		2.3		V
REF Output Current			±300		µA
Temperature Drift			±10		ppm/°C
Line Regulation	VDD = 5 V ± 5%		±15		ppm/V
Long-Term Drift	1000 hours		50		ppm
Turn-On Settling Time	CREF = 10 µF		5		ms
EXTERNAL REFERENCE					
Voltage Range	REF input	0.5		VDD + 0.3	V
	REFIN input (buffered)	0.5		VDD − 0.5	V
Current Drain	250 kSPS, REF = 5 V		50		µA
TEMPERATURE SENSOR					
Output Voltage[8]	@ 25°C		283		mV
Temperature Sensitivity			1		mV/°C
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.3 × VIO	V
V_{IH}		0.7 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format[9]					
Pipeline Delay[10]					
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD	Specified performance	2.3		5.5	V
VIO	Specified performance	2.3		VDD + 0.3	V
	Operating range	1.8		VDD + 0.3	V
Standby Current[11, 12]	VDD and VIO = 5 V, @ 25°C		50		nA
Power Dissipation	VDD = 2.5 V, 100 SPS throughput		1.5		µW
	VDD = 2.5 V, 100 kSPS throughput		1.45	2.0	mW
	VDD = 2.5 V, 200 kSPS throughput		2.9	4.0	mW
	VDD = 5 V, 250 kSPS throughput		10.8	12.5	mW
	VDD = 5 V, 250 kSPS throughput with internal reference		13.5	15.5	mW
Energy per Conversion			50		nJ
TEMPERATURE RANGE[13]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] See the Analog Inputs section.
[2] The bandwidth is set in the configuration register.
[3] LSB means least significant bit. With the 5 V input range, one LSB = 305 µV.
[4] See the Terminology section. These specifications include full temperature range variation but not the error contribution from the external reference.
[5] With VDD = 5 V, unless otherwise noted.
[6] All specifications expressed in decibels are referred to a full-scale input FSR and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[7] This is the output from the internal band gap.
[8] The output voltage is internal and present on a dedicated multiplexer input.
[9] Unipolar mode: serial 14-bit straight binary.
Bipolar mode: serial 14-bit twos complement.
[10] Conversion results available immediately after completed conversion.
[11] With all digital inputs forced to VIO or GND as required.
[12] During acquisition phase.
[13] Contact an Analog Devices, Inc., sales representative for the extended temperature range.

TIMING SPECIFICATIONS

VDD = 4.5 V to 5.5 V, VIO = 1.8 V to VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1]	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}			2.2	µs
Acquisition Time	t_{ACQ}	1.8			µs
Time Between Conversions	t_{CYC}	4.0			µs
Data Write/Read During Conversion	t_{DATA}			1.0	µs
CNV Pulse Width	t_{CNVH}	10			ns
SCK Period	t_{SCK}	t_{DSDO} + 2			ns
SCK Low Time	t_{SCKL}	11			ns
SCK High Time	t_{SCKH}	11			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	4			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				23	ns
VIO Above 1.8 V				28	ns
CNV Low to SDO D15 MSB Valid	t_{EN}				
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				22	ns
VIO Above 1.8 V				25	ns
CNV High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}			32	ns
CNV Low to SCK Rising Edge	t_{CLSCK}	10			ns
DIN Valid Setup Time from SCK Rising Edge	t_{SDIN}	5			ns
DIN Valid Hold Time from SCK Rising Edge	t_{HDIN}	5			ns

[1] See Figure 2 and Figure 3 for load conditions.

VDD = 2.3 V to 4.5 V, VIO = 1.8 V to VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1]	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}			3.2	µs
Acquisition Time	t_{ACQ}	1.8			µs
Time Between Conversions	t_{CYC}	5			µs
Data Write/Read During Conversion	t_{DATA}			1.2	µs
CNV Pulse Width	t_{CNVH}	10			ns
SCK Period	t_{SCK}	t_{DSDO} + 2			ns
SCK Low Time	t_{SCKL}	12			ns
SCK High Time	t_{SCKH}	12			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 3 V				24	ns
VIO Above 2.7 V				30	ns
VIO Above 2.3 V				38	ns
VIO Above 1.8 V				48	ns
CNV Low to SDO D15 MSB Valid	t_{EN}				
VIO Above 3 V				21	ns
VIO Above 2.7 V				27	ns
VIO Above 2.3 V				35	ns
VIO Above 1.8 V				45	ns
CNV High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}			50	ns
CNV Low to SCK Rising Edge	t_{CLSCK}	10			ns
DIN Valid Setup Time from SCK Rising Edge	t_{SDIN}	5			ns
DIN Valid Hold Time from SCK Rising Edge	t_{HDIN}	5			ns

[1] See Figure 2 and Figure 3 for load conditions.

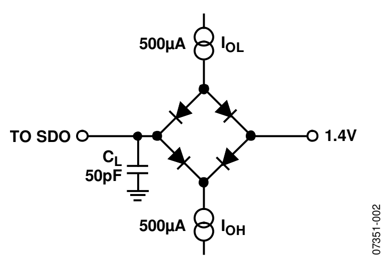


Figure 2. Load Circuit for Digital Interface Timing

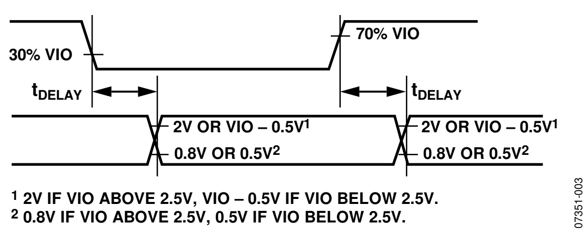


Figure 3. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs	
INx,[1] COM[1]	GND − 0.3 V to VDD + 0.3 V or VDD ± 130 mA
REF, REFIN	GND − 0.3 V to VDD + 0.3 V
Supply Voltages	
VDD, VIO to GND	−0.3 V to +7 V
VIO to VDD	−0.3 V to VDD + 0.3 V
DIN, CNV, SCK to GND	−0.3 V to VIO + 0.3 V
SDO to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (LFCSP)	47.6°C/W
θ_{JC} Thermal Impedance (LFCSP)	4.4°C/W

[1] See the Analog Inputs section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

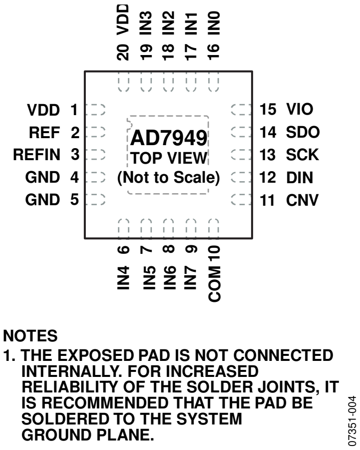


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 20	VDD	P	Power Supply. Nominally 2.5 V to 5.5 V when using an external reference and decoupled with 10 µF and 100 nF capacitors. When using the internal reference for 2.5 V output, the minimum should be 3.0 V. When using the internal reference for 4.096 V output, the minimum should be 4.5 V.
2	REF	AI/O	Reference Input/Output. See the Voltage Reference Output/Input section. When the internal reference is enabled, this pin produces a selectable system reference = 2.5 V or 4.096 V. When the internal reference is disabled and the buffer is enabled, REF produces a buffered version of the voltage present on the REFIN pin (4.096 V maximum), useful when using low cost, low power references. For improved drift performance, connect a precision reference to REF (0.5 V to VDD). For any reference method, this pin needs decoupling with an external 10 µF capacitor connected as close to REF as possible. See the Reference Decoupling section.
3	REFIN	AI/O	Internal Reference Output/Reference Buffer Input. See the Voltage Reference Output/Input section. When using the internal reference, the internal unbuffered reference voltage is present and needs decoupling with a 0.1 µF capacitor. When using the internal reference buffer, apply a source between 0.5 V and 4.096 V that is buffered to the REF pin as described above.
4, 5	GND	P	Power Supply Ground.
6 to 9	IN4 to IN7	AI	Channel 4 through Channel 7 Analog Inputs.
10	COM	AI	Common Channel Input. All input channels, IN[7:0], can be referenced to a common-mode point of 0 V or $V_{REF}/2$ V.
11	CNV	DI	Convert Input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is held high, the busy indictor is enabled.
12	DIN	DI	Data Input. This input is used for writing to the 14-bit configuration register. The configuration register can be written to during and after conversion.
13	SCK	DI	Serial Data Clock Input. This input is used to clock out the data on SDO and clock in data on DIN in an MSB first fashion.
14	SDO	DO	Serial Data Output. The conversion result is output on this pin, synchronized to SCK. In unipolar modes, conversion results are straight binary; in bipolar modes, conversion results are twos complement.
15	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
16 to 19	IN0 to IN3	AI	Channel 0 through Channel 3 Analog Inputs.
21 (EPAD)	Exposed Pad (EPAD)	NC	The exposed pad is not connected internally. For increased reliability of the solder joints, it is recommended that the pad be soldered to the system ground plane.

[1]AI = analog input, AI/O = analog input/output, DI = digital input, DO = digital output, and P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 2.5 V to 5.5 V, V_{REF} = 2.5 V to 5 V, VIO = 2.3 V to VDD, unless otherwise noted.

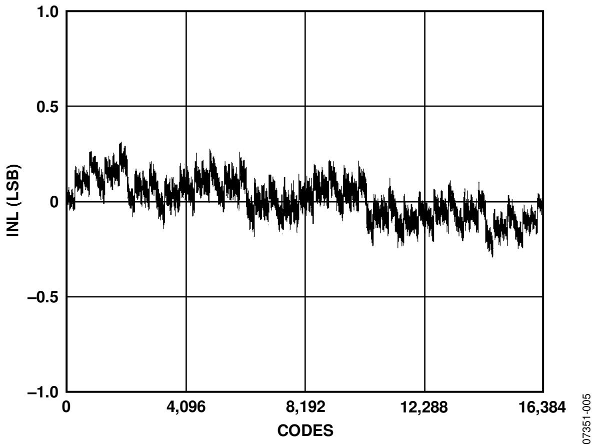


Figure 5. Integral Nonlinearity vs. Code, V_{REF} = VDD = 5 V

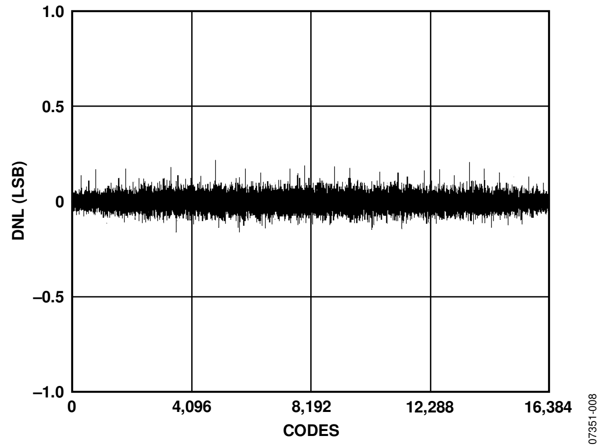


Figure 8. Differential Nonlinearity vs. Code, V_{REF} = VDD = 5 V

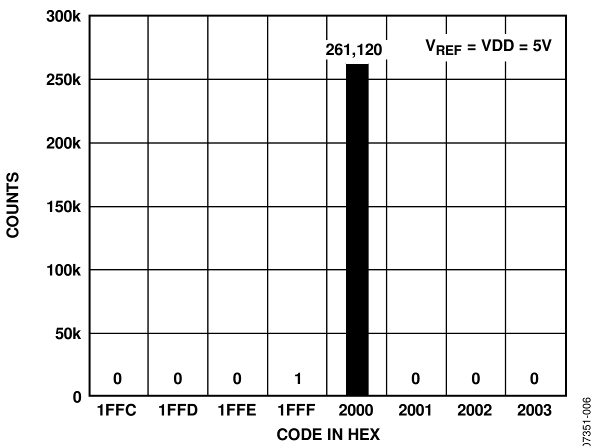


Figure 6. Histogram of a DC Input at Code Center

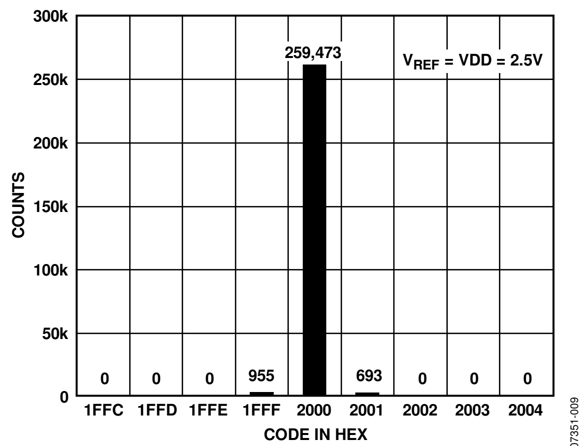


Figure 9. Histogram of a DC Input at Code Center

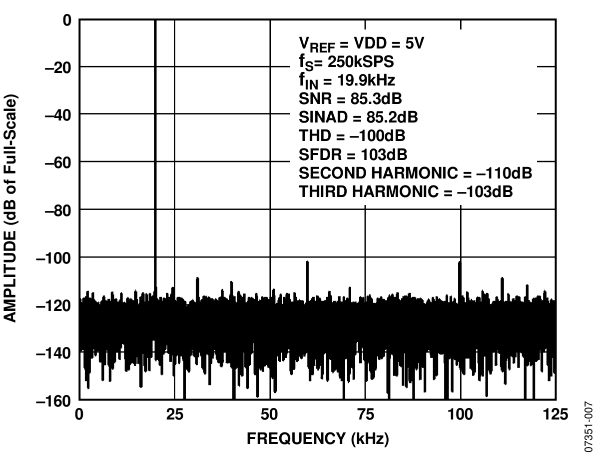


Figure 7. 20 kHz FFT, V_{REF} = VDD = 5 V

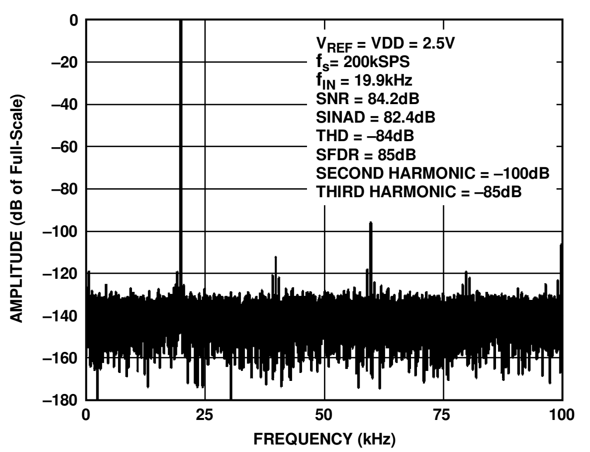


Figure 10. 20 kHz FFT, V_{REF} = VDD = 2.5 V

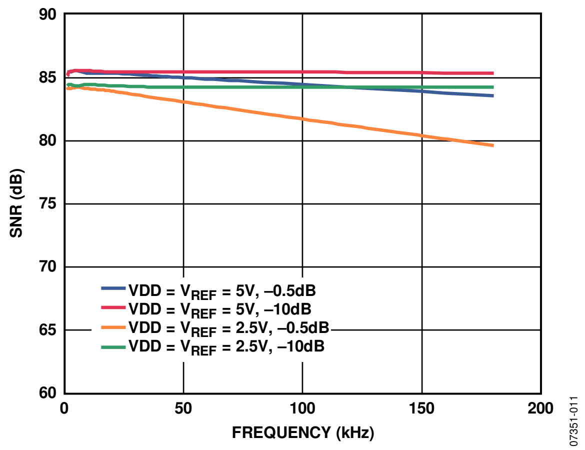


Figure 11. SNR vs. Frequency

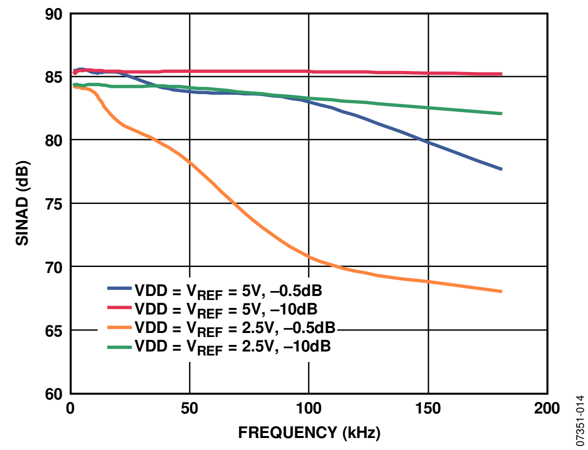


Figure 14. SINAD vs. Frequency

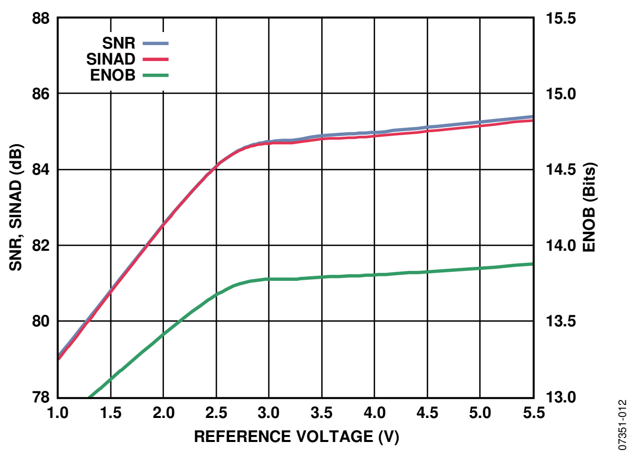


Figure 12. SNR, SINAD, and ENOB vs. Reference Voltage

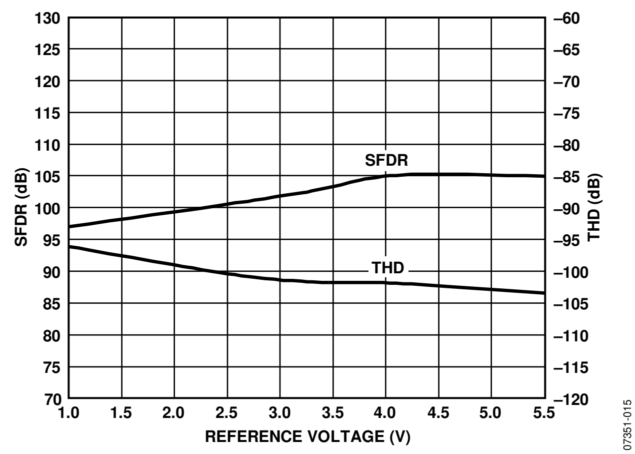


Figure 15. SFDR and THD vs. Reference Voltage

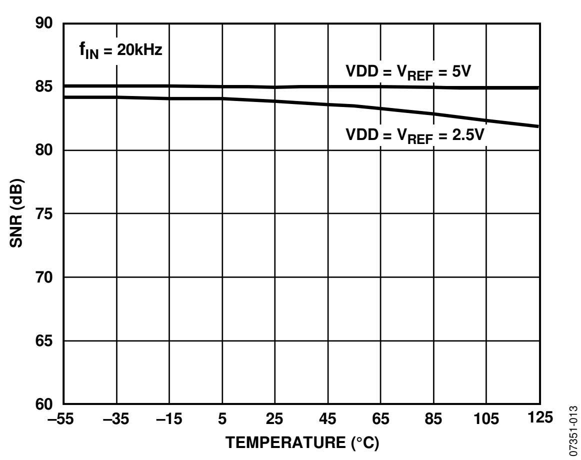


Figure 13. SNR vs. Temperature

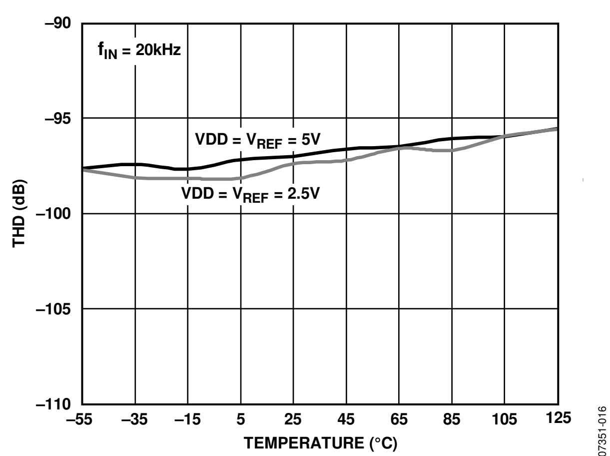


Figure 16. THD vs. Temperature

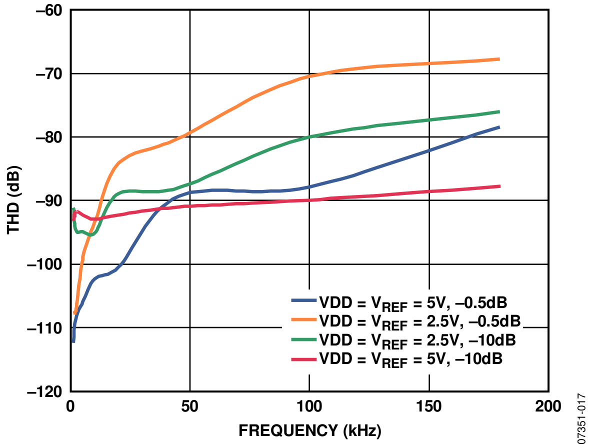


Figure 17. THD vs. Frequency

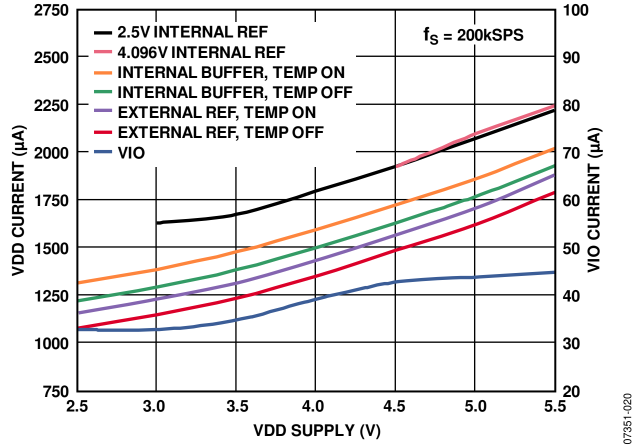


Figure 20. Operating Currents vs. Supply

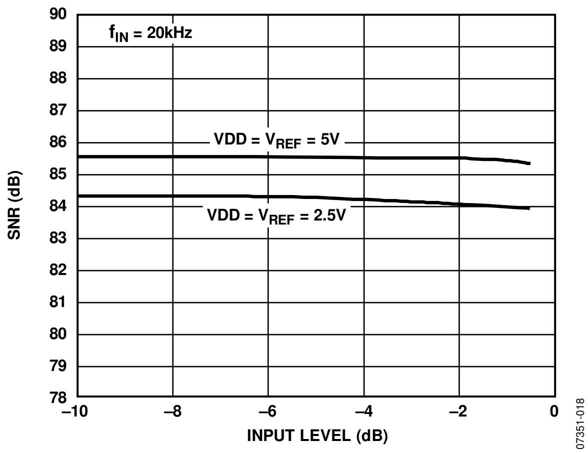


Figure 18. SNR vs. Input Level

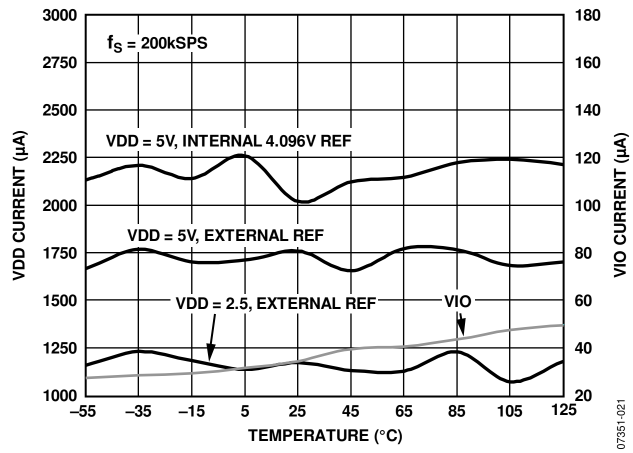


Figure 21. Operating Currents vs. Temperature

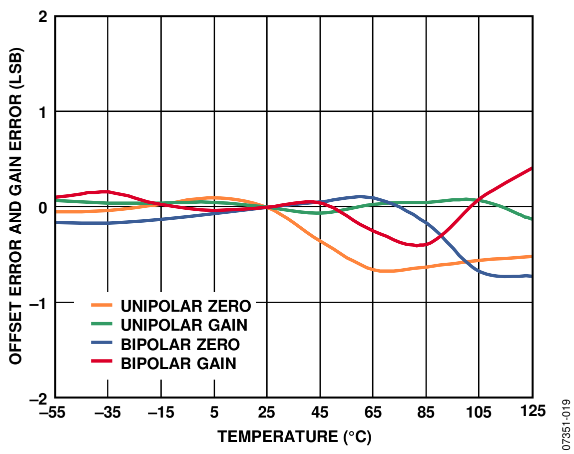


Figure 19. Offset and Gain Errors vs. Temperature

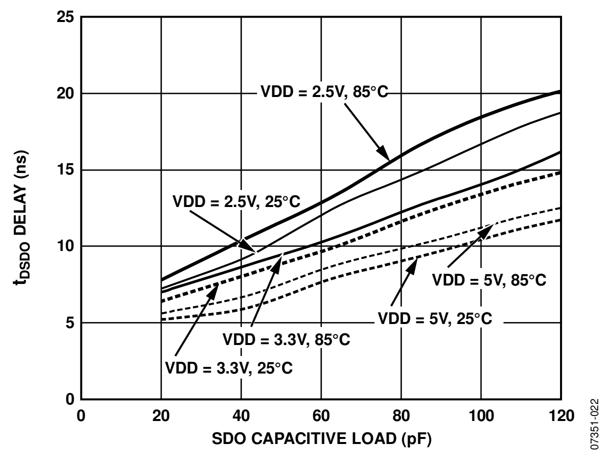


Figure 22. t_{DSDO} Delay vs. SDO Capacitance Load and Supply

TERMINOLOGY

Least Significant Bit (LSB)
The LSB is the smallest increment that can be represented by a converter. For an analog-to-digital converter with N bits of resolution, the LSB expressed in volts is

$$LSB\,(\text{V}) = \frac{V_{REF}}{2^N}$$

Integral Nonlinearity Error (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 24).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error
The first transition should occur at a level ½ LSB above analog ground. The offset error is the deviation of the actual transition from that point.

Gain Error
The last transition (from 111 … 10 to 111 … 11) should occur for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation in LSB (or percentage of full-scale range) of the actual level of the last transition from the ideal level after the offset error is adjusted out. Closely related is the full-scale error (also in LSB or percentage of full-scale range), which includes the effects of the offset error.

Aperture Delay
Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the CNV input and the point at which the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the formula

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

and is expressed in bits.

Channel-to-Channel Crosstalk
Channel-to-channel crosstalk is a measure of the level of crosstalk between any two adjacent channels. It is measured by applying a dc to the channel under test and applying a full-scale, 100 kHz sine wave signal to the adjacent channel(s). The crosstalk is the amount of signal that leaks into the test channel and is expressed in decibels.

Reference Voltage Temperature Coefficient
Reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN}, T (25°C), and T_{MAX}. It is expressed in ppm/°C as

$$TCV_{REF}\,(\text{ppm/°C}) = \frac{V_{REF}\,(Max) - V_{REF}\,(Min)}{V_{REF}\,(25°C) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:
V_{REF} (*Max*) = maximum V_{REF} at T_{MIN}, T (25°C), or T_{MAX}.
V_{REF} (*Min*) = minimum V_{REF} at T_{MIN}, T (25°C), or T_{MAX}.
V_{REF} (25°C) = V_{REF} at 25°C.
T_{MAX} = +85°C.
T_{MIN} = −40°C.

THEORY OF OPERATION

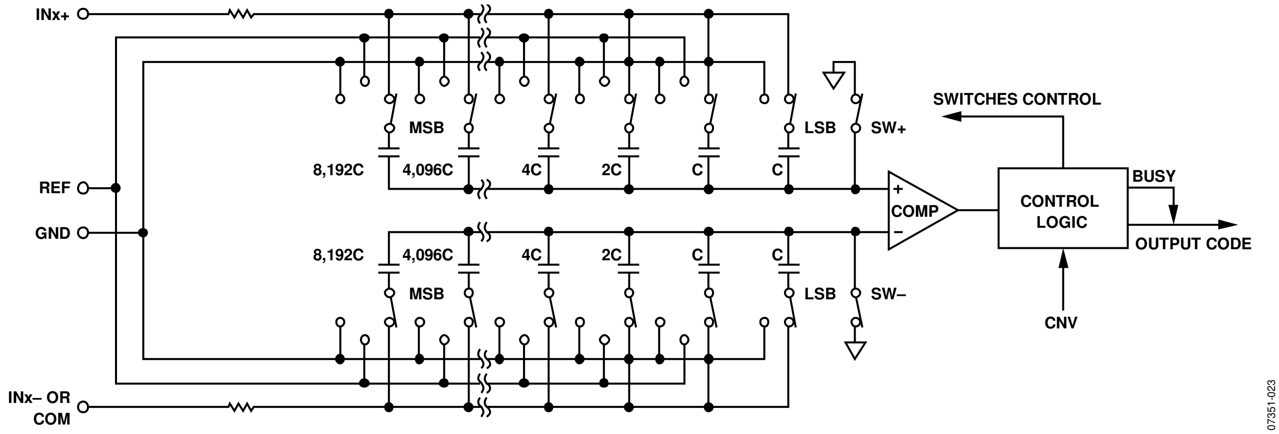


Figure 23. ADC Simplified Schematic

OVERVIEW

The AD7949 is an 8-channel, 14-bit, charge redistribution successive approximation register (SAR) analog-to-digital converter (ADC). The AD7949 is capable of converting 250,000 samples per second (250 kSPS) and powers down between conversions. For example, when operating with an external reference at 1 kSPS, it consumes 15 µW typically, ideal for battery-powered applications.

The AD7949 contains all of the components for use in a multichannel, low power data acquisition system, including

- 14-bit SAR ADC with no missing codes
- 8-channel, low crosstalk multiplexer
- Internal low drift reference and buffer
- Temperature sensor
- Selectable one-pole filter
- Channel sequencer

These components are configured through an SPI-compatible, 14-bit register. Conversion results, also SPI compatible, can be read after or during conversions with the option for reading back the configuration associated with the conversion.

The AD7949 provides the user with an on-chip track-and-hold and does not exhibit pipeline delay or latency.

The AD7949 is specified from 2.3 V to 5.5 V and can be interfaced to any 1.8 V to 5 V digital logic family. The part is housed in a 20-lead, 4 mm × 4 mm LFCSP that combines space savings and allows flexible configurations. It is pin-for-pin compatible with the 16-bit AD7682, AD7689, and AD7699.

CONVERTER OPERATION

The AD7949 is a successive approximation ADC based on a charge redistribution DAC. Figure 23 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 14 binary-weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator input are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs.

Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the INx+ and INx− (or COM) inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the INx+ and INx− (or COM) inputs captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary-weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$, ... $V_{REF}/8,192$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the part returns to the acquisition phase, and the control logic generates the ADC output code and a busy signal indicator.

Because the AD7949 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

TRANSFER FUNCTIONS

With the inputs configured for unipolar range (single-ended, COM with ground sense, or paired differentially with INx− as ground sense), the data output is straight binary.

With the inputs configured for bipolar range (COM = $V_{REF}/2$ or paired differentially with INx− = $V_{REF}/2$), the data outputs are twos complement.

The ideal transfer characteristic for the AD7949 is shown in Figure 24 and for both unipolar and bipolar ranges with the internal 4.096 V reference.

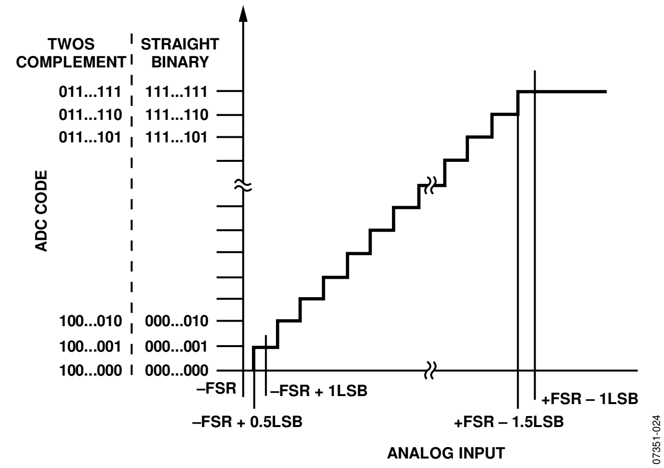


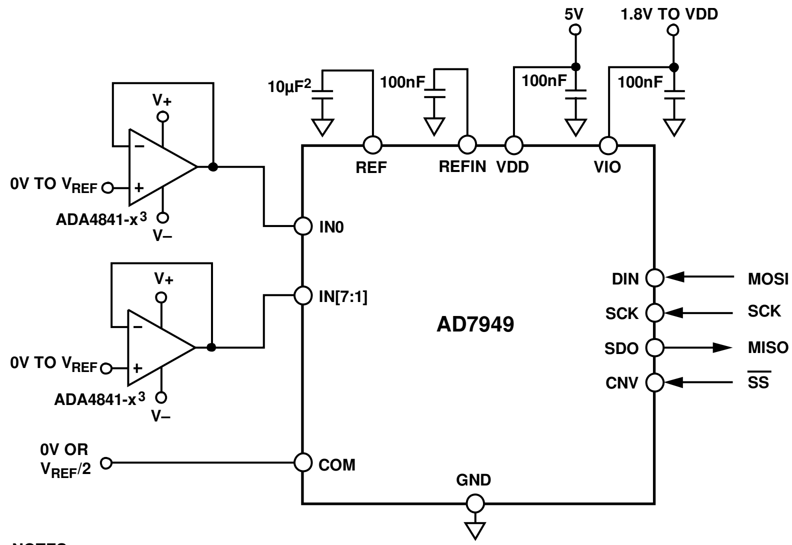
Figure 24. ADC Ideal Transfer Function

Table 7. Output Codes and Ideal Input Voltages

Description	Unipolar Analog Input[1] V_{REF} = 4.096 V	Digital Output Code (Straight Binary Hex)	Bipolar Analog Input[2] V_{REF} = 4.096 V	Digital Output Code (Twos Complement Hex)
FSR – 1 LSB	4.095750 V	0x3FFF[3]	2.047750 V	0x1FFF[3]
Midscale + 1 LSB	2.048250 V	0x2001	250 µV	0x0001
Midscale	2.048000 V	0x2000	0 V	0x0000
Midscale – 1 LSB	2.047750 V	0x1FFF	−250 µV	0x3FFF
−FSR + 1 LSB	250 µV	0x0001	−2.047750 V	0x2001
−FSR	0 V	0x0000[4]	−2.048 V	0x2000[4]

[1] With COM or INx− = 0 V or all INx referenced to GND.
[2] With COM or INx− = V_{REF} /2.
[3] This is also the code for an overranged analog input ((INx+) − (INx−), or COM, above V_{REF} − GND).
[4] This is also the code for an underranged analog input ((INx+) − (INx−), or COM, below GND).

TYPICAL CONNECTION DIAGRAMS



NOTES
1. INTERNAL REFERENCE SHOWN. SEE VOLTAGE REFERENCE OUTPUT/INPUT SECTION FOR REFERENCE SELECTION.
2. C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR (X5R).
3. SEE THE DRIVER AMPLIFIER CHOICE SECTION FOR ADDITIONAL RECOMMENDED AMPLIFIERS.
4. SEE THE DIGITAL INTERFACE SECTION FOR CONFIGURING AND READING CONVERSION DATA.

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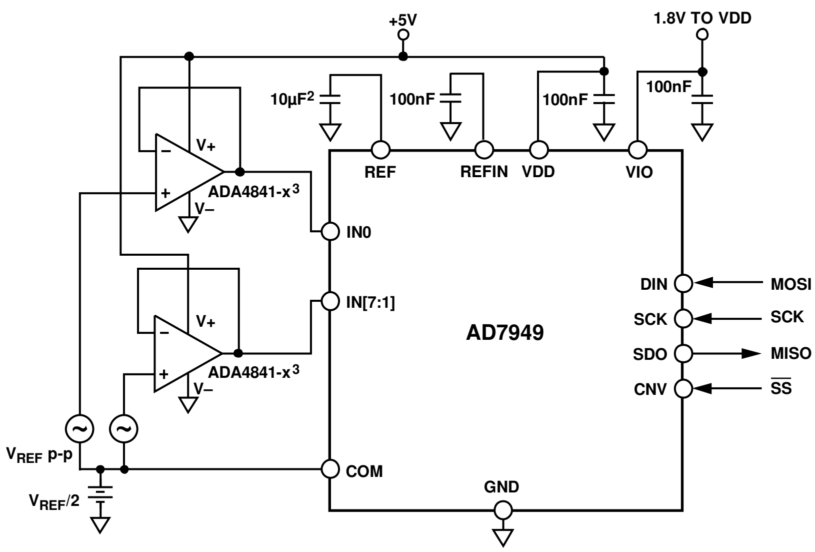
Figure 25. Typical Application Diagram with Multiple Supplies



NOTES
1. INTERNAL REFERENCE SHOWN. SEE VOLTAGE REFERENCE OUTPUT/INPUT SECTION FOR REFERENCE SELECTION.
2. C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR (X5R).
3. SEE THE DRIVER AMPLIFIER CHOICE SECTION FOR ADDITIONAL RECOMMENDED AMPLIFIERS.
4. SEE THE DIGITAL INTERFACE SECTION FOR CONFIGURING AND READING CONVERSION DATA.

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Figure 26. Typical Application Diagram Using Bipolar Input

Unipolar or Bipolar

Figure 25 shows an example of the recommended connection diagram for the AD7949 when multiple supplies are available.

Bipolar Single Supply

Figure 26 shows an example of a system with a bipolar input using single supplies with the internal reference (optional different VIO supply). This circuit is also useful when the amplifier/signal conditioning circuit is remotely located with some common mode present. Note that for any input configuration, the INx inputs are unipolar and are always referenced to GND (no negative voltages even in bipolar range).

For this circuit, a rail-to-rail input/output amplifier can be used; however, the offset voltage vs. input common-mode range should be noted and taken into consideration (1 LSB = 250 μV with V_{REF} = 4.096 V). Note that the conversion results are in twos complement format when using the bipolar input configuration. Refer to the AN-581 Application Note, *Biasing and Decoupling Op Amps in Single Supply Applications,* at www.analog.com for additional details about using single-supply amplifiers.

ANALOG INPUTS

Input Structure

Figure 27 shows an equivalent circuit of the input structure of the AD7949. The two diodes, D1 and D2, provide ESD protection for the analog inputs, IN[7:0] and COM. Care must be taken to ensure that the analog input signal does not exceed the supply rails by more than 0.3 V because this causes the diodes to become forward biased and to start conducting current.

These diodes can handle a forward-biased current of 130 mA maximum. For instance, these conditions may eventually occur when the input buffer supplies are different from VDD. In such a case, for example, an input buffer with a short circuit, the current limitation can be used to protect the part.

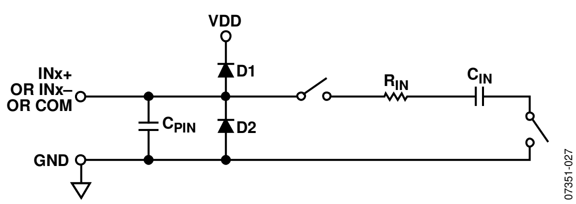

Figure 27. Equivalent Analog Input Circuit

This analog input structure allows the sampling of the true differential signal between INx+ and COM or INx+ and INx–. (COM or INx– = GND ± 0.1 V or V_{REF} ± 0.1 V). By using these differential inputs, signals common to both inputs are rejected, as shown in Figure 28.

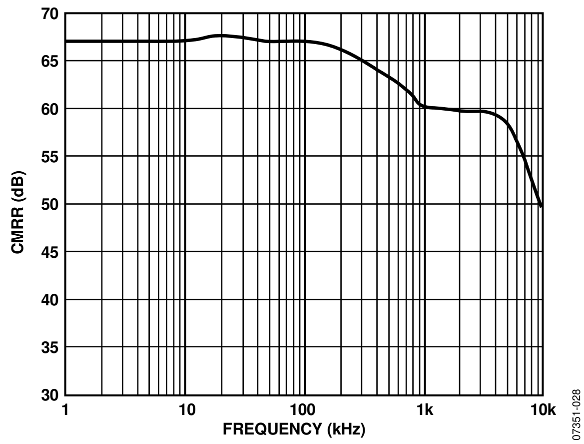

Figure 28. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog inputs can be modeled as a parallel combination of the capacitor, C_{PIN}, and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 2.4 kΩ and is a lumped component composed of serial resistors and the on resistance of the switches. C_{IN} is typically 27 pF and is mainly the ADC sampling capacitor.

Selectable Low-Pass Filter

During the conversion phase, where the switches are opened, the input impedance is limited to C_{PIN}. While the AD7949 is acquiring, R_{IN} and C_{IN} make a one-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise from the driving circuitry. The low-pass filter can be programmed for the full bandwidth or ¼ of the bandwidth with CFG[6], as shown in Table 9. This setting changes R_{IN} to 19 kΩ. Note that the converter throughput must also be reduced by ¼ when using the filter. If the maximum throughput is used with the bandwidth (BW) set to ¼, the converter acquisition time, t_{ACQ}, is violated, resulting in increased THD.

Input Configurations

Figure 29 shows the different methods for configuring the analog inputs with the configuration register, CFG[12:10]. Refer to the Configuration Register, CFG, section for more details.

The analog inputs can be configured as

- Figure 29A, single-ended referenced to system ground; CFG[12:10] = 111_2.
  In this configuration, all inputs (IN[7:0]) have a range of GND to V_{REF}.
- Figure 29B, bipolar differential with a common reference point; COM = $V_{REF}/2$; CFG[12:10] = 010_2.
  Unipolar differential with COM connected to a ground sense; CFG[12:10] = 110_2.
  In these configurations, all inputs IN[7:0] have a range of GND to V_{REF}.
- Figure 29C, bipolar differential pairs with the negative input channel referenced to $V_{REF}/2$; CFG[12:10] = $00X_2$.
  Unipolar differential pairs with the negative input channel referenced to a ground sense; CFG[12:10] = $10X_2$.
  In these configurations, the positive input channels have the range of GND to V_{REF}. The negative input channels are senses referred to $V_{REF}/2$ for bipolar pairs, or GND for unipolar pairs. The positive channel is configured with CFG[9:7]. If CFG[9:7] is even, then IN0, IN2, IN4, and IN6 are used. If CFG[9:7] is odd, then IN1, IN3, IN5, and IN7 are used (channels with parentheses). For example, for IN0/IN1 pairs with the positive channel on IN0, CFG[9:7] = 000_2. For IN4/IN5 pairs with the positive channel on IN5, CFG[9:7] = 101_2.
  Note that for the sequencer, detailed in the Channel Sequencer section, the positive channels are always IN0, IN2, IN4, and IN6.
- Figure 29D, inputs configured in any of the preceding combinations (showing that the AD7949 can be configured dynamically).

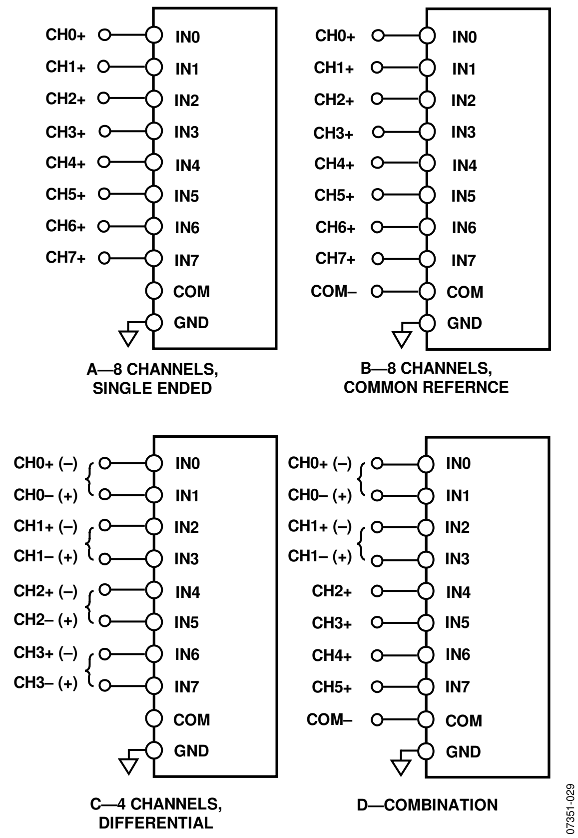

Figure 29. Multiplexed Analog Input Configurations

Sequencer

The AD7949 includes a channel sequencer useful for scanning channels in a repeated fashion. Refer to the Channel Sequencer section for further details of the sequencer operation.

Source Resistance

When the source impedance of the driving circuit is low, the AD7949 can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

DRIVER AMPLIFIER CHOICE

Although the AD7949 is easy to drive, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and transition noise performance of the AD7949. Note that the AD7949 has a noise much lower than most of the other 14-bit ADCs and, therefore, can be driven by a noisier amplifier to meet a given system noise specification. The noise from the amplifier is filtered by the AD7949 analog input circuit low-pass filter made by R_{IN} and C_{IN} or by an external filter, if one is used.
- For ac applications, the driver should have a THD performance commensurate with the AD7949. Figure 17 shows THD vs. frequency for the AD7949.
- For multichannel, multiplexed applications on each input or input pair, the driver amplifier and the AD7949 analog input circuit must settle a full-scale step onto the capacitor array at a 14-bit level (0.0015%). In amplifier data sheets, settling at 0.1% to 0.01% is more commonly specified. This may differ significantly from the settling time at a 14-bit level and should be verified prior to driver selection.

Table 8. Recommended Driver Amplifiers

Amplifier	Typical Application
ADA4841-1	Very low noise, small, and low power
AD8655	5 V single supply, low noise
AD8021	Very low noise and high frequency
AD8022	Low noise and high frequency
OP184	Low power, low noise, and low frequency
AD8605, AD8615	5 V single supply, low power

VOLTAGE REFERENCE OUTPUT/INPUT

The AD7949 allows the choice of a very low temperature drift internal voltage reference, an external reference, or an external buffered reference.

The internal reference of the AD7949 provides excellent performance and can be used in almost all applications. There are six possible choices of voltage reference schemes briefly described in Table 9, with more details in each of the following sections.

Internal Reference/Temperature Sensor

The precision internal reference, suitable for most applications, can be set for either a 2.5 V or a 4.096 V output, as detailed in Table 9. With the internal reference enabled, the band gap voltage is also present on the REFIN pin, which requires an external 0.1 µF capacitor. Because the current output of REFIN is limited, it can be used as a source if followed by a suitable buffer, such as the AD8605. Note that the voltage of REFIN changes depending on the 2.5 V or 4.096 V internal reference.

Enabling the reference also enables the internal temperature sensor, which measures the internal temperature of the AD7949 and is thus useful for performing a system calibration. For applications requiring the use of the temperature sensor, the internal reference must be active (internal buffer can be disabled in this case). Note that, when using the temperature sensor, the output is straight binary referenced from the AD7949 GND pin.

The internal reference is temperature-compensated to within 10 mV. The reference is trimmed to provide a typical drift of ±10 ppm/°C.

Connect the AD7949 as shown in Figure 30 for either a 2.5 V or 4.096 V internal reference.

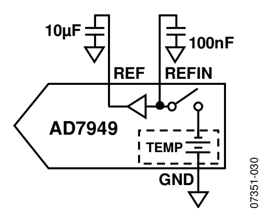

Figure 30. 2.5 V or 4.096 V Internal Reference Connection

External Reference and Internal Buffer

For improved drift performance, an external reference can be used with the internal buffer, as shown in Figure 31. The external source is connected to REFIN, the input to the on-chip unity gain buffer, and the output is produced on the REF pin. An external reference can be used with the internal buffer with or without the temperature sensor enabled. Refer to Table 9 for register details. With the buffer enabled, the gain is unity and is limited to an input/output of VDD = −0.2 V; however, the maximum voltage allowable must be ≤(VDD − 0.5 V).

The internal reference buffer is useful in multiconverter applications because a buffer is typically required in these applications. In addition, a low power reference can be used because the internal buffer provides the necessary performance to drive the SAR architecture of the AD7949.

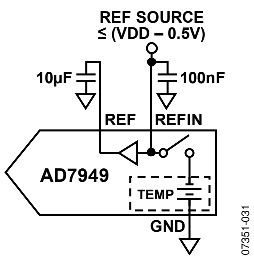

Figure 31. External Reference Using Internal Buffer

External Reference

In any of the six voltage reference schemes, an external reference can be connected directly on the REF pin as shown in Figure 32 because the output impedance of REF is >5 kΩ. To reduce power consumption, the reference and buffer should be powered down. When using only the external reference (and optional reference buffer as shown in Figure 35), the internal buffer is disabled. Refer to Table 9 for register details. For improved drift performance, an external reference such as the ADR430/ADR431/ADR433/ADR434/ADR435 or ADR440/ADR441/ADR443/ADR444/ADR445 is recommended.

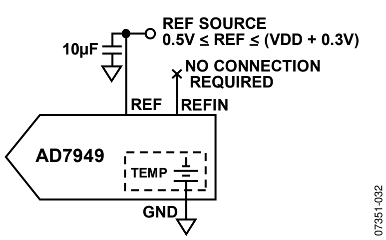

Figure 32. External Reference

Note that the best SNR is achieved with a 5 V external reference as the internal reference is limited to 4.096 V. The SNR degradation is as follows:

$$SNR_{LOSS} = 20 \log \frac{4.096}{5}$$

Reference Decoupling

Whether using an internal or external reference, the AD7949 voltage reference output/input, REF, has a dynamic input impedance and should therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins. This decoupling depends on the choice of the voltage reference but usually consists of a low ESR capacitor connected to REF and GND with minimum parasitic inductance. A 10 µF (X5R, 1206 size) ceramic chip capacitor is appropriate when using the internal reference, the ADR430/ADR431/ADR433/ADR434/ADR435 or ADR440/ADR441/ADR443/ADR444/ADR445 external reference, or a low impedance buffer such as the AD8031 or the AD8605.

The placement of the reference decoupling capacitor is also important to the performance of the AD7949, as explained in the Layout section. Mount the decoupling capacitor on the same side as the ADC at the REF pin with a thick PCB trace. The GND should also be connected to the reference decoupling capacitor with the shortest distance and to the analog ground plane with several vias.

If desired, smaller reference decoupling capacitor values down to 2.2 µF can be used with minimal impact on performance, especially on DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and GND pins.

For applications that use multiple AD7949 devices or other PulSAR devices, it is more effective to use the internal reference buffer to buffer the external reference voltage, thus reducing SAR conversion crosstalk.

The voltage reference temperature coefficient (TC) directly impacts full scale; therefore, in applications where full-scale accuracy matters, care must be taken with the TC. For instance, a ±10 ppm/°C TC of the reference changes full scale by ±1 LSB/°C.

POWER SUPPLY

The AD7949 uses two power supply pins: an analog and digital core supply (VDD) and a digital input/output interface supply (VIO). VIO allows direct interface with any logic between 1.8 V and VDD. To reduce the supplies needed, the VIO and VDD pins can be tied together. The AD7949 is independent of power supply sequencing between VIO and VDD. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 33.

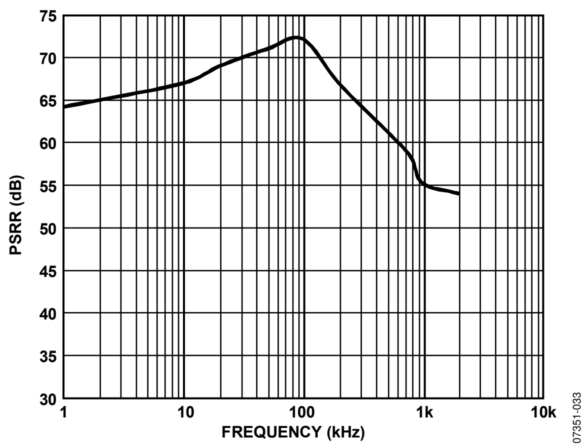

Figure 33. PSRR vs. Frequency

The AD7949 powers down automatically at the end of each conversion phase; therefore, the operating currents and power scale linearly with the sampling rate. This makes the part ideal for low sampling rates (even of a few hertz) and low battery-powered applications.

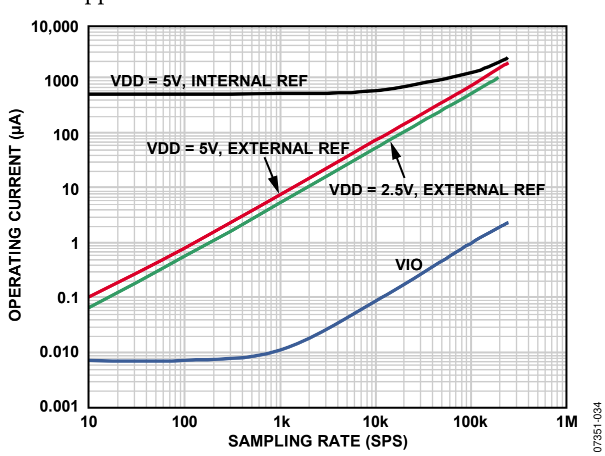

Figure 34. Operating Currents vs. Sampling Rate

SUPPLYING THE ADC FROM THE REFERENCE

For simplified applications, the AD7949, with its low operating current, can be supplied directly using an external reference circuit like the one shown in Figure 35. The reference line can be driven by:

- The system power supply directly
- A reference voltage with enough current output capability, such as the ADR430/ADR431/ADR433/ADR434/ADR435 or ADR440/ADR441/ADR443/ADR444/ADR445
- A reference buffer, such as the AD8605, which can also filter the system power supply, as shown in Figure 35

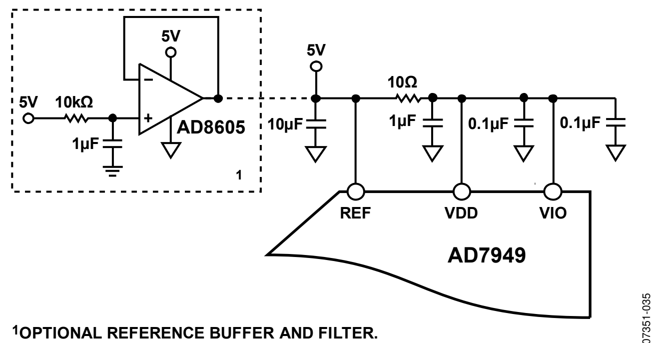

Figure 35. Example of an Application Circuit

DIGITAL INTERFACE

The AD7949 uses a simple 4-wire interface and is compatible with SPI, MICROWIRE™, QSPI™, digital hosts, and DSPs, for example, Blackfin® ADSP-BF53x , SHARC®, ADSP-219x, and ADSP-218x.

The interface uses the CNV, DIN, SCK, and SDO signals and allows CNV, which initiates the conversion, to be independent of the readback timing. This is useful in low jitter sampling or simultaneous sampling applications.

A 14-bit register, CFG[13:0], is used to configure the ADC for the channel to be converted, the reference selection, and other components, which are detailed in the Configuration Register, CFG, section.

When CNV is low, reading/writing can occur during conversion, acquisition, and spanning conversion (acquisition plus conversion), as detailed in the following sections. The CFG word is updated on the first 14 SCK rising edges, and conversion results are output on the first 13 (or 14 if busy mode is selected) SCK falling edges. If the CFG readback is enabled, an additional 14 SCK falling edges are required to output the CFG word associated with the conversion results with the CFG MSB following the LSB of the conversion result.

A discontinuous SCK is recommended because the part is selected with CNV low, and SCK activity begins to write a new configuration word and clock out data.

Note that in the following sections, the timing diagrams indicate digital activity (SCK, CNV, DIN, SDO) during the conversion. However, due to the possibility of performance degradation, digital activity should occur only prior to the safe data reading/writing time, t_{DATA}, because the AD7949 provides error correction circuitry that can correct for an incorrect bit during this time. From t_{DATA} to t_{CONV}, there is no error correction and conversion results may be corrupted. The user should configure the AD7949 and initiate the busy indicator (if desired) prior to t_{DATA}. It is also possible to corrupt the sample by having SCK or DIN transitions near the sampling instant. Therefore, it is recommended to keep the digital pins quiet for approximately 20 ns before and 10 ns after the rising edge of CNV, using a discontinuous SCK whenever possible to avoid any potential performance degradation.

READING/WRITING DURING CONVERSION, FAST HOSTS

When reading/writing during conversion (n), conversion results are for the previous (n − 1) conversion, and writing the CFG register is for the next (n + 1) acquisition and conversion.

After the CNV is brought high to initiate conversion, it must be brought low again to allow reading/writing during conversion. Reading/writing should only occur up to t_{DATA} and, because this time is limited, the host must use a fast SCK.

The SCK frequency required is calculated by

$$f_{SCK} \geq \frac{Number\_SCK\_Edges}{t_{DATA}}$$

The time between t_{DATA} and t_{CONV} is a safe time when digital activity should not occur, or sensitive bit decisions may be corrupted.

READING/WRITING AFTER CONVERSION, ANY SPEED HOSTS

When reading/writing after conversion, or during acquisition (n), conversion results are for the previous (n − 1) conversion, and writing is for the (n + 1) acquisition.

For the maximum throughput, the only time restriction is that the reading/writing take place during the t_{ACQ} (minimum) time. For slow throughputs, the time restriction is dictated by the throughput required by the user, and the host is free to run at any speed. Thus for slow hosts, data access must take place during the acquisition phase.

READING/WRITING SPANNING CONVERSION, ANY SPEED HOST

When reading/writing spanning conversion, the data access starts at the current acquisition (n) and spans into the conversion (n). Conversion results are for the previous (n − 1) conversion, and writing the CFG register is for the next (n + 1) acquisition and conversion.

Similar to reading/writing during conversion, reading/writing should only occur up to t_{DATA}. For the maximum throughput, the only time restriction is that reading/writing take place during the t_{ACQ} + t_{DATA} time.

For slow throughputs, the time restriction is dictated by the user's required throughput, and the host is free to run at any speed. Similar to reading/writing during acquisition, for slow hosts, the data access must take place during the acquisition phase with additional time into the conversion.

Note that data access spanning conversion requires the CNV to be driven high to initiate a new conversion, and data access is not allowed when CNV is high. Thus, the host must perform two bursts of data access when using this method.

CONFIGURATION REGISTER, CFG

The AD7949 uses a 14-bit configuration register (CFG[13:0]), as detailed in Table 9, to configure the inputs, the channel to be converted, the one-pole filter bandwidth, the reference, and the channel sequencer. The CFG register is latched (MSB first) on DIN with 14 SCK rising edges. The CFG update is edge dependent, allowing for asynchronous or synchronous hosts.

The register can be written to during conversion, during acquisition, or spanning acquisition/conversion, and is updated at the end of conversion, t_{CONV} (maximum). There is always a one deep delay when writing the CFG register. Note that, at power-up, the CFG register is undefined and two dummy conversions are required to update the register. To preload the CFG register with a factory setting, hold DIN high for two conversions. Thus CFG[13:0] = 0x3FFF. This sets the AD7949 for the following:

- IN[7:0] unipolar referenced to GND, sequenced in order
- Full bandwidth for a one-pole filter
- Internal reference/temperature sensor disabled, buffer enabled
- Enables the internal sequencer
- No readback of the CFG register

Table 9 summarizes the configuration register bit details. See the Theory of Operation section for more details.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG	INCC	INCC	INCC	INx	INx	INx	BW	REF	REF	REF	SEQ	SEQ	RB

Table 9. Configuration Register Description

Bit(s)	Name	Description			
[13]	CFG	Configuration update.			
		0 = keep current configuration settings.			
		1 = overwrite contents of register.			
[12:10]	INCC	Input channel configuration. Selection of pseudo bipolar, pseudo differential, pairs, single-ended, or temperature sensor. Refer to the Input Configurations section.			
		Bit 12	**Bit 11**	**Bit 10**	**Function**
		0	0	X[1]	Bipolar differential pairs; INx– referenced to $V_{REF}/2 \pm 0.1$ V.
		0	1	0	Bipolar; INx referenced to COM = $V_{REF}/2 \pm 0.1$ V.
		0	1	1	Temperature sensor.
		1	0	X[1]	Unipolar differential pairs; INx– referenced to GND ± 0.1 V.
		1	1	0	Unipolar, INx referenced to COM = GND ± 0.1 V.
		1	1	1	Unipolar, INx referenced to GND.
[9:7]	INx	Input channel selection in binary fashion.			
		Bit 9	**Bit 8**	**Bit 7**	**Channel**
		0	0	0	IN0
		0	0	1	IN1
		…	…	…	
		1	1	1	IN7
[6]	BW	Select bandwidth for low-pass filter. Refer to the Selectable Low-Pass Filter section.			
		0 = ¼ of BW, uses an additional series resistor to further bandwidth limit the noise. Maximum throughput must also be reduced to ¼.			
		1 = full BW.			
[5:3]	REF	Reference/buffer selection. Selection of internal, external, external buffered, and enabling of the on-chip temperature sensor. Refer to the Voltage Reference Output/Input section.			
		Bit 5	**Bit 4**	**Bit 3**	**Function**
		0	0	0	Internal reference, REF = 2.5 V output, temperature enabled.
		0	0	1	Internal reference, REF = 4.096 V output, temperature enabled.
		0	1	0	External reference, temperature enabled.
		0	1	1	External reference, internal buffer, temperature enabled.
		1	1	0	External reference, temperature disabled.
		1	1	1	External reference, internal buffer, temperature disabled.
[2:1]	SEQ	Channel sequencer. Allows for scanning channels in an IN0 to IN[7:0] fashion. Refer to the Channel Sequencer section.			
		Bit 2	**Bit 1**		**Function**
		0	0		Disable sequencer.
		0	1		Update configuration during sequence.
		1	0		Scan IN0 to IN[7:0] (set in CFG[9:7]), then temperature.
		1	1		Scan IN0 to IN[7:0] (set in CFG[9:7]).
[0]	RB	Read back the CFG register.			
		0 = read back current configuration at end of data.			
		1 = do not read back contents of configuration.			

[1] X = don't care.