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4-Channel, 12-/10-/8-Bit ADC with I²C-Compatible Interface in 8-Lead SOT-23

AD7991/AD7995/AD7999

FEATURES

- 12-/10-/8-bit ADCs with fast conversion time: 1 µs typical
- 4 analog input channels/3 analog input channels with reference input
- Specified for V_{DD} of 2.7 V to 5.5 V
- Sequencer operation
- Temperature range: −40°C to +125°C
- I²C-compatible serial interface supports standard, fast, and high speed modes
- 2 versions allow 2 I²C addresses
- Low power consumption
  - Shutdown mode: 1 µA maximum
- 8-lead SOT-23 package

APPLICATIONS

- System monitoring
- Battery-powered systems
- Data acquisition
- Medical instruments

FUNCTIONAL BLOCK DIAGRAM

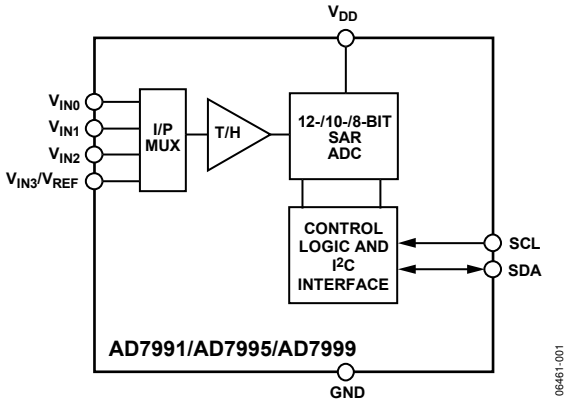

Figure 1.

GENERAL DESCRIPTION

The AD7991/AD7995/AD7999 are 12-/10-/8-bit, low power, successive approximation ADCs with an I²C®-compatible interface. Each part operates from a single 2.7 V to 5.5 V power supply and features a 1 µs conversion time. The track-and-hold amplifier allows each part to handle input frequencies of up to 14 MHz, and a multiplexer allows taking samples from four channels.

Each AD7991/AD7995/AD7999 provides a 2-wire serial interface compatible with I²C interfaces. The AD7991 and AD7995 come in two versions and each version has an individual I²C address. This allows two of the same devices to be connected to the same I²C bus. Both versions support standard, fast, and high speed I²C interface modes. The AD7999 comes in one version.

The AD7991/AD7995/AD7999 normally remain in a shutdown state, powering up only for conversions. The conversion process is controlled by a command mode, during which each I²C read operation initiates a conversion and returns the result over the I²C bus.

When four channels are used as analog inputs, the reference for the part is taken from V_{DD}; this allows the widest dynamic input range to the ADC. Therefore, the analog input range to the ADC is 0 V to V_{DD}. An external reference, applied through the V_{IN3}/V_{REF} input, can also be used with this part.

PRODUCT HIGHLIGHTS

1. Four single-ended analog input channels, or three single-ended analog input channels and one reference input channel.
2. I²C-compatible serial interface. Standard, fast, and high speed modes.
3. Automatic shutdown.
4. Reference derived from the power supply or external reference.
5. 8-lead SOT-23 package.

Table 1. Related Devices

Device	Resolution	Input Channels
AD7998	12	8
AD7997	10	8
AD7994	12	4
AD7993	10	4
AD7992	12	2

Rev. B

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TABLE OF CONTENTS

REVISION HISTORY

10/10—Rev. A to Rev. B

Changes to Max Offset Error Parameter in Table 2 ... 3
Changes to Max Offset Error Parameter (Y Version) in Table 3 ... 5
Changes to Max Offset Error Parameter (Y Version) in Table 4 ... 7
Changes to Ordering Guide ... 27

10/09—Rev. 0 to Rev. A

Changes to Table 3 ... 5
Changes to Table 4 ... 7
Updated Ordering Guide ... 27

12/07—Revision 0: Initial Version

SPECIFICATIONS

AD7991[1]

The temperature range of the Y version is −40°C to +125°C. Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V, V_{REF} = 2.5 V, f_{SCL} = 3.4 MHz, and $T_A = T_{MIN}$ to T_{MAX}.

Table 2.

	Y Version				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DYNAMIC PERFORMANCE[2, 3]					See the Sample Delay and Bit Trial Delay section, f_{IN} = 10 kHz sine wave for f_{SCL} from 1.7 MHz to 3.4 MHz f_{IN} = 1 kHz sine wave for f_{SCL} up to 400 kHz
Signal-to-Noise and Distortion (SINAD)[4]	69.5	70		dB	
Signal-to-Noise Ratio (SNR)[4]	70	71		dB	
Total Harmonic Distortion (THD)[4]			−75.5	dB	
Peak Harmonic or Spurious Noise (SFDR)[4]			−77.5	dB	
Intermodulation Distortion (IMD)[4]					fa = 11 kHz, fb = 9 kHz for f_{SCL} from 1.7 MHz to 3.4 MHz fa = 5.4 kHz, fb = 4.6 kHz for f_{SCL} up to 400 kHz
Second-Order Terms		−92		dB	
Third-Order Terms		−88		dB	
Channel-to-Channel Isolation[4]		−90		dB	f_{IN} = 10 kHz
Full-Power Bandwidth[4]		14		MHz	@ 3 dB
		1.5		MHz	@ 0.1 dB
DC ACCURACY[2, 5]					
Resolution	12			Bits	
Integral Nonlinearity[4]			±1	LSB	
		±0.5		LSB	
Differential Nonlinearity[4]			±0.9	LSB	Guaranteed no missed codes to 12 bits
		±0.5		LSB	
Offset Error[4]		±1	±7	LSB	
Offset Error Matching			±0.5	LSB	
Offset Temperature Drift		4.43		ppm/°C	
Gain Error[4]			±2	LSB	
Gain Error Matching			±0.7	LSB	
Gain Temperature Drift		0.69		ppm/°C	
ANALOG INPUT					
Input Voltage Range	0		V_{REF}	V	$V_{REF} = V_{IN3}/V_{REF}$ or V_{DD}
DC Leakage Current			±1	μA	
Input Capacitance		34		pF	Channel 0 to Channel 2—during acquisition phase
		4		pF	Channel 0 to Channel 2—outside acquisition phase
		35		pF	Channel 3—during acquisition phase
		5		pF	Channel 3—outside acquisition phase
REFERENCE INPUT					
V_{REF} Input Voltage Range	1.2		V_{DD}	V	
DC Leakage Current			±1	μA	
V_{REF} Input Capacitance		5		pF	Outside conversion phase
		35		pF	During conversion phase
Input Impedance		69		kΩ	

Parameter	Y Version Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS (SDA, SCL)					
Input High Voltage, V_{INH}	0.7 (V_{DD})			V	V_{DD} = 2.7 V to 5.5 V
	0.9 (V_{DD})			V	V_{DD} = 2.35 V to 2.7 V
Input Low Voltage, V_{INL}			0.3 (V_{DD})	V	V_{DD} = 2.7 V to 5.5 V
			0.1 (V_{DD})	V	V_{DD} = 2.35 V to 2.7 V
Input Leakage Current, I_{IN}			±1	µA	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[6]			10	pF	
Input Hysteresis, V_{HYST}	0.1 (V_{DD})			V	
LOGIC OUTPUTS (OPEN DRAIN)					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 3 mA
			0.6	V	I_{SINK} = 6 mA
Floating-State Leakage Current			±1	µA	
Floating-State Output Capacitance[6]			10	pF	
Output Coding	Straight (natural) binary				
THROUGHPUT RATE			$18 \times (1/f_{SCL})$		$f_{SCL} \leq 1.7$ MHz; see the Serial Interface section
			$17.5 \times (1/f_{SCL})$ + 2 µs		$f_{SCL} > 1.7$ MHz; see the Serial Interface section
POWER REQUIREMENTS[2]					$V_{REF} = V_{DD}$; for f_{SCL} = 3.4 MHz, clock stretching is implemented
V_{DD}	2.7		5.5	V	
I_{DD}					Digital inputs = 0 V or V_{DD}
ADC Operating, Interface Active (Fully Operational)			0.09/0.25	mA	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
			0.25/0.8	mA	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power-Down, Interface Active[7]			0.07/0.16	mA	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
			0.26/0.85	mA	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power-Down, Interface Inactive[7]			1/1.6	µA	V_{DD} = 3.3 V/5.5 V
Power Dissipation					
ADC Operating, Interface Active (Fully Operational)			0.3/1.38	mW	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
			0.83/4.4	mW	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power-Down, Interface Active[7]			0.24/0.88	mW	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
			0.86/4.68	mW	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power-Down, Interface Inactive[7]			3.3/8.8	µW	V_{DD} = 3.3 V/5.5 V

[1] Functional from V_{DD} = 2.35 V.
[2] Sample delay and bit trial delay enabled, $t_1 = t_2 = 0.5/f_{SCL}$.
[3] For f_{SCL} up to 400 kHz, clock stretching is not implemented. Above f_{SCL} = 400 kHz, clock stretching is implemented.
[4] See the Terminology section.
[5] For $f_{SCL} \leq 1.7$ MHz, clock stretching is not implemented; for $f_{SCL} > 1.7$ MHz, clock stretching is implemented.
[6] Guaranteed by initial characterization.
[7] See the Reading from the AD7991/AD7995/AD7999 section.

AD7995[1]

The temperature range for the Y version is −40°C to +125°C. Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V, V_{REF} = 2.5 V, f_{SCL} = 3.4 MHz, and $T_A = T_{MIN}$ to T_{MAX}.

Table 3.

	A Version[2]			Y Version				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DYNAMIC PERFORMANCE[3, 4]								See the Sample Delay and Bit Trial Delay section, f_{IN} = 10 kHz sine wave for f_{SCL} from 1.7 MHz to 3.4 MHz
								f_{IN} = 1 kHz sine wave for f_{SCL} up to 400 kHz
Signal-to-Noise and Distortion (SINAD)[5]		61.5		61			dB	
Total Harmonic Distortion (THD)[5]		−85				−75	dB	
Peak Harmonic or Spurious Noise (SFDR)[5]		−85				−76	dB	
Intermodulation Distortion (IMD)[5]								fa = 11 kHz, fb = 9 kHz for f_{SCL} from 1.7 MHz to 3.4 MHz
								fa = 5.4 kHz, fb = 4.6 kHz for f_{SCL} up to 400 kHz
Second-Order Terms		−90			−90		dB	
Third-Order Terms		−86			−86		dB	
Channel-to-Channel Isolation[5]		−90			−90		dB	f_{IN} = 10 kHz
Full-Power Bandwidth[5]		14			14		MHz	@ 3 dB
		1.5			1.5		MHz	@ 0.1 dB
DC ACCURACY[3, 6]								
Resolution	10			10			Bits	
Integral Nonlinearity[5]			±0.4			±0.4	LSB	
Differential Nonlinearity[5]			±0.4			±0.4	LSB	Guaranteed no missed codes to 10 bits
Offset Error[5]		±1				±2.25	LSB	
Offset Error Matching		±0.04				±0.2	LSB	
Offset Temperature Drift		4.13			4.13		ppm/°C	
Gain Error[5]		±0.15				±0.5	LSB	
Gain Error Matching		±0.06				±0.25	LSB	
Gain Temperature Drift		0.50			0.50		ppm/°C	
ANALOG INPUT								
Input Voltage Range	0		V_{REF}	0		V_{REF}	V	$V_{REF} = V_{IN3}/V_{REF}$ or V_{DD}
DC Leakage Current			±1			±1	µA	
Input Capacitance		34			34		pF	Channel 0 to Channel 2—during acquisition phase
		4			4		pF	Channel 0 to Channel 2—outside acquisition phase
		35			35		pF	Channel 3—during acquisition phase
		5			5		pF	Channel 3—outside acquisition phase
REFERENCE INPUT								
V_{REF} Input Voltage Range	1.2		V_{DD}	1.2		V_{DD}	V	
DC Leakage Current			±1			±1	µA	
V_{REF} Input Capacitance		5			5		pF	Outside conversion phase
		35			35		pF	During conversion phase
Input Impedance		69			69		kΩ	

Parameter	A Version[2] Min	Typ	Max	Y Version Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS (SDA, SCL)								
Input High Voltage, V_{INH}	0.7 (V_{DD})			0.7 (V_{DD})			V	V_{DD} = 2.7 V to 5.5 V
				0.9 (V_{DD})			V	V_{DD} = 2.35 V to 2.7 V
Input Low Voltage, V_{INL}			0.3 (V_{DD})			0.3 (V_{DD})	V	V_{DD} = 2.7 V to 5.5 V
						0.1 (V_{DD})	V	V_{DD} = 2.35 V to 2.7 V
Input Leakage Current, I_{IN}			±1			±1	µA	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[7]			10			10	pF	
Input Hysteresis, V_{HYST}	0.1 (V_{DD})			0.1 (V_{DD})			V	
LOGIC OUTPUTS (OPEN DRAIN)								
Output Low Voltage, V_{OL}			0.4			0.4	V	I_{SINK} = 3 mA
			0.6			0.6	V	I_{SINK} = 6 mA
Floating-State Leakage Current			±1			±1	µA	
Floating-State Output Capacitance[7]			10			10	pF	
Output Coding	Straight (natural) binary			Straight (natural) binary				
THROUGHPUT RATE			18 × (1/f_{SCL})			18 × (1/f_{SCL})		f_{SCL} ≤ 1.7 MHz; see the Serial Interface section
			17.5 × (1/f_{SCL}) + 2 µs			17.5 × (1/f_{SCL}) + 2 µs		f_{SCL} > 1.7 MHz; see the Serial Interface section
POWER REQUIREMENTS[3]								V_{REF} = V_{DD}; for f_{SCL} = 3.4 MHz, clock stretching is implemented
V_{DD}	2.7		5.5	2.7		5.5	V	
I_{DD}								Digital inputs = 0 V or V_{DD}
ADC Operating, Interface Active (Fully Operational)						0.09/0.25	mA	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
			0.25			0.25/0.8	mA	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power-Down, Interface Active[8]						0.07/0.16	mA	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
			0.26			0.26/0.85	mA	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power-Down, Interface Inactive[8]			1			1/1.6	µA	V_{DD} = 3.3 V/5.5 V
Power Dissipation								
ADC Operating, Interface Active (Fully Operational)						0.3/1.38	mW	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
			0.83			0.83/4.4	mW	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power-Down, Interface Active[8]						0.24/0.88	mW	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
			0.86			0.86/4.68	mW	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power-Down, Interface Inactive[8]			3.3			3.3/8.8	µW	V_{DD} = 3.3 V/5.5 V

[1] Functional from V_{DD} = 2.35 V.
[2] A Version tested at V_{DD} = 3.3 V and f_{SCL} = 3.4 MHz. Functionality tested at f_{SCL} = 400 kHz.
[3] Sample delay and bit trial delay enabled, $t_1 = t_2 = 0.5/f_{SCL}$.
[4] For f_{SCL} up to 400 kHz, clock stretching is not implemented. Above f_{SCL} = 400 kHz, clock stretching is implemented.
[5] See the Terminology section.
[6] For f_{SCL} ≤ 1.7 MHz, clock stretching is not implemented; for f_{SCL} > 1.7 MHz, clock stretching is implemented.
[7] Guaranteed by initial characterization.
[8] See the Reading from the AD7991/AD7995/AD7999 section.

AD7999[1]

The temperature range for the Y version is −40°C to +125°C. Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V, V_{REF} = 2.5 V, f_{SCL} = 3.4 MHz, and $T_A = T_{MIN}$ to T_{MAX}.

Table 4.

	A Version[2]			Y Version				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DYNAMIC PERFORMANCE[3, 4]								See the Sample Delay and Bit Trial Delay section, f_{IN} = 10 kHz sine wave for f_{SCL} from 1.7 MHz to 3.4 MHz f_{IN} = 1 kHz sine wave for f_{SCL} up to 400 kHz
Signal-to-Noise and Distortion (SINAD)[5]	49.5			49.5			dB	
Total Harmonic Distortion (THD)[5]			−65			−65	dB	
Peak Harmonic or Spurious Noise (SFDR)[5]			−65			−65	dB	
Intermodulation Distortion (IMD)[5]								fa = 11 kHz, fb = 9 kHz for f_{SCL} from 1.7 MHz to 3.4 MHz fa = 5.4 kHz, fb = 4.6 kHz for f_{SCL} up to 400 kHz
Second-Order Terms		−83			−83		dB	
Third-Order Terms		−75			−75		dB	
Channel-to-Channel Isolation[5]		−90			−90		dB	f_{IN} = 10 kHz
Full-Power Bandwidth[5]		14			14		MHz	@ 3 dB
		1.5			1.5		MHz	@ 0.1 dB
DC ACCURACY[3, 6]								
Resolution	8			8			Bits	
Integral Nonlinearity[5]		±0.04				±0.1	LSB	
Differential Nonlinearity[5]		±0.05				±0.1	LSB	Guaranteed no missed codes to eight bits
Offset Error[5]		±0.3				±0.5	LSB	
Offset Error Matching		±0.02				±0.05	LSB	
Offset Temperature Drift		4.26			4.26		ppm/°C	
Gain Error[5]		±0.06				±0.175	LSB	
Gain Error Matching		±0.03				±0.06	LSB	
Gain Temperature Drift		0.59			0.59		ppm/°C	
ANALOG INPUT								
Input Voltage Range	0		V_{REF}	0		V_{REF}	V	$V_{REF} = V_{IN3}/V_{REF}$ or V_{DD}
DC Leakage Current			±1			±1	μA	
Input Capacitance		34			34		pF	Channel 0 to Channel 2—during acquisition phase
		4			4		pF	Channel 0 to Channel 2—outside acquisition phase
		35			35		pF	Channel 3—during acquisition phase
		5			5		pF	Channel 3—outside acquisition phase
REFERENCE INPUT								
V_{REF} Input Voltage Range	1.2		V_{DD}	1.2		V_{DD}	V	
DC Leakage Current			±1			±1	μA	
V_{REF} Input Capacitance		5			5		pF	Outside conversion phase
		35			35		pF	During conversion phase
Input Impedance		69			69		kΩ	

Parameter	A Version[2] Min	Typ	Max	Y Version Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS (SDA, SCL)								
Input High Voltage, V_{INH}	0.7 (V_{DD})			0.7 (V_{DD})			V	V_{DD} = 2.7 V to 5.5 V
				0.9 (V_{DD})			V	V_{DD} = 2.35 V to 2.7 V
Input Low Voltage, V_{INL}			0.3 (V_{DD})			0.3 (V_{DD})	V	V_{DD} = 2.7 V to 5.5 V
						0.1 (V_{DD})	V	V_{DD} = 2.35 V to 2.7 V
Input Leakage Current, I_{IN}			±1			±1	µA	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[7]			10			10	pF	
Input Hysteresis, V_{HYST}	0.1 (V_{DD})			0.1 (V_{DD})			V	
LOGIC OUTPUTS (OPEN DRAIN)								
Output Low Voltage, V_{OL}			0.4			0.4	V	I_{SINK} = 3 mA
			0.6			0.6	V	I_{SINK} = 6 mA
Floating-State Leakage Current			±1			±1	µA	
Floating-State Output Capacitance[7]			10			10	pF	
Output Coding	Straight (natural) binary			Straight (natural) binary				
THROUGHPUT RATE			18×(1/f_{SCL})			18×(1/f_{SCL})		f_{SCL} ≤ 1.7 MHz; see the Serial Interface section
			17.5×(1/f_{SCL}) + 2 µs			17.5×(1/f_{SCL}) + 2 µs		f_{SCL} > 1.7 MHz; see the Serial Interface section
POWER REQUIREMENTS[3]								V_{REF} = V_{DD}; for f_{SCL} = 3.4 MHz, clock stretching is implemented
V_{DD}	2.7		5.5	2.7		5.5	V	
I_{DD}								Digital inputs = 0 V or V_{DD}
ADC Operating, Interface Active (Fully Operational)						0.09/0.25	mA	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
			0.25			0.25/0.8	mA	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power-Down, Interface Active[8]						0.07/0.16	mA	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
			0.26			0.26/0.85	mA	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power-Down , Interface Inactive[8]			1			1/1.6	µA	V_{DD} = 3.3 V/5.5 V
Power Dissipation						0.3/1.38	mW	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
ADC Operating, Interface Active (Fully Operational)			0.83			0.83/4.4	mW	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power-Down, Interface Active[8]						0.24/0.88	mW	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
			0.86			0.86/4.68	mW	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power-Down , Interface Inactive[8]			3.3			3.3/8.8	µW	V_{DD} = 3.3 V/5.5 V

[1] Functional from V_{DD} = 2.35 V.
[2] A Version tested at V_{DD}=3.3 V and f_{SCL}= 3.4 MHz. Functionality tested at f_{SCL} = 400 kHz.
[3] Sample delay and bit trial delay enabled, $t_1 = t_2 = 0.5/f_{SCL}$.
[4] For f_{SCL} up to 400 kHz, clock stretching is not implemented. Above f_{SCL} = 400 kHz, clock stretching is implemented.
[5] See the Terminology section.
[6] For f_{SCL} ≤ 1.7 MHz, clock stretching is not implemented; for f_{SCL} > 1.7 MHz, clock stretching is implemented.
[7] Guaranteed by initial characterization.
[8] See the Reading from the AD7991/AD7995/AD7999 section.

I²C TIMING SPECIFICATIONS

Guaranteed by initial characterization. All values were measured with the input filtering enabled. C_B refers to the capacitive load on the bus line, with t_r and t_f measured between 0.3 V_{DD} and 0.7 V_{DD} (see Figure 2). Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V and T_A = T_{MIN} to T_{MAX}.

Table 5.

		Limit at t_{MIN}, t_{MAX}				
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**	**Description**
f_{SCL}[1]	Standard mode			100	kHz	Serial clock frequency
	Fast mode			400	kHz	
	High speed mode					
	C_B = 100 pF maximum			3.4	MHz	
	C_B = 400 pF maximum			1.7	MHz	
t_1[1]	Standard mode	4			µs	t_{HIGH}, SCL high time
	Fast mode	0.6			µs	
	High speed mode					
	C_B = 100 pF maximum	60			ns	
	C_B = 400 pF maximum	120			ns	
t_2[1]	Standard mode	4.7			µs	t_{LOW}, SCL low time
	Fast mode	1.3			µs	
	High speed mode					
	C_B = 100 pF maximum	160			ns	
	C_B = 400 pF maximum	320			ns	
t_3[1]	Standard mode	250			ns	$t_{SU;DAT}$, data setup time
	Fast mode	100			ns	
	High speed mode	10			ns	
t_4[1, 2]	Standard mode	0		3.45	µs	$t_{HD;DAT}$, data hold time
	Fast mode	0		0.9	µs	
	High Speed mode					
	C_B = 100 pF maximum	0		70[3]	ns	
	C_B = 400 pF maximum	0		150	ns	
t_5[1]	Standard mode	4.7			µs	$t_{SU;STA}$, setup time for a repeated start condition
	Fast mode	0.6			µs	
	High Speed mode	160			ns	
t_6[1]	Standard mode	4			µs	$t_{HD;STA}$, hold time for a repeated start condition
	Fast mode	0.6			µs	
	High speed mode	160			ns	
t_7[1]	Standard mode	4.7			µs	t_{BUF}, bus-free time between a stop and a start condition
	Fast mode	1.3			µs	
t_8[1]	Standard mode	4			µs	$t_{SU;STO}$, setup time for a stop condition
	Fast mode	0.6			µs	
	High speed mode	160			ns	
t_9	Standard mode			1000	ns	t_{RDA}, rise time of the SDA signal
	Fast mode	20 + 0.1 C_B		300	ns	
	High speed mode					
	C_B = 100 pF maximum	10		80	ns	
	C_B = 400 pF maximum	20		160	ns	

Parameter	Conditions	Limit at t_{MIN}, t_{MAX} Min	Typ	Max	Unit	Description
t_{10}	Standard mode			300	ns	t_{FDA}, fall time of the SDA signal
	Fast mode	20 + 0.1 C_B		300	ns	
	High speed mode					
	C_B = 100 pF maximum	10		80	ns	
	C_B = 400 pF maximum	20		160	ns	
t_{11}	Standard mode			1000	ns	t_{RCL}, rise time of the SCL signal
	Fast mode	20 + 0.1 C_B		300	ns	
	High speed mode					
	C_B = 100 pF maximum	10		40	ns	
	C_B = 400 pF maximum	20		80	ns	
t_{11A}	Standard mode			1000	ns	t_{RCL1}, rise time of the SCL signal after a repeated start condition and after an acknowledge bit
	Fast mode	20 + 0.1 C_B		300	ns	
	High speed mode					
	C_B = 100 pF maximum	10		80	ns	
	C_B = 400 pF maximum	20		160	ns	
t_{12}	Standard mode			300	ns	t_{FCL}, fall time of the SCL signal
	Fast mode	20 + 0.1 C_B		300	ns	
	High speed mode					
	C_B = 100 pF maximum	10		40	ns	
	C_B = 400 pF maximum	20		80	ns	
t_{SP}[1]	Fast mode	0		50	ns	Pulse width of the suppressed spike
	High speed mode	0		10	ns	
$t_{POWER-UP}$			0.6		µs	Power-up and acquisition time

[1] Functionality is tested during production.
[2] A device must provide a data hold time for SDA in order to bridge the undefined region of the SCL falling edge.
[3] For 3 V supplies, the maximum hold time with C_B = 100 pF maximum is 100 ns maximum.

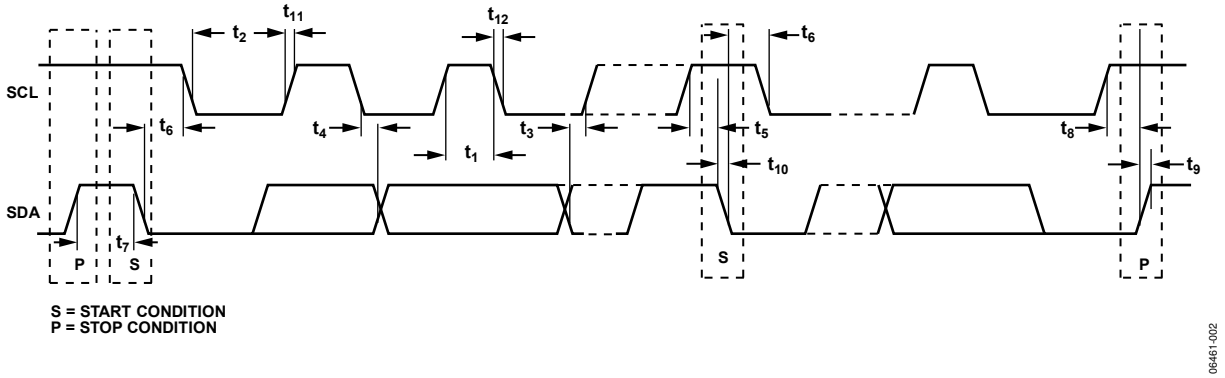

Figure 2. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to GND	−0.3 V to 7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Ranges	
Industrial (Y Version) Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
8-Lead SOT-23 Package	
θ_{JA} Thermal Impedance	170°C/W
θ_{JC} Thermal Impedance	90°C/W
RoHS Compliant Temperature, Soldering Reflow	260 + 0°C
ESD	1 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

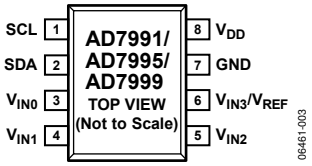

Figure 3. SOT-23 Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCL	Digital Input. Serial bus clock. External pull-up resistor required.
2	SDA	Digital I/O. Serial bus bidirectional data. Open-drain output. External pull-up resistor required.
3	V_{IN0}	Analog Input 1. Single-ended analog input channel. The input range is 0 V to V_{REF}.
4	V_{IN1}	Analog Input 2. Single-ended analog input channel. The input range is 0 V to V_{REF}.
5	V_{IN2}	Analog Input 3. Single-ended analog input channel. The input range is 0 V to V_{REF}.
6	V_{IN3}/V_{REF}	Analog Input 4. Single-ended analog input channel. The input range is 0 V to V_{REF}. Can also be used to input an external V_{REF} signal.
7	GND	Analog Ground. Ground reference point for all circuitry on the AD7991/AD7995/AD7999. All analog input signals should be referred to this AGND voltage.
8	V_{DD}	Power Supply Input. The V_{DD} range for the AD7991/AD7995/AD7999 is from 2.7 V to 5.5 V.

Table 8. I^2C Address Selection

Part Number	I^2C Address
AD7991-0	010 1000
AD7991-1	010 1001
AD7995-0	010 1000
AD7995-1	010 1001
AD7999-1	010 1001

TYPICAL PERFORMANCE CHARACTERISTICS

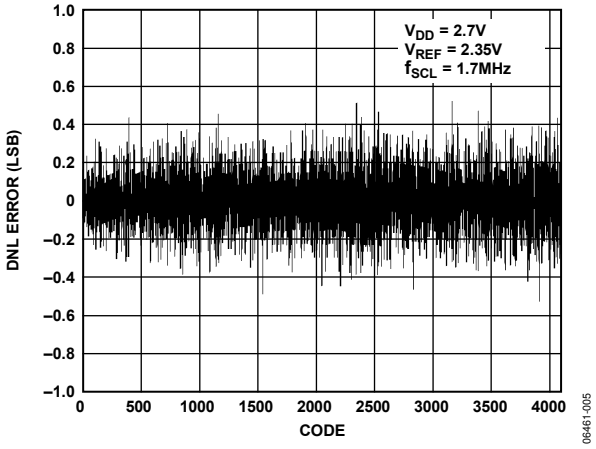

Figure 4. DNL Error, V_{DD} = 2.7 V, V_{REF} = 2.35 V, f_{SCL} = 1.7 MHz Without Clock Stretching

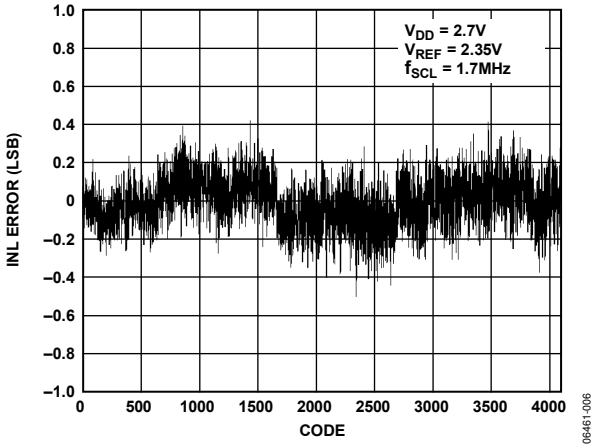

Figure 5. INL Error, V_{DD} = 2.7 V, V_{REF} = 2.35 V, f_{SCL} = 1.7 MHz Without Clock Stretching

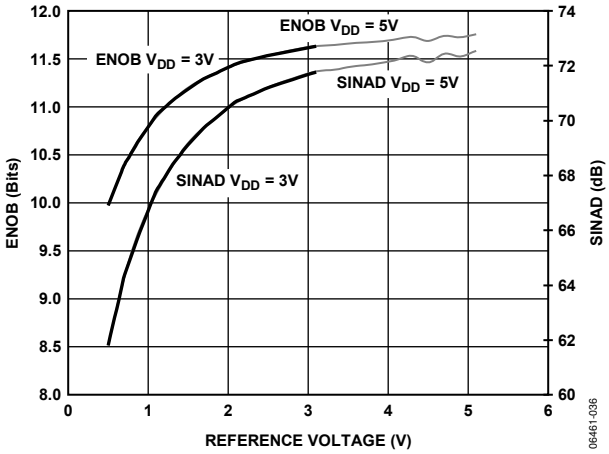

Figure 6. ENOB/SINAD vs. Reference Voltage, f_{SCL} = 1.7 MHz Without Clock Stretching

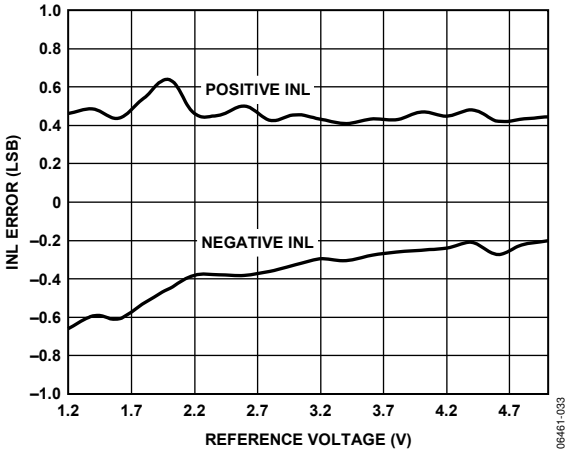

Figure 7. INL Error vs. Reference Voltage , f_{SCL} = 1.7 MHz Without Clock Stretching

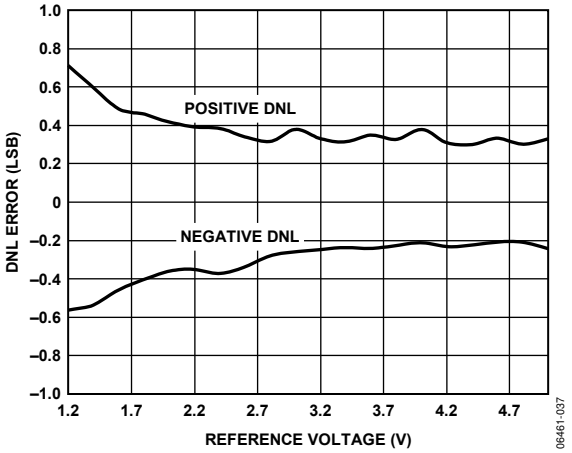

Figure 8. DNL Error vs. Reference Voltage, f_{SCL} = 1.7 MHz Without Clock Stretching

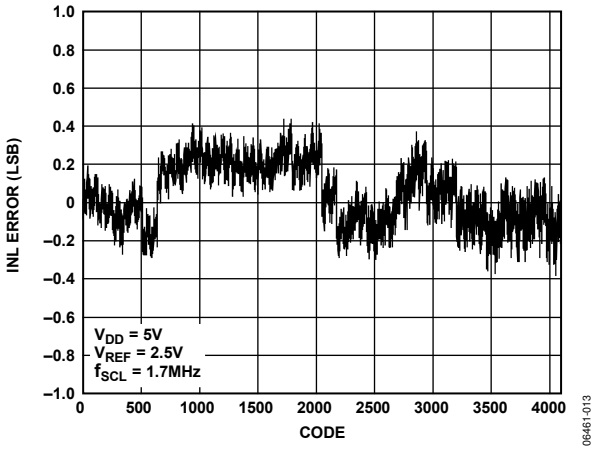

Figure 9. INL Error, V_{DD} = 5 V, V_{REF} = 2.5 V, f_{SCL} = 1.7 MHz Without Clock Stretching

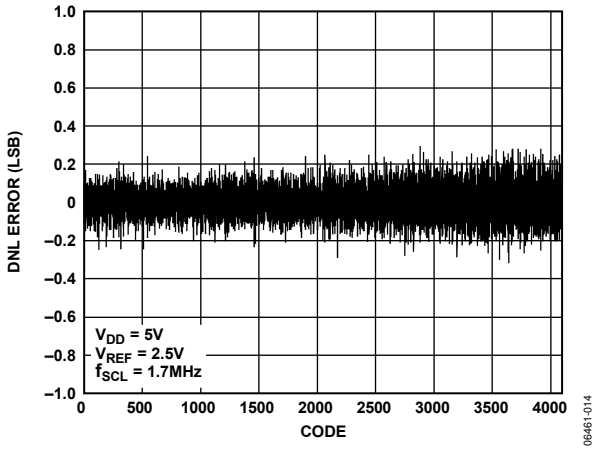

Figure 10. DNL Error, V_{DD} = 5 V, V_{REF} = 2.5 V, f_{SCL} = 1.7 MHz Without Clock Stretching

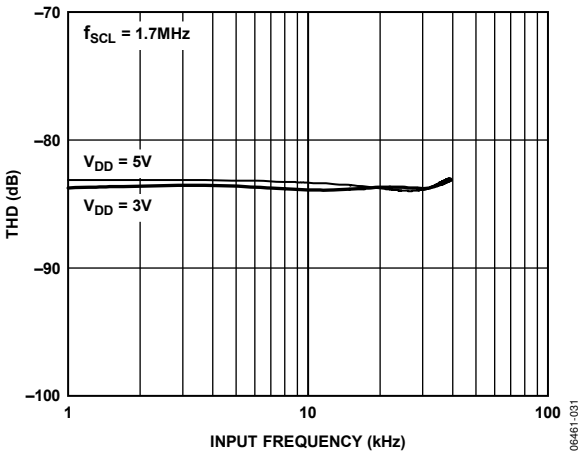

Figure 13. THD vs. Input Frequency, V_{REF} = 2.5 V, f_{SCL} = 1.7 MHz Without Clock Stretching

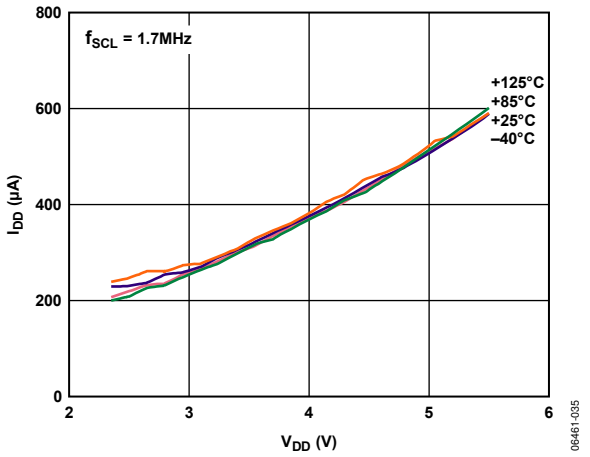

Figure 11. I_{DD} Supply Current vs. Supply Voltage, f_{SCL} = 1.7 MHz Without Clock Stretching, −40°C to +125°C

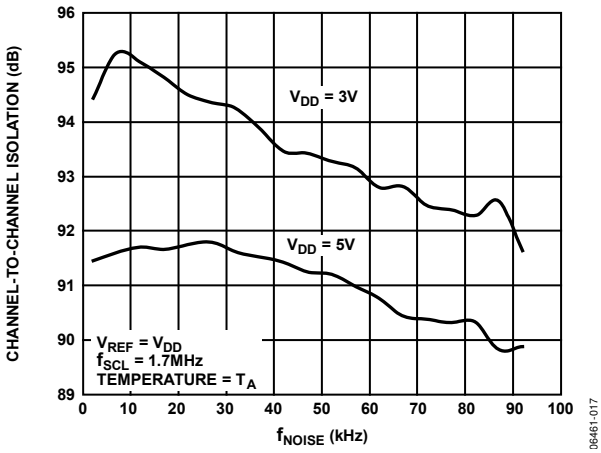

Figure 14. AD7991 Channel-to-Channel Isolation , f_{SCL} = 1.7 MHz Without Clock Stretching

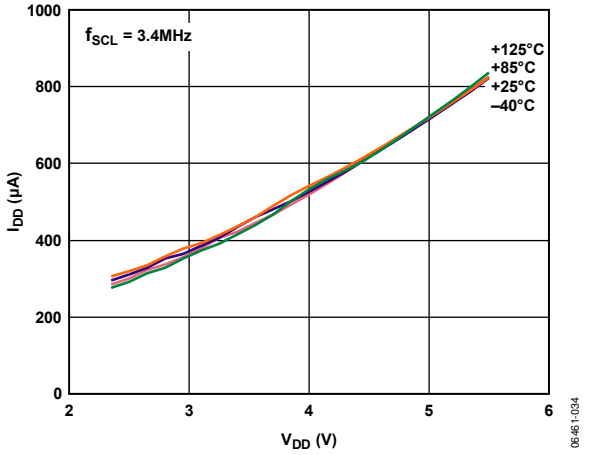

Figure 12. I_{DD} Supply Current vs. Supply Voltage, f_{SCL} = 3.4 MHz with Clock Stretching, −40°C to +125°C

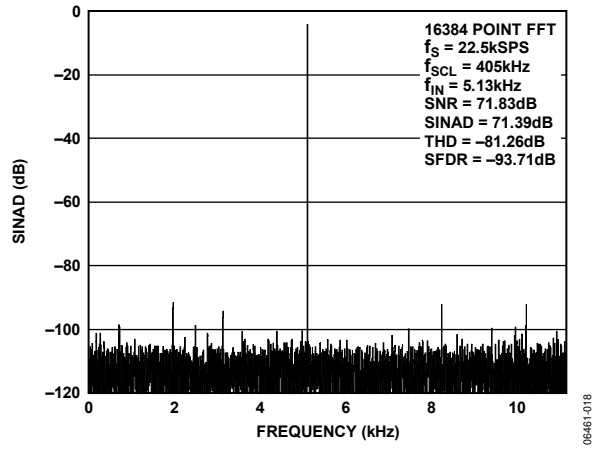

Figure 15. Dynamic Performance, f_{SCL} = 405 kHz Without Clock Stretching, V_{DD} = 5 V, Full-Scale Input, Seven-Term Blackman-Harris Window

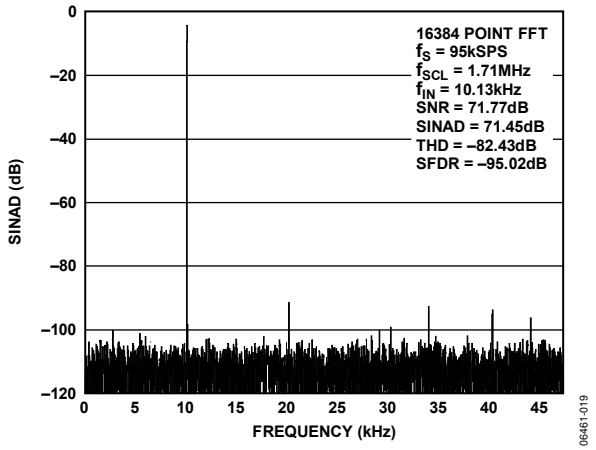

Figure 16. Dynamic Performance, f_{SCL} = 1.71 MHz Without Clock Stretching, V_{DD} = 5 V, Full-Scale Input, Seven-Term Blackman-Harris Window

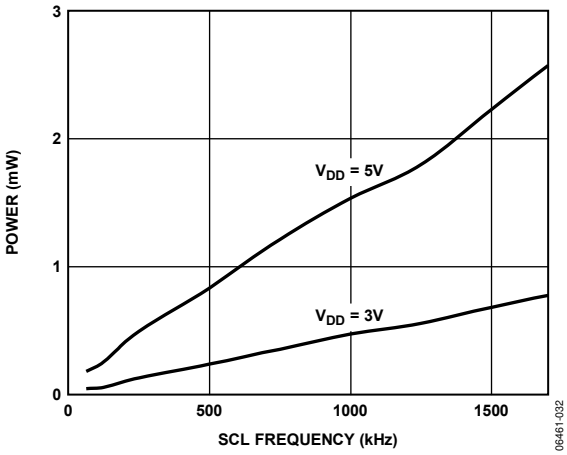

Figure 17. Power vs. SCL Frequency, V_{REF} = 2.5 V

TERMINOLOGY

Signal-to-Noise and Distortion (SINAD) Ratio
The measured ratio of signal-to-noise and distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of the nonfundamental signals excluding dc, up to half the sampling frequency ($f_S/2$). The ratio is dependent on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. The theoretical SINAD ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02\ N + 1.76)\ \text{dB}$$

Therefore, SINAD is 49.92 dB for an 8-bit converter, 61.96 dB for a 10-bit converter, and 74 dB for a 12-bit converter.

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. For the AD7991/AD7995/AD7999, it is defined as

$$THD\ (\text{dB}) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics.

Peak Harmonic or Spurious Noise
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Typically, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, the largest harmonic may be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither *m* nor *n* equals 0. For example, second-order terms include (fa + fb) and (fa − fb), and third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7991/AD7995/AD7999 are tested using the CCIF standard, where two input frequencies near the maximum input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of intermodulation distortion is, like the THD specification, the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals, expressed in decibels.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between any two channels. It is measured by applying a full-scale sine wave signal to all unselected input channels and then determining the degree to which the signal attenuates in the selected channel with a 10 kHz signal. The frequency of the signal in each of the unselected channels is increased from 2 kHz up to 92 kHz. Figure 14 shows the worst-case across all four channels for the AD7991.

Full-Power Bandwidth
The input frequency at which the amplitude of the reconstructed fundamental is reduced by 0.1 dB or 3 dB for a full-scale input.

Integral Nonlinearity
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints are at zero scale (a point 1 LSB below the first code transition) and full scale (a point 1 LSB above the last code transition).

Differential Nonlinearity
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (00 … 000 to 00 … 001) from the ideal—that is, AGND + 1 LSB.

Offset Error Match
The difference in offset error between any two channels.

Gain Error
The deviation of the last code transition (111 … 110 to 111 … 111) from the ideal (that is, V_{REF} − 1 LSB) after the offset error has been adjusted out.

Gain Error Match
The difference in gain error between any two channels.

THEORY OF OPERATION

The AD7991/AD7995/AD7999 are low power, 12-/10-/8-bit, single-supply, 4-channel ADCs. Each part can be operated from a single 2.35 V to 5.5 V supply.

The AD7991/AD7995/AD7999 provide the user with a 4-channel multiplexer, an on-chip track-and-hold, an ADC, and an I²C-compatible serial interface, all housed in an 8-lead SOT-23 package that offers the user considerable space-saving advantages over alternative solutions.

The AD7991/AD7995/AD7999 normally remains in a power-down state while not converting. Therefore, when supplies are first applied, the part is in a power-down state. Power-up is initiated prior to a conversion, and the device returns to the power-down state upon completion of the conversion. This automatic power-down feature allows the device to save power between conversions. This means any read or write operations across the I²C interface can occur while the device is in power-down.

CONVERTER OPERATION

The AD7991/AD7995/AD7999 are successive approximation ADCs built around a capacitive DAC. Figure 18 and Figure 19 show simplified schematics of the ADC during its acquisition and conversion phases, respectively. Figure 18 shows the ADC during its acquisition phase: SW2 is closed, SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on V_{IN}. The source driving the analog input needs to settle the analog input signal to within one LSB in 0.6 µs, which is equivalent to the duration of the power-up and acquisition time.

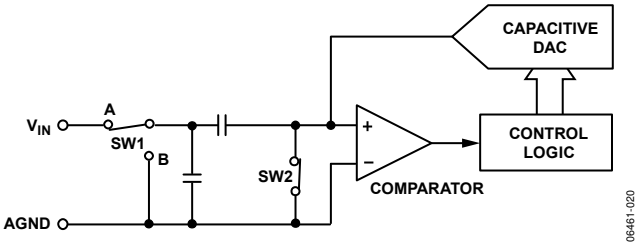

Figure 18. ADC Acquisition Phase

When the ADC starts a conversion, as shown in Figure 19, SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The input is disconnected when the conversion begins. The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 20 shows the ADC transfer function.

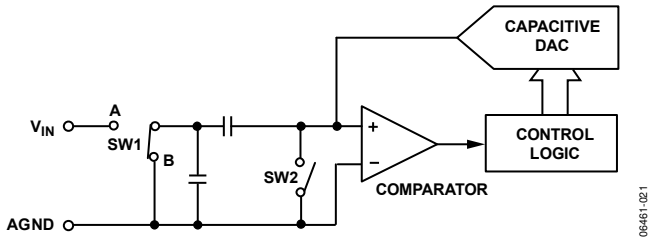

Figure 19. ADC Conversion Phase

ADC Transfer Function

The output coding of the AD7991/AD7995/AD7999 is straight binary. The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSB, and so on). The LSB size for the AD7991/AD7995/AD7999 is $V_{REF}/4096$, $V_{REF}/1024$, and $V_{REF}/256$, respectively. Figure 20 shows the ideal transfer characteristics for the AD7991/AD7995/AD7999.

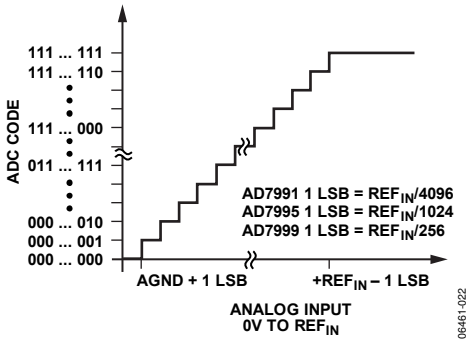

Figure 20. AD7991/AD7995/AD7999 Transfer Characteristics

TYPICAL CONNECTION DIAGRAM

Figure 22 shows the typical connection diagram for the AD7991/AD7995/AD7999.

The reference voltage can be taken from the supply voltage, V_{DD}. However, the AD7991/AD7995/AD7999 can be configured to be a 3-channel device with the reference voltage applied to the V_{IN3}/V_{REF} pin. In this case, a 1 µF decoupling capacitor on the V_{IN3}/V_{REF} pin is recommended.

SDA and SCL form the 2-wire I^2C compatible interface. External pull-up resistors are required for both the SDA and SCL lines.

The AD7991-0/AD7995-0 and the AD7991-1/AD7995-1/AD7999-1 support standard, fast, and high speed I^2C interface modes. Both the -0 and -1 devices have independent I^2C addresses, which allows the devices to connect to the same I^2C bus without contention issues.

The part requires approximately 0.6 µs to wake up from power-down and to acquire the analog input. Once the acquisition phase ends, the conversion phase starts and takes approximately 1 µs to complete. The AD7991/AD7995/AD7999 enters shutdown mode after each conversion, which is useful in applications where power consumption is a concern.

ANALOG INPUT

Figure 21 shows an equivalent circuit of the AD7991/AD7995/AD7999 analog input structure. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal does not exceed the supply rails by more than 300 mV. If the signal does exceed this level, the diodes become forward-biased and start conducting current into the substrate. Each diode can conduct a maximum current of 10 mA without causing irreversible damage to the part.

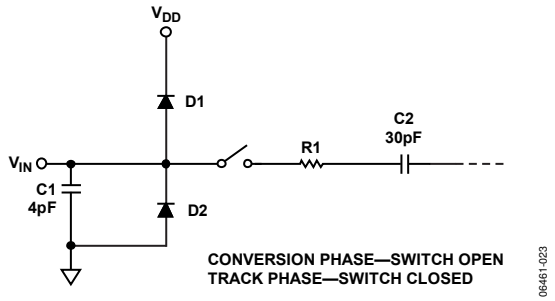

Figure 21. Equivalent Analog Input Circuit

Capacitor C1 in Figure 21 is typically about 4 pF and can primarily be attributed to pin capacitance. Resistor R1 is a lumped component composed of the on resistance (R_{ON}) of both a track-and-hold switch and the input multiplexer. The total resistor is typically about 400 Ω. Capacitor C2, the ADC sampling capacitor, has a typical capacitance of 30 pF.

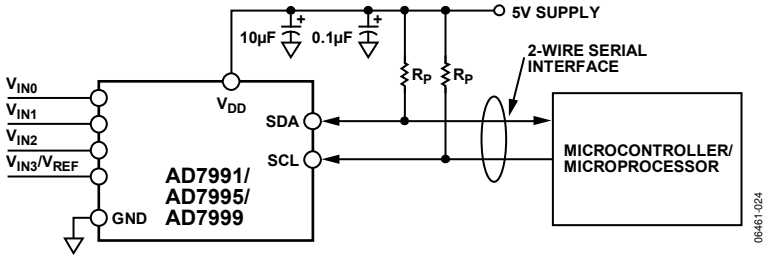

Figure 22. AD7991/AD7995/AD7999 Typical Connection Diagram

For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC band-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of THD that can be tolerated. THD increases as the source impedance increases and performance degrades. Figure 23 shows the THD vs. the analog input signal frequency for different source impedances at a supply voltage of 5 V.

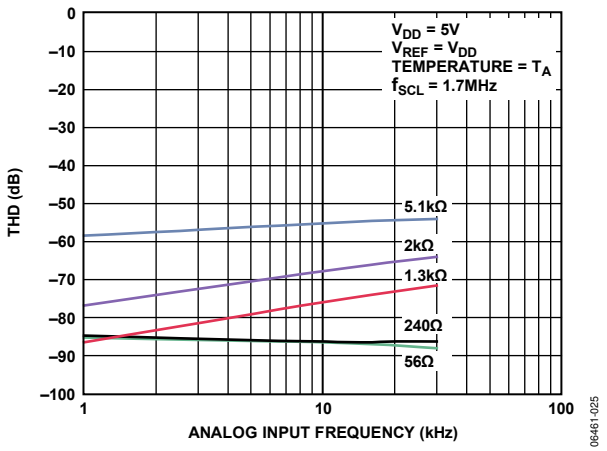

Figure 23. THD vs. Analog Input Frequency for Various Source Impedances for V_{DD} = 5 V, f_{SCL} = 1.7 MHz Without Clock Stretching

INTERNAL REGISTER STRUCTURE

CONFIGURATION REGISTER

The configuration register is an 8-bit write-only register that is used to set the operating modes of the AD7991/AD7995/AD7999. The bit functions are outlined in Table 10. A single-byte write is necessary when writing to the configuration register. D7 is the MSB. When the master writes to the AD7991/AD7995/AD7999, the first byte is written to the configuration register.

Table 9. Configuration Register Bit Map and Default Settings at Power-Up

D7	D6	D5	D4	D3	D2	D1	D0
CH3	CH2	CH1	CH0	REF_SEL	FLTR	Bit trial delay	Sample delay
1	1	1	1	0	0	0	0

Table 10. Bit Function Descriptions

Bit	Mnemonic	Comment
D7 to D4	CH3 to CH0	These four channel address bits select the analog input channel(s) to be converted. If a channel address bit (Bit D7 to Bit D4) is set to 1, a channel is selected for conversion. If more than one channel bit is set to 1, the AD7991/AD7995/AD7999 sequence through the selected channels, starting with the lowest channel. All unused channels should be set to 0. Table 11 shows how these four channel address bits are decoded. Prior to the device initiating a conversion, the channel(s) must be selected in the configuration register.
D3	REF_SEL	This bit allows the user to select the supply voltage as the reference or choose to use an external reference. If this bit is 0, the supply is used as the reference, and the device acts as a 4-channel input part. If this bit is set to 1, an external reference must be used and applied to the V_{IN3}/V_{REF} pin, and the device acts as a 3-channel input part.
D2	FLTR	The value written to this bit of the control register determines whether the filtering on SDA and SCL is enabled or bypassed. If this bit is set to 0, the filtering is enabled; if it set to 1, the filtering is bypassed.
D1	Bit trial delay	See the Sample Delay and Bit Trial Delay section.
D0	Sample delay	See the Sample Delay and Bit Trial Delay section.

Table 11. Channel Selection

D7	D6	D5	D4	Analog Input Channel[1]
0	0	0	0	No channel selected
0	0	0	1	Convert on V_{IN0}
0	0	1	0	Convert on V_{IN1}
0	0	1	1	Sequence between V_{IN0} and V_{IN1}
0	1	0	0	Convert on V_{IN2}
0	1	0	1	Sequence between V_{IN0} and V_{IN2}
0	1	1	0	Sequence between V_{IN1} and V_{IN2}
0	1	1	1	Sequence among V_{IN0}, V_{IN1}, and V_{IN2}
1	0	0	0	Convert on V_{IN3}
1	0	0	1	Sequence between V_{IN0} and V_{IN3}
1	0	1	0	Sequence between V_{IN1} and V_{IN3}
1	0	1	1	Sequence among V_{IN0}, V_{IN1}, and V_{IN3}
1	1	0	0	Sequence between V_{IN2} and V_{IN3}
1	1	0	1	Sequence among V_{IN0}, V_{IN2}, and V_{IN3}
1	1	1	0	Sequence among V_{IN1}, V_{IN2}, and V_{IN3}
1	1	1	1	Sequence among V_{IN0}, V_{IN1}, V_{IN2}, and V_{IN3}

[1] The AD7991/AD7995/AD7999 converts on the selected channel in the sequence in ascending order, starting with the lowest channel in the sequence.

SAMPLE DELAY AND BIT TRIAL DELAY

It is recommended that no I²C bus activity occur while a conversion is taking place (see Figure 27 and the Placing the AD7991/AD7995/AD7999 into High Speed Mode section). However, if this is not always possible, then in order to maintain the performance of the ADC, Bits D0 and D1 in the configuration register are used to delay critical sample intervals and bit trials from occurring while there is activity on the I²C bus. This results in a quiet period for each bit decision. However, the sample delay protection may introduce excessive jitter, degrading the SNR for large signals above 300 Hz. For guaranteed ac performance, use of clock stretching is recommended.

When Bit D0 and Bit D1 are both 0, the bit trial and sample interval delay mechanism is implemented. The default setting of D0 and D1 is 0. To turn off both delay mechanisms, set D0 and D1 to 1.

CONVERSION RESULT REGISTER

The conversion result register is a 16-bit read-only register that stores the conversion result from the ADC in straight binary format. A 2-byte read is necessary to read data from this register. Table 12 shows the contents of the first byte to be read from AD7991/AD7995/AD7999, and Table 13 shows the contents of the second byte to be read.

Each AD7991/AD7995/AD7999 conversion result consists of two leading 0s, two channel identifier bits, and the 12-/10-/8-bit data result. For the AD7995, the two LSBs (D1 and D0) of the second read contain two trailing 0s. For the AD7999, the four LSBs (D3, D2, D1, and D0) of the second read contain four trailing 0s.

Table 12. Conversion Value Register (First Read)

D15	D14	D13	D12	D11	D10	D9	D8
Leading 0	Leading 0	CH_{ID1}	CH_{ID0}	MSB	B10	B9	B8

Table 13. Conversion Value Register (Second Read)

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3/0	B2/0	B1/0	B0/0

SERIAL INTERFACE

Control of the AD7991/AD7995/AD7999 is accomplished via the I²C-compatible serial bus. The AD7991/AD7995/AD7999 is connected to this bus as a slave device under the control of a master device, such as the processor.

SERIAL BUS ADDRESS

Like all I²C-compatible devices, the AD7991/AD7995/AD7999 has a 7-bit serial address. The devices are available in two versions, the AD7991-0/AD7995-0 and the AD7991-1/AD7995-1/AD7999-1. Each version has a different address (see Table 8), which allows up to two AD7991/AD7995 devices to be connected to a single serial bus. AD7999 has only one version.

The serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line SDA while the serial clock line, SCL, remains high. This indicates that an address/data stream follows.
2. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/$\overline{W}$ bit that determines the direction of the data transfer—that is, whether data is written to or read from the slave device.
3. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is set to 0, the master writes to the slave device. If the R/$\overline{W}$ bit is set to 1, the master reads from the slave device.
4. Data is sent over the serial bus in sequences of nine clock pulses—eight bits of data followed by an acknowledge bit from the receiver of data. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period because a low-to-high transition when the clock is high may be interpreted as a stop signal.
5. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device pulls the data line high during the low period before the ninth clock pulse. This is known as a no acknowledge. The master takes the data line low during the low period before the 10th clock pulse, and then high during the 10th clock pulse to assert a stop condition.
6. Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix reads and writes in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

WRITING TO THE AD7991/AD7995/AD7999

By default, each part operates in read-only mode and all four channels are selected as enabled in the configuration register. To write to the AD7991/AD7995/AD7999 configuration register, the user must first address the device.

The configuration register is an 8-bit register; therefore, only one byte of data can be written to this register. However, writing a single byte of data to this register consists of writing the serial bus write address, followed by the data byte written (see Figure 24).

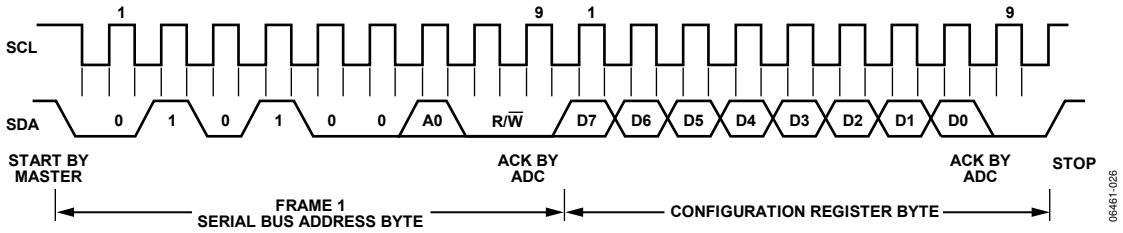

Figure 24. Writing to the AD7991/AD7995/AD7999 Configuration Register

READING FROM THE AD7991/AD7995/AD7999

Reading data from the conversion result register is a 2-byte operation, as shown in Figure 25. Therefore, a read operation always involves two bytes.

After the AD7991/AD7995/AD7999 have received a read address, any number of reads can be performed from the conversion result register.

Following a start condition, the master writes the 7-bit address of the AD7991/AD7995/AD7999 and then sets R/$\overline{W}$ to 1. The AD7991/AD7995/AD7999 acknowledge this by pulling the SDA line low. They then output the conversion result over the I^2C bus, preceded by four status bits. The status bits are two leading 0s followed by the channel identifier bits. For the AD7995 there are two trailing 0s, and for the AD7999 there are four trailing 0s.

After the master has addressed the AD7991/AD7995/AD7999, the part begins to power up on the ninth SCLK rising edge. At the same time, the acquisition phase begins. When approximately 0.6 µs have elapsed, the acquisition phase ends. The input is sampled and a conversion begins. This is done in parallel to the read operation and should not affect the read operation. The master reads back two bytes of data. On the ninth SCLK rising edge of the second byte, if the master sends an ACK, it keeps reading conversion results and the AD7991/AD7995/AD7999 powers up and performs a second conversion. If the master sends a NO ACK, the AD7991/AD7995/AD7999 does not power up on the ninth SCLK rising edge of the second byte. If a further conversion is required, the part converts on the next channel, as selected in the configuration register. See Table 11 for information about the channel selection.

If the master sends a NO ACK on the ninth SCLK rising edge of the second byte, the conversion is finished and no further conversion is preformed.

To put the part into full shutdown mode, the user should issue a stop condition to the AD7991/AD7995/AD7999. If the AD7991/AD7995/AD7999 is not put into full shutdown mode, it will draw a few tens of microamperes from the supply.

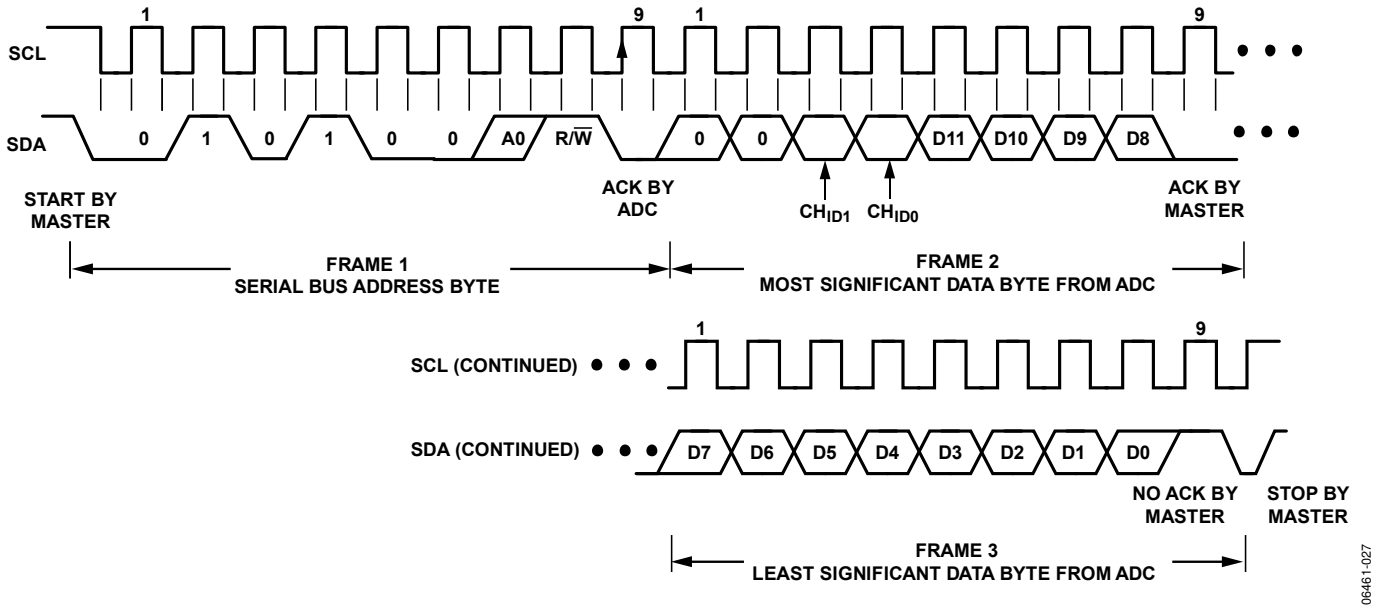

Figure 25. Reading Two Bytes of Data from the AD7991Conversion Result Register

PLACING THE AD7991/AD7995/AD7999 INTO HIGH SPEED MODE

High speed mode communication commences after the master addresses all devices connected to the bus with the master code, 00001XXX, to indicate that a high speed mode transfer is to begin. No device connected to the bus is allowed to acknowledge the high speed master code; therefore, the code is followed by a NO ACK (see Figure 26). The master must then issue a repeated start, followed by the device address and an R/$\overline{W}$ bit. The selected device then acknowledges its address.

All devices continue to operate in high speed mode until the master issues a stop condition. When the stop condition is issued, the devices return to fast mode.

To guarantee performance above f_{SCL} = 1.7 MHz, the user must perform clock stretching—that is, the clock must be held high—for 2 µs after the ninth clock rising edge (see Figure 27). Therefore, the clock must be held high for 2 µs after the device starts to power up (see the Reading from the AD7991/AD7995/AD7999 section).

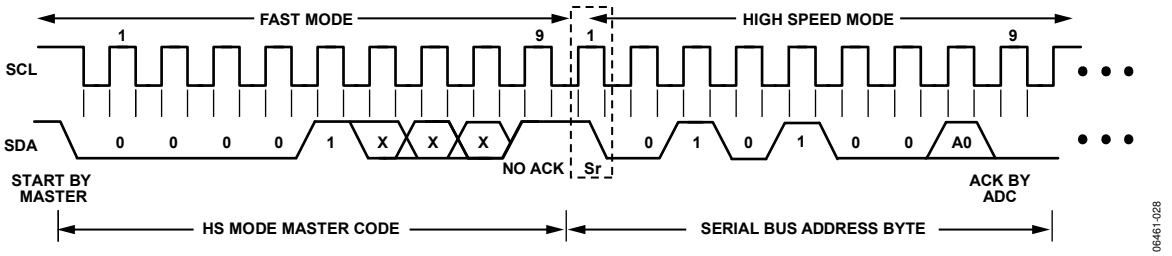

Figure 26. Placing the Part into High Speed Mode

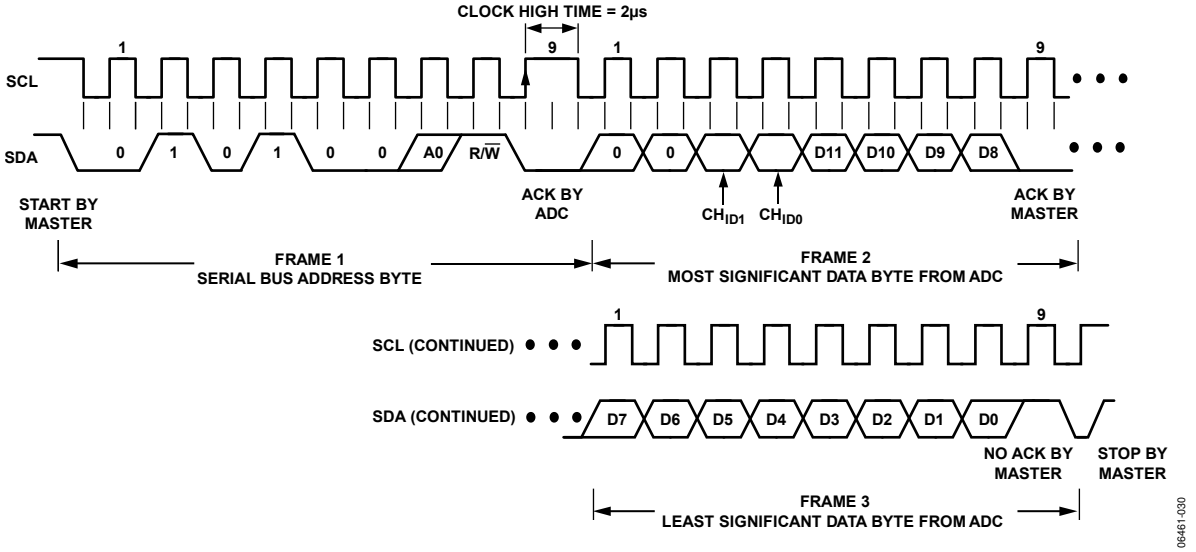

Figure 27. Reading Two Bytes of Data from the Conversion Result Register in High Speed Mode for AD7991