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600 MHz, 32 × 16 Buffered Analog Crosspoint Switch

AD8104/AD8105

FEATURES

High channel count, 32 × 16 high speed, nonblocking
  switch array
Differential or single-ended operation
Differential G = +1 (AD8104) or G = +2 (AD8105)
Pin compatible with AD8117/AD8118, 32 × 32 switch arrays
Flexible power supplies
  Single +5 V supply, or dual ±2.5 V supplies
Serial or parallel programming of switch array
High impedance output disable allows connection of
  multiple devices with minimal loading on output bus
Excellent video performance
  >50 MHz 0.1 dB gain flatness
  0.05% differential gain error (R_L = 150 Ω)
  0.05° phase error (R_L = 150 Ω)
Excellent ac performance
  Bandwidth: 600 MHz
  Slew rate: 1800 V/μs
  Settling time: 2.5 ns to 1%
Low power of 1.7 W
Low all hostile crosstalk
  < −70 dB at 5 MHz
  < −40 dB at 600 MHz
Reset pin allows disabling of all outputs (connected through
  a capacitor to ground provides power-on reset capability)
304-ball BGA package (31 mm × 31 mm)

APPLICATIONS

Routing of high speed signals including
  RGB and component video routing
  KVM
  Compressed video (MPEG, wavelet)
  Data communications

GENERAL DESCRIPTION

The AD8104/AD8105 are high speed, 32 × 16 analog crosspoint switch matrices. They offer 600 MHz bandwidth and slew rate of 1800 V/μs for high resolution computer graphics (RGB) signal switching. With less than −70 dB of crosstalk and −90 dB isolation (at 5 MHz), the AD8104/AD8105 are useful in many high speed applications. The 0.1 dB flatness, which is greater than 50 MHz, makes the AD8104/AD8105 ideal for composite video switching.

The AD8104/AD8105 include 16 independent output buffers that can be placed into a high impedance state for paralleling crosspoint outputs so that off-channels present minimal loading to an output bus. The AD8104 has a differential gain of +1,
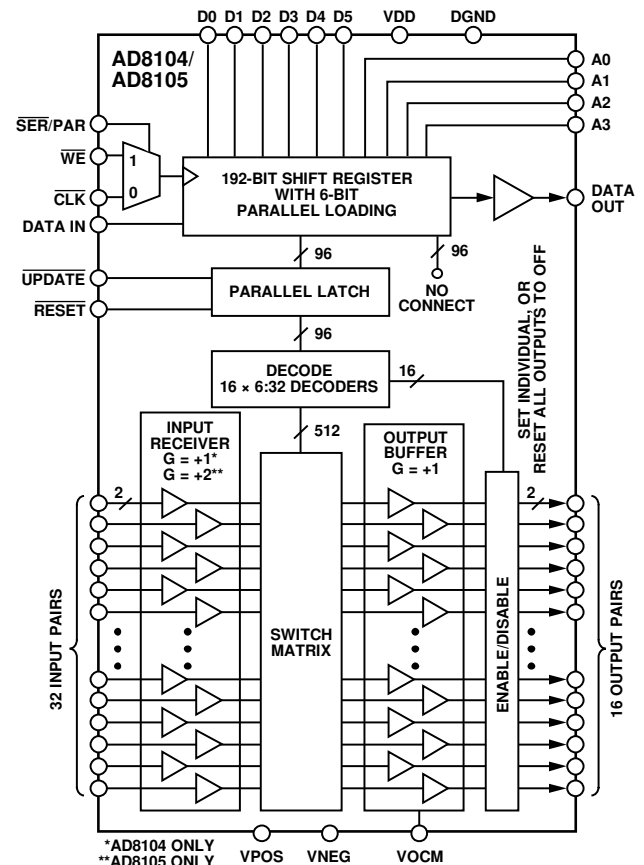
while the AD8105 has a differential gain of +2 for ease of use in back-terminated load applications. They operate as fully differential devices or can be configured for single-ended operation. Either a single +5 V supply or dual ±2.5 V supplies can be used, while consuming only 340 mA of idle current with all outputs enabled. The channel switching is performed via a double-buffered, serial digital control (which can accommodate daisy-chaining of several devices), or via a parallel control, allowing updating of an individual output without reprogramming the entire array.

The AD8104/AD8105 are packaged in a 304-ball BGA package and are available over the extended industrial temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

Figure 1.

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REVISION HISTORY

SPECIFICATIONS

$V_S = \pm 2.5$ V at $T_A = 25°C$, $R_{L, diff} = 200\ \Omega$, $V_{OCM} = 0$ V, differential I/O mode, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	AD8104/AD8105			Unit
		Min	Typ	Max	
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	200 mV p-p, typical channel		600		MHz
	2 V p-p, typical channel		420/525		MHz
Gain Flatness	0.1 dB, 200 mV p-p		100/50		MHz
	0.1 dB, 2 V p-p		70/50		MHz
Propagation Delay	2 V p-p		1.3		ns
Settling Time	1%, 2 V step		2.5		ns
Slew Rate	2 V step, peak		1800		V/μs
	2 V step, 10% to 90%		1500		V/μs
NOISE/DISTORTION PERFORMANCE					
Differential Gain Error	NTSC or PAL, $R_L = 150\ \Omega$		0.05		%
Differential Phase Error	NTSC or PAL, $R_L = 150\ \Omega$		0.05		Degrees
Crosstalk, All Hostile	f = 5 MHz		−80/−70		dB
	f = 10 MHz		−72/−68		dB
	f = 100 MHz		−48/−50		dB
	f = 600 MHz		−40/−50		dB
Off Isolation, Input to Output	f = 5 MHz, one channel		−92		dB
Input Voltage Noise	0.1 MHz to 50 MHz		45/53		nV/√Hz
DC PERFORMANCE					
Voltage Gain	Differential		+1/+2		V/V
Gain Error			±1		%
	No load		±1	±3	%
Gain Matching	Channel-to-channel		±1		%
Differential Offset			±5	±25	mV
Common-Mode Offset			±25	±90	mV
OUTPUT CHARACTERISTICS					
Output Impedance	DC, enabled		0.1		Ω
	Disabled, differential		30		kΩ
Output Disable Capacitance	Disabled		4		pF
Output Leakage Current	Disabled		1		μA
Output Voltage Range	No load	2.8	3.8		V p-p
V_{OCM} Input Range	$V_{OUT, diff} = 2$ V p-p	−0.5		+0.8	V
	$V_{OUT, diff} = 2.8$ V p-p	−0.25		+0.6	V
Output Swing Limit	Single-ended output	−1.3		+1.3	V
Output Current	Maximum operating signal		30		mA
INPUT CHARACTERISTICS					
Input Voltage Range	Common mode, $V_{IN, diff} = 2$ V p-p	−2		+2	V
	Differential		2/1		V
Common-Mode Rejection Ratio	f = 10 MHz		48		dB
Input Capacitance	Any switch configuration		2		pF
Input Resistance	Differential		5		kΩ
Input Offset Current			1		μA
V_{OCM} Input Bias Current			64		μA
V_{OCM} Input Impedance			4		kΩ

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
			AD8104/AD8105		
SWITCHING CHARACTERISTICS					
Enable On Time	50% update to 1% settling		100		ns
Switching Time, 2 V Step	50% update to 1% settling		100		ns
Switching Transient (Glitch)	Differential		40		mV p-p
POWER SUPPLIES					
Supply Current	VPOS, outputs enabled, no load		340	420	mA
	VPOS, outputs disabled		210	240	mA
	VNEG, outputs enabled, no load		340	420	mA
	VNEG, outputs disabled		210	240	mA
	VDD, outputs enabled, no load			1.2	mA
Supply Voltage Range			4.5 to 5.5		V
PSRR	VNEG, VPOS, f = 1 MHz		85		dB
	VOCM, f = 1 MHz		75		dB
OPERATING TEMPERATURE RANGE					
Temperature Range	Operating (still air)		−40 to +85		°C
θ_{JA}	Operating (still air)		14		°C/W
θ_{JC}	Operating (still air)		1		°C/W

TIMING CHARACTERISTICS (SERIAL MODE)

Specifications subject to change without notice.

Table 2.

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Serial Data Setup Time	t_1	40			ns
$\overline{CLK}$ Pulse Width	t_2	50			ns
Serial Data Hold Time	t_3	50			ns
$\overline{CLK}$ Pulse Separation	t_4	150			ns
$\overline{CLK}$ to $\overline{UPDATE}$ Delay	t_5	10			ns
$\overline{UPDATE}$ Pulse Width	t_6	90			ns
$\overline{CLK}$ to DATA OUT Valid	t_7	120			ns
Propagation Delay, $\overline{UPDATE}$ to Switch On or Off			100		ns
$\overline{RESET}$ Pulse Width		60			ns
$\overline{RESET}$ Time			200		ns
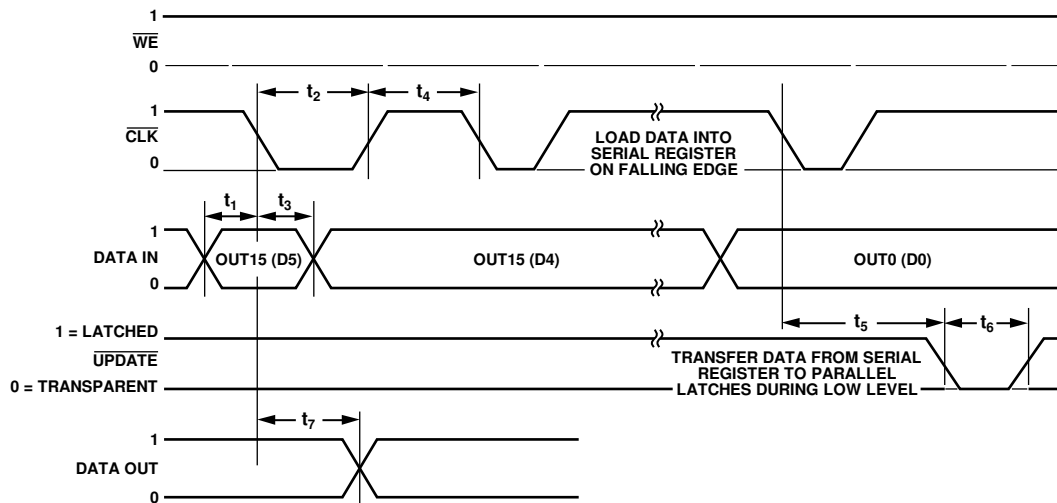
Figure 2. Timing Diagram, Serial Mode

Table 3. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{RESET}$, $\overline{SER/PAR}$, $\overline{CLK}$, DATA IN, $\overline{UPDATE}$	$\overline{RESET}$, $\overline{SER/PAR}$, $\overline{CLK}$, DATA IN, $\overline{UPDATE}$	DATA OUT	DATA OUT	$\overline{RESET}$[1], $\overline{SER/PAR}$, $\overline{CLK}$, DATA IN, $\overline{UPDATE}$	$\overline{RESET}$[1], $\overline{SER/PAR}$, $\overline{CLK}$, DATA IN, $\overline{UPDATE}$	DATA OUT	DATA OUT
2.0 V min	0.6 V max	VDD − 0.3 V min	DGND + 0.5 V max	1 μA max	−1 μA min	−1 mA max	1 mA min

[1] See Figure 15.

TIMING CHARACTERISTICS (PARALLEL MODE)

Specifications subject to change without notice.

Table 4.

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Parallel Data Setup Time	t_1	80			ns
$\overline{WE}$ Pulse Width	t_2	110			ns
Parallel Data Hold Time	t_3	150			ns
$\overline{WE}$ Pulse Separation	t_4	90			ns
$\overline{WE}$ to $\overline{UPDATE}$ Delay	t_5	10			ns
$\overline{UPDATE}$ Pulse Width	t_6	90			ns
Propagation Delay, $\overline{UPDATE}$ to Switch On or Off			100		ns
$\overline{RESET}$ Pulse Width		60			ns
$\overline{RESET}$ Time			200		ns
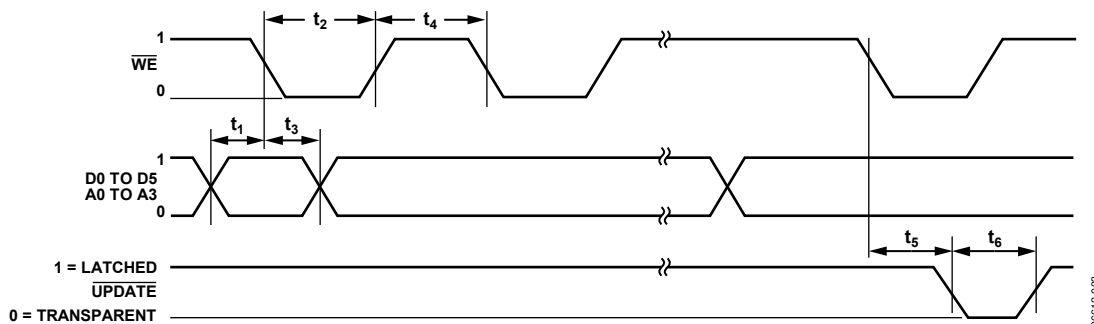
Figure 3. Timing Diagram, Parallel Mode

Table 5. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{RESET}$, $\overline{SER/PAR}$, $\overline{WE}$, D0, D1, D2, D3, D4, D5, A0, A1, A2, A3, $\overline{UPDATE}$	$\overline{RESET}$, $\overline{SER/PAR}$, $\overline{WE}$, D0, D1, D2, D3, D4, D5, A0, A1, A2, A3, $\overline{UPDATE}$	DATA OUT	DATA OUT	$\overline{RESET}$[1], $\overline{SER/PAR}$, $\overline{WE}$, D0, D1, D2, D3, D4, D5, A0, A1, A2, A3, $\overline{UPDATE}$	$\overline{RESET}$[1], $\overline{SER/PAR}$, $\overline{WE}$, D0, D1, D2, D3, D4, D5, A0, A1, A2, A3, $\overline{UPDATE}$	DATA OUT	DATA OUT
2.0 V min	0.6 V max	Disabled	Disabled	1 µA max	−1 µA min	Disabled	Disabled

[1] See Figure 15.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Supply Voltage (VPOS – VNEG)	6 V
Digital Supply Voltage (VDD – DGND)	6 V
Ground Potential Difference (VNEG – DGND)	+0.5 V to –2.5 V
Maximum Potential Difference (VDD – VNEG)	8 V
Common-Mode Analog Input Voltage	VNEG to VPOS
Differential Analog Input Voltage	±2 V
Digital Input Voltage	VDD
Output Voltage (Disabled Analog Output)	(VPOS – 1 V) to (VNEG + 1 V)
Output Short-Circuit Duration	Momentary
Output Short-Circuit Current	80 mA
Storage Temperature Range	–65°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	θ_{JB}	ψ_{JT}	ψ_{JB}	Unit
304-Ball BGA	14	1	6.5	0.6	5.7	°C/W

POWER DISSIPATION

The AD8104/AD8105 are operated with ±2.5 V or +5 V supplies and can drive loads down to 100 Ω, resulting in a large range of possible power dissipations. For this reason, extra care must be taken derating the operating conditions based on ambient temperature.

Packaged in a 304-ball BGA, the AD8104/AD8105 junction-to-ambient thermal impedance (θ_{JA}) is 14°C/W. For long-term reliability, the maximum allowed junction temperature of the die should not exceed 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. The following curve shows the range of allowed internal die power dissipations that meet these conditions over the –40°C to +85°C ambient temperature range. When using Table 6, do not include external load power in the maximum power calculation, but do include load current dropped on the die output transistors.
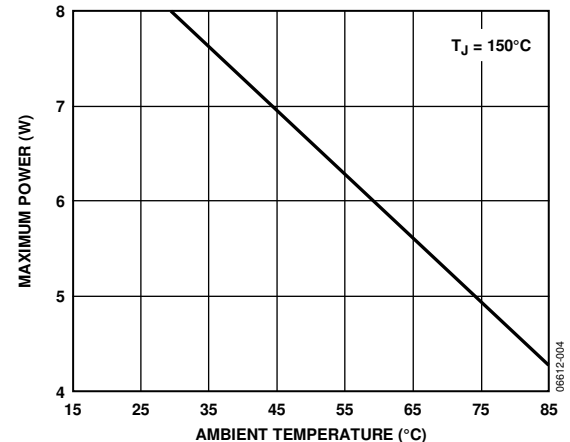

Figure 4. Maximum Die Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 5. 304-Ball BGA Pin Configuration (Bottom View)

AD8104/AD8105

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	VPOS	VPOS	VPOS	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VPOS	VPOS	VPOS	VPOS	A
B	VPOS	VPOS	VPOS	VPOS	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VPOS	VPOS	VPOS	B
C	VPOS	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VPOS	C
D	VPOS	IP0	VPOS	VNEG	VOCM	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VOCM	VNEG	VPOS	VPOS	IN16	D
E	IP1	IN0	VNEG	VOCM																VOCM	VNEG	IN17	IP16	E
F	IN1	IP2	VNEG	VDD																VDD	VNEG	IP17	IN18	F
G	IP3	IN2	VNEG	DGND																DGND	VNEG	IN19	IP18	G
H	IN3	IP4	VNEG	DATA OUT																RESET	VNEG	IP19	IN20	H
J	IP5	IN4	VNEG	CLK																UPDATE	VNEG	IN21	IP20	J
K	IN5	IP6	VNEG	DATA IN																WE	VNEG	IP21	IN22	K
L	IP7	IN6	VPOS	SER/PAR																D5	VPOS	IN23	IP22	L
M	IN7	IP8	VPOS	DGND																D4	VPOS	IP23	IN24	M
N	IP9	IN8	VPOS	A3																D3	VPOS	IN25	IP24	N
P	IN9	IP10	VNEG	A2																D2	VNEG	IP25	IN26	P
R	IP11	IN10	VNEG	A1																D1	VNEG	IN27	IP26	R
T	IN11	IP12	VNEG	A0																D0	VNEG	IP27	IN28	T
U	IP13	IN12	VNEG	VDD																VDD	VNEG	IN29	IP28	U
V	IN13	IP14	VNEG	DGND																DGND	VNEG	IP29	IN30	V
W	IP15	IN14	VNEG	VOCM																VOCM	VNEG	IN31	IP30	W
Y	IN15	VPOS	VPOS	VNEG	VOCM	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VOCM	VNEG	VPOS	IP31	VPOS	Y
AA	VPOS	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VNEG	VNEG	VNEG	VNEG	VNEG	VPOS	VPOS	VPOS	VPOS	VPOS	AA
AB	VPOS	VPOS	VPOS	OP0	ON0	OP2	ON2	OP4	ON4	OP6	ON6	OP8	ON8	OP10	ON10	OP12	ON12	OP14	ON14	VPOS	VPOS	VPOS	VPOS	AB
AC	VPOS	VPOS	VPOS	VPOS	OP1	ON1	OP3	ON3	OP5	ON5	OP7	ON7	OP9	ON9	OP11	ON11	OP13	ON13	OP15	ON15	VPOS	VPOS	VPOS	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

AD8104/AD8105
TOP VIEW
(Not to Scale)

06612-006

Figure 6. 304-Ball BGA Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description	Pin No.	Mnemonic	Description
A1	VPOS	Analog Positive Power Supply.	A17	NC	No Connect.
A2	VPOS	Analog Positive Power Supply.	A18	NC	No Connect.
A3	VPOS	Analog Positive Power Supply.	A19	NC	No Connect.
A4	NC	No Connect.	A20	VPOS	Analog Positive Power Supply.
A5	NC	No Connect.	A21	VPOS	Analog Positive Power Supply.
A6	NC	No Connect.	A22	VPOS	Analog Positive Power Supply.
A7	NC	No Connect.	A23	VPOS	Analog Positive Power Supply.
A8	NC	No Connect.	B1	VPOS	Analog Positive Power Supply.
A9	NC	No Connect.	B2	VPOS	Analog Positive Power Supply.
A10	NC	No Connect.	B3	VPOS	Analog Positive Power Supply.
A11	NC	No Connect.	B4	VPOS	Analog Positive Power Supply.
A12	NC	No Connect.	B5	NC	No Connect.
A13	NC	No Connect.	B6	NC	No Connect.
A14	NC	No Connect.	B7	NC	No Connect.
A15	NC	No Connect.	B8	NC	No Connect.
A16	NC	No Connect.	B9	NC	No Connect.

Pin No.	Mnemonic	Description
B10	NC	No Connect.
B11	NC	No Connect.
B12	NC	No Connect.
B13	NC	No Connect.
B14	NC	No Connect.
B15	NC	No Connect.
B16	NC	No Connect.
B17	NC	No Connect.
B18	NC	No Connect.
B19	NC	No Connect.
B20	NC	No Connect.
B21	VPOS	Analog Positive Power Supply.
B22	VPOS	Analog Positive Power Supply.
B23	VPOS	Analog Positive Power Supply.
C1	VPOS	Analog Positive Power Supply.
C2	VPOS	Analog Positive Power Supply.
C3	VPOS	Analog Positive Power Supply.
C4	VPOS	Analog Positive Power Supply.
C5	VNEG	Analog Negative Power Supply.
C6	VNEG	Analog Negative Power Supply.
C7	VNEG	Analog Negative Power Supply.
C8	VNEG	Analog Negative Power Supply.
C9	VNEG	Analog Negative Power Supply.
C10	VNEG	Analog Negative Power Supply.
C11	VPOS	Analog Positive Power Supply.
C12	VPOS	Analog Positive Power Supply.
C13	VPOS	Analog Positive Power Supply.
C14	VNEG	Analog Negative Power Supply.
C15	VNEG	Analog Negative Power Supply.
C16	VNEG	Analog Negative Power Supply.
C17	VNEG	Analog Negative Power Supply.
C18	VNEG	Analog Negative Power Supply.
C19	VNEG	Analog Negative Power Supply.
C20	VPOS	Analog Positive Power Supply.
C21	VPOS	Analog Positive Power Supply.
C22	VPOS	Analog Positive Power Supply.
C23	VPOS	Analog Positive Power Supply.
D1	VPOS	Analog Positive Power Supply.
D2	IP0	Input Number 0, Positive Phase.
D3	VPOS	Analog Positive Power Supply.
D4	VNEG	Analog Negative Power Supply.
D5	VOCM	Output Common-Mode Reference Supply.
D6	VNEG	Analog Negative Power Supply.
D7	VNEG	Analog Negative Power Supply.
D8	VNEG	Analog Negative Power Supply.
D9	VNEG	Analog Negative Power Supply.
D10	VNEG	Analog Negative Power Supply.
D11	VPOS	Analog Positive Power Supply.
D12	VPOS	Analog Positive Power Supply.
D13	VPOS	Analog Positive Power Supply.
D14	VNEG	Analog Negative Power Supply.
D15	VNEG	Analog Negative Power Supply.

Pin No.	Mnemonic	Description
D16	VNEG	Analog Negative Power Supply.
D17	VNEG	Analog Negative Power Supply.
D18	VNEG	Analog Negative Power Supply.
D19	VOCM	Output Common-Mode Reference Supply.
D20	VNEG	Analog Negative Power Supply.
D21	VPOS	Analog Positive Power Supply.
D22	VPOS	Analog Positive Power Supply.
D23	IN16	Input Number 16, Negative Phase.
E1	IP1	Input Number 1, Positive Phase.
E2	IN0	Input Number 0, Negative Phase.
E3	VNEG	Analog Negative Power Supply.
E4	VOCM	Output Common-Mode Reference Supply.
E20	VOCM	Output Common-Mode Reference Supply.
E21	VNEG	Analog Negative Power Supply.
E22	IN17	Input Number 17, Negative Phase.
E23	IP16	Input Number 16, Positive Phase.
F1	IN1	Input Number 1, Negative Phase.
F2	IP2	Input Number 2, Positive Phase.
F3	VNEG	Analog Negative Power Supply.
F4	VDD	Logic Positive Power Supply.
F20	VDD	Logic Positive Power Supply.
F21	VNEG	Analog Negative Power Supply.
F22	IP17	Input Number 17, Positive Phase.
F23	IN18	Input Number 18, Negative Phase.
G1	IP3	Input Number 3, Positive Phase.
G2	IN2	Input Number 2, Negative Phase.
G3	VNEG	Analog Negative Power Supply.
G4	DGND	Logic Negative Power Supply.
G20	DGND	Logic Negative Power Supply.
G21	VNEG	Analog Negative Power Supply.
G22	IN19	Input Number 19, Negative Phase.
G23	IP18	Input Number 18, Positive Phase.
H1	IN3	Input Number 3, Negative Phase.
H2	IP4	Input Number 4, Positive Phase.
H3	VNEG	Analog Negative Power Supply.
H4	DATA OUT	Control Pin: Serial Data Out.
H20	$\overline{\text{RESET}}$	Control Pin: Second Rank Data Reset.
H21	VNEG	Analog Negative Power Supply.
H22	IP19	Input Number 19, Positive Phase.
H23	IN20	Input Number 20, Negative Phase.
J1	IP5	Input Number 5, Positive Phase.
J2	IN4	Input Number 4, Negative Phase.
J3	VNEG	Analog Negative Power Supply.
J4	$\overline{\text{CLK}}$	Control Pin: Serial Data Clock.
J20	$\overline{\text{UPDATE}}$	Control Pin: Second Rank Write Strobe.
J21	VNEG	Analog Negative Power Supply.
J22	IN21	Input Number 21, Negative Phase.
J23	IP20	Input Number 20, Positive Phase.
K1	IN5	Input Number 5, Negative Phase.

Pin No.	Mnemonic	Description
K2	IP6	Input Number 6, Positive Phase.
K3	VNEG	Analog Negative Power Supply.
K4	DATA IN	Control Pin: Serial Data In.
K20	$\overline{WE}$	Control Pin: First Rank Write Strobe.
K21	VNEG	Analog Negative Power Supply.
K22	IP21	Input Number 21, Positive Phase.
K23	IN22	Input Number 22, Negative Phase.
L1	IP7	Input Number 7, Positive Phase.
L2	IN6	Input Number 6, Negative Phase.
L3	VPOS	Analog Positive Power Supply.
L4	$\overline{SER}/PAR$	Control Pin: Serial/Parallel Mode Select.
L20	D5	Control Pin: Input Address Bit 5.
L21	VPOS	Analog Positive Power Supply.
L22	IN23	Input Number 23, Negative Phase.
L23	IP22	Input Number 22, Positive Phase.
M1	IN7	Input Number 7, Negative Phase.
M2	IP8	Input Number 8, Positive Phase.
M3	VPOS	Analog Positive Power Supply.
M4	DGND	Logic Negative Power Supply
M20	D4	Control Pin: Input Address Bit 4.
M21	VPOS	Analog Positive Power Supply.
M22	IP23	Input Number 23, Positive Phase.
M23	IN24	Input Number 24, Negative Phase.
N1	IP9	Input Number 9, Positive Phase.
N2	IN8	Input Number 8, Negative Phase.
N3	VPOS	Analog Positive Power Supply.
N4	A3	Control Pin: Output Address Bit 3.
N20	D3	Control Pin: Input Address Bit 3.
N21	VPOS	Analog Positive Power Supply.
N22	IN25	Input Number 25, Negative Phase.
N23	IP24	Input Number 24, Positive Phase.
P1	IN9	Input Number 9, Negative Phase.
P2	IP10	Input Number 10, Positive Phase.
P3	VNEG	Analog Negative Power Supply.
P4	A2	Control Pin: Output Address Bit 2.
P20	D2	Control Pin: Input Address Bit 2.
P21	VNEG	Analog Negative Power Supply.
P22	IP25	Input Number 25, Positive Phase.
P23	IN26	Input Number 26, Negative Phase.
R1	IP11	Input Number 11, Positive Phase.
R2	IN10	Input Number 10, Negative Phase.
R3	VNEG	Analog Negative Power Supply.
R4	A1	Control Pin: Output Address Bit 1.
R20	D1	Control Pin: Input Address Bit 1.
R21	VNEG	Analog Negative Power Supply.
R22	IN27	Input Number 27, Negative Phase.
R23	IP26	Input Number 26, Positive Phase.
T1	IN11	Input Number 11, Negative Phase.
T2	IP12	Input Number 12, Positive Phase.
T3	VNEG	Analog Negative Power Supply.
T4	A0	Control Pin: Output Address Bit 0.
T20	D0	Control Pin: Input Address Bit 0.

Pin No.	Mnemonic	Description
T21	VNEG	Analog Negative Power Supply.
T22	IP27	Input Number 27, Positive Phase.
T23	IN28	Input Number 28, Negative Phase.
U1	IP13	Input Number 13, Positive Phase.
U2	IN12	Input Number 12, Negative Phase.
U3	VNEG	Analog Negative Power Supply.
U4	VDD	Logic Positive Power Supply.
U20	VDD	Logic Positive Power Supply.
U21	VNEG	Analog Negative Power Supply.
U22	IN29	Input Number 29, Negative Phase.
U23	IP28	Input Number 28, Positive Phase.
V1	IN13	Input Number 13, Negative Phase.
V2	IP14	Input Number 14, Positive Phase.
V3	VNEG	Analog Negative Power Supply.
V4	DGND	Logic Negative Power Supply.
V20	DGND	Logic Negative Power Supply.
V21	VNEG	Analog Negative Power Supply.
V22	IP29	Input Number 29, Positive Phase.
V23	IN30	Input Number 30, Negative Phase.
W1	IP15	Input Number 15, Positive Phase.
W2	IN14	Input Number 14, Negative Phase.
W3	VNEG	Analog Negative Power Supply.
W4	VOCM	Output Common-Mode Reference Supply.
W20	VOCM	Output Common-Mode Reference Supply.
W21	VNEG	Analog Negative Power Supply.
W22	IN31	Input Number 31, Negative Phase.
W23	IP30	Input Number 30, Positive Phase.
Y1	IN15	Input Number 15, Negative Phase.
Y2	VPOS	Analog Positive Power Supply.
Y3	VPOS	Analog Positive Power Supply.
Y4	VNEG	Analog Negative Power Supply.
Y5	VOCM	Output Common-Mode Reference Supply.
Y6	VNEG	Analog Negative Power Supply.
Y7	VNEG	Analog Negative Power Supply.
Y8	VNEG	Analog Negative Power Supply.
Y9	VNEG	Analog Negative Power Supply.
Y10	VNEG	Analog Negative Power Supply.
Y11	VPOS	Analog Positive Power Supply.
Y12	VPOS	Analog Positive Power Supply.
Y13	VPOS	Analog Positive Power Supply.
Y14	VNEG	Analog Negative Power Supply.
Y15	VNEG	Analog Negative Power Supply.
Y16	VNEG	Analog Negative Power Supply.
Y17	VNEG	Analog Negative Power Supply.
Y18	VNEG	Analog Negative Power Supply.
Y19	VOCM	Output Common-Mode Reference Supply.
Y20	VNEG	Analog Negative Power Supply.
Y21	VPOS	Analog Positive Power Supply.
Y22	IP31	Input Number 31, Positive Phase.

Pin No.	Mnemonic	Description	Pin No.	Mnemonic	Description
Y23	VPOS	Analog Positive Power Supply.	AB14	OP10	Output Number 10, Positive Phase.
AA1	VPOS	Analog Positive Power Supply.	AB15	ON10	Output Number 10, Negative Phase.
AA2	VPOS	Analog Positive Power Supply.	AB16	OP12	Output Number 12, Positive Phase.
AA3	VPOS	Analog Positive Power Supply.	AB17	ON12	Output Number 12, Negative Phase.
AA4	VPOS	Analog Positive Power Supply.	AB18	OP14	Output Number 14, Positive Phase.
AA5	VNEG	Analog Negative Power Supply.	AB19	ON14	Output Number 14, Negative Phase.
AA6	VNEG	Analog Negative Power Supply.	AB20	VPOS	Analog Positive Power Supply.
AA7	VNEG	Analog Negative Power Supply.	AB21	VPOS	Analog Positive Power Supply.
AA8	VNEG	Analog Negative Power Supply.	AB22	VPOS	Analog Positive Power Supply.
AA9	VNEG	Analog Negative Power Supply.	AB23	VPOS	Analog Positive Power Supply.
AA10	VNEG	Analog Negative Power Supply.	AC1	VPOS	Analog Positive Power Supply.
AA11	VPOS	Analog Positive Power Supply.	AC2	VPOS	Analog Positive Power Supply.
AA12	VPOS	Analog Positive Power Supply.	AC3	VPOS	Analog Positive Power Supply.
AA13	VPOS	Analog Positive Power Supply.	AC4	VPOS	Analog Positive Power Supply.
AA14	VNEG	Analog Negative Power Supply.	AC5	OP1	Output Number 1, Positive Phase.
AA15	VNEG	Analog Negative Power Supply.	AC6	ON1	Output Number 1, Negative Phase.
AA16	VNEG	Analog Negative Power Supply.	AC7	OP3	Output Number 3, Positive Phase.
AA17	VNEG	Analog Negative Power Supply.	AC8	ON3	Output Number 3, Negative Phase.
AA18	VNEG	Analog Negative Power Supply.	AC9	OP5	Output Number 5, Positive Phase.
AA19	VNEG	Analog Negative Power Supply.	AC10	ON5	Output Number 5, Negative Phase.
AA20	VPOS	Analog Positive Power Supply.	AC11	OP7	Output Number 7, Positive Phase.
AA21	VPOS	Analog Positive Power Supply.	AC12	ON7	Output Number 7, Negative Phase.
AA22	VPOS	Analog Positive Power Supply.	AC13	OP9	Output Number 9, Positive Phase.
AA23	VPOS	Analog Positive Power Supply.	AC14	ON9	Output Number 9, Negative Phase.
AB1	VPOS	Analog Positive Power Supply.	AC15	OP11	Output Number 11, Positive Phase.
AB2	VPOS	Analog Positive Power Supply.	AC16	ON11	Output Number 11, Negative Phase.
AB3	VPOS	Analog Positive Power Supply.	AC17	OP13	Output Number 13, Positive Phase.
AB4	OP0	Output Number 0, Positive Phase.	AC18	ON13	Output Number 13, Negative Phase.
AB5	ON0	Output Number 0, Negative Phase.	AC19	OP15	Output Number 15, Positive Phase.
AB6	OP2	Output Number 2, Positive Phase.	AC20	ON15	Output Number 15, Negative Phase.
AB7	ON2	Output Number 2, Negative Phase.	AC21	VPOS	Analog Positive Power Supply.
AB8	OP4	Output Number 4, Positive Phase.	AC22	VPOS	Analog Positive Power Supply.
AB9	ON4	Output Number 4, Negative Phase.	AC23	VPOS	Analog Positive Power Supply.
AB10	OP6	Output Number 6, Positive Phase.			
AB11	ON6	Output Number 6, Negative Phase.			
AB12	OP8	Output Number 8, Positive Phase.			
AB13	ON8	Output Number 8, Negative Phase.			

TRUTH TABLE AND LOGIC DIAGRAM

Table 9. Operation Truth Table

$\overline{WE}$	$\overline{UPDATE}$	$\overline{CLK}$	Data Input	Data Output	$\overline{RESET}$	$\overline{SER}/PAR$	Operation/Comment
X	X	X	X	X	0	X	Asynchronous reset. All outputs are disabled. Remainder of logic in 192-bit shift register is unchanged.
1	X	⌐	$Data_i$ [1]	$Data_{i-192}$	1	0	Serial mode. The data on the serial DATA IN line is loaded into the serial register. The first bit clocked into the serial register appears at DATA OUT 192 clock cycles later.
0	X	X	D0…D5 [2] A0…A3 [3]	Not applicable in parallel mode	1	1	Parallel mode. The data on parallel lines D0 to D5 are loaded into the shift register location addressed by A0 to A3.
1	0	X	X	Not applicable in parallel mode	1	X	Switch matrix update. Data in the 192-bit shift register transfers into the parallel latches that control the switch array.
1	X	X	X	X	1	1	No change in logic.

[1] $Data_i$: serial data.
[2] D0…D5: data bits.
[3] A0…A3: address bits.
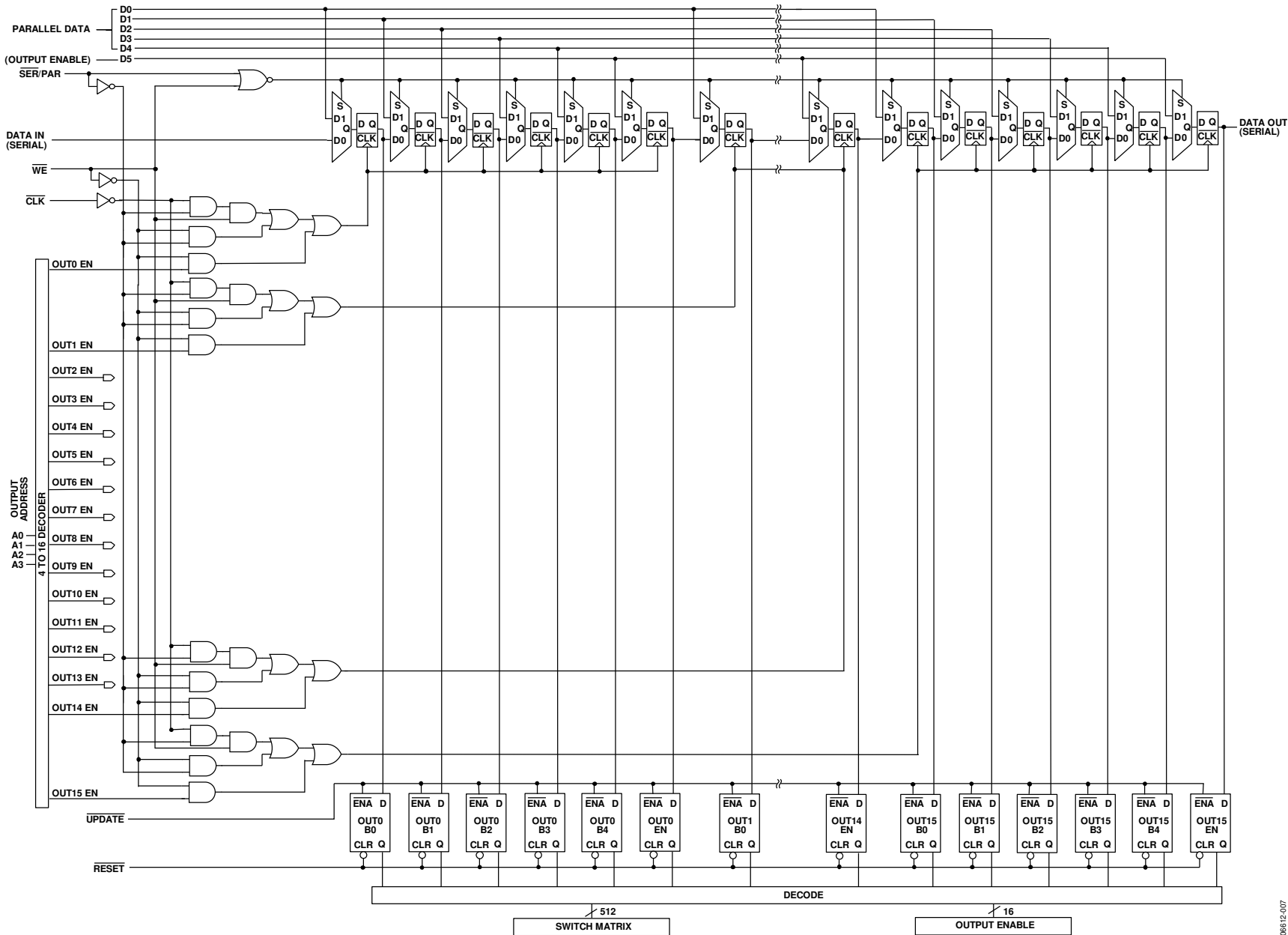
Figure 7. Logic Diagram

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I/O SCHEMATICS
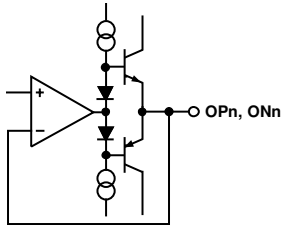
Figure 8. *AD8104*/*AD8105* Enabled Output
(see also ESD Protection Map, Figure 18)
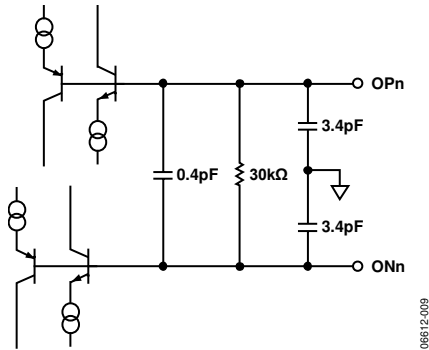
Figure 9. *AD8104*/*AD8105* Disabled Output
(see also ESD Protection Map, Figure 18)
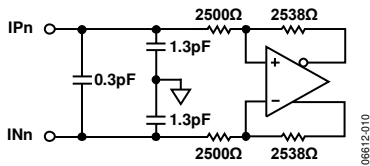
Figure 10. *AD8104* Receiver (see also ESD Protection Map, Figure 18)
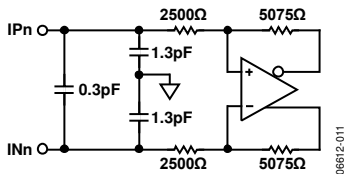
Figure 11. *AD8105* Receiver (see also ESD Protection Map, Figure 18)
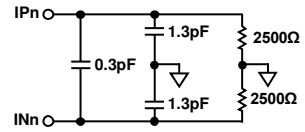
Figure 12. *AD8104*/*AD8105* Receiver Simplified Equivalent Circuit When
Driving Differentially
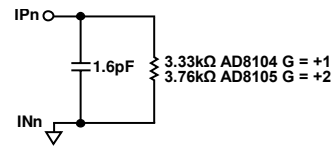
Figure 13. *AD8104*/*AD8105* Receiver Simplified Equivalent Circuit When
Driving Single-Ended
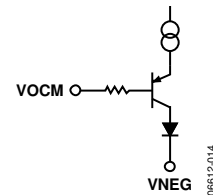
Figure 14. VOCM Input (see also ESD Protection Map, Figure 18)
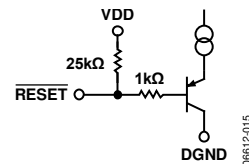
Figure 15. Reset Input (see also ESD Protection Map, Figure 18)
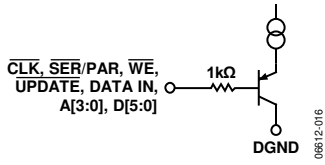
Figure 16. Logic Input (see also ESD Protection Map, Figure 18)
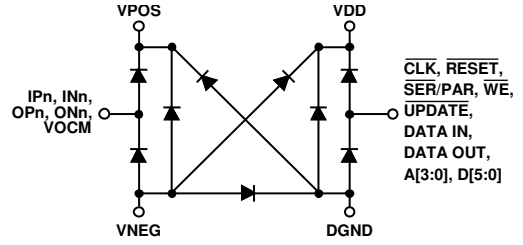
Figure 18. ESD Protection Map
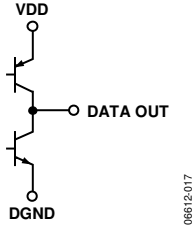
Figure 17. Logic Output (see also ESD Protection Map, Figure 18)

TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = \pm 2.5$ V at $T_A = 25°C$, $R_{L, diff} = 200$ Ω, $V_{OCM} = 0$ V, differential I/O mode, unless otherwise noted.
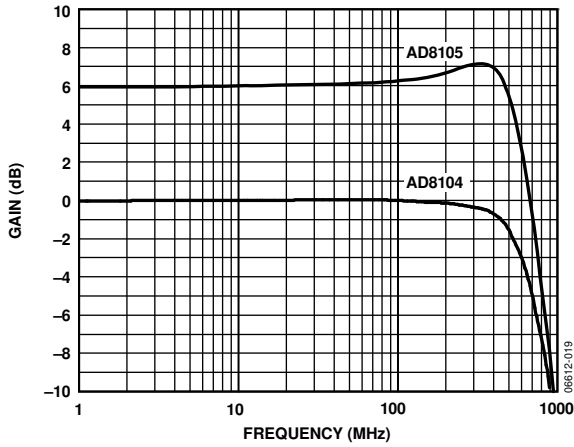
Figure 19. *AD8104*, *AD8105* Small Signal Frequency Response, 200 mV p-p
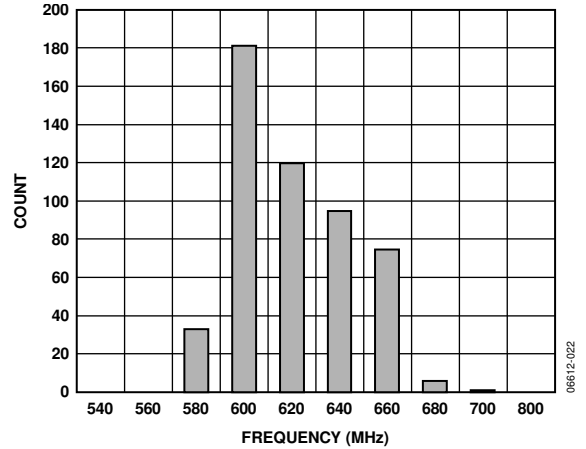
Figure 22. *AD8104* −3 dB Bandwidth Histogram,
One Device, All 512 Channels
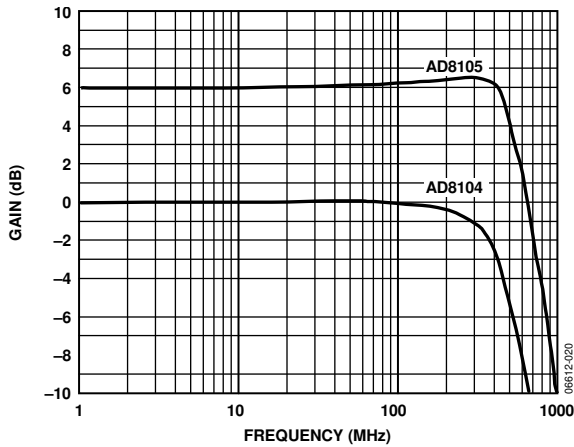
Figure 20. *AD8104*, *AD8105* Large Signal Frequency Response, 2 V p-p
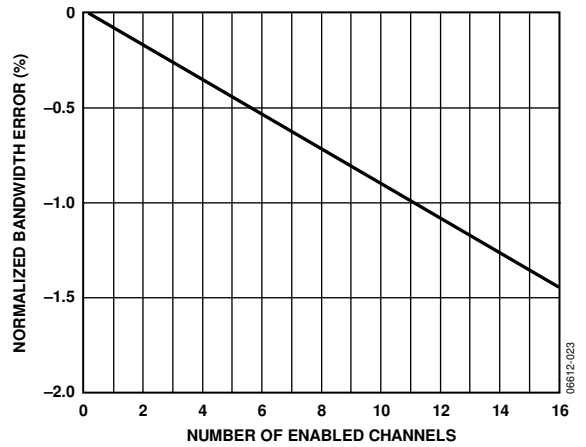
Figure 23. *AD8104* Bandwidth Error vs. Enabled Channels
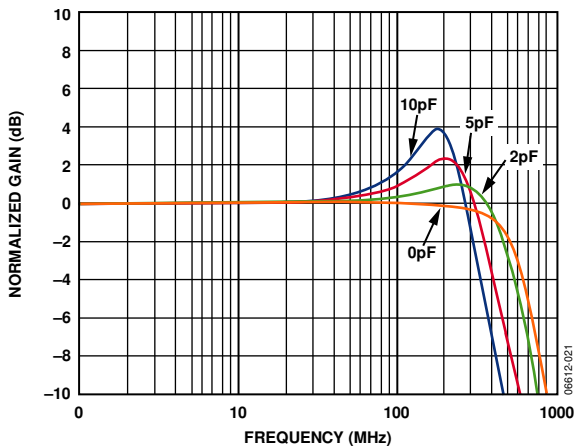
Figure 21. *AD8104* Small Signal Frequency Response with Capacitive Loads,
200 mV p-p
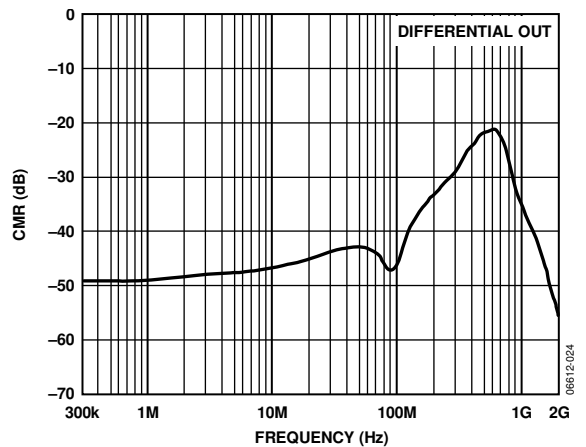
Figure 24. *AD8104*, *AD8105* Common-Mode Rejection
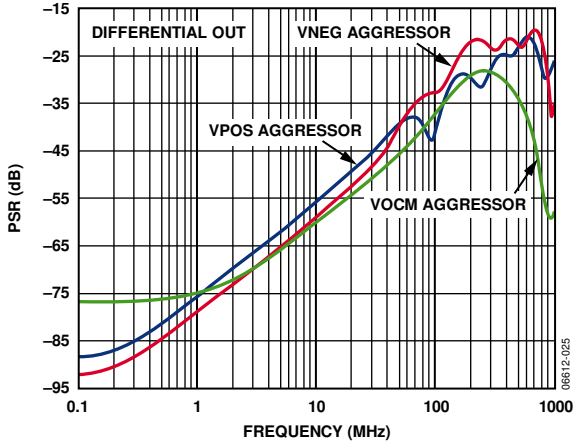
Figure 25. AD8104 Power Supply Rejection

Figure 26. AD8104 Power Supply Rejection, Single-Ended

Figure 27. AD8104, AD8105 Noise Spectral Density, RTO

Figure 28. AD8104 Crosstalk, One Adjacent Channel

Figure 29. AD8105 Crosstalk, One Adjacent Channel
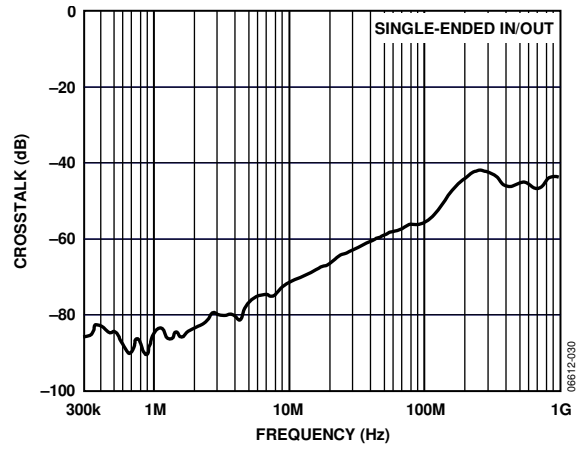
Figure 30. AD8104 Crosstalk, One Adjacent Channel, Single-Ended
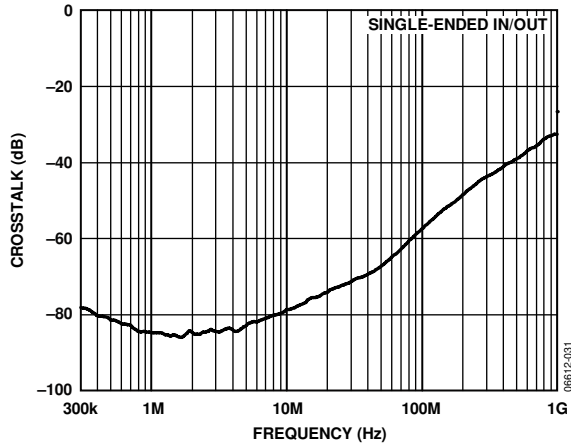
Figure 31. *AD8105 Crosstalk, One Adjacent Channel, Single-Ended*
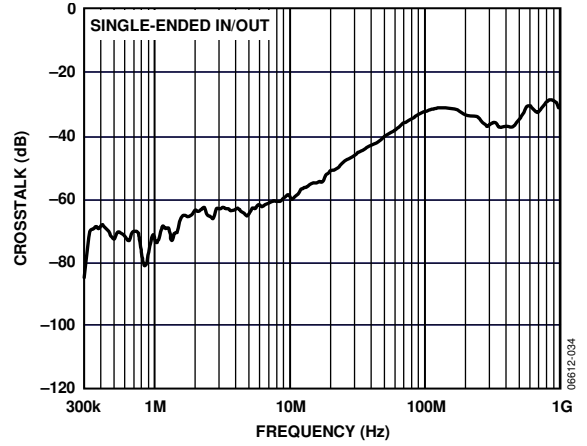
Figure 34. *AD8104 Crosstalk, All Hostile, Single-Ended*
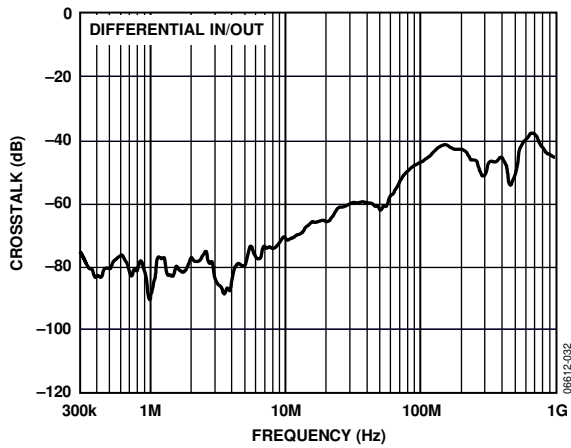
Figure 32. *AD8104 Crosstalk, All Hostile*
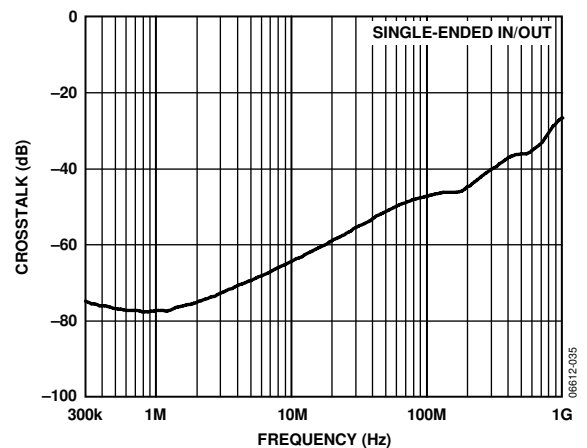
Figure 35. *AD8105 Crosstalk, All Hostile, Single-Ended*
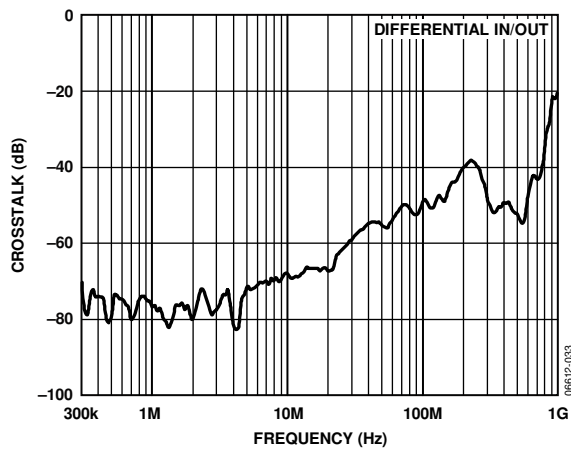
Figure 33. *AD8105 Crosstalk, All Hostile*
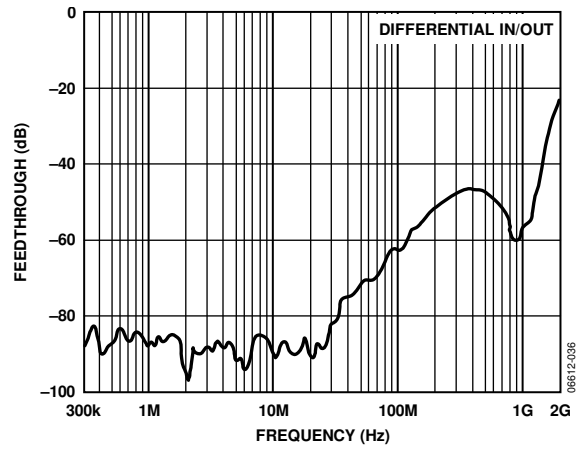
Figure 36. *AD8104 Crosstalk, Off Isolation*
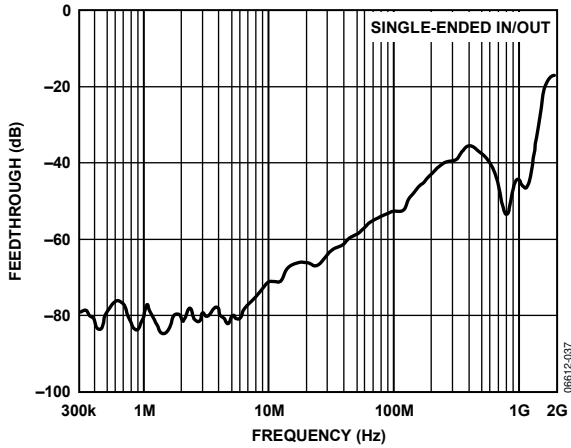
Figure 37. *AD8104 Crosstalk, Off Isolation, Single-Ended*
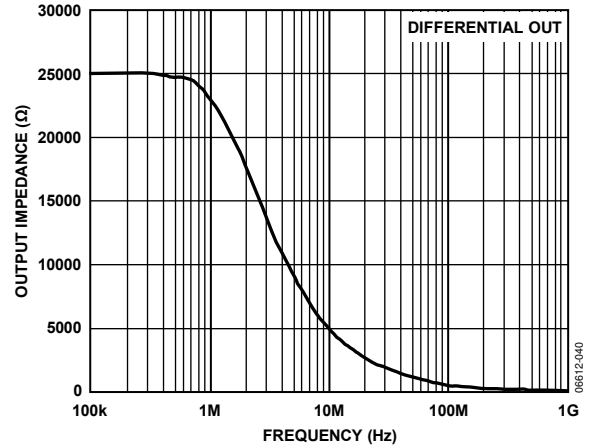
Figure 40. *AD8104, AD8105 Output Impedance, Disabled*
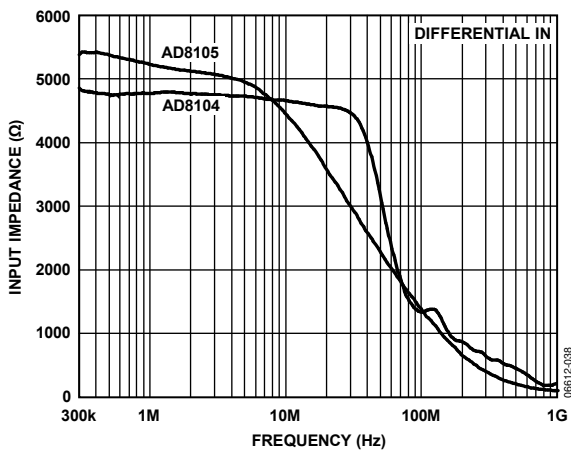
Figure 38. *AD8104, AD8105 Input Impedance*
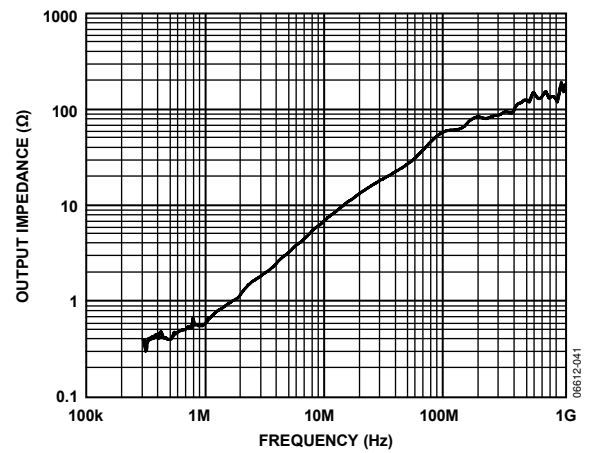
Figure 41. *AD8104, AD8105 Output Impedance, Enabled*
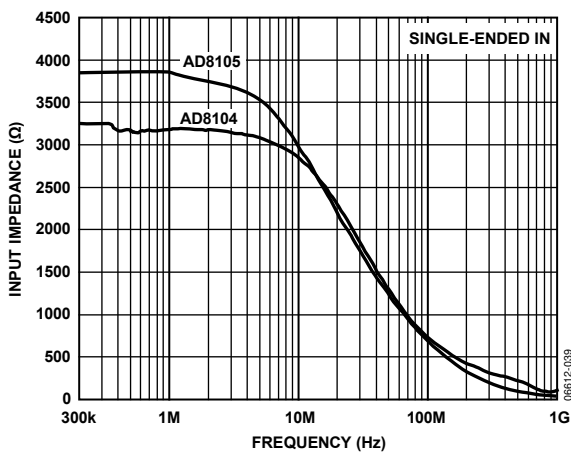
Figure 39. *AD8104, AD8105 Input Impedance, Single-Ended*
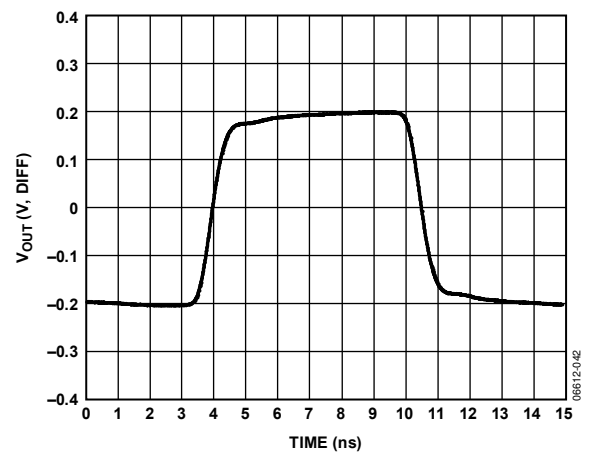
Figure 42. *AD8104 Small Signal Pulse Response, 200 mV p-p*
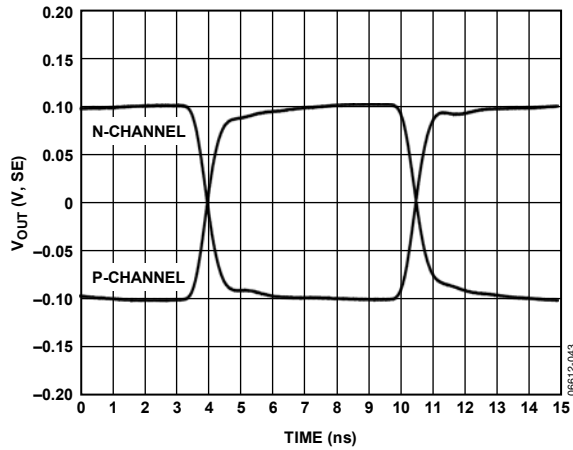
Figure 43. *AD8104 Small Signal Pulse Response, Single-Ended, 200 mV p-p*

Figure 44. *AD8104 Large Signal Pulse Response, 2 V p-p*

Figure 45. *AD8104 Large Signal Pulse Response, Single-Ended, 2 V p-p*

Figure 46. *AD8104 Switching Time*

Figure 47. *AD8104 Large Signal Rising Edge and Slew Rate*
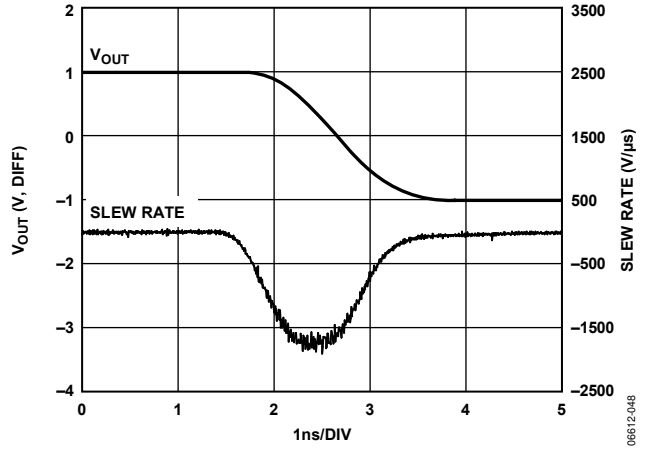
Figure 48. *AD8104 Large Signal Falling Edge and Slew Rate*
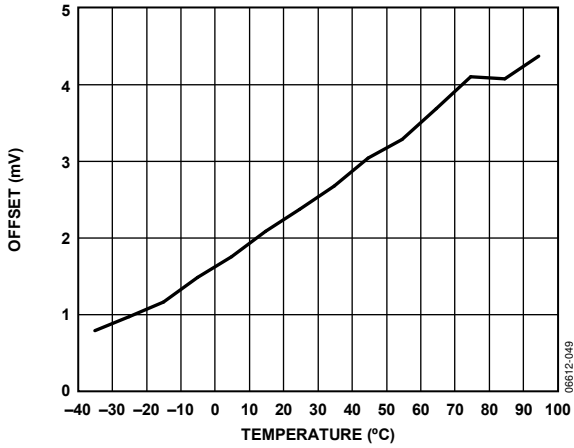
Figure 49. *AD8104* V_{OS} *vs. Temperature with All Outputs Enabled*
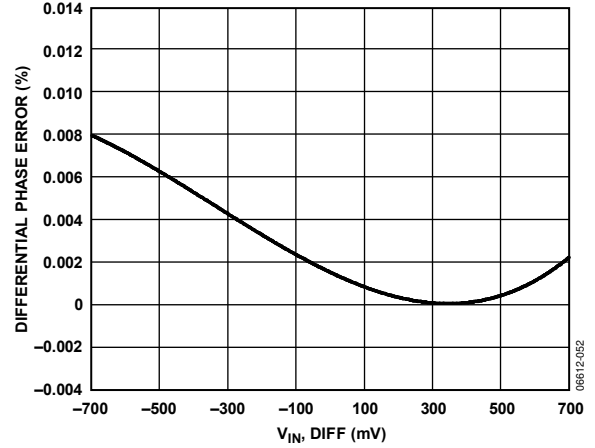
Figure 52. *AD8104 Phase vs. DC Voltage, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 600 mV p-p, Differential*
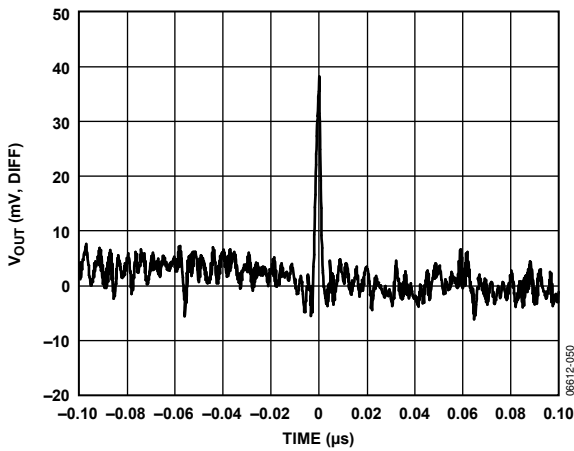
Figure 50. *AD8104 Switching Transient (Glitch)*
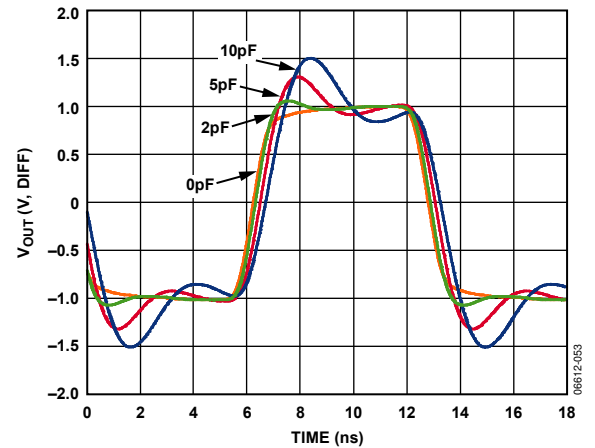
Figure 53. *AD8104 Large Signal Pulse Response with Capacitive Loads*
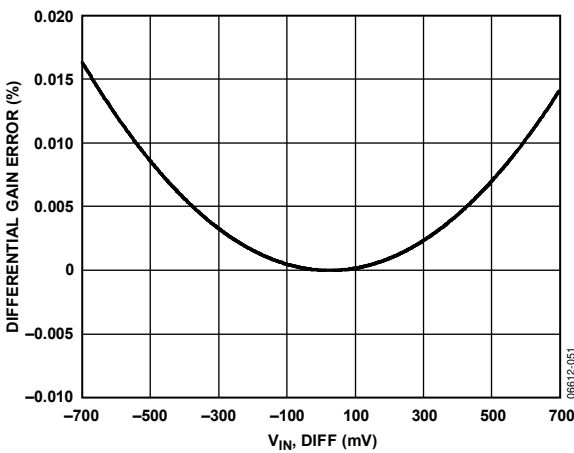
Figure 51. *AD8104 Gain vs. DC Voltage, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 600 mV p-p, Differential*
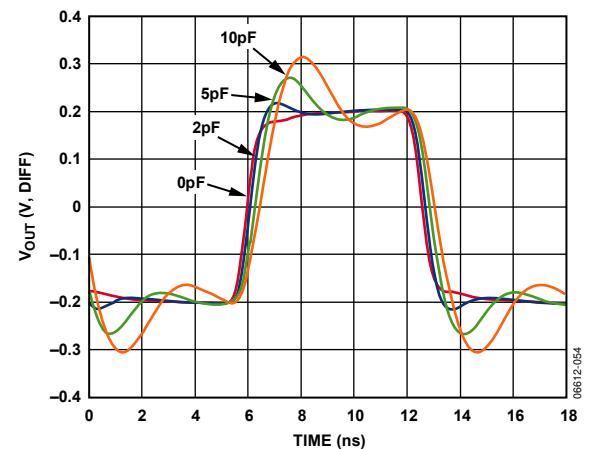
Figure 54. *AD8104 Small Signal Pulse Response with Capacitive Loads*
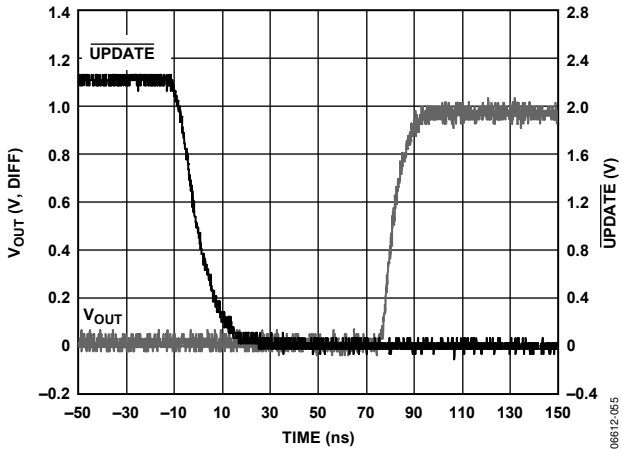
Figure 55. AD8104 Enable Time

Figure 56. AD8104 Disable Time

Figure 57. AD8104 DC Gain vs. Temperature

Figure 58. AD8104, AD8105 Quiescent Supply Currents vs. Temperature

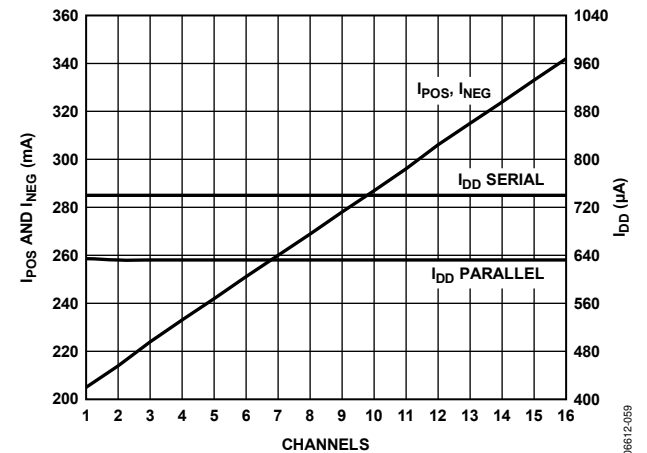*Figure 59. AD8104, AD8105 Quiescent Supply Currents vs. Enabled Outputs*

Figure 60. AD8104 Settling Time
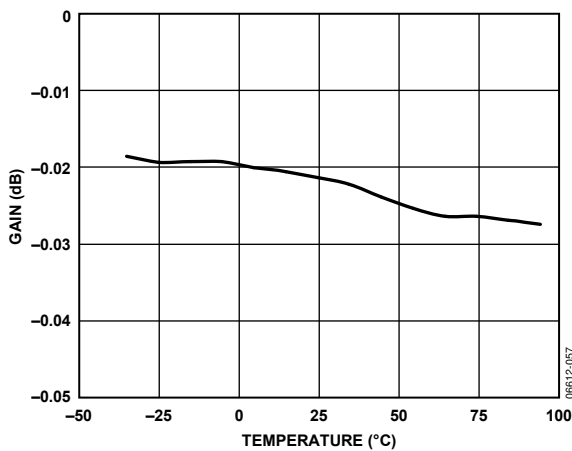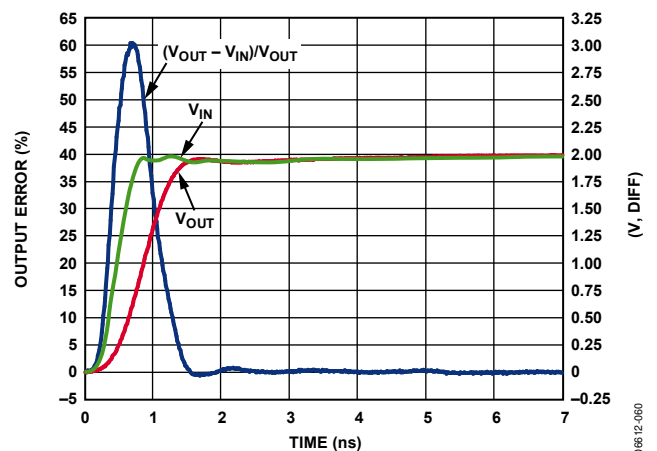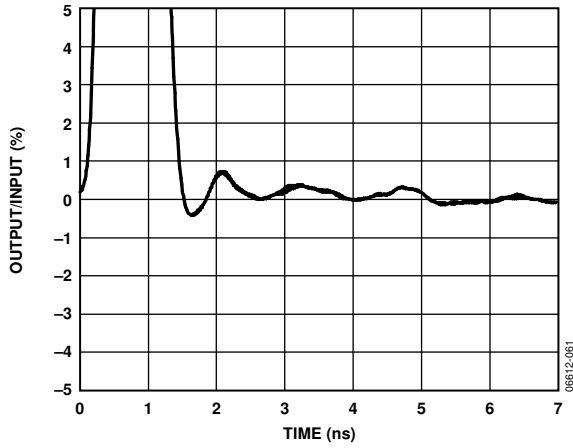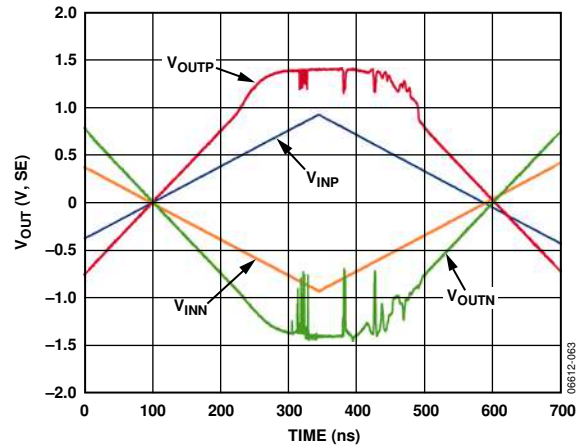
Figure 61. *AD8104 Settling Time (Zoom)*

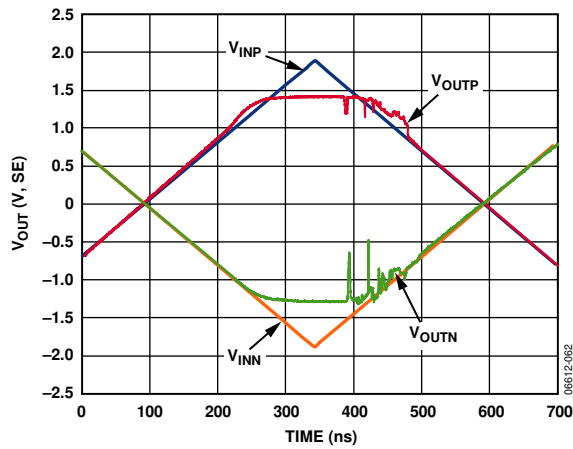Figure 63. *AD8105 Overdrive Recovery, Single-Ended*

Figure 62. *AD8104 Overdrive Recovery, Single-Ended*
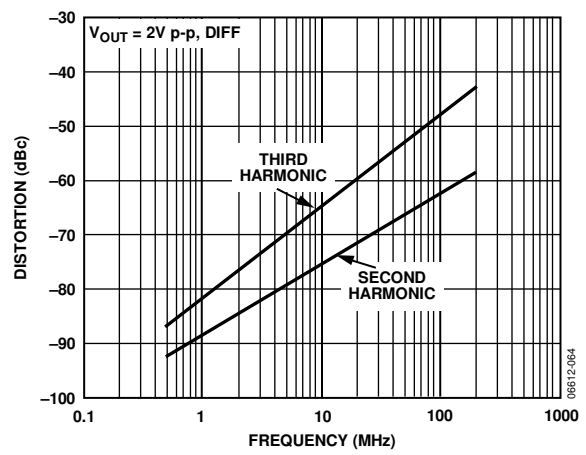

Figure 64. *AD8104 Harmonic Distortion*

THEORY OF OPERATION

The AD8104/AD8105 are fully differential crosspoint arrays with 16 outputs, each of which can be connected to any one of 32 inputs. Organized by output row, 32 switchable input transconductance stages are connected to each output buffer to form 32-to-1 multiplexers. There are 16 of these multiplexers, each with its inputs wired in parallel, for a total array of 512 transconductance stages forming a multicast-capable crosspoint switch.

Decoding logic for each output selects one (or none) of the transconductance stages to drive the output stage. The enabled transconductance stage drives the output stage, and feedback forms a closed-loop amplifier with a differential gain of +1 (the difference between the output voltages is equal to the difference between the input voltages). A second feedback loop controls the common-mode output level, forcing the average of the differential output voltages to match the voltage on the VOCM reference pin. Although each output has an independent common-mode control loop, the VOCM reference is common for the entire chip, and as such needs to be driven with a low impedance to avoid crosstalk.

Each differential input to the AD8104/AD8105 is buffered by a receiver. The purpose of this receiver is to provide an extended input common-mode range, and to remove this common mode from the signal chain. Like the output multiplexers, the input receiver has both a differential loop and a common-mode control loop. A mask-programmable feedback network sets the closed-loop differential gain. For the AD8104, this differential gain is +1, and for the AD8105, this differential gain is +2. The receiver has an input stage that does not respond to the common mode of the signal. This architecture, along with the attenuating feedback network, allows the user to apply input voltages that extend from rail to rail. Excess differential loop gain bandwidth product reduces the effect of the closed-loop gain on the bandwidth of the device.

The output stage of the AD8104/AD8105 is designed for low differential gain and phase error when driving composite video signals. It also provides slew current for fast pulse response when driving component video signals. Unlike many multiplexer designs, these requirements are balanced such that large signal bandwidth is very similar to small signal bandwidth. The design load is 150 Ω, but provisions are made to drive loads as low as 75 Ω as long as on-chip power dissipation limits are not exceeded.

The outputs of the AD8104/AD8105 can be disabled to minimize on-chip power dissipation. When disabled, there is a feedback network of 25 kΩ between the differential outputs. This high impedance allows multiple ICs to be bussed together without additional buffering. Care must be taken to reduce output capacitance, which results in more overshoot and frequency domain peaking. A series of internal amplifiers drive internal nodes such that a wideband high impedance is presented at the disabled output, even while the output bus is under large signal swings. When the outputs are disabled and driven externally, the voltage applied to them should not exceed the valid output swing range for the AD8104/AD8105 in order to keep these internal amplifiers in their linear range of operation. Applying excess differential voltages to the disabled outputs can cause damage to the AD8104/AD8105 and should be avoided (see the Absolute Maximum Ratings section for guidelines).

The connection of the AD8104/AD8105 is controlled by a flexible TTL-compatible logic interface. Either parallel or serial loading into a first rank of latches preprograms each output. A global update signal moves the programming data into the second rank of latches, simultaneously updating all outputs. In serial mode, a serial-out pin allows devices to be daisy-chained together for single-pin programming of multiple ICs. A power-on reset pin is available to avoid bus conflicts by disabling all outputs. This power-on reset clears the second rank of latches, but does not clear the first rank of latches. In parallel mode, to quickly clear the first rank, a broadcast parallel programming feature is available. In serial mode, preprogramming individual inputs is not possible and the entire shift register needs to be flushed.

The AD8104/AD8105 can operate on a single +5 V supply, powering both the signal path (with the VPOS/VNEG supply pins), and the control logic interface (with the VDD/DGND supply pins). However, to easily interface to ground-referenced video signals, split supply operation is possible with ±2.5 V supplies. In this case, a flexible logic interface allows the control logic supplies (VDD/DGND) to be run off +2 V/0 V to +5 V/0 V while the core remains on split supplies. Additional flexibility in the analog output common-mode level facilitates unequal split supplies. If +3 V/−2 V supplies to +2 V/−3 V supplies are desired, the VOCM pin can still be set to 0 V for ground-referenced video signals.