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ANALOG DEVICES

Low Cost 270 MHz Differential Receiver Amplifiers

AD8129/AD8130

FEATURES

High speed
- **AD8130: 270 MHz, 1090 V/μs @ G = +1**
- **AD8129: 200 MHz, 1060 V/μs @ G = +10**

High CMRR
- **94 dB min, dc to 100 kHz**
- **80 dB min @ 2 MHz**
- **70 dB @ 10 MHz**

High input impedance: 1 MΩ differential

Input common-mode range ±10.5 V

Low noise
- **AD8130: 12.5 nV/√Hz**
- **AD8129: 4.5 nV/√Hz**

Low distortion, 1 V p-p @ 5 MHz
- **AD8130, −79 dBc worst harmonic @ 5 MHz**
- **AD8129, −74 dBc worst harmonic @ 5 MHz**

User-adjustable gain
- **No external components for G = +1**

Power supply range +4.5 V to ±12.6 V

Power-down

APPLICATIONS

High speed differential line receivers
Differential-to-single-ended converters
High speed instrumentation amps
Level shifting

CONNECTION DIAGRAM

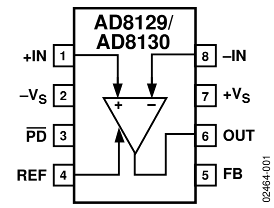

Figure 1.

The AD8129/AD8130 are differential-to-single-ended amplifiers with extremely high CMRR at high frequency. Therefore, they can also be effectively used as high speed instrumentation amps or for converting differential signals to single-ended signals.

The AD8129 is a low noise, high gain (10 or greater) version intended for applications over very long cables, where signal attenuation is significant. The AD8130 is stable at a gain of 1 and can be used for applications where lower gains are required. Both have user-adjustable gain to help compensate for losses in the transmission line. The gain is set by the ratio of two resistor values. The AD8129/AD8130 have very high input impedance on both inputs, regardless of the gain setting.

GENERAL DESCRIPTION

The AD8129/AD8130 are designed as receivers for the transmission of high speed signals over twisted-pair cables to work with the AD8131 or AD8132 drivers. Either can be used for analog or digital video signals and for high speed data transmission.

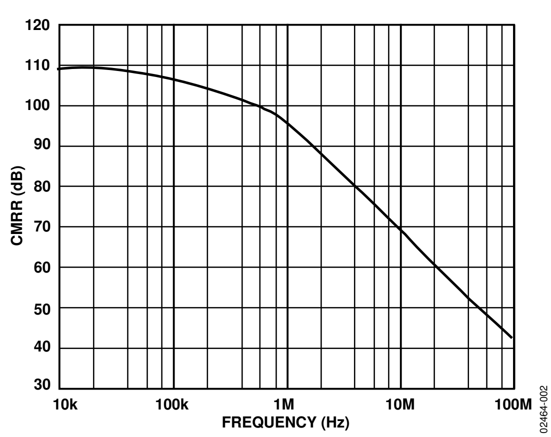

Figure 2. AD8129 CMRR vs. Frequency

The AD8129/AD8130 have excellent common-mode rejection (70 dB @ 10 MHz), allowing the use of low cost, unshielded twisted-pair cables without fear of corruption by external noise sources or crosstalk. The AD8129/AD8130 have a wide power supply range from single +5 V to ±12 V, allowing wide common-mode and differential-mode voltage ranges while maintaining signal integrity. The wide common-mode voltage range enables the driver-receiver pair to operate without isolation transformers in many systems where the ground potential difference between drive and receive locations is many volts. The AD8129/AD8130 have considerable cost and performance improvements over op amps and other multiamplifier receiving solutions.

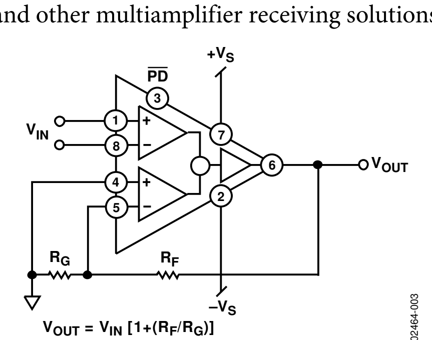

Figure 3. Typical Connection Configuration

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AD8129/AD8130 SPECIFICATIONS

5 V SPECIFICATIONS

AD8129 G = +10, AD8130 G = +1, T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, REF = 2.5 V, $\overline{PD} \geq V_{IH}$, R_L = 1 kΩ, C_L = 2 pF, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +125°C, unless otherwise noted.

Table 1.

Model		AD8129			AD8130			
Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE								
−3 dB Bandwidth	V_{OUT} ≤ 0.3 V p-p	160	185		220	250		MHz
	V_{OUT} = 1 V p-p	160	185		180	205		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} ≤ 0.3 V p-p, SOIC/MSOP		25/40			25		MHz
Slew Rate	V_{OUT} = 2 V p-p, 25% to 75%	810	930		810	930		V/μs
Settling Time	V_{OUT} = 2 V p-p, 0.1%		20			20		ns
Rise and Fall Times	V_{OUT} ≤ 1 V p-p, 10% to 90%		1.8			1.5		ns
Output Overdrive Recovery			20			30		ns
NOISE/DISTORTION								
Second Harmonic/Third Harmonic	V_{OUT} = 1 V p-p, 5 MHz		−68/−75			−72/−79		dBc
	V_{OUT} = 2 V p-p, 5 MHz		−62/−64			−65/−71		dBc
	V_{OUT} = 1 V p-p, 10 MHz		−63/−70			−60/−62		dBc
	V_{OUT} = 2 V p-p, 10 MHz		−56/−58			−68/−68		dBc
IMD	V_{OUT} = 2 V p-p, 10 MHz		−67			−70		dBc
Output IP3	V_{OUT} = 2 V p-p, 10 MHz		25			26		dBm
Input Voltage Noise (RTI)	f ≥ 10 kHz		4.5			12.3		nV/√Hz
Input Current Noise (+IN, −IN)	f ≥ 100 kHz		1			1		pA/√Hz
Input Current Noise (REF, FB)	f ≥ 100 kHz		1.4			1.4		pA/√Hz
Differential Gain Error	AD8130, G = +2, NTSC 100 IRE, R_L ≥ 150 Ω		0.3			0.13		%
Differential Phase Error	AD8130, G = +2, NTSC 100 IRE, R_L ≥ 150 Ω		0.1			0.15		Degrees
INPUT CHARACTERISTICS								
Common-Mode Rejection Ratio	DC to 100 kHz, V_{CM} = 1.5 V to 3.5 V	86	96		86	96		dB
	V_{CM} = 1 V p-p @ 1 MHz	80			80			dB
	V_{CM} = 1 V p-p @ 10 MHz		70			70		dB
CMRR with V_{OUT} = 1 V p-p	V_{CM} = 1 V p-p @ 1 kHz, V_{OUT} = ±0.5 V dc		80			72		dB
Common-Mode Voltage Range	$V_{+IN} - V_{-IN}$ = 0 V		1.25 to 3.7			1.25 to 3.8		V
Differential Operating Range			±0.5			±2.5		V
Differential Clipping Level		±0.6	±0.75	±0.85	±2.3	±2.8	±3.3	V
Resistance	Differential		1			6		MΩ
	Common mode		4			4		MΩ
Capacitance	Differential		3			3		pF
	Common mode		4			4		pF

Model Parameter	Conditions	AD8129 Min	AD8129 Typ	AD8129 Max	AD8130 Min	AD8130 Typ	AD8130 Max	Unit
DC PERFORMANCE								
Closed-Loop Gain Error	V_{OUT} = ±1 V, R_L ≥ 150 Ω		±0.25	±1.25		±0.1	±0.6	%
	T_{MIN} to T_{MAX}		20			20		ppm/°C
Open-Loop Gain	V_{OUT} = ±1 V		86			71		dB
Gain Nonlinearity	V_{OUT} = ±1 V		250			200		ppm
Input Offset Voltage			0.2	0.8		0.4	1.8	mV
	T_{MIN} to T_{MAX}		2			20		µV/°C
	T_{MIN} to T_{MAX}			1.4			3.5	mV
Input Offset Voltage vs. Supply	$+V_S$ = 5 V, $-V_S$ = −0.5 V to +0.5 V		−88	−80		−74	−70	dB
	$-V_S$ = 0 V, $+V_S$ = +4.5 V to +5.5 V		−100	−86		−90	−76	dB
Input Bias Current (+IN, −IN)			±0.5	±2		±0.5	±2	µA
Input Bias Current (REF, FB)			±1	±3.5		±1	±3.5	µA
	T_{MIN} to T_{MAX} (+IN, −IN, REF, FB)		5			5		nA/°C
Input Offset Current	(+IN, −IN, REF, FB)		±0.08	±0.4		±0.08	±0.4	µA
	T_{MIN} to T_{MAX}		0.2			0.2		nA/°C
OUTPUT PERFORMANCE								
Voltage Swing	R_{LOAD} ≥ 150 Ω	1.1		3.9	1.1		3.9	V
Output Current			35			35		mA
Short-Circuit Current	To common		−60/+55			−60/+55		mA
	T_{MIN} to T_{MAX}		−240			−240		µA/°C
Output Impedance	$\overline{PD}$ ≤ V_{IL}, in power-down mode		10			10		pF
POWER SUPPLY								
Operating Voltage Range	Total supply voltage	±2.25		±12.6	±2.25		±12.6	V
Quiescent Supply Current			9.9	10.6		9.9	10.6	mA
	T_{MIN} to T_{MAX}		33			33		µA/°C
	$\overline{PD}$ ≤ V_{IL}		0.65	0.85		0.65	0.85	mA
	$\overline{PD}$ ≤ V_{IL}, T_{MIN} to T_{MAX}			1			1	mA
$\overline{PD}$ PIN								
V_{IH}		$+V_S$ − 1.5			$+V_S$ − 1.5			V
V_{IL}				$+V_S$ − 2.5			$+V_S$ − 2.5	V
I_{IH}	$\overline{PD}$ = min V_{IH}			−30			−30	µA
I_{IL}	$\overline{PD}$ = max V_{IL}			−50			−50	µA
Input Resistance	$\overline{PD}$ ≤ $+V_S$ − 3 V		12.5			12.5		kΩ
	$\overline{PD}$ ≥ $+V_S$ − 2 V		100			100		kΩ
Enable Time			0.5			0.5		µs
OPERATING TEMPERATURE RANGE		−40		+125	−40		+125	°C

±5 V SPECIFICATIONS

AD8129 G = +10, AD8130 G = +1, T_A = 25°C, V_S = ±5 V, REF = 0 V, $\overline{PD}$ ≥ V_{IH}, R_L = 1 kΩ, C_L = 2 pF, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Conditions	AD8129 Min	AD8129 Typ	AD8129 Max	AD8130 Min	AD8130 Typ	AD8130 Max	Unit
DYNAMIC PERFORMANCE								
−3 dB Bandwidth	V_{OUT} ≤ 0.3 V p-p	175	200		240	270		MHz
	V_{OUT} = 2 V p-p	170	190		140	155		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} ≤ 0.3 V p-p, SOIC/MSOP		30/50			45		MHz
Slew Rate	V_{OUT} = 2 V p-p, 25% to 75%	925	1060		950	1090		V/µs
Settling Time	V_{OUT} = 2 V p-p, 0.1%		20			20		ns
Rise and Fall Times	V_{OUT} ≤ 1 V p-p, 10% to 90%		1.7			1.4		ns
Output Overdrive Recovery			30			40		ns
NOISE/DISTORTION								
Second Harmonic/Third Harmonic	V_{OUT} = 1 V p-p, 5 MHz		−74/−84			−79/−86		dBc
	V_{OUT} = 2 V p-p, 5 MHz		−68/−74			−74/−81		dBc
	V_{OUT} = 1 V p-p, 10 MHz		−67/−81			−74/−80		dBc
	V_{OUT} = 1 V p-p, 10 MHz		−61/−70			−74/−76		dBc
IMD	V_{OUT} = 2 V p-p, 10 MHz		−67			−70		dBc
Output IP3	V_{OUT} = 2 V p-p, 10 MHz		25			26		dBm
Input Voltage Noise (RTI)	f ≥ 10 kHz		4.5			12.5		nV/√Hz
Input Current Noise (+IN, −IN)	f ≥ 100 kHz		1			1		pA/√Hz
Input Current Noise (REF, FB)	f ≥ 100 kHz		1.4			1.4		pA/√Hz
Differential Gain Error	AD8130, G = +2, NTSC 200 IRE, R_L ≥ 150 Ω		0.3			0.13		%
Differential Phase Error	AD8130, G = +2, NTSC 200 IRE, R_L ≥ 150 Ω		0.1			0.15		Degrees
INPUT CHARACTERISTICS								
Common-Mode Rejection Ratio	DC to 100 kHz, V_{CM} = −3 V to +3.5 V	94	110		90	110		dB
	V_{CM} = 1 V p-p @ 2 MHz	80			80			dB
	V_{CM} = 1 V p-p @ 10 MHz		70			70		dB
CMRR with V_{OUT} = 1 V p-p	V_{CM} = 2 V p-p @ 1 kHz, V_{OUT} = ±0.5 V dc		100			83		dB
Common-Mode Voltage Range	V_{+IN} − $V_{−IN}$ = 0 V		±3.5			±3.8		V
Differential Operating Range			±0.5			±2.5		V
Differential Clipping Level		±0.6	±0.75	±0.85	±2.3	±2.8	±3.3	V
Resistance	Differential		1			6		MΩ
	Common mode		4			4		MΩ
Capacitance	Differential		3			3		pF
	Common mode		4			4		pF

Parameter	Conditions	AD8129 Min	AD8129 Typ	AD8129 Max	AD8130 Min	AD8130 Typ	AD8130 Max	Unit
DC PERFORMANCE								
Closed-Loop Gain Error	V_{OUT} = ±1 V, R_L ≥ 150 Ω		±0.4	±1.5		±0.15	±0.6	%
	T_{MIN} to T_{MAX}		20			10		ppm/°C
Open-Loop Gain	V_{OUT} = ±1 V		88			74		dB
Gain Nonlinearity	V_{OUT} = ±1 V		250			200		ppm
Input Offset Voltage			0.2	0.8		0.4	1.8	mV
	T_{MIN} to T_{MAX}		2			20		μV/°C
	T_{MIN} to T_{MAX}			1.4			3.5	mV
Input Offset Voltage vs. Supply	$+V_S$ = +5 V, $-V_S$ = −4.5 V to −5.5 V		−90	−84		−78	−74	dB
	$-V_S$ = −5 V, $+V_S$ = +4.5 V to +5.5 V		−94	−86		−80	−74	dB
Input Bias Current (+IN, −IN)			±0.5	±2		±0.5	±2	μA
Input Bias Current (REF, FB)			±1	±3.5		±1	±3.5	μA
	T_{MIN} to T_{MAX} (+IN, −IN, REF, FB)		5			5		nA/°C
Input Offset Current	(+IN, −IN, REF, FB)		±0.08	±0.4		±0.08	±0.4	μA
	T_{MIN} to T_{MAX}		0.2			0.2		nA/°C
OUTPUT PERFORMANCE								
Voltage Swing	R_{LOAD} = 150 Ω/1 kΩ	3.6/4.0			3.6/4.0			±V
Output Current			40			40		mA
Short-Circuit Current	To common		−60/+55			−60/+55		mA
	T_{MIN} to T_{MAX}		−240			−240		μA/°C
Output Impedance	$\overline{PD}$ ≤ V_{IL}, in power-down mode		10			10		pF
POWER SUPPLY								
Operating Voltage Range	Total supply voltage	±2.25		±12.6	±2.25		±12.6	V
Quiescent Supply Current			10.8	11.6		10.8	11.6	mA
	T_{MIN} to T_{MAX}		36			36		μA/°C
	$\overline{PD}$ ≤ V_{IL}		0.68	0.85		0.68	0.85	mA
	$\overline{PD}$ ≤ V_{IL}, T_{MIN} to T_{MAX}			1			1	mA
$\overline{PD}$ PIN								
V_{IH}		$+V_S$ − 1.5			$+V_S$ − 1.5			V
V_{IL}				$+V_S$ − 2.5			$+V_S$ − 2.5	V
I_{IH}	$\overline{PD}$ = min V_{IH}			−30			−30	μA
I_{IL}	$\overline{PD}$ = max V_{IL}			−50			−50	μA
Input Resistance	$\overline{PD}$ ≤ $+V_S$ − 3 V		12.5			12.5		kΩ
	$\overline{PD}$ ≥ $+V_S$ − 2 V		100			100		kΩ
Enable Time			0.5			0.5		μs
OPERATING TEMPERATURE RANGE		−40		+125	−40		+125	°C

±12 V SPECIFICATIONS

AD8129 G = +10, AD8130 G = +1, T_A = 25°C, V_S = ±12 V, REF = 0 V, $\overline{PD} \geq V_{IH}$, R_L = 1 kΩ, C_L = 2 pF, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	Conditions	AD8129 Min	AD8129 Typ	AD8129 Max	AD8130 Min	AD8130 Typ	AD8130 Max	Unit
DYNAMIC PERFORMANCE								
−3 dB Bandwidth	V_{OUT} ≤ 0.3 V p-p	175	200		250	290		MHz
	V_{OUT} = 2 V p-p	170	195		150	175		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} ≤ 0.3 V p-p, SOIC/MSOP		50/70			110		MHz
Slew Rate	V_{OUT} = 2 V p-p, 25% to 75%	935	1070		960	1100		V/µs
Settling Time	V_{OUT} = 2 V p-p, 0.1%		20			20		ns
Rise and Fall Times	V_{OUT} ≤ 1 V p-p, 10% to 90%		1.7			1.4		ns
Output Overdrive Recovery			40			40		ns
NOISE/DISTORTION								
Second Harmonic/Third Harmonic	V_{OUT} = 1 V p-p, 5 MHz		−71/−84			−79/−86		dBc
	V_{OUT} = 2 V p-p, 5 MHz		−65/−74			−74/−81		dBc
	V_{OUT} = 1 V p-p, 10 MHz		−65/−82			−74/−80		dBc
	V_{OUT} = 2 V p-p, 10 MHz		−59/−70			−74/−74		dBc
IMD	V_{OUT} = 2 V p-p, 10 MHz		−67			−70		dBc
Output IP3	V_{OUT} = 2 V p-p, 10 MHz		25			26		dBm
Input Voltage Noise (RTI)	f ≥ 10 kHz		4.6			13		nV/√Hz
Input Current Noise (+IN, −IN)	f ≥ 100 kHz		1			1		pA/√Hz
Input Current Noise (REF, FB)	f ≥ 100 kHz		1.4			1.4		pA/√Hz
Differential Gain Error	AD8130, G = +2, NTSC 200 IRE, R_L ≥ 150 Ω		0.3			0.13		%
Differential Phase Error	AD8130, G = +2, NTSC 200 IRE, R_L ≥ 150 Ω		0.1			0.2		Degrees
INPUT CHARACTERISTICS								
Common-Mode Rejection Ratio	DC to 100 kHz, V_{CM} = ±10 V	92	105		88	105		dB
	V_{CM} = 1 V p-p @ 2 MHz	80			80			dB
	V_{CM} = 1 V p-p @ 10 MHz		70			70		dB
CMRR with V_{OUT} = 1 V p-p	V_{CM} = 4 V p-p @ 1 kHz, V_{OUT} = ±0.5 V dc		93			80		dB
Common-Mode Voltage Range	$V_{+IN} - V_{-IN}$ = 0 V		±10.3			±10.5		V
Differential Operating Range			±0.5			±2.5		V
Differential Clipping Level		±0.6	±0.75	±0.85	±2.3	±2.8	±3.3	V
Resistance	Differential		1			6		MΩ
	Common mode		4			4		MΩ
Capacitance	Differential		3			3		pF
	Common mode		4			4		pF

Parameter	Conditions	AD8129 Min	AD8129 Typ	AD8129 Max	AD8130 Min	AD8130 Typ	AD8130 Max	Unit
DC PERFORMANCE								
Closed-Loop Gain Error	V_{OUT} = ±1 V, R_L ≥ 150 Ω		±0.8	±1.8		±0.15	±0.6	%
	T_{MIN} to T_{MAX}		20			10		ppm/°C
Open-Loop Gain	V_{OUT} = ±1 V		87			73		dB
Gain Nonlinearity	V_{OUT} = ±1 V		250			200		ppm
Input Offset Voltage			0.2	0.8		0.4	1.8	mV
	T_{MIN} to T_{MAX}		2			20		μV/°C
	T_{MIN} to T_{MAX}			1.4			3.5	mV
Input Offset Voltage vs. Supply	$+V_S$ = +12 V, $-V_S$ = −11.0 V to −13.0 V		−88	−82		−77	−70	dB
	$-V_S$ = −12 V, $+V_S$ = +11.0 V to +13.0 V		−92	−84		−88	−70	dB
Input Bias Current (+IN, −IN)			±0.25	±2		±0.25	±2	μA
Input Bias Current (REF, FB)			±0.5	±3.5		±0.5	±3.5	μA
	T_{MIN} to T_{MAX} (+IN, −IN, REF, FB)		2.5			2.5		nA/°C
Input Offset Current	(+IN, −IN, REF, FB)		±0.08	±0.4		±0.08	±0.4	μA
	T_{MIN} to T_{MAX}		0.2			0.2		nA/°C
OUTPUT PERFORMANCE								
Voltage Swing	R_{LOAD} = 700 Ω	±10.8			±10.8			V
Output Current			40			40		mA
Short-Circuit Current	To common		−60/+55			−60/+55		mA
	T_{MIN} to T_{MAX}		−240			−240		μA/°C
Output Impedance	$\overline{PD}$ ≤ V_{IL}, in power-down mode		10			10		pF
POWER SUPPLY								
Operating Voltage Range	Total supply voltage	±2.25		±12.6	±2.25		±12.6	V
Quiescent Supply Current			13	13.9		13	13.9	mA
	T_{MIN} to T_{MAX}		43			43		μA°C
	$\overline{PD}$ ≤ V_{IL}		0.73	0.9		0.73	0.9	mA
	$\overline{PD}$ ≤ V_{IL}, T_{MIN} to T_{MAX}			1.1			1.1	mA
$\overline{PD}$ PIN								
V_{IH}		$+V_S$ − 1.5			$+V_S$ − 1.5			V
V_{IL}				$+V_S$ − 2.5			$+V_S$ − 2.5	V
I_{IH}	$\overline{PD}$ = min V_{IH}			−30			−30	μA
I_{IL}	$\overline{PD}$ = max V_{IL}			−50			−50	μA
Input Resistance	$\overline{PD}$ ≤ $+V_S$ − 3 V		3			3		kΩ
	$\overline{PD}$ ≥ $+V_S$ − 2 V		100			100		kΩ
Enable Time			0.5			0.5		μs
OPERATING TEMPERATURE RANGE		−40		+85	−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	26.4 V
Power Dissipation	Refer to Figure 4
Input Voltage (Any Input)	$-V_S - 0.3$ V to $+V_S + 0.3$ V
Differential Input Voltage (AD8129)	
$V_S \geq \pm 11.5$ V	±0.5 V
Differential Input Voltage (AD8129)	
$V_S < \pm 11.5$ V	±6.2 V
Differential Input Voltage (AD8130)	±8.4 V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered in a circuit board in still air.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead SOIC/4-Layer	121	°C/W
8-Lead MSOP/4-Layer	142	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the AD8129/AD8130 packages is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8129/AD8130. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow reduces θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces through holes, ground, and power planes reduces the θ_{JA}.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8-lead SOIC (121°C/W) and MSOP (θ_{JA} = 142°C/W) packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

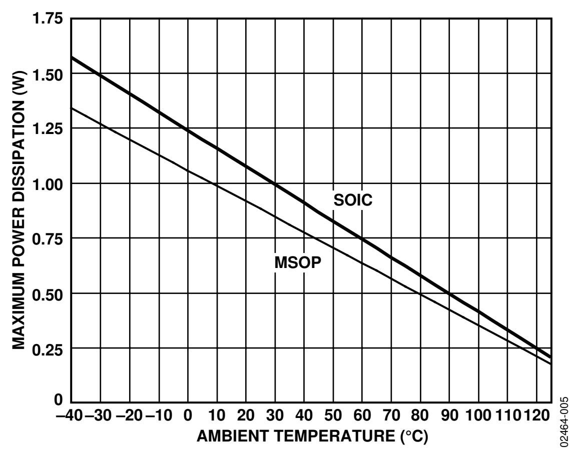


Figure 4. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

TYPICAL PERFORMANCE CHARACTERISTICS

AD8130 FREQUENCY RESPONSE CHARACTERISTICS

G = +1, R_L = 1 kΩ, C_L = 2 pF, V_{OUT} = 0.3 V p-p, T_A = 25°C, unless otherwise noted.

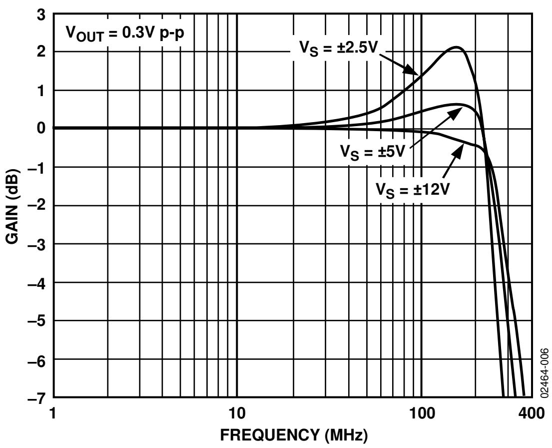


Figure 5. AD8130 Frequency Response vs. Supply, V_{OUT} = 0.3 V p-p

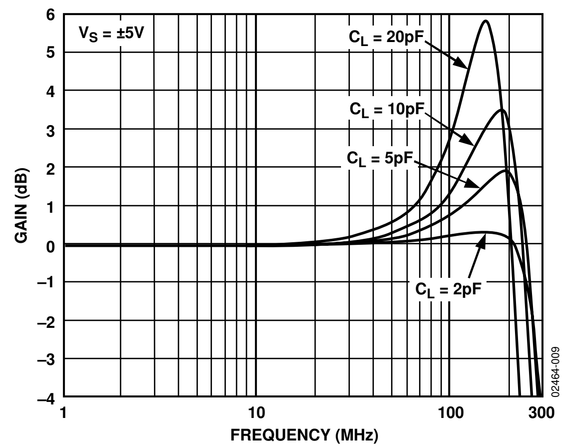


Figure 8. AD8130 Frequency Response vs. Load Capacitance

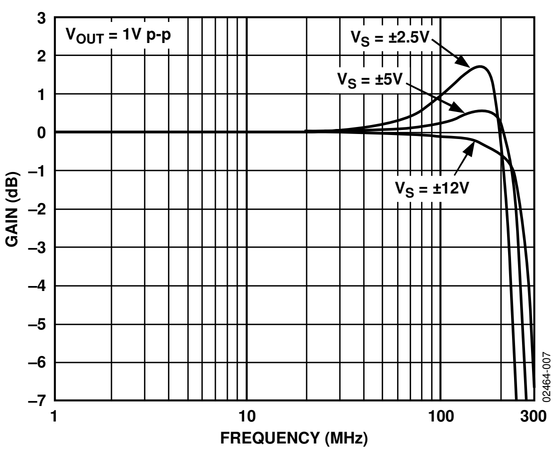


Figure 6. AD8130 Frequency Response vs. Supply, V_{OUT} = 1 V p-p

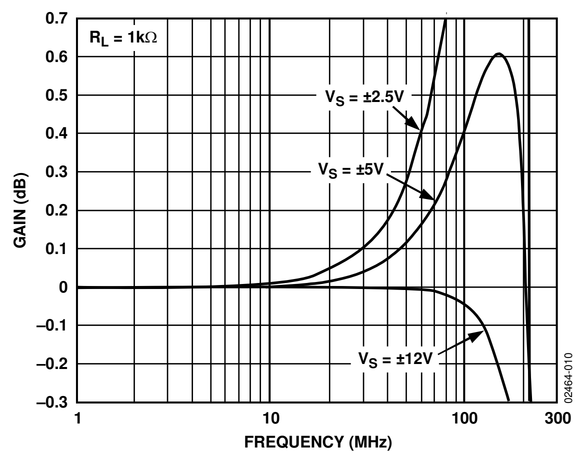


Figure 9. AD8130 Fine Scale Response vs. Supply, R_L = 1 kΩ

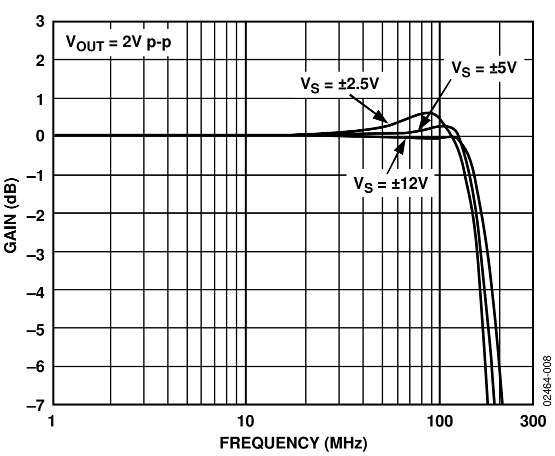


Figure 7. AD8130 Frequency Response vs. Supply, V_{OUT} = 2 V p-p

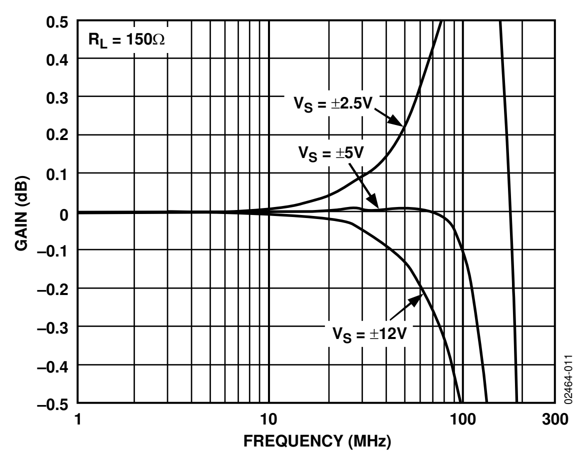


Figure 10. AD8130 Fine Scale Response vs. Supply, R_L = 150 Ω

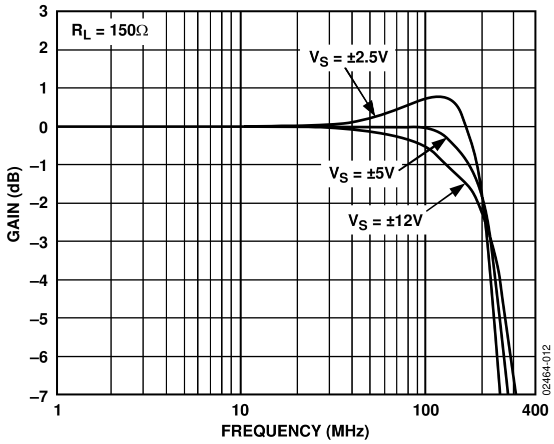


Figure 11. AD8130 Frequency Response vs. Supply, $R_L = 150\ \Omega$

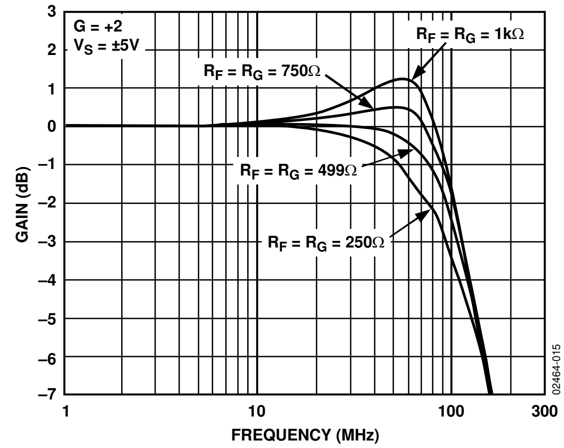


Figure 14. AD8130 Frequency Response for Various R_F/R_G

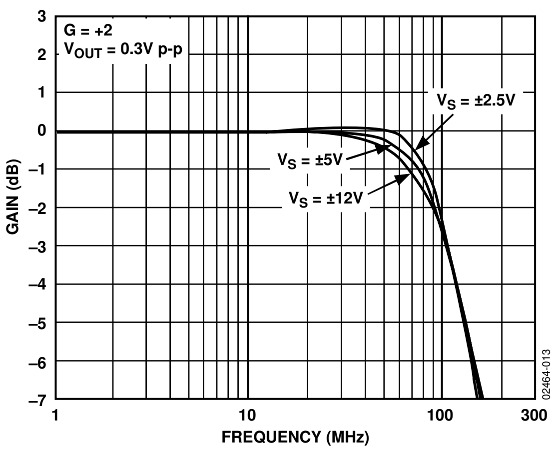


Figure 12. AD8130 Frequency Response vs. Supply, $G = +2$, $V_{OUT} = 0.3$ V p-p

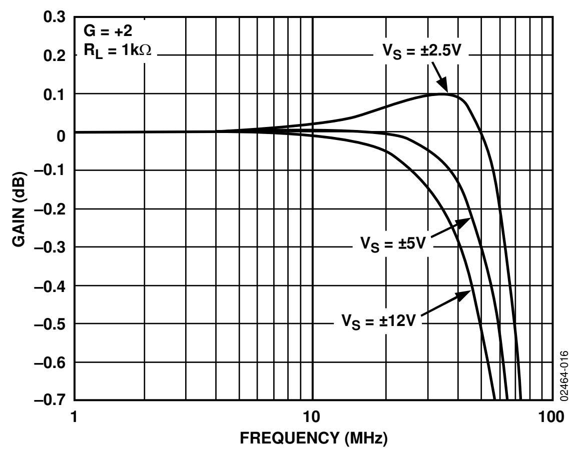


Figure 15. AD8130 Fine Scale Response vs. Supply, $G = +2$, $R_L = 1\ k\Omega$

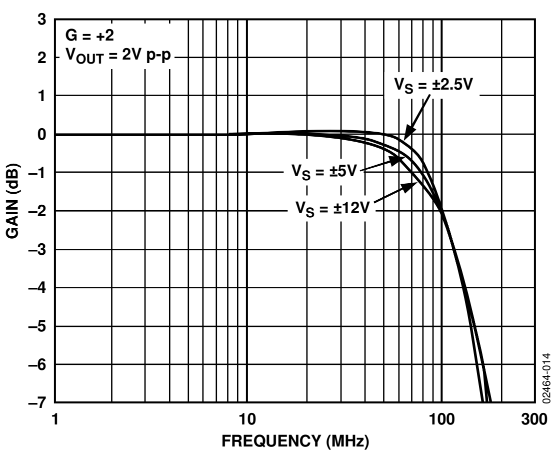


Figure 13. AD8130 Frequency Response vs. Supply, $G = +2$, $V_{OUT} = 2$ V p-p

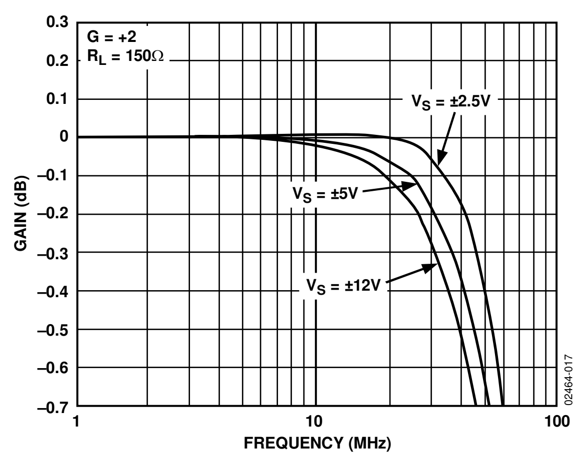


Figure 16. AD8130 Fine Scale Response vs. Supply, $G = +2$, $R_L = 150\ \Omega$

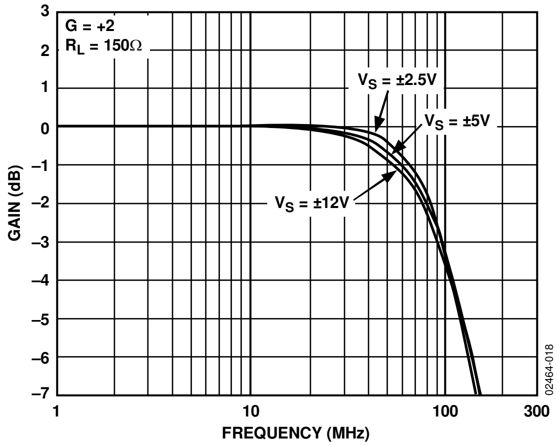


Figure 17. AD8130 Frequency Response vs. Supply, $G = +2$, $R_L = 150\ \Omega$

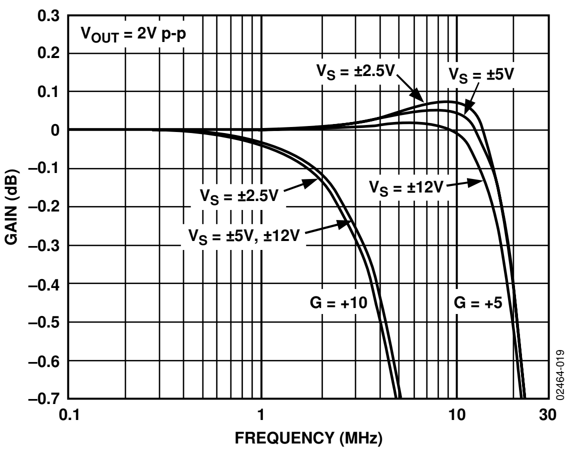


Figure 18. AD8130 Fine Scale Response vs. Supply, $G = +5$, $G = +10$, $V_{OUT} = 2\ V$ p-p

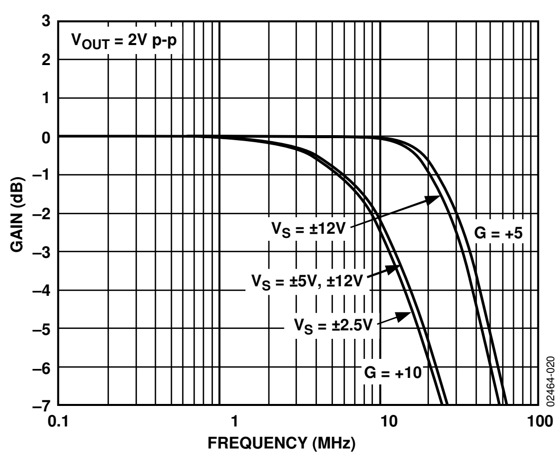


Figure 19. AD8130 Frequency Response vs. Supply, $G = +5$, $G = +10$, $V_{OUT} = 2\ V$ p-p

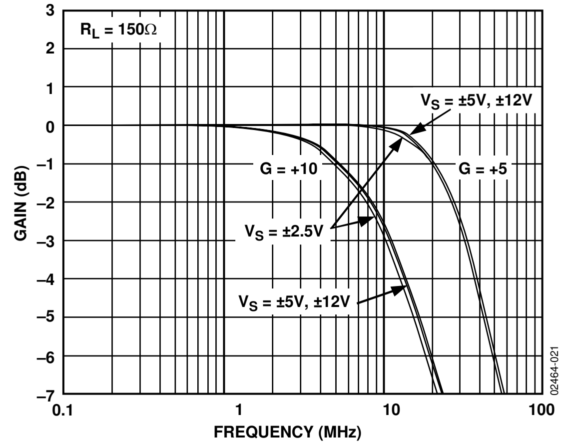


Figure 20. AD8130 Frequency Response vs. Supply, $G = +5$, $G = +10$, $R_L = 150\ \Omega$

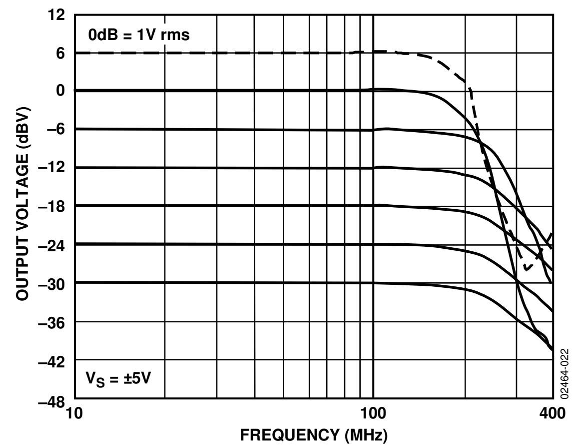
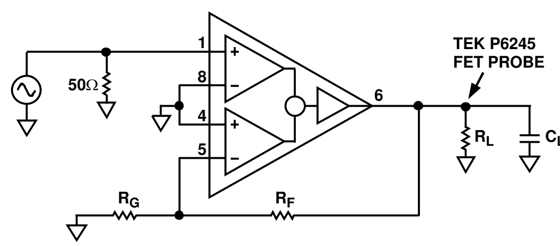


Figure 21. AD8130 Frequency Response for Various Output Levels



G	R_F	R_G
1	0Ω	–
2	499Ω	499Ω
5	8.06kΩ	2kΩ
10	4.99kΩ	549Ω

Figure 22. AD8130 Basic Frequency Response Test Circuit

AD8129 FREQUENCY RESPONSE CHARACTERISTICS

G = +10, R_L = 1 kΩ, C_L = 2 pF, V_{OUT} = 0.3 V p-p, T_A = 25°C, unless otherwise noted.

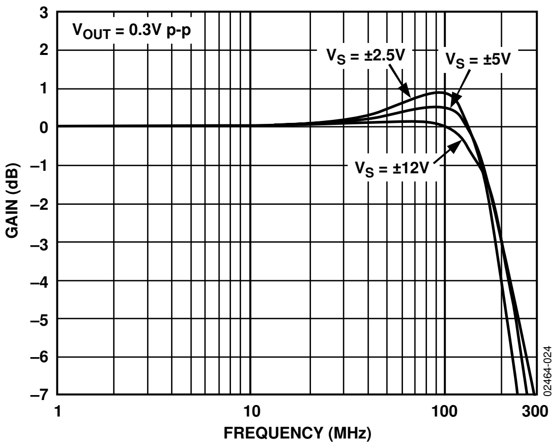


Figure 23. AD8129 Frequency Response vs. Supply, V_{OUT} = 0.3 V p-p

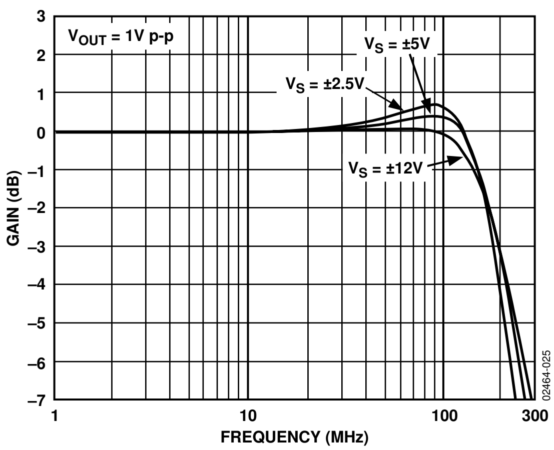


Figure 24. AD8129 Frequency Response vs. Supply, V_{OUT} = 1 V p-p

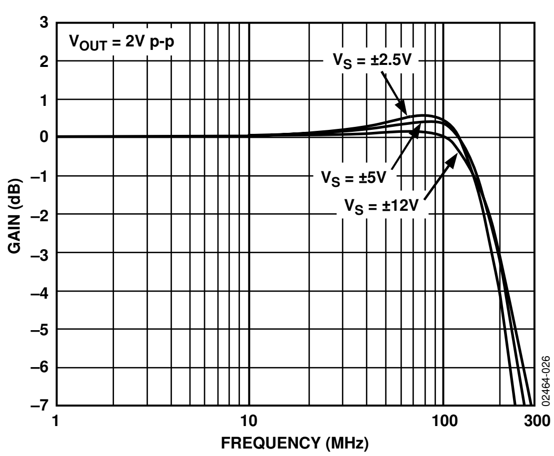


Figure 25. AD8129 Frequency Response vs. Supply, V_{OUT} = 2 V p-p

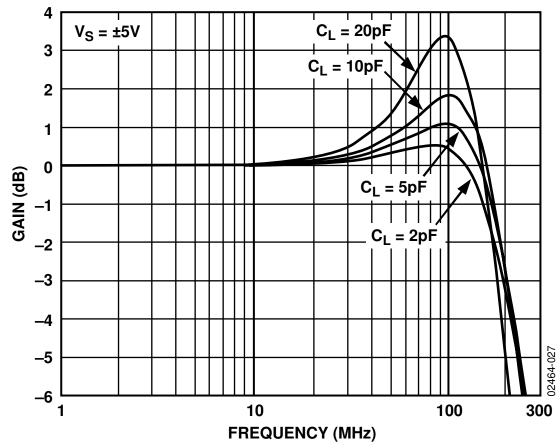


Figure 26. AD8129 Frequency Response vs. Load Capacitance

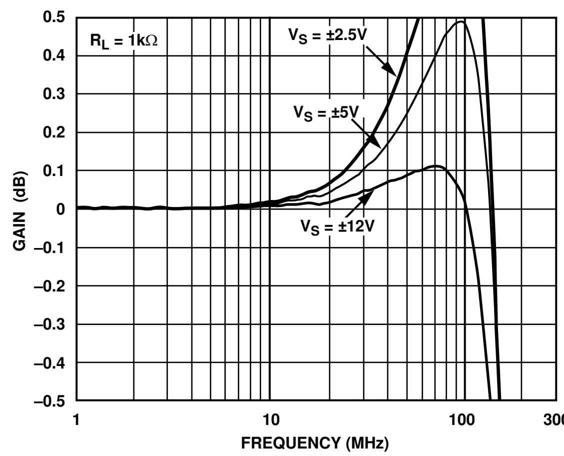


Figure 27. AD8129 Fine Scale Response vs. Supply, R_L = 1 kΩ

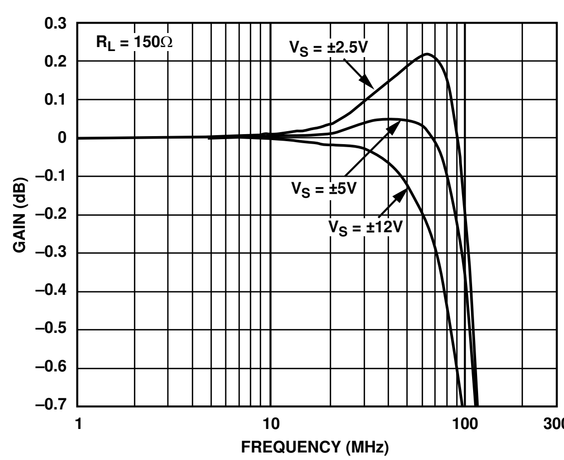


Figure 28. AD8129 Fine Scale Response vs. Supply, R_L = 150 Ω

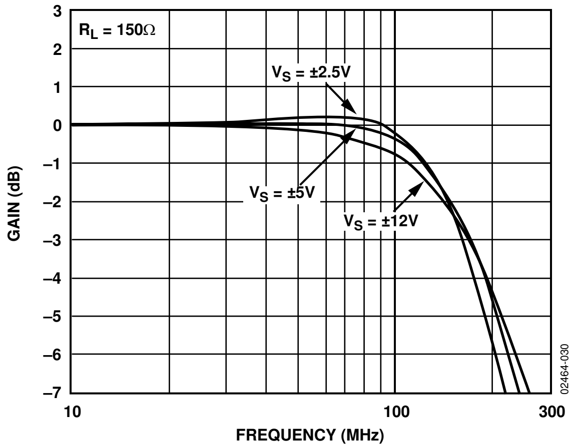


Figure 29. AD8129 Frequency Response vs. Supply, R_L = 150 Ω

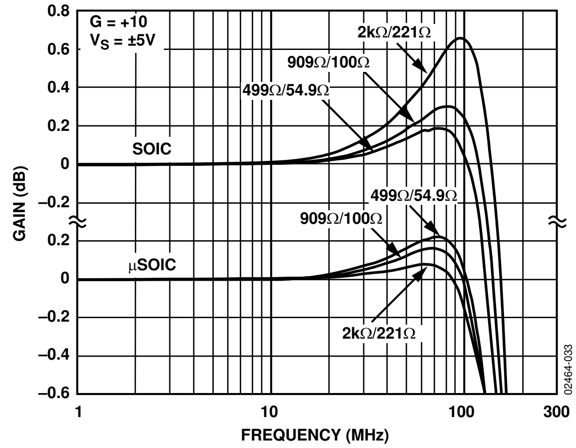


Figure 32. AD8129 Fine Scale Response vs. SOIC and MSOP for Various R_F/R_G

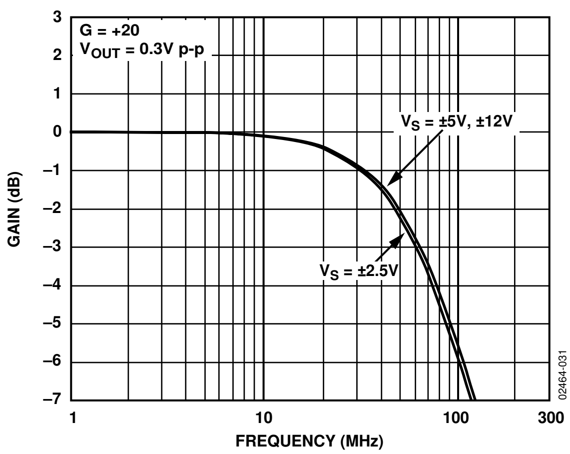


Figure 30. AD8129 Frequency Response vs. Supply, G = +20, V_{OUT} = 0.3 V p-p

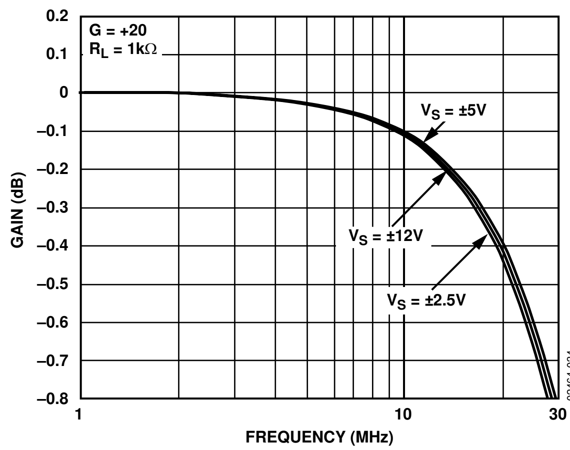


Figure 33. AD8129 Fine Scale Response vs. Supply

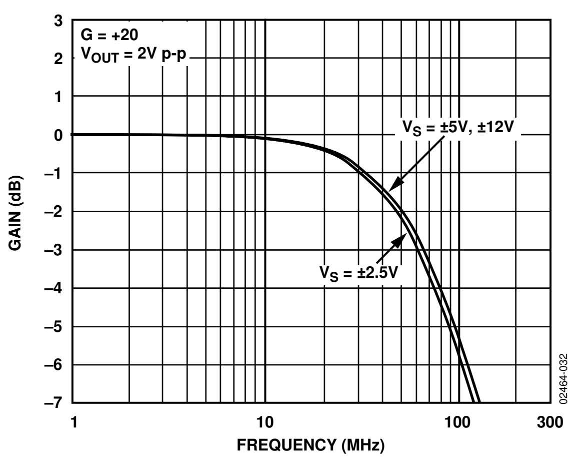


Figure 31. AD8129 Frequency Response vs. Supply, G = +20, V_{OUT} = 2 V p-p

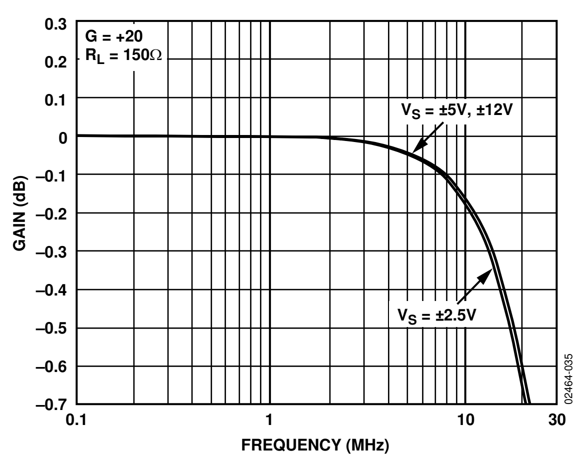


Figure 34. AD8129 Fine Scale Response vs. Supply

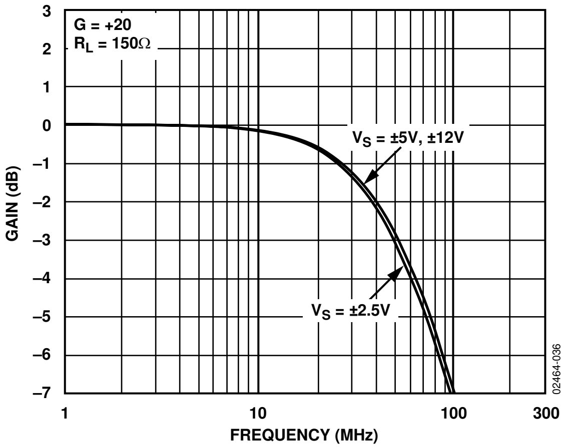


Figure 35. AD8129 Frequency Response vs. Supply, G = +20, R_L = 150 Ω

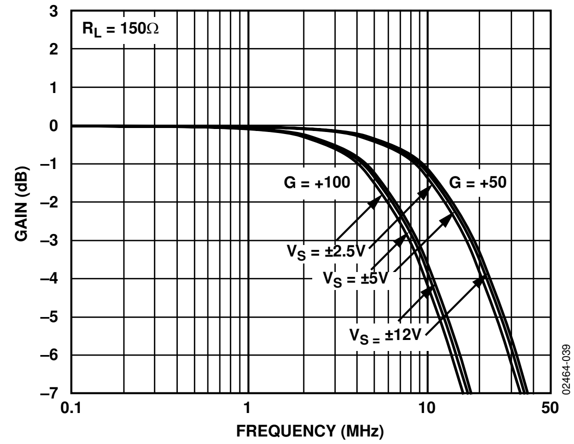


Figure 38. AD8129 Frequency Response vs. Supply, G = +50, G = +100, R_L = 150 Ω

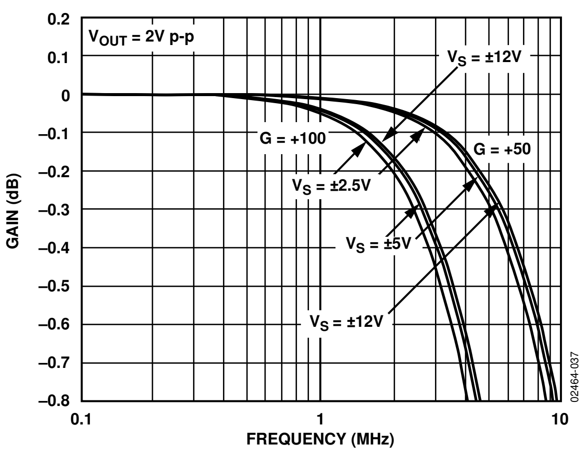


Figure 36. AD8129 Fine Scale Response vs. Supply, G = +50, G = +100, V_{OUT} = 2 V p-p

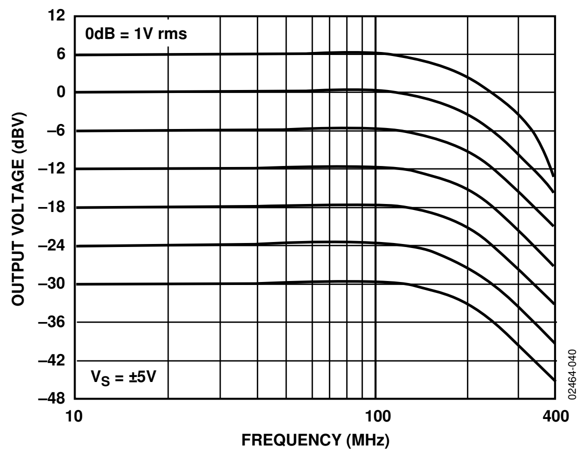


Figure 39. AD8129 Frequency Response for Various Output Levels

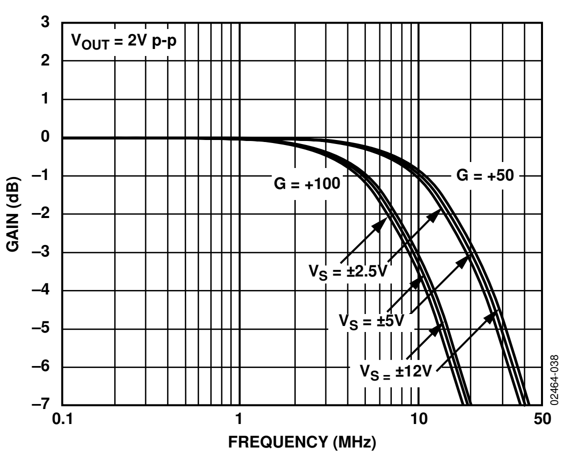
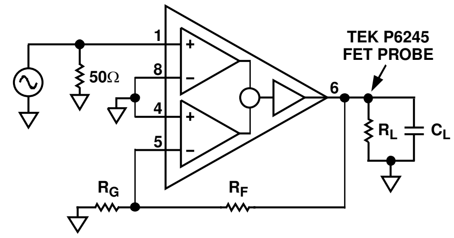


Figure 37. AD8129 Frequency Response vs. Supply, G = +50, G = +100, V_{OUT} = 2 V p-p



G	R_F	R_G
10	2kΩ	221Ω
20	2kΩ	105Ω
50	2kΩ	41.2Ω
100	2kΩ	20Ω

Figure 40. AD8129 Basic Frequency Response Test Circuit

AD8130 HARMONIC DISTORTION CHARACTERISTICS

R_L = 1 kΩ, C_L = 2 pF, T_A = 25°C, unless otherwise noted.

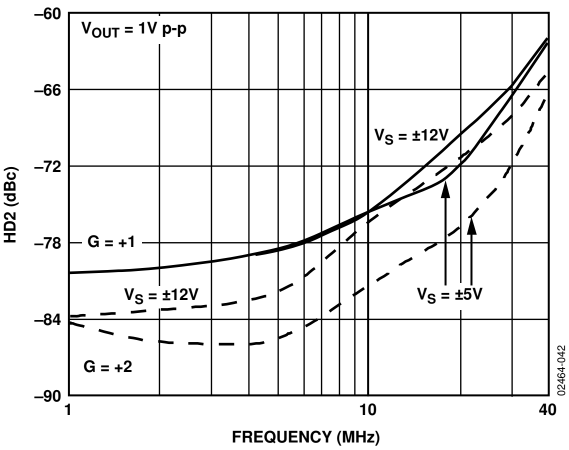


Figure 41. AD8130 Second Harmonic Distortion vs. Frequency

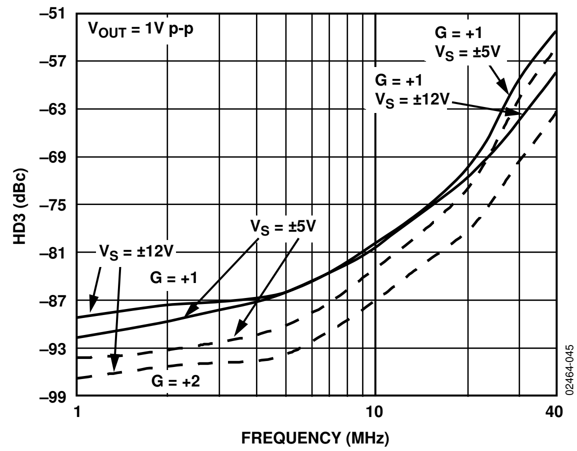


Figure 44. AD8130 Third Harmonic Distortion vs. Frequency

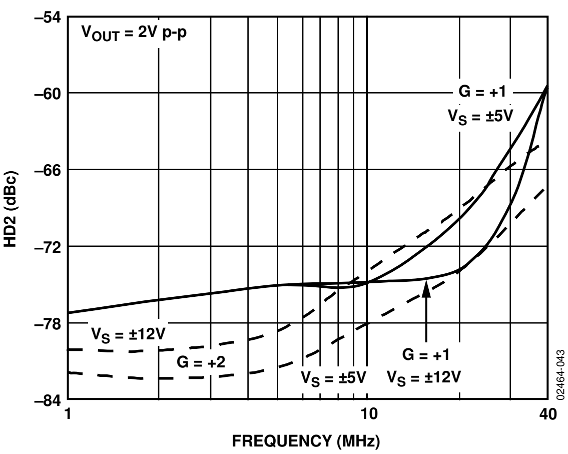


Figure 42. AD8130 Second Harmonic Distortion vs. Frequency

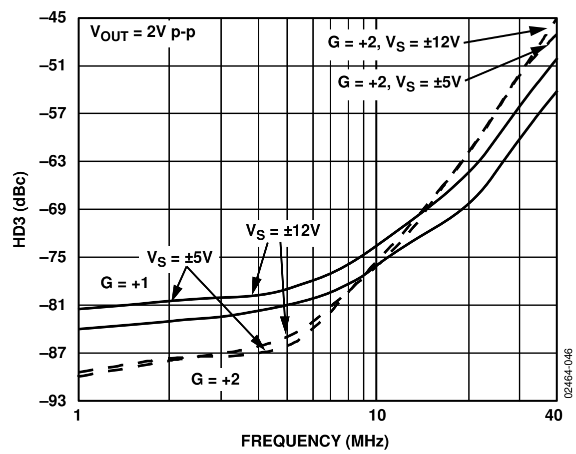


Figure 45. AD8130 Third Harmonic Distortion vs. Frequency

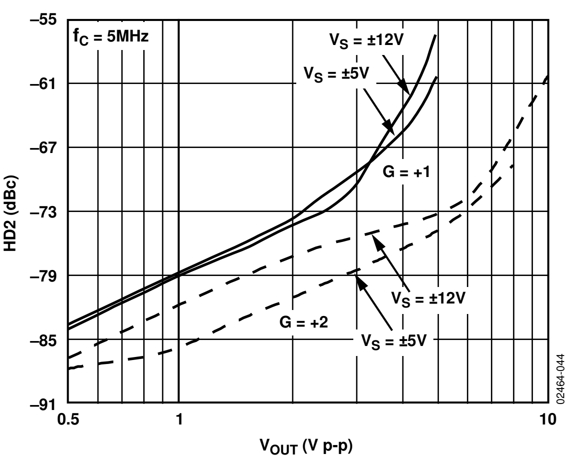


Figure 43. AD8130 Second Harmonic Distortion vs. Output Voltage

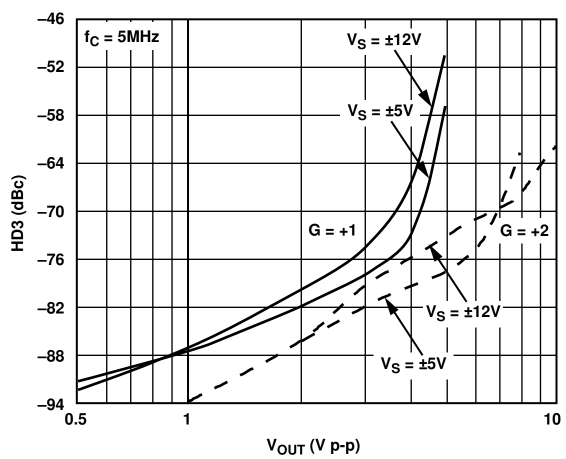


Figure 46. AD8130 Third Harmonic Distortion vs. Output Voltage

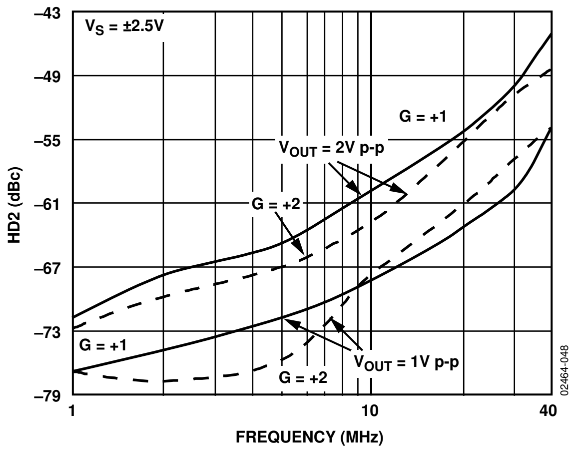


Figure 47. AD8130 Second Harmonic Distortion vs. Frequency

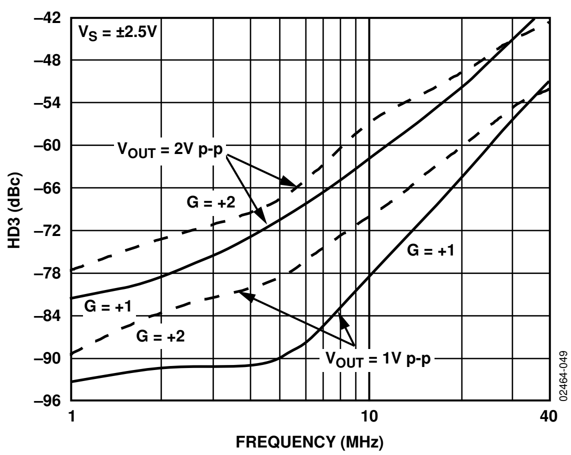


Figure 48. AD8130 Third Harmonic Distortion vs. Frequency

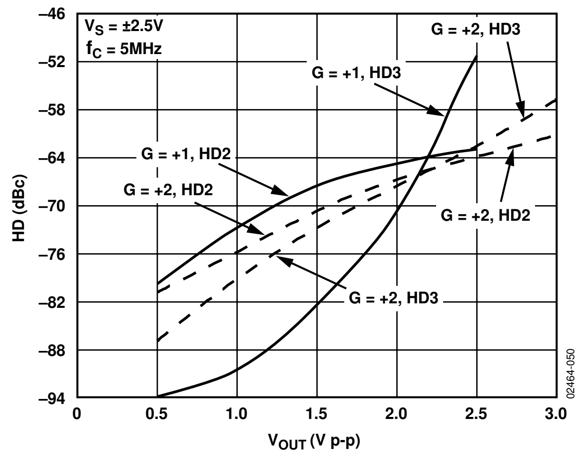


Figure 49. AD8130 Harmonic Distortion vs. Output Voltage

AD8129 HARMONIC DISTORTION CHARACTERISTICS

$R_L = 1\ k\Omega$, $C_L = 2\ pF$, $T_A = 25°C$, unless otherwise noted.

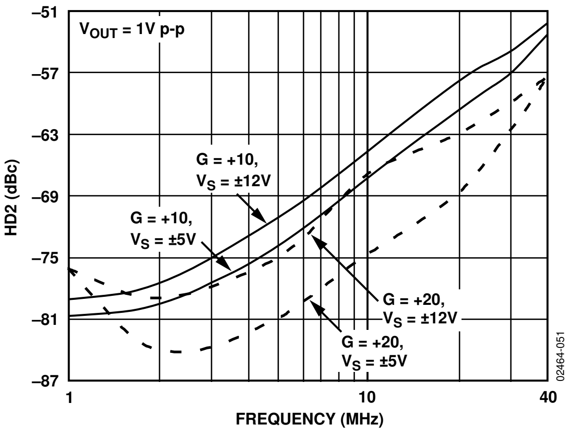


Figure 50. AD8129 Second Harmonic Distortion vs. Frequency

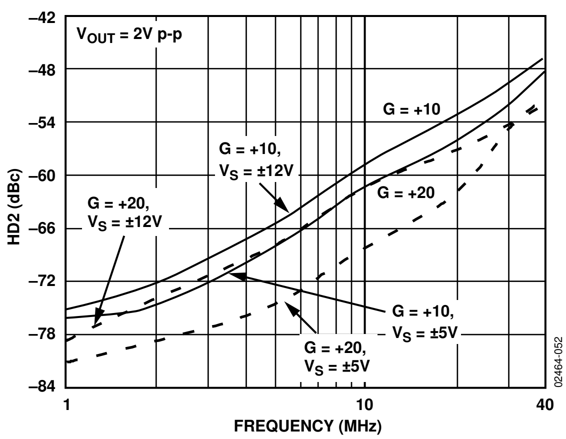


Figure 51. AD8129 Second Harmonic Distortion vs. Frequency

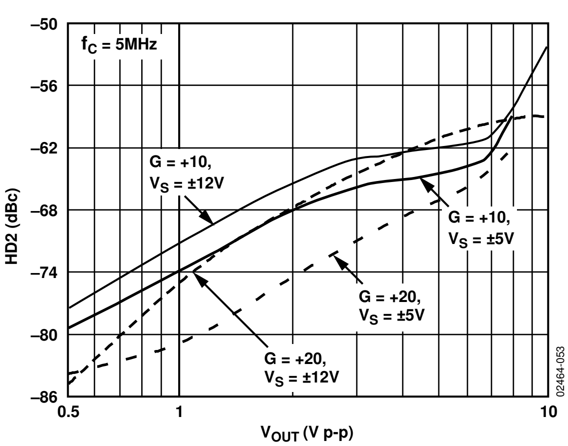


Figure 52. AD8129 Second Harmonic Distortion vs. Output Voltage

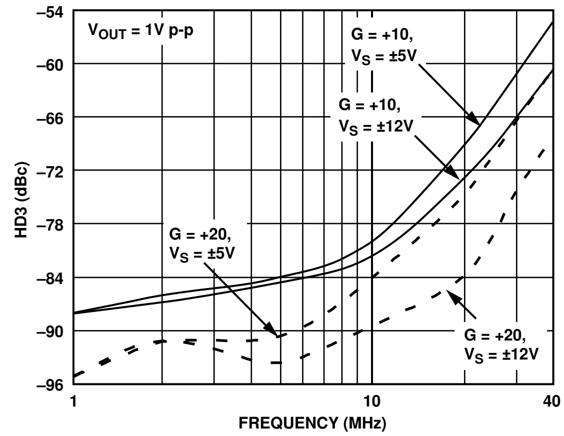


Figure 53. AD8129 Third Harmonic Distortion vs. Frequency

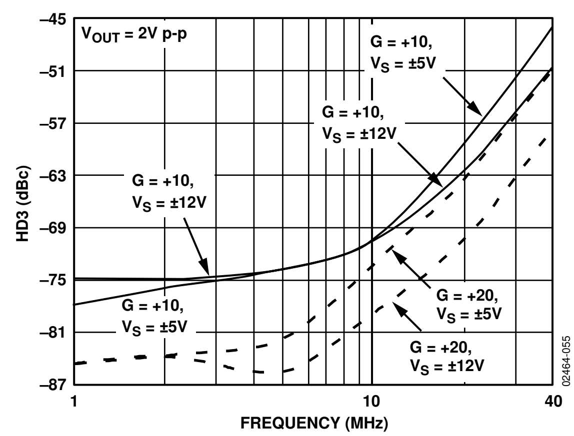


Figure 54. AD8129 Third Harmonic Distortion vs. Frequency

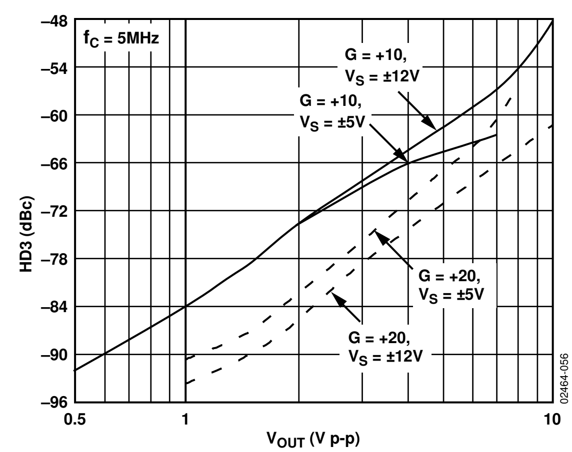


Figure 55. AD8129 Third Harmonic Distortion vs. Output Voltage

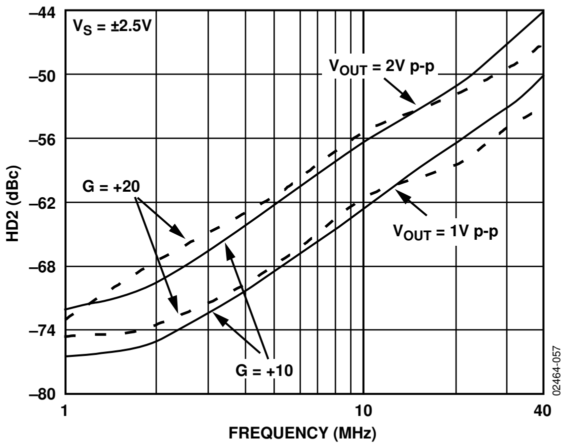


Figure 56. AD8129 Second Harmonic Distortion vs. Frequency

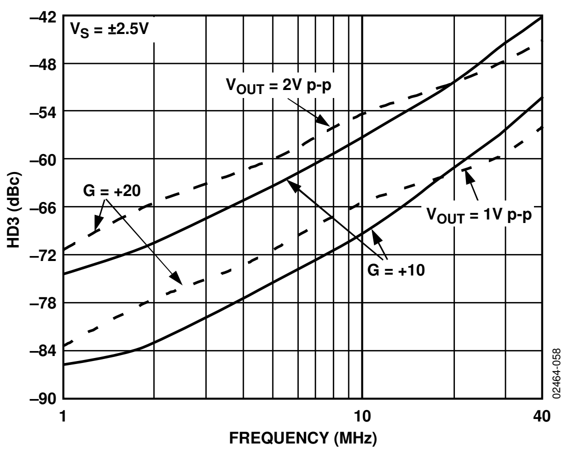


Figure 57. AD8129 Third Harmonic Distortion vs. Frequency

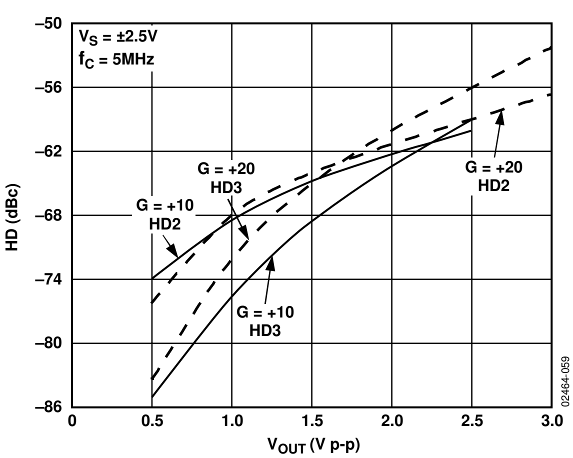


Figure 58. AD8129 Harmonic Distortion vs. Output Voltage

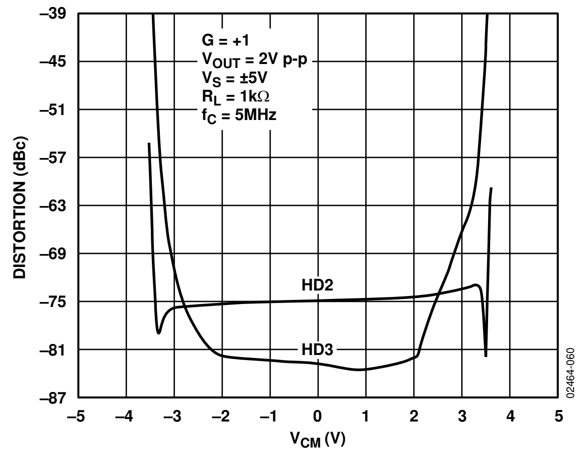


Figure 59. AD8130 Harmonic Distortion vs. Common-Mode Voltage

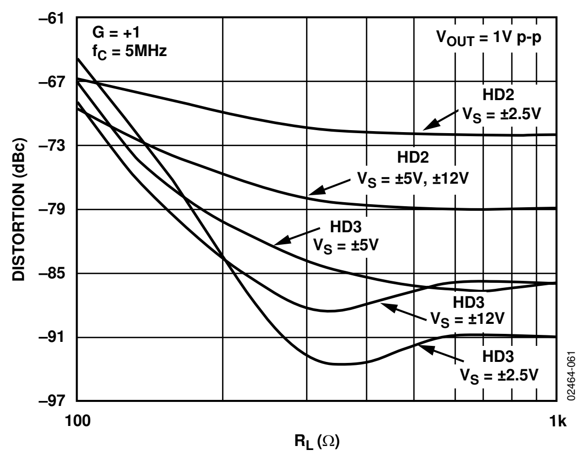


Figure 60. AD8130 Harmonic Distortion vs. Load Resistance

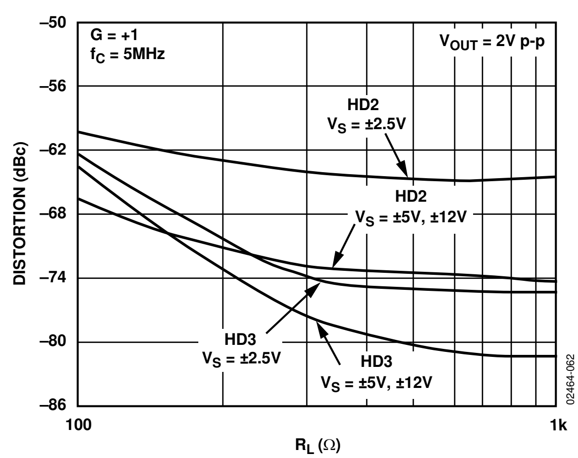


Figure 61. AD8130 Harmonic Distortion vs. Load Resistance

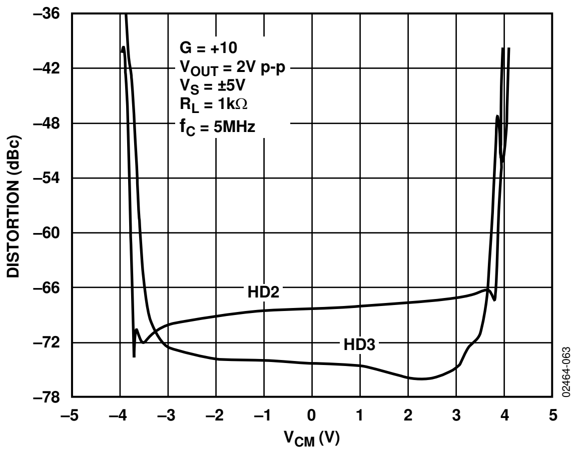


Figure 62. AD8129 Harmonic Distortion vs. Common-Mode Voltage

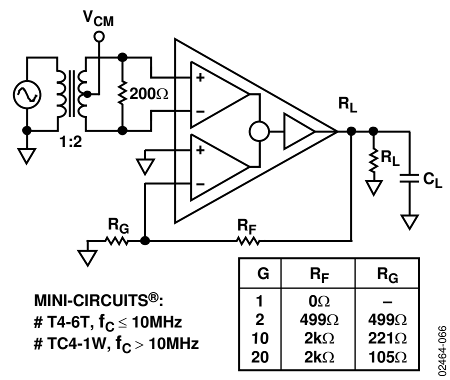


Figure 65. AD8129/AD8130 Basic Distortion Test Circuit, V_{CM} = 0 V, Unless Otherwise Noted

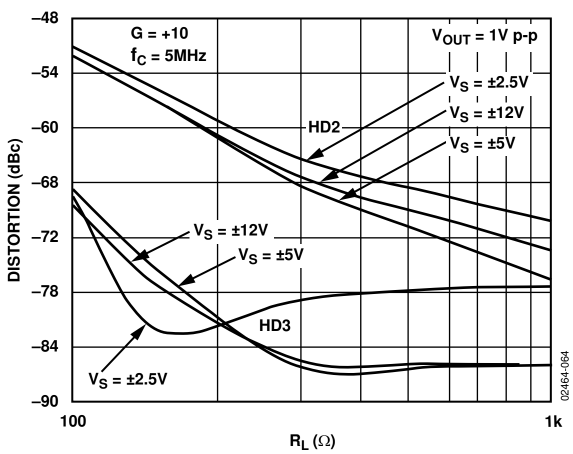


Figure 63. AD8129 Harmonic Distortion vs. Load Resistance

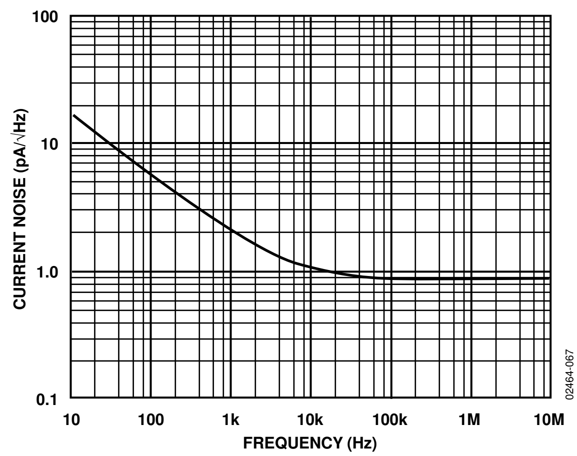


Figure 66. AD8129/AD8130 Input Current Noise vs. Frequency

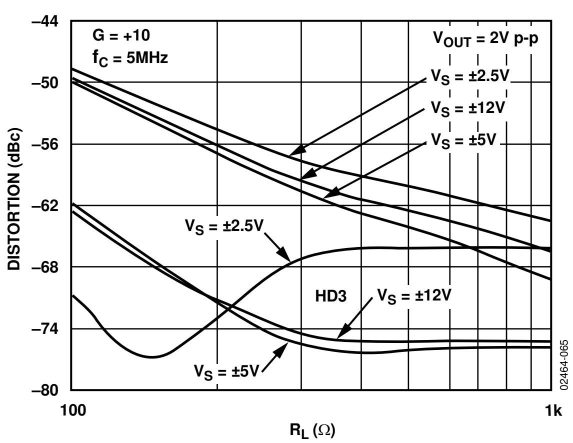


Figure 64. AD8129 Harmonic Distortion vs. Load Resistance

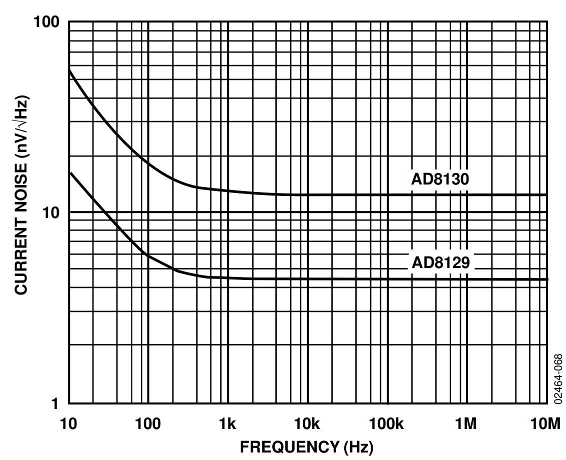


Figure 67. AD8129/AD8130 Input Voltage Noise vs. Frequency

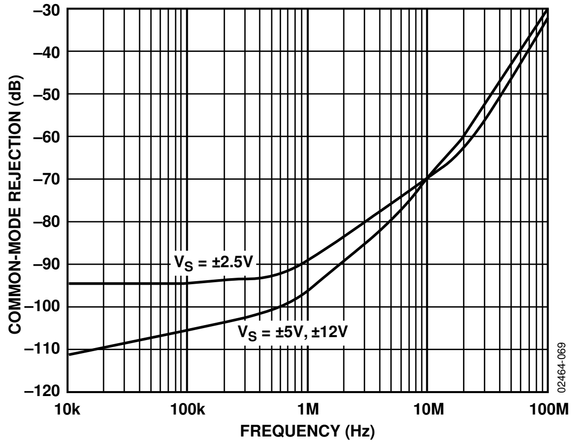


Figure 68. AD8130 Common-Mode Rejection vs. Frequency

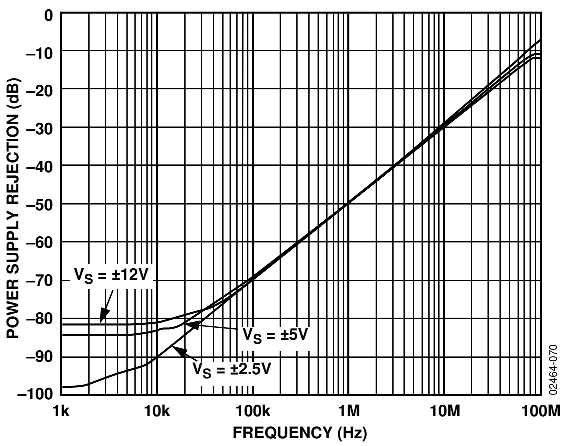


Figure 69. AD8130 Positive Power Supply Rejection vs. Frequency

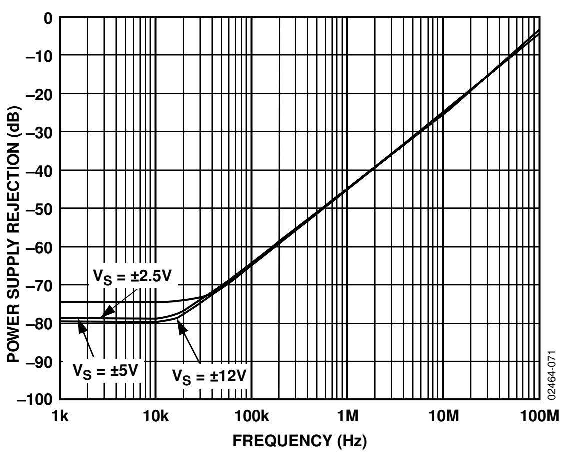


Figure 70. AD8130 Negative Power Supply Rejection vs. Frequency

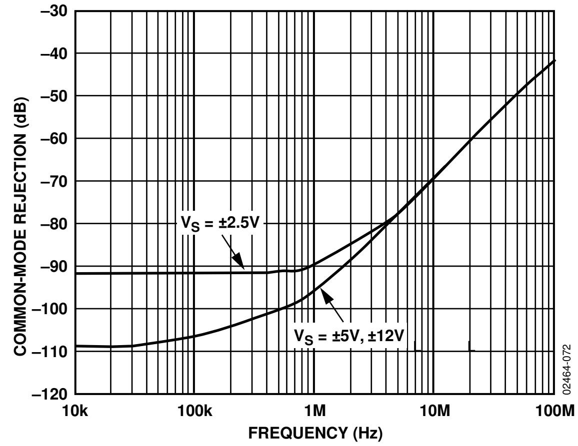


Figure 71. AD8139 Common-Mode Rejection vs. Frequency

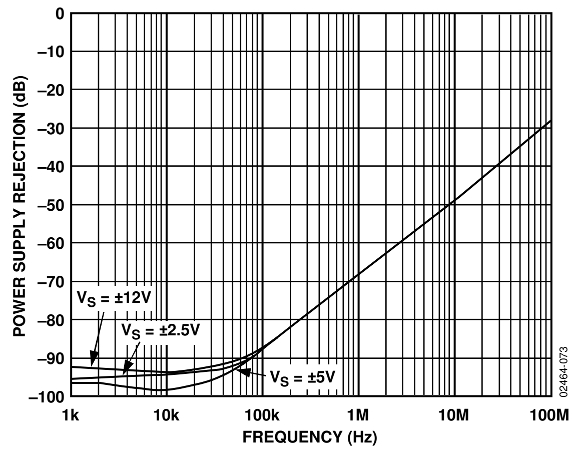


Figure 72. AD8129 Positive Power Supply Rejection vs. Frequency

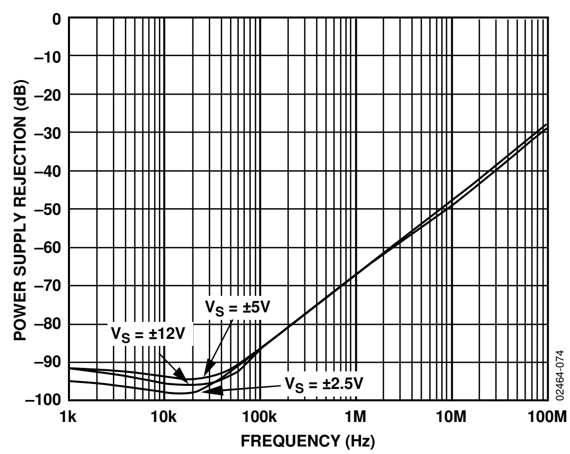


Figure 73. AD8129 Negative Power Supply Rejection vs. Frequency

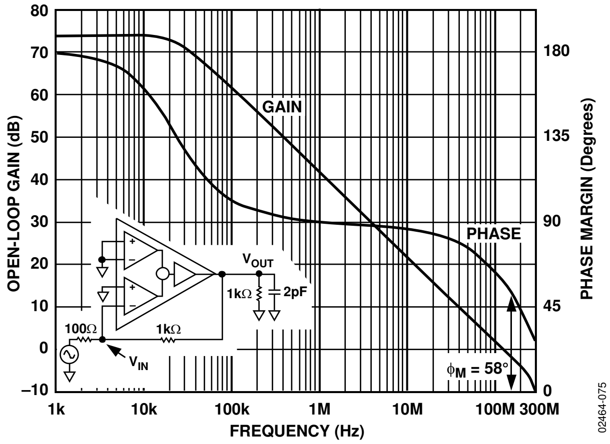


Figure 74. AD8130 Open-Loop Gain and Phase vs. Frequency

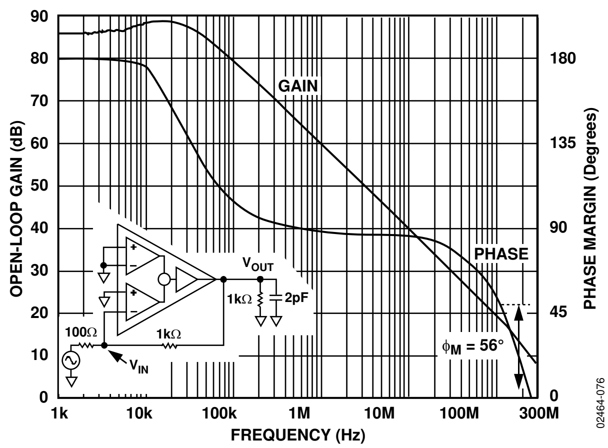


Figure 75. AD8129 Open-Loop Gain and Phase vs. Frequency

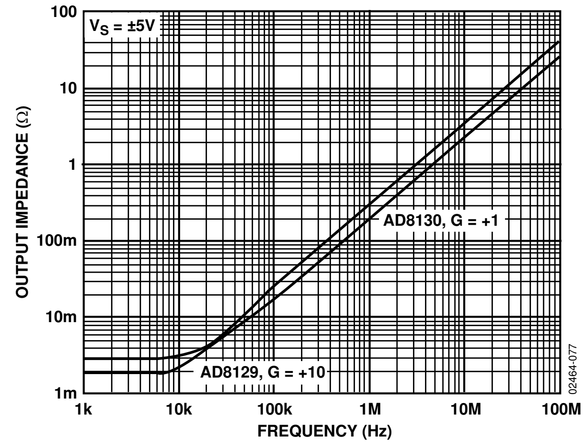


Figure 76. Closed-Loop Output Impedance vs. Frequency

AD8130 TRANSIENT RESPONSE CHARACTERISTICS

G = +1, R_L = 1 kΩ, C_L = 2 pF, V_S = ±5 V, T_A = 25°C, unless otherwise noted.

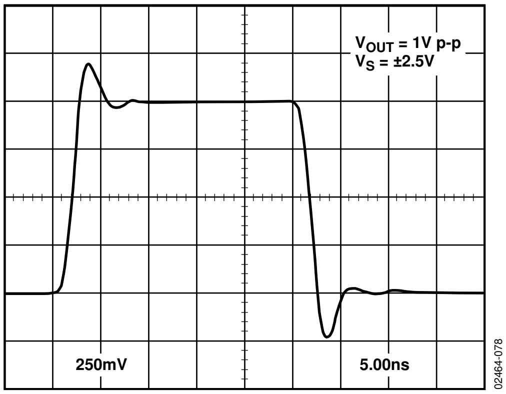


Figure 77. AD8130 Transient Response, V_S = ±2.5 V, V_{OUT} = 1 V p-p

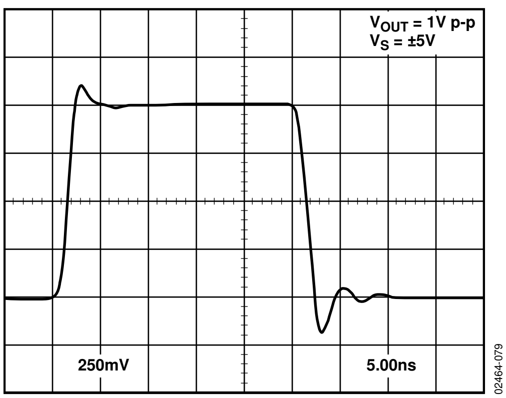


Figure 78. AD8130 Transient Response, V_S = ±5 V, V_{OUT} = 1 V p-p

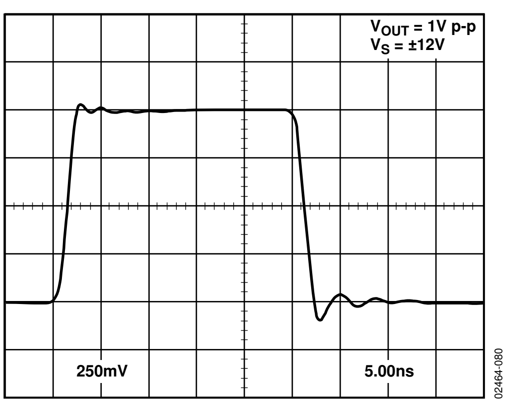


Figure 79. AD8130 Transient Response, V_S = ±12 V, V_{OUT} = 1 V p-p

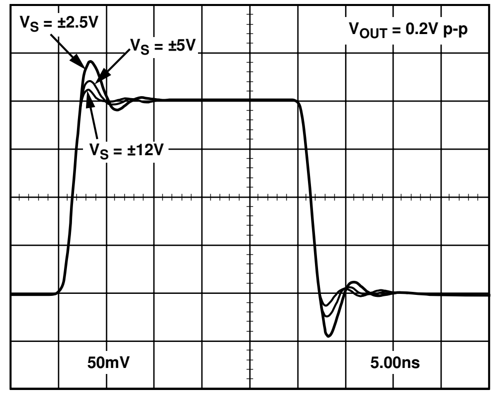


Figure 80. AD8130 Transient Response vs. Supply, V_{OUT} = 0.2 V p-p

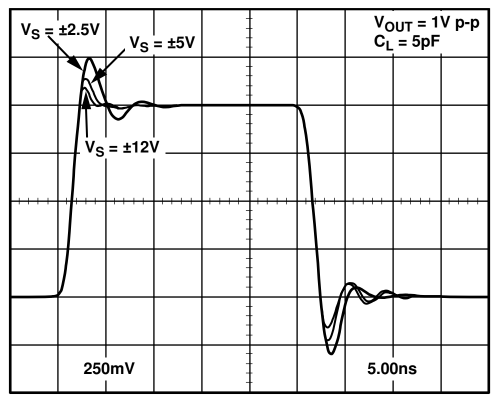


Figure 81. AD8130 Transient Response vs. Supply, V_{OUT} = 1 V p-p, C_L = 5 pF

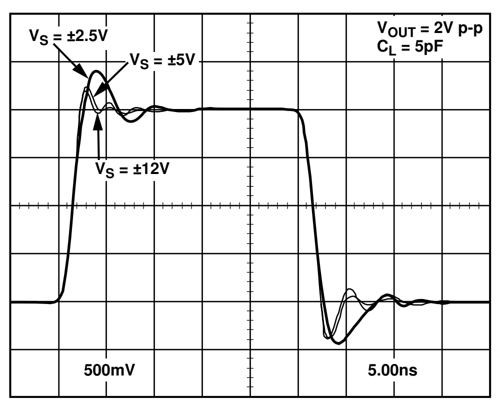


Figure 82. AD8130 Transient Response vs. Supply, V_{OUT} = 2 V p-p, C_L = 5 pF

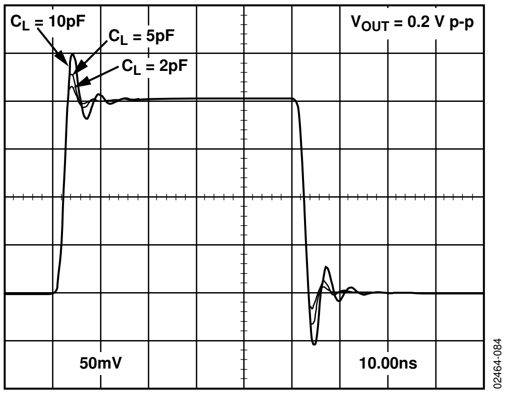


Figure 83. AD8130 Transient Response vs. Load Capacitance, V_{OUT} = 0.2 V p-p

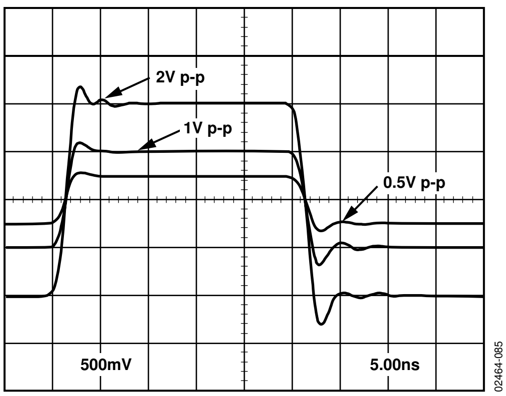


Figure 84. AD8130 Transient Response vs. Output Amplitude, V_{OUT} = 0.5 V p-p, 1 V p-p, 2 V p-p

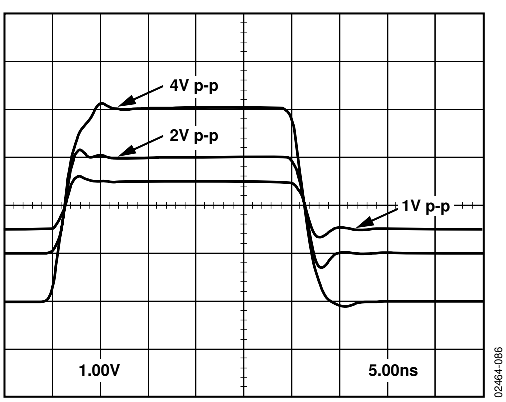


Figure 85. AD8130 Transient Response vs. Output Amplitude, V_{OUT} = 1 V p-p, 2 V p-p, 4 V p-p

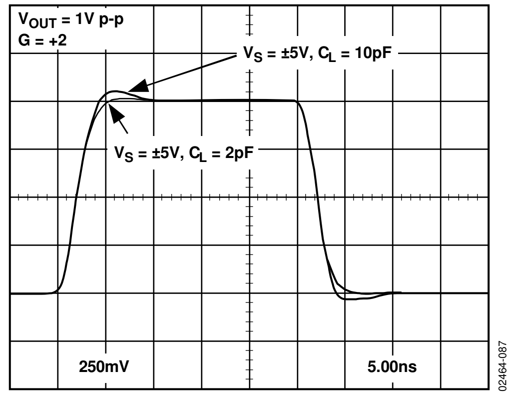


Figure 86. AD8130 Transient Response vs. Load Capacitance, V_{OUT} = 1 V p-p, G = +2

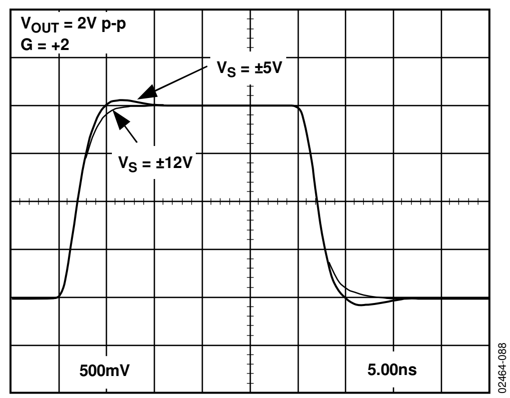


Figure 87. AD8130 Transient Response vs. Supply, V_{OUT} = 2 V p-p, G = +2

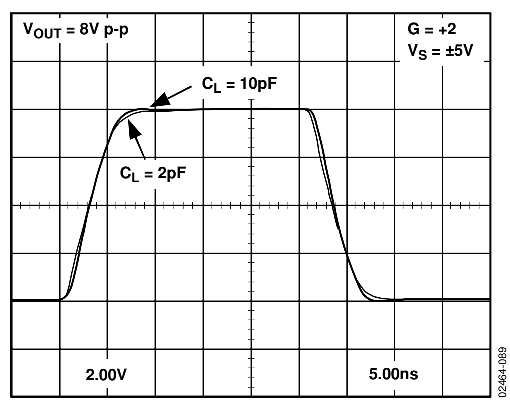


Figure 88. AD8130 Transient Response vs. Load Capacitance, V_{OUT} = 8 V p-p

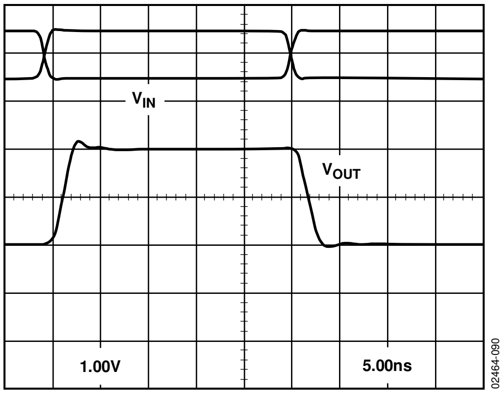


Figure 89. AD8130 Transient Response with +3 V Common-Mode Input

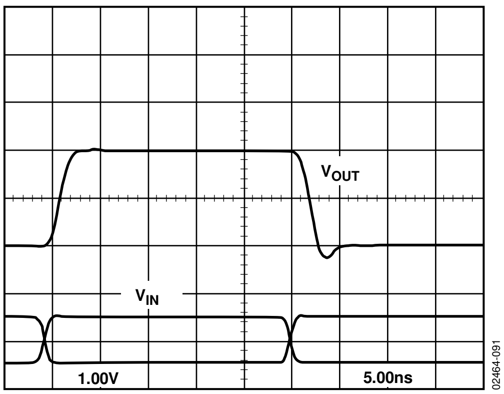


Figure 90. AD8130 Transient Response with −3 V Common-Mode Input

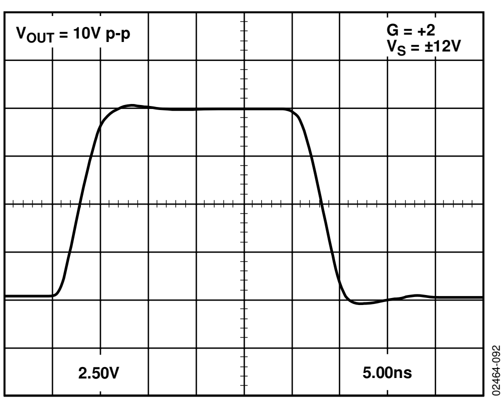


Figure 91. AD8130 Transient Response, V_{OUT} = 10 V p-p, G = +2, V_S = ±12 V

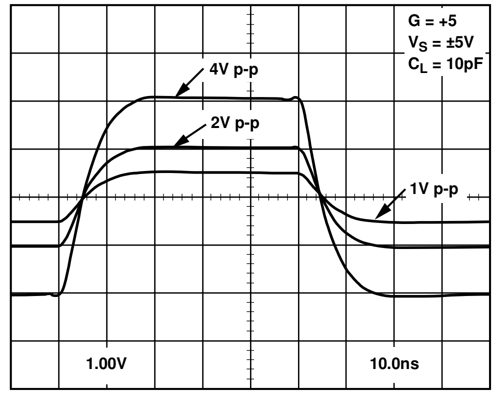


Figure 92. AD8130 Transient Response vs. Output Amplitude

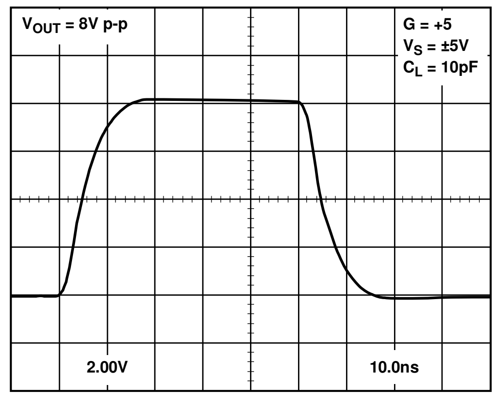


Figure 93. AD8130 Transient Response, V_{OUT} = 8 V p-p, G = +5, V_S = ±5 V

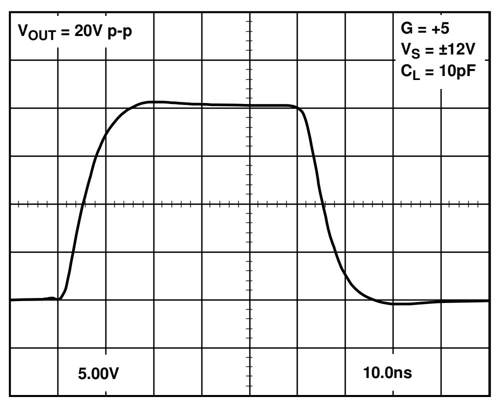


Figure 94. AD8130 Transient Response, V_{OUT} = 20 V p-p, G = +5, V_S = ±12 V