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Low Cost, High Speed Differential Amplifier

AD8132

FEATURES

High speed
- **350 MHz, −3 dB bandwidth**
- **1200 V/µs slew rate**

Resistor set gain
Internal common-mode feedback
Improved gain and phase balance: −68 dB @ 10 MHz
Separate input to set the common-mode output voltage
Low distortion: −99 dBc SFDR @ 5 MHz, 800 Ω load
Low power: 10.7 mA @ 5 V
Power supply range: +2.7 V to ±5.5 V
Fully AEC-Q100 qualified (AD8132W)

APPLICATIONS

Low power differential ADC drivers
Differential gain and differential filtering
Video line drivers
Differential in/out level shifting
Single-ended input to differential output drivers
Active transformers
Automotive driver assistance
Automotive infotainment

GENERAL DESCRIPTION

The AD8132 is a low cost differential or single-ended input to differential output amplifier with resistor set gain. The AD8132 is a major advancement over op amps for driving differential input ADCs or for driving signals over long lines. The AD8132 has a unique internal feedback feature that provides output gain and phase matching balanced to −68 dB at 10 MHz, suppressing harmonics and reducing radiated EMI.

Manufactured using the next-generation of Analog Devices, Inc., XFCB bipolar process, the AD8132 has a −3 dB bandwidth of 350 MHz and delivers a differential signal with −99 dBc SFDR at 5 MHz, despite its low cost. The AD8132 eliminates the need for a transformer with high performance ADCs, preserving the low frequency and dc information. The common-mode level of the differential output is adjustable by applying a voltage on the V_{OCM} pin, easily level shifting the input signals for driving single-supply ADCs. Fast overload recovery preserves sampling accuracy.

CONNECTION DIAGRAM

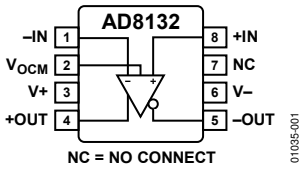

Figure 1.

The AD8132 is also used as a differential driver for the transmission of high speed signals over low cost twisted pair or coaxial cables. The feedback network can be adjusted to boost the high frequency components of the signal. The AD8132 is used for either analog or digital video signals or for other high speed data transmission. The AD8132 is capable of driving either a Category 3 or Category 5 twisted pair or coaxial cable with minimal line attenuation. The AD8132 has considerable cost and performance improvements over discrete line driver solutions.

Differential signal processing reduces the effects of ground noise that plagues ground-referenced systems. The AD8132 can be used for differential signal processing (gain and filtering) throughout a signal chain, easily simplifying the conversion between differential and single-ended components.

The AD8132W is the automotive grade version, qualified for 125°C operation per the AEC-Q100. See the Automotive Products section for more details.

The AD8132 is available in both 8-lead SOIC and 8-lead MSOP packages for operation over the extended industrial temperature range of −40°C to +125°C.

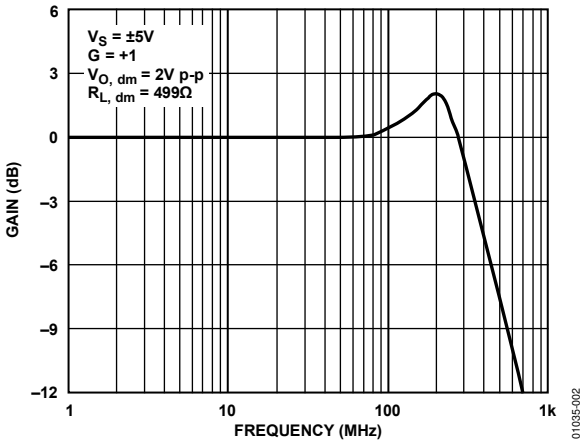

Figure 2. Large Signal Frequency Response

Rev. I

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

AD8132* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- Universal Evaluation Board for Single Differential Amplifiers

DOCUMENTATION

Application Notes

- AN-0990: Terminating a Differential Amplifier in Single-Ended Input Applications
- AN-0992: Active Filter Evaluation Board for Differential Amplifiers
- AN-1026: High Speed Differential ADC Driver Design Considerations
- AN-1363: Meeting Biasing Requirements of Externally Biased RF/Microwave Amplifiers with Active Bias Controllers
- AN-282: Fundamentals of Sampled Data Systems
- AN-584: Using the AD813X Differential Amplifier
- AN-589: Ways to Optimize the Performance of a Difference Amplifier
- AN-649: Using the Analog Devices Active Filter Design Tool

Data Sheet

- AD8132: Low-Cost, High Speed Differential Amplifier Data Sheet

User Guides

- UG-474: Evaluation Board for Differential Amplifiers Offered in 8-Lead SOIC Packages
- UG-888: Evaluation Board for Differential Amplifiers Offered in 8-Lead MSOP Packages

TOOLS AND SIMULATIONS

- ADI DiffAmpCalc™
- AD8132 SPICE Macro-Model

REFERENCE MATERIALS

Product Selection Guide

- Amplifiers for Video Distribution
- High Speed Amplifiers Selection Table

Tutorials

- MT-075: Differential Drivers for High Speed ADCs Overview
- MT-076: Differential Driver Analysis
- MT-218: Multiple Feedback Band-Pass Design Example

DESIGN RESOURCES

- AD8132 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD8132 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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1/02—Rev. A to Rev. B

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SPECIFICATIONS

±D_{IN} TO ±OUT SPECIFICATIONS

At T_A = 25°C, V_S = ±5 V, V_{OCM} = 0 V, G = +1, $R_{L, dm}$ = 499 Ω, R_F = R_G = 348 Ω, unless otherwise noted. For G = +2, $R_{L, dm}$ = 200 Ω, R_F = 1000 Ω, R_G = 499 Ω. Refer to Figure 56 and Figure 57 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Large Signal Bandwidth	V_{OUT} = 2 V p-p	300	350		MHz
	AD8132W only, T_{MIN} to T_{MAX}	280			MHz
	V_{OUT} = 2 V p-p, G = +2		190		MHz
−3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p		360		MHz
	V_{OUT} = 0.2 V p-p, G = +2		160		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.2 V p-p		90		MHz
	V_{OUT} = 0.2 V p-p, G = +2		50		MHz
Slew Rate	V_{OUT} = 2 V p-p	1000	1200		V/µs
	AD8132W only, T_{MIN} to T_{MAX}	950			V/µs
Settling Time	0.1%, V_{OUT} = 2 V p-p		15		ns
Overdrive Recovery Time	V_{IN} = 5 V to 0 V step, G = +2		5		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 2 V p-p, 1 MHz, $R_{L, dm}$ = 800 Ω		−96		dBc
	V_{OUT} = 2 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		−83		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		−73		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 1 MHz, $R_{L, dm}$ = 800 Ω		−102		dBc
	V_{OUT} = 2 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		−98		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		−67		dBc
IMD	20 MHz, $R_{L, dm}$ = 800 Ω		−76		dBc
IP3	20 MHz, $R_{L, dm}$ = 800 Ω		40		dBm
Input Voltage Noise (RTI)	f = 0.1 MHz to 100 MHz		8		nV/√Hz
Input Current Noise	f = 0.1 MHz to 100 MHz		1.8		pA/√Hz
Differential Gain Error	NTSC, G = +2, $R_{L, dm}$ = 150 Ω		0.01		%
Differential Phase Error	NTSC, G = +2, $R_{L, dm}$ = 150 Ω		0.10		Degrees
INPUT CHARACTERISTICS					
Offset Voltage (RTI)	$V_{OS, dm}$ = $V_{OUT, dm}$/2; V_{DIN+} = V_{DIN-} = V_{OCM} = 0 V		±1.0	±3.5	mV
	AD8132W only, T_{MIN} to T_{MAX}			±6	mV
	T_{MIN} to T_{MAX} variation		10		µV/°C
Input Bias Current	T_A = 25°C		3	7	µA
	AD8132W only, T_{MIN} to T_{MAX}			8	µA
Input Resistance	Differential		12		MΩ
	Common mode		3.5		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			−4.7 to +3.0		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = ±1 V; resistors matched to 0.01%		−70	−60	dB
	AD8132W only, T_{MIN} to T_{MAX}			−60	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; single-ended output		−3.6 to +3.6		V
Output Current			+70		mA
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V		−70		dB

V_{OCM} TO ±OUT SPECIFICATIONS

At T_A = 25°C, V_S = ±5 V, V_{OCM} = 0 V, G = +1, $R_{L, dm}$ = 499 Ω, R_F = R_G = 348 Ω, unless otherwise noted. For G = +2, $R_{L, dm}$ = 200 Ω, R_F = 1000 Ω, R_G = 499 Ω. Refer to Figure 56 and Figure 57 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	ΔV_{OCM} = 600 mV p-p		210		MHz
Slew Rate	ΔV_{OCM} = −1 V to +1 V		400		V/µs
Input Voltage Noise (RTI)	f = 0.1 MHz to 100 MHz		12		nV/√Hz
DC PERFORMANCE					
Input Voltage Range			±3.6		V
Input Resistance			50		kΩ
Input Offset Voltage	$V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 0 V		±1.5	±7	mV
	AD8132W only, T_{MIN} to T_{MAX}			±9	mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V; resistors matched to 0.01%		−68		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V	0.985	1	1.015	V/V
	AD8132W only, T_{MIN} to T_{MAX}	0.985		1.015	V/V
POWER SUPPLY					
Operating Range		±1.35		±5.5	V
Quiescent Current	$V_{DIN+} = V_{DIN-} = V_{OCM}$ = 0 V	11	12	13	mA
	AD8132W only, T_{MIN} to T_{MAX}	9		14.5	mA
	T_{MIN} to T_{MAX} variation		16		µA/°C
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ±1 V		−70	−60	dB
	AD8132W only, T_{MIN} to T_{MAX}			−60	dB
OPERATING TEMPERATURE RANGE		−40		+125	°C

±D_{IN} TO ±OUT SPECIFICATIONS

At T_A = 25°C, V_S = 5 V, V_{OCM} = 2.5 V, G = +1, $R_{L, dm}$ = 499 Ω, R_F = R_G = 348 Ω, unless otherwise noted. For G = +2, $R_{L, dm}$ = 200 Ω, R_F = 1000 Ω, R_G = 499 Ω. Refer to Figure 56 and Figure 57 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Large Signal Bandwidth	V_{OUT} = 2 V p-p	250	300		MHz
	AD8132W only, T_{MIN} to T_{MAX}	240			MHz
	V_{OUT} = 2 V p-p, G = +2		180		MHz
−3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p		360		MHz
	V_{OUT} = 0.2 V p-p, G = +2		155		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.2 V p-p		65		MHz
	V_{OUT} = 0.2 V p-p, G = +2		50		MHz
Slew Rate	V_{OUT} = 2 V p-p	800	1000		V/µs
	AD8132W only, T_{MIN} to T_{MAX}	750			V/µs
Settling Time	0.1%, V_{OUT} = 2 V p-p		20		ns
Overdrive Recovery Time	V_{IN} = 2.5 V to 0 V step, G = +2		5		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 2 V p-p, 1 MHz, $R_{L, dm}$ = 800 Ω		−97		dBc
	V_{OUT} = 2 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		−100		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		−74		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 1 MHz, $R_{L, dm}$ = 800 Ω		−100		dBc
	V_{OUT} = 2 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		−99		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		−67		dBc
IMD	20 MHz, $R_{L, dm}$ = 800 Ω		−76		dBc
IP3	20 MHz, $R_{L, dm}$ = 800 Ω		40		dBm
Input Voltage Noise (RTI)	f = 0.1 MHz to 100 MHz		8		nV/√Hz
Input Current Noise	f = 0.1 MHz to 100 MHz		1.8		pA/√Hz
Differential Gain Error	NTSC, G = +2, $R_{L, dm}$ = 150 Ω		0.025		%
Differential Phase Error	NTSC, G = +2, $R_{L, dm}$ = 150 Ω		0.15		Degrees
INPUT CHARACTERISTICS					
Offset Voltage (RTI)	$V_{OS, dm}$ = $V_{OUT, dm}$/2; V_{DIN+} = V_{DIN-} = V_{OCM} = 2.5 V		±1.0	±3.5	mV
	AD8132W only, T_{MIN} to T_{MAX}			±6	mV
	T_{MIN} to T_{MAX} variation		6		µV/°C
Input Bias Current	T_A = 25°C		3	7	µA
				8	µA
Input Resistance	Differential AD8132W only, T_{MIN} to T_{MAX}		10		MΩ
	Common-mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			0.3 to 3.0		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = ±1 V; resistors matched to 0.01%		−70	−60	dB
	AD8132W only, T_{MIN} to T_{MAX}			−60	dB
OUTPUT CHARACTERISTICS	AD8132W only, T_{MIN} to T_{MAX}				
Output Voltage Swing	Maximum ΔV_{OUT}; single-ended output		1.0 to 4.0		V
Output Current			50		mA
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V		−68		dB

V_{OCM} TO ±OUT SPECIFICATIONS

At T_A = 25°C, V_S = 5 V, V_{OCM} = 2.5 V, G = +1, $R_{L, dm}$ = 499 Ω, R_F = R_G = 348 Ω, unless otherwise noted. For G = +2, $R_{L, dm}$ = 200 Ω, R_F = 1000 Ω, R_G = 499 Ω. Refer to Figure 56 and Figure 57 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 4.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	ΔV_{OCM} = 600 mV p-p		210		MHz
Slew Rate	ΔV_{OCM} = 1.5 V to 3.5 V		340		V/µs
Input Voltage Noise (RTI)	f = 0.1 MHz to 100 MHz		12		nV/√Hz
DC PERFORMANCE					
Input Voltage Range			1.0 to 3.7		V
Input Resistance			30		kΩ
Input Offset Voltage	$V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 2.5 V		±5	±11	mV
	AD8132W only, T_{MIN} to T_{MAX}			±13	mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = 2.5 V ±1 V; resistors matched to 0.01%		−66		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = 2.5 V ±1 V	0.985	1	1.015	V/V
	AD8132W only, T_{MIN} to T_{MAX}	0.985		1.015	V/V
POWER SUPPLY					
Operating Range		2.7		11	V
Quiescent Current	$V_{DIN+} = V_{DIN-} = V_{OCM}$ = 2.5 V	9.4	10.7	12	mA
	AD8132W only, T_{MIN} to T_{MAX}	6		13	mA
	T_{MIN} to T_{MAX} variation		10		µA/°C
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ±1 V		−70	−60	dB
	AD8132W only, T_{MIN} to T_{MAX}			−60	dB
OPERATING TEMPERATURE RANGE		−40		+125	°C

±D_{IN} TO ±OUT SPECIFICATIONS

At T_A = 25°C, V_S = 3 V, V_{OCM} = 1.5 V, G = +1, $R_{L, dm}$ = 499 Ω, R_F = R_G = 348 Ω, unless otherwise noted. For G = +2, $R_{L, dm}$ = 200 Ω, R_F = 1000 Ω, R_G = 499 Ω. Refer to Figure 56 and Figure 57 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 5.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Large Signal Bandwidth	V_{OUT} = 1 V p-p		350		MHz
	V_{OUT} = 1 V p-p, G = +2		165		MHz
−3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p		350		MHz
	V_{OUT} = 0.2 V p-p, G = +2		150		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.2 V p-p		45		MHz
	V_{OUT} = 0.2 V p-p, G = +2		50		MHz
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 1 V p-p, 1 MHz, $R_{L, dm}$ = 800 Ω		−100		dBc
	V_{OUT} = 1 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		−94		dBc
	V_{OUT} = 1 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		−77		dBc
Third Harmonic	V_{OUT} = 1 V p-p, 1 MHz, $R_{L, dm}$ = 800 Ω		−90		dBc
	V_{OUT} = 1 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		−85		dBc
	V_{OUT} = 1 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		−66		dBc
INPUT CHARACTERISTICS					
Offset Voltage (RTI)	$V_{OS, dm}$ = $V_{OUT, dm}$/2; V_{DIN+} = $V_{DIN−}$ = V_{OCM} = 1.5 V		±10		mV
Input Bias Current			3		μA
Input Common-Mode Voltage			0.3 to 1.0		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = ±0.5 V; resistors matched to 0.01%		−60		dB

V_{OCM} TO ±OUT SPECIFICATIONS

At T_A = 25°C, V_S = 3 V, V_{OCM} = 1.5 V, G = +1, $R_{L, dm}$ = 499 Ω, R_F = R_G = 348 Ω, unless otherwise noted. For G = +2, $R_{L, dm}$ = 200 Ω, R_F = 1000 Ω, R_G = 499 Ω. Refer to Figure 56 and Figure 57 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 6.

Parameter	Conditions	Min	Typ	Max	Unit
DC PERFORMANCE					
Input Offset Voltage	$V_{OS, cm}$ = $V_{OUT, cm}$; V_{DIN+} = $V_{DIN−}$ = V_{OCM} = 1.5 V		±7		mV
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±0.5 V		1		V/V
POWER SUPPLY					
Operating Range		2.7		11	V
Quiescent Current	V_{DIN+} = $V_{DIN−}$ = V_{OCM} = 0 V		7.25		mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ±0.5 V		−70		dB
OPERATING TEMPERATURE RANGE		−40		+125	°C

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Supply Voltage	±5.5 V
V_{OCM}	$\pm V_S$
Internal Power Dissipation	250 mW
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered in a circuit board in still air.

Table 8.

Package Type	θ_{JA}	Unit
8-Lead SOIC, 4-Layer	121	°C/W
8-Lead MSOP, 4-Layer	142	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8132 packages is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8132. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The load current consists of the differential and common-mode currents flowing to the load, as well as currents flowing through the external feedback networks and the internal common-mode feedback loop. The internal resistor tap used in the common-mode feedback loop places a 1 kΩ differential load on the output. Consider rms voltages and currents when dealing with ac signals.

Airflow reduces θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces through holes, ground, and power planes reduces the θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8-lead SOIC (θ_{JA} = 121°C/W) and 8-lead MSOP (θ_{JA} = 142°C/W) packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

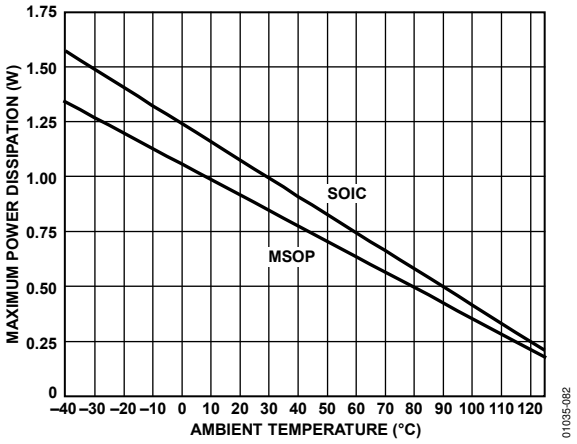

Figure 3. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

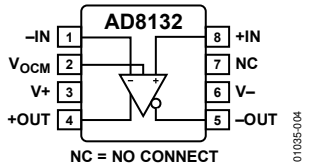

Figure 4. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN	Negative Input.
2	V_{OCM}	Voltage applied to this pin sets the common-mode output voltage with a ratio of 1:1. For example, 1 V dc on V_{OCM} sets the dc bias level on +OUT and −OUT to 1 V.
3	V+	Positive Supply Voltage.
4	+OUT	Positive Output. Note that the voltage at $-D_{IN}$ is inverted at +OUT (see Figure 64).
5	−OUT	Negative Output. Note that the voltage at $+D_{IN}$ is inverted at −OUT (see Figure 64).
6	V−	Negative Supply Voltage.
7	NC	No Connect.
8	+IN	Positive Input.

TYPICAL PERFORMANCE CHARACTERISTICS

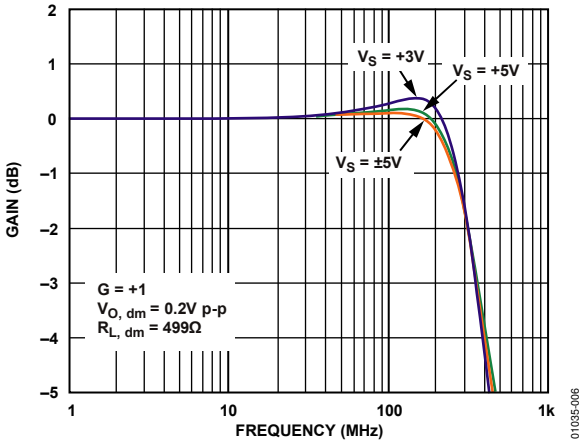

Figure 5. Small Signal Frequency Response (See Figure 56)

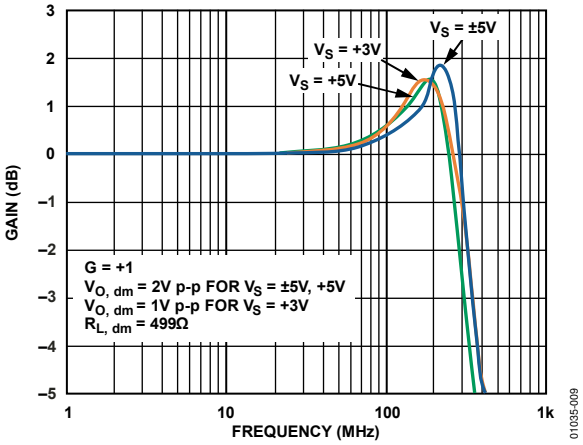

Figure 8. Large Signal Frequency Response; C_F = 0 pF (See Figure 56)

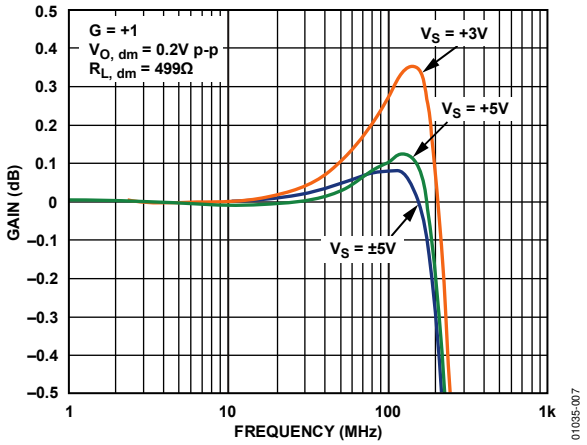

Figure 6. 0.1 dB Flatness vs. Frequency; C_F = 0 pF (See Figure 56)

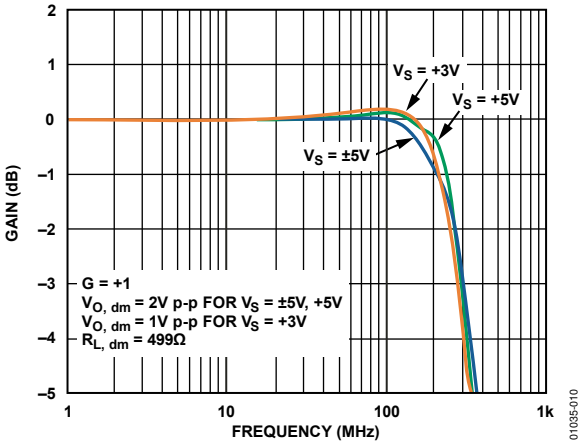

Figure 9. Large Signal Frequency Response; C_F = 0.5 pF (See Figure 56)

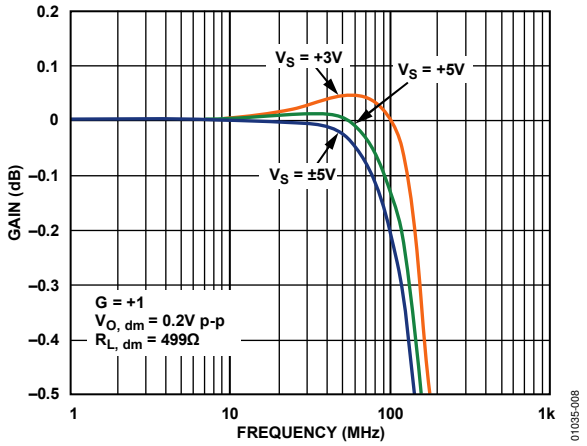

Figure 7. 0.1 dB Flatness vs. Frequency; C_F = 0.5 pF (See Figure 56)

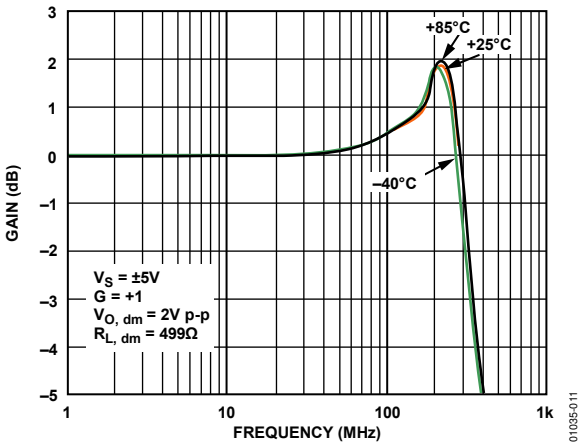

Figure 10. Large Signal Frequency Response at Various Temperatures (See Figure 56)

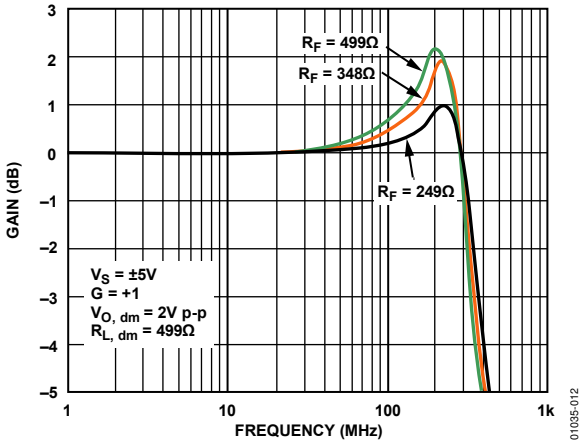

Figure 11. Large Signal Frequency Response vs. R_F (See Figure 56)

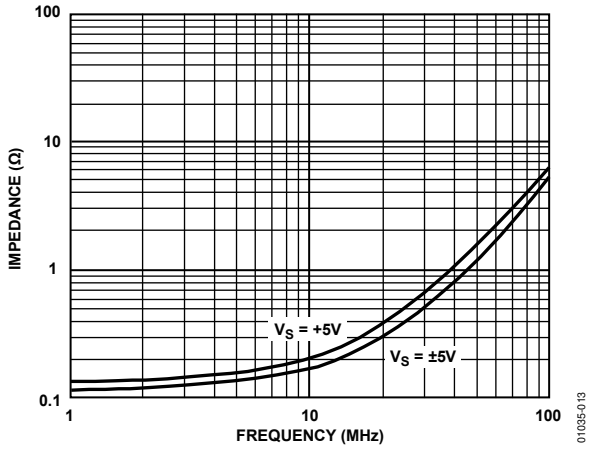

Figure 12. Closed-Loop Single-Ended Z_{OUT} vs. Frequency; G = +1 (See Figure 56)

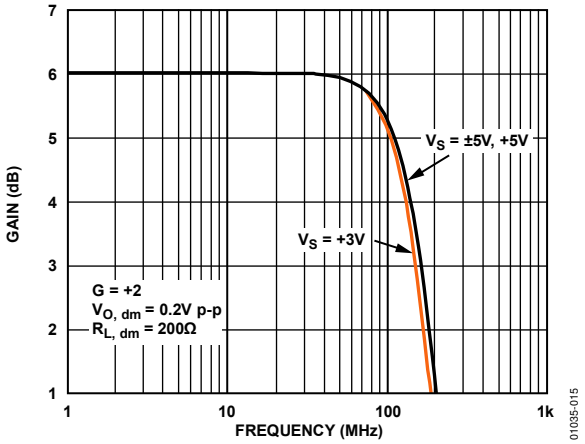

Figure 13. Small Signal Frequency Response (See Figure 57)

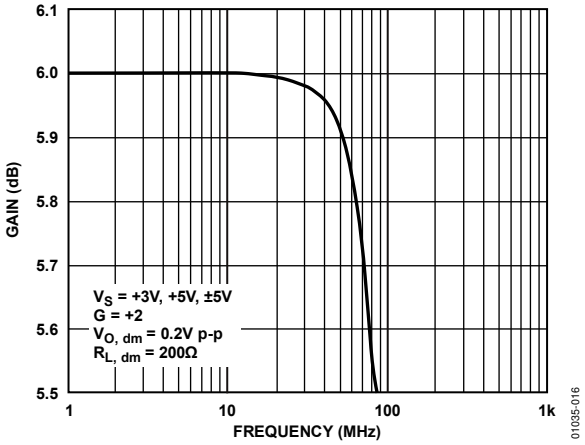

Figure 14. 0.1 dB Flatness vs. Frequency (See Figure 57)

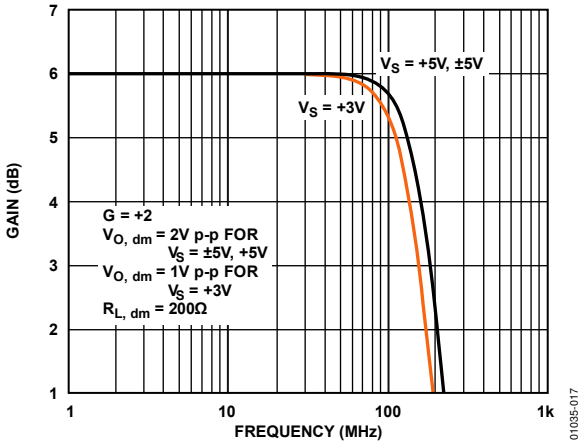

Figure 15. Large Signal Frequency Response (See Figure 57)

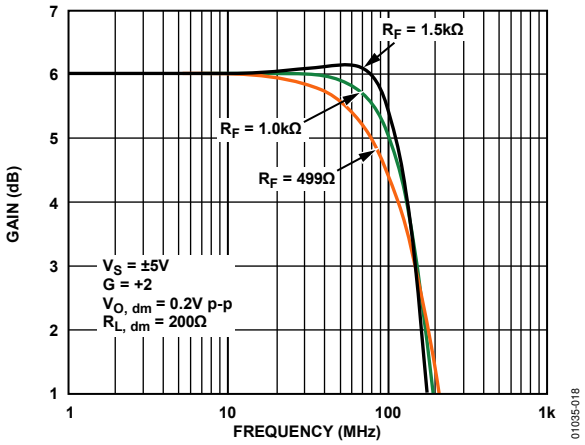

Figure 16. Small Signal Frequency Response vs. R_F (See Figure 57)

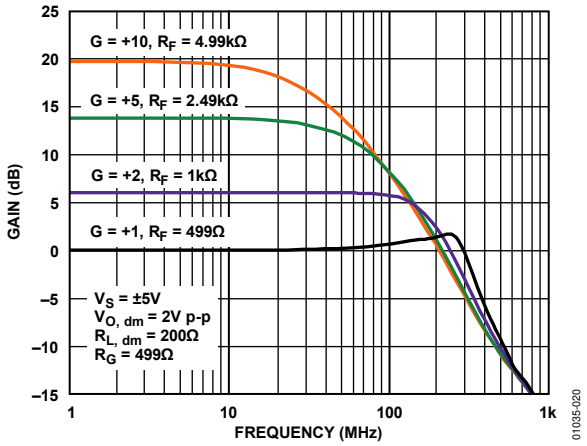

Figure 17. Large Signal Frequency Response for Various Gains (See Figure 58)

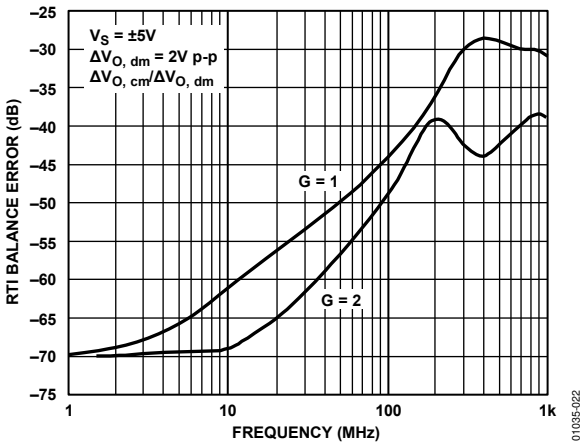

Figure 18. RTI Output Balance Error vs. Frequency (See Figure 59)

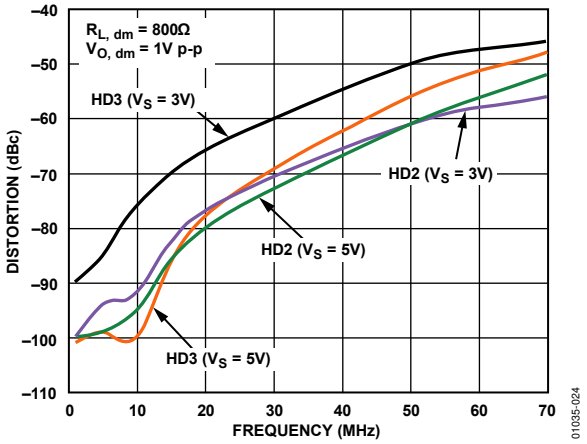

Figure 19. Harmonic Distortion vs. Frequency, G = +1 (See Figure 62)

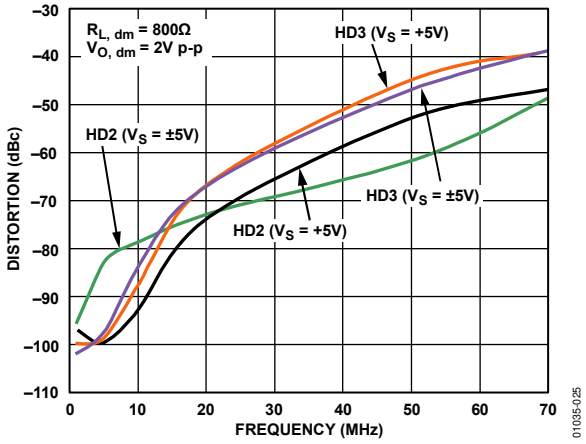

Figure 20. Harmonic Distortion vs. Frequency, G = 1 (See Figure 62)

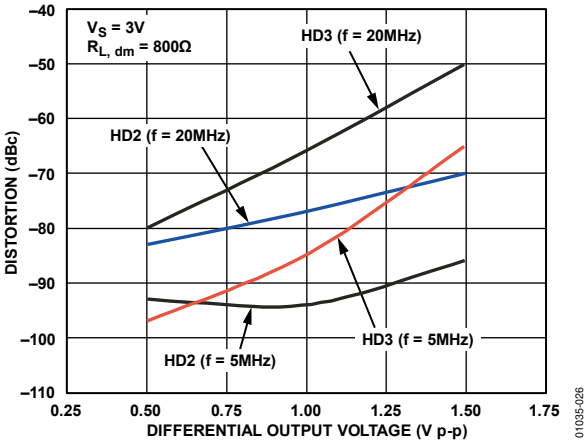

Figure 21. Harmonic Distortion vs. Differential Output Voltage, G = 1 (See Figure 62)

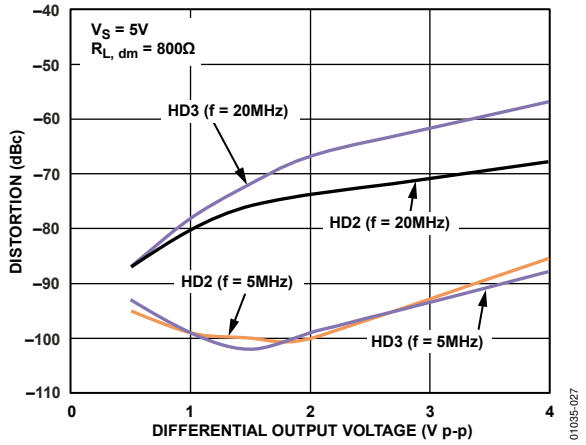

Figure 22. Harmonic Distortion vs. Differential Output Voltage, G = +1 (See Figure 62)

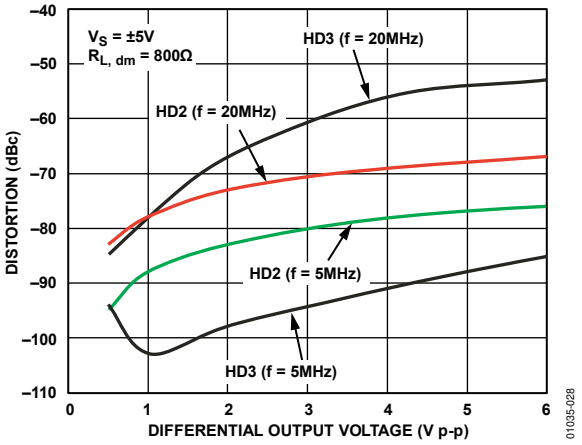

Figure 23. Harmonic Distortion vs. Differential Output Voltage, G = +1 (See Figure 62)

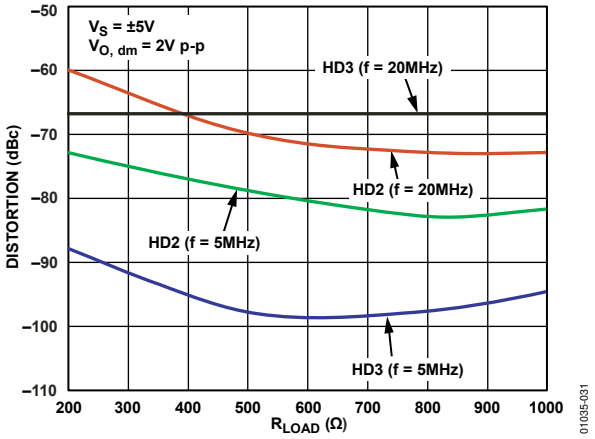

Figure 26. Harmonic Distortion vs. R_{LOAD}, G = +1 (See Figure 62)

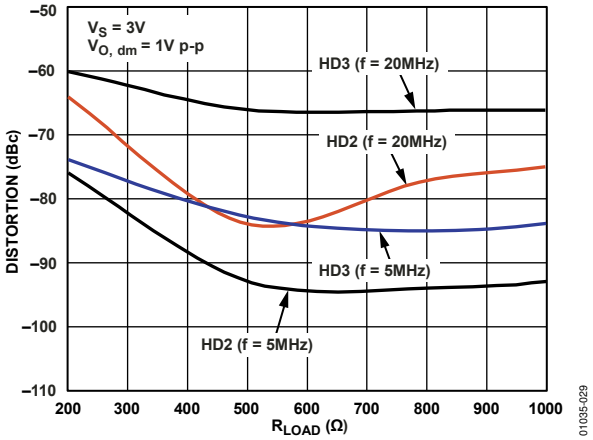

Figure 24. Harmonic Distortion vs. R_{LOAD}, G = +1 (See Figure 62)

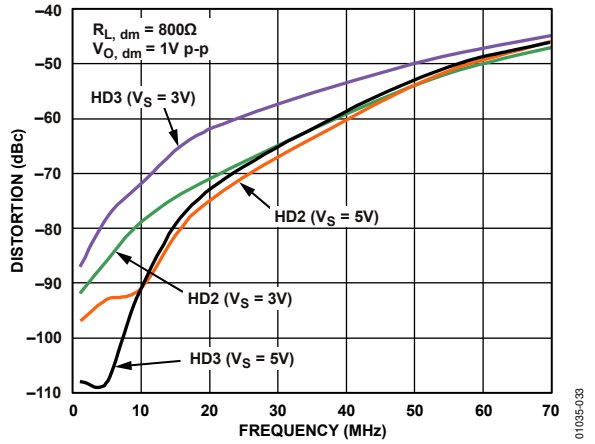

Figure 27. Harmonic Distortion vs. Frequency, G = +2 (See Figure 63)

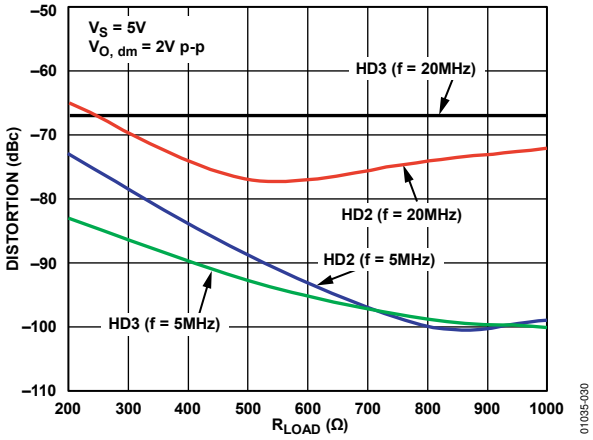

Figure 25. Harmonic Distortion vs. R_{LOAD}, G = +1 (See Figure 62)

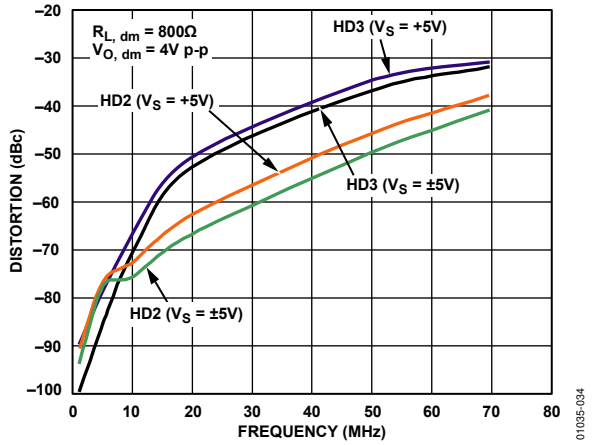

Figure 28. Harmonic Distortion vs. Frequency, G = +2 (See Figure 63)

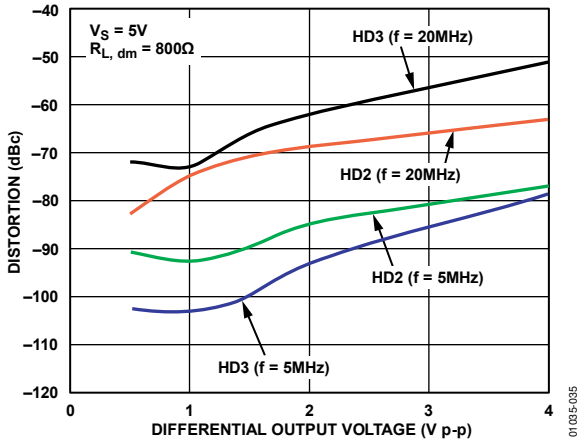

Figure 29. Harmonic Distortion vs. Differential Output Voltage, G = +2 (See Figure 63)

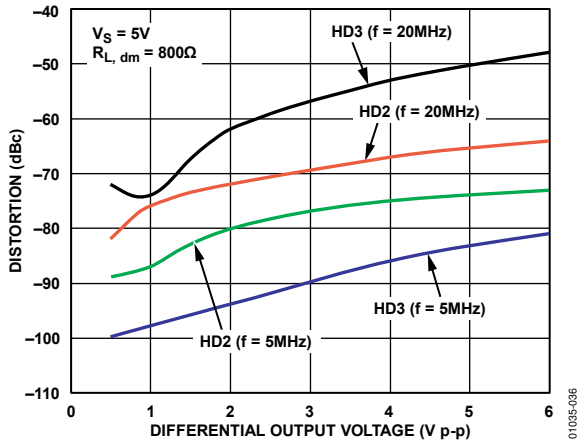

Figure 30. Harmonic Distortion vs. Differential Output Voltage, G = +2 (See Figure 63)

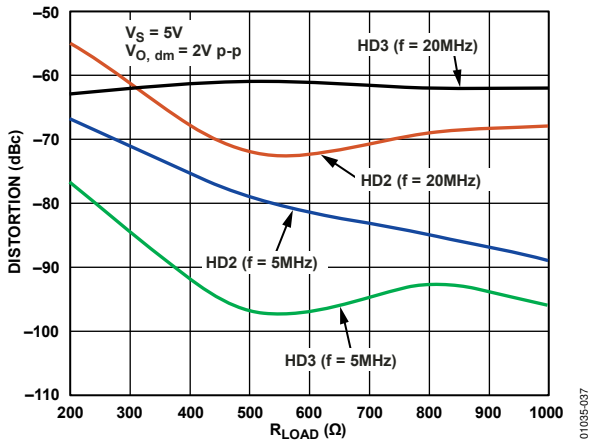

Figure 31. Harmonic Distortion vs. R_{LOAD}, G = +2 (See Figure 63)

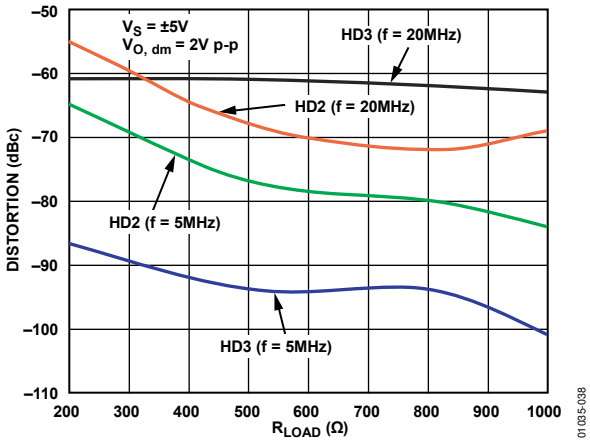

Figure 32. Harmonic Distortion vs. R_{LOAD}, G = +2 (See Figure 63)

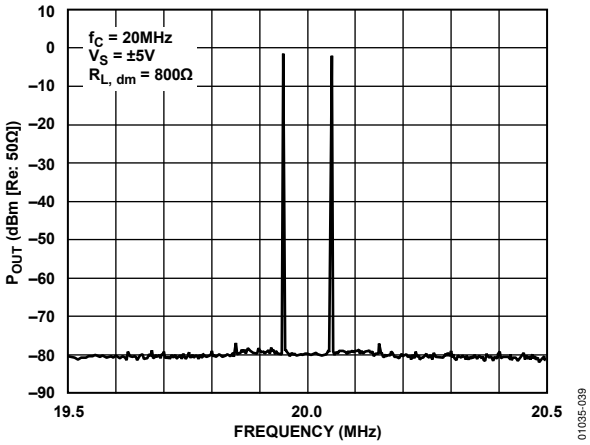

Figure 33. Intermodulation Distortion, G = +1

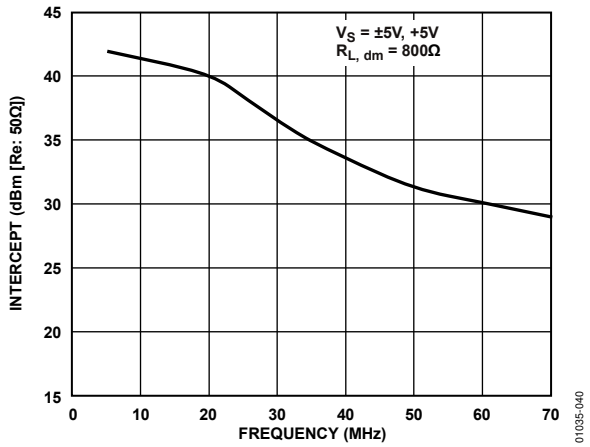

Figure 34. Third-Order Intercept vs. Frequency, G = +1

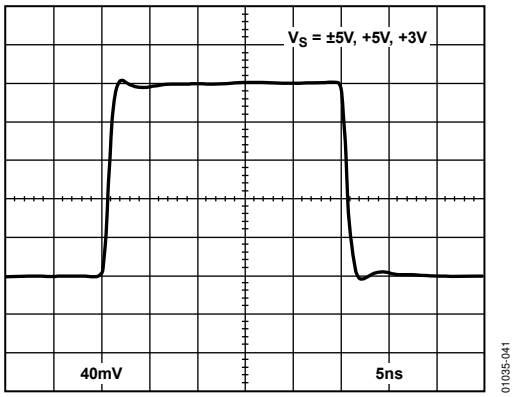

Figure 35. Small Signal Transient Response, G = +1

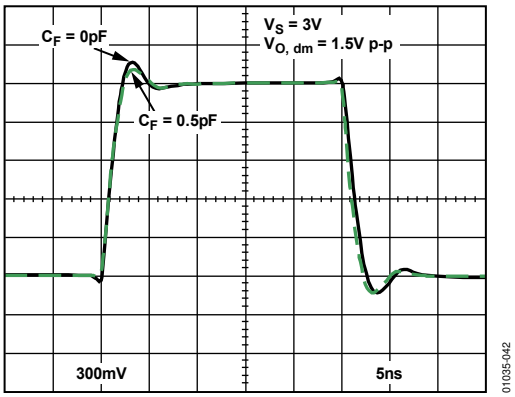

Figure 36. Large Signal Transient Response, G = +1

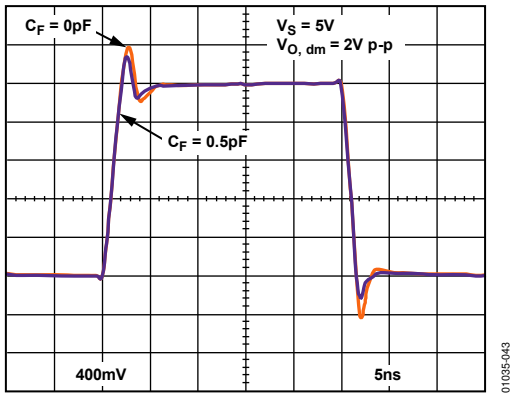

Figure 37. Large Signal Transient Response, G = +1

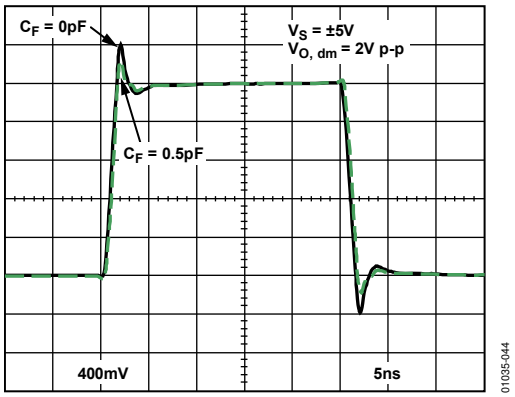

Figure 38. Large Signal Transient Response, G = +1

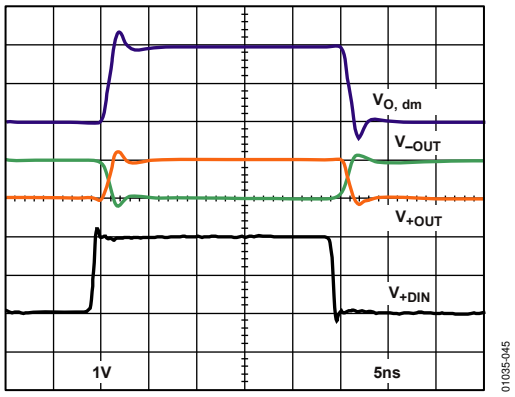

Figure 39. Large Signal Transient Response, G = +1

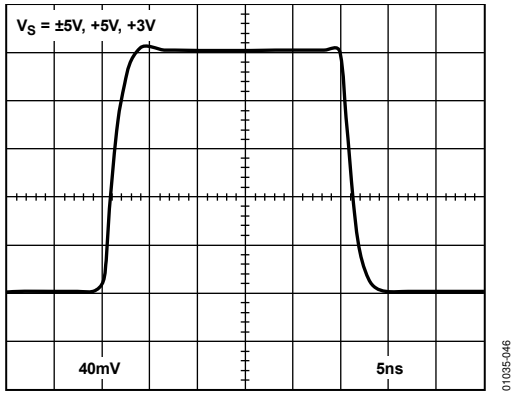

Figure 40. Small Signal Transient Response, G = +2

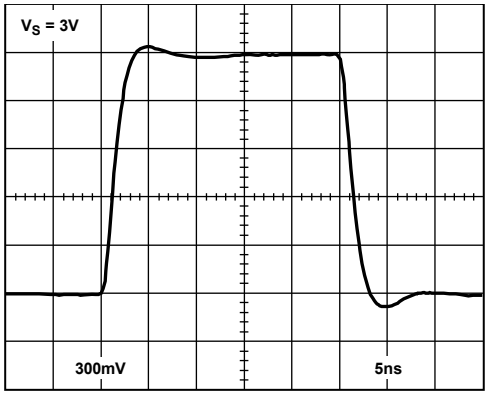

Figure 41. Large Signal Transient Response, G = +2

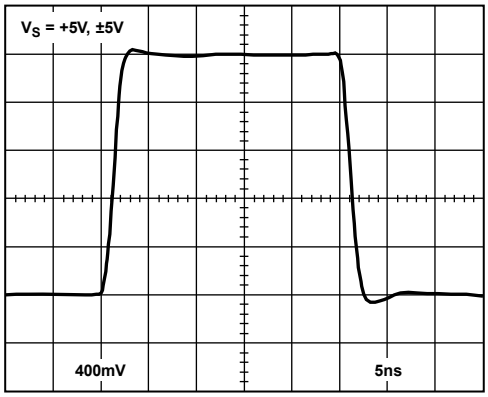

Figure 42. Large Signal Transient Response, G = +2

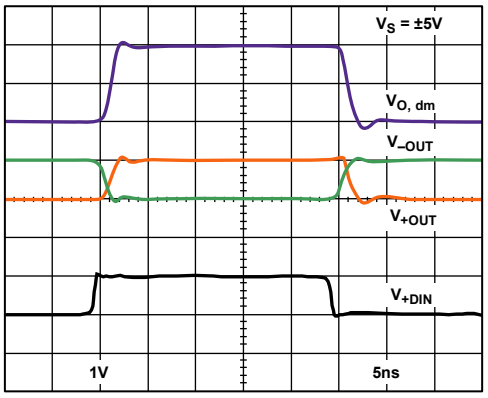

Figure 43. Large Signal Transient Response, G = +2

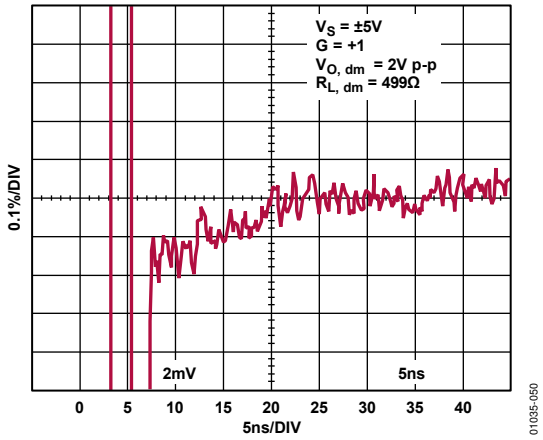

Figure 44. 0.1% Settling Time

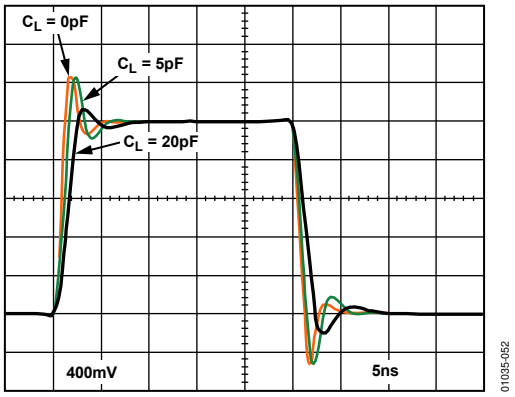

Figure 45. Large Signal Transient Response for Various Capacitor Loads (See Figure 60)

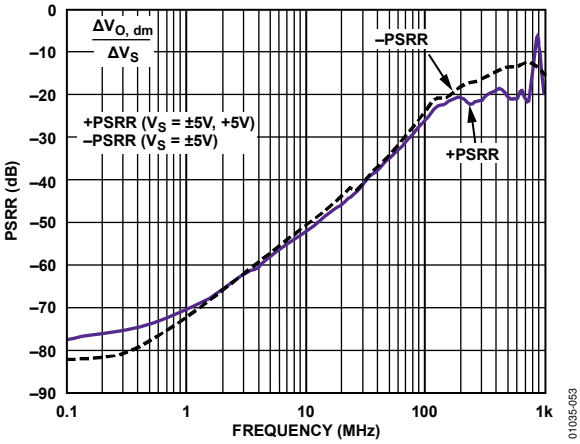

Figure 46. PSRR vs. Frequency

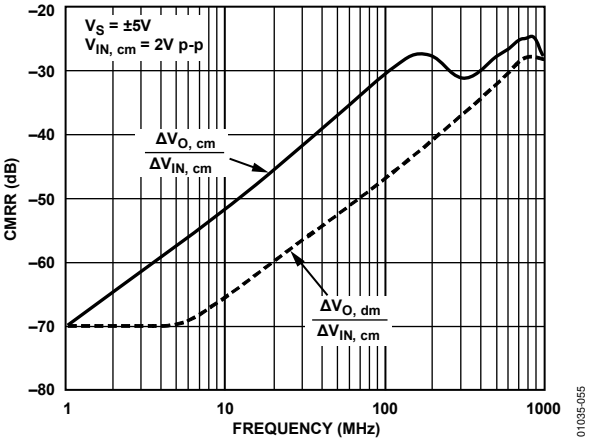

Figure 47. CMRR vs. Frequency (See Figure 61)

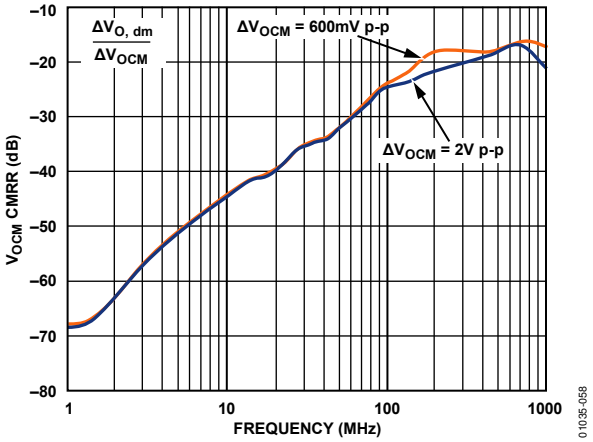

Figure 50. V_{OCM} CMRR vs. Frequency

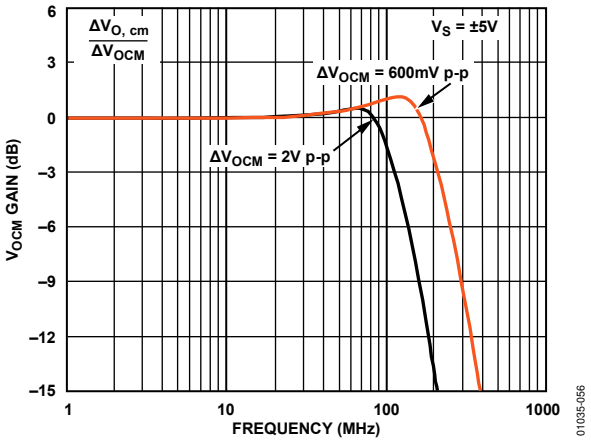

Figure 48. V_{OCM} Gain Response

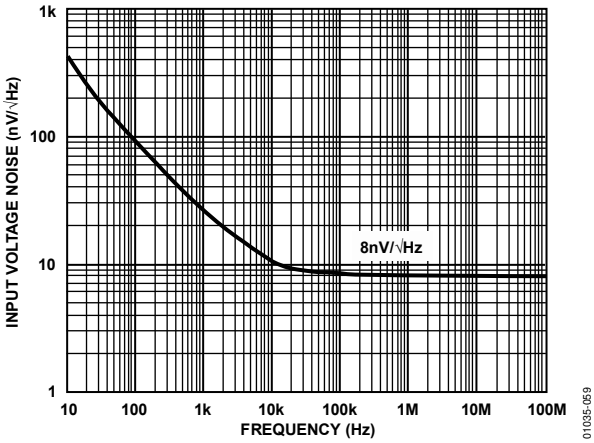

Figure 51. Input Voltage Noise vs. Frequency

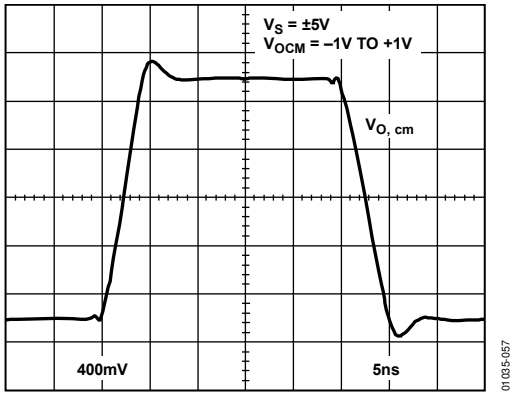

Figure 49. V_{OCM} Transient Response

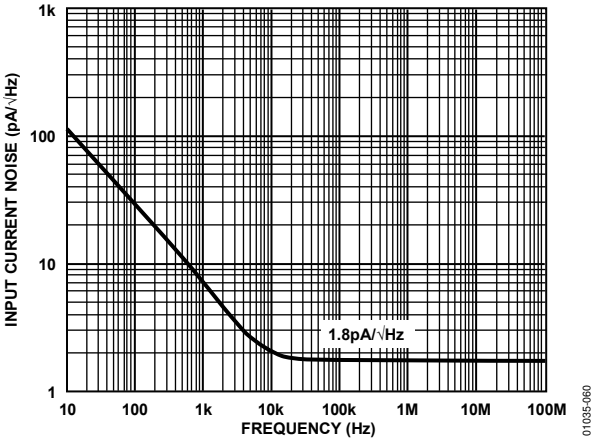

Figure 52. Input Current Noise vs. Frequency

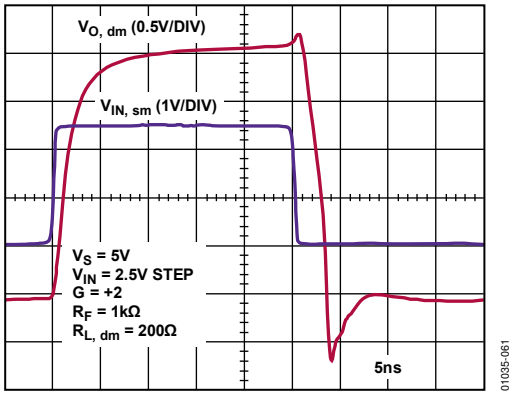

Figure 53. Overdrive Recovery

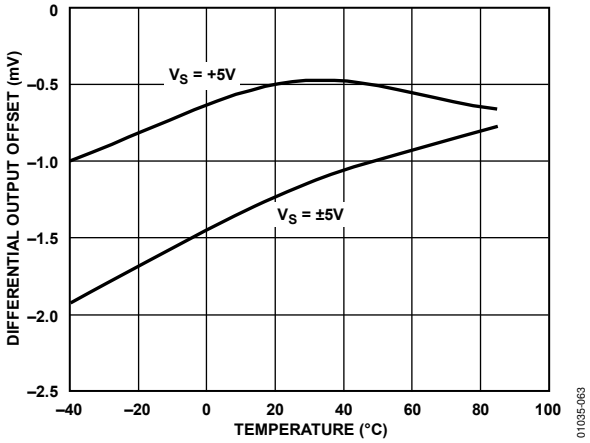

Figure 55. Differential Output Offset Voltage vs. Temperature

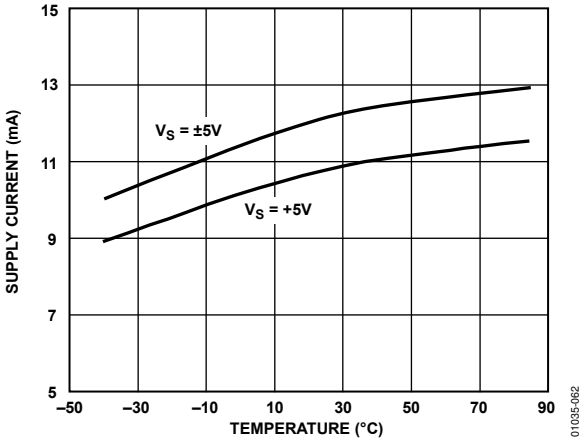

Figure 54. Supply Current vs. Temperature

TEST CIRCUITS

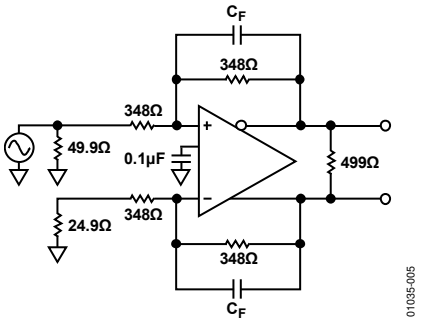

Figure 56. Basic Test Circuit, G = +1

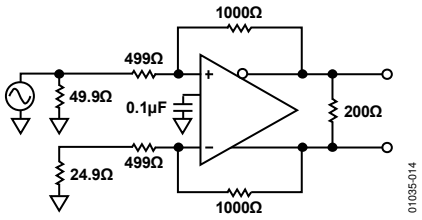

Figure 57. Basic Test Circuit, G = +2

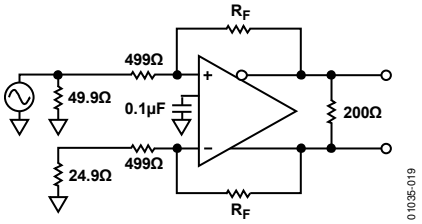

Figure 58. Test Circuit for Various Gains

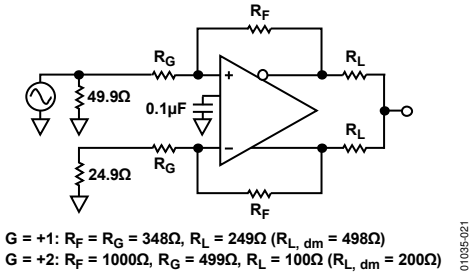

Figure 59. Test Circuit for Output Balance

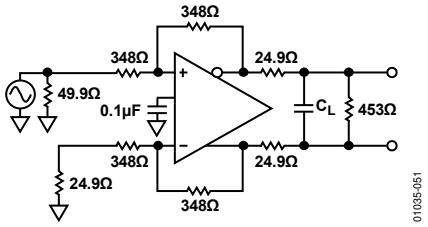

Figure 60. Test Circuit for Capacitor Load Drive

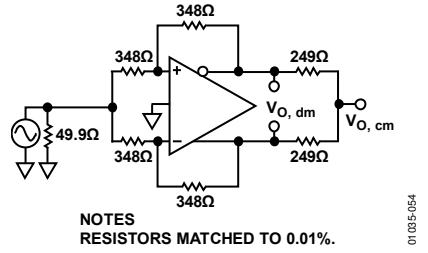

Figure 61. CMRR Test Circuit

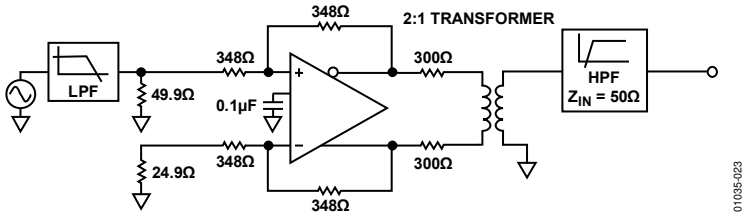

Figure 62. Harmonic Distortion Test Circuit, G = +1, $R_{L, dm}$ = 800 Ω

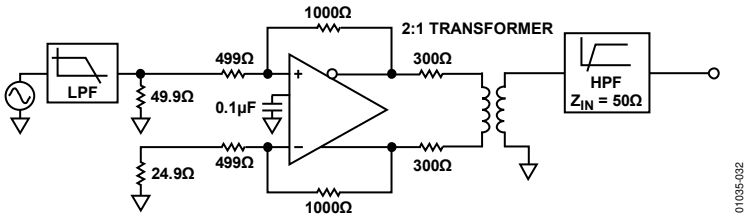

Figure 63. Harmonic Distortion Test Circuit, G = +2, $R_{L, dm}$ = 800 Ω

OPERATIONAL DESCRIPTION

DEFINITION OF TERMS

Differential Voltage

It is the difference between two node voltages. For example, the output differential voltage (or equivalently output differential mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{+OUT} - V_{-OUT})$$

where V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and −OUT terminals with respect to a common reference.

Common-Mode Voltage

It is the average of two node voltages. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{+OUT} + V_{-OUT})/2$$

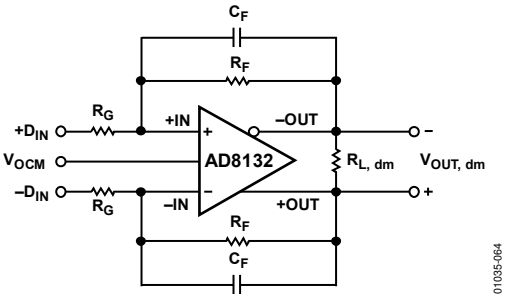

Figure 64. Circuit Definitions

BASIC CIRCUIT OPERATION

One of the more useful and easy to understand ways to use the AD8132 is to provide two equal ratio feedback networks. To match the effect of parasitics, comprise these networks of two equal value feedback resistors (R_F) and two equal value gain resistors (R_G). This circuit is shown in Figure 64.

Like a conventional op amp, the AD8132 has two differential inputs that can be driven with both differential mode input voltage ($V_{IN,\,dm}$) and common-mode input voltage ($V_{IN,\,cm}$).

There is another input to consider (V_{OCM}) on the AD8132 that is not present on conventional op amps. V_{OCM} is completely separate from the previous inputs.

There are two complementary outputs whose response can be defined by a differential mode output ($V_{OUT,\,dm}$) and a common-mode output ($V_{OUT,\,cm}$).

Table 10 shows the gain from any type of input to either type of output.

Table 10. Differential and Common-Mode Gains

Input	$V_{OUT,\,dm}$	$V_{OUT,\,cm}$
$V_{IN,\,dm}$	R_F/R_G	0 (by design)
$V_{IN,\,cm}$	0	0 (by design)
V_{OCM}	0	1 (by design)

As listed in Table 10, the differential output ($V_{OUT,\,dm}$) is equal to the differential input voltage ($V_{IN,\,dm}$) times R_F/R_G. In this case, it does not matter if both differential inputs are driven, or only one output is driven and the other is tied to a reference voltage, such as ground. As seen from the two zero entries in the $V_{OUT,\,dm}$ column, neither of the common-mode inputs has any effect on this gain.

The gain from $V_{IN,\,dm}$ to $V_{OUT,\,cm}$ is 0, and first-order, does not depend on the ratio matching of the feedback networks. The common-mode feedback loop within the AD8132 provides a corrective action to keep this gain term minimized. The term balance error describes the degree that this gain term differs from 0.

The gain from $V_{IN,\,cm}$ to $V_{OUT,\,dm}$ directly depends on the matching of the feedback networks. The analogous term for this transfer function (used in conventional op amps) is common-mode rejection ratio (CMRR). Therefore, if it has a high CMRR, the feedback ratios must be well matched.

The gain from $V_{IN,\,cm}$ to $V_{OUT,\,cm}$ is ideally 0 and is first-order independent of the feedback ratio matching. As in the case of $V_{IN,\,dm}$ to $V_{OUT,\,cm}$, the common-mode feedback loop keeps this term minimized.

The gain from V_{OCM} to $V_{OUT,\,dm}$ is ideally 0 when the feedback ratios are matched only. The amount of differential output signal that is created by varying V_{OCM} is related to the degree of mismatch in the feedback networks.

V_{OCM} controls the output common-mode voltage $V_{OUT,\,cm}$ with a unity-gain transfer function. With equal ratio feedback networks (as previously assumed), its effect on each output is the same, that is the gain from V_{OCM} to $V_{OUT,\,dm}$ is 0. If not driven, the output common-mode voltage is set with an internal voltage divider to a level that is nominally midsupply. It is recommended that a 0.1 μF bypass capacitor be connected to V_{OCM}.

When unequal feedback ratios are used, the two gains associated with $V_{OUT,\,dm}$ become nonzero. This significantly complicates the mathematical analysis along with any intuitive understanding of how the part operates.

THEORY OF OPERATION

The AD8132 differs from conventional op amps by the external presence of an additional input and output. The additional input, V_{OCM}, controls the output common-mode voltage. The additional output is the analog complement of the single output of a conventional op amp. For its operation, the AD8132 uses two feedback loops as compared to the single loop of conventional op amps. Although this provides significant freedom to create various novel circuits, basic op amp theory can still be used to analyze the operation.

One of the feedback loops controls the output common-mode voltage, $V_{OUT, cm}$. Its input is V_{OCM} (Pin 2) and the output is the common mode, or average voltage, of the two differential outputs (+OUT and −OUT). The gain of this circuit is internally set to unity. When the AD8132 is operating in its linear region, this establishes one of the operational constraints: $V_{OUT, cm} = V_{OCM}$.

The second feedback loop controls the differential operation. Similar to an op amp, the gain and gain shaping of the transfer function can be controlled by adding passive feedback networks. However, only one feedback network is required to close the loop and fully constrain the operation, but depending on the function desired, two feedback networks can be used. This is possible because there are two outputs that are each inverted with respect to the differential inputs.

GENERAL USAGE OF THE AD8132

Several assumptions are made here for a first-order analysis; they are the typical assumptions used for the analysis of op amps.

- The input bias currents are sufficiently small so they can be neglected.
- The output impedances are arbitrarily low.
- The open-loop gain is arbitrarily large and drives the amplifier to a state where the input differential voltage is effectively 0.
- Offset voltages are assumed to be 0.

Though it is possible to operate the AD8132 with a purely differential input, many of its applications call for a circuit that has a single-ended input with a differential output.

For a single-ended-to-differential circuit, the R_G of the input that is not driven is tied to a reference voltage or to ground. Additional conditions are discussed in the following sections. In addition, the voltage at V_{OCM}, and therefore $V_{OUT, cm}$, is assumed to be ground. Figure 67 shows a generalized schematic of such a circuit using an AD8132 with two feedback paths.

For each feedback network, a feedback factor can be defined as the fraction of the output signal that is fed back to the opposite sign input. These terms are

$$\beta 1 = R_{G1}/(R_{G1} + R_{F1})$$

$$\beta 2 = R_{G2}/(R_{G2} + R_{F2})$$

The feedback factor, β1, is for the side that is driven, and the feedback factor, β2, is for the side that is tied to a reference voltage (ground). Note that each feedback factor can vary anywhere between 0 and 1.

A single-ended-to-differential gain equation can be derived (this is true for all values of β1 and β2) from

$$G = \frac{2(1 - \beta 1)}{(\beta 1 + \beta 2)}$$

This expression is not very intuitive, but some further examples can provide better understanding of its implications. One observation that can be made immediately is that a tolerance error in β1 does not have the same effect on gain as the same tolerance error in β2.

DIFFERENTIAL AMPLIFIER WITHOUT RESISTORS (HIGH INPUT IMPEDANCE INVERTING AMPLIFIER)

The simplest closed-loop circuit that can be made does not require any resistors and is shown in Figure 70. In this circuit, β1 is equal to 0, and β2 is equal to 1. The gain is equal to 2.

A more intuitive method to figure the gain is by simple inspection. +OUT is connected to −IN, whose voltage is equal to the voltage at +IN under equilibrium conditions. Therefore, $+V_{OUT}$ is equal to V_{IN}, and there is unity gain in this path. Because −OUT has to swing in the opposite direction from +OUT due to the common-mode constraint, its effect doubles the output signal and produces a gain of 2.

One useful function that this circuit provides is a high input impedance inverter. If +OUT is ignored, there is a unity-gain, high input impedance amplifier formed from +IN to −OUT. Most traditional op amp inverters have relatively low input impedances, unless they are buffered with another amplifier.

V_{OCM} is assumed to be at midsupply. Because there is still the constraint that $+V_{OUT}$ must equal V_{IN}, changing the V_{OCM} voltage does not change $+V_{OUT}$ (equal to V_{IN}). Therefore, the effect of changing V_{OCM} must show up at −OUT.

For example, if V_{OCM} is raised by 1 V, then $-V_{OUT}$ must increase by 2 V. This makes $V_{OUT, cm}$ also increase by 1 V because it is defined as the average of the two differential output voltages. This means that the gain from V_{OCM} to the differential output is 2.

OTHER β2 = 1 CIRCUITS

The preceding simple configuration with β2 = 1 and its gain of 2 is the highest gain circuit that can be made under this condition. Because β1 was equal to 0, only higher β1 values are possible. The circuits with higher values of β1 have gains lower than 2. However, circuits with β1 equal to 1 are not practical because they have no effective input and result in a gain of 0.

To increase β1 from 0, it is necessary to add two resistors in a feedback network. A generalized circuit that has β1 with a value higher than 0 is shown in Figure 69. A couple of different convenient gains that can be created are a gain of 1, when β1 is equal to 1/3, and a gain of 0.5, when β1 equals 0.6.

With β2 equal to 1 in these circuits, V_{OCM} serves as the reference voltage that measures the input voltage and the individual output voltages. In general, when V_{OCM} is varied in circuits with unmatched feedback networks, a differential output signal is generated that is proportional to the applied V_{OCM} voltage.

VARYING β2

Though the β2 = 1 circuit sets β2 to 1, another class of simple circuits can be made that sets β2 equal to 0. This means that there is no feedback from +OUT to −IN. This class of circuits is very similar to a conventional inverting op amp. However, the AD8132 circuits have an additional output and common-mode input that can be analyzed separately (see Figure 71).

With −IN connected to ground, +IN becomes a virtual ground in the sense that the term is used for conventional op amps. Both inputs must maintain the same voltage for equilibrium operation; therefore, if one is set to ground, the other is driven to ground. The input impedance can also be seen to be equal to R_G, just as in a conventional op amp.

In this case, however, the positive input and negative output are used for the feedback network. Because a conventional op amp does not have a negative output, only its inverting input can be used for the feedback network. The AD8132 is symmetrical, therefore, the feedback network on either side can be used to produce the same results.

Because +IN is a summing junction, by an analogy to conventional op amps, the gain from V_{IN} to −OUT is $-R_F/R_G$. This holds true regardless of the voltage on V_{OCM}, and because +OUT moves the same amount in the opposite direction from −OUT, the overall gain is $-2(R_F/R_G)$.

V_{OCM} still governs $V_{OUT, cm}$; therefore, +OUT must be the only output that moves when V_{OCM} is varied. Because $V_{OUT, cm}$ is the average of the two outputs, +OUT must move twice as far, and in the same direction as V_{OCM}, to create the proper $V_{OUT, cm}$. Therefore, the gain from V_{OCM} to +OUT must be 2.

With β2 equal to 0 in these circuits, the gain can theoretically be set to any value from close to 0 to infinity, just as it can with a conventional op amp in the inverting mode. However, practical real-world limitations and parasitics limit the range of acceptable gain to more modest values.

β1 = 0

There is yet another class of circuits where there is no feedback from −OUT to +IN. This is the case where β1 = 0. The differential amplifier without a resistor described in the Differential Amplifier Without Resistors (High Input Impedance Inverting Amplifier) section meets this condition, but it was presented only with the condition that β2 = 1. Recall that this circuit had a gain equal to 2.

If β2 decreases in this circuit from unity, a smaller part of $+V_{OUT}$ is fed back to −IN and the gain increases (see Figure 68). This circuit is very similar to a noninverting op amp configuration, except for the presence of the additional complementary output. Therefore, the overall gain is twice that of a noninverting op amp or $2 \times (1 + R_{F2}/R_{G2})$ or $2 \times (1/\beta 2)$.

Once again, varying V_{OCM} does not affect both outputs in the same way; therefore, in addition to varying $V_{OUT, cm}$ with unity gain, there is also an effect on $V_{OUT, dm}$ by changing V_{OCM}.

ESTIMATING THE OUTPUT NOISE VOLTAGE

Similar to the case of a conventional op amp, the differential output errors (noise and offset voltages) can be estimated by multiplying the input-referred terms, at +IN and −IN, by the circuit noise gain. The noise gain is defined as

$$G_N = 1 + \left(\frac{R_F}{R_G} \right)$$

To compute the total output-referred noise for the circuit of Figure 64, consideration must be given to the contribution of resistors, R_F and R_G. See Table 11 for estimated output noise voltage densities at various closed-loop gains.

Table 11. Recommended Resistor Values and Noise Performance for Specific Gains

Gain	R_G (Ω)	R_F (Ω)	Bandwidth −3 dB (MHz)	Output Noise AD8132 Only (nV/√Hz)	Output Noise AD8132 + R_G, R_F (nV/√Hz)
1	499	499	360	16	17
2	499	1.0 k	160	24.1	26.1
5	499	2.49 k	65	48.4	53.3
10	499	4.99 k	20	88.9	98.6

When using the AD8132 in gain configurations where β1 ≠ β2, differential output noise appears due to input-referred voltage noise in the V_{OCM} circuitry according to the following formula:

$$V_{OND} = 2\,V_{NOCM}\left[\frac{\beta 1 - \beta 2}{\beta 1 + \beta 2}\right]$$

where:
V_{OND} is the output differential noise.
V_{NOCM} is the input-referred voltage noise on V_{OCM}.

CALCULATING INPUT IMPEDANCE OF THE APPLICATION CIRCUIT

The effective input impedance of a circuit, such as that in Figure 64, at $+D_{IN}$ and $-D_{IN}$, depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the input impedance ($R_{IN, dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is simply

$$R_{IN,\,dm} = 2 \times R_G$$

In the case of a single-ended input signal (for example, if $-D_{IN}$ is grounded and the input signal is applied to $+D_{IN}$), the input impedance becomes

$$R_{IN,dm} = \left(\frac{R_G}{1 - \dfrac{R_F}{2 \times \left(R_G + R_F\right)}}\right)$$

The circuit input impedance is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor, R_G.

INPUT COMMON-MODE VOLTAGE RANGE IN SINGLE-SUPPLY APPLICATIONS

The AD8132 is optimized for level-shifting, ground-referenced input signals. For a single-ended input, this implies that the voltage at $-D_{IN}$ in Figure 64 is 0 V when the negative power supply voltage (at V−) of the amplifier is also set to 0 V.

SETTING THE OUTPUT COMMON-MODE VOLTAGE

The V_{OCM} pin of the AD8132 is internally biased at a voltage approximately equal to the midsupply point (average value of the voltage on V+ and V−). Relying on this internal bias results in an output common-mode voltage that is within approximately 100 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is a best practice that an external source or resistor divider (with R_{SOURCE} < 10 kΩ) be used. The output common-mode offset values in the Specifications section assume the V_{OCM} input is driven by a low impedance voltage source.

DRIVING A CAPACITIVE LOAD

A purely capacitive load can react with the pin and bond wire inductance of the AD8132, resulting in high frequency ringing in the pulse response. One way to minimize this effect is to place a small capacitor across each of the feedback resistors. The added capacitance must be small to avoid destabilizing the amplifier. An alternative technique is to place a small resistor in series with the amplifier outputs, as shown in Figure 60.

OPEN-LOOP GAIN AND PHASE

Open-loop gain and phase plots are shown in Figure 65 and Figure 66.

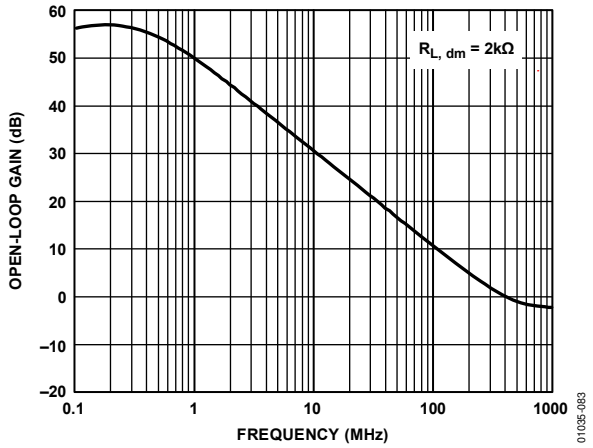

Figure 65. Open-Loop Gain vs. Frequency

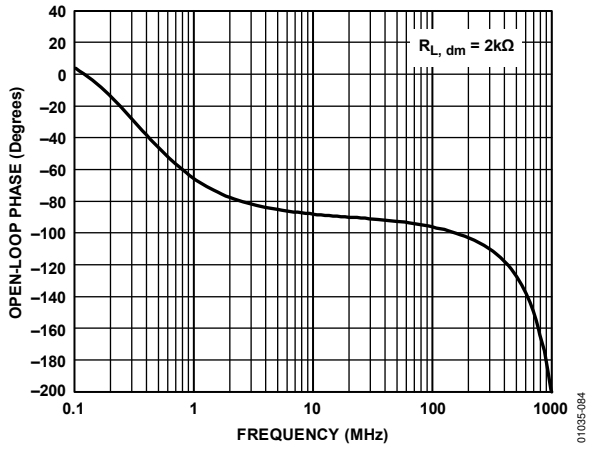

Figure 66. Open-Loop Phase vs. Frequency