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FEATURES
Low cost
33 × 17, fully differential, nonblocking array
>1.5 Gbps per port NRZ data rate
Wide power supply range: +5 V, +3.3 V, -3.3 V, -5 V
Low power
400 mA (outputs enabled)
30 mA (outputs disabled)
PECL and ECL compatible
CMOS/TTL-level control inputs: 3 V to 5 V
Low jitter: <50 ps p-p
No heat sinks required
Drives a backplane directly
Programmable output current
Optimize termination impedance
User-controlled voltage at the load
Minimize power dissipation
Individual output disable for busing and building
Larger arrays
Double row latch
Buffered inputs
Available in 184-lead LQFP
APPLICATIONS
HD and SD digital video
Fiber optic network switching
GENERAL DESCRIPTION

AD8150 is a member of the Xstream line of products and is a breakthrough in digital switching, offering a large switch array (33 × 17) on very little power, typically less than 1.5 W.

Additionally, it operates at data rates in excess of 1.5 Gbps per port, making it suitable for HDTV applications. Further, the pricing of the AD8150 makes it affordable enough to be used for SD applications. The AD8150 is also useful for OC-24 optical network switching.

The AD8150's flexible supply voltages allow the user to operate with either PECL or ECL data levels and will operate down to 3.3 V for further power reduction. The control interface is CMOS/TTL compatible (3 V to 5 V).

Its fully differential signal path reduces jitter and crosstalk while allowing the use of smaller single-ended voltage swings. The AD8150 is offered in a 184-lead LQFP package that operates over the industrial temperature range of 0°C to 85°C.

Rev. A

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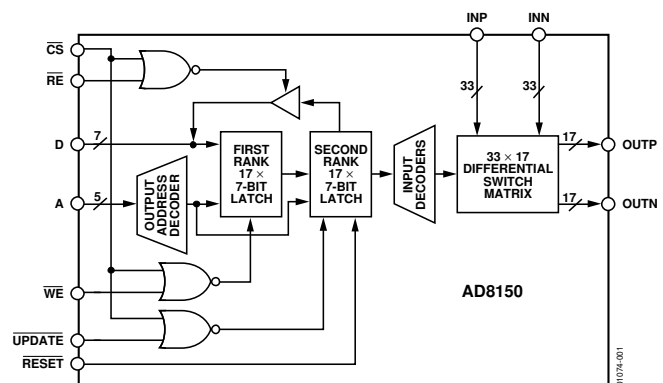
FUNCTIONAL BLOCK DIAGRAM


Figure 1. Functional Block Diagram

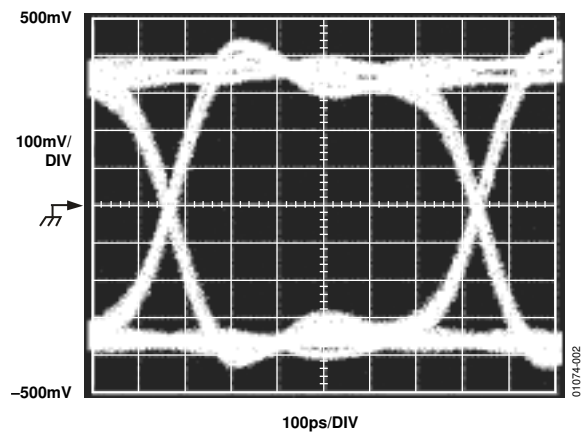


Figure 2. Output Eye Pattern, 1.5 Gbps

AD8150* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-214: Ground Rules for High Speed Circuits

Data Sheet

- AD8150: Xstream™ 33 x 17, 1.5 Gbps Digital Crosspoint Switch Data Sheet

REFERENCE MATERIALS

Informational

- Optical and High Speed Networking ICs

DESIGN RESOURCES

- AD8150 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD8150 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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REVISION HISTORY

9/05—Rev. 0 to Rev. A

Updated Format.....	Universal
Change to Absolute Maximum Ratings.....	4
Changes to Maximum Power Dissipation Section.....	4
Change to Figure 3	4
Changes to Figure 40.....	26
Updated Outline Dimensions	42
Changes to Ordering Guide	42

Revision 0: Initial Version

SPECIFICATIONS

At 25°C, $V_{CC} = 3.3\text{ V}$ to 5 V , $V_{EE} = 0\text{ V}$, $R_L = 50\ \Omega$ (see Figure 25), $I_{OUT} = 16\text{ mA}$, unless otherwise noted.

Table 1

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Max Data Rate/Channel (NRZ)		1.5			Gbps
Channel Jitter	Data rate < 1.5 Gbps		50		ps p-p
RMS Channel Jitter	$V_{CC} = 5\text{ V}$		10		ps
Propagation Delay	Input to output		650		ps
Propagation Delay Match			50	100	ps
Output Rise/Fall Time	20% to 80%		100		ps
INPUT CHARACTERISTICS					
Input Voltage Swing	Differential	200		1000	mV p-p
Input Voltage Range	Common mode	$V_{CC} - 2$		V_{CC}	V
Input Bias Current			2		μA
Input Capacitance			2		pF
Input V_{IN} High		$V_{CC} - 1.2$		$V_{CC} - 0.2$	V
Input V_{IN} Low		$V_{CC} - 2.4$		$V_{CC} - 1.4$	V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Differential (see Figure 25)		800		mV p-p
Output Voltage Range		$V_{CC} - 1.8$		V_{CC}	V
Output Current		5		25	mA
Output Capacitance			2		pF
POWER SUPPLY					
Operating Range					
PECL, V_{CC}	$V_{EE} = 0\text{ V}$	3.3		5	V
ECL, V_{EE}	$V_{CC} = 0\text{ V}$	-5		-3.3	V
V_{DD}		3		5	V
V_{SS}			0		V
Quiescent Current			2		mA
V_{DD}	All outputs enabled, $I_{OUT} = 16\text{ mA}$		400		mA
V_{EE}	T_{MIN} to T_{MAX}			450	mA
	All outputs disabled		30		mA
THERMAL CHARACTERISTICS					
Operating Temperature Range		0		85	°C
θ_{JA}			30		°C/W
LOGIC INPUT CHARACTERISTICS					
Input V_{IN} High	$V_{DD} = 3\text{ V dc}$ to 5 V dc	1.9		V_{DD}	V
Input V_{IN} Low		0		0.9	V

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage $V_{DD} - V_{EE}$	10.5 V
Internal Power Dissipation ¹ AD8150 184-Lead Plastic LQFP (ST)	4.2 W
Differential Input Voltage	$V_{CC} - V_{EE}$
Output Short-Circuit Duration	Observe power derating curves
Storage Temperature Range ²	-65°C to +125°C

¹ Specification is for device in free air ($T_A = 25^\circ\text{C}$):
184-lead plastic LQFP (ST): $\theta_{JA} = 30^\circ\text{C}/\text{W}$.

² Maximum reflow temperatures are to JEDEC industry standard J-STD-020.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8150 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 125°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 125°C for an extended period can result in device failure.

While the AD8150 is internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (125°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 3.

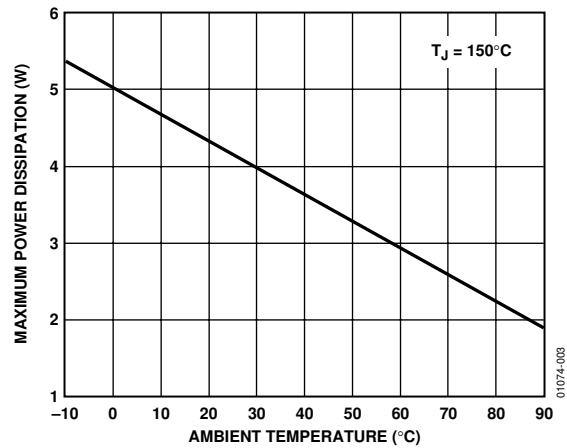


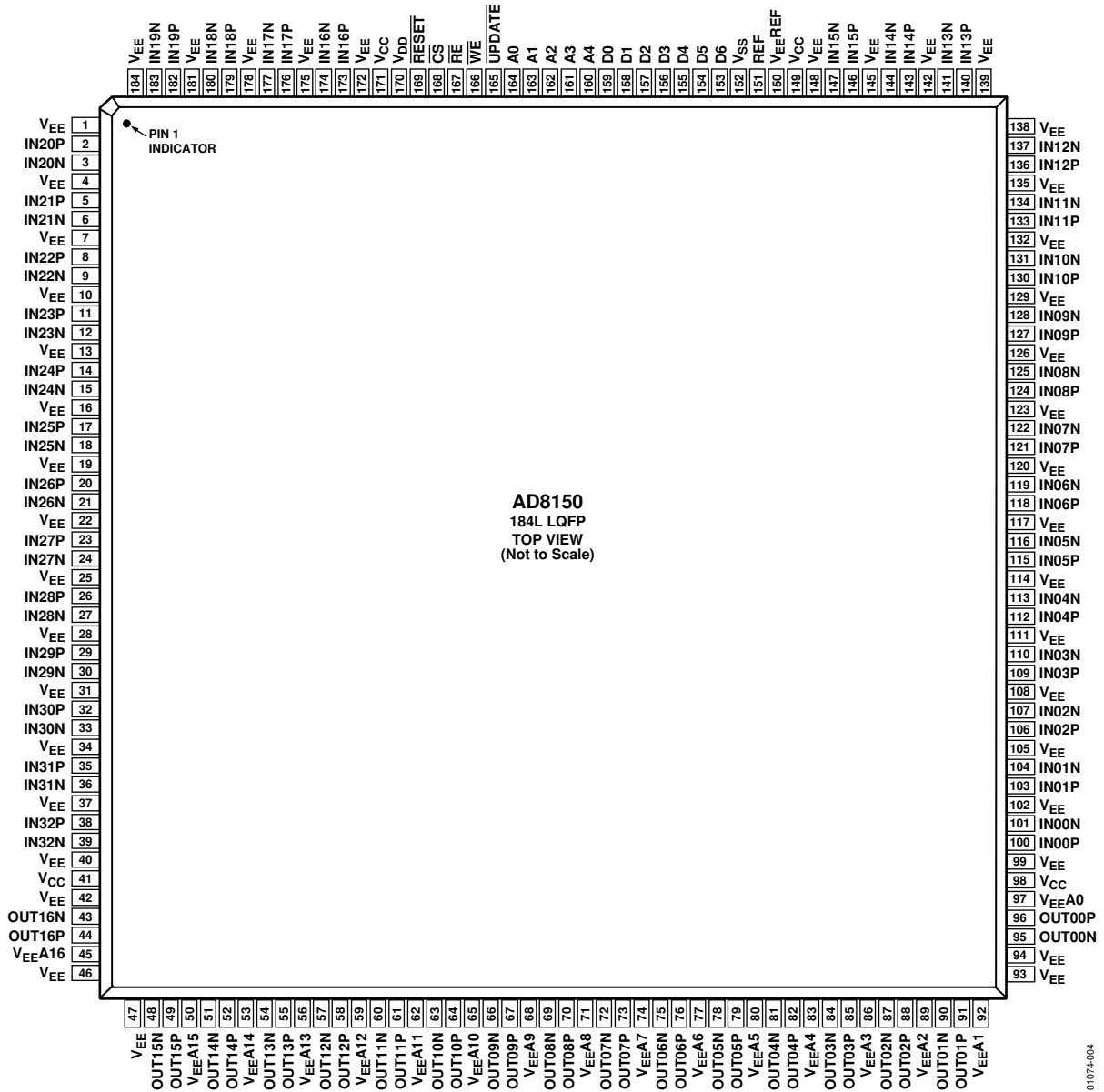
Figure 3. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



AD8150
184L LQFP
TOP VIEW
(Not to Scale)

Figure 4. Pin Configuration

01074-004

AD8150

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31, 34, 37, 40, 42, 46, 47, 92, 93, 99, 102, 105, 108, 111, 114, 117, 120, 123, 126, 129, 132, 135, 138, 139, 142, 145, 148, 172, 175, 178, 181, 184	V _{EE}	Power supply	Most Negative PECL Supply (common with other points labeled V _{EE})
2	IN20P	PECL	High Speed Input
3	IN20N	PECL	High Speed Input Complement
5	IN21P	PECL	High Speed Input
6	IN21N	PECL	High Speed Input Complement
8	IN22P	PECL	High Speed Input
9	IN22N	PECL	High Speed Input Complement
11	IN23P	PECL	High Speed Input
12	IN23N	PECL	High Speed Input Complement
14	IN24P	PECL	High Speed Input
15	IN24N	PECL	High Speed Input Complement
17	IN25P	PECL	High Speed Input
18	IN25N	PECL	High Speed Input Complement
20	IN26P	PECL	High Speed Input
21	IN26N	PECL	High Speed Input Complement
23	IN27P	PECL	High Speed Input
24	IN27N	PECL	High Speed Input Complement
26	IN28P	PECL	High Speed Input
27	IN28N	PECL	High Speed Input Complement
29	IN29P	PECL	High Speed Input
30	IN29N	PECL	High Speed Input Complement
32	IN30P	PECL	High Speed Input
33	IN30N	PECL	High Speed Input Complement
35	IN31P	PECL	High Speed Input
36	IN31N	PECL	High Speed Input Complement
38	IN32P	PECL	High Speed Input
39	IN32N	PECL	High Speed Input Complement
41, 98, 149, 171	V _{CC}	Power supply	Most Positive PECL Supply (common with other points labeled V _{CC})
43	OUT16N	PECL	High Speed Output Complement
44	OUT16P	PECL	High Speed Output
45	V _{EE} A16	Power supply	Most Negative PECL Supply (unique to this output)
48	OUT15N	PECL	High Speed Output Complement
49	OUT15P	PECL	High Speed Output
50	V _{EE} A15	Power supply	Most Negative PECL Supply (unique to this output)
51	OUT14N	PECL	High Speed Output Complement
52	OUT14P	PECL	High Speed Output
53	V _{EE} A14	Power supply	Most Negative PECL Supply (unique to this output)
54	OUT13N	PECL	High Speed Output Complement
55	OUT13P	PECL	High Speed Output
56	V _{EE} A13	Power supply	Most Negative PECL Supply (unique to this output)
57	OUT12N	PECL	High Speed Output Complement
58	OUT12P	PECL	High Speed Output
59	V _{EE} A12	Power supply	Most Negative PECL Supply (unique to this output)
60	OUT11N	PECL	High Speed Output Complement
61	OUT11P	PECL	High Speed Output
62	V _{EE} A11	Power supply	Most Negative PECL Supply (unique to this output)
63	OUT10N	PECL	High Speed Output Complement
64	OUT10P	PECL	High Speed Output

Pin No.	Mnemonic	Type	Description
65	V _{EE} A10	Power supply	Most Negative PECL Supply (unique to this output)
66	OUT09N	PECL	High Speed Output Complement
67	OUT09P	PECL	High Speed Output
68	V _{EE} A9	Power supply	Most Negative PECL Supply (unique to this output)
69	OUT08N	PECL	High Speed Output Complement
70	OUT08P	PECL	High Speed Output
71	V _{EE} A8	Power supply	Most Negative PECL Supply (unique to this output)
72	OUT07N	PECL	High Speed Output Complement
73	OUT07P	PECL	High Speed Output
74	V _{EE} A7	Power supply	Most Negative PECL Supply (unique to this output)
75	OUT06N	PECL	High Speed Output Complement
76	OUT06P	PECL	High Speed Output
77	V _{EE} A6	Power supply	Most Negative PECL Supply (unique to this output)
78	OUT05N	PECL	High Speed Output Complement
79	OUT05P	PECL	High Speed Output
80	V _{EE} A5	Power supply	Most Negative PECL Supply (unique to this output)
81	OUT04N	PECL	High Speed Output Complement
82	OUT04P	PECL	High Speed Output
83	V _{EE} A4	Power supply	Most Negative PECL Supply (unique to this output)
84	OUT03N	PECL	High Speed Output Complement
85	OUT03P	PECL	High Speed Output
86	V _{EE} A3	Power supply	Most Negative PECL Supply (unique to this output)
87	OUT02N	PECL	High Speed Output Complement
88	OUT02P	PECL	High Speed Output
89	V _{EE} A2	Power supply	Most Negative PECL Supply (unique to this output)
90	OUT01N	PECL	High Speed Output Complement
91	OUT01P	PECL	High Speed Output
94	V _{EE} A1	Power supply	Most Negative PECL Supply (unique to this output)
95	OUT00N	PECL	High Speed Output Complement
96	OUT00P	PECL	High Speed Output
97	V _{EE} A0	Power supply	Most Negative PECL Supply (unique to this output)
100	IN00P	PECL	High Speed Input
101	IN00N	PECL	High Speed Input Complement
103	IN01P	PECL	High Speed Input
104	IN01N	PECL	High Speed Input Complement
106	IN02P	PECL	High Speed Input
107	IN02N	PECL	High Speed Input Complement
109	IN03P	PECL	High Speed Input
110	IN03N	PECL	High Speed Input Complement
112	IN04P	PECL	High Speed Input
113	IN04N	PECL	High Speed Input Complement
115	IN05P	PECL	High Speed Input
116	IN05N	PECL	High Speed Input Complement
118	IN06P	PECL	High Speed Input
119	IN06N	PECL	High Speed Input Complement
121	IN07P	PECL	High Speed Input
122	IN07N	PECL	High Speed Input Complement
124	IN08P	PECL	High Speed Input
125	IN08N	PECL	High Speed Input Complement
127	IN09P	PECL	High Speed Input
128	IN09N	PECL	High Speed Input Complement
130	IN10P	PECL	High Speed Input

AD8150

Pin No.	Mnemonic	Type	Description
131	IN10N	PECL	High Speed Input Complement
133	IN11P	PECL	High Speed Input
134	IN11N	PECL	High Speed Input Complement
136	IN12P	PECL	High Speed Input
137	IN12N	PECL	High Speed Input Complement
140	IN13P	PECL	High Speed Input
141	IN13N	PECL	High Speed Input Complement
143	IN14P	PECL	High Speed Input
144	IN14N	PECL	High Speed Input Complement
146	IN15P	PECL	High Speed Input
147	IN15N	PECL	High Speed Input Complement
150	V _{EE} REF	R-program	Connection Point for Output Logic Pull-Down Programming Resistor (must be connected to V _{EE})
151	REF	R-program	Connection Point for Output Logic Pull-Down Programming Resistor
152	V _{SS}	Power supply	Most <u>Negative</u> Control Logic Supply
153	D6	TTL	Enable/DISABLE Output
154	D5	TTL	(32) MSB Input Select
155	D4	TTL	(16)
156	D3	TTL	(8)
157	D2	TTL	(4)
158	D1	TTL	(2)
159	D0	TTL	(1) LSB Input Select
160	A4	TTL	(16) MSB Output Select
161	A3	TTL	(8)
162	A2	TTL	(4)
163	A1	TTL	(2)
164	A0	TTL	(1) LSB Output Select
165	<u>UPDATE</u>	TTL	Second-Rank Program
166	<u>WE</u>	TTL	First-Rank Program
167	<u>RE</u>	TTL	Enable Readback
168	<u>CS</u>	TTL	Enable Chip to Accept Programming
169	<u>RESET</u>	TTL	Disable All Outputs (Hi-Z)
170	V _{DD}	Power supply	Most Positive Control Logic Supply
173	IN16P	PECL	High Speed Input
174	IN16N	PECL	High Speed Input Complement
176	IN17P	PECL	High Speed Input
177	IN17N	PECL	High Speed Input Complement
179	IN18P	PECL	High Speed Input
180	IN18N	PECL	High Speed Input Complement
182	IN19P	PECL	High Speed Input
183	IN19N	PECL	High Speed Input Complement

TYPICAL PERFORMANCE CHARACTERISTICS

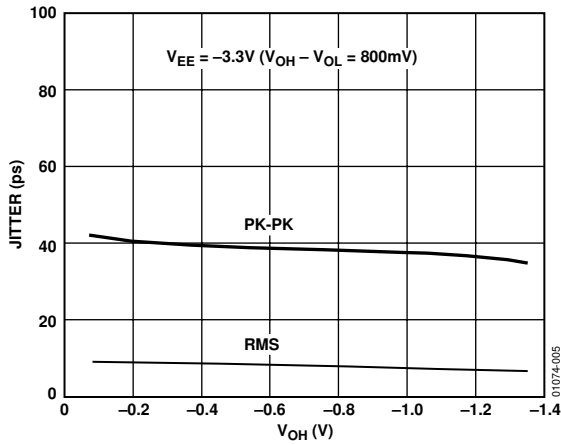


Figure 5. Jitter vs. V_{OH} 1.5 Gbps, PRBS 23

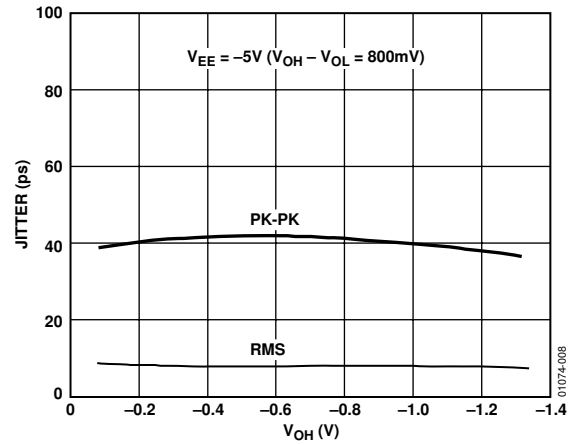


Figure 8. Jitter vs. V_{OH} 1.5 Gbps, PRBS 23

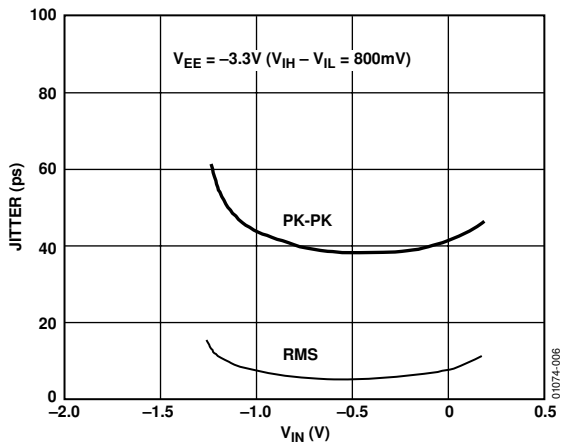


Figure 6. Jitter vs. V_{IH} 1.5 Gbps, PRBS 23

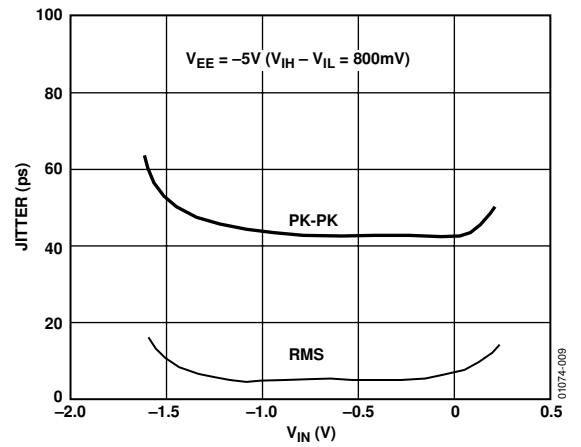


Figure 9. Jitter vs. V_{IH} 1.5 Gbps, PRBS 23

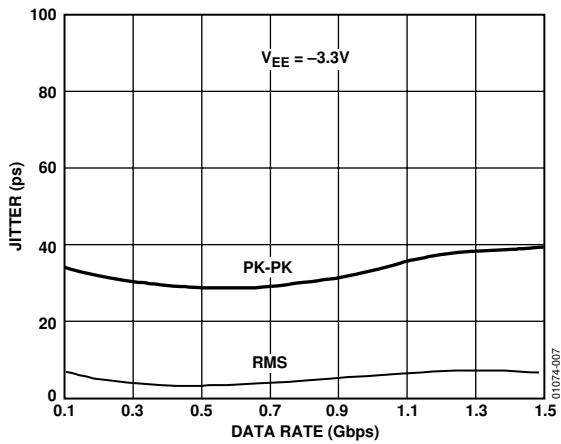


Figure 7. Jitter vs. Data Rate, PRBS 23

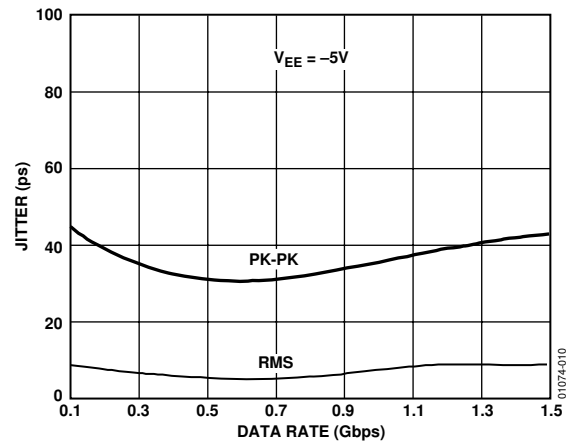


Figure 10. Jitter vs. Data Rate, PRBS 23

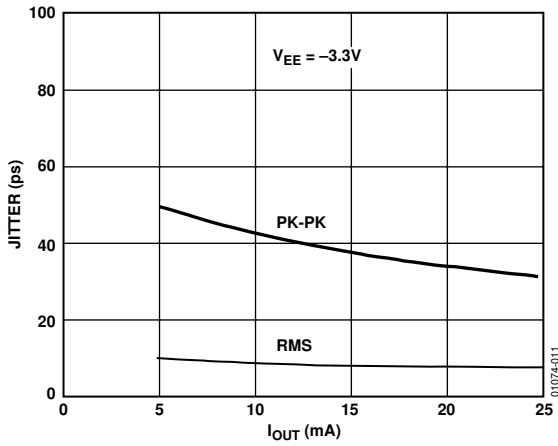


Figure 11. Jitter vs. I_{OUT} 1.5 Gbps, PRBS 23

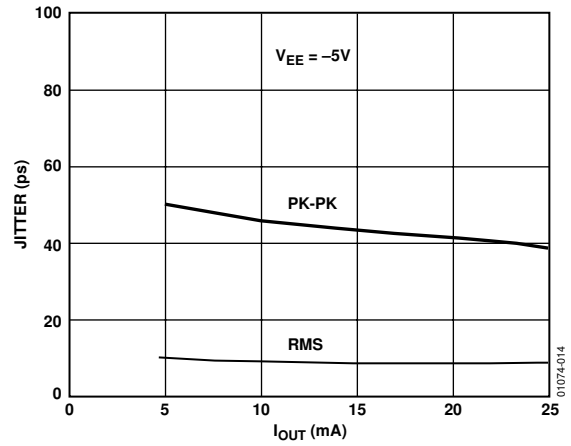


Figure 14. Jitter vs. I_{OUT} 1.5 Gbps, PRBS 23

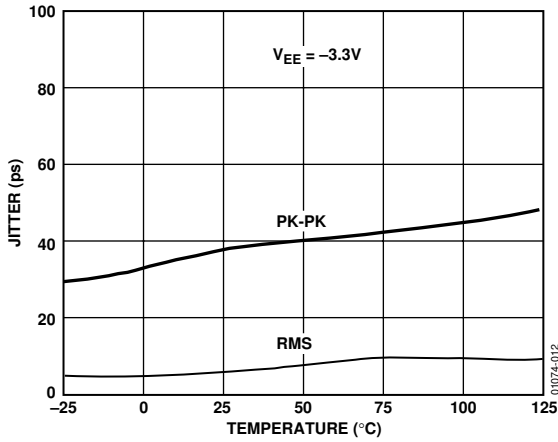


Figure 12. Jitter vs. Temperature 1.5 Gbps, PRBS 23

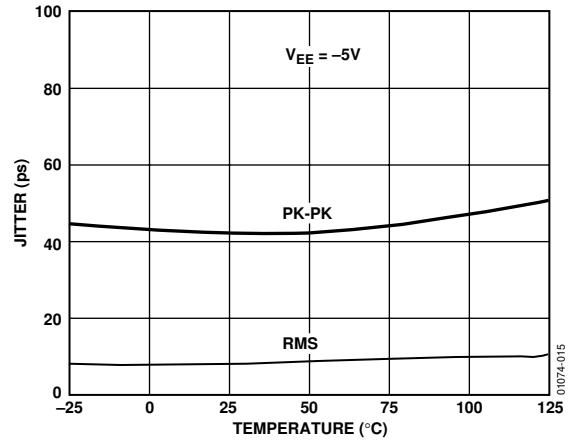


Figure 15. Jitter vs. Temperature 1.5 Gbps, PRBS 23

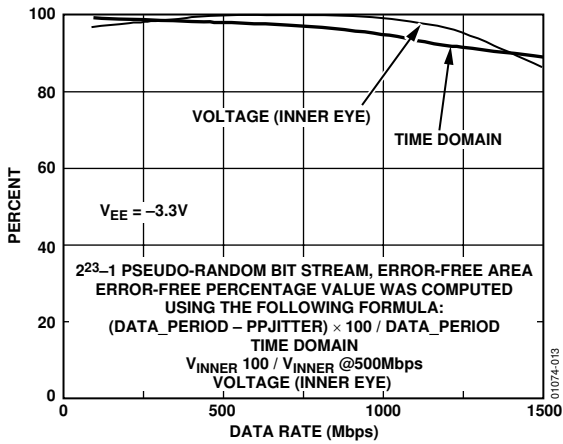


Figure 13. AC Performance

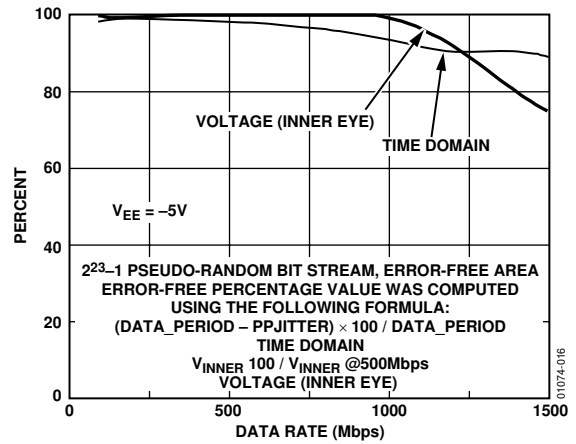


Figure 16. AC Performance

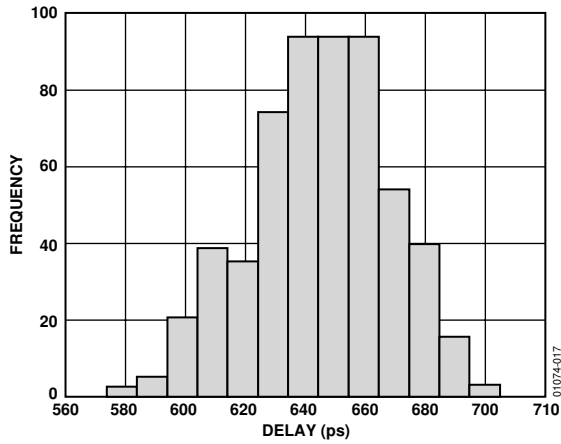


Figure 17. Variation in Channel-to-Channel Delay, All 561 Points

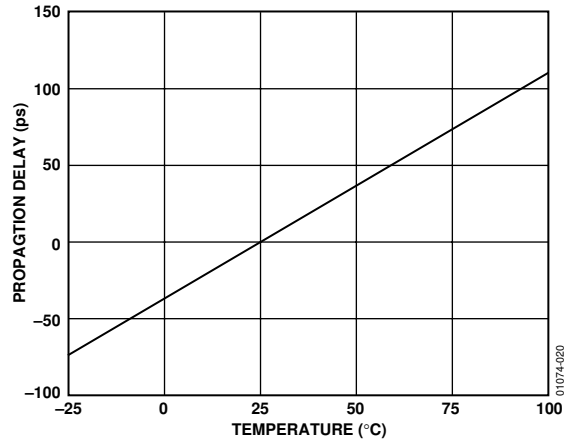


Figure 20. Propagation Delay, Normalized at 25°C vs. Temperature

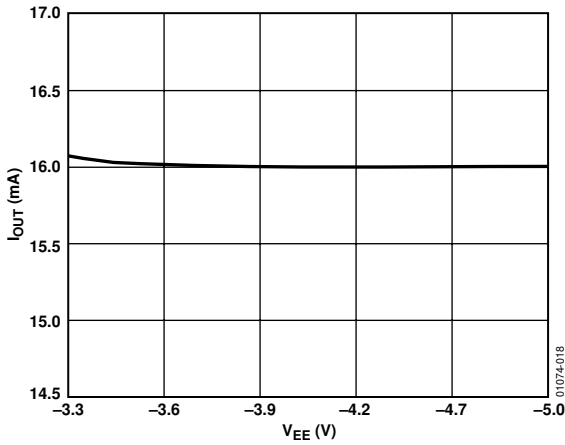


Figure 18. I_{OUT} vs. Supply, V_{EE}

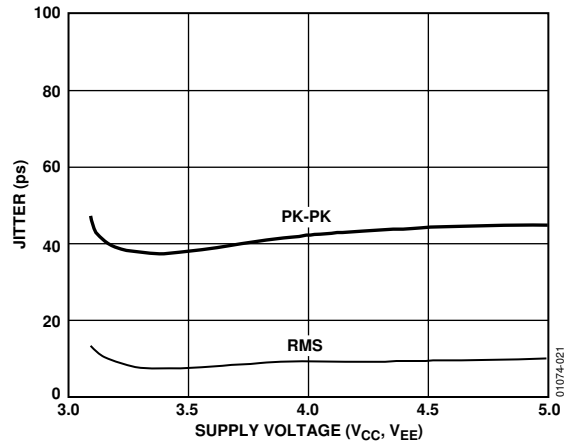


Figure 21. Jitter vs. Supply 1.5 Gbps, PRBS 23

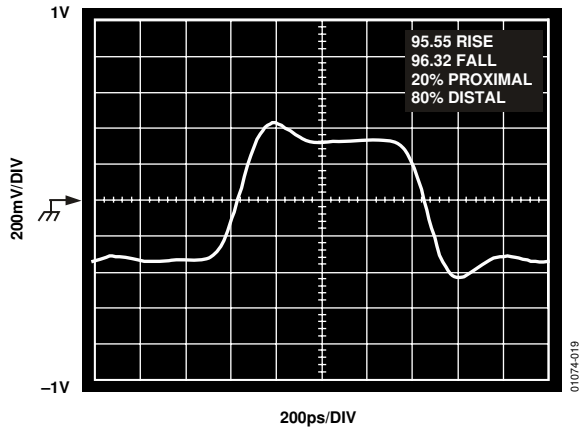


Figure 19. Rise/Fall Times, $V_{EE} = -3.3 V$

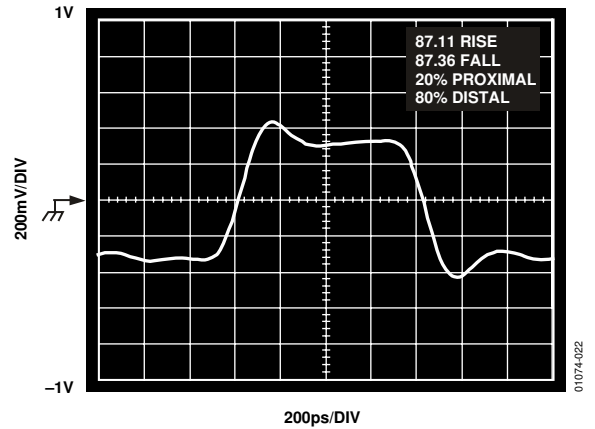


Figure 22. Rise/Fall Times, $V_{EE} = -5 V$

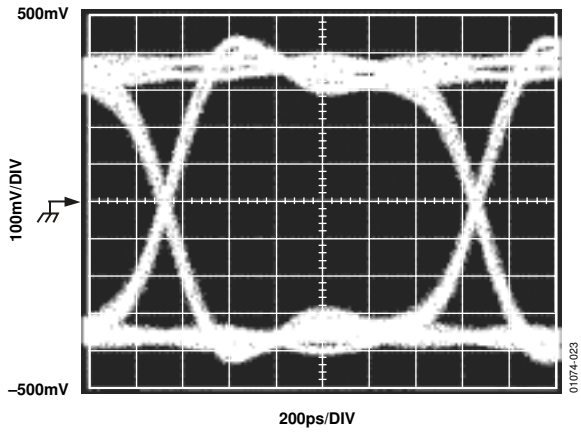


Figure 23. Eye Pattern, $V_{EE} = -3.3\text{ V}$, 1.5 Gbps PRBS 23

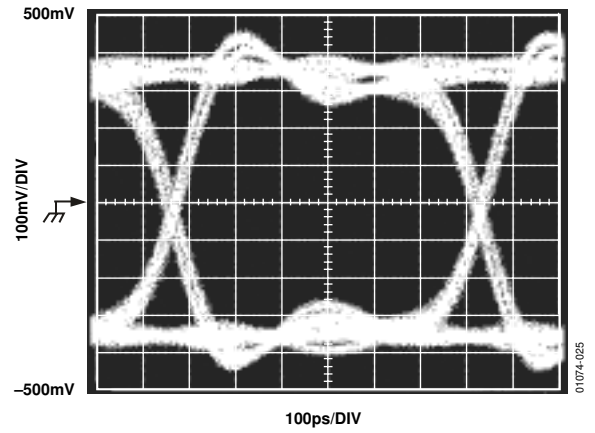


Figure 24. Eye Pattern, $V_{EE} = -5\text{ V}$, 1.5 Gbps PRBS 23

TEST CIRCUIT

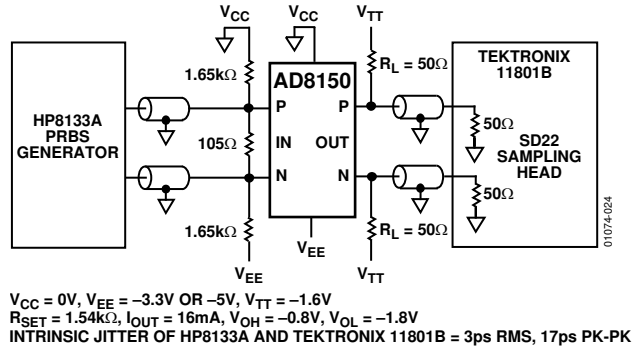


Figure 25. Eye Pattern Test Circuit

CONTROL INTERFACE

CONTROL INTERFACE TRUTH TABLES

The following are truth tables for the control interface.

Table 4. Basic Control Functions

Control Pins					Function
RESET	CS	WE	RE	UPDATE	
0	X	X	X	X	Global Reset. Reset all second-rank enable bits to 0 (disable all outputs).
1	1	X	X	X	Control Disable. Ignore all logic (but the signal matrix still functions as programmed). D[6:0] are high impedance.
1	0	0	X	X	Single Output Preprogram. Write input configuration data from Data Bus D[6:0] into first rank of latches for the output selected by the Output Address Bus A[4:0].
1	0	X	0	X	Single Output Readback. Readback input configuration data from second rank of latches onto Data Bus D[6:0] for the single output selected by the Output Address Bus A[4:0].
1	0	X	X	0	Global Update. Copy input configuration data from all 17 first-rank latches into second rank of latches, updating signal matrix connections for all outputs.
1	0	0	1	0	Transparent Write and Update. It is possible to write data directly onto rank two. This simplifies logic when synchronous signal matrix updating is not necessary.

Table 5. Address Data Examples

Output Address Pins MSB to LSB					Enable Bit	Input Address Pins MSB to LSB							Function
A4	A3	A2	A1	A0		D6/E	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	X	0	0	0	0	0	0	0	Lower Address/Data Range. Connect Output 00 (A[4:0] = 00000) to Input 00 (D[5:0] = 000000).
1	0	0	0	0	X	1	0	0	0	0	0	0	Upper Address/Data Range. Connect Output 16 (A[4:0] = 10000) to Input 32 (D[5:0] = 100000).
<Binary Output Number ¹ >					1	<Binary Input Number>							Enable Output. Connect selected output (A[4:0] = 0 to 16) to designated input (D[5:0] = 0 to 32) and enable output (D6 = 1).
<Binary Output Number ¹ >					0	X	X	X	X	X	X	X	Disable Output. Disable specified output (D6 = 0).
1	0	0	0	1	X	<Binary Input Number>							Broadcast Connection. Connect all 17 outputs to the same designated input and set all 17 enable bits to the value of D6. Readback is not possible with the broadcast address.
1	0	0	1	0	X	1	0	0	0	0	0	1	Reserved. Any address or data code greater or equal to these are reserved for future expansion or factory testing.

¹ The binary output number may also be the broadcast connection designator, 10001X.

CONTROL INTERFACE TIMING DIAGRAMS

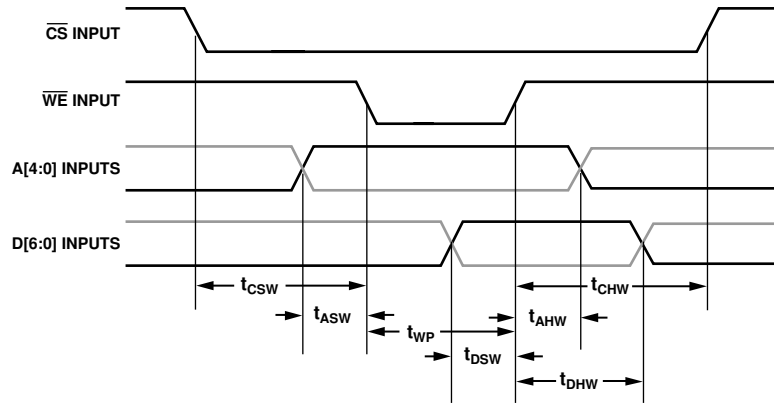


Figure 26. First-Rank Write Cycle

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Table 6. First-Rank Write Cycle

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CSW}	Setup Time	Chip select to write enable	0			ns
t_{ASW}		Address to write enable	0			ns
t_{DSW}		Data to write enable	15			ns
t_{CHW}	Hold Time	Chip select from write enable	0			ns
t_{AHW}		Address from write enable	0			ns
t_{DHW}		Data from write enable	0			ns
t_{WP}	Width of Write Enable Pulse		15			ns

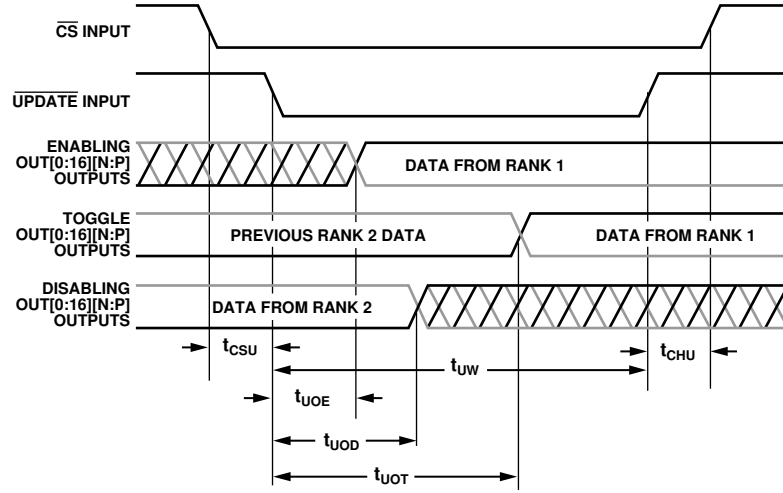


Figure 27. Second-Rank Update Cycle

Table 7. Second-Rank Update Cycle

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CSU}	Setup Time	Chip select to update	0			ns
t_{CHU}	Hold Time	Chip select from update	0			ns
t_{UOE}	Output Enable Times	Update to output enable		25	40	ns
t_{UOT}	Output Toggle Times	Update to output reprogram		25	40	ns
t_{UOD}	Output Disable Times	Update to output disabled		25	30	ns
t_{UW}	Width of Update Pulse		15			ns

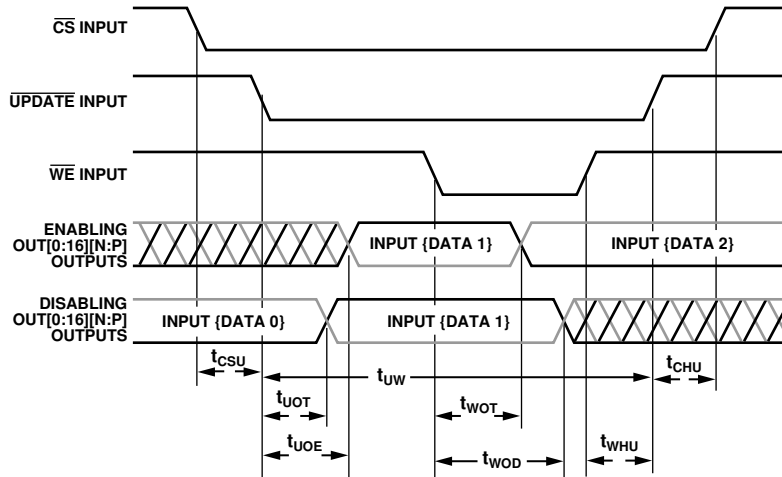


Figure 28. First-Rank Write Cycle and Second-Rank Update Cycle

Table 8. First-Rank Write Cycle and Second-Rank Update Cycle

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CSU}	Setup Time	Chip select to update	0			ns
t_{CHU}	Hold Time	Chip select from update	0			ns
t_{UOE}	Output Enable Times	Update to output enable		25	40	ns
t_{WOE}^1		Write enable to output enable		25	40	ns
t_{UOT}	Output Toggle Times	Update to output reprogram		25	30	ns
t_{WOT}		Write enable to output reprogram		25	30	ns
t_{UOD}^1	Output Disable Times	Update to output disabled		25	30	ns
t_{WOD}		Write enable to output disabled		25	30	ns
t_{WHU}	Setup Time	Write enable to update	10			ns
t_{UW}	Width of Update Pulse		15			ns

¹ Not shown.

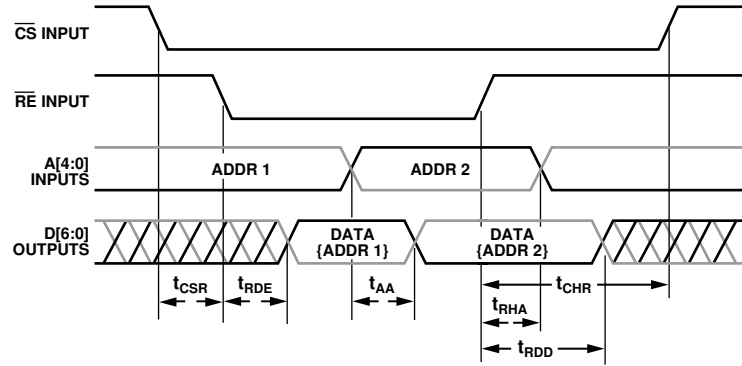
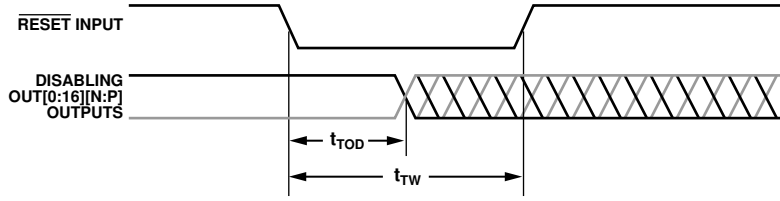


Figure 29. Second-Rank Readback Cycle

Table 9. Second-Rank Readback Cycle

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CSR}	Setup Time	Chip select to read enable	0			ns
t_{CHR}	Hold Time	Chip select from read enable	0			ns
t_{RHA}		Address from read enable	5			ns
t_{RDE}	Enable Time	Data from read enable		15		ns
t_{AA}	Access Time	Data from address		15		ns
t_{RDD}	Release Time	Data from read enable		15	30	ns



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Figure 30, Asynchronous Reset

Table 10. Asynchronous Reset

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{TOD}	Disable Time	Output disable from reset		25	30	ns
t_{TW}	Width of Reset Pulse		15			ns

AD8150

CONTROL INTERFACE PROGRAMMING EXAMPLE

The following conservative pattern connects all outputs to Input 7, except Output 16, which is connected to Input 32. The vector clock period, T_0 , is 15 ns. It is possible to accelerate the execution of this pattern by deleting Vectors 1, 4, 7, and 9.

Table 11. Basic Test Pattern

Vector No.	RESET	CS	WE	RE	UPDATE	A[4:0]	D[6:0]	Comments
0	0	1	1	1	1	xxxxx	xxxxxxx	Disable all outputs
1	1	1	1	1	1	xxxxx	xxxxxxx	
2	1	0	1	1	1	10001	1000111	All outputs to Input 07
3	1	0	0	1	1	10001	1000111	Write to first rank
4	1	0	1	1	1	10001	1000111	
5	1	0	1	1	1	10000	1100000	Output 16 to Input 32
6	1	0	0	1	1	10000	1100000	Write to first rank
7	1	0	1	1	1	10000	1100000	
8	1	0	1	1	0	xxxxx	xxxxxxx	Transfer to second rank
9	1	0	1	1	1	xxxxx	xxxxxxx	
10	1	1	1	1	1	xxxxx	xxxxxxx	Disable interface

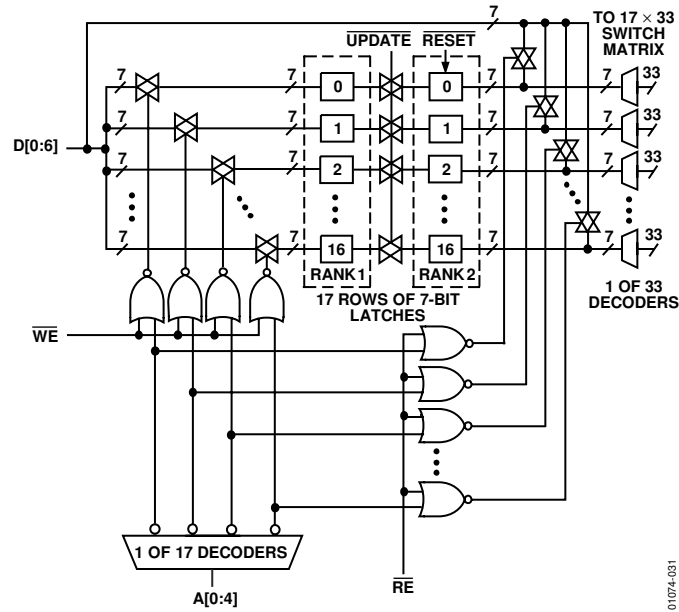


Figure 31. Control Interface (Simplified Schematic)

CONTROL INTERFACE DESCRIPTION

The AD8150 control interface receives and stores the desired connection matrix for the 33 input and 17 output signal pairs. The interface consists of 17 rows of double-rank 7-bit latches, one row for each output. The 7-bit data-word stored in each of these latches indicates to which (if any) of the 33 inputs the output will be connected.

One output at a time can be preprogrammed by addressing the output and writing the desired connection data into the first rank of latches. This process can be repeated until each of the desired output changes has been preprogrammed. All output connections can then be programmed at once by passing the data from the first rank of latches into the second rank. The output connections always reflect the data programmed into the second rank of latches and do not change until the first rank of data is passed into the second rank.

If necessary for system verification, the data in the second rank of latches can be read back from the control interface.

At any time, a reset pulse can be applied to the control interface to globally reset the appropriate second-rank data bits, disabling all 17 signal output pairs. This feature can be used to avoid output bus contention on system start-up. The contents of the first rank remain unchanged.

The control interface pins are connected via logic-level translators. These translators allow programming and readback of the control interface using logic levels different from those in the signal matrix.

To facilitate multiple chip address decoding, there is a chip-select pin. All logic signals except the reset pulse are ignored unless the chip-select pin is active. The chip-select pin disables only the control logic interface and does not change the operation of the signal matrix. The chip-select pin does not power down any of the latches, so any data programmed in the latches is preserved.

All control pins are level-sensitive, not edge-triggered.

CONTROL PIN DESCRIPTION

A[4:0] Inputs

Output address pins. The binary encoded address applied to these five input pins determines which one of the 17 outputs is being programmed (or being read back). The most significant bit is A4.

D[6:0] Inputs/Outputs

Input configuration data pins. In write mode, the binary encoded data applied to Pins D[6:0] determine which one of 33 inputs is to be connected to the output specified with the A[4:0] pins. The most significant bit is D5, and the least significant bit is D0. Bit D6 is the enable bit, setting the specified output signal pair to an enabled state if D6 is logic high, or to a disabled state, high impedance, if D6 is logic low.

In readback mode, Pins D[6:0] are low impedance outputs, indicating the data-word stored in the second rank for the output specified with the A[4:0] pins. The readback drivers were designed to drive high impedances only, so external drivers connected to D[6:0] should be disabled during readback mode.

WE Input

First-rank write enable. Forcing this pin to logic LOW allows the data on Pins D[6:0] to be stored in the first-rank latch for the output specified by Pins A[4:0]. The WE pin must be returned to a logic high state after a write cycle to avoid overwriting the first-rank data.

UPDATE Input

Second-rank write enable. Forcing this pin to logic low allows the data stored in all 17 first-rank latches to be transferred to the second-rank latches. The signal connection matrix will be reprogrammed when the second-rank data is changed. This is a global pin, transferring all 17 rows of data at once. It is not necessary to program the address pins. It should be noted that after initial power-up of the device, the first-rank data is undefined. It may be desirable to preprogram all seventeen outputs before performing the first update cycle.

\overline{RE} Input

Second-rank read enable. Forcing this pin to logic low enables the output drivers on the bidirectional D[6:0] pins, entering the readback mode of operation. By selecting an output address with the A[4:0] pins and forcing \overline{RE} to logic low, the 7-bit data stored in the second-rank latch for that output address will be written to the D[6:0] pins. Data should not be written to the D[6:0] pins externally while in readback mode. The \overline{RE} and \overline{WE} pins are not exclusive and may be used at the same time, but data should not be written to the D[6:0] pins from external sources while in readback mode.

\overline{CS} Input

Chip select. This pin must be forced to logic low to program or receive data from the logic interface, with the exception of the \overline{RESET} pin, described below. This pin has no effect on the signal pairs and does not alter any of the stored control data.

\overline{RESET} Input

Global output disable pin. Forcing the \overline{RESET} pin to logic low will reset the enable bit, D6, in all 17 second-rank latches, regardless of the state of any other pins. This has the effect of immediately disabling the 17 output signal pairs in the matrix.

It is useful to momentarily hold \overline{RESET} at a logic low state when powering up the AD8150 in a system that has multiple output signal pairs connected together. Failure to do this may result in several signal outputs contending after power-up. The reset pin is not gated by the state of the chip-select pin, \overline{CS} . It should be noted that the \overline{RESET} pin does not program the first rank, which will contain undefined data after power-up.

CONTROL INTERFACE TRANSLATORS

The AD8150 control interface has two supply pins, V_{DD} and V_{SS} . The potential between the positive logic supply V_{DD} and the negative logic supply V_{SS} must be at least 3 V and no more than 5 V. Regardless of supply, the logic threshold is approximately 1.6 V above V_{SS} , allowing the interface to be used with most CMOS and TTL logic drivers.

The signal matrix supplies, V_{CC} and V_{EE} , can be set independent of the voltage on V_{DD} and V_{SS} , with the constraints that $(V_{DD} - V_{EE}) \leq 10$ V. These constraints will allow operation of the control interface on 3 V or 5 V while the signal matrix is operated on 3.3 V or 5 V PECL, or on -3.3 V or -5 V ECL.

CIRCUIT DESCRIPTION

The AD8150 is a high speed 33×17 differential crosspoint switch designed for data rates up to 1.5 Gbps per channel. The AD8150 supports PECL-compatible input and output levels when operated from a 5 V supply ($V_{CC} = 5\text{ V}$, $V_{EE} = \text{GND}$) or ECL-compatible levels when operated from a -5 V supply ($V_{CC} = \text{GND}$, $V_{EE} = -5\text{ V}$). To save power, the AD8150 can run from a 3.3 V supply to interface with low voltage PECL circuits or a -3.3 V supply to interface with low voltage ECL circuits. The AD8150 utilizes differential current-mode outputs with individual disable control, which facilitates busing together the outputs of multiple AD8150s to assemble larger switch arrays. This feature also reduces the system to assemble larger switch arrays, reduces system crosstalk, and can greatly reduce power dissipation in a large switch array. A single external resistor programs the current for all enabled output stages, allowing for user control over output levels with different output termination schemes and transmission line characteristic impedances.

HIGH SPEED DATA INPUTS (INxxP, INxxN)

The AD8150 has 33 pairs of differential voltage-mode inputs. The common-mode input range extends from the positive supply voltage (V_{CC}) down to include standard ECL or PECL input levels ($V_{CC} - 2\text{ V}$). The minimum differential input voltage is less than 300 mV. Unused inputs may be connected directly to any level within the allowed common-mode input range. A simplified schematic of the input circuit is shown in Figure 32.

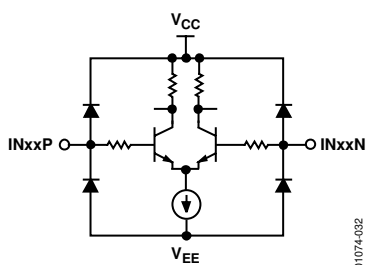


Figure 32. Simplified Input Circuit

To maintain signal fidelity at the high data rates supported by the AD8150, the input transmission lines should be terminated as close to the input pins as possible. The preferred input termination structure will depend primarily on the application and the output circuit of the data source. Standard ECL components have open emitter outputs that require pull-down resistors. Three input termination networks suitable for this type of source are shown in Figure 33. The characteristic impedance of the transmission line is shown as Z_0 . The resistors, R_1 and R_2 , in the Thevenin termination are chosen to synthesize a V_{TT} source with an output resistance of Z_0 and an open-circuit output voltage equal to $V_{CC} - 2\text{ V}$. The load

resistors (R_L) in the differential termination scheme are needed to bias the emitter followers of the ECL source.

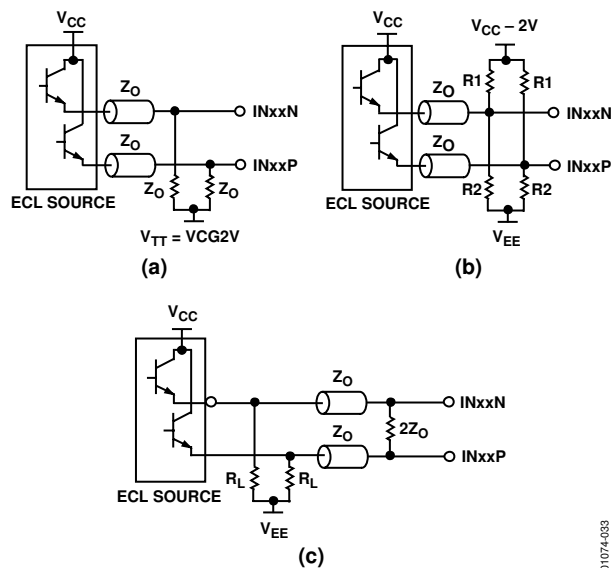


Figure 33. AD8150 Input Termination from ECL/PECL Sources: a) Parallel Termination Using V_{TT} Supply; b) Thevenin Equivalent Termination; and c) Differential Termination

If the AD8150 is driven from a current-mode output stage such as another AD8150, the input termination should be chosen to accommodate that type of source, as explained in the following section.

HIGH SPEED DATA OUTPUTS (OUTyyP, OUTyyN)

The AD8150 has 17 pairs of differential current-mode outputs. The output circuit, shown in Figure 34, is an open-collector NPN current switch with resistor-programmable tail current and output compliance extending from the positive supply voltage (V_{CC}) down to standard ECL or PECL output levels ($V_{CC} - 2\text{ V}$). The outputs may be disabled individually to permit outputs from multiple AD8150's to be connected directly. Since the output currents of multiple enabled output stages connected in this way sum, care should be taken to ensure that the output compliance limit is not exceeded at any time; this can be achieved by disabling the active output driver before enabling an inactive driver.

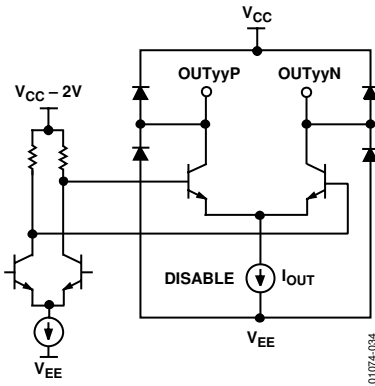


Figure 34. Simplified Output Circuit

To ensure proper operation, all outputs (including unused output) must be pulled high, using external pull-up networks, to a level within the output compliance range. If outputs from multiple AD8150s are wired together, a single pull-up network may be used for each output bus. The pull-up network should be chosen to keep the output voltage levels within the output compliance range at all times. Recommended pull-up networks to produce PECL/ECL 100K- and 10K-compatible outputs are shown in Figure 35. Alternatively, a separate supply can be used to provide V_{COM} , making R_{COM} and D_{COM} unnecessary.

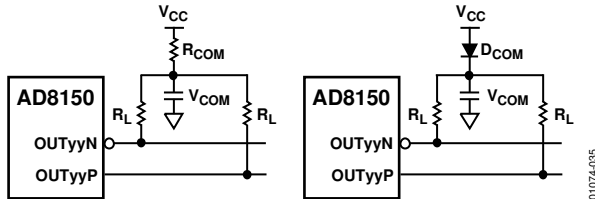


Figure 35. Output Pull-Up Networks: a) ECL 100K, b) ECL 10K

The output levels are simply:

$$\begin{aligned}
 V_{OH} &= V_{COM} \\
 V_{OL} &= V_{COM} - I_{OUT}R_L \\
 V_{SWING} &= V_{OH} - V_{OL} = I_{OUT}R_L \\
 V_{COM} &= V_{CC} - I_{OUT}R_{COM} \text{ (100K Mode)} \\
 V_{COM} &= V_{CC} - V(D_{COM}) \text{ (10K Mode)}
 \end{aligned}$$

The common-mode adjustment element (R_{COM} or D_{COM}) may be omitted if the input range of the receiver includes the positive supply voltage. The bypass capacitors reduce common-mode perturbations by providing an ac short from the common nodes (V_{COM}) to ground.

When busing together the outputs of multiple AD8150s or when running at high data rates, double termination of its outputs is recommended to mitigate the impact of reflections due to open transmission line stubs and the lumped capacitance of the AD8150 output pins. A possible connection is shown in Figure 36; the bypass capacitors provide an ac short from the common nodes of the termination resistors to ground.

maintain signal fidelity at high data rates, the stubs connecting the output pins to the output transmission lines or load resistors should be as short as possible.

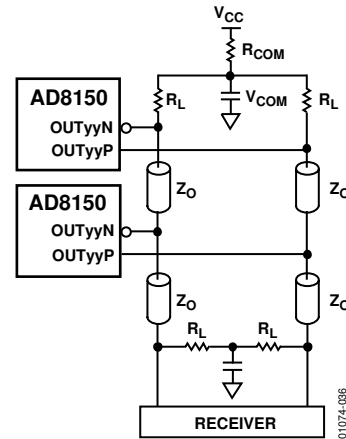


Figure 36. Double Termination of AD8150 Outputs

In this case, the output levels are:

$$\begin{aligned}
 V_{OH} &= V_{COM} - (1/4)I_{OUT}R_L \\
 V_{OL} &= V_{COM} - (3/4)I_{OUT}R_L \\
 V_{SWING} &= V_{OH} - V_{OL} = (1/2)I_{OUT}R_L
 \end{aligned}$$

OUTPUT CURRENT SET PIN (REF)

A simplified schematic of the reference circuit is shown in Figure 37. A single external resistor connected between the REF pin and V_{EE} determines the output current for all output stages. This feature allows a choice of pull-up networks and transmission line characteristic impedances while still achieving a nominal output swing of 800 mV. At low data rates, substantial power savings can be achieved by using lower output swings and higher load resistances.

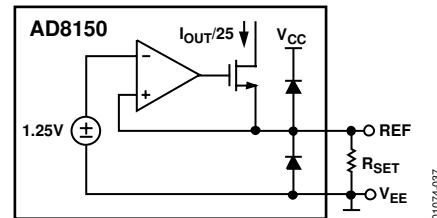


Figure 37. Simplified Reference Circuit