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# Xstream™ 33 × 17, 3.2 Gbps Digital Crosspoint Switch

# AD8151

## FEATURES

**Low cost**
**33 × 17, fully differential, nonblocking array**
**3.2 Gbps per port NRZ data rate**
**Wide power supply range: +3.3 V, –3.3 V**
**Low power**
**425 mA (outputs enabled)**
**35 mA (outputs disabled)**
**LV PECL- and LV ECL-compatible**
**CMOS/TTL-level control inputs: 3 V to 5 V**
**Low jitter**
**No heat sinks required**
**Drives a backplane directly**
**Programmable output current**
**Optimize termination impedance**
**User-controlled voltage at the load**
**Minimize power dissipation**
**Individual output disable for busing and reducing power**
**Double row latch**
**Buffered inputs**
**184-lead LQFP package**

## APPLICATIONS

**High speed serial backplane routing to Sonet OC-48 applications with FEC**
**Fiber optic network switching**
**Fiber channel**
**LVDS**

## FUNCTIONAL BLOCK DIAGRAM

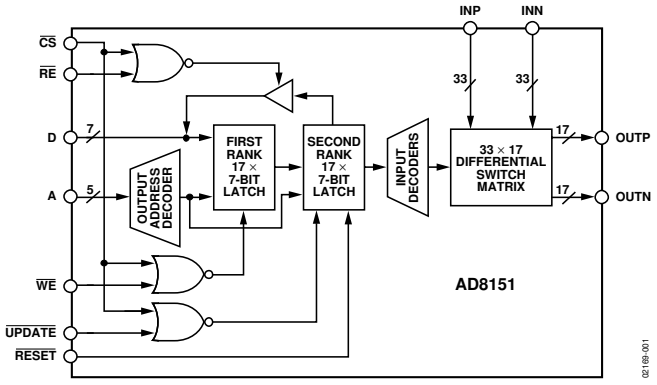


*Figure 1.*

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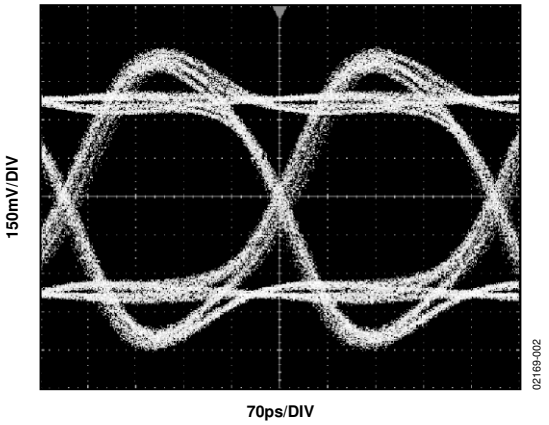


*Figure 2. Eye Pattern, 3.2 Gbps, PRBS 23*

## GENERAL DESCRIPTION

The AD8151[1] is a member of the Xstream line of products, offering a breakthrough in digital switching and a large switch array (33 × 17) on very little power—typically less than 1.5 W. It also operates at data rates in excess of 3.2 Gbps per port, making it suitable for Sonet OC-48 applications with 8/10-bit forward-error correction (FEC). Furthermore, the price of the AD8151 makes it affordable enough to be used for lower data rates. The AD8151's flexible supply voltages allow the user to operate with either emitter-coupled logic (ECL) or positive emitter-coupled logic (PECL) data levels, and with 3.3 V for further power reduction. The control interface is CMOS-/TTL-compatible (3 V to 5 V).

Its fully differential signal path reduces jitter and crosstalk, while allowing the use of smaller, single-ended voltage swings. The AD8151 is offered in a 184-lead LQFP package that operates over the extended commercial temperature range of 0°C to 85°C.

[1] Patent pending.

**Rev. B**
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View a parametric search of comparable parts.

## EVALUATION KITS

- AD8151 Evaluation Board

## DOCUMENTATION

**Data Sheet**

- AD8151: X Stream™ 33 x 17, 3.2Gbps Digital Crosspoint Switch Data Sheet

## REFERENCE MATERIALS

**Informational**

- Optical and High Speed Networking ICs

## DESIGN RESOURCES

- AD8151 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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**9/05—Rev. 0 to Rev. A**

Updated Format ..... Universal
Change to Figure 51 ..... 34
Change to Ordering Guide ..... 37

**4/01—Revision 0: Initial Version**

# SPECIFICATIONS

@ 25°C, $V_{CC}$ = 3.3 V to 5 V, $V_{EE}$ = 0 V, $R_L$ = 50 Ω (see Figure 26), $I_{OUT}$ = 16 mA, unless otherwise noted.

**Table 1.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| Max Data Rate/Channel (NRZ) | | 2.5 | 3.2 | | Gbps |
| Channel Jitter | Data rate = 3.2 Gbps | | 52 | | ps p-p |
| RMS Channel Jitter | | | 8 | | ps |
| Propagation Delay | Input to output | | 650 | | ps |
| Propagation Delay Match | See Figure 23 | | ±50 | ±100 | ps |
| Output Rise/Fall Time | 20% to 80% | | 100 | | ps |
| INPUT CHARACTERISTICS | | | | | |
| Input Voltage Swing | Single-ended (see Figure 18) | 200 | | 1000 | mV p-p |
| Input Bias Current | | | 2 | | µA |
| Input Capacitance | | | 2 | | pF |
| Input $V_{IN}$ High | | $V_{CC}$ – 1.2 | | $V_{CC}$ | V |
| Input $V_{IN}$ Low | | $V_{CC}$ – 2.4 | | $V_{CC}$ – 1.4 | V |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing | Differential | | 800 | | mV p-p |
| Output Voltage Range | (See Figure 19) | $V_{CC}$ – 1.8 | | $V_{CC}$ | V |
| Output Current | | 5 | | 25 | mA |
| Output Capacitance | | | 2 | | pF |
| Output $V_{OUT}$ High | | $V_{CC}$ – 1.8 | | | V |
| Output $V_{OUT}$ Low | | | | $V_{CC}$ | V |
| POWER SUPPLY | | | | | |
| Operating Range | | | | | |
| PECL, $V_{CC}$ | $V_{EE}$ = 0 V | 3.0 | | 5.25 | V |
| ECL, $V_{EE}$ | $V_{CC}$ = 0 V | –5.25 | | –3.0 | V |
| $V_{DD}$ | | 3 | | 5 | V |
| $V_{SS}$ | | | 0 | | V |
| Quiescent Current | | | | | |
| $V_{DD}$ | | | 2 | | mA |
| $V_{EE}$ | All outputs enabled, $I_{OUT}$ = 16 mA | | 425 | | mA |
| | $T_{MIN}$ to $T_{MAX}$ | | | 450 | mA |
| | All outputs disabled | | 35 | | mA |
| THERMAL CHARACTERISTICS | | | | | |
| Operating Temperature Range | | 0 | | 85 | °C |
| $\theta_{JA}$ | | | 30 | | °C/W |
| LOGIC INPUT CHARACTERISTICS | $V_{DD}$ = 3 V dc to 5 V dc | | | | |
| Input $V_{IN}$ High | | 1.9 | | $V_{DD}$ | V |
| Input $V_{IN}$ Low | | 0 | | 0.9 | V |

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 2.**

| Parameter | Rating |
|---|---|
| Supply Voltage | |
| $V_{DD} - V_{EE}$ | 10.5 V |
| $V_{CC} - V_{EE}$ | 5.5 V |
| $V_{DD} - V_{SS}$ | 5.5 V |
| $V_{SS} - V_{EE}$ | 5.5 V |
| $V_{SS} - V_{CC}$ | 5.5 V |
| $V_{DD} - V_{CC}$ | 5.5 V |
| Internal Power Dissipation | |
| 184-Lead LQFP (ST-184) | 4.2 W |
| Differential Input Voltage | 2.0 V |
| Storage Temperature Range | –65°C to +125°C |
| Lead Temperature (Soldering 10 sec) | 300°C |
| Junction Temperature, $\theta_{JA}$ | 30°C/W |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8151 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 3.

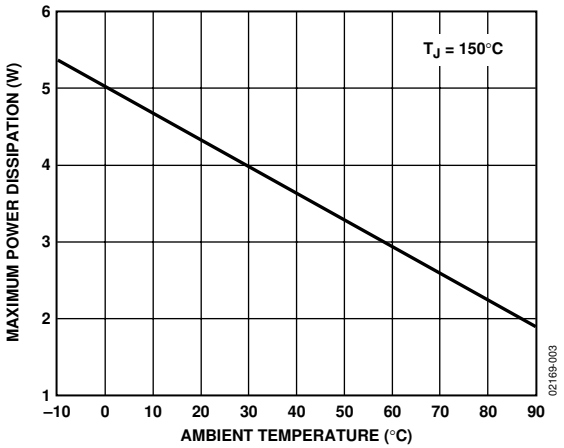


*Figure 3.*

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

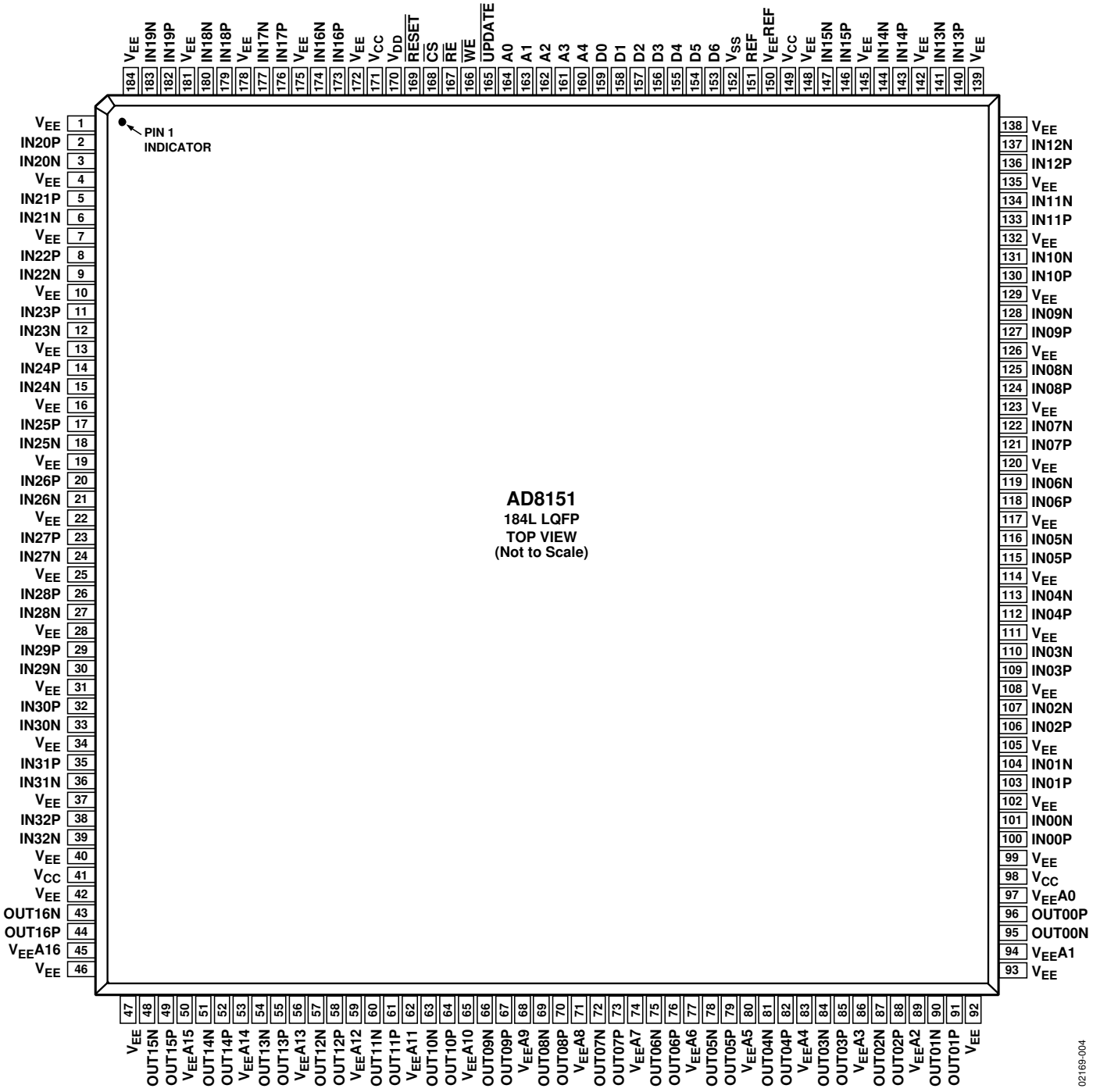


*Figure 4. Pin Configuration*

**Table 3. Pin Function Descriptions**

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| 1, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31, 34, 37, 40, 42, 46, 47, 92, 93, 99, 102, 105, 108, 111, 114, 117, 120, 123, 126, 129, 132, 135, 138, 139, 142, 145, 148, 172, 175, 178, 181, 184 | $V_{EE}$ | Power Supply | Most Negative PECL Supply (Common with Other Points Labeled $V_{EE}$) |
| 2 | IN20P | PECL/ECL | High Speed Input |
| 3 | IN20N | PECL/ECL | High Speed Input Complement |
| 5 | IN21P | PECL/ECL | High Speed Input |
| 6 | IN21N | PECL/ECL | High Speed Input Complement |
| 8 | IN22P | PECL/ECL | High Speed Input |
| 9 | IN22N | PECL/ECL | High Speed Input Complement |
| 11 | IN23P | PECL/ECL | High Speed Input |
| 12 | IN23N | PECL/ECL | High Speed Input Complement |
| 14 | IN24P | PECL/ECL | High Speed Input |
| 15 | IN24N | PECL/ECL | High Speed Input Complement |
| 17 | IN25P | PECL/ECL | High Speed Input |
| 18 | IN25N | PECL/ECL | High Speed Input Complement |
| 20 | IN26P | PECL/ECL | High Speed Input |
| 21 | IN26N | PECL/ECL | High Speed Input Complement |
| 23 | IN27P | PECL/ECL | High Speed Input |
| 24 | IN27N | PECL/ECL | High Speed Input Complement |
| 26 | IN28P | PECL/ECL | High Speed Input |
| 27 | IN28N | PECL/ECL | High Speed Input Complement |
| 29 | IN29P | PECL/ECL | High Speed Input |
| 30 | IN29N | PECL/ECL | High Speed Input Complement |
| 32 | IN30P | PECL/ECL | High Speed Input |
| 33 | IN30N | PECL/ECL | High Speed Input Complement |
| 35 | IN31P | PECL/ECL | High Speed Input |
| 36 | IN31N | PECL/ECL | High Speed Input Complement |
| 38 | IN32P | PECL/ECL | High Speed Input |
| 39 | IN32N | PECL/ECL | High Speed Input Complement |
| 41, 98, 149, 171 | $V_{CC}$ | Power Supply | Most Positive PECL Supply (Common with Other Points Labeled $V_{CC}$) |
| 43 | OUT16N | PECL/ECL | High Speed Output Complement |
| 44 | OUT16P | PECL/ECL | High Speed Output |
| 45 | $V_{EE}$A16 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 48 | OUT15N | PECL/ECL | High Speed Output Complement |
| 49 | OUT15P | PECL/ECL | High Speed Output |
| 50 | $V_{EE}$A15 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 51 | OUT14N | PECL/ECL | High Speed Output Complement |
| 52 | OUT14P | PECL/ECL | High Speed Output |
| 53 | $V_{EE}$A14 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 54 | OUT13N | PECL/ECL | High Speed Output Complement |
| 55 | OUT13P | PECL/ECL | High Speed Output |
| 56 | $V_{EE}$A13 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 57 | OUT12N | PECL/ECL | High Speed Output Complement |
| 58 | OUT12P | PECL/ECL | High Speed Output |
| 59 | $V_{EE}$A12 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 60 | OUT11N | PECL/ECL | High speed Output Complement |
| 61 | OUT11P | PECL/ECL | High speed Output |
| 62 | $V_{EE}$A11 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 63 | OUT10N | PECL/ECL | High Speed Output Complement |

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| 64 | OUT10P | PECL/ECL | High Speed Output |
| 65 | $V_{EE}$A10 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 66 | OUT09N | PECL/ECL | High Speed Output Complement |
| 67 | OUT09P | PECL/ECL | High Speed Output |
| 68 | $V_{EE}$A9 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 69 | OUT08N | PECL/ECL | High speed Output Complement |
| 70 | OUT08P | PECL/ECL | High Speed Output |
| 71 | $V_{EE}$A8 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 72 | OUT07N | PECL/ECL | High Speed Output Complement |
| 73 | OUT07P | PECL/ECL | High Speed Output |
| 74 | $V_{EE}$A7 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 75 | OUT06N | PECL/ECL | High Speed Output Complement |
| 76 | OUT06P | PECL/ECL | High Speed Output |
| 77 | $V_{EE}$A6 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 78 | OUT05N | PECL/ECL | High Speed Output Complement |
| 79 | OUT05P | PECL/ECL | High Speed Output |
| 80 | $V_{EE}$A5 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 81 | OUT04N | PECL/ECL | High Speed Output Complement |
| 82 | OUT04P | PECL/ECL | High Speed Output |
| 83 | $V_{EE}$A4 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 84 | OUT03N | PECL/ECL | High Speed Output Complement |
| 85 | OUT03P | PECL/ECL | High Speed Output |
| 86 | $V_{EE}$A3 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 87 | OUT02N | PECL/ECL | High Speed Output Complement |
| 88 | OUT02P | PECL/ECL | High Speed Output |
| 89 | $V_{EE}$A2 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 90 | OUT01N | PECL/ECL | High Speed Output Complement |
| 91 | OUT01 | P PECL/ECL | High Speed Output |
| 94 | $V_{EE}$A1 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 95 | OUT00N | PECL/ECL | High Speed Output Complement |
| 96 | OUT00P | PECL/ECL | High Speed Output |
| 97 | $V_{EE}$A0 | Power Supply | Most Negative PECL Supply (Unique to this Output) |
| 100 | IN00P | PECL/ECL | High Speed Input |
| 101 | IN00N | PECL/ECL | High Speed Input Complement |
| 103 | IN01P | PECL/ECL | High Speed Input |
| 104 | IN01N | PECL/ECL | High Speed Input Complement |
| 106 | IN02P | PECL/ECL | High Speed Input |
| 107 | IN02N | PECL/ECL | High Speed Input Complement |
| 109 | IN03P | PECL/ECL | High Speed Input |
| 110 | IN03N | PECL/ECL | High Speed Input Complement |
| 112 | IN04P | PECL/ECL | High Speed Input |
| 113 | IN04N | PECL/ECL | High Speed Input Complement |
| 115 | IN05P | PECL/ECL | High Speed Input |
| 116 | IN05N | PECL/ECL | High Speed Input Complement |
| 118 | IN06P | PECL/ECL | High Speed Input |
| 119 | IN06N | PECL/ECL | High Speed Input Complement |
| 121 | IN07P | PECL/ECL | High Speed Input |
| 122 | IN07N | PECL/ECL | High Speed Input Complement |
| 124 | IN08P | PECL/ECL | High Speed Input |
| 125 | IN08N | PECL/ECL | High Speed Input Complement |
| 127 | IN09P | PECL/ECL | High Speed Input |
| 128 | IN09N | PECL/ECL | High Speed Input Complement |

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| 130 | IN10P | PECL/ECL | High Speed Input |
| 131 | IN10N | PECL/ECL | High Speed Input Complement |
| 133 | IN11P | PECL/ECL | High Speed Input |
| 134 | IN11N | PECL/ECL | High Speed Input Complement |
| 136 | IN12P | PECL/ECL | High Speed Input |
| 137 | IN12N | PECL/ECL | High Speed Input Complement |
| 140 | IN13P | PECL/ECL | High Speed Input |
| 141 | IN13N | PECL/ECL | High Speed Input Complement |
| 143 | IN14P | PECL/ECL | High Speed Input |
| 144 | IN14N | PECL/ECL | High Speed Input Complement |
| 146 | IN15P | PECL/ECL | High Speed Input |
| 147 | IN15N | PECL/ECL | High Speed Input Complement |
| 150 | $V_{EE}$REF | R Program | Connection Point for Output Logic Pull-Down Programming Resistor (Must be Connected to $V_{EE}$) |
| 151 | REF | R Program | Connection Point for Output Logic Pull-Down Programming Resistor |
| 152 | $V_{SS}$ | Power Supply | Most Negative Control Logic Supply |
| 153 | D6 | TTL | Enable/$\overline{\text{Disable}}$ Output |
| 154 | D5 | TTL | Bit 32—MSB Input Select |
| 155 | D4 | TTL | Bit 16 |
| 156 | D3 | TTL | Bit 8 |
| 157 | D2 | TTL | Bit 4 |
| 158 | D1 | TTL | Bit 2 |
| 159 | D0 | TTL | Bit 1—LSB Input Select |
| 160 | A4 | TTL | Bit 16—MSB Output Select |
| 161 | A3 | TTL | Bit 8 |
| 162 | A2 | TTL | Bit 4 |
| 163 | A1 | TTL | Bit 2 |
| 164 | A0 | TTL | Bit 1—LSB Output Select |
| 165 | $\overline{\text{UPDATE}}$ | TTL | Second Rank Program |
| 166 | $\overline{\text{WE}}$ | TTL | First Rank Program |
| 167 | $\overline{\text{RE}}$ | TTL | Enable Readback |
| 168 | $\overline{\text{CS}}$ | TTL | Enable Chip to Accept Programming |
| 169 | $\overline{\text{RESET}}$ | TTL | Disable All Outputs (Hi-Z) |
| 170 | $V_{DD}$ | Power Supply | Most Positive Control Logic Supply |
| 173 | IN16P | PECL/ECL | High Speed Input |
| 174 | IN16N | PECL/ECL | High Speed Input Complement |
| 176 | IN17P | PECL/ECL | High Speed Input |
| 177 | IN17N | PECL/ECL | High Speed Input Complement |
| 179 | IN18P | PECL/ECL | High Speed Input |
| 180 | IN18N | PECL/ECL | High Speed Input Complement |
| 182 | IN19P | PECL/ECL | High Speed Input |
| 183 | IN19N | PECL/ECL | High Speed Input Complement |

# TYPICAL PERFORMANCE CHARACTERISTICS

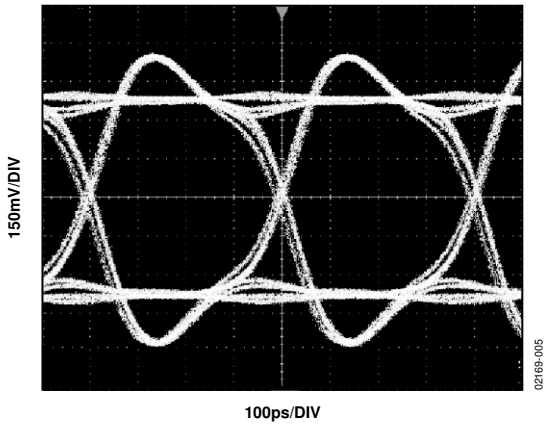


Figure 5. Eye Pattern 2.5 Gbps, PRBS 23

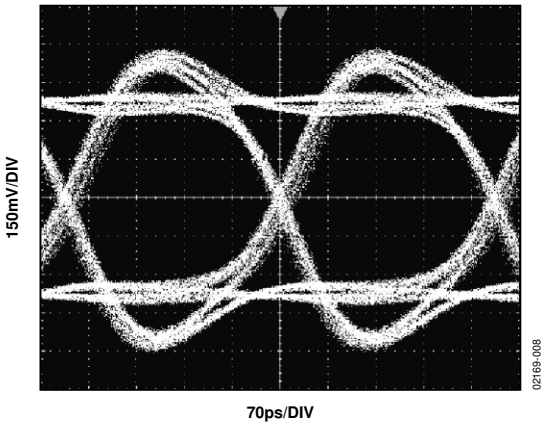


Figure 8. Eye Pattern 3.2 Gbps, PRBS 23

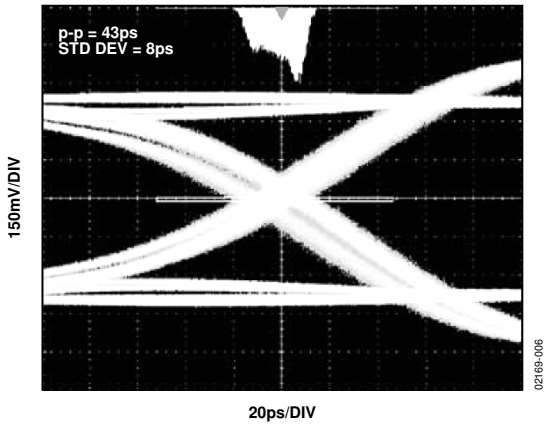


Figure 6. Jitter @ 2.5 Gbps, PRBS 23

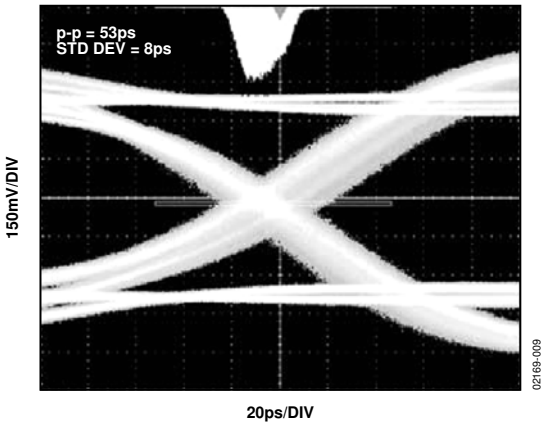


Figure 9. Jitter @ 3.2 Gbps, PRBS 23

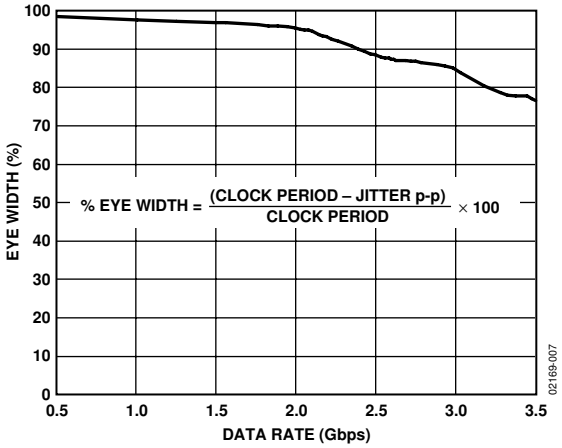


Figure 7. Eye Width vs. Data Rate, PRBS 23

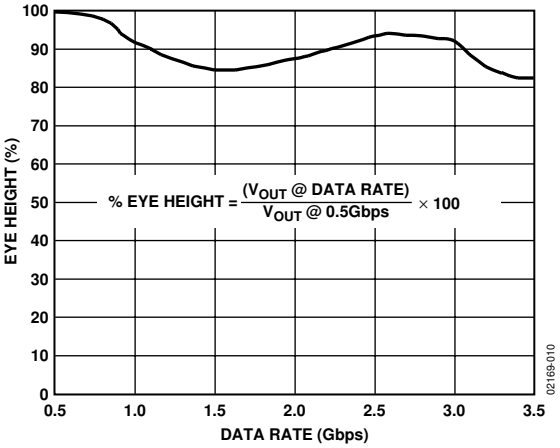


Figure 10. Eye Height vs. Data Rate, PRBS 23

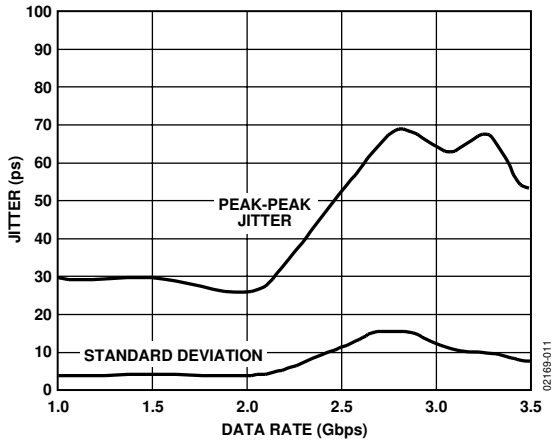


Figure 11. Jitter vs. Data Rate, PRBS 23

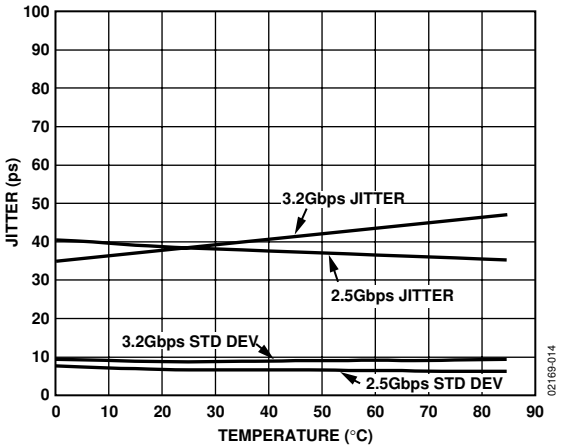


Figure 14. Jitter vs. Temperature, PRBS 23

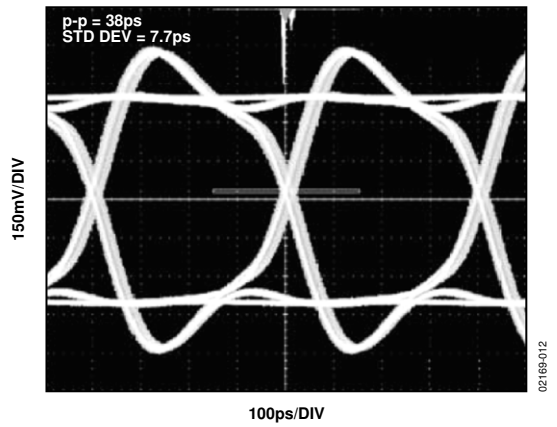


Figure 12. Crosstalk, 2.5 Gbps, PRBS 23, Attack Signal Is Off

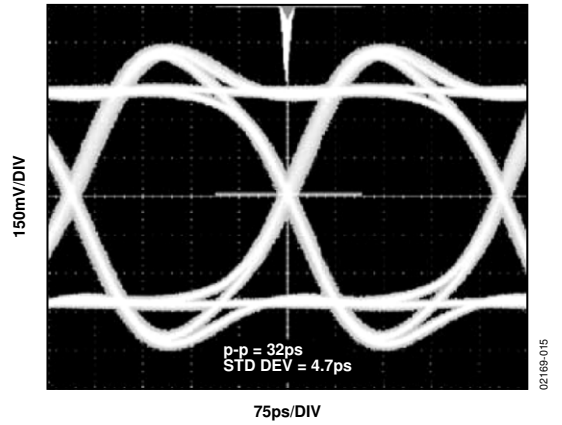


Figure 15. Crosstalk, 3.2 Gbps, PRBS 23, Attack Signal Is Off

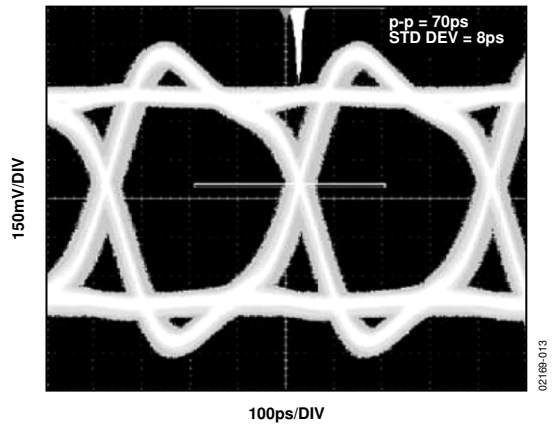


Figure 13. Crosstalk, 2.5 Gbps, PRBS 23, Attack Signal Is On

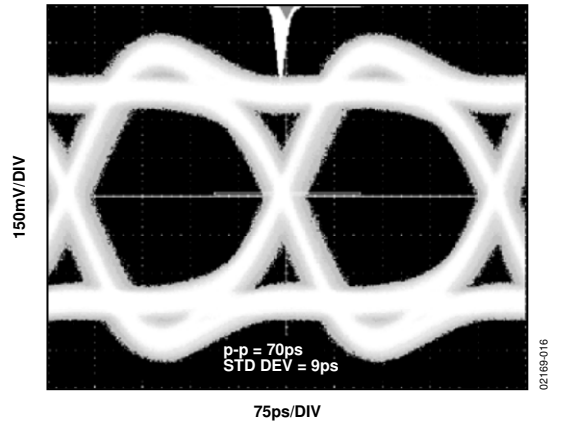


Figure 16. Crosstalk, 3.2 Gbps, PRBS 23, Attack Signal Is On

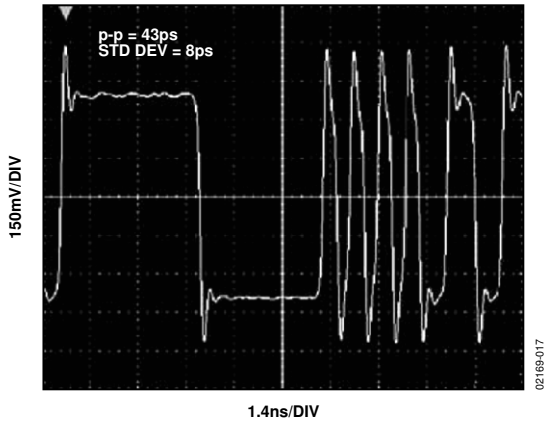


Figure 17. Response, 2.5 Gbps,
32-Bit Pattern 1111 1111 0000 0000 0101 0101 0011 0011

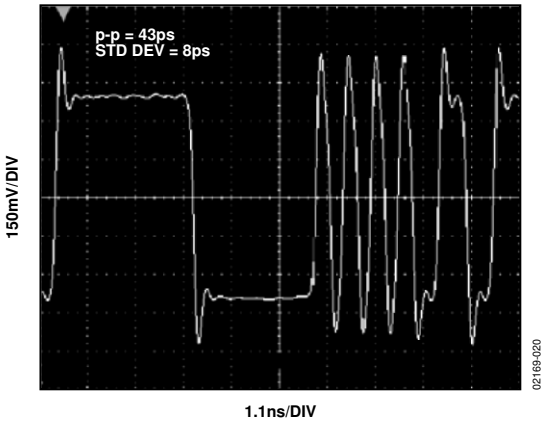


Figure 20. Response, 3.2 Gbps,
32-Bit Pattern 1111 1111 0000 0000 0101 0101 0011 0011

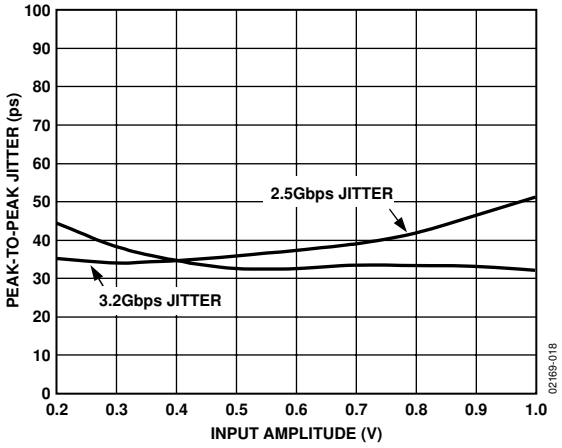


Figure 18. Jitter vs. Single-Ended Input Amplitude, PRBS 23

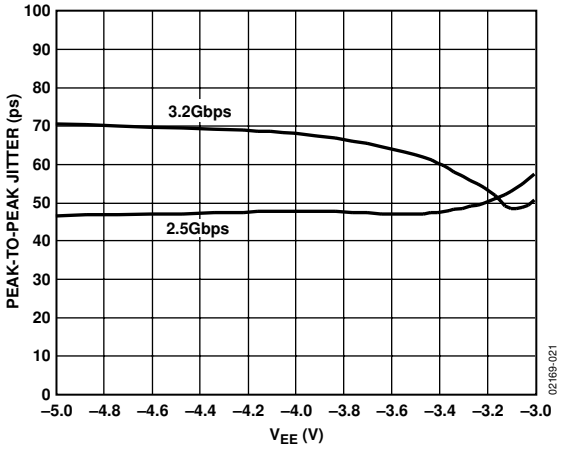


Figure 21. Jitter vs. Supply, PRBS 23

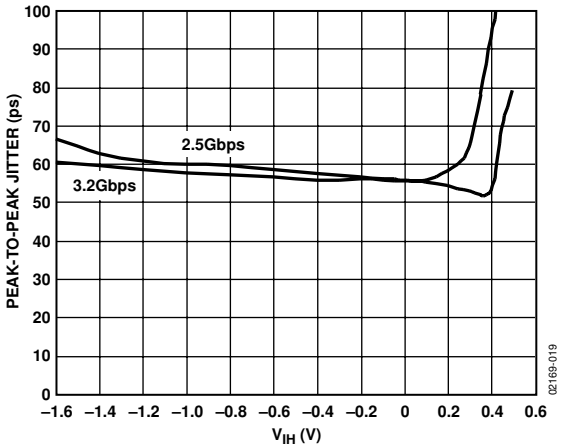


Figure 19. Jitter vs. VIH, PRBS 23

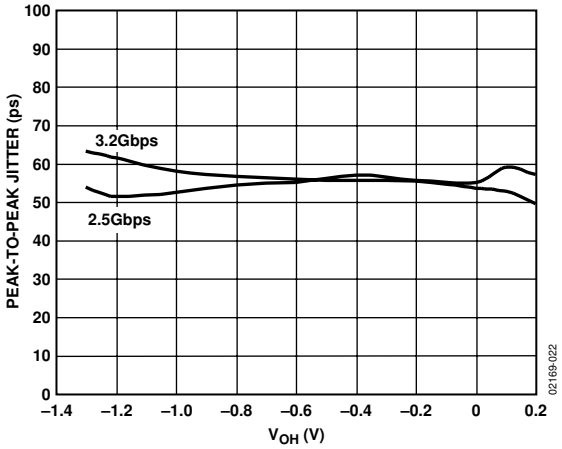


Figure 22. Jitter vs. $V_{OH}$, PRBS 23, Output Amplitude = 0.4 V Single-Ended

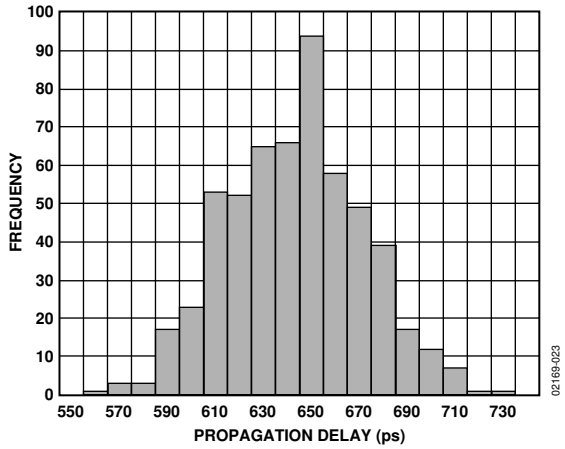


Figure 23. Variation in Channel-to-Channel Delay, All 561 Points

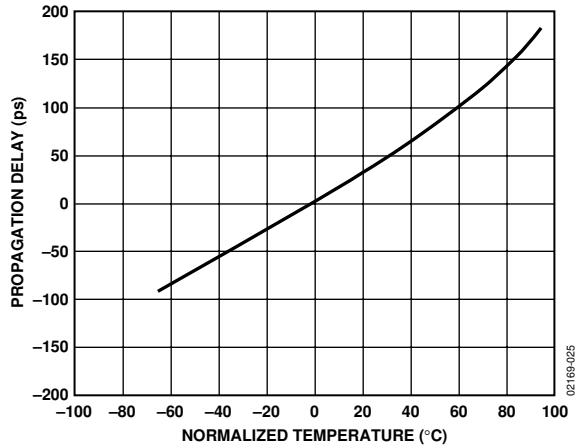


Figure 25. Propagation Delay, Normalized at 25°C vs. Temperature

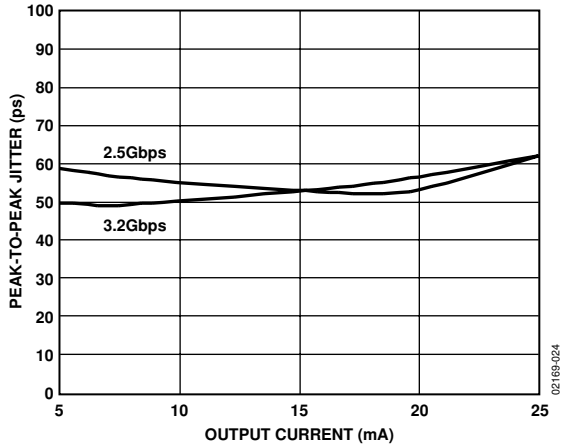


Figure 24. Jitter vs. $I_{OUT}$, PRBS 23

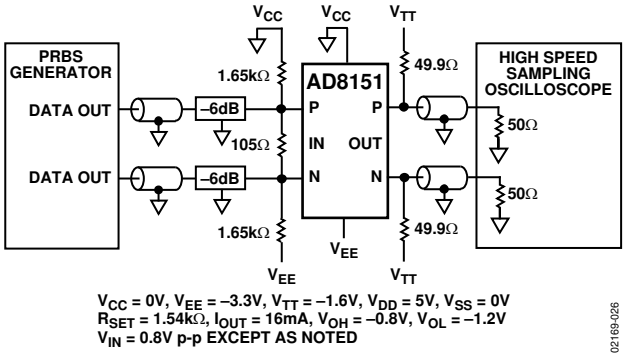


Figure 26. Test Circuit

# CONTROL INTERFACE TRUTH TABLES

**Table 4. Basic Control Functions**

| Control Pins[1] | | | | | |
|---|---|---|---|---|---|
| $\overline{\text{RESET}}$ | $\overline{\text{CS}}$ | $\overline{\text{WE}}$ | $\overline{\text{RE}}$ | $\overline{\text{UPDATE}}$ | Function |
| 0 | X | X | X | X | Global Reset. Reset all second rank enable bits to zero (disable all outputs). |
| 1 | 1 | X | X | X | Control Disable. Ignore all logic (but the signal matrix still functions as programmed). D [6:0] are high impedance. |
| 1 | 0 | 0 | 1 | 1 | Single Output Preprogram. Write input configuration data from Data Bus D [6:0] into first rank of latches for the output selected by the Output Address Bus A [4:0]. |
| 1 | 0 | 1 | 0 | 1 | Single Output Readback. Readback input configuration data from second rank of latches onto Data Bus D [6:0] for the single output selected by the Output Address Bus A [4:0]. |
| 1 | 0 | 1 | 1 | 0 | Global Update. Copy input configuration data from all 17 first rank latches into second rank of latches, updating signal matrix connections for all outputs. |
| 1 | 0 | 0 | 1 | 0 | Transparent Write and Update. It is possible to write data directly onto rank two. This simplifies logic when synchronous signal matrix updating is not necessary. |

[1] X means don't care.

**Table 5. Address/Data Examples**

| Output Address Pins MSB–LSB | | | | | Enable Bit[1] | Input Address Pins MSB–LSB[1] | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A4 | A3 | A2 | A1 | A0 | D6/E | D5 | D4 | D3 | D2 | D1 | D0 | Function |
| 0 | 0 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 0 | 0 | Lower Address/Data Range. Connect Output 00 (A[4:0] = 00000) to Input 00 (D[5:0] = 000000). |
| 1 | 0 | 0 | 0 | 0 | X | 1 | 0 | 0 | 0 | 0 | 0 | Upper Address/Data Range. Connect Output 16 (A[4:0] = 10000) to Input 32 (D[5:0] = 100000). |
| Binary Output Number [2] | | | | | 1 | | Binary Input Number | | | | | Enable Output. Connect Selected Output (A[4:0] = 0 to 16) to Designated Input (D[5:0] = 0 to 32) and Enable Output (D6 = 1). |
| Binary Output Number[2] | | | | | 0 | X | X | X | X | X | X | Disable Output. Disable Specified Output (D6 = 0). |
| 1 | 0 | 0 | 0 | 1 | X | | Binary Input Number | | | | | Broadcast Connection. Connect all 17 outputs to same designated input and set all 17 enable bits to D6. Readback is not possible with the broadcast address. |
| 1 | 0 | 0 | 1 | 0 | X | 1 | 0 | 0 | 0 | 0 | 1 | Reserved. Any address or data code greater or equal to these are reserved for future expansion or factory testing. |

[1] X means don't care.
[2] The binary output number can also be the broadcast connection designator, 10001.

# CONTROL INTERFACE TIMING DIAGRAMS

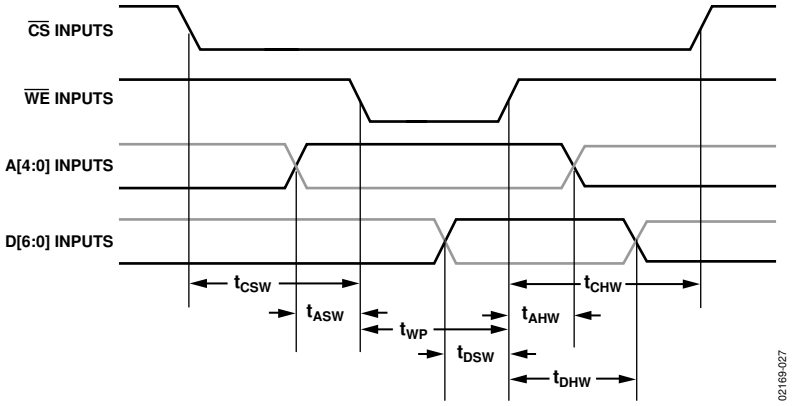


*Figure 27. First Rank Write Cycle*

**Table 6. First Rank Write Cycle**

| Parameter | Mnemonic | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Setup Time | $t_{CSW}$ | Chip select to write enable | $T_A$ = 25°C | 0 | | | ns |
| | $t_{ASW}$ | Address to write enable | $V_{DD}$ = 5 V | 0 | | | ns |
| | $t_{DSW}$ | Data to write enable | $V_{CC}$ = 3.3 V | 15 | | | ns |
| Hold Time | $t_{CHW}$ | Chip select from write enable | | 0 | | | ns |
| | $t_{AHW}$ | Address from write enable | | 0 | | | ns |
| | $t_{DHW}$ | Data from write enable | | 0 | | | ns |
| Enable Pulse | $t_{WP}$ | Width of write enable pulse | | 15 | | | ns |

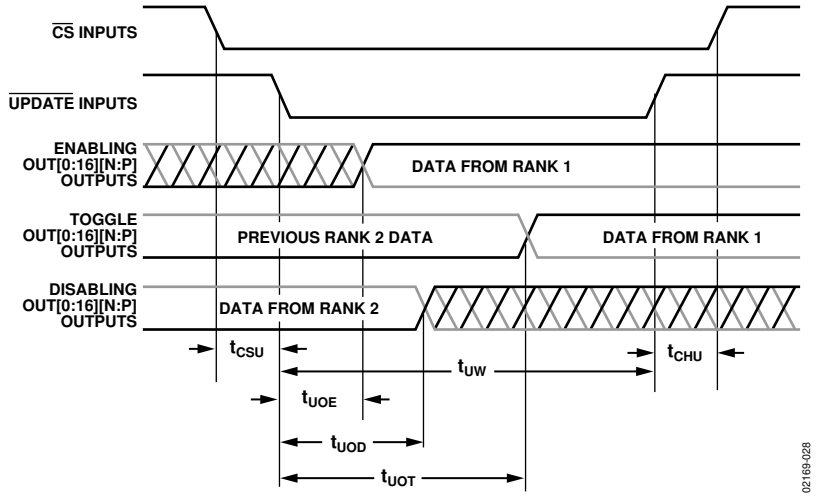


*Figure 28. Second Rank Update Cycle*

**Table 7. Second Rank Update Cycle**

| Parameter | Mnemonic | Function | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Setup Time | $t_{CSU}$ | Chip select to update | $T_A$ = 25°C | 0 | | | ns |
| Hold Time | $t_{CHU}$ | Chip select from update | $V_{DD}$ = 5 V | | | | ns |
| Output Enable Times | $t_{UOE}$ | Update to output enable | $V_{CC}$ = 3.3 V | | 25 | 40 | ns |
| Output Toggle Times | $t_{UOT}$ | Update to output reprogram | | | 25 | 40 | ns |
| Output Disable Times | $t_{UOD}$ | Update to output disabled | | | 25 | 30 | ns |
| Update Pulse | $t_{UW}$ | Width of update pulse | | 15 | | | ns |

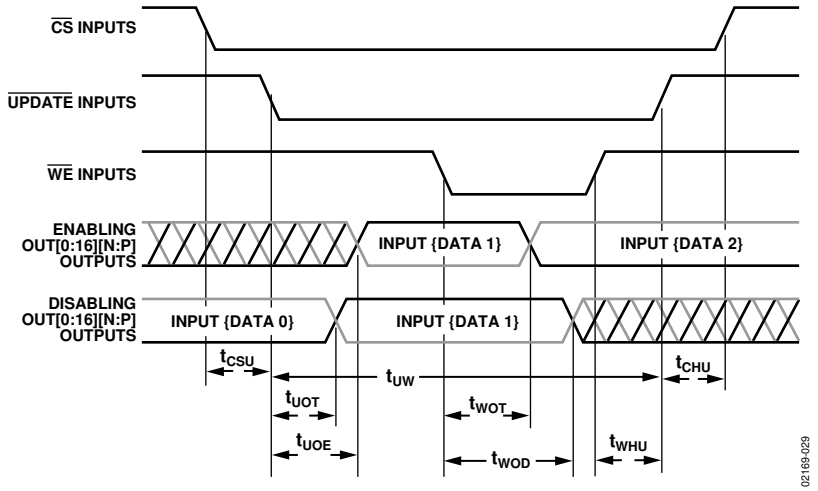


*Figure 29. First Rank Write Cycle and Second Rank Update Cycle*

**Table 8. First Rank Write Cycle and Second Rank Update Cycle**

| Parameter | Mnemonic | Function | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Setup Time | $t_{CSU}$ | Chip select to update | $T_A$ = 25°C | 0 | | | ns |
| Hold Time | $t_{CHU}$ | Chip select from update | $V_{DD}$ = 5 V | 0 | | | ns |
| Output Enable Times | $t_{UOE}$ | Update to output enable | $V_{CC}$ = 3.3 V | | 25 | 40 | ns |
| | $t_{WOE}$ | Write enable to output enable | | | 25 | 40 | ns |
| Output Toggle Times | $t_{UOT}$ | Update to output reprogram | | | 25 | 30 | ns |
| | $t_{WOT}$ | Write enable to output reprogram | | | 25 | 30 | ns |
| Output Disable Times | $t_{UOD}$[1] | Update to output disabled | | | 25 | 30 | ns |
| | $t_{WOD}$ | Write enable to output disabled | | | 25 | 30 | ns |
| Setup Time | $t_{WHU}$ | Write enable to update | | 10 | | | ns |
| Update Pulse | $t_{UW}$ | Width of update pulse | | 15 | | | ns |

[1] Not shown.

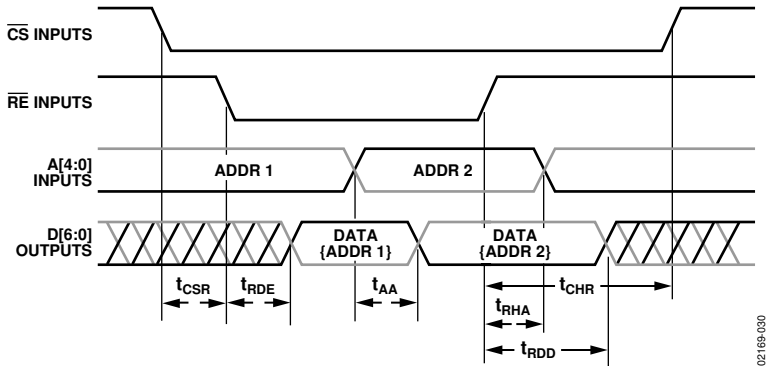


*Figure 30. Second Rank Readback Cycle*

**Table 9. Second Rank Readback Cycle**

| Parameter | Mnemonic | Function | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Setup Time | $t_{CSR}$ | Chip select to read enable | $T_A$ = 25°C | 0 | | | ns |
| Hold Time | $t_{CHR}$ | Chip select from read enable | $V_{DD}$ = 5 V | 0 | | | ns |
| Read Enable | $t_{RHA}$ | Address from read enable | $V_{CC}$ = 3.3 V | 5 | | | ns |
| Enable Time | $t_{RDE}$ | Data from read enable | 10 kΩ | | 15 | | ns |
| Access Time | $t_{AA}$ | Data from address | 20 pF on D[6:0] | | 15 | | ns |
| Release Time | $t_{RDD}$ | Data from read enable | Bus | | 15 | 30 | ns |

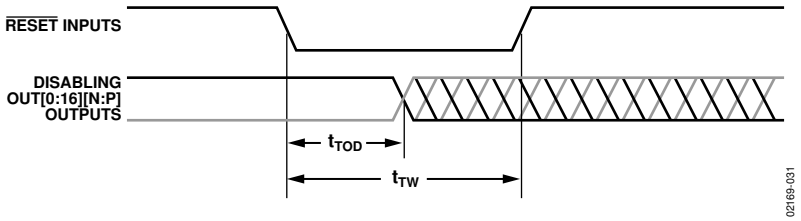


*Figure 31. Asynchronous Reset*

**Table 10. Asynchronous Reset**

| Parameter | Mnemonic | Function | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Disable Time | $t_{TOD}$ | Output disable from reset | $T_A$ = 25°C | | 25 | 30 | ns |
| Width of Reset Pulse | $t_{TW}$ | | $V_{DD}$ = 5 V | 15 | | | ns |
| | | | $V_{CC}$ = 3.3 V | | | | |

## CONTROL INTERFACE PROGRAMMING EXAMPLE

The following conservative pattern connects all outputs to Input 7, except Output 16, which is connected to Input 32. The vector clock period $t_0$ is 15 ns. It is possible to accelerate the execution of this pattern by deleting Vectors 1, 4, 7, and 9.

**Table 11. Basic Test Pattern**

| Vector No. | $\overline{\text{RESET}}$ | $\overline{\text{CS}}$ | $\overline{\text{WE}}$ | $\overline{\text{RE}}$ | $\overline{\text{UPDATE}}$ | A[4:0] | D[6:0] | Comments |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 | xxxxx | xxxxxxx | Disable all outputs |
| 1 | 1 | 1 | 1 | 1 | 1 | xxxxx | xxxxxxx | |
| 2 | 1 | 0 | 1 | 1 | 1 | 10001 | 1000111 | All outputs connected to Input 7 |
| 3 | 1 | 0 | 0 | 1 | 1 | 10001 | 1000111 | Write to first rank |
| 4 | 1 | 0 | 1 | 1 | 1 | 10001 | 1000111 | |
| 5 | 1 | 0 | 1 | 1 | 1 | 10000 | 1100000 | Connects Output 16 to Input 32 |
| 6 | 1 | 0 | 0 | 1 | 1 | 10000 | 1100000 | Write to first rank |
| 7 | 1 | 0 | 1 | 1 | 1 | 10000 | 1100000 | |
| 8 | 1 | 0 | 1 | 1 | 0 | xxxxx | xxxxxxx | Transfer to second rank |
| 9 | 1 | 0 | 1 | 1 | 1 | xxxxx | xxxxxxx | |
| 10 | 1 | 1 | 1 | 1 | 1 | xxxxx | xxxxxxx | Disable interface |

# CONTROL INTERFACE

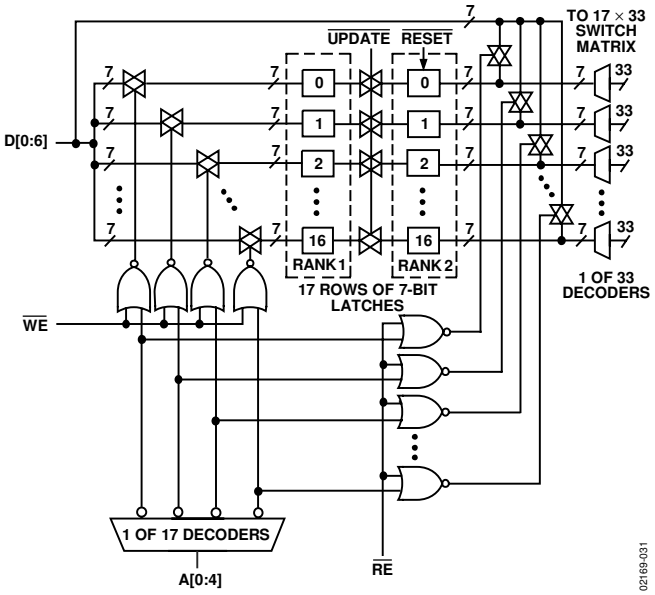


*Figure 32. Control Interface (Simplified Schematic)*

The AD8151 control interface receives and stores the desired connection matrix for the 33 input and 17 output signal pairs. The interface consists of 17 rows of double-rank 7-bit latches, 1 row for each output. The 7-bit data-word stored in each of these latches indicates to which (if any) of the 33 inputs the output is connected.

One output at a time can be preprogrammed by addressing the output and writing the desired connection data into the first rank of latches. This process can be repeated until each of the desired output changes has been preprogrammed. All output connections can then be programmed at once by passing the data from the first rank of latches into the second rank. The output connections always reflect the data programmed into the second rank of latches and do not change until the first rank of data is passed into the second rank.

If necessary for system verification, the data in the second rank of latches can be read back from the control interface.

At any time, a reset pulse can be applied to the control interface to globally reset the appropriate second rank data bits, disabling all 17 signal output pairs. This feature can be used to avoid output bus contention on system startup. The contents of the first rank remain unchanged.

The control interface pins are connected via logic-level translators. These translators allow programming and readback of the control interface using logic levels different from those in the signal matrix.

To facilitate multiple chip address decoding, there is a chip-select pin. All logic signals except the reset pulse are ignored unless the chip select pin is active. The chip select pin disables only the control logic interface and does not change the operation of the signal matrix. The chip select pin does not power down any of the latches, so any data programmed in the latches is preserved.

All control pins are level-sensitive, not edge-triggered.

## CONTROL PIN DESCRIPTION

### *A[4:0] Inputs*

Output address pins. The binary encoded address applied to these 5 input pins determines which one of the 17 outputs is being programmed (or being read back). The most significant bit (MSB) is A4.

### *D[6:0] Inputs/Outputs*

Input configuration data pins. In write mode, the binary encoded data applied to the D pins [6:0] determines which of 33 inputs is to be connected to the output specified with the A pins [4:0]. The MSB is D5 and the least significant bit (LSB) is D0. Bit D6 is the enable bit, setting the specified output signal pair to an enabled state if D6 is logic high or disabled to a high impedance state if D6 is logic low. In readback mode, the D pins [6:0] are low impedance outputs, indicating the data-word stored in the second rank for the output specified with the A pins [4:0]. The readback drivers are designed to drive high impedances only, so external drivers connected to the D pins [6:0] should be disabled during readback mode.

### *$\overline{\text{WE}}$ Input*

First Rank Write Enable. Forcing this pin to logic low allows the data on the D pins [6:0] to be stored in the first rank latch for the output specified by the A pins [4:0]. The $\overline{\text{WE}}$ pin must be returned to a logic high state after a write cycle to avoid overwriting the first rank data.

### *$\overline{\text{UPDATE}}$ Input*

Second Rank Write Enable. Forcing this pin to logic low allows the data stored in all 17 first rank latches to be transferred to the second rank latches. The signal connection matrix is reprogrammed when the second rank data is changed. This is a global pin, transferring all 17 rows of data at once. It is not necessary to program the address pins. It should be noted that after the initial power-up of the device, the first rank data is undefined. It may be desirable to preprogram all 17 outputs before performing the first update cycle.

### $\overline{RE}$ Input

Second Rank Read-Enable. Forcing this pin to logic low enables the output drivers on the bidirectional D pins [6:0], entering the readback mode of operation. By selecting an output address with the A pins [4:0] and forcing $\overline{RE}$ to logic low, the 7-bit data stored in the second rank latch for that output address is written to the D pins [6:0]. Data should not be written to the D pins [6:0] externally while in readback mode.

The $\overline{RE}$ and $\overline{WE}$ pins are not exclusive, and can be used at the same time, but data should not be written to the D pins [6:0] from external sources while in readback mode.

### $\overline{CS}$ Input

Chip-Select. This pin must be forced to logic low to program or receive data from the logic interface, with the exception of the $\overline{RESET}$ pin, described in the next section. This pin has no effect on the signal pairs and does not alter any of the stored control data.

### $\overline{RESET}$ Input

Global Output Disable Pin. Forcing the $\overline{RESET}$ pin to logic low resets the enable bit, D6, in all 17 second rank latches, regardless of the state of any of the other pins. This has the effect of immediately disabling the 17 output signal pairs in the matrix.

It is useful to momentarily hold $\overline{RESET}$ at a logic low state when powering up the AD8151 in a system that has multiple output signal pairs connected together. Failure to do this can result in several signal outputs contending after power-up. The $\overline{RESET}$ pin is not gated by the state of the chip-select pin, $\overline{CS}$. It should be noted that the $\overline{RESET}$ pin does not program the first rank, which contains undefined data after power-up.

## CONTROL INTERFACE TRANSLATORS

The AD8151 control interface has two supply pins, $V_{DD}$ and $V_{SS}$. The potential between the positive logic supply, $V_{DD}$, and the negative logic supply, $V_{SS}$, must be at least 3 V and no more than 5 V. Regardless of supply, the logic threshold is approximately 1.6 V above $V_{SS}$, allowing the interface to be used with most CMOS and TTL logic drivers. The signal matrix supplies, $V_{CC}$ and $V_{EE}$, can be set independently of the voltage on $V_{DD}$ and $V_{SS}$, with the constraints that $(V_{DD} - V_{EE}) \leq 10$ V. These constraints allow operation of the control interface on 3 V or 5 V, while the signal matrix is operated on 3.3 V or 5 V PECL or –3.3 V or –5 V ECL.

# CIRCUIT DESCRIPTION

The AD8151 is a high speed 33 × 17 differential crosspoint switch designed for data rates up to 3.2 Gbps per channel. The AD8151 supports PECL-compatible input and output levels when operated from a 5 V supply ($V_{CC}$ = 5 V, $V_{EE}$ = GND), or ECL-compatible levels when operated from a –5 V supply ($V_{CC}$ = GND, $V_{EE}$ = –5 V). To save power, the AD8151 can run from a +3.3 V supply to interface with low voltage PECL circuits or a –3.3 V supply to interface with low voltage ECL circuits. The AD8151 utilizes differential current-mode outputs with an individual disable control, which facilitates busing the outputs of multiple AD8151s together to assemble larger switch arrays. This feature also reduces system crosstalk and can greatly reduce power dissipation in a large switch array. A single external resistor programs the current for all enabled output stages, allowing user control over output levels with different output termination schemes and transmission line characteristic impedances.

### *High Speed Data Inputs (INxxP, INxxN)*

The AD8151 has 33 pairs of differential voltage-mode inputs. The common-mode input range extends from the positive supply voltage ($V_{CC}$) down to include standard ECL or PECL input levels ($V_{CC}$ – 2 V). The minimum differential input voltage is 200 mV. Unused inputs may be connected directly to any level within the allowed common-mode input range. A simplified schematic of the input circuit is shown in Figure 33.

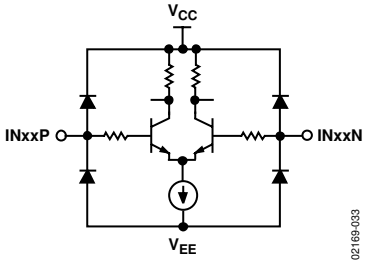


*Figure 33. Simplified Input Circuit*

To maintain signal fidelity at the high data rates supported by the AD8151, the input transmission lines should be terminated as close to the input pins as possible. The preferred input termination structure depends primarily on the application and the output circuit of the data source. Standard ECL components have open emitter outputs that require pull-down resistors. Three input termination networks suitable for this type of source are shown in Figure 34. The characteristic impedance of the transmission line is shown as $Z_O$. The resistors, R1 and R2, in the Thevenin termination are chosen to synthesize a $V_{TT}$ source with an output resistance of $Z_O$ and an open-circuit output voltage equal to $V_{CC}$ – 2 V. The load resistors (RL) in the differential termination scheme are needed to bias the emitter followers of the ECL source.

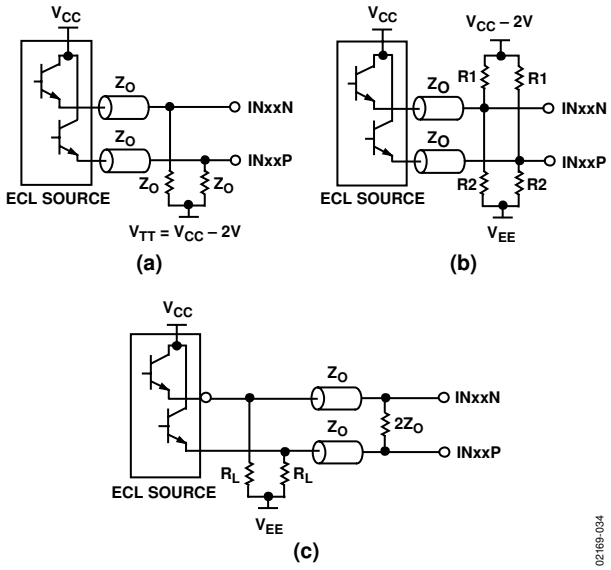


*Figure 34. AD8151 Input Termination from ECL/PECL Sources: (a) Parallel Termination Using $V_{TT}$ Supply, (b) Thevenin Equivalent Termination, and (c) Differential Termination*

If the AD8151 is driven from a current-mode output stage such as another AD8151, the input termination should be chosen to accommodate that type of source, as explained in the following section.

### *High speed Data Outputs (OUTyyP, OUTyyN)*

The AD8151 has 17 pairs of differential current-mode outputs. The output circuit, shown in Figure 35, is an open-collector NPN current switch with resistor-programmable tail current and output compliance extending from the positive supply voltage ($V_{CC}$) down to standard ECL or PECL output levels ($V_{CC}$ – 2 V). The outputs can be disabled individually to permit outputs from multiple AD8151s to be connected directly. Since the output currents of multiple enabled output stages sum when directly connected, care should be taken to ensure that the output compliance limit is not exceeded at any time by disabling the active output driver before enabling an inactive driver.

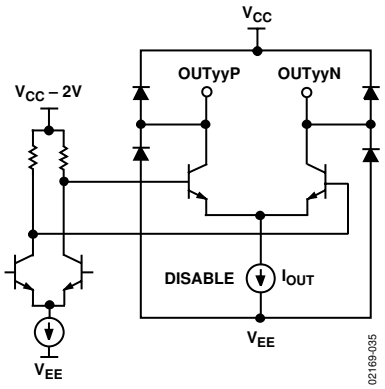


*Figure 35. Simplified Output Circuit*

To ensure proper operation, all outputs (including unused output) must be pulled high using external pull-up networks to a level within the output compliance range. If outputs from multiple AD8151s are wired together, a single pull-up network can be used for each output bus. The pull-up network should be chosen to keep the output voltage levels within the output compliance range at all times. Recommended pull-up networks to produce PECL/ECL 100 kΩ and 10 kΩ compatible outputs are shown in Figure 36. Alternatively, a separate supply can be used to provide $V_{COM}$, making $R_{COM}$ and $D_{COM}$ unnecessary.

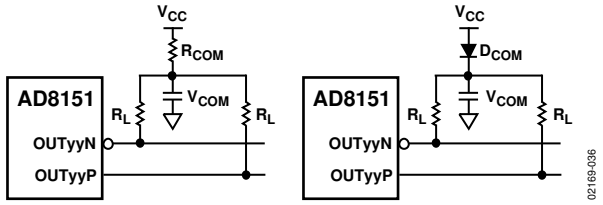


*Figure 36. Output Pull-Up Networks for PECL/ECL: a) 100 kΩ and b) 10kΩ*

The output levels are

$V_{OH} = V_{COM}$
$V_{OL} = V_{COM} - I_{OUT}R_L$
$V_{SWING} = V_{OH} - V_{OL} = I_{OUT}R_L$
$V_{COM} = V_{CC} - I_{OUT}R_{COM}$ (100 kΩ mode)
$V_{COM} = V_{CC} - V(D_{COM})$ (10 kΩ mode)

The common-mode adjustment element ($R_{COM}$ or $D_{COM}$) can be omitted if the input range of the receiver includes the positive supply voltage. The bypass capacitors reduce common-mode perturbations by providing an ac short from the common nodes ($V_{COM}$) to ground. When busing together the outputs of multiple AD8151s or when running at high data rates, double termination of its outputs is recommended to mitigate the impact of reflections due to open transmission line stubs and the lumped capacitance of the AD8151 output pins. A possible connection is shown in Figure 37; the bypass capacitors provide an ac short from the common nodes of the termination resistors to ground. To maintain signal fidelity at high data rates, the stubs connecting the output pins to the output transmission lines or load resistors should be as short as possible.

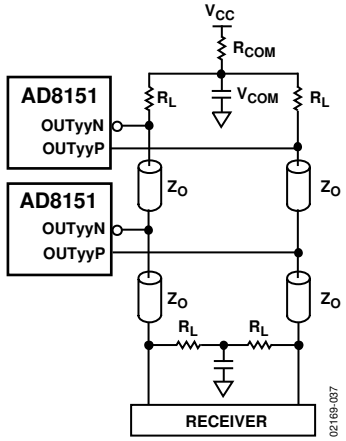


*Figure 37. Double Termination of AD8151 Outputs*

In this case, the output levels are

$V_{OH} = V_{COM} - (¼)I_{OUT}R_L$
$V_{OL} = V_{COM} - (¾)I_{OUT}R_L$
$V_{SWING} = V_{OH} - V_{OL} = (½)I_{OUT}R_L$

### Output Current Set Pin (REF)

A simplified schematic of the reference circuit is shown in Figure 38. A single external resistor connected between the REF pin and $V_{EE}$ determines the output current for all output stages. This feature allows a choice of pull-up networks and transmission line characteristic impedances while still achieving a nominal output swing of 800 mV. At low data rates, substantial power savings can be achieved by using lower output swings and higher load resistances.

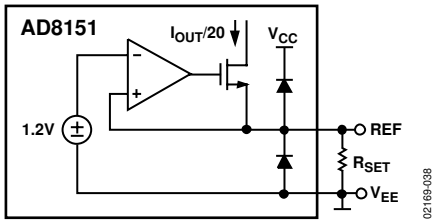


*Figure 38. Simplified Reference Circuit*

The nominal output current is given by the following:

$$I_{OUT} = 20\left(\frac{1.2\text{ V}}{R_{SET}}\right)$$

The minimum set resistor is $R_{SET, MIN}$ = 960 Ω resulting in $I_{OUT, MAX}$ = 25 mA. The maximum set resistor is $R_{SET, MAX}$ = 4.8 kΩ resulting in $I_{OUT, MIN}$ = 5 mA. Nominal 800 mV differential output swing can be achieved in a 50 Ω load using $R_{SET}$ = 1.5 kΩ ($I_{OUT}$ = 16 mA), or in a doubly terminated 75 Ω load using $R_{SET}$ = 1.13 kΩ ($I_{OUT}$ = 21.3 mA). To minimize stray capacitance and avoid the pickup of unwanted signals, the external set resistor should be located close to the REF pin. Bypassing the set resistor is not recommended.

### Power Supplies

There are several options for the power supply voltages for the AD8151, as there are two separate sections of the chip that require power supplies. These are the control logic and the high speed data paths. Depending on the system architecture, the voltage levels of these supplies can vary.

### Logic Supplies

The control (programming) logic is CMOS and is designed to interface with any of the standard single-ended logic families (CMOS or TTL). Its supply voltage pins are $V_{DD}$ (Pin 170, logic positive) and $V_{SS}$ (Pin 152, logic ground). In all cases the logic ground should be connected to the system digital ground. $V_{DD}$ should be supplied at between 3.3 V to 5 V to match the supply voltage of the logic family that is used to drive the logic inputs. $V_{DD}$ should be bypassed to ground with a 0.1 µF ceramic capacitor. The absolute maximum voltage from $V_{DD}$ to $V_{SS}$ is 5.5 V.

### Data Path Supplies

The data path supplies have more options for their voltage levels. The choices here affect several other areas, such as power dissipation, bypassing, and common-mode levels of the inputs and outputs. The more positive voltage supply for the data paths is $V_{CC}$ (Pin 41, Pin 98, Pin 149, and Pin 171). The more negative supply is $V_{EE}$, which appears on many pins that are not listed here. The maximum allowable voltage across these supplies is 5.5 V. The first choice in the data path power supplies is to decide whether to run the device as ECL or PECL. For ECL operation, $V_{CC}$ is at ground potential, while $V_{EE}$ is at a negative supply between –3.3 V to –5 V. This makes the common-mode voltage of the inputs and outputs a negative voltage (see Figure 39).

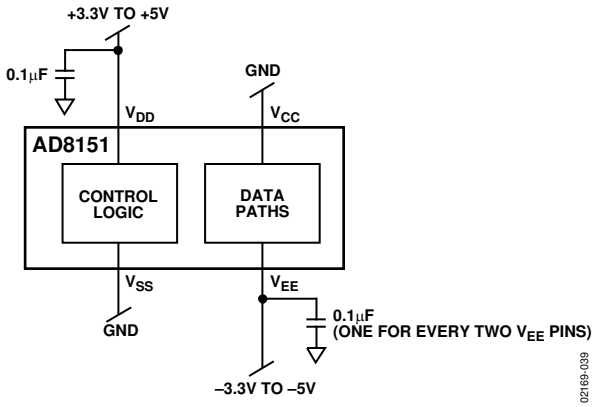


*Figure 39. Power Supplies and Bypassing for ECL Operation*

The proper way to run the device is to dc-couple the data paths to other ECL logic devices that use ground as the most positive supply and use a negative voltage for $V_{EE}$. However, if the part is to be ac-coupled, it is not necessary to have the input/output common mode at the same level as the other system circuits, but it is probably more convenient to use the same supply rails for all devices. For PECL operation, $V_{EE}$ is at ground potential and $V_{CC}$ is a positive voltage from 3.3 V to 5 V. Thus, the common mode of the inputs and outputs is at a positive voltage. These can then be dc-coupled to other PECL operated devices. If the data paths are ac-coupled, then the common-mode levels do not matter (see Figure 40).

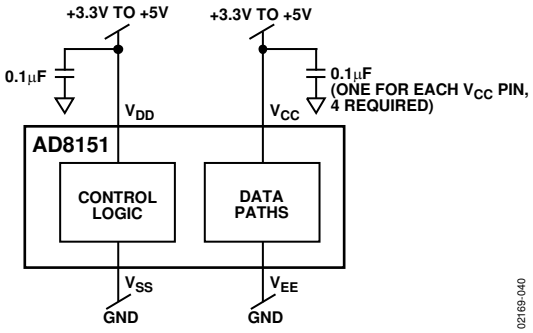


*Figure 40. Power Supplies and Bypassing for PECL Operation*

### POWER DISSIPATION

For analysis, the power dissipation of the AD8151 can be divided into three separate parts. These are the control logic, the data path circuits, and the (ECL or PECL) outputs, which are part of the data path circuits but can be dealt with separately. The control logic is CMOS technology and does not dissipate a significant amount of power. This power is, of course, greater when the logic supply is 5 V rather than 3 V, but overall it is not a significant amount of power and can be ignored for thermal analysis.

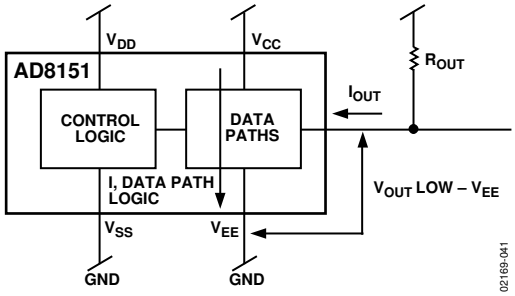


*Figure 41. Major Power Consumption Paths*

The data path circuits operate between the supplies $V_{CC}$ and $V_{EE}$. As described in the power supply section, this voltage can range from 3.3 V to 5 V. The current consumed by this section is constant, so operating at a lower voltage can decrease power dissipation by about 35 percent. The power dissipated in the data path outputs is affected by several factors. The first is whether the outputs are enabled or disabled. The worst case occurs when all of the outputs are enabled. The current consumed by the data path logic can be approximated by

$$I_{CC} = 35\ \text{mA} + [I_{OUT}/20\ \text{mA} \times 3\ \text{mA})] \times (\textit{no. of outputs enabled})$$

This equation states that a minimum $I_{CC}$ of 35 mA always flows. $I_{CC}$ increases by a factor that is proportional to both the number of enabled outputs and the programmed output current.

The power dissipated in this circuit section is simply the voltage of this section ($V_{CC} – V_{EE}$) times the current. To calculate the worst case, assume that $V_{CC} – V_{EE}$ is 5.0 V, all outputs are enabled, and the programmed output current is 25 mA. The power dissipated by the data path logic is

$$P = 5.0\ \text{V}\ \{35\ \text{mA} + [4.5\ \text{mA} + (25\ \text{mA}/20\ \text{mA} \times 3\ \text{mA})] \times 17\} = 876\ \text{mW}$$

The power dissipated by the output current depends on several factors. These are the programmed output current, the voltage drop from a logic low output to $V_{EE}$, and the number of enabled outputs. A simplifying assumption is that one of each (enabled) differential output pair is low and draws the full output current (and dissipates most of the power for that output), while the complementary output of the pair is high and draws insignificant current.

Thus, the power dissipation of the high output can be ignored and the output power dissipation for each output can be assumed to occur in a single static low output that sinks the full output programmed current. The voltage across which this current flows can also vary, depending on the output circuit design and the supplies that are used for the data path circuitry. In general, however, there is a voltage difference between a logic low signal and $V_{EE}$. This is the drop across which the output current flows. For a worst case, this voltage can be as high as 3.5 V. Thus, for all outputs enabled and the programmed output current set to 25 mA, the power dissipated by the outputs is

$$P = 3.5\text{ V } (25\text{ mA}) \times 17 = 1.49\text{ W}$$

### *Heat Sinking*

Depending on several factors in its operation, the AD8151 can dissipate upwards of 2 W or more. The part is designed to operate without the need for an explicit external heat sink. However, the package design offers enhanced heat removal via some of the package pins to the PC board traces. The $V_{EE}$ pins on the input sides of the package (Pin 1 to Pin 46 and Pin 93 to Pin 138) have finger extensions inside the package that connect to the paddle upon which the IC chip is mounted. These pins provide a lower thermal resistance from the IC to the $V_{EE}$ pins than other pins that just have a bond wire. As a result, these pins can be used to enhance the heat removal process from the IC to the circuit board and ultimately to the ambient. The $V_{EE}$ pins described earlier should be connected to a large area of circuit board trace material to take the most advantage of their lower thermal resistance. If there is a large area available on an inner layer that is at $V_{EE}$ potential, then vias can be provided from the package pin traces to this layer.

There should be no thermal-relief pattern when connecting the vias to the inner layers for these $V_{EE}$ pins. Additional vias in parallel and close to the pin leads can provide an even lower thermal resistive path. If possible, use 2 oz copper foil to provide better heat removal than 1 oz copper foil. The AD8151 package has a specified thermal impedance $\theta_{JA}$ of 30°C/W. This is the worst case still-air value that can be expected when the circuit board does not significantly enhance the heat removal from the package. By using the concept described earlier or by using forced-air circulation, the thermal impedance can be lowered.

For an extreme worst case analysis, the junction temperature increase above the ambient can be calculated assuming 2 W of power dissipation and a $\theta_{JA}$ of 30°C/W to yield a 60°C rise above the ambient. There are many techniques described earlier that can mitigate this situation. Most actual circuits do not result in this high an increase of the junction temperature above the ambient.

# APPLICATIONS

## INPUT AND OUTPUT BUSING

Although the AD8151 is a digital part, in any application that runs at high speed, analog design details have to be given very careful consideration. At high data rates, the design of the signal channels have a strong influence on data integrity and its associated jitter and ultimately bit error rate (BER).

While it might be considered very helpful to have a suggested circuit board layout for any particular system configuration, this is not something that can be practically realized. Systems come in all shapes, sizes, speeds, performance criteria, and cost constraints. Therefore, some general design guidelines are presented that can be used for all systems and judiciously modified where appropriate.

High speed signals travel best, that is, they maintain their integrity when they are carried by a uniform transmission line that is properly terminated at either end. Any abrupt mismatches in impedance or improper termination creates reflections that add to or subtract from parts of the desired signal. Small amounts of this effect are unavoidable, but too much distorts the signal to the point that the channel BER increases. It is difficult to fully quantify these effects because they are influenced by many factors in the overall system design.

A constant-impedance transmission line is characterized by having a uniform cross-section profile over its entire length. In particular, there should be no stubs, which are branches that intersect the main run of the transmission line. These can have an electrical appearance that is approximated by a lumped element, such as a capacitor, or if long enough, by another transmission line. If stubs are unavoidable in a design, their effect can be minimized by making them as short as possible and as high an impedance as possible.

Figure 37 shows a differential transmission line that connects two differential outputs from the AD8151 to a generic receiver. A more generalized system can have more outputs bused and more receivers on the same bus, but the same concepts apply. The inputs of the AD8151 can also be considered as a receiver. The transmission lines that bus the devices together are shown with terminations at each end.

The individual outputs of the AD8151 are stubs that intersect the main transmission line. Ideally, their current source outputs would be infinite impedance, and they would have no effect on signals that propagate along the transmission line. In reality, each external pin of the AD8151 projects into the package and has a bond wire connected to the chip inside. On-chip wiring then connects to the collectors of the output transistors and to ESD protection diodes.

Unlike some other high speed digital components, the AD8151 does not have on-chip terminations. While this location would be closer to the actual end of the transmission line for some architectures, this concept can limit system design options. In particular, it is not possible to bus more than two inputs or outputs on the same transmission line and it is also not possible to change the value of these terminations to use for different impedance transmission lines. The AD8151, with the added ability to disable its outputs, is much more versatile in these types of architectures.

If the external traces are kept to a bare minimum, then the output presents a mostly lumped capacitive load of about 2 pF. A single stub of 2 pF does not adversely affect signal integrity to a large extent for most transmission lines, but the more of these stubs, the greater their adverse influence.

One way to mitigate this effect is to locally reduce the capacitance of the main transmission line near the point of stub intersection. Some practical means for doing this are to narrow the PC board traces in the region of the stub and/or to remove some of the ground plane(s) near this intersection. The effect of these techniques is to locally lower the capacitance of the main transmission line at these points, while the added capacitance of the AD8151 outputs compensate for this reduction in capacitance. The overall intent is to create as uniform a transmission line as possible.

In selecting the location of the termination resistors, it is important to keep in mind that, as their name implies, they should be placed at either end of the line. There should be minimal or no projection of the transmission line beyond the point where it connects to the termination resistors.

## EVALUATION BOARD

An evaluation board has been designed and is available to rapidly test the main features of the AD8151. This board allows the user to analyze the analog performance of the AD8151 channels and easily control the configuration of the board with a PC. The board has limited numbers of differential input/output pairs. Each differential pair of microstrips is connected to either top mount or side launch SMA connectors. The top mount SMA connectors are drilled and stubbed for superior performance. The FR4 type board contains a total of nine outputs (all even numbered outputs) and 20 inputs (0, 2, 4, 6, 8, 10, 12, 13, 14, 15, 16, 17, 18, 20, 22, 24, 26, 28, 30, 32). It is important to note that the shells of the SMA connectors are attached to $V_{CC}$. This makes only ECL or negative level swings possible during testing.

## POWER SUPPLIES

The AD8151 is designed to work with standard ECL logic levels. This means that $V_{CC}$ is at ground and $V_{EE}$ is at a negative supply. The shells of the I/O SMA connectors are at $V_{CC}$ potential. Thus, when operating in the standard ECL configuration, test equipment can be directly connected to the board, since the test equipment also has its connector shells at ground potential.

Operating in PECL mode requires $V_{CC}$ to be at a positive voltage while $V_{EE}$ is at ground. Since this generates a positive voltage at the shells of the I/O connectors, it can cause problems when directly connecting to test equipment. Some equipment, such as battery-operated oscilloscopes, can be floated from ground, but care should be taken with line-powered equipment to avoid creating a dangerous situation. Refer to the manual of the test equipment that is being used.

The voltage difference from $V_{CC}$ to $V_{EE}$ can range from 3 V to 5 V. Power savings can be realized by operating at a lower voltage without any compromise in performance.

A separate connection is provided for $V_{TT}$, the termination potential of the outputs. This can be at a voltage as high as $V_{CC}$, but power savings can be realized if $V_{TT}$ is at a voltage that is somewhat lower.

As a practical matter, current on the evaluation board flows from the $V_{TT}$ supply through the termination resistors into the multiple outputs of the AD8151 and to the $V_{EE}$ supply. When running in ECL mode, $V_{TT}$ should be at a negative supply.

Most power supplies do not allow a simultaneous ground connection to $V_{CC}$ and a negative supply at $V_{TT}$, because it would force the source current to originate from a negative supply, which wants to flow to the more-negative $V_{EE}$. In this case, the source current does not then return to the ground terminal of the $V_{TT}$ supply. Thus, $V_{TT}$ should be referenced to $V_{EE}$ when running in ECL mode or a true bipolar supply should be used.

The digital supply is provided to the AD8151 by the $V_{DD}$ and $V_{SS}$ pins. $V_{SS}$ should always be at ground potential to make it compatible with standard CMOS or TTL logic. $V_{DD}$ can range from 3 V to 5 V, and should be matched to the supply voltage of the logic used to control the AD8151. However, since PCs use 5 V logic on their parallel port, $V_{DD}$ should be 5 V when using a PC to program the AD8151.

### *Bypassing*

Most of the board's bypass capacitors are opposite the DUT on the solder side and are connected between $V_{CC}$ and $V_{EE}$. This is where they are most effective. For low inductance, use 0.01 µF ceramic chip capacitors.

There are additional higher value capacitors elsewhere on the board for bypassing at lower frequencies. The location of these capacitors is not as critical.

### *Input and Output Considerations*

Each input contains a 100 Ω differential termination. Although differential termination eases board layout due to its compact nature, it can cause problems with the driving generator. A typical pulse or pattern generator wants to see 50 Ω to ground (or to –2 V in some cases). High speed probing of the input has shown that if this type of termination is not present, input amplitudes can be slightly off. The dc input levels can be even more affected. Depending on the generator used, these levels can be off as much as 800 mV in either direction. A correction for this problem is to attach a 6 dB attenuator to each P and N input. Because the AD8151 has a large common-mode voltage range on its input stage, it is not significantly affected by dc level errors.

On this evaluation board, all unused inputs are tied to $V_{CC}$ (GND). All outputs, whether attached to connectors or not, are tied to $V_{TT}$ through a 49.9 Ω resistor. The AD8151 device is on the component side of the board, while input terminations and output back terminations are on the circuit side. The input signals from the circuit side transit through via holes to the DUT's pads. The component-side output signals connect to via holes and to circuit-side 49.9 Ω termination resistors.

### *Board Construction*

For this board, FR4 material was chosen over more exotic board materials. Tests show exotic materials are unnecessary. This is a 4-layer board, so power is bused on both external and internal layers. Test structures show microstrip performance is unaffected by the dc bias levels on the plane beneath it.

The board manufacturing process should ensure a controlled impedance board. The board stack consists of a 5-mil-thick layer between external and internal layers. This allows the use of an 8-mil-wide microstrip trace running from the SMA connector to the DUT's pads. The narrow trace eliminates the need to reduce the trace width as the DUT's pads are approached and helps to control the microstrip trace impedance. The thin 5-mil dielectric also reduces crosstalk by confining the electromagnetic fields between the trace and the plane below.